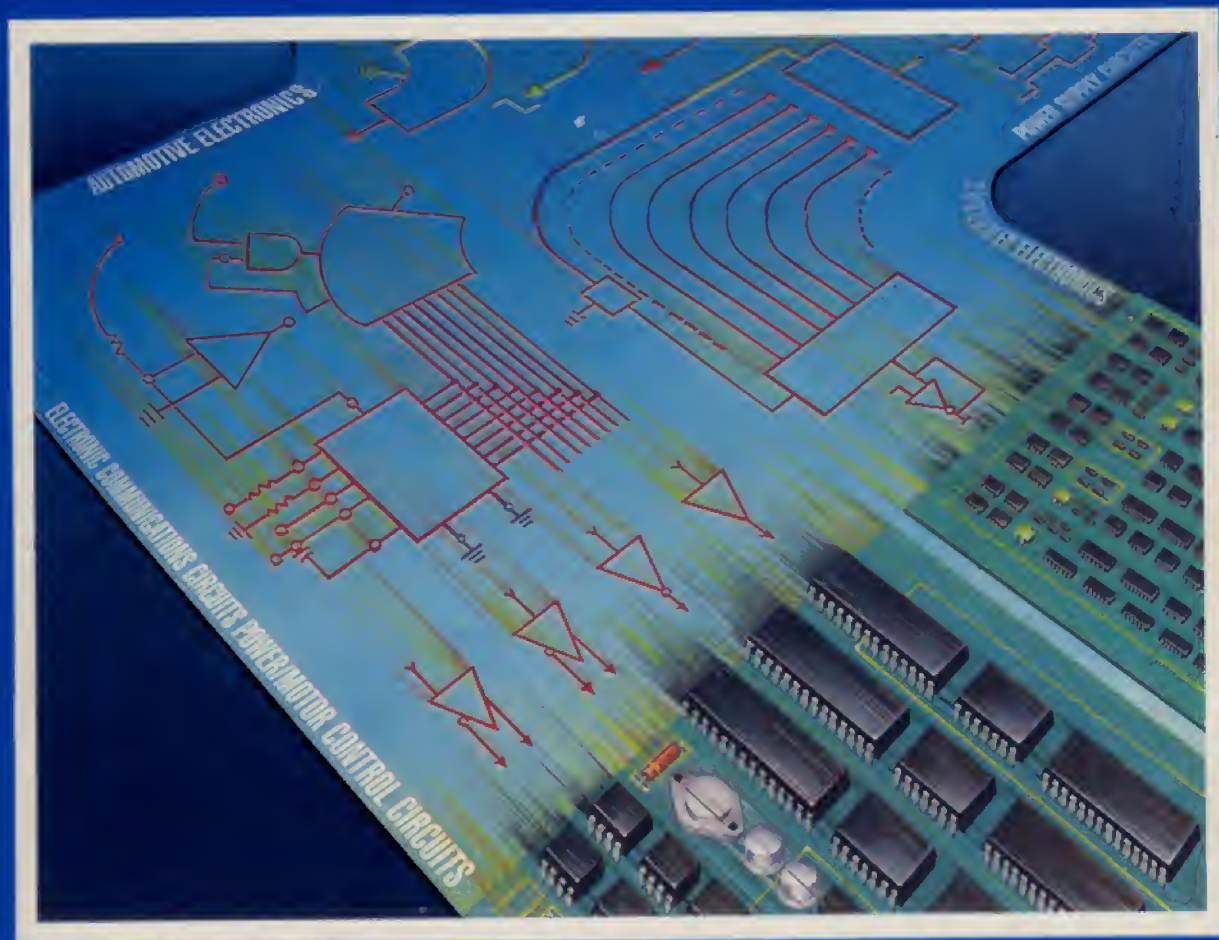




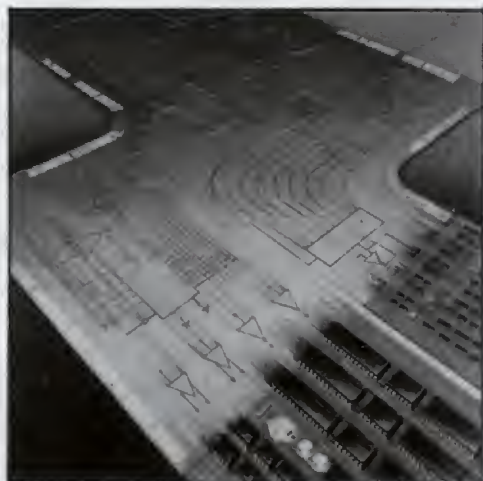
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MOTOROLA LINEAR AND INTERFACE ICS



LINEAR AND INTERFACE INTEGRATED CIRCUITS



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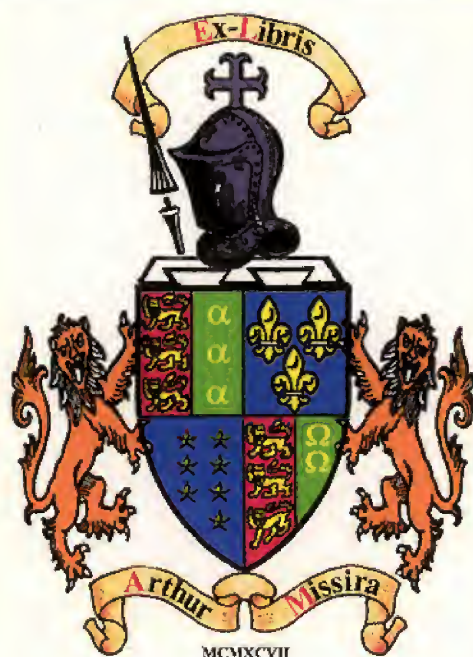
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AN1003	AN1077
AN1004	AN1078
AN1006	AN1081
AN1019	ANE424
AN1044	SG98 Rev. 4

*See Telecommunication Device Data (DL136 Rev.2)



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LINEAR AND INTERFACE INTEGRATED CIRCUITS

This publication presents technical information for the broad line of Linear and Interface Integrated Circuit products. Complete device specifications are provided in the form of **Data Sheets** which are categorized by product type into ten chapters for easy reference. **Selector Guides** by product family are provided in the beginning of each Chapter to enable quick comparisons of performance characteristics. A **Cross Reference** chapter lists Motorola direct replacement and functional equivalent part numbers for other industry products.

A chapter is provided to illustrate **Package Outline** and mounting hardware drawings, and includes information on Surface Mount Devices (SMD), and Industry Package Cross Reference Guide.

Additionally, chapters are provided with information on **Quality** program concepts, high-reliability processing, and abstracts of available **Technical Literature**.

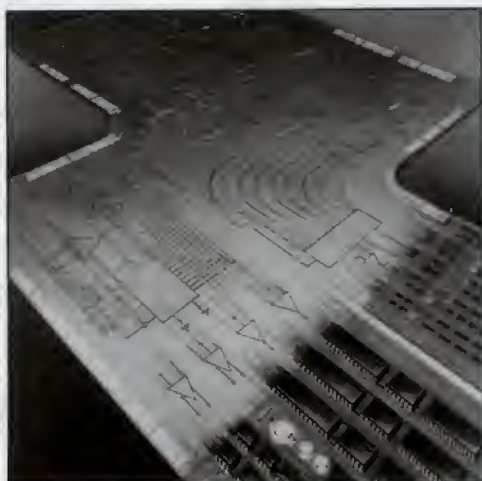
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Index/Cross Reference

In Brief . . .

In the Cross Reference Section of this chapter, a complete interchangeability list linking over 3000 devices is offered by most major Linear Integrated Circuits manufacturers to the nearest equivalent Motorola device. The "Motorola Direct Replacement" column lists devices with identical pin connections and package and the same or better electrical characteristics and temperature range. The "Motorola Similar Replacement" column provides a device which performs the same function but with possible differences in package configurations, pin connections, temperature range or electrical specifications.

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NOTE: All "Motorola Direct Replacement" devices which have part numbers identical to the "Part Number" being searched for are not included in this Cross Reference table. Please refer to the Alphanumeric Index on pages 1-1 to 1-6.

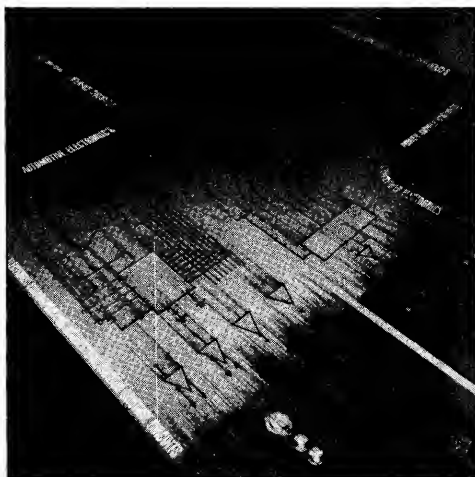
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Amplifiers and Comparators

2

In Brief . . .

For over two decades, Motorola has continually refined and updated integrated circuit technologies, analog circuit design techniques and processes in response to the ever-expanding needs of the market place. The enhanced performance of present day operational amplifiers and comparators have come into being through innovative application of these technologies, designs and processes. Some early designs, though of inferior performance by today's standards, are still available but are rapidly giving way to the new, higher performance operational amplifier and comparator circuits. Motorola has pioneered in JFET inputs, low temperature coefficient input stages, Miller loop compensation, all NPN output stages, dual-doublet frequency compensation and analog "in-the-package" trimming of resistors to produce superior high performance operational amplifiers and comparators, operating in many cases from a single supply, with low input offset, low noise, low power, high output swing, high slew rate and high gain-bandwidth product at reasonable cost to the customer.

Present day operational amplifiers and comparators find application in all segments of society to include motor controls, instrumentation, aerospace, automotive, telecommunication, medical and consumer products.

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Amplifiers and Comparators

Operational Amplifiers

Motorola offers a broad line of bipolar operational amplifiers to meet a wide range of applications. From low-cost industry-standard types to high precision circuits, the span encompasses a large range of performance capabilities. These linear integrated circuits are available as single, dual, and quad monolithic devices

in a variety of temperature ranges and package styles. Most devices may be obtained in unencapsulated "chip" form as well. For price and delivery information on chips, please contact your Motorola Sales Representative or Distributor.

Single Operational Amplifiers

Device	I _B μA Max	V _{IO} mV Max	TCV _{IO} μV/°C Typ	I _O nA Max	A _{vol} V/mV Min	BW (A _v = 1) MHz Typ	SR (A _v = 1) V/μs Typ	Supply Voltage V Min Max		Description	Package Suffix
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Noncompensated

Commercial Temperature Range (0°C to +70°C)

LM301A	0.25	7.5	10	50	25	1.0	0.5	±3.0	±18	General Purpose	H, N/626, J/693
LM308	7.0	7.5	15	1.0	25	1.0	0.3	±3.0	±18	Precision	H, N/626
LM308A	7.0	0.5	5.0	1.0	80	1.0	0.3	±3.0	±18	Precision	H, N/626
MC1439	1.0	7.5	15	100	15	2.0	4.2	±6.0	±18	High Slew Rate	G/601, P1
MC1709C	1.5	7.5	15	500	15	1.0	0.3	±3.0	±18	General Purpose	G/601, P1, U
MC1748C	0.5	6.0	15	200	20	1.0	0.5	±3.0	±18	General Purpose	G/601, P1, U

Industrial Temperature Range (–25°C to +85°C)

LM201A	0.075	2.0	10	10	50	1.0	0.5	±3.0	±22	General Purpose	H, N/626, J/693
LM208	0.002	2.0	3.0	0.2	50	1.0	0.3	±3.0	±20	Precision	H, N/626, J/632, J-8
LM208A	0.002	0.5	1.0	0.2	80	1.0	0.3	±3.0	±20	Precision	H, N/626, J/632, J-8

Military Temperature Range (–55°C to +125°C)

LM101A	0.075	2.0	10	10	50	1.0	0.5	±3.0	±22	General Purpose	H, J/693
LM108	0.002	2.0	3.0	0.2	50	1.0	0.3	±3.0	±20	Precision	H, J, J-8/693
LM108A	0.002	0.5	1.0	0.2	80	1.0	0.3	±3.0	±20	Precision	H, J, J-8/693
MC1539	0.5	3.0	15	60	50	2.0	4.2	±4.0	±18	High Slew Rate	G/601
MC1709	0.5	5.0	15	200	25	1.0	0.3	±3.0	±18	General Purpose	G/601, U
MC1709A	0.6	3.0	5.0	100	25	1.0	0.5	±3.0	±18	High Performance	G/601
MC1748	0.5	5.0	15	200	50	1.0	0.5	±3.0	±22	General Purpose	G/601, U

Device	I _{IB} μA Max	V _{IO} mV Max	TC _{VIO} μV/°C Typ	I _{IO} nA Max	A _{Vol} V/mV Min	BW (A _V = 1) MHz Typ	SR (A _V = 1) V/μs Typ	Supply Voltage V Min Max		Description	Package Suffix
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Internally Compensated**Commercial Temperature Range (0°C to +70°C)**

LF351	200 pA	10	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	N/626
LF355	200 pA	10	5.0	50 pA	50	1.0	5.0	±5.0	±18	JFET Input	H/601, J/693
LF355B	100 pA	5.0	5.0	20 pA	50	2.5	5.0	±5.0	±22	JFET Input	H/601, J/693
LF356	200 pA	10	5.0	50 pA	50	2.0	15	±5.0	±18	JFET Input	H/601, J/693
LF356B	100 pA	5.0	5.0	20 pA	50	5.0	12	±5.0	±22	JFET Input	H/601, J/693
LF357	200 pA	10	5.0	50 pA	50	3.0	75	±5.0	±18	Wideband FET Input	H/601, J/693
LF357B	100 pA	5.0	5.0	20 pA	50	20	50	±5.0	±22	JFET Input	H/601, J/693
LF441C	100 pA	5.0	10	50 pA	25	2.0	6.0	±5.0	±18	Low Power JFET Input	N/626
LM11C	100 pA	0.6	2.0	10 pA	250	1.0	0.3	±3.0	±20	Precision	H, N/626, J/632, J-8/693
LM11CL	200 pA	5.0	3.0	25 pA	50	1.0	0.3	±3.0	±20	Precision	H, N/626, J/632, J-8/693
LM307	0.25	7.5	10	50	25	1.0	0.5	±3.0	±18	General Purpose	N/626
MC1436	0.04	10	12	10	70	1.0	2.0	±15	±34	High Voltage	G/601, U
MC1456	0.03	10	12	10	70	1.0	2.5	±3.0	±18	High Performance	G/601, P1, U
MC1733C	30	—	—	5.0 μA	80	90	—	±4.0	±8.0	Differential Wideband Video Amp	G/601, L, P/646
MC1741C	0.5	6.0	15	200	20	1.0	0.5	±3.0	±18	General Purpose	G/601, P1, U
MC1741SC	0.5	6.0	15	200	20	1.0	10	±3.0	±18	High Slew Rate	G/601, P1
MC1776C	0.003	6.0	15	3.0	100	1.0	0.2	±1.2	±18	μPower, Programmable	G/601, P1, U
MC3476	0.05	6.0	15	25	50	1.0	0.2	±1.5	±18	Low Cost	G/601, P1, U
MC34001	200 pA	10	10	100 pA	25	4.0	13	±5.0	±18	μPower, Programmable	G/601, P/626, U
MC34001B	200 pA	5.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	G/601, P/626, U
MC34071	0.5	5.0	10	75	25	4.5	10	+3.0	+44	High Performance, Single Supply	P/626, U
MC34071A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	Single Supply	P/626, U
MC34080	200 pA	1.0	10	100 pA	25	16	55	±5.0	±22	Decompensated	P/626, U
MC34080A	200 pA	0.5	10	100 pA	50	16	55	±5.0	±22	MC34081 for A _V ≥ 2	P/626, U
MC34081	200 pA	1.0	10	100 pA	25	8.0	30	±5.0	±22	High Speed, JFET Input	P/626, U
MC34081A	200 pA	0.5	10	100 pA	50	8.0	30	±5.0	±22	High Speed, JFET Input	P/626, U
MC34181	0.1 nA	2.0	10	0.05	25	4.0	10	±2.5	±18	Low Power JFET Input	P/626
OP-27F	0.055	0.06	0.3	50	1000	8.0	2.8	±4.0	±22	Low Noise, Precision	P/626
OP-27G	0.08	0.1	0.4	75	700	8.0	2.8	±4.0	±22	Low Noise, Precision	P/626
TL061AC	200 pA	6.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power JFET Input	P/626
TL061C	200 pA	15	10	200 pA	4.0	2.0	6.0	±2.5	±18	Low Power JFET Input	P/626
TL071AC	200 pA	6.0	10	50 pA	50	4.0	13	±5.0	±18	Low Noise, JFET Input	P/626, JG
TL071C	200 pA	10	10	50 pA	25	4.0	13	±5.0	±18	Low Noise, JFET Input	P/626, JG
TL081AC	200 pA	6.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	P/626, JG
TL081C	400 pA	15	10	200 pA	25	4.0	13	±5.0	±18	JFET Input	P/626, JG

Industrial Temperature Range (−25°C to +85°C)

OP-27F	0.055	0.06	0.3	50	1000	8.0	2.8	±4.0	±22	Low Noise, Precision	Z
OP-27G	0.08	0.1	0.4	75	700	8.0	2.8	±4.0	±22	Low Noise, Precision	Z

Automotive Temperature Range (−40°C to +85°C)

MC33071	0.5	5.0	10	75	25	4.5	10	+3.0	+44	High Performance, Single Supply	P/626, U
MC33071A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	Single Supply	P/626, U
MC33171	0.1	4.5	10	20	50	1.8	2.1	+3.0	+44	Low Power, Single Supply	P/626
MC33181	0.1 nA	2.0	10	0.05	25	4.0	10	±2.5	±18	Low Power JFET Input	P/626
TL061V	200 pA	6.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power JFET Input	P/626

OPERATIONAL AMPLIFIERS (continued)

Device	I _B μ A Max	V _{IO} mV Max	TCV _{IO} μ V/°C Typ	I _O nA Max	A _{vol} V/mV Min	BW (A _v = 1) MHz Typ	SR (A _v = 1) V/ μ s Typ	Supply Voltage V Min Max		Description	Package Suffix
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Internally Compensated

Military Temperature Range (–55°C to +125°C)

MC1536	0.02	5.0	10	3.0	100	1.0	2.0	±15	±40	High Voltage	G/601, U
MC1556	0.015	4.0	10	2.0	100	1.0	2.5	±3.0	±22	High Performance	G/601, 693/U
MC1733	0.2	—	—	3.0 μ A	90	90	—	±4.0	±8.0	Differential Wideband Video Amp	G/603, L
MC1741	0.5	5.0	15	200	50	1.0	0.5	±3.0	±22	General Purpose	G/601, U
MC1741S	0.5	5.0	15	200	50	1.0	10	±3.0	±22	High Slew Rate	G/601, U
MC1776	0.0075	5.0	15	3.0	200	1.0	0.2	±1.2	±18	μ Power, Programmable	G/601, L
MC35001	100 pA	10	10	100 pA	25	4.0	13	±5.0	±22	JFET Input	G/601, U
MC35001B	100 pA	5.0	10	50 pA	50	4.0	13	±5.0	±22	JFET Input	G/601, U
MC35071	0.5	5.0	10	75	25	4.5	10	+3.0	+44	High Performance,	U
MC35071A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	Single Supply	U
MC35080	200 pA	1.0	10	100 pA	25	16	55	±5.0	±22	Decompensated	U
MC35080A	200 pA	0.5	10	100 pA	50	16	55	±5.0	±22	MC35081 for A _v ≥ 2	U
MC35081	200 pA	1.0	10	100 pA	25	8.0	30	±5.0	±22	High Speed, JFET Input	U
MC35081A	200 pA	0.5	10	100 pA	50	8.0	30	±5.0	±22	High Speed, JFET Input	U
MC35171	0.1	4.5	10	20	50	1.8	2.1	+3.0	+44	Low Power, Single Supply	U
MC35181	0.1 nA	2.0	10	0.05	25	4.0	10	±2.5	±18	Low Power JFET Input	U
OP-27B	0.055	0.06	0.3	50	1000	8.0	2.8	±4.0	±22	Low Noise, Precision	Z
OP-27C	0.08	0.1	0.4	75	700	8.0	2.8	±4.0	±22	Low Noise, Precision	Z
TL061M	200 pA	6.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power JFET Input	JG
TL081M	200 pA	9.0	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	JG

Dual Operational Amplifiers

Device	I _B μ A Max	V _{IO} mV Max	TCV _{IO} μ V/°C Typ	I _O nA Max	A _{vol} V/mV Min	BW (A _v = 1) MHz Typ	SR (A _v = 1) V/ μ s Typ	Supply Voltage V Min Max		Description	Package Suffix
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Noncompensated

Commercial Temperature Range (0°C to +70°C)

MC1437	1.5	7.5	10	500	15	1.0	0.25	±3.0	±18	Dual MC1709	L, P/646
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Military Temperature Range (–55°C to +125°C)

MC1537	0.5	5.0	10	200	25	1.0	0.25	±3.0	±18	Dual MC1709	L
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Internally Compensated

Commercial Temperature Range (0°C to +70°C)

LF353	200 pA	10	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	N/626
LF442C	100 pA	5.0	10	50 pA	25	2.0	6.0	±5.0	±18	Low Power JFET Input	N/626
LM358	0.25	6.0	7.0	50	25	1.0	0.6	±1.5	±18	Single Supply (Low Power Consumption)	H, N/626, J/693
LM833	1.0	5.0	2.0	200	31.6	15	7.0	±2.5	±18	Dual, Low Noise, Audio	N/626
MC1458	0.5	6.0	10	200	20	1.1	0.8	±3.0	±18	Dual MC1741	G/601, P1, U
MC1458C	0.7	10	10	300	20	1.1	0.8	±3.0	±18	Dual General Purpose	G/601, P1
MC1458S	0.5	6.0	10	200	20	1.0	10	±3.0	±18	High Slew Rate	G/601, P1, U
MC1747C	0.5	6.0	10	200	25	1.0	0.5	±3.0	±18	Dual MC1741	G/603, L, P2
MC3458	0.5	10	7.0	50	20	1.0	0.6	±1.5	±18	Split Supplies	G/601, P1, U
								+3.0	+36	Single Supply (Low Crossover Distortion)	

OPERATIONAL AMPLIFIERS (continued)

Device	I _B μA Max	V _{IO} mV Max	TCV _{IO} μV/°C Typ	I _O nA Max	A _{Vol} V/mV Min	BW (A _V = 1) MHz Typ	SR (A _V = 1) V/μs Typ	Supply Voltage V Min Max		Description	Package Suffix
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Commercial Temperature Range (0°C to +70°C) (continued)

MC4558AC	0.5	5.0	10	200	50	2.8	1.6	±3.0	±22	High Frequency	P1
MC4558C	0.5	6.0	10	200	20	2.8	1.6	±3.0	±18	High Frequency	G/601, P1, U
MC34002	100 pA	10	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	G/601, P/626, U
MC34002B	100 pA	5.0	10	70 pA	25	4.0	13	±5.0	±18	JFET Input	G/601, P/626, U
MC34072	0.5	5.0	10	75	25	4.5	10	+3.0	+44	High Performance,	P/626, U
MC34072A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	Single Supply	P/626, U
MC34082	200 pA	3.0	10	100 pA	25	8.0	30	±5.0	±22	High Speed, JFET Input	P/626, U
MC34082A	200 pA	1.0	10	100 pA	50	8.0	30	±5.0	±22	High Speed, JFET Input	P/626, U
MC34083	200 pA	3.0	10	100 pA	25	16	55	±5.0	±22	Decompensated	P/626, U
MC34083A	200 pA	1.0	10	100 pA	50	16	55	±5.0	±22	MC34082 for A _V ≥ 2	P/626, U
MC34182	0.1 nA	3.0	10	0.05	25	4.0	10	±2.5	±18	Low Power JFET Input	P/626
TL062AC	200 pA	6.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power JFET Input	P/626
TL062C	200 pA	15	10	200 pA	4.0	2.0	6.0	±2.5	±18	Low Power JFET Input	P/626
TL072AC	200 pA	6.0	10	50 pA	50	4.0	13	±5.0	±18	Low Noise, JFET Input	P/626, JG/693
TL072C	200 pA	10	10	50 pA	25	4.0	13	±5.0	±18	Low Noise, JFET Input	P/626, JG/693
TL082AC	200 pA	6.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	P/626, JG/693
TL082C	400 pA	15	10	200 pA	25	4.0	13	±5.0	±18	JFET Input	P/626, JG/693

Industrial Temperature Range (–25°C to +85°C)

LM258	0.15	5.0	10	30	50	1.0	0.6	±1.5	±18	Split or Single	H, N/626, J/693
								±3.0	±36	Supply Op Amp	

Automotive Temperature Range (–40°C to +85°C)

LM2904	0.25	7.0	7.0	50	100	1.0	0.6	±1.5	±13	Split or Single	H, N/626, J/693
					typ			±3.0	±26	Supply Op Amp	
MC3358	5.0	8.0	10	75	20	1.0	0.6	±1.5	±18	Split Supplies	P1/626
								±3.0	±36	Single Supply	
MC33072	0.50	5.0	10	75	25	4.5	10	+3.0	+44	High Performance,	P/626, U
MC33072A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	Single Supply	P/626, U
MC33077	1.0	1.0	2.0	180	150	37	11	±2.5	±18	Dual, Low Noise	P/626
MC33078	750 nA	2.0	2.0	150	31.6	16	7.0	±5.0	±18	Low Noise	N/626
MC33172	0.10	4.5	10	20	50	1.8	2.1	+3.0	+44	Low Power, Single	P/626
									Supply		
MC33182	0.1 nA	3.0	10	0.05	25	4.0	10	±2.5	±18	Low Power JFET Input	P/626
MC33282	100 pA	200 μV	5.0	50 pA	50	30	12	±2.5	±18	Low Input Offset JFET	P/646
TL062V	200 pA	6.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power JFET Input	P/626

Military Temperature Range (–55°C to +125°C)

LM158	0.15	5.0	10	30	50	1.0	0.6	±1.5	±18	Split Supplies	H, J/693
								+3.0	+36	Single Supply	
										(Low Power Consumption)	
MC1558	0.5	5.0	10	200	50	1.1	0.8	±3.0	±22	Dual MC1741	G/601, U
MC1558S	0.5	5.0	10	200	50	1.0	10	±3.0	±22	High Slew Rate	G/601, U
MC1747	0.5	5.0	10	200	50	1.0	0.5	±3.0	±22	Dual MC1741	G/601, L
MC3558	0.5	5.0	10	50	50	1.0	0.6	±1.5	±18	Split Supplies	G/601, U
								+3.0	+36	Single Supply	
MC4558	0.5	5.0	10	200	50	2.8	1.6	±3.0	±22	High Frequency	G/601, U
MC35002	100 pA	10	10	100 pA	25	4.0	13	±5.0	±22	JFET Input	G/601, U
MC35002B	100 pA	5.0	10	50 pA	50	4.0	13	±5.0	±22	JFET Input	G/601, U
MC35072	0.5	5.0	10	75	25	4.5	10	+3.0	+44	High Performance,	U
MC35072A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	Single Supply	U
MC35082	200 pA	3.0	10	100 pA	25	8.0	30	±5.0	±22	High Speed, JFET Input	U
MC35082A	200 pA	1.0	10	100 pA	50	8.0	30	±5.0	±22	High Speed, JFET Input	U

OPERATIONAL AMPLIFIERS (continued)

Device	I _B μA	V _{IO} mV	TC _{VIO} μV/°C	I _O nA	A _{vol} V/mV	BW (A _V = 1) MHz	SR (A _V = 1) V/μs	Supply Voltage V		Description	Package Suffix
	Max	Max	Typ	Max	Min	Typ	Typ	Min	Max		
Military Temperature Range (–55°C to +125°C)											
MC35083	200 pA	3.0	10	100 pA	25	16	55	±5.0	±22	Decompensated MC35082 for A _V ≥ 2 Low Power, Single Supply	U
MC35083A	200 pA	1.0	10	100 pA	50	16	55	±5.0	±22		U
MC35172	0.1	4.5	10	20	50	1.8	2.1	+3.0	+44		U
MC35182	0.1 nA	3.0	10	0.05	25	4.0	10	±2.5	±18	Low Power JFET Input	U
TL062M	200 pA	6.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power JFET Input	JG
TL072M	200 pA	6.0	10	50 pA	35	4.0	13	±5.0	±18	Low Noise JFET Input	JG
TL082M	200 pA	6.0	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	JG

Quad Operational Amplifiers

Device	I _B μA Max	V _{IO} mV Max	TC _{VIO} μV/°C Typ	I _O nA Max	A _{vol} V/mV Min	BW (A _V = 1) MHz Typ	SR (A _V = 1) V/μs Typ	Supply Voltage V Min Max		Description	Package Suffix
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Internally Compensated

Commercial Temperature Range (0°C to +70°C)

LF347	200 pA	10	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	N/646
LF347B	200 pA	5.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	N/646
LF444C	100 pA	10	10	50 pA	25	2.0	6.0	±5.0	±18	Low Power JFET Input	N/646
LM324	0.25	6.0	7.0	50	25	1.0	0.6	±1.5	±16	Low Power Consumption	J/632, N/646
LM348	0.2	6.0	—	50	25	1.0	0.5	±3.0	±18	Quad MC1741	J/632, N/646
MC3401/ LM3900	0.3	—	—	—	1.0	5.0	0.6	±1.5	±18	Norton Input	J/632, N/646
MC3403	0.5	10	7.0	50	20	1.0	0.6	±3.0	+36	No Crossover Distortion	L, P/646
MC4741C	0.5	6.0	15	200	20	1.0	0.5	±3.0	±18	Quad MC1741	L, P/646
MC34004	200 pA	10	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	L, P/646
MC34004B	200 pA	5.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	L, P/646
MC34074	0.5	5.0	10	75	25	4.5	10	+3.0	+44	High Performance, Single Supply	L, P/646
MC34074A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	Single Supply	L, P/646
MC34084	200 pA	12	10	100 pA	25	8.0	30	±5.0	±22	High Speed, JFET Input	P/646
MC34084A	200 pA	6.0	10	100 pA	50	8.0	30	±5.0	±22	High Speed, JFET Input	P/646
MC34085	200 pA	12	10	100 pA	25	16	55	±5.0	±22	Decompensated	P/646
MC34085A	200 pA	6.0	10	100 pA	50	16	55	±5.0	±22	MC34084 for A _V ≥ 2	P/646
MC34184	0.1 nA	10	10	0.05	25	4.0	10	±2.5	±18	Low Power JFET Input	P/646
TL064AC	200 pA	6.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power JFET Input	N/646
TL064C	200 pA	15	10	200 pA	4.0	2.0	6.0	±2.5	±18	Low Power JFET Input	N/646
TL074AC	200 pA	6.0	10	50 pA	50	4.0	13	±5.0	±18	Low Noise JFET Input	J/632, N/646
TL074C	200 pA	10	10	50 pA	25	4.0	13	±5.0	±18	Low Noise JFET Input	J/632, N/646
TL084AC	200 pA	6.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	J/632, N/646
TL084C	400 pA	15	10	200 pA	25	4.0	13	±5.0	±18	JFET Input	J/632, N/646

Industrial Temperature Range (–25°C to +85°C)

LM224	0.15	5.0	7.0	30	50	1.0	0.6	±1.5	±16	Split or Single Supply OP Amp	J/632, N/646
LM248	0.2	6.0	—	50	25	1.0	0.5	±3.0	±18	Quad MC1741	J/632, N/646

Automotive Temperature Range (–40°C to +85°C)

LM2902	0.5	10	—	50	—	1.0	0.6	±1.5	±13	Differential Low Power	J/632, N/646
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OPERATIONAL AMPLIFIERS (continued)

	I _B μA Max	V _{IO} mV Max	TCV _{IO} μV/°C Typ	I _O nA Max	A _{vol} V/mV Min	BW (A _V =1) MHz Typ	SR (A _V =1) V/μs Typ	Supply Voltage V Min Max		Description	Package Suffix
Automotive Temperature Range (–40°C to +85°C) (continued)											
MC3301/ LM2900	0.3	—	—	—	1.0	4.0	0.6	±2.0	±15	Norton Input	P/646
MC3303	0.5	8.0	10	75	20	1.0	0.6	±4.0	±28	Differential	N/646
MC33074	0.5	4.5	10	75	25	4.5	10	±1.5	±18	General Purpose	P/646
MC33074A	500 nA	3.0	10	50	50	4.5	10	+3.0	+36	High Performance, Single Supply	L, P/646
MC33079	750 nA	2.5	2.0	150	31.6	9.0	7.0	+3.0	+44	Quad High Performance	L, P/646
MC33174	0.1	4.5	10	20	50	1.8	2.1	±5.0	±18	Quad Low Noise	N/646
MC33184	0.1 nA	10	10	0.05	25	4.0	10	+3.0	+44	Low Power, Single Supply	P/646
MC33274	650 nA	1.0	0.56	25 nA	31.6	5.5	11.5	±2.5	±18	Low Power JFET Input	P/646
MC33284	100 pA	2.0	5.0	50 pA	50	30	12	±1.5	±18	High Performance	P/626
TL064V	200 pA	9.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Input Offset JFET	P/646
								±2.5	±18	Low Power JFET Input	N/646
Telecommunications Temperature Range (–40°C to +85°C)											
MC143403	1.0 nA	30	—	200 pA	45 dB	0.8	1.5	4.75	12.6	CMOS, Low Power, Drives Low-Impedance Loads	L, P/646
MC143404	1.0 nA	30	—	200 pA	60 dB	0.8	1.0	4.75	12.6	CMOS, Very Low Power	L, P/646
Military Temperature Range (–55°C to +125°C)											
LM124	0.15	5.0	7.0	30	50	1.0	0.6	±1.5	±16	Low Power Consumption	J/632, N/646
LM148	0.1	5.0	—	25	50	1.0	0.5	+3.0	+32	Quad MC1741	J/632
MC3503	0.5	5.0	7.0	50	50	1.0	0.6	±3.0	±18	General Purpose	L, P/646
MC4741	0.5	5.0	15	200	50	1.0	0.5	+3.0	+36	Low Power	L
MC35004	100 pA	10	10	100 pA	25	4.0	13	±5.0	±22	Quad MC1741	L
MC35004B	100 pA	5.0	10	50 pA	50	4.0	13	±3.0	±22	JFET Input	L
MC35074	0.5	5.0	10	75	25	4.5	10	±5.0	±22	JFET Input	L
MC35074A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	High Performance, Single Supply	L
MC35084	200 pA	12	10	100 pA	25	8.0	30	±5.0	±22	Quad High Performance	L
MC35084A	200 pA	6.0	10	100 pA	50	8.0	30	±5.0	±22	High Speed, JFET Input	L
MC35085	200 pA	12	10	100 pA	25	16	55	±5.0	±22	High Speed, JFET Input	L
MC35085A	200 pA	6.0	10	100 pA	50	16	55	±5.0	±22	Decompensated	L
MC35174	0.1	4.5	10	20	50	1.8	2.1	MC35084 for A _V ≥2		L	L
MC35184	0.1 nA	10	10	0.05	25	4.0	10	+3.0	+44	Low Power, Single Supply	L
TL064M	200 pA	9.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power JFET Input	J/632
TL074M	200 pA	9.0	10	50 pA	35	4.0	13	±2.5	±18	Low Power JFET Input	J/632
TL084M	200 pA	9.0	10	100 pA	25	4.0	13	±5.0	±18	Low Noise JFET Input	J/632
TL084M	200 pA	9.0	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	J/632

High Frequency Amplifiers

A variety of high frequency circuits with features ranging from low cost simplicity to multi-function versatility marks Motorola's line of integrated amplifiers. Devices described here are intended for industrial and communications appli-

cations. For devices especially dedicated to consumer products, i.e., TV and entertainment radio, see the "Consumer Electronics" section.

AGC Amplifiers

MC1590G Family — Wide-Band General Purpose Amplifiers

The MC1590G, MC1490, MC1350 family are basic building blocks — AGC (Automatic Gain Controlled) RF/Video Amplifiers. These parts are recommended for applications up through 70 MHz. The best high frequency performance may be obtained by using the physically smaller SOIC version (shorter leads) — MC1350D. There are currently no other RF IC's like these, because other manufacturers have dropped their copies. Applications include variable gain video and instrumentation amplifiers, IF (Intermediate Frequency) amplifiers for radio and TV receivers, and transmitter power output control. Many uses will be found in medical instrumentation, remote monitoring, video/graphics processing, and a variety of communications equipment. The family of parts using the same basic die (identical circuit with slightly different test parameters) is listed in the following table.

MC1545/1445 — Gated 2-Channel Input

Differential input and output amplifier with gated 2-channel input for a wide variety of switching purposes. Typical 50 MHz bandwidth makes it suitable for high

frequency applications such as video switching, FSK circuits, multiplexers, etc. Gating circuit is useful for AGC control.

Non-AGC Amplifiers

SE/NE592 — Differential Two Stage Video Amplifier

A monolithic, two stage differential output, wideband video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high pass, low pass, or band pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display and video recorder systems.

MC1733/MC1733C — Video Amplifier

Differential input and output amplifier provides three fixed gain options with bandwidth to 120 MHz. External resistor permits any gain setting from 10 to 400 V/V. Extremely fast rise time (2.5 ns typ) and propagation delay time (3.6 ns typ) makes this unit particularly useful as pulse amplifier in tape, drum, or disc memory read applications.

High-Frequency Amplifier Specifications

Operating Temperature Range			A _v dB	Bandwidth @ MHz	V _{CC} /V _{EE} V _{dc}		Package/Suffix
–55° to +125°C	–40° to +85°C	0° to +70°C			Min	Max	
MC1590G	—	—	50 35	10 100	+6.0	+18	601
—	—	MC1350	50 50	45 45	+6.0	+18	626/P, 751/D
—	MC1490	—	50 35	10 100	+6.0	+18	626/P
MC1545	—	MC1445	19	50	±4.0	±12	632/L
SE592	—	NE592	52 40	40 90	±4.0	±8.0	603/H, 632/F 646/N
MC1733	—	MC1733C	52 40 20	40 90 120	±4.0	±8.0	603/G, 632/L 646/P

Miscellaneous Amplifiers

Motorola provides several bipolar and CMOS special purpose amplifiers which fill specific needs. These

devices range from low power CMOS programmable amplifiers and comparators to variable-gain bipolar power amplifiers.

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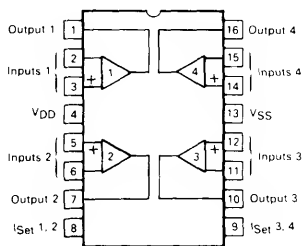
CMOS

MC14573: Quad Programmable Operational Amplifier

MC14574: Quad Programmable Comparator

MC14575: Dual Programmable Operational Amplifier and Dual Programmable Comparator

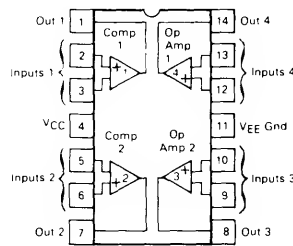
These low power devices are designed for applications such as active filters, voltage reference circuits, function generators, oscillators, and limit set alarms.



Bipolar

MC3505/MC3405: Dual Operational Amplifier and Dual Comparator

This device contains two Differential Input Operational Amplifiers and two Comparators each set capable of single supply operation. This operational amplifier-comparator circuit will find its applications as a general purpose product for automotive circuits and as an industrial "building block."



Device	I_B μA Max	V_{IO} mV Max	I_{IO} nA Max	A_{vol} V/mV Min	Response μs Typ	Supply Voltage		Package Suffix
						Single	Dual	
Bipolar								
MC3505	0.5	5.0	50	20	1.3	3.0 to 36	± 1.5 to ± 18	L/632
MC3405		10						L/632, P/646
CMOS								
MC14573	0.001	± 30	0.0001	1.0	10*	3.0 to 15	± 1.5 to ± 7.5	D/751B, P/648
MC14574								
MC14575								

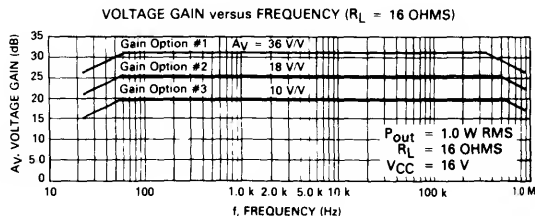
*Propagation Delay

Power Amplifiers Variable Gain

MC1554G— $T_A = -55^\circ$ to $+125^\circ C$, Case 603C

MC1454G— $T_A = 0^\circ$ to $+70^\circ C$, Case 603C

One-watt Power Amplifier for single or split supply operation. Typical voltage gain of 10, 18, or 33 V/V with 0.4% THD.



Comparators

Device	I_B μA Max	V_{IO} mV Max	I_{IO} μA Max	A_V V/V Typ	I_O mA Min	Response Time ns	Supply Voltage V	Description	Temperature Range (°C)	Package Suffix
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Single BIPOLAR

LM111	0.1	3.0	0.01	200 k	8.0	200	+ 15, - 15	With strobe, will operate from single supply	- 55 to + 125	H, J-8
LM211	0.1	3.0	0.01	200 k	8.0	200	+ 15, - 15		- 25 to + 85	H, J-8
LM311	0.25	7.5	0.05	200 k	8.0	200	+ 15, - 15		0 to + 70	H, N/626, J-8

CMOS

MC14578	1.0 pA	50	—	—	1.1	—	+ 3.5 to + 14	Requires only 10 μA from single-ended supply	- 30 to + 70	D/751B, P/648
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Dual BIPOLAR

LM193	0.1	5.0	0.025	200 k	6.0	1300	± 1.5 to ± 18 or + 3.0 to + 36	Designed for single or split supply operation, input common mode includes ground (negative supply)	- 55 to + 125	H
LM193A	0.1	2.0	0.025	200 k	6.0	1300			- 55 to + 125	H
LM293	0.25	5.0	0.05	200 k	6.0	1300			- 25 to + 85	H
LM293A	0.25	2.0	0.05	200 k	6.0	1300			- 25 to + 85	H
LM393	0.25	5.0	0.05	200 k	6.0	1300			0 to + 70	H, N/626
LM393A	0.25	2.0	0.05	200 k	6.0	1300			0 to + 70	H, N/626
LM2903	0.25	7.0	0.05	200 k	6.0	1500			- 40 to + 85	N/626
MC3405	0.5	10	0.05	200 k	6.0	1300	± 1.5 to ± 7.5 or + 3.0 to 15	This device contains two op amps and two comparators in a single package	0 to + 70	L/632, P/646
MC3505	0.5	5.0	0.05	200 k	6.0	1300			- 55 to + 125	L/632

CMOS

MC14575	0.001	30	0.0001	20 k	3.0	1000	± 1.5 to ± 7.5 or + 3.0 to 15	This device contains two op amps and two comparators in a single package	- 40 to + 85	P/648 D/751B
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Quad BIPOLAR

LM139	0.1	5.0	0.025	200 k	6.0	1300	± 1.5 to ± 18 or + 3.0 to + 36	Designed for single or split supply operation, input common mode includes ground (negative supply)	- 55 to + 125	J
LM139A	0.1	2.0	0.025	200 k	6.0	1300			- 55 to + 125	J
LM239	0.25	5.0	0.05	200 k	6.0	1300			- 25 to + 85	J, N/646
LM239A	0.25	2.0	0.05	200 k	6.0	1300			- 25 to + 85	J, N/646
LM339	0.25	5.0	0.05	200 k	6.0	1300			0 to + 70	J, N/646
LM339A	0.25	2.0	0.05	200 k	6.0	1300			0 to + 70	J, N/646
LM2901	0.25	7.0	0.05	100 k	6.0	1300			- 40 to + 85	N/646
MC3302	0.5	20	0.5	30 k	6.0	1300			- 40 to + 85	P/646
MC3430	40	6.0	1.0 Typ	1.2 k	16	33	+ 5.0, - 5.0	High speed comparator/sense-amplifier	0 to + 70	L, P
MC3431	40	10	1.0 Typ	1.2 k	16	33	+ 5.0, - 5.0		0 to + 70	L, P
MC3432	40	6.0	1.0 Typ	1.2 k	16	40	+ 5.0, - 5.0		0 to + 70	L, P
MC3433	40	10	1.0 Typ	1.2 k	16	40	+ 5.0, - 5.0		0 to + 70	L, P

CMOS

MC14574	0.001	30	0.0001	20 k	3.0	10000	± 1.5 to ± 7.5 or + 3.0 to + 15	Externally programmable power dissipation with one or two resistors	- 40 to + 85	P/648 D/751B
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AMPLIFIERS

Operational Amplifiers

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AMPLIFIERS

Operational Amplifiers (con't)

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AMPLIFIERS

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RELATED APPLICATION NOTES

Application Note	Title	Related Device
AN926, AR115	Techniques for Improving the Settling of a DAC and Op. Amp. Combination	LF357, MC34084, MC34085, MC34087
AN273A	Getting More Value Out of an Int. Op. Amp. Data Sheet	MC1439, 1539
AN587, EB20	Analysis and Design of the Op. Amp. Current Source	MC1741
EB57	An Economical FM Trans. Voice Proc. from a Single Integrated Circuit	MC3401

JFET INPUT OPERATIONAL AMPLIFIERS

These low cost JFET input operational amplifiers combine two state-of-the-art linear technologies on a single monolithic integrated circuit. Each internally compensated operational amplifier has well matched high voltage JFET input devices for low input offset voltage. The BIFET technology provides wide bandwidths and fast slew rates with low input bias currents, input offset currents, and supply currents.

These devices are available in single, dual and quad operational amplifiers which are pin-compatible with the industry standard MC1741, MC1458, and the MC3403/LM324 bipolar devices.

- Input Offset Voltage of 5.0 mV Max (LF347B)
- Low Input Bias Current – 50 pA
- Low Input Noise Voltage – $16 \text{ nV}/\sqrt{\text{Hz}}$
- Wide Gain Bandwidth – 4.0 MHz
- High Slew Rate – $13 \text{ V}/\mu\text{s}$
- Low Supply Current – 1.8 mA per Amplifier
- High Input Impedance – $10^{12} \Omega$
- High Common-Mode and Supply Voltage Rejection Ratios – 100 dB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC} V_{EE}	+ 18 – 18	V
Differential Input Voltage	V_{ID}	± 30	V
Input Voltage Range (Note 1)	V_{IDR}	± 15	V
Output Short Circuit Duration (Note 2)	t_S	Continuous	
Power Dissipation at $T_A = +25^\circ\text{C}$	P_D	900	mW
Derate above $T_A = +25^\circ\text{C}$	$1/\theta_{JA}$	10	mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Operating Junction Temperature Range	T_J	115	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

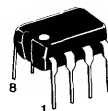
NOTES:

1. Unless otherwise specified, the absolute maximum negative input voltage is limited to the negative power supply.

2. Any amplifier output can be shorted to ground indefinitely. However, if more than one amplifier output is shorted simultaneously, maximum junction temperature ratings may be exceeded.

LF347 LF351 LF353

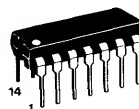
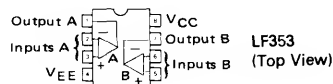
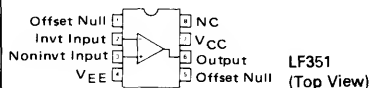
FAMILY OF BIFET OPERATIONAL AMPLIFIERS SILICON MONOLITHIC INTEGRATED CIRCUITS



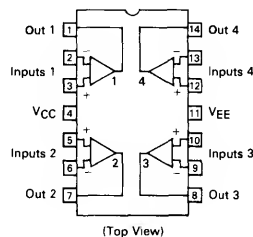
N SUFFIX
 PLASTIC PACKAGE
 CASE 626
 (LF351, LF353 Only)



D SUFFIX
 PLASTIC PACKAGE
 CASE 751
 (SO-8)
 (LF351, LF353 Only)



N SUFFIX
 PLASTIC PACKAGE
 CASE 646
 (LF347 Only)



ORDERING INFORMATION

Function	Device	Package
Single	LF351D	SO-8
Single	LF351N	Plastic DIP
Dual	LF353D	SO-8
Dual	LF353N	Plastic DIP
Quad	LF347BN	Plastic DIP
Quad	LF347N	Plastic DIP

LF347, LF351, LF353

ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = 25^\circ\text{C}$ unless otherwise noted).

Characteristic	Symbol	LF347B			LF347, LF351, LF353			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10\text{ k}$, $V_{CM} = 0$) $T_A = +25^\circ\text{C}$ $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$	V_{IO}	— —	1.0 —	5.0 8.0	— —	5.0 —	10 13	mV
Average Temperature Coefficient of Input Offset Voltage $R_S \leq 10\text{ k}$, $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$	$\Delta V_{IO}/\Delta T$	—	10	—	—	10	—	$\mu\text{V}/^\circ\text{C}$
Input Offset Current ($V_{CM} = 0$, Note 3) $T_A = +25^\circ\text{C}$ $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$	I_{IO}	— —	25 —	100 4.0	— —	25 —	100 4.0	pA nA
Input Bias Current ($V_{CM} = 0$, Note 3) $T_A = +25^\circ\text{C}$ $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$	I_{IB}	— —	50 —	200 8.0	— —	50 —	200 8.0	pA nA
Input Resistance	r_i	—	10^{12}	—	—	10^{12}	—	Ω
Common Mode Input Voltage Range	V_{ICR}	± 11	+15 -12	—	± 11	+15 -12	—	V
Large-Signal Voltage Gain ($V_O = \pm 10\text{ V}$, $R_L = 2.0\text{ k}$) $T_A = +25^\circ\text{C}$ $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$	A_{VOL}	50 25	100 —	— —	25 15	100 —	— —	V/mV
Output Voltage Swing ($R_L = 10\text{ k}$)	V_O	± 12	± 14	—	± 12	± 14	—	V
Common Mode Rejection Ratio ($R_S \leq 10\text{ k}$)	CMRR	80	100	—	70	100	—	dB
Supply Voltage Rejection Ratio ($R_S \leq 10\text{ k}$)	PSRR	80	100	—	70	100	—	dB
Supply Current	I_D	— — —	7.2 — —	11 — —	— — —	7.2 1.8 3.6	11 3.4 6.5	mA
Slew Rate ($A_V = +1$)	SR	—	13	—	—	13	—	$\text{V}/\mu\text{s}$
Gain-Bandwidth Product	BW _p	—	4.0	—	—	4.0	—	MHz
Equivalent Input Noise Voltage ($R_S = 100\text{ }\Omega$, $f = 1000\text{ Hz}$)	e_n	—	24	—	—	24	—	$\text{nV}/\sqrt{\text{Hz}}$
Equivalent Input Noise Current ($f = 1000\text{ Hz}$)	i_n	—	0.01	—	—	0.01	—	$\text{pA}/\sqrt{\text{Hz}}$
Channel Separation (LF347, LF353) 1.0 Hz $\leq f \leq 20\text{ kHz}$ (Input Referred)	—	—	-120	—	—	-120	—	dB

For Typical Characteristic Performance Curves, refer to MC34001/34002/34004 data sheet.

NOTES: (continued)

3. Input bias currents of JFET input op amps approximately double for every 10°C rise in junction temperature. To maintain junction temperatures as close to ambient as is possible, pulse techniques are utilized during test.

MONOLITHIC JFET INPUT OPERATIONAL AMPLIFIERS

These internally compensated operational amplifiers incorporate highly matched JFET devices on the same chip with standard bipolar transistors. The JFET devices enhance the input characteristics of these operational amplifiers by more than an order of magnitude over conventional amplifiers.

This series of op amps combines the low current characteristics typical of FET amplifiers with the low initial offset voltage and offset voltage stability of bipolar amplifiers. Also, nulling the offset voltage does not degrade the drift or common mode rejection.

- Low Input Bias Current — 30 pA
- Low Input Offset Current — 3.0 pA
- Low Input Offset Voltage — 1.0 mV
- Temperature Compensation of Input Offset Voltage — $3.0 \mu\text{V}/^\circ\text{C}$
- Low Input Noise Current — $0.01 \text{ pA}/\sqrt{\text{Hz}}$
- High Input Impedance — $10^{12}\Omega$
- High Common-Mode Rejection Ratio — 100 dB
- High DC Voltage Gain — 106 dB

SERIES FEATURES

- LF355/355B — Low Power Supply Current
- LF356/356B — Wide Bandwidth
- LF357/357B — **Wider Bandwidth Decompensated** ($A_{V\text{min}} = 5$)

	LF355/355B	LF356/356B	LF357/357B
Fast Settling Time to 0.01%	4.0 μs	1.5 μs	1.5 μs
Fast Slew Rate	5.0 V/ μs	12 V/ μs	50 V/ μs
Wide Gain Bandwidth	2.5 MHz	5.0 MHz	20 MHz
Low Input Noise Voltage	20 nV/ $\sqrt{\text{Hz}}$	12 nV/ $\sqrt{\text{Hz}}$	12 nV/ $\sqrt{\text{Hz}}$

ORDERING INFORMATION

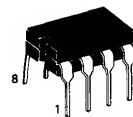
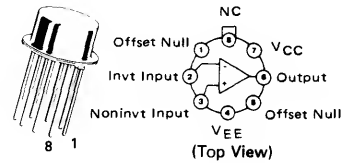
Device	Temperature Range	Package
LF355BH,H LF355BJ,J	0 to +70°C	Metal Can Ceramic DIP
LF356H LF356BJ,J		Metal Can Ceramic DIP
LF357BH,H LF357BJ,J		Metal Can Ceramic DIP

**LF355, LF356,
LF357*, LF355B,
LF356B, LF357B***

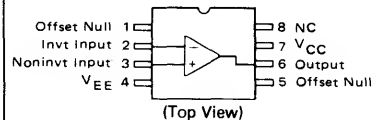
MONOLITHIC JFET OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUITS

H SUFFIX METAL PACKAGE CASE 601



J SUFFIX CERAMIC PACKAGE CASE 693



APPLICATIONS

The LF series is suggested for all general purpose FET input amplifier requirements where precision and frequency response flexibility are of prime importance.

Specific applications include:

- Sample and Hold Circuits
- High Impedance Buffers
- Fast D/A and A/D Converters
- Precision High Speed Integrators
- Wideband, Low Noise, Low Drift Amplifiers

***NOTE:** The LF357/357B are designed for wider bandwidth applications. They are decompensated ($A_{V\text{min}} = 5$).

LF355, LF356, LF357, LF355B, LF356B, LF357B

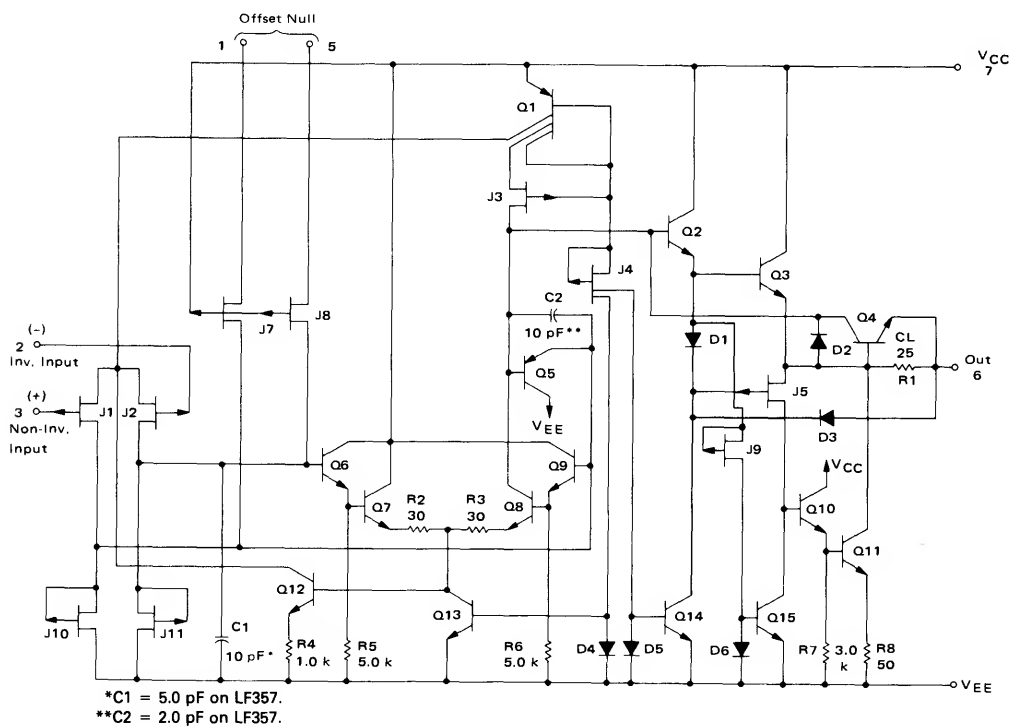
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MAXIMUM RATINGS

Rating	Symbol	LF355B/ 356B/357B	LF355/356/357	Unit
Supply Voltage	V_{CC}	+22	+18	V
	V_{EE}	-22	-18	
Differential Input Voltage	V_{ID}	± 40	± 30	V
Input Voltage Range (Note 1)	V_{IDR}	± 20	± 16	V
Output Short-Circuit Duration	T_S	Continuous		
Operating Ambient Temperature Range	T_A	0 to +70		$^{\circ}\text{C}$
Operating Junction Temperature	T_J	150		$^{\circ}\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150		$^{\circ}\text{C}$

Note 1. Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

CIRCUIT SCHEMATIC



LF355, LF356, LF357, LF355B, LF356B, LF357B

2

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = 15$ to 20 V, $V_{EE} = -15$ to -20 V for LF355B/356B/357B; $V_{CC} = 15$ V, $V_{EE} = -15$ V for LF355/356/357; $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	LF355B/6B/7B			LF355/6/7			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S = 50\ \Omega$, $V_{CM} = 0$) ($T_A = 25^\circ\text{C}$) (Over Temperature)	V_{IO}	—	3.0	5.0 6.5	—	3.0	10 13	mV
Average Temperature Coefficient of Input Offset Voltage ($R_S = 50\ \Omega$)	$\Delta V_{IO}/\Delta T$	—	5.0	—	—	5.0	—	$\mu\text{V}/^\circ\text{C}$
Change in Average TC with V_{IO} Adjust ($R_S = 50\ \Omega$) (Note 2)	$\Delta TC/\Delta V_{IO}$	—	0.5	—	—	0.5	—	$\mu\text{V}/^\circ\text{C}$ per mV
Input Offset Current ($V_{CM} = 0$) (Note 3) ($T_J = 25^\circ\text{C}$) ($T_J \leq 70^\circ\text{C}$)	I_{IO}	—	3.0	20 1.0	—	3.0	50 2.0	pA nA
Input Bias Current ($V_{CM} = 0$) (Note 3) ($T_J = 25^\circ\text{C}$) ($T_J \leq 70^\circ\text{C}$)	I_{IB}	—	30	100 5.0	—	30	200 8.0	pA nA
Input Resistance ($T_J = 25^\circ\text{C}$)	r_i	—	10^{12}	—	—	10^{12}	—	Ω
Large Signal Voltage Gain ($V_O = \pm 10$ V, $R_L = 2.0$ k, $V_{CC} = 15$ V, $V_{EE} = -15$ V) ($T_A = 25^\circ\text{C}$) ($0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$)	A_{VOL}	50 25	200 —	— —	25 15	200 —	— —	V/mV
Output Voltage Swing ($V_{CC} = 15$ V, $V_{EE} = -15$ V, $R_L = 10$ k Ω) ($V_{CC} = 15$ V, $V_{EE} = -15$ V, $R_L = 2$ k Ω)	V_O	± 12 ± 10	± 13 ± 12	— —	± 12 ± 10	± 13 ± 12	— —	V
Input Common-Mode Voltage Range ($V_{CC} = 15$ V, $V_{EE} = -15$ V)	V_{ICR}	± 11	$+15.1$ -12.0	—	± 10	$+15.1$ -12.0	—	V
Common-Mode Rejection Ratio	CMRR	85	100	—	80	100	—	dB
Supply Voltage Rejection Ratio (Note 4)	PSRR	85	100	—	80	100	—	dB
Supply Current ($T_A = 25^\circ\text{C}$, $V_{CC} = 15$ V, $V_{EE} = -15$ V) LF355B/355 LF356B/357B LF356/357	I_D	— — —	2.0 5.0 —	4.0 7.0 —	— — —	2.0 — 5.0	4.0 — 10	mA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 15$ V, $V_{EE} = -15$ V, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	LF355B/355			LF356B/356			LF357B/357			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Slew Rate (Note 5) ($A_V = 1$) LF355/356 ($A_V = 5$) LF357	SR	—	5.0	—	7.5	12	—	—	30	50	V/ μs
Gain-Bandwidth Product	GBW	—	2.5	—	—	5.0	—	—	20	—	MHz
Settling Time to 0.01% (Note 6)	t_s	—	4.0	—	—	1.5	—	—	1.5	—	μs
Equivalent Input Noise Voltage ($R_S = 100\ \Omega$, $f = 100$ Hz) ($R_S = 100\ \Omega$, $f = 1000$ Hz)	e_n	—	25 20	—	—	15 12	—	—	15 12	—	nV/ $\sqrt{\text{Hz}}$
Equivalent Input Noise Current ($f = 100$ Hz) ($f = 1000$ Hz)	i_n	—	0.01 0.01	—	—	0.01 0.01	—	—	0.01 0.01	—	pA/ $\sqrt{\text{Hz}}$
Input Capacitance	C_i	—	3.0	—	—	3.0	—	—	3.0	—	pF

NOTES

- (1) Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply.
- (2) The temperature coefficient of the adjusted input offset voltage changes only a small amount ($0.5\ \mu\text{V}/^\circ\text{C}$ typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.
- (3) The input bias currents approximately double for every 10°C rise in junction temperature, T_J . Due to limited test time, the input bias currents are correlated to junction temperature. Use of a heat sink is recommended if input bias current is to be kept to a minimum.
- (4) Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.
- (5) The Min. slew rate limits apply for the LF356B and the LF357B, but do not apply for the LF356 or LF357.
- (6) Settling time is defined here, for a unity gain inverter connection using 2.0 k resistors for the LF355/6. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10 V step input is applied to the inverter. For the LF357, $A_V = -5.0$, the feedback resistor from output to input is 2.0 k and the output step is 10 V (see settling time test circuit).

TYPICAL DC PERFORMANCE CHARACTERISTICS
(Curves are for LF355, LF356, and LF357 series unless otherwise specified)
INPUT BIAS CURRENT versus CASE TEMPERATURE

FIGURE 1 — (LF355 SERIES)

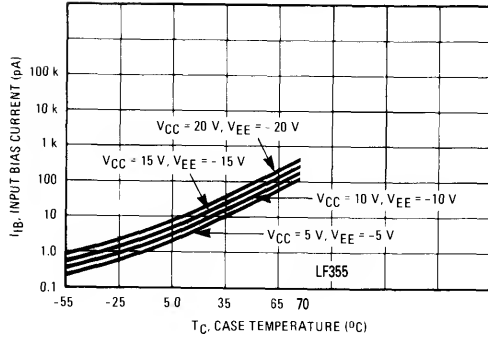


FIGURE 2 — (LF356 AND LF357 SERIES)

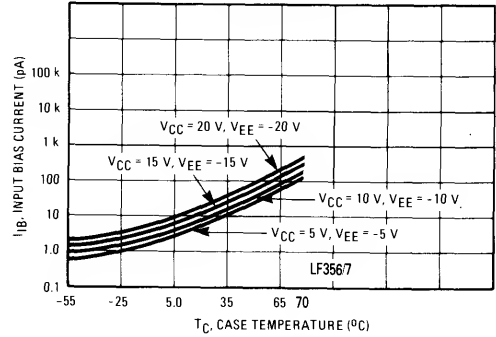


FIGURE 3 — INPUT BIAS CURRENT versus INPUT COMMON-MODE VOLTAGE

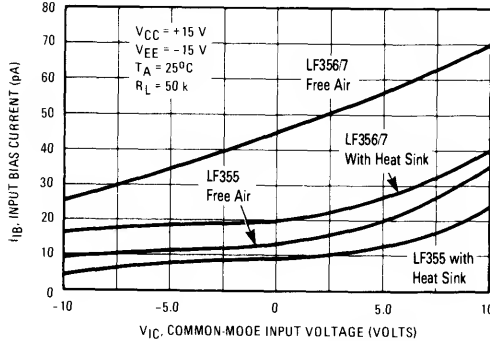
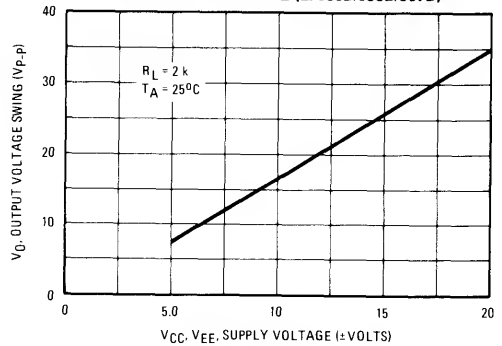


FIGURE 4 — OUTPUT VOLTAGE SWING versus SUPPLY VOLTAGE (LF355B/356B/357B)



SUPPLY CURRENT versus SUPPLY VOLTAGE

FIGURE 5 — (LF355 SERIES)

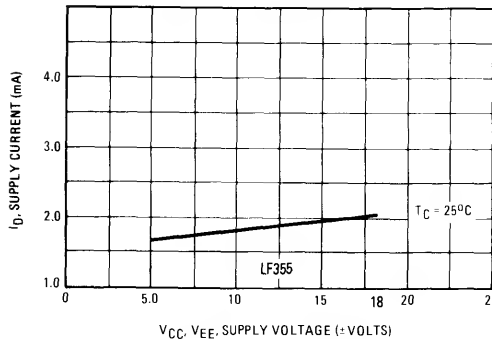
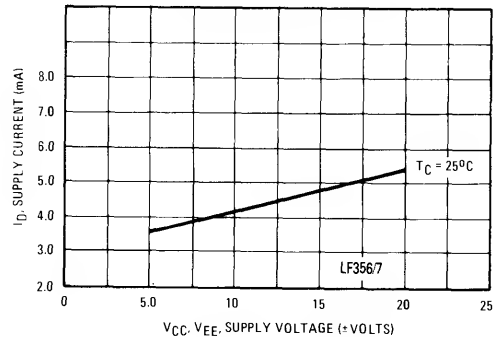


FIGURE 6 — (LF356 AND LF357 SERIES)



TYPICAL DC PERFORMANCE CHARACTERISTICS (continued)

2

FIGURE 7 — NEGATIVE CURRENT LIMIT

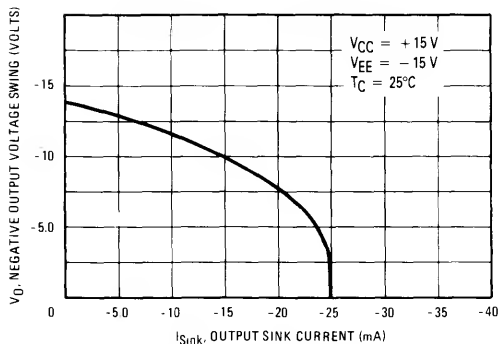


FIGURE 8 — POSITIVE CURRENT LIMIT

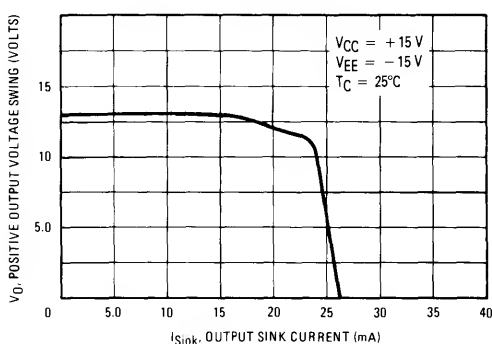


FIGURE 9 — POSITIVE COMMON-MODE INPUT VOLTAGE LIMIT

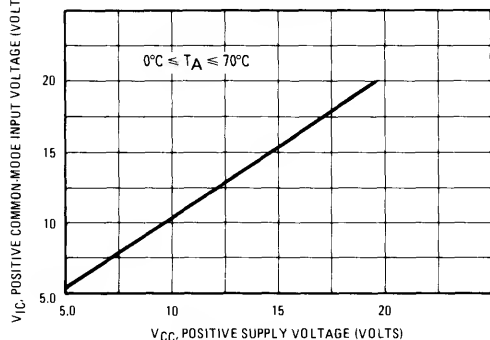


FIGURE 10 — NEGATIVE COMMON-MODE INPUT VOLTAGE LIMIT

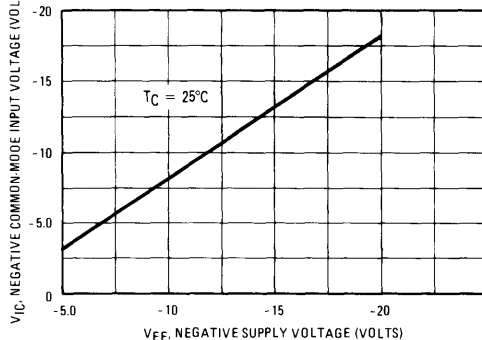


FIGURE 11 — OPEN LOOP VOLTAGE GAIN

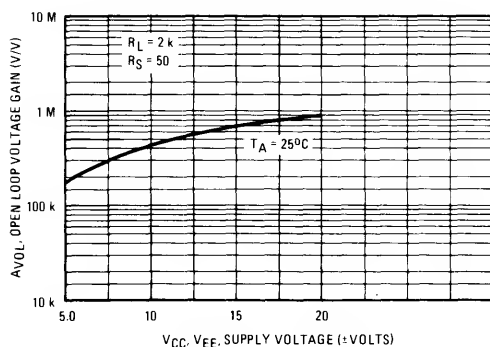
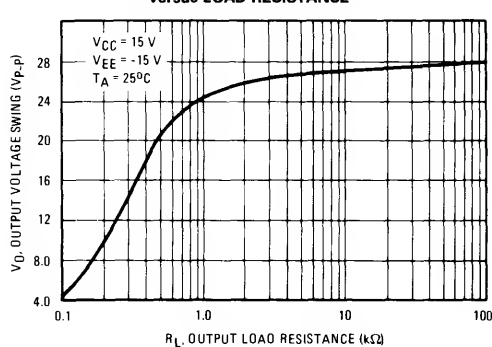


FIGURE 12 — OUTPUT VOLTAGE SWING versus LOAD RESISTANCE



LF355, LF356, LF357, LF355B, LF356B, LF357B

TYPICAL AC PERFORMANCE CHARACTERISTICS

GAIN BANDWIDTH PRODUCT

FIGURE 13 — (LF355 SERIES)

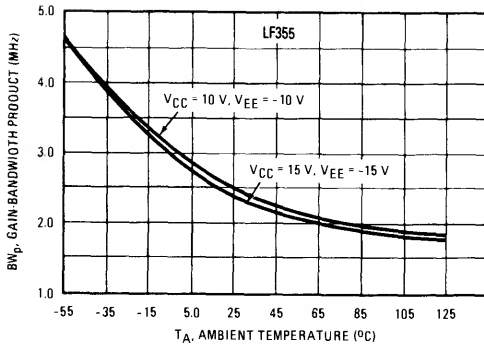
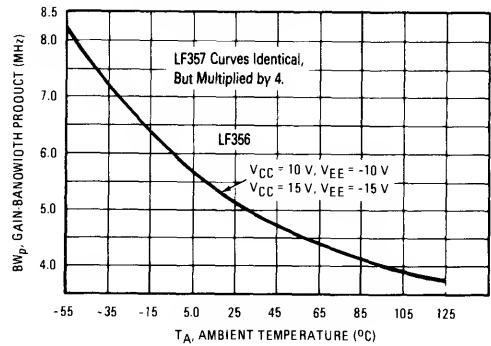


FIGURE 14 — (LF356/357 SERIES)



INVERTER SETTLING TIME

FIGURE 15 — (LF355 SERIES)

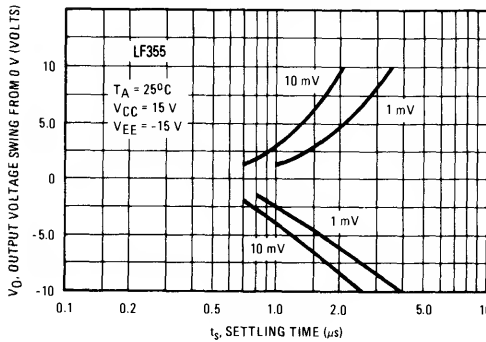


FIGURE 16 — (LF356 AND LF357 SERIES)

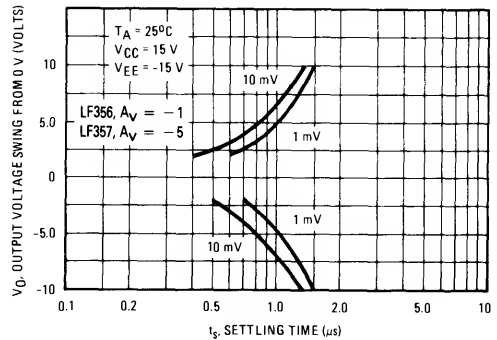


FIGURE 17 — NORMALIZED SLEW RATE

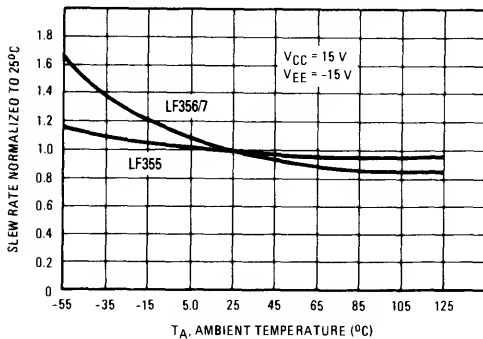
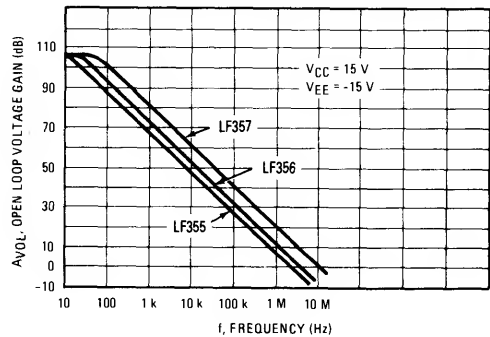


FIGURE 18 — OPEN LOOP FREQUENCY RESPONSE



LF355, LF356, LF357, LF355B, LF356B, LF357B

TYPICAL AC PERFORMANCE CHARACTERISTICS (continued)

BODE PLOT

FIGURE 19 — (LF355 SERIES)

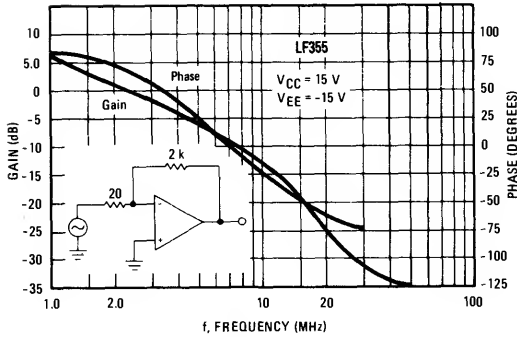


FIGURE 20 — (LF356 SERIES)

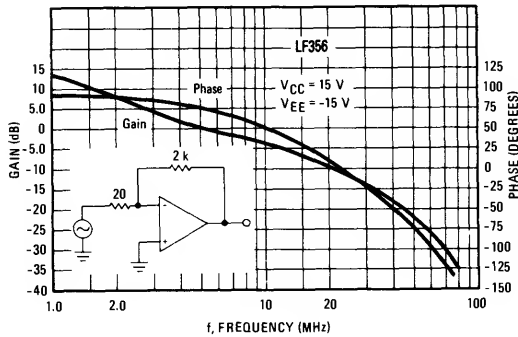
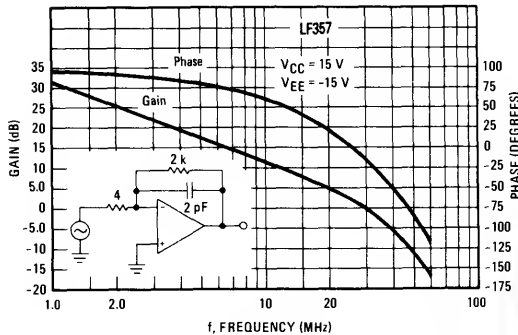


FIGURE 21 — (LF357 SERIES)



OUTPUT IMPEDANCE

FIGURE 22 — (LF355 SERIES)

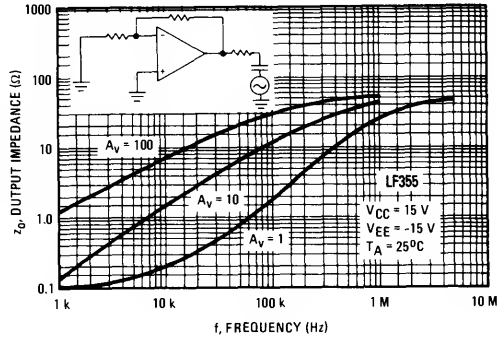


FIGURE 23 — (LF356 SERIES)

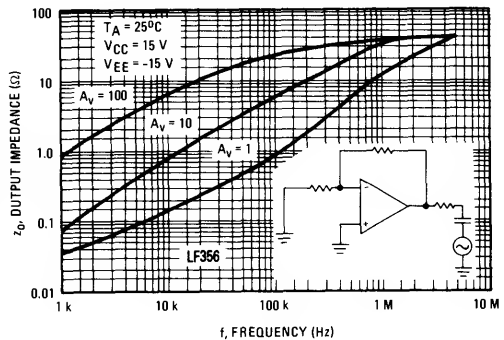
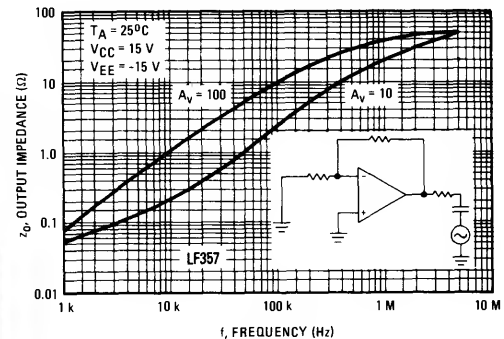


FIGURE 24 — (LF357 SERIES)



LF355, LF356, LF357, LF355B, LF356B, LF357B

TYPICAL AC PERFORMANCE CHARACTERISTICS (continued)

2

FIGURE 25 — COMMON-MODE REJECTION RATIO

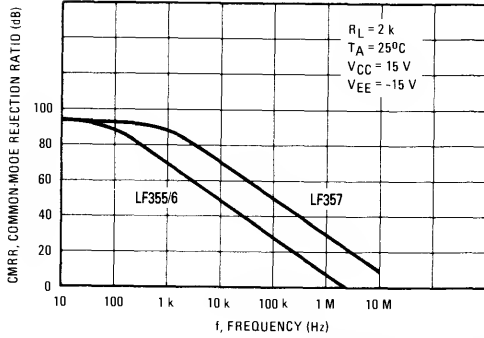
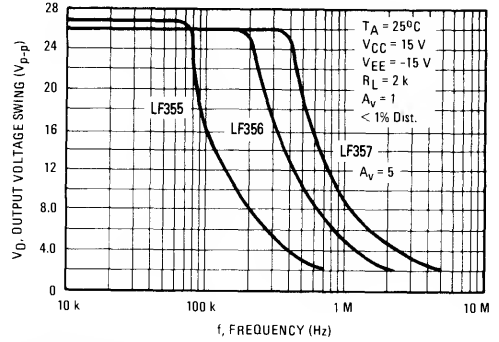


FIGURE 26 — UNDISTORTED OUTPUT VOLTAGE SWING



POWER SUPPLY VOLTAGE REJECTION RATIO

FIGURE 27 — (LF355 SERIES)

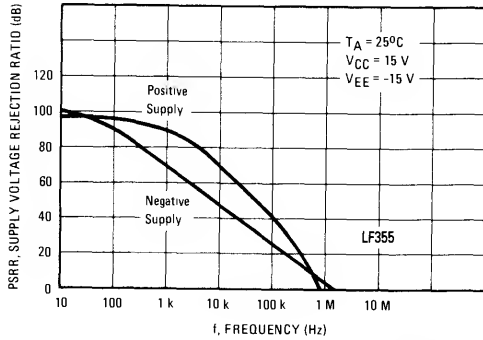
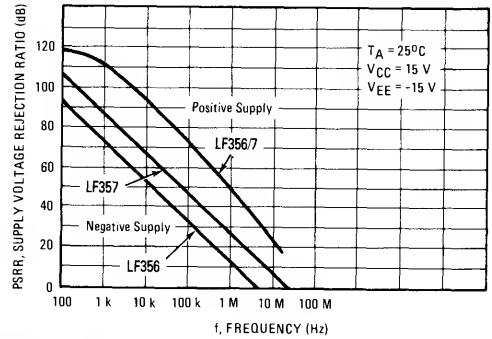


FIGURE 28 — (LF356 AND LF357 SERIES)



EQUIVALENT NOISE VOLTAGE

FIGURE 29 — (LF355/356/357 SERIES)

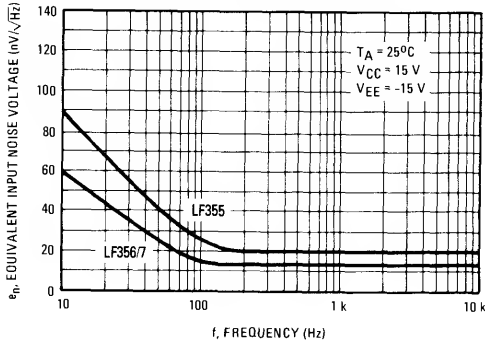
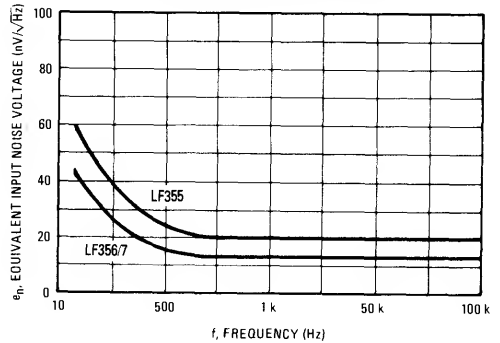


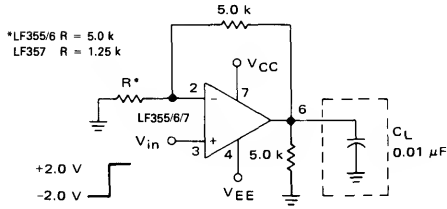
FIGURE 30 (EXPANDED SCALE)



LF355, LF356, LF357, LF355B, LF356B, LF357B

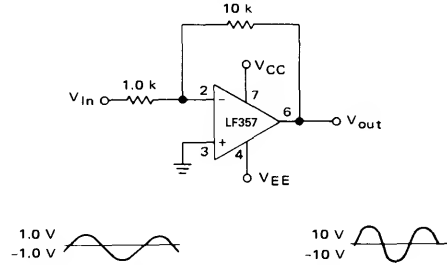
TYPICAL CIRCUIT CONNECTIONS

FIGURE 31 — DRIVING CAPACITIVE LOADS



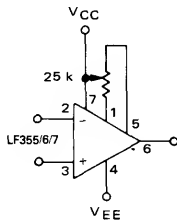
Due to a unique output stage design these amplifiers have the ability to drive large capacitive loads and still maintain stability.
 $C_L(\text{max}) \approx 0.01 \mu\text{F}$.
 Overshoot $\leq 20\%$
 Settling time (t_s) $\approx 5.0 \mu\text{s}$

FIGURE 32 — LARGE POWER BANDWIDTH AMPLIFIER



For distortion $< 1\%$ and a 20 Vp-p V_{out} swing, power bandwidth is: 500 kHz.

FIGURE 33 — INPUT OFFSET VOLTAGE ADJUSTMENT



- V_{IO} is adjusted with a 25 k potentiometer
- The potentiometer wiper is connected to V_{CC}
- For potentiometers with temperature coefficient of 100 ppm/ $^{\circ}\text{C}$ or less the additional drift with adjust is $\approx 0.5 \mu\text{V}/^{\circ}\text{C/mV}$ of adjustment.
- Typical overall drift: $5.0 \mu\text{V}/^{\circ}\text{C} \pm (0.5 \mu\text{V}/^{\circ}\text{C/mV}$ of adjustment.)

FIGURE 34 — SETTLING TIME TEST CIRCUIT

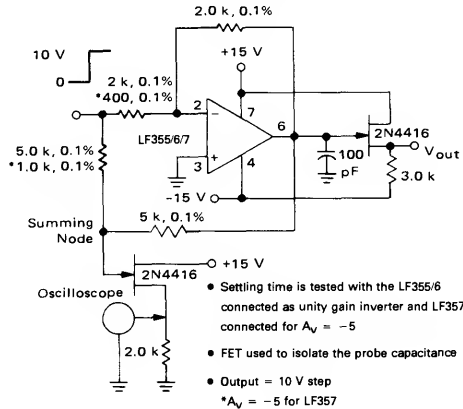


FIGURE 35 — NONINVERTING UNITY GAIN OPERATION FOR LF357

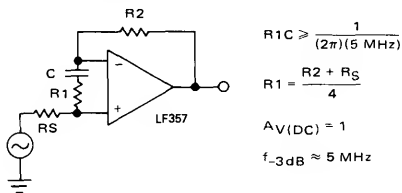
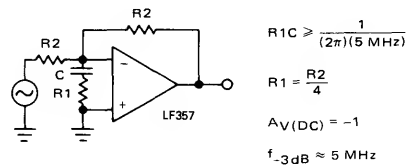
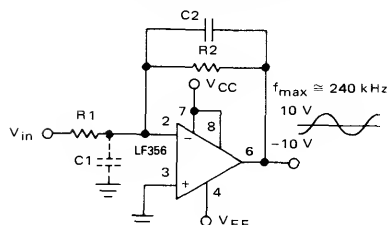


FIGURE 36 — INVERTING UNITY GAIN FOR LF357



TYPICAL APPLICATIONS

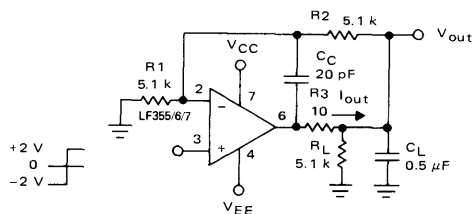
FIGURE 37 — WIDE BW, LOW NOISE, LOW DRIFT AMPLIFIER



• Power BW: $f_{max} = \frac{S_T}{2\pi V_p} \approx 240 \text{ kHz}$

- Parasitic input capacitance ($C_1 = 3 \text{ pF}$ for LF355, LF356, and LF357 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate add C_2 such that: $R_2 C_2 \approx R_1 C_1$.

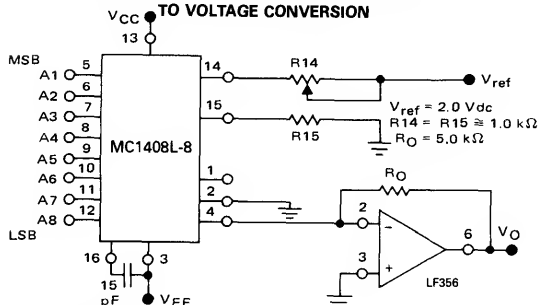
FIGURE 38 — ISOLATING LARGE CAPACITIVE LOADS



- Overshoot 6%
- $t_s = 10 \mu\text{s}$
- When driving large C_L , the V_{out} slew rate is determined by C_L and $I_{out(max)}$:

$$\frac{\Delta V_{out}}{\Delta t} = \frac{I_{out}}{C_L} \approx \frac{0.02}{0.5} \text{ V}/\mu\text{s} = 0.04 \text{ V}/\mu\text{s} \text{ (with } C_L \text{ shown)}$$

FIGURE 39 — 8-BIT D/A WITH OUTPUT CURRENT TO VOLTAGE CONVERSION



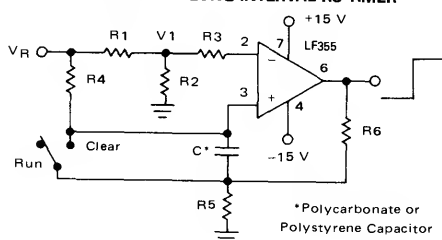
Theoretical V_O

$$V_O = \frac{V_{ref}}{R_{14}} (R_O) \left[\frac{A_1}{2} + \frac{A_2}{4} + \frac{A_3}{8} + \frac{A_4}{16} + \frac{A_5}{32} + \frac{A_6}{64} + \frac{A_7}{128} + \frac{A_8}{256} \right]$$

Adjust V_{ref} , R_{14} or R_O so that V_O with all digital inputs at high level is equal to 9.961 volts.

$$V_O = \frac{2V}{1k} (5k) \left[\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256} \right] = 10V \left[\frac{255}{256} \right] = 9.961V$$

FIGURE 41 — LONG INTERVAL RC TIMER



Time (t) = $R_4 C \ln(V_R/V_R - V_1)$, $R_3 = R_4$, $R_5 = 0.1 R_6$

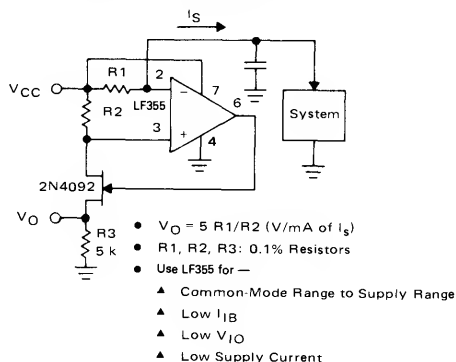
If $R_1 = R_2$: $t = 0.693 R_4 C$

Design Example: 100 Second Timer

$V_R = 10V$, $C = 1 \mu\text{F}$, $R_3 = R_4 = 144M$

$R_6 = 20k$, $R_5 = 2k$, $R_1 = R_2 = 1k$

FIGURE 40 — PRECISION CURRENT MONITOR



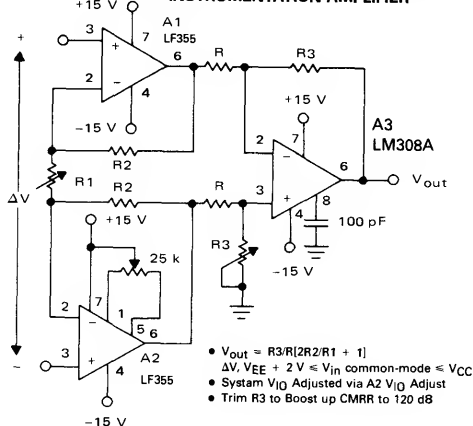
• $V_O = 5 R_1/R_2 (V/mA \text{ of } I_S)$

• R_1, R_2, R_3 : 0.1% Resistors

• Use LF355 for —

- ▲ Common-Mode Range to Supply Range
- ▲ Low I_{IB}
- ▲ Low V_{IO}
- ▲ Low Supply Current

FIGURE 42 — HIGH IMPEDANCE, LOW DRIFT INSTRUMENTATION AMPLIFIER



• $V_{out} = R_3/R_1(2R_2/R_1 + 1)$

• $\Delta V, V_{EE} + 2V \leq V_{in} \text{ common-mode} \leq V_{CC}$

• System V_{IO} Adjusted via $A_2 V_{IO}$ Adjust

• Trim R_3 to Boost up CMRR to 120 dB

**LOW OFFSET, LOW DRIFT JFET INPUT
 OPERATIONAL AMPLIFIER**

Through innovative design concepts and precision matching this monolithic high speed JFET input operational amplifier family offers very low input offset voltage as well as low temperature coefficient of input offset voltage. The amplifier requires less than 3.4 mA per amplifier of supply current yet exhibits greater than 2.7 MHz of gain bandwidth product and more than 8.0 V/ μ s slew rate. Through the use of JFET inputs the amplifier has very low input bias currents and low input offset currents. The amplifier utilizes industry standard pinouts which afford the user the opportunity to directly upgrade circuit performance without the need for redesign.

The LF411C and LF412C are available in the industry standard plastic 8-pin DIP and SO-8 surface mount packages, and specified over the commercial temperature range.

- Low Input Offset Voltage: 2.0 mV Max (Single)
 3.0 mV Max (Dual)
- Low T.C. of Input Offset Voltage: 10 μ V/ $^{\circ}$ C
- Low Input Offset Current: 20 pA
- Low Input Bias Current: 60 pA
- Low Input Noise Voltage: 18 nV/ $\sqrt{\text{Hz}}$
- Low Input Noise Current: 0.01 pA/ $\sqrt{\text{Hz}}$
- Low Total Harmonic Distortion: 0.05%
- Low Supply Current: 2.5 mA
- High Input Resistance: $10^{12} \Omega$
- Wide Gain Bandwidth: 8.0 MHz
- High Slew Rate: 25 V/ μ s (Typ)
- Fast Settling Time: 1.6 μ s (to within 0.01%)

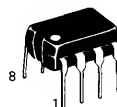
ORDERING INFORMATION

Op Amp Function	Device	Test Temperature Range	Package
Single	LF411CD LF411CN	0 $^{\circ}$ C to +70 $^{\circ}$ C	SO-8 Plastic DIP
Dual	LF412CD LF412CN	0 $^{\circ}$ C to +70 $^{\circ}$ C	SO-8 Plastic DIP

**LF411C
 LF412C**

**SINGLE/DUAL JFET
 OPERATIONAL
 AMPLIFIER**

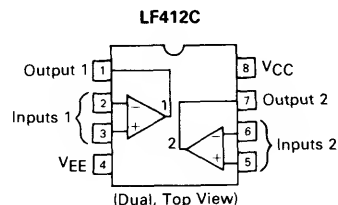
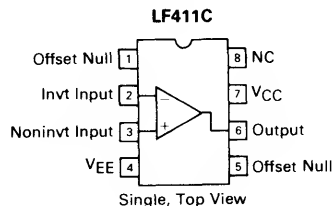
**SILICON MONOLITHIC
 INTEGRATED CIRCUIT**



N SUFFIX
 PLASTIC PACKAGE
 CASE 626



D SUFFIX
 PLASTIC PACKAGE
 CASE 751
 (SO-8)



LF411C, LF412C

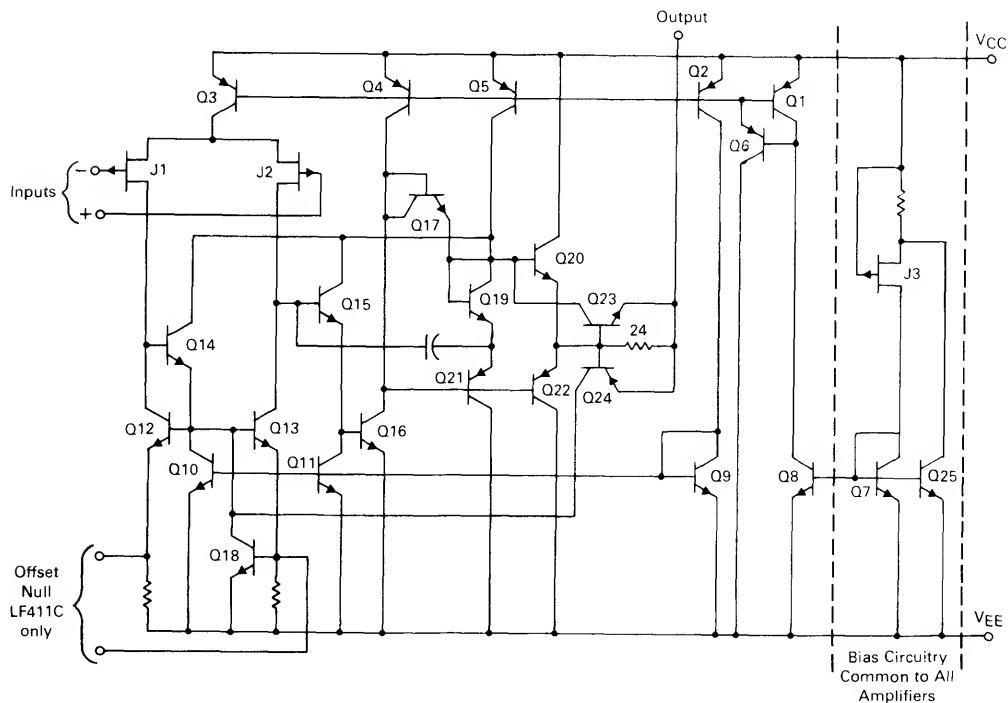
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltages	$V_{CC}, V_{EE} $	+ 18	Volts
Input Differential Voltage Range (Note 1)	V_{IDR}	- 30	Volts
Input Voltage Range (Note 1)	V_{IR}	- 15	Volts
Output Short-Circuit Duration (Note 2)	t_S	Indefinite	Seconds
Maximum Junction Temperature	T_J	+ 150	C
Operating Ambient Temperature Range	T_A	0 to 70	C
Thermal Resistance (Junction to Ambient)	$R_{\theta JA}$	100 180	C/Watt
Storage Temperature	T_{stg}	- 60 to + 150	C
Maximum Power Dissipation	P_D	(Note 2)	mW

NOTES:

1. Input voltages should not exceed V_{CC} or V_{EE} .
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded.
3. Measured with V_{CC} and V_{EE} simultaneously varied.

REPRESENTATIVE CIRCUIT SCHEMATIC (Each Amplifier)



LF411C, LF412C

2

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = 0^\circ\text{C}$ to 70°C unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S = 10\text{ k}\Omega$, $V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$) LF411 LF412	$ V_{IO} $	— —	0.5 1.0	2.0 3.0	mV
Average Temperature Coefficient of Input Offset Voltage ($R_S = 10\text{ k}\Omega$, $V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$)	$\Delta V_{IO} / \Delta T$	—	10	—	$\mu\text{V}/^\circ\text{C}$
Input Offset Current ($V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$) LF411 $T_A = 25^\circ\text{C}$ $T_A = 0^\circ\text{C}$ to 70°C LF412 $T_A = 25^\circ\text{C}$ $T_A = 0^\circ\text{C}$ to 70°C	I_{IO}	— — — —	20 — 25 —	100 2.0 100 2.0	pA nA pA nA
Input Bias Current ($V_{CM} = 0\text{ V}$) LF411 $T_A = 25^\circ\text{C}$ $T_A = 0^\circ\text{C}$ to 70°C LF412 $T_A = 25^\circ\text{C}$ $T_A = 0^\circ\text{C}$ to 70°C	I_{IB}	— — — —	0.6 — 0.5 —	200 4.0 200 4.0	pA nA pA nA
Large Signal Voltage Gain ($V_O = \pm 10\text{ V}$, $R_L = 2.0\text{ k}\Omega$) LF411 $T_A = 25^\circ\text{C}$ $T_A = 0^\circ\text{C}$ to 70°C LF412 $T_A = 25^\circ\text{C}$ $T_A = 0^\circ\text{C}$ to 70°C	A_{VOL}	25 15 25 15	80 — 150 —	— — — —	V/mV
Output Voltage Swing ($V_{ID} = \pm 1.0\text{ V}$, $R_L = 10\text{ k}\Omega$) LF411 LF412	V_{O+} V_{O-} V_{O+} V_{O-}	12 — 12 —	13.9 -14.7 14 -14	— -12 — -12	V
Common Mode Input Voltage Range ($V_O = 0\text{ V}$) LF411 LF412	V_{ICR}	+11 — +11 —	+14 -14 +15 -12	-11 — -11 —	V
Common Mode Rejection ($V_{CM} = \pm 11\text{ V}$, $R_S = 10\text{ k}\Omega$) LF411 LF412	CMR	70 70	90 100	— —	dB
Power Supply Rejection (Note 3) (V_{CC} $V_{EE} = -15\text{ V}$ - 15 V to -5.0 V - 5.0 V) LF411 LF412	PSR	70 70	86 100	— —	dB
Power Supply Current ($V_O = 0\text{ V}$) LF411 LF412	I_D	— —	2.5 2.8	3.4 6.8	mA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
Slew Rate ($V_{IN} = 10\text{ V}$ to -10 V , $R_L = 2.0\text{ k}\Omega$, $A_V = +1.0$) LF411 LF412	SR	8.0 8.0	25 13	— —	V/ μs
Gain Bandwidth Product LF411 LF412	GBW	2.7 2.7	8.0 4.0	— —	MHz
Channel Separation ($f = 1.0\text{ Hz}$ to 20 kHz , LF412)	CS	—	-120	—	dB
Differential Input Resistance ($V_{CM} = 0\text{ V}$)	R_{in}	—	10^{12}	—	$\text{k}\Omega$
Equivalent Input Voltage Noise ($R_S = 100\text{ }\Omega$, $f = 1.0\text{ kHz}$) LF411 LF412	e_n	— —	30 25	— —	nV $\sqrt{\text{Hz}}$
Equivalent Input Noise Current ($f = 1.0\text{ kHz}$) LF411 LF412	i_n	— —	0.01 0.01	— —	pA $\sqrt{\text{Hz}}$

**LOW POWER JFET INPUT
 OPERATIONAL AMPLIFIER**

These JFET input operational amplifiers are designed for low power applications. They feature high input impedance, low input bias current and low input offset current. Advanced design techniques allow for higher slew rates, gain bandwidth products and output swing. The LF441C device provides for the external null adjustment of input offset voltage.

These devices are specified over the commercial temperature range. All are available in plastic dual in-line and SOIC packages.

- Low Supply Current — 200 μ A/Amplifier
- Low Input Bias Current — 5.0 pA
- High Gain Bandwidth — 2.0 MHz
- High Slew Rate — 6.0 V/ μ s
- High Input Impedance — $10^{12} \Omega$
- Large Output Voltage Swing — ± 14 V
- Output Short Circuit Protection

LF441C
LF442C
LF444C

**LOW POWER
 JFET INPUT
 OPERATIONAL AMPLIFIERS**

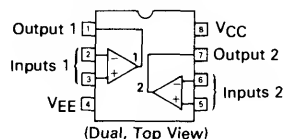
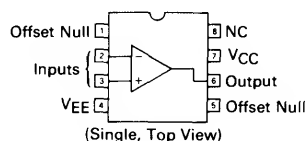
**SILICON MONOLITHIC
 INTEGRATED CIRCUITS**



N SUFFIX
 PLASTIC PACKAGE
 CASE 626

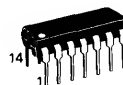


D SUFFIX
 PLASTIC PACKAGE
 CASE 751
 (SO-8)

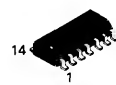


ORDERING INFORMATION

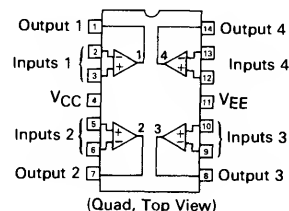
Op Amp Function	Device	Tested Temperature Range	Package
Single	LF441CD LF441CN	0 to +70°C	SO-8 Plastic DIP
Dual	LF442CD LF442CN		SO-8 Plastic DIP
Quad	LF444CD LF444CN		SO-14 Plastic DIP



N SUFFIX
 PLASTIC PACKAGE
 CASE 646



D SUFFIX
 PLASTIC PACKAGE
 CASE 751A
 (SO-14)



LF441C, LF442C, LF444C

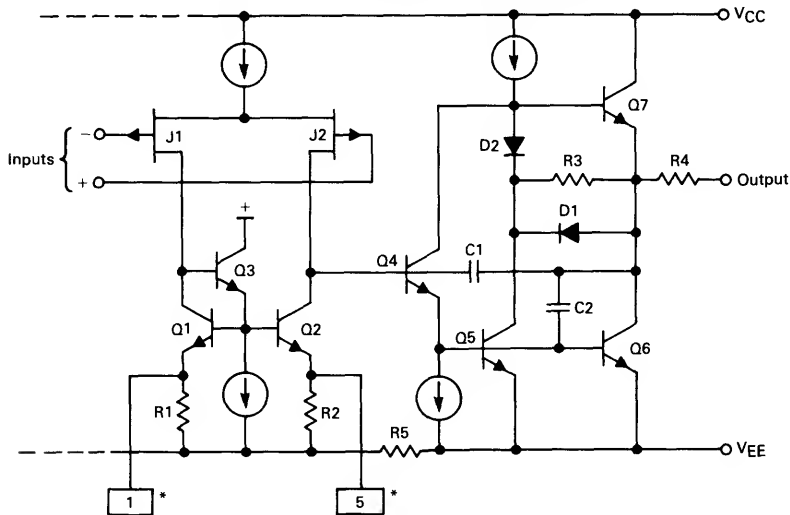
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (from V_{CC} to V_{EE})	V_S	+36	V
Input Differential Voltage Range (Note 1)	V_{IDR}	± 30	V
Input Voltage Range (Notes 1 and 2)	V_{IR}	± 15	V
Output Short-Circuit Duration (Note 3)	t_S	Indefinite	Seconds
Operating Junction Temperature (Note 3)	T_J	+150	$^{\circ}\text{C}$
Storage Temperature Range	T_{stg}	-60 to +150	$^{\circ}\text{C}$

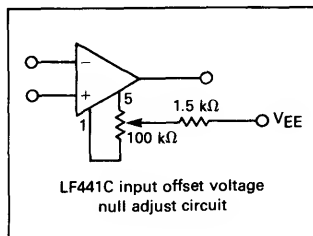
NOTES:

1. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
2. The magnitude of the input voltage must never exceed the magnitude of the supply or 15 volts, whichever is less.
3. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded. (See Figure 1.)

EQUIVALENT CIRCUIT SCHEMATIC (EACH AMPLIFIER)



*Null adjustment pins for LF441 only.



LF441C, LF442C, LF444C

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DC ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S = 10\text{ k}\Omega$, $V_O = 0\text{ V}$)	V_{IO}				mV
Single					
$T_A = +25^\circ\text{C}$		—	3.0	5.0	
$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$		—	—	7.5	
Dual					
$T_A = +25^\circ\text{C}$		—	3.0	5.0	
$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$		—	—	7.5	
Quad					
$T_A = +25^\circ\text{C}$		—	3.0	10	
$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$		—	—	12	
Average Temperature Coefficient of Offset Voltage ($R_S = 10\text{ k}\Omega$, $V_O = 0\text{ V}$)	$\Delta V_{IO}/\Delta T$	—	10	—	$\mu\text{V}/^\circ\text{C}$
Input Offset Current ($V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$)	I_{IO}				
$T_A = +25^\circ\text{C}$		—	0.5	50	pA
$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$		—	—	1.5	nA
Input Bias Current ($V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$)	I_{IB}				
$T_A = +25^\circ\text{C}$		—	3.0	100	pA
$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$		—	—	3.0	nA
Common Mode Input Voltage Range ($T_A = +25^\circ\text{C}$)	V_{ICR}	— -11	+14.5 -12	+11 —	V
Large Signal Voltage Gain ($V_O = \pm 10\text{ V}$, $R_L = 10\text{ k}\Omega$)	A_{VOL}				V/mV
$T_A = +25^\circ\text{C}$		25	60	—	
$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$		15	—	—	
Output Voltage Swing ($R_L = 10\text{ k}\Omega$)	V_{O+} V_{O-}	+12 —	+14 -14	— -12	V
Common Mode Rejection ($R_S \leq 10\text{ k}\Omega$, $V_{CM} = V_{ICR}$, $V_O = 0\text{ V}$)	CMR	70	86	—	dB
Power Supply Rejection ($R_S = 100\text{ }\Omega$, $V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$)	PSR	70	84	—	dB
Power Supply Current (No Load, $V_O = 0\text{ V}$)	I_D				μA
Single		—	200	250	
Dual		—	400	500	
Quad		—	800	1000	

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = +25^\circ\text{C}$, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Slew Rate ($V_{in} = -10\text{ V}$ to $+10\text{ V}$, $R_L = 10\text{ k}\Omega$, $C_L = 10\text{ pF}$, $A_V = +1.0$)	SR	0.6	6.0	—	V/ μs
Settling Time ($A_V = -1.0$, $R_L = 10\text{ k}\Omega$, $V_O = 0\text{ V}$ to $+10\text{ V}$)	t_s				
To within 10 mV		—	1.6	—	μs
To within 1.0 mV		—	2.2	—	
Gain Bandwidth Product ($f = 200\text{ kHz}$)	GBW	0.6	2.0	—	MHz
Equivalent Input Noise Voltage ($R_S = 100\text{ }\Omega$, $f = 1.0\text{ kHz}$)	e_n	—	47	—	nV/ $\sqrt{\text{Hz}}$
Equivalent Input Noise Current ($f = 1.0\text{ kHz}$)	i_n	—	0.01	—	pA/ $\sqrt{\text{Hz}}$
Input Resistance	R_i	—	10^{12}	—	Ω
Channel Separation ($f = 1.0\text{ Hz}$ to 20 kHz)	CS	—	120	—	dB

LF441C, LF442C, LF444C

TYPICAL PERFORMANCE CURVES

FIGURE 1 — MAXIMUM POWER DISSIPATION versus TEMPERATURE FOR PACKAGE VARIATIONS

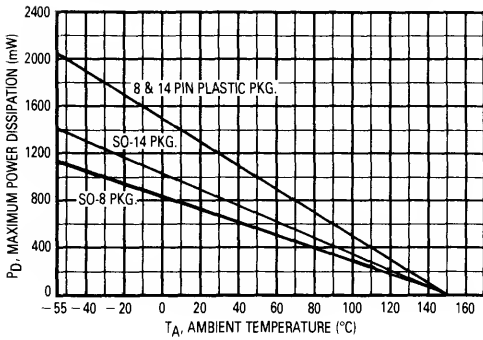


FIGURE 2 — INPUT BIAS CURRENT versus INPUT COMMON-MODE VOLTAGE

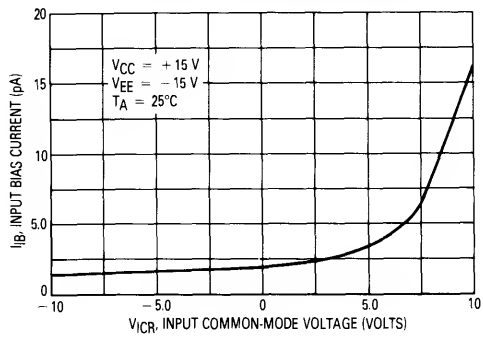


FIGURE 3 — INPUT BIAS CURRENT versus TEMPERATURE

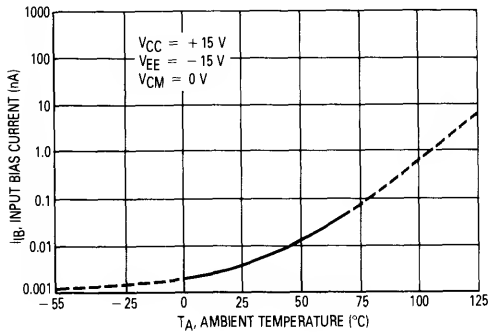


FIGURE 4 — SUPPLY CURRENT versus SUPPLY VOLTAGE

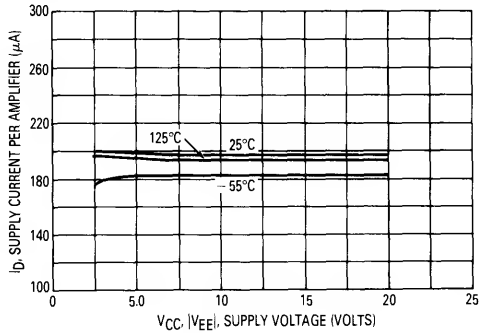


FIGURE 5 — POSITIVE INPUT COMMON-MODE VOLTAGE RANGE versus POSITIVE SUPPLY VOLTAGE

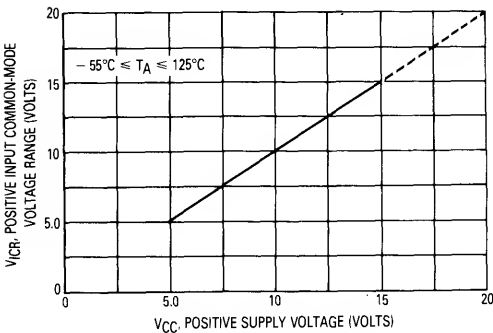
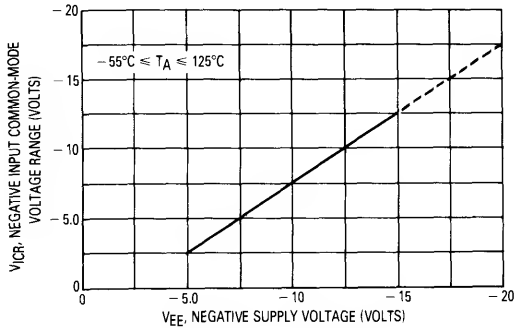


FIGURE 6 — NEGATIVE INPUT COMMON-MODE VOLTAGE RANGE versus NEGATIVE SUPPLY VOLTAGE



LF441C, LF442C, LF444C

2

FIGURE 7 — OUTPUT VOLTAGE versus OUTPUT SOURCE CURRENT

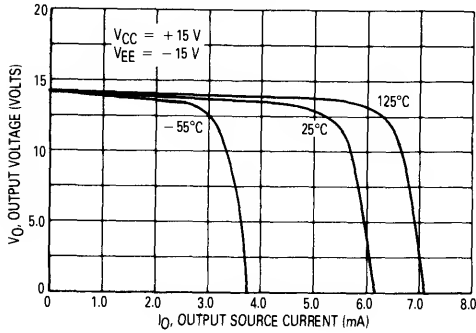


FIGURE 8 — OUTPUT VOLTAGE versus OUTPUT SINK CURRENT

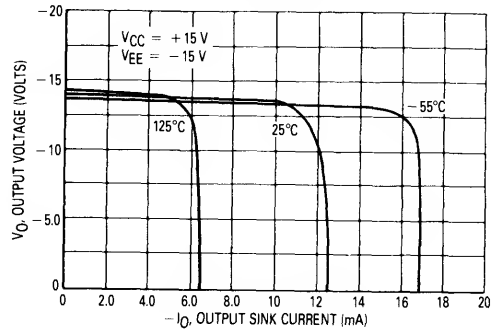


FIGURE 9 — OUTPUT VOLTAGE SWING versus SUPPLY VOLTAGE

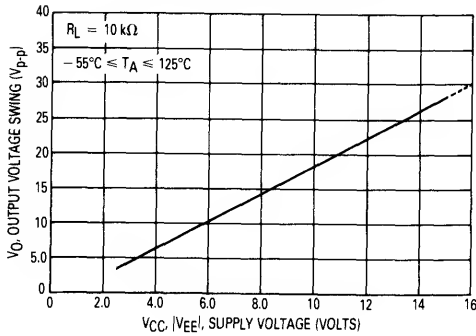


FIGURE 10 — OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

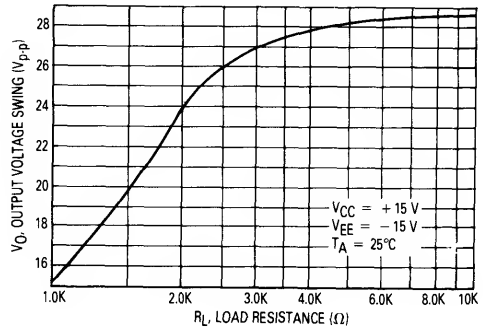


FIGURE 11 — NORMALIZED GAIN BANDWIDTH PRODUCT versus TEMPERATURE

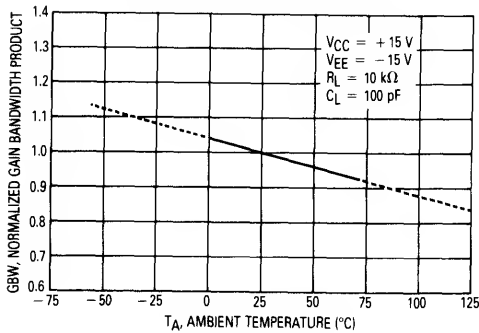
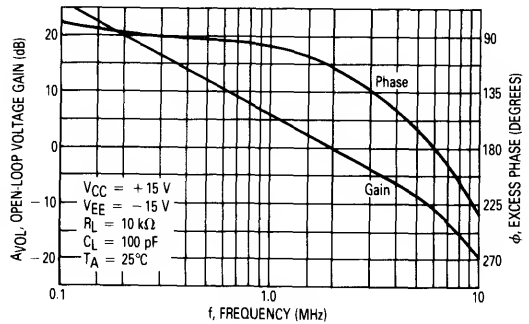


FIGURE 12 — OPEN-LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY



LF441C, LF442C, LF444C

FIGURE 13 — SLEW RATE versus TEMPERATURE

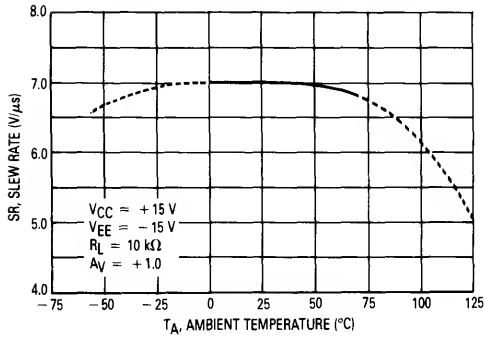


FIGURE 14 — TOTAL OUTPUT DISTORTION versus FREQUENCY

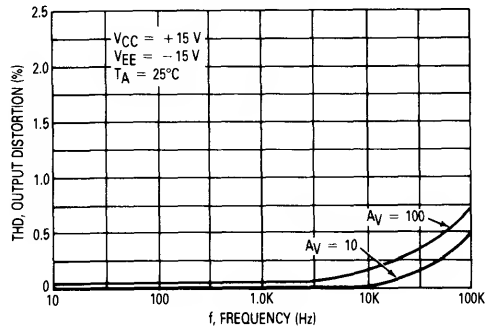


FIGURE 15 — OUTPUT VOLTAGE SWING versus FREQUENCY

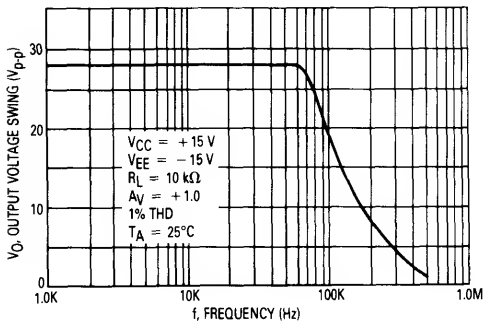


FIGURE 16 — OPEN-LOOP VOLTAGE GAIN versus FREQUENCY

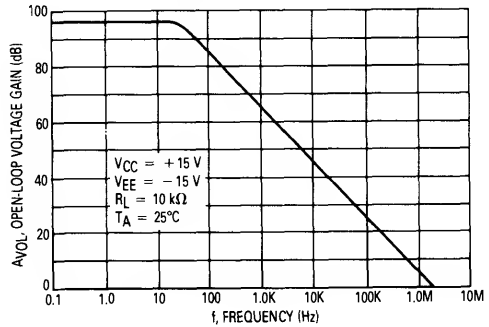


FIGURE 17 — COMMON-MODE REJECTION versus FREQUENCY

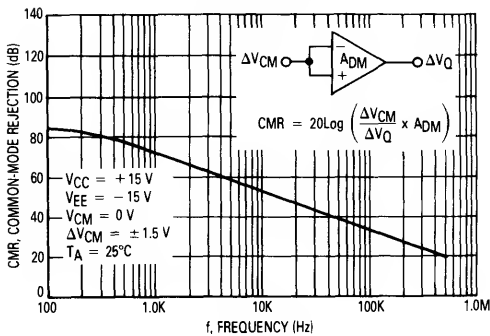


FIGURE 18 — POWER SUPPLY REJECTION versus FREQUENCY

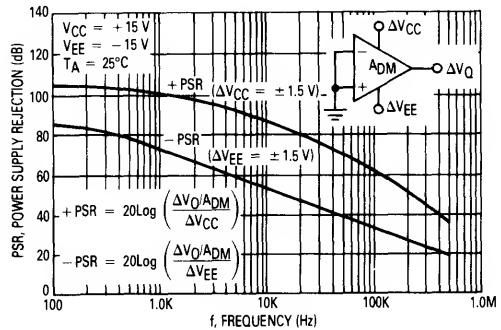


FIGURE 19 — INPUT NOISE VOLTAGE versus FREQUENCY

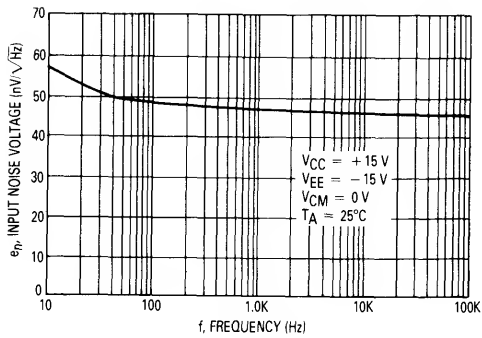


FIGURE 20 — OPEN-LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE

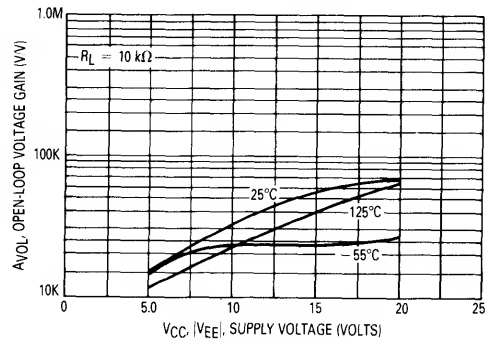


FIGURE 21 — OUTPUT IMPEDANCE versus FREQUENCY

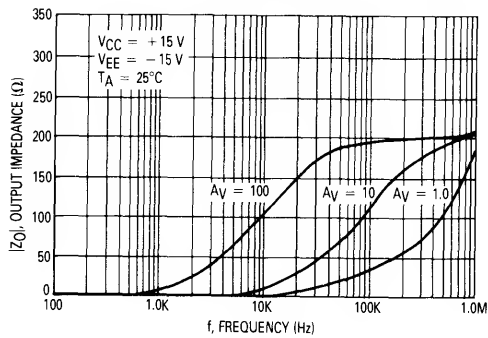
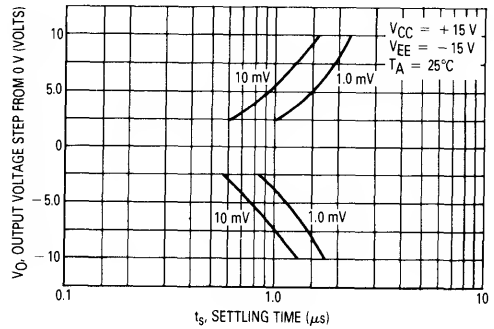


FIGURE 22 — INVERTER SETTLING TIME



LF441C, LF442C, LF444C

SMALL SIGNAL RESPONSE

FIGURE 23 — INVERTING

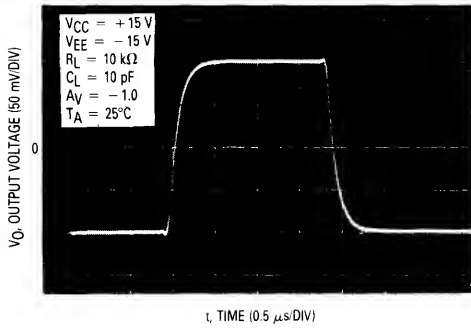
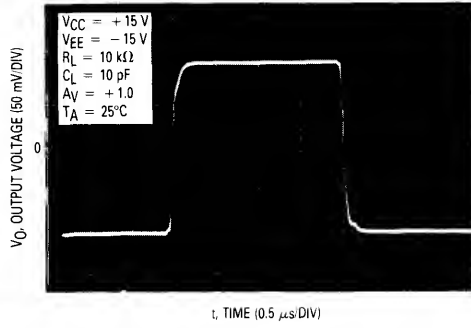


FIGURE 24 — NON-INVERTING



LARGE SIGNAL RESPONSE

FIGURE 25 — INVERTING

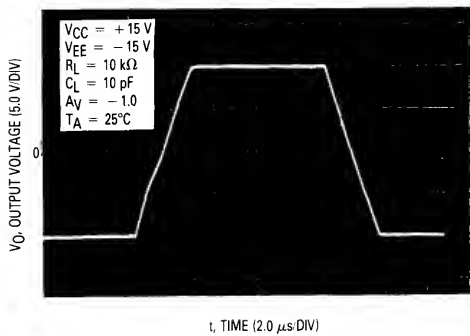
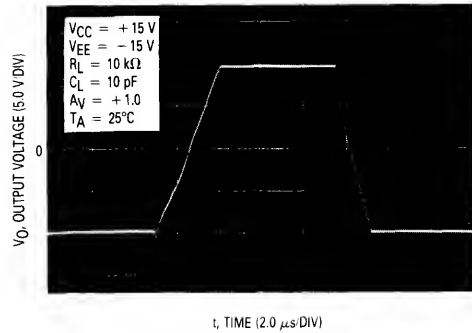


FIGURE 26 — NON-INVERTING



PRECISION OPERATIONAL AMPLIFIERS

The LM11C is a precision, low drift operational amplifier providing the best features of existing FET and Bipolar op amps. Implementation of super gain transistors allows reduction of input bias currents by an order of magnitude over earlier devices such as the LM108A. Offset voltage and drift have also been reduced. Although bandwidth and slew rate are not as great as FET devices, input offset voltage, drift and bias current are inherently lower, particularly over temperature. Power consumption is also much lower, eliminating warm-up stabilization time in critical applications.

Offset balancing is provided, with the range determined by an external low resistance potentiometer. Compensation is provided internally, but external compensation can be added for improved stability when driving capacitive loads.

The precision characteristics of the LM11C make this device ideal for applications such as charge integrators, analog memories, electrometers, active filters, light meters and logarithmic amplifiers.

- Low Input Offset Voltage: 100 μ V
- Low Input Bias Current: 17 pA
- Low Input Offset Current: 0.5 pA
- Low Input Offset Voltage Drift: 1.0 μ V/ $^{\circ}$ C
- Long-Term Stability: 10 μ V/year
- High Common Mode Rejection: 130 dB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} to V_{EE}	40	Vdc
Differential Input Current (Note 1)	I_{ID}	± 10	mA
Output Short-Circuit Duration (Note 2)	t_s	Indefinite	
Power Dissipation (Note 3)	P_D	500	mW
Operating Junction Temperature	T_J	85	$^{\circ}$ C
Storage Temperature Range Metal and Ceramic Packages Plastic Package	T_{stg}	-65 to +150 -55 to +125	$^{\circ}$ C

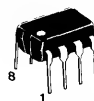
ORDERING INFORMATION

Device	Operating Ambient Temperature Range	Package
LM11CLN, CN	0 to +70 $^{\circ}$ C	Plastic 8-Pin DIP
LM11CLJ-8, CJ-8		Ceramic 8-Pin DIP
LM11CLJ, CJ		Ceramic 14-Pin DIP
LM11CLH, CH		Metal Can

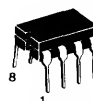
LM11C LM11CL

PRECISION OPERATIONAL AMPLIFIERS

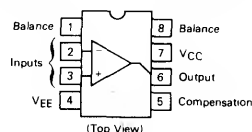
SILICON MONOLITHIC INTEGRATED CIRCUIT



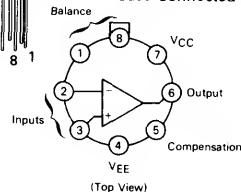
N SUFFIX
PLASTIC PACKAGE
CASE 626



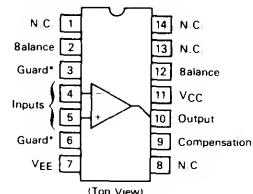
J-8 SUFFIX
CERAMIC PACKAGE
CASE 693



H SUFFIX
METAL CAN
CASE 601
Case Connected To VEE



J SUFFIX
CERAMIC PACKAGE
CASE 632



*Unused pin (no internal connection) to allow for input anti-leakage guard ring on printed circuit board layout.

LM11C, LM11CL

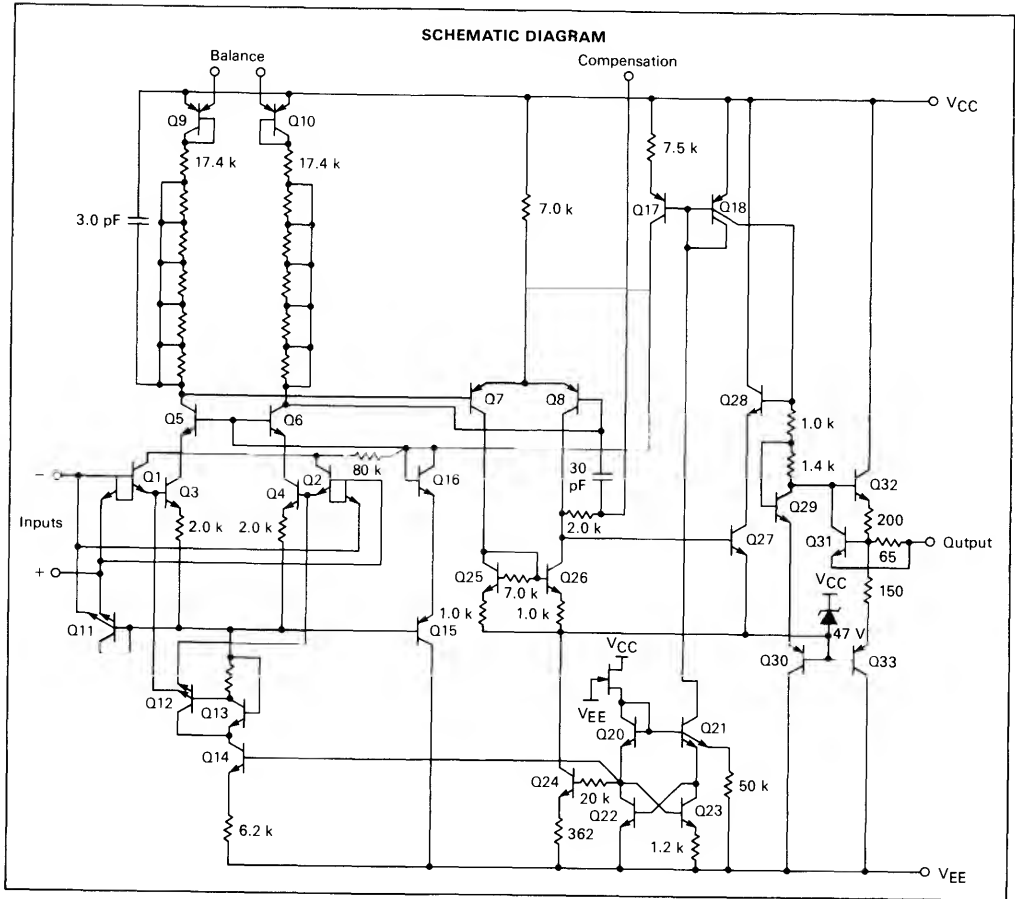
2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted [Note 4])

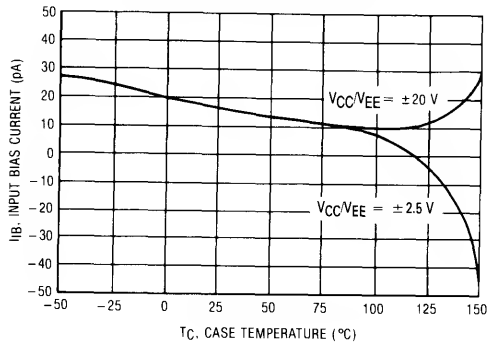
Characteristics	Symbol	LM11C			LM11CL			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage T _{low} to T _{high}	V _{IO}	—	0.2	0.6	—	0.5	5.0	mV
		—	—	0.8	—	—	6.0	
Input Offset Current T _{low} to T _{high}	I _{IO}	—	1.0	10	—	4.0	25	pA
		—	—	20	—	—	50	
Input Bias Current T _{low} to T _{high}	I _{IB}	—	17	100	—	17	200	pA
		—	—	150	—	—	300	
Input Resistance	r _i	—	10 ¹¹	—	—	10 ¹¹	—	Ω
Input Offset Voltage Drift T _{low} to T _{high}	ΔV _{IO} /ΔT	—	2.0	5.0	—	3.0	—	μV/°C
Input Offset Current Drift T _{low} to T _{high}	ΔI _{IO} /ΔT	—	10	—	—	50	—	fA/°C
Input Bias Current Drift T _{low} to T _{high}	ΔI _{IB} /ΔT	—	0.8	3.0	—	1.4	—	pA/°C
Large Signal Voltage Gain V _S = ±15 V, V _{out} = ±12 V, I _{out} = ±2.0 mA T _{low} to T _{high} (Note 5)	A _{VOL}	100	300	—	25	300	—	V/mV
		50	—	—	15	—	—	
V _S = ±15 V, V _{out} = ±12 V, I _{out} = ±0.5 mA T _{low} to T _{high}		250	1200	—	50	800	—	
		100	—	—	30	—	—	
Common Mode Rejection Ratio V _S = ±15 V, -13 V ≤ V _{CM} ≤ 14 V V _S = ±15 V, -12.5 V ≤ V _{CM} ≤ 14 V, T _{low} to T _{high}	CMRR	110	130	—	96	110	—	dB
		100	—	—	90	—	—	
Power Supply Rejection Ratio ±2.5 V ≤ V _S ≤ ±20 V T _{low} to T _{high}	PSRR	100	118	—	84	100	—	dB
		96	—	—	80	—	—	
Power Supply Current T _{low} to T _{high}	I _D	—	0.3	0.8	—	0.3	0.8	mA
		—	—	1.0	—	—	1.0	
Output Short-Circuit Current T _J = 150°C, Output Shorted to Ground	I _{OS}	—	±10	—	—	±10	—	mA

NOTES:

1. The inputs are shunted by back-to-back diodes for over-voltage protection. Excessive current will flow if the input differential voltage is in excess of 1.0 V if no limiting resistance is used. Additionally, a 2.0 kΩ resistance in each input is suggested to prevent possible latch-up initiated by supply reversals.
2. The output is current limited when shorted to ground or any voltages less than the supplies. Continuous overloads will require package dissipation to be considered and heatsinking should be provided when necessary.
3. Devices must be derated based on package thermal resistance (see package outline dimensions).
4. These specifications apply for V_{EE} + 2.0 V ≤ V_{CM} ≤ V_{CC} - 1.0 V (V_{EE} + 2.5 V ≤ V_{CM} ≤ V_{CC} - 1.0 V for T_{low} to T_{high}) and ±2.5 V ≤ V_S ≤ ±20 V
T_{low} to T_{high}: 0°C ≤ T_J ≤ +70°C for LM11C and LM11CL
5. V_{out} = ±11.5 V, all other conditions unchanged.



**FIGURE 1 — INPUT BIAS CURRENT
versus CASE TEMPERATURE**



**FIGURE 2 — INPUT OFFSET CURRENT
versus CASE TEMPERATURE**

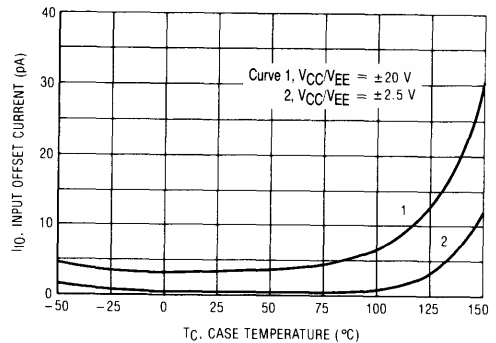


FIGURE 3 — TEMPERATURE COEFFICIENT OF INPUT OFFSET VOLTAGE versus INPUT OFFSET VOLTAGE

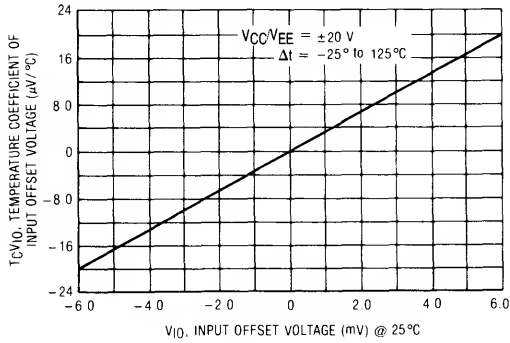


FIGURE 4 — SPECTRAL NOISE DENSITY

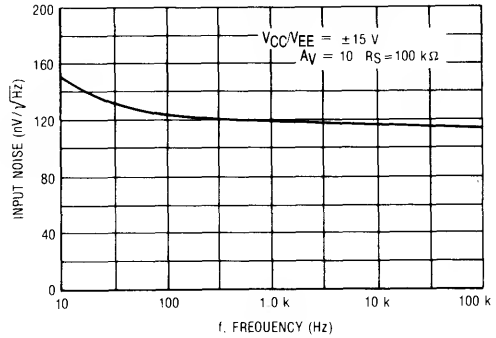


FIGURE 5 — COMMON-MODE LIMITS versus TEMPERATURE

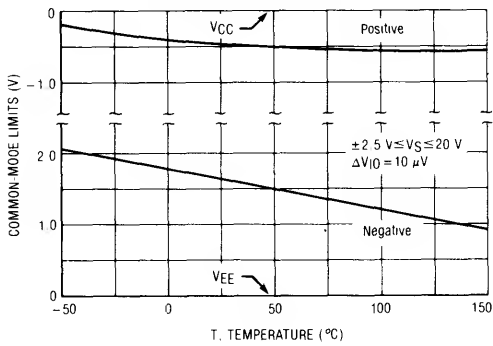


FIGURE 6 — COMMON-MODE REJECTION AND SLEW LIMIT versus FREQUENCY

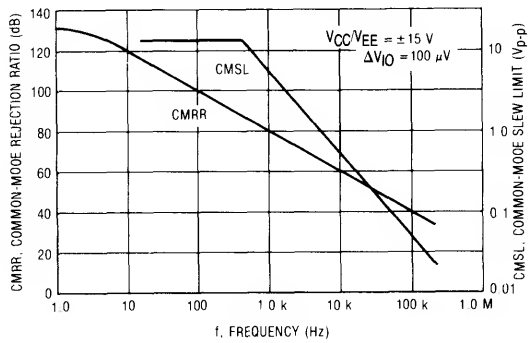


FIGURE 7 — OPEN LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE

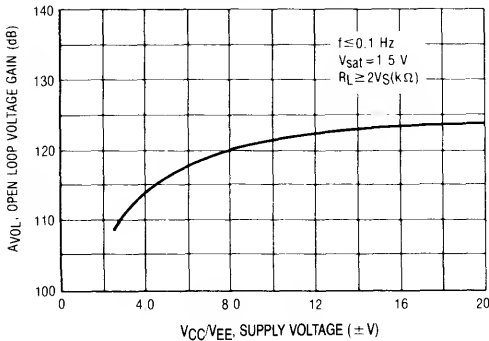


FIGURE 8 — OUTPUT SATURATION versus LOAD CURRENT

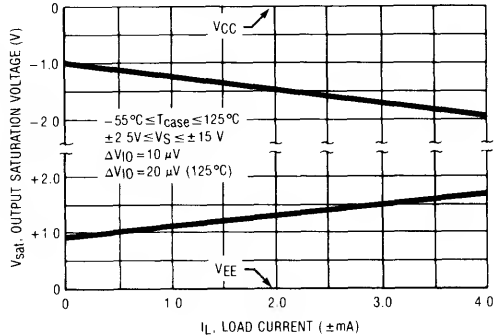


FIGURE 9 — POWER SUPPLY REJECTION RATIO
versus FREQUENCY

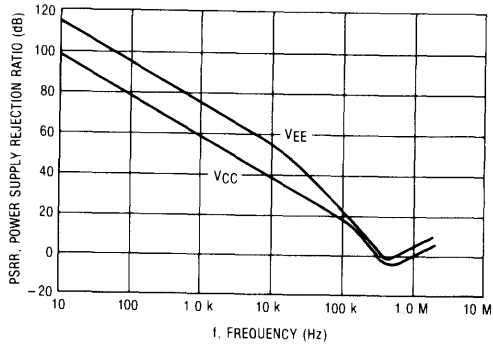


FIGURE 10 — SUPPLY CURRENT versus
SUPPLY VOLTAGE

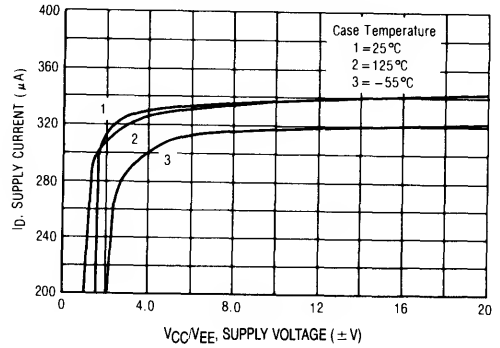


FIGURE 11 — OPEN LOOP VOLTAGE GAIN AND PHASE
versus FREQUENCY

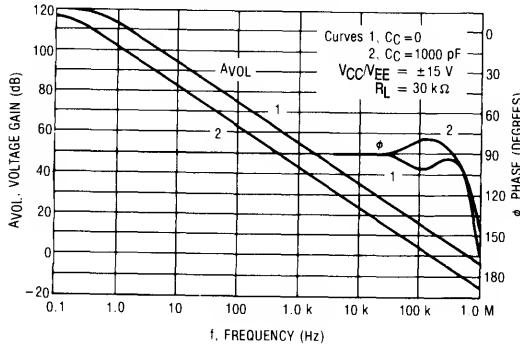


FIGURE 12 — SLEW RATE versus
EXTERNAL COMPENSATION CAPACITOR

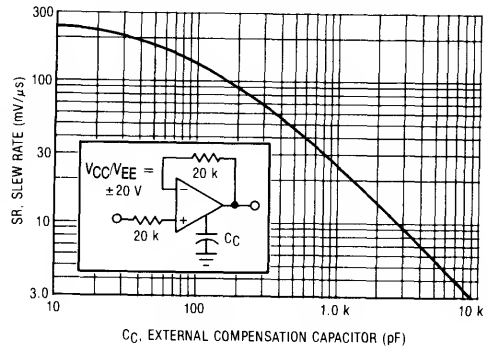
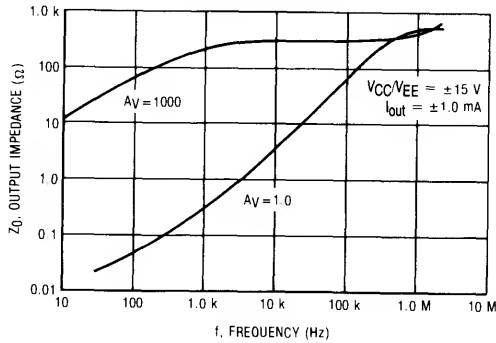


FIGURE 13 — CLOSED LOOP OUTPUT IMPEDANCE
versus FREQUENCY



APPLICATIONS INFORMATION

Due to the extremely low input bias currents of this device, it may be tempting to remove the bias current compensation resistor normally associated with a summing amplifier configuration. Direct connection of the inputs to a low impedance source or ground should be avoided when supply voltages greater than approximately 3.0 volts are used. The potential problem involves reversal of one supply which can cause excessive current to flow in the second supply. Possible destruction of the IC could result if the second supply is not current limited to approximately 100 mA or if bypass capacitors greater than $1.0\ \mu\text{F}$ are used in the supply bus.

Disconnecting one supply will generally cause reversal due to loading of the other supply within the IC and in external circuitry. Although the problem can usually be avoided by placing clamp diodes across the power supplies of each printed circuit board, a careful design will include sufficient resistance in the input leads to limit the current to 10 mA if the input leads are pulled to either supply by internal currents. This precaution is not limited to only the LM11C.

The LM11C is capable of resolving picoampere level signals. Leakage currents external to the IC can severely impair the performance of the device. It is important that high quality insulating materials such as teflon be employed. Proper cleaning to remove fluxes and other residues from printed circuit boards, sockets and the device package are necessary to minimize surface leakage.

When operating in high humidity environments or temperatures near 0°C , a surface coating is suggested to set up a moisture barrier.

Leakage effects on printed circuit boards can be reduced by encircling the inputs (both sides of p.c. board) with a conductive guard ring connected to a low impedance potential nearly the same as that of the inputs.

The suggested printed circuit board layout for input guarding is shown in Figure 14. Guard ring electrical connections for common operational amplifier configurations are illustrated in Figure 15. For critical appli-

cations, a 14-pin dual in-line package is available with guard pins (internally unconnected) adjacent to the inputs for minimal package leakage effects.

Electrostatic shielding is suggested in high-impedance circuits.

Error voltages in external circuitry can be generated by thermocouple effects. Dissimilar metals along with temperature gradients can set up an error voltage ranging in the hundreds of microvolts. Some of the best thermocouples are junctions of dissimilar metals made up of IC package pins and printed circuit boards. Problems can be avoided by keeping low level circuitry away from heat generating elements.

The LM11C is internally compensated, but external compensation can be added to improve stability, particularly when driving capacitive loads.

FIGURE 14 — SUGGESTED PRINTED CIRCUIT BOARD LAYOUT FOR INPUT GUARDING USING METAL PACKAGED DEVICE

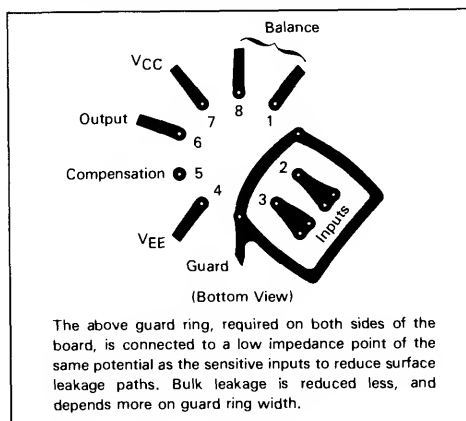


FIGURE 15 — GUARD RING ELECTRICAL CONNECTIONS FOR COMMON AMPLIFIER CONFIGURATIONS

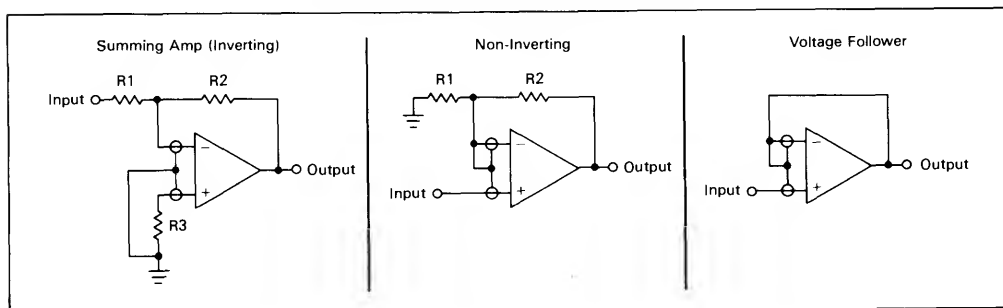


FIGURE 16 — INPUT PROTECTION FOR SUMMING (INVERTING) AMPLIFIER

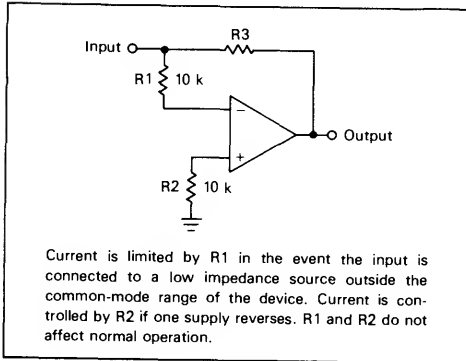


FIGURE 17 — INPUT PROTECTION FOR A VOLTAGE FOLLOWER

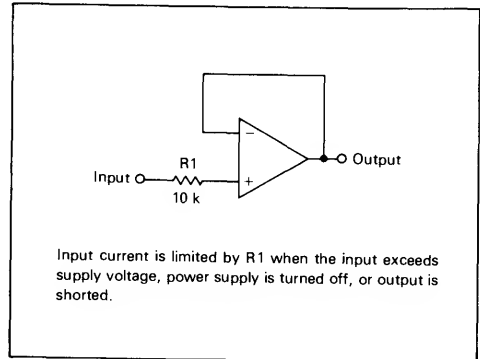


FIGURE 18 — CABLE BOOT STRAPPING AND INPUT SHIELDS

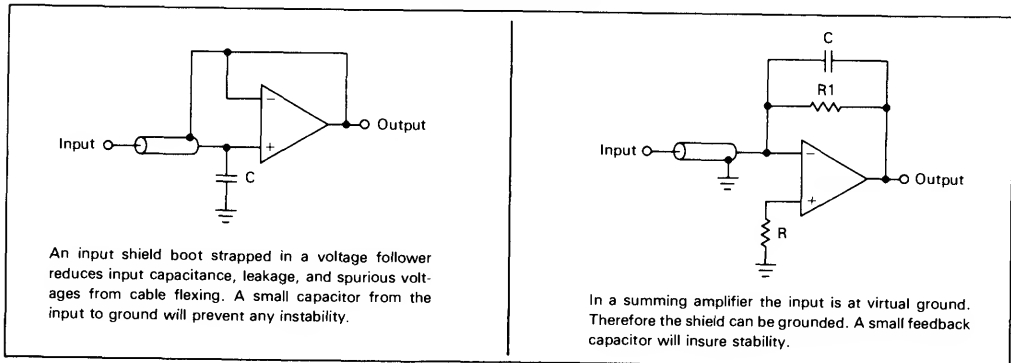
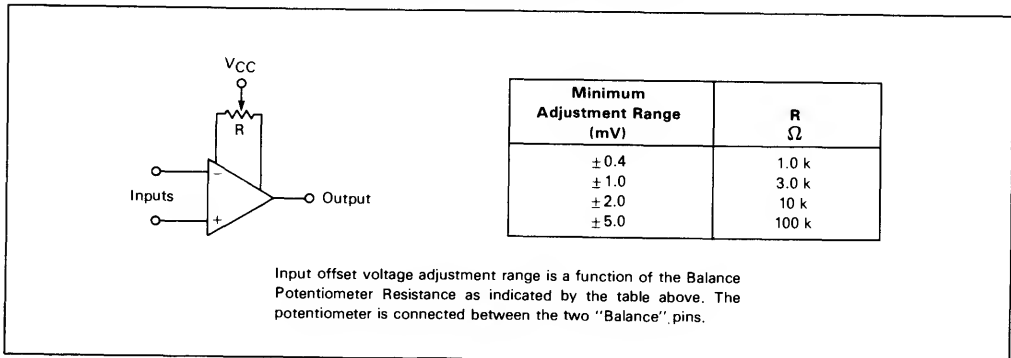


FIGURE 19 — ADJUSTING INPUT OFFSET VOLTAGE WITH BALANCE POTENTIOMETER



OPERATIONAL AMPLIFIER

A general purpose operational amplifier that allows the user to choose the compensation capacitor best suited to his needs. With proper compensation, summing amplifier slew rates to 10 V/ μ s can be obtained.

- Low Input Offset Current — 20 nA Maximum Over Temperature Range
- External Frequency Compensation for Flexibility
- Class AB Output Provides Excellent Linearity
- Output Short Circuit Protection
- Guaranteed Drift Characteristics

FIGURE 1 — STANDARD COMPENSATION AND OFFSET BALANCING CIRCUIT

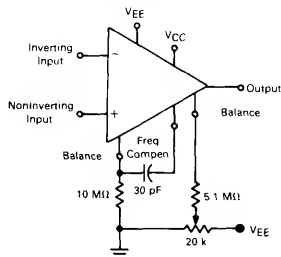


FIGURE 2 — DOUBLE-ENDED LIMIT DETECTOR

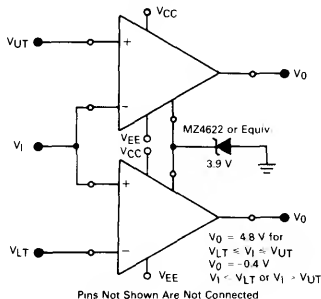
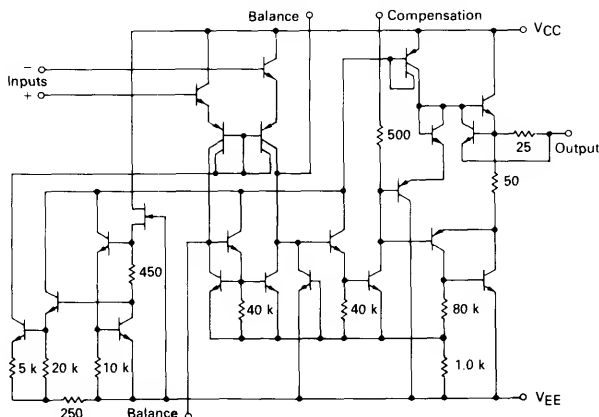


FIGURE 3 — REPRESENTATIVE CIRCUIT SCHEMATIC



LM101A LM201A LM301A

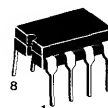
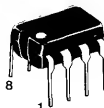
OPERATIONAL AMPLIFIER

SILICON MONOLITHIC
INTEGRATED CIRCUIT

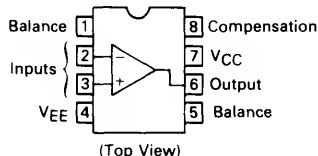
N SUFFIX
PLASTIC PACKAGE
CASE 626

J SUFFIX
CERAMIC PACKAGE
CASE 693

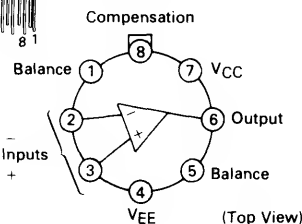
(LM201A and LM301A)



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)



H SUFFIX
METAL PACKAGE
CASE 601



ORDERING INFORMATION

Device	Temperature Range	Package
LM101AH LM101AJ	-55°C to +125°C	Metal Can Ceramic DIP
LM201AD LM201AH LM201AN LM201AJ	-25°C to +85°C	SO-8 Metal Can Plastic DIP Ceramic DIP
LM301AD LM301AH LM301AN LM301AJ	0°C to +70°C	SO-8 Metal Can Plastic DIP Ceramic DIP

LM101A, LM201A, LM301A

MAXIMUM RATINGS

Rating	Symbol	VALUE			Unit
		LM101A	LM201A	LM301A	
Power Supply Voltage	V_{CC}, V_{EE}	± 22	± 22	± 18	Vdc
Input Differential Voltage	V_{ID}	± 30			Volts
Input Common-Mode Range (Note 1)	V_{ICR}	± 15			Volts
Output Short-Circuit Duration	t_S	Continuous			
Power Dissipation (Package Limitation)	P_D				
Metal Can		500			mW
Derate above $T_A = +75^\circ\text{C}$		6.8			mW/ $^\circ\text{C}$
Plastic Dual In-Line Package (LM201A/301A)		625			mW
Derate above $T_A = +25^\circ\text{C}$		5.0			mW/ $^\circ\text{C}$
Ceramic Package		750			mW
Derate above 25°C		6.6			mW/ $^\circ\text{C}$
Operating Ambient Temperature Range	T_A	-55 to $+125$	-25 to $+85$	0 to $+70$	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to $+150$			$^\circ\text{C}$

Note 1. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.

ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted.) Unless otherwise specified, these specifications apply for supply voltages from ± 5.0 V to ± 20 V for the LM101A and LM201A, and from ± 5.0 V to ± 15 V for the LM301A.

Characteristics	Symbol	LM101A LM201A			LM301A			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 50$ k Ω)	V_{IO}	—	0.7	2.0	—	2.0	7.5	mV
Input Offset Current	I_{IO}	—	1.5	10	—	3.0	50	nA
Input Bias Current	I_{IB}	—	30	75	—	70	250	nA
Input Resistance	r_i	1.5	4.0	—	0.5	2.0	—	Megohms
Supply Current	I_{CC}, I_{EE}	—	1.8	3.0	—	—	—	mA
$V_{CC}/V_{EE} = \pm 20$ V		—	—	—	—	1.8	3.0	
$V_{CC}/V_{EE} = \pm 15$ V		—	—	—	—	—	—	
Large Signal Voltage Gain ($V_{CC}/V_{EE} = \pm 15$ V, $V_O = \pm 10$ V, $R_L > 2.0$ k Ω)	A_V	50	160	—	25	160	—	V/mV

The following specifications apply over the operating temperature range.

Input Offset Voltage ($R_S \leq 50$ k Ω)	V_{IO}	—	—	3.0	—	—	10	mV
Input Offset Current	I_{IO}	—	—	20	—	—	70	nA
Average Temperature Coefficient of Input Offset Voltage $T_A(\text{min}) \leq T_A \leq T_A(\text{max})$	$\Delta V_{IO}/\Delta T$	—	3.0	15	—	6.0	30	$\mu\text{V}/^\circ\text{C}$
Average Temperature Coefficient of Input Offset Current $+25^\circ\text{C} \leq T_A \leq T_A(\text{max})$ $T_A(\text{min}) \leq T_A \leq 25^\circ\text{C}$	$\Delta I_{IO}/\Delta T$	—	0.01 0.02	0.1 0.2	—	0.01 0.02	0.3 0.6	nA/ $^\circ\text{C}$
Input Bias Current	I_{IB}	—	—	100	—	—	300	nA
Large Signal Voltage Gain ($V_{CC}/V_{EE} = \pm 15$ V, $V_O = \pm 10$ V, $R_L > 2.0$ k Ω)	A_V	25	—	—	15	—	—	V/mV
Input Voltage Range $V_{CC}/V_{EE} = \pm 20$ V $V_{CC}/V_{EE} = \pm 15$ V	V_I	± 15 —	— —	— —	— ± 12	— —	— —	V
Common-Mode Rejection Ratio $R_S \leq 50$ k Ω	CMRR	80	96	—	70	90	—	dB
Supply Voltage Rejection Ratio $R_S \leq 50$ k Ω	PSRR	80	96	—	70	96	—	dB
Output Voltage Swing $V_{CC}/V_{EE} = \pm 15$ V, $R_L = 10$ k Ω , $R_L = 2.0$ k Ω	V_O	± 12 ± 10	± 14 ± 13	— —	± 12 ± 10	± 14 ± 13	— —	V
Supply Currents ($T_A = T_A(\text{max})$, $V_{CC}/V_{EE} = \pm 20$ V)	I_{CC}, I_{EE}	—	1.2	2.5	—	—	—	mA

LM101A, LM201A, LM301A

TYPICAL CHARACTERISTICS

($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 4 — MINIMUM INPUT VOLTAGE RANGE

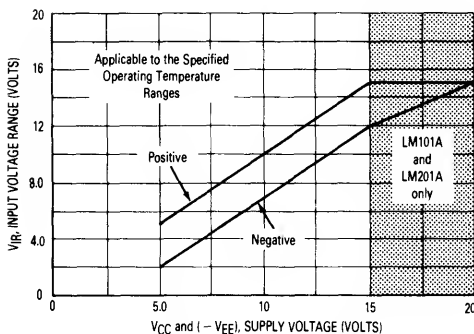


FIGURE 5 — MINIMUM OUTPUT VOLTAGE SWING

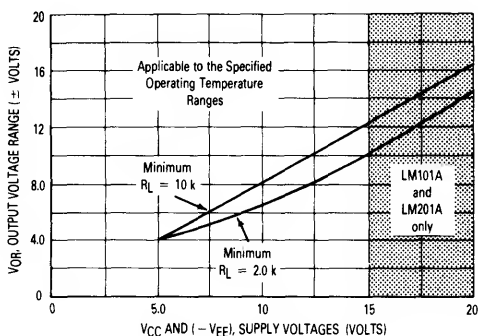


FIGURE 6 — MINIMUM VOLTAGE GAIN

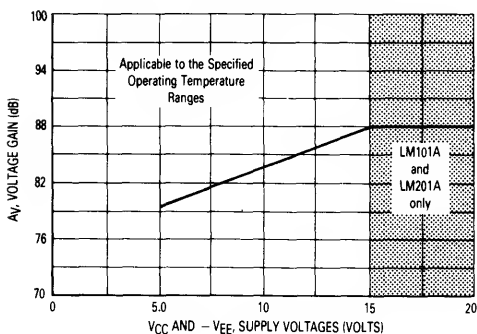


FIGURE 7 — TYPICAL SUPPLY CURRENTS

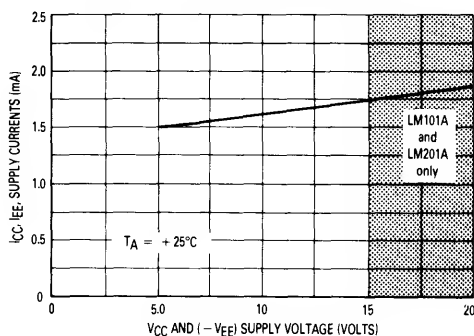


FIGURE 8 — OPEN-LOOP FREQUENCY RESPONSE

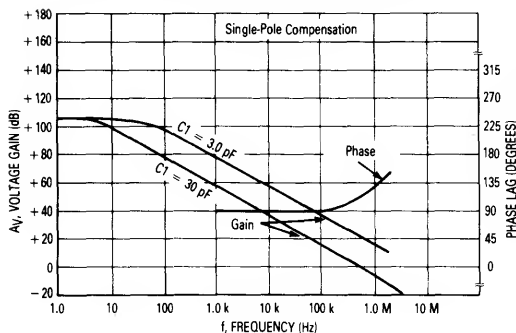
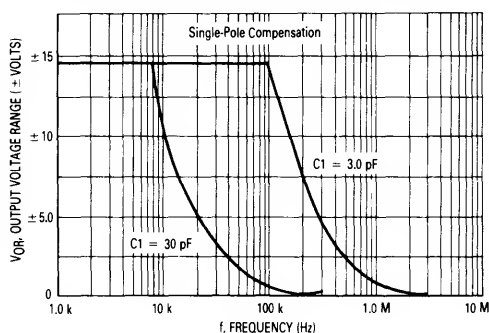


FIGURE 9 — LARGE-SIGNAL FREQUENCY RESPONSE



LM101A, LM201A, LM301A

TYPICAL CHARACTERISTICS (continued)

($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 10 — VOLTAGE FOLLOWER PULSE RESPONSE

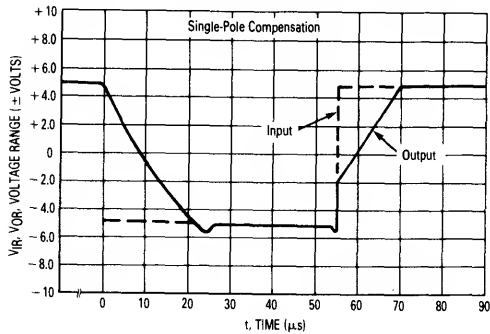


FIGURE 11 — OPEN-LOOP FREQUENCY RESPONSE

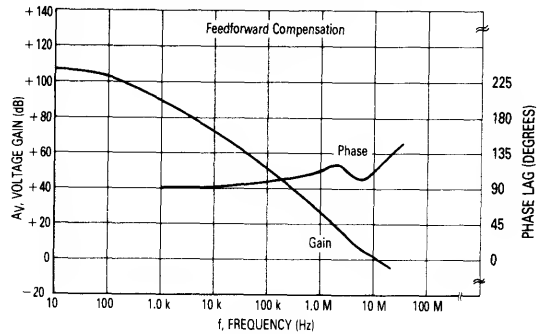


FIGURE 12 — LARGE-SIGNAL FREQUENCY RESPONSE

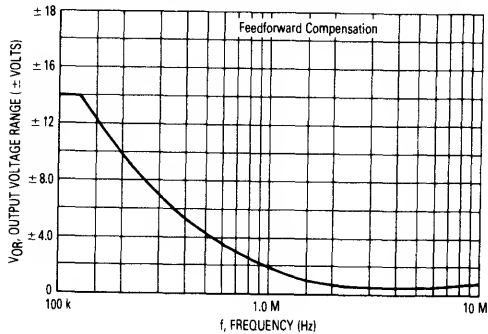
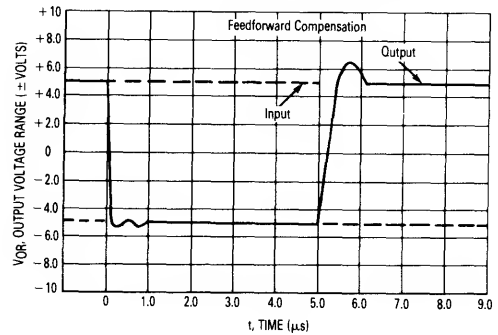


FIGURE 13 — INVERTER PULSE RESPONSE



TYPICAL COMPENSATION CIRCUITS

FIGURE 14 — SINGLE-POLE COMPENSATION

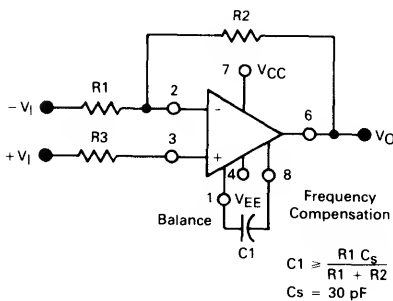
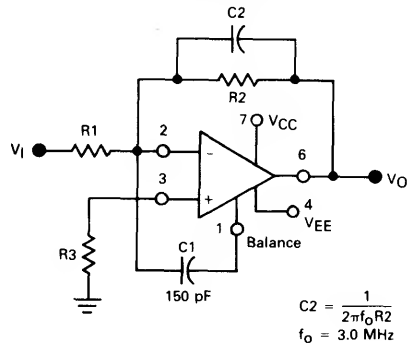


FIGURE 15 — FEEDFORWARD COMPENSATION



PRECISION OPERATIONAL AMPLIFIERS

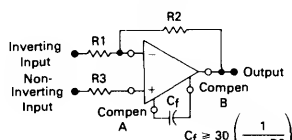
The LM108/LM208/LM308 Series operational amplifiers provide high input impedance, low input offsets and temperature drifts, and low noise. These characteristics are made possible by use of a special Super Beta processing technology. This series of amplifiers is particularly useful for applications where high-accuracy and low-drift performance are essential. In addition high-speed performance may be improved by employing feed-forward compensation techniques to maximize slew rate without compromising other performance criteria.

The LM108A/LM208A/LM308A Series offers extremely low input offset voltage and drift specifications allowing usage in even the most critical applications without external offset nulling.

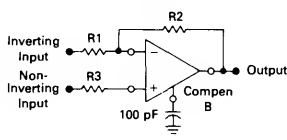
- Operation From a Wide Range of Power Supply Voltages
- Low Input Bias and Offset Currents
- Low Input Offset Voltage and Guaranteed Offset Voltage Drift Performance
- High Input Impedance

FREQUENCY COMPENSATION

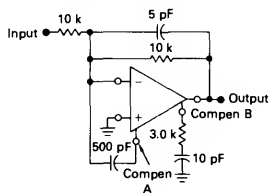
Standard Compensation



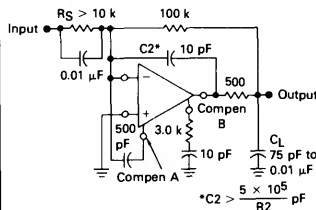
Modified Compensation



Standard Feedforward Compensation



Feedforward Compensations for Decoupling Load Capacitance



ORDERING INFORMATION

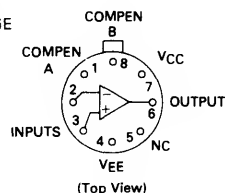
Device	Temperature Range	Package
LM108AH, H LM108AJ, J, AJ-8, J-8	-55 to +125°C	Metal Can Ceramic DIP
LM208AH, H LM208AJ, J, AJ-8, J-8 LM208AN, N LM208AD, D	-25 to +85°C	Metal Can Ceramic DIP Plastic DIP SO-8
LM308H, H LM308AJ, J, AJ-8, J-8 LM308AN, N LM308AD, D	0 to +70°C	Metal Can Ceramic DIP Plastic DIP SO-8

LM108, LM108A LM208, LM208A LM308, LM308A

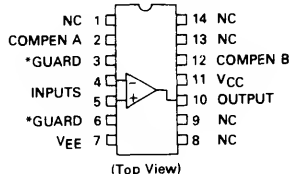
SUPER GAIN OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUIT

H SUFFIX METAL PACKAGE CASE 601



J SUFFIX CERAMIC PACKAGE CASE 632



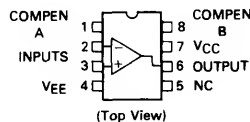
N SUFFIX PLASTIC PACKAGE CASE 626 (LM208, LM208A) (LM308, LM308A Only)



J-8 SUFFIX CERAMIC PACKAGE CASE 693



D SUFFIX PLASTIC PACKAGE CASE 751 (SO-8)



*Unused pin (no internal connection) to allow for input anti-leakage guard ring on printed circuit board layout.

LM108, LM108A, LM208, LM208A, LM308, LM308A

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted.)

Rating	Symbol	Value			Unit
		LM108, LM108A	LM208, LM208A	LM308, LM308A	
Power Supply Voltage	V_{CC}, V_{EE}	± 20	± 20	± 18	Vdc
Input Voltage (See Note 1)	V_I	± 15			Volts
Input Differential Current (See Note 2)	I_{ID}	± 10			mA
Output Short-Circuit Duration	t_S	Indefinite			
Operating Ambient Temperature Range	T_A	-55 to $+125$	-25 to $+85$	0 to $+70$	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to $+150$			$^\circ\text{C}$
Junction Temperature Metal, Ceramic Package	T_J	$+175$			$^\circ\text{C}$
Plastic Package		$+150$			

Note 1. For supply voltages less than ± 15 V, the maximum input voltage is equal to the supply voltage.

Note 2. The inputs are shunted with back-to-back diodes for over-voltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1.0 V is applied between the inputs unless some limiting resistance is used.

ELECTRICAL CHARACTERISTICS (Unless otherwise noted these specifications apply for supply voltages of $+5.0\text{ V} \leq V_{CC} \leq +20\text{ V}$ and $-5.0\text{ V} \geq V_{EE} \geq -20\text{ V}$, $T_A = +25^\circ\text{C}$.)

Characteristic	Symbol	LM108A LM208A			LM108 LM208			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	—	0.3	0.5	—	0.7	2.0	mV
Input Offset Current	I_{IO}	—	0.05	0.2	—	0.005	0.2	nA
Input Bias Current	I_{IB}	—	0.8	2.0	—	0.8	2.0	nA
Input Resistance	r_i	30	70	—	30	70	—	Megohms
Power Supply Currents $V_{CC} = +20\text{ V}$, $V_{EE} = -20\text{ V}$	I_{CC}, I_{EE}	—	± 0.3	± 0.6	—	± 0.3	± 0.6	mA
Large Signal Voltage Gain $V_{CC} = V_{EE} = +15\text{ V}$, $V_O = \pm 10\text{ V}$, $R_L \geq 10\text{ k}\Omega$	A_{VOL}	80	300	—	50	300	—	V/mV

The following specifications apply over the operating temperature range.

Input Offset Voltage	V_{IO}	—	—	1.0	—	—	3.0	mV
Input Offset Current	I_{IO}	—	—	0.4	—	—	0.4	nA
Average Temperature Coefficient of Input Offset Voltage $T_A(\text{min}) \leq T_A \leq T_A(\text{max})$	$\Delta V_{IO}/\Delta T$	—	1.0	5.0	—	3.0	15	$\mu\text{V}/^\circ\text{C}$
Average Temperature Coefficient of Input Offset Current	$\Delta I_{IO}/\Delta T$	—	0.5	2.5	—	0.5	2.5	$\text{pA}/^\circ\text{C}$
Input Bias Current	I_{IB}	—	—	3.0	—	—	3.0	nA
Large Signal Voltage Gain $V_{CC} = V_{EE} = +15\text{ V}$, $V_O = \pm 10\text{ V}$, $R_L = 10\text{ k}\Omega$	A_{VOL}	40	—	—	25	—	—	V/mV
Input Voltage Range $V_{CC} = V_{EE} = +15\text{ V}$	V_{IR}	± 13.5	—	—	± 13.5	—	—	V
Common-Mode Rejection Ratio	CMRR	96	110	—	85	100	—	dB
Power Supply Voltage Rejection Ratio	PSRR	96	100	—	80	96	—	dB
Output Voltage Range $V_{CC} = V_{EE} = +15\text{ V}$, $R_L = 10\text{ k}\Omega$	V_{OR}	± 13	± 14	—	± 13	± 14	—	V
Supply Current ($T_A = T_A(\text{max})$)	I_{CC}, I_{EE}	—	± 0.15	± 0.4	—	± 0.15	± 0.4	mA

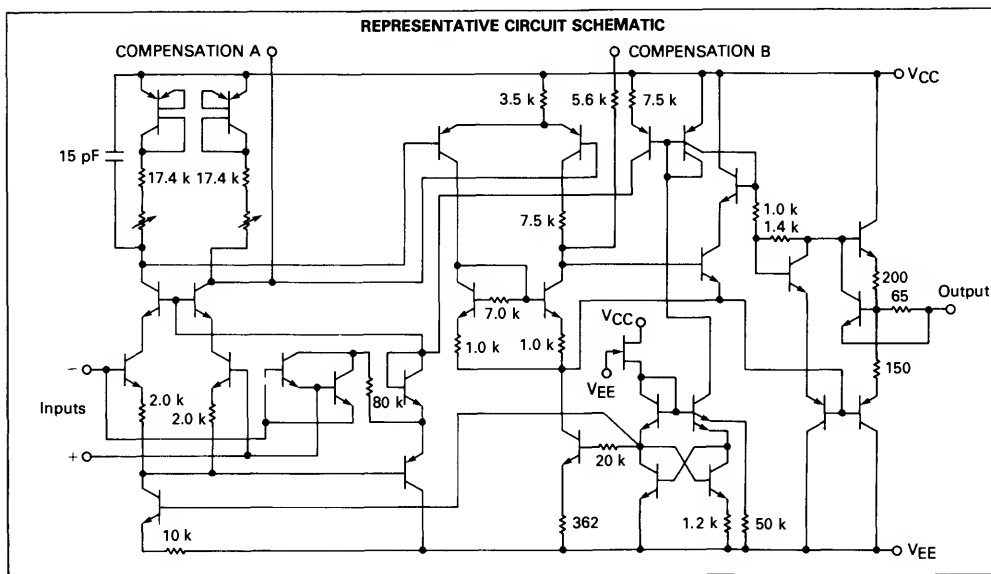
LM108, LM108A, LM208, LM208A, LM308, LM308A

ELECTRICAL CHARACTERISTICS (Unless otherwise noted these specifications apply for supply voltages of $+5.0\text{ V} \leq V_{CC} \leq +15\text{ V}$ and $-5.0\text{ V} \geq V_{EE} \geq -15\text{ V}$, $T_A = +25^\circ\text{C}$.)

Characteristic	Symbol	LM308A			LM308			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	—	0.3	0.5	—	2.0	7.5	mV
Input Offset Current	I_{IO}	—	0.2	1.0	—	0.2	1.0	nA
Input Bias Current	I_{IB}	—	1.5	7.0	—	1.5	7.0	nA
Input Resistance	r_i	10	40	—	10	40	—	Megohms
Power Supply Currents $V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$	I_{CC}, I_{EE}	—	± 0.3	± 0.8	—	± 0.3	± 0.8	mA
Large Signal Voltage Gain $V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $V_O = \pm 10\text{ V}$, $R_L \geq 10\text{ k}\Omega$	A_{VOL}	80	300	—	25	300	—	V/mV

The following specifications apply over the operating temperature range.

Input Offset Voltage	V_{IO}	—	—	0.73	—	—	10	mV
Input Offset Current	I_{IO}	—	—	1.5	—	—	1.5	nA
Average Temperature Coefficient of Input Offset Voltage $T_A(\text{min}) \leq T_A \leq T_A(\text{max})$	$\Delta V_{IO}/\Delta T$	—	1.0	5.0	—	6.0	30	$\mu\text{V}/^\circ\text{C}$
Average Temperature Coefficient of Input Offset Current	$\Delta I_{IO}/\Delta T$	—	2.0	10	—	2.0	10	$\text{pA}/^\circ\text{C}$
Input Bias Current	I_{IB}	—	—	10	—	—	10	nA
Large Signal Voltage Gain $V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $V_O = \pm 10\text{ V}$, $R_L \geq 10\text{ k}\Omega$	A_{VOL}	60	—	—	15	—	—	V/mV
Input Voltage Range $V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$	V_{IR}	± 14	—	—	± 14	—	—	V
Common-Mode Rejection Ratio $R_S \leq 50\text{ k}\Omega$	CMRR	96	110	—	80	100	—	dB
Supply Voltage Rejection Ratio $R_S \leq 50\text{ k}\Omega$	PSRR	96	110	—	80	96	—	dB
Output Voltage Range $V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $R_L = 10\text{ k}\Omega$	VOR	± 13	± 14	—	± 13	± 14	—	V



LM108, LM108A, LM208, LM208A, LM308, LM308A

TYPICAL CHARACTERISTICS

2

FIGURE 1 – INPUT BIAS AND INPUT OFFSET CURRENTS

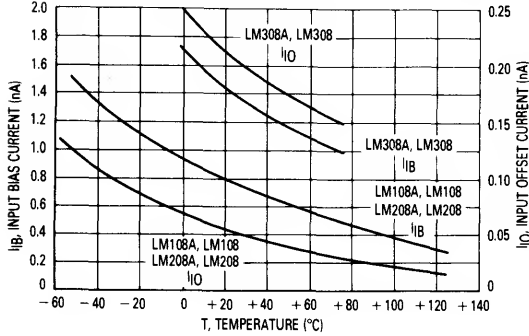


FIGURE 2 – MAXIMUM EQUIVALENT INPUT OFFSET VOLTAGE ERROR versus INPUT RESISTANCE

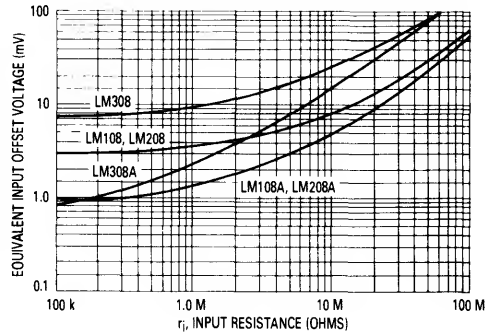


FIGURE 3 – VOLTAGE GAIN versus SUPPLY VOLTAGES

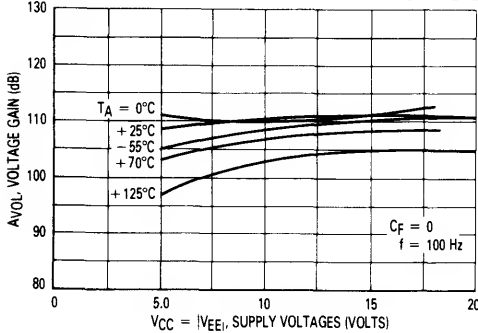


FIGURE 4 – POWER SUPPLY CURRENTS versus POWER SUPPLY VOLTAGE

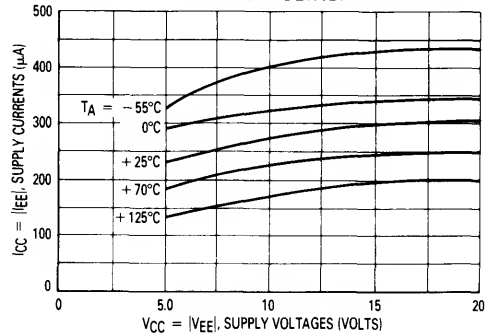


FIGURE 5 – OPEN-LOOP FREQUENCY RESPONSE

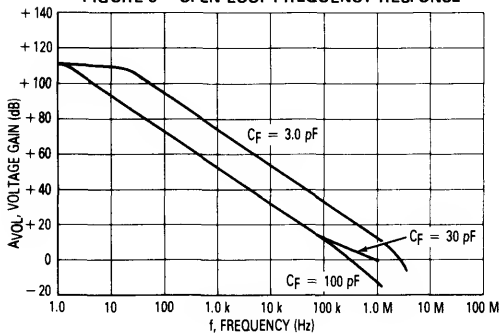
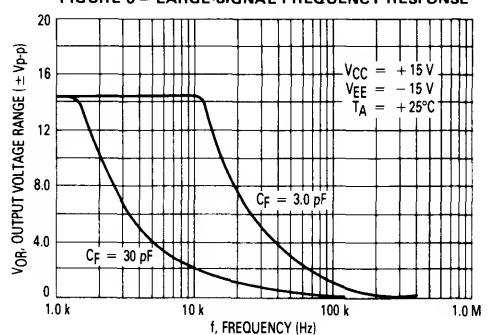


FIGURE 6 – LARGE-SIGNAL FREQUENCY RESPONSE



LM108, LM108A, LM208, LM208A, LM308, LM308A

SUGGESTED DESIGN APPLICATIONS

FIGURE 7 — FAST (1) SUMMING AMPLIFIER WITH LOW INPUT CURRENT

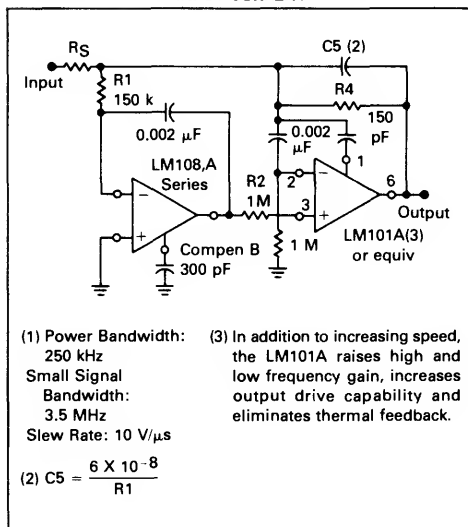


FIGURE 8 — SAMPLE AND HOLD

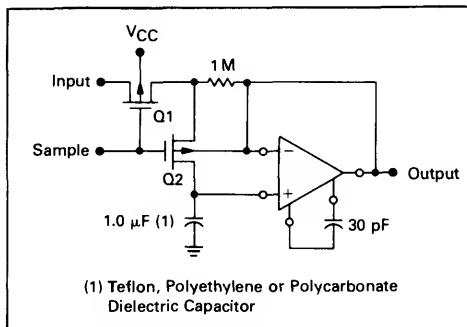
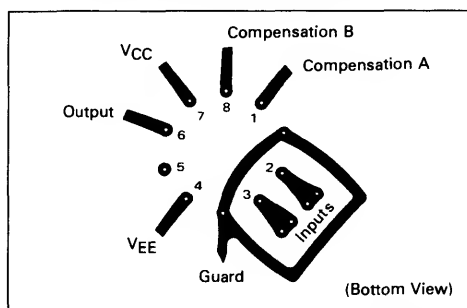


FIGURE 9 — SUGGESTED PRINTED CIRCUIT BOARD LAYOUT for INPUT GUARDING USING METAL PACKAGED DEVICE



INPUT GUARDING

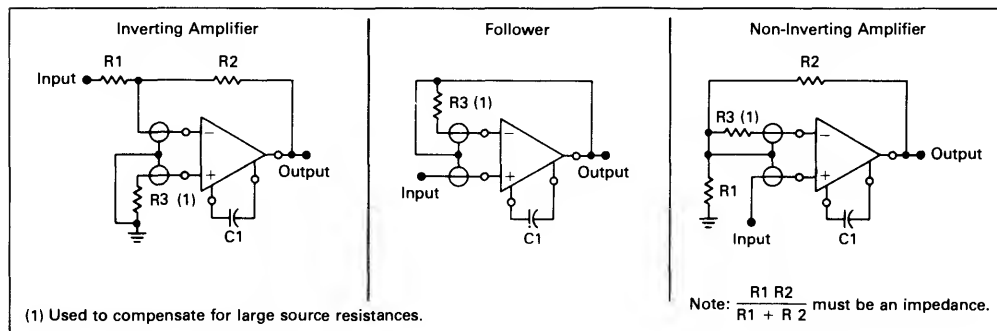
Special care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the LM108A amplifier series. Boards must be thoroughly cleaned with alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble at +125°C, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8-lead TO-99 type package is accomplished by using a 10-lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the boards. The

guard, which is a conductive ring surrounding the inputs, is connected to a low-impedance point that is at approximately the same voltage as the inputs. Leakage currents from high-voltage pins are then absorbed by the guard.

The pin configuration of the dual in-line package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard MC1741 and LM101A pin configuration).

FIGURE 10 — CONNECTION OF INPUT GUARDS



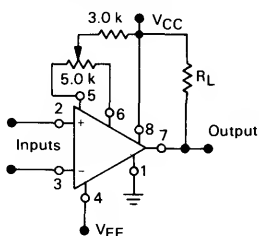
MOTOROLA SEMICONDUCTOR TECHNICAL DATA

HIGHLY FLEXIBLE VOLTAGE COMPARATORS

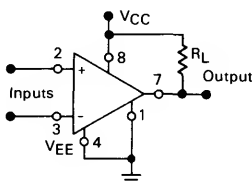
The ability to operate from a single power supply of 5.0 to 30 volts or ± 15 volt split supplies, as commonly used with operational amplifiers, makes the LM111/LM211/LM311 a truly versatile comparator. Moreover, the inputs of the device can be isolated from system ground while the output can drive loads referenced either to ground, the V_{CC} or the V_{EE} supply. This flexibility makes it possible to drive DTL, RTL, TTL, or MOS logic. The output can also switch voltages to 50 volts at currents to 50 mA. Thus the LM111/LM211/LM311 can be used to drive relays, lamps or solenoids.

TYPICAL COMPARATOR DESIGN CONFIGURATIONS

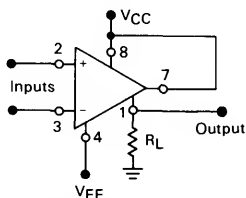
Split Power-Supply with Offset Balance



Single Supply

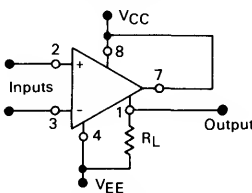


Ground-Referred Load



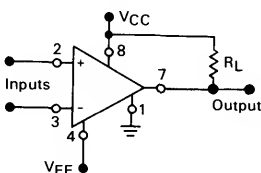
Input polarity is reversed when Gnd pin is used as an output

Load Referred to Negative Supply

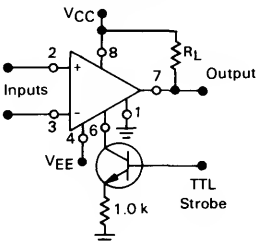


Input polarity is reversed when Gnd pin is used as an output.

Load Referred to Positive Supply



Strobe Capability

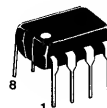
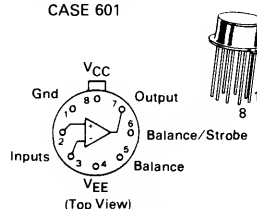


LM111 LM211 LM311

HIGH PERFORMANCE VOLTAGE COMPARATORS

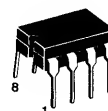
**SILICON MONOLITHIC
INTEGRATED CIRCUIT**

**H SUFFIX
METAL PACKAGE
CASE 601**

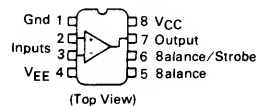


**N SUFFIX
PLASTIC PACKAGE
CASE 626
(LM311 Only)**

**J-8 SUFFIX
CERAMIC PACKAGE
CASE 693**



**D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)
(LM211/LM311 Only)**



ORDERING INFORMATION

Device	Temperature Range	Package
LM111H LM111J-8	-55°C to +125°C	Metal Can Ceramic DIP
LM211D LM211H LM211J-8	-25°C to +85°C	SO-8 Metal Can Ceramic DIP
LM311D LM311J-8 LM311N	0°C to +70°C	SO-8 Ceramic DIP Plastic DIP

LM111, LM211, LM311

2

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value		Unit
		LM111 LM211	LM311	
Total Supply Voltage	V _{CC} + V _{EE}	36	36	V _{dc}
Output to Negative Supply Voltage	V _O - V _{EE}	50	40	V _{dc}
Ground to Negative Supply Voltage	V _{EE}	30	30	V _{dc}
Input Differential Voltage	V _{ID}	±30	±30	V _{dc}
Input Voltage (Note 2)	V _{in}	±15	±15	V _{dc}
Voltage at Strobe Pin	—	V _{CC} to V _{CC} -5	V _{CC} to V _{CC} -5	V _{dc}
Power Dissipation and Thermal Characteristics				
Metal Package	P _D	680		mW
Derate above T _A = +25°C	1/θ _{JA}	5.5		mW/°C
Plastic and Ceramic Dual In-Line Packages	P _D	625		mW
Derate above T _A = +25°C	1/θ _{JA}	5.0		mW/°C
Operating Ambient Temperature Range	T _A	-55 to +125 -25 to +85 —	— — 0 to +70	°C
Operating Junction Temperature	T _{J(max)}	+150	+150	°C
Storage Temperature Range	T _{stg}	-65 to +150	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = -15 V, T_A = +25°C unless otherwise noted [Note 1].)

Characteristic	Symbol	LM111 LM211			LM311			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 3) R _S ≤ 50 kΩ, T _A = +25°C R _S ≤ 50 kΩ, T _{low} ≤ T _A ≤ T _{high} *	V _{IO}	—	0.7	3.0	—	2.0	7.5	mV
		—	—	4.0	—	—	10	
Input Offset Current (Note 3) T _A = +25°C T _{low} ≤ T _A ≤ T _{high} *	I _{IO}	—	1.7	10	—	1.7	50	nA
		—	—	20	—	—	70	
Input Bias Current, T _A = +25°C T _{low} ≤ T _A ≤ T _{high} *	I _{IB}	—	45	100	—	45	250	nA
		—	—	150	—	—	300	
Voltage Gain	A _V	40	200	—	40	200	—	V/mV
Response Time (Note 4)		—	200	—	—	200	—	ns
Saturation Voltage V _{ID} ≤ -5.0 mV, I _O = 50 mA } T _A = +25°C V _{ID} ≤ -10 mV, I _O = 50 mA } V _{CC} ≥ 4.5 V, V _{EE} = 0, T _{low} ≤ T _A ≤ T _{high} * V _{ID} ≤ -6.0 mV, I _{sink} ≤ 8.0 mA V _{ID} ≤ -10 mV, I _{sink} ≤ 8.0 mA	V _{OL}	—	0.75	1.5	—	—	—	V
		—	—	—	—	0.75	1.5	
		—	0.23	0.4	—	—	—	
		—	—	—	—	0.23	0.4	
Strobe "On" Current (Note 5)	I _S	—	3.0	—	—	3.0	—	mA
Output Leakage Current V _{ID} ≥ 5.0 mV, V _O = 35 V } T _A = +25°C V _{ID} ≥ 10 mV, V _O = 35 V } I _{strobe} = 3.0 mA V _{ID} ≥ 5.0 mV, V _O = 35 V, T _{low} ≤ T _A ≤ T _{high} *		—	0.2	10	—	—	—	nA
		—	—	—	—	0.2	50	nA
		—	0.1	0.5	—	—	—	μA
Input Voltage Range (T _{low} ≤ T _A ≤ T _{high} *)	V _{IR}	-14.5	-14.7 to 13.8	13.0	-14.5	-14.7 to 13.8	13.0	V
Positive Supply Current	I _{CC}	—	+2.4	+6.0	—	+2.4	+7.5	mA
Negative Supply Current	I _{EE}	—	-1.3	-5.0	—	-1.3	-5.0	mA

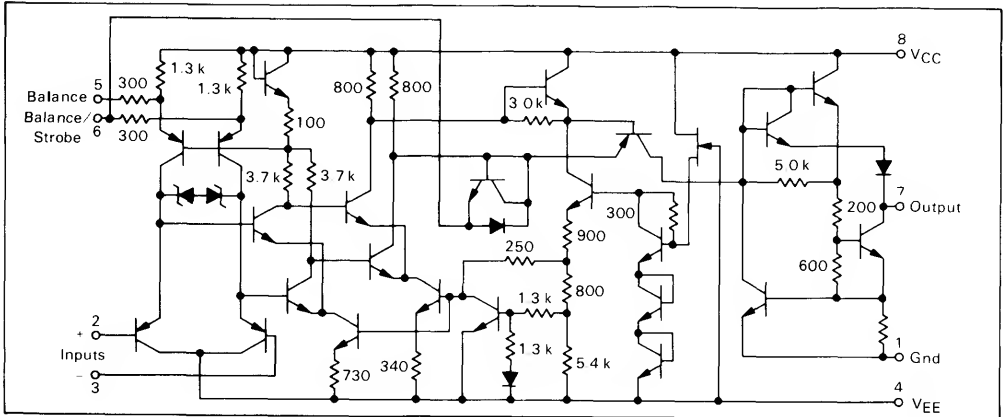
NOTES:

- * T_{low} = -55°C for LM111
= -25°C for LM211
= 0°C for LM311
- T_{high} = +125°C for LM111
= +85°C for LM211
= +70°C for LM311
- Offset voltage, offset current and bias current specifications apply for a supply voltage range from a single 5.0 volt supply up to ±15 volt supplies.
 - This rating applies for ±15 volt supplies. The positive input voltage limit is 30 volts above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30 volts below the positive supply, whichever is less.

- The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1.0 mA load. Thus, these parameters define an error band and take into account the "worst case" effects of voltage gain and input impedance.
- The response time specified is for a 100 mV input step with 5.0 mV overdrive.
- Do not short the strobe pin to ground; it should be current driven at 3.0 to 5.0 mA.

LM111, LM211, LM311

FIGURE 1 — CIRCUIT SCHEMATIC



TYPICAL PERFORMANCE CHARACTERISTICS

FIGURE 2 — INPUT BIAS CURRENT versus TEMPERATURE

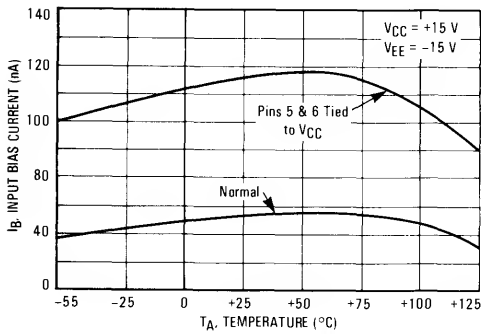


FIGURE 3 — INPUT OFFSET CURRENT versus TEMPERATURE

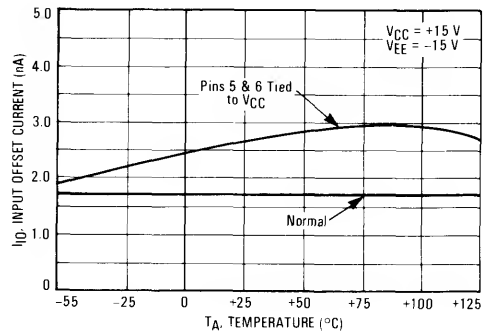


FIGURE 4 — INPUT BIAS CURRENT versus DIFFERENTIAL INPUT VOLTAGE

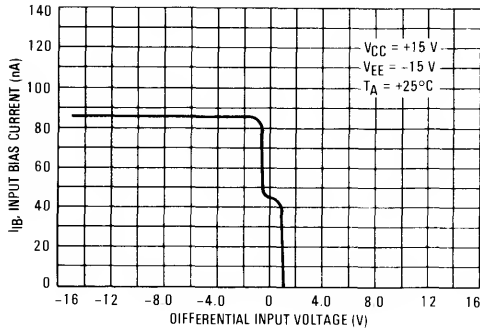
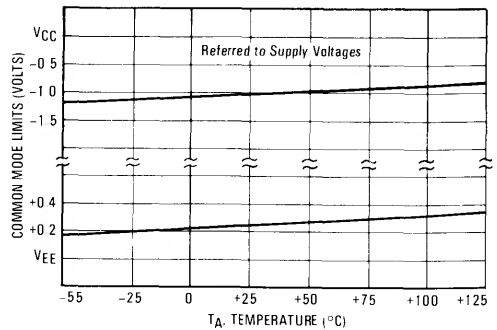


FIGURE 5 — COMMON MODE LIMITS versus TEMPERATURE



TYPICAL PERFORMANCE CHARACTERISTICS

FIGURE 6 — RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

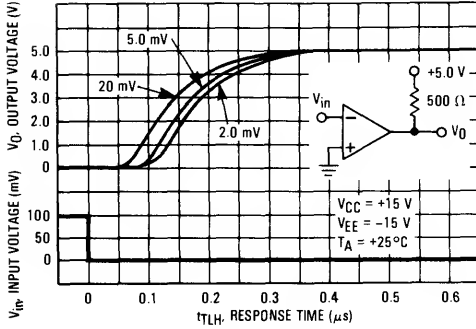


FIGURE 7 — RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

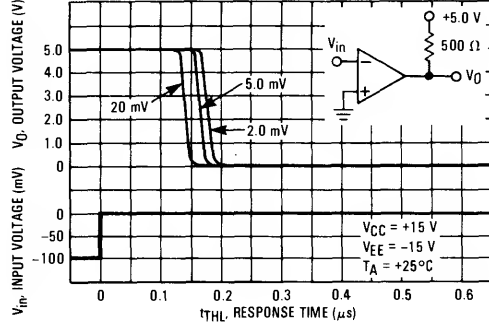


FIGURE 8 — RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

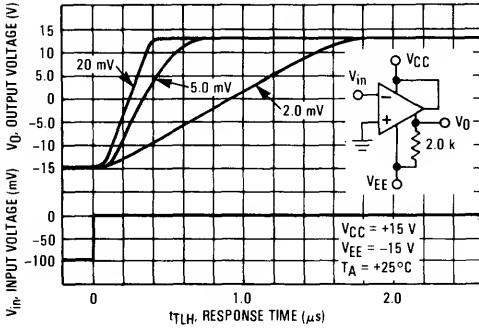


FIGURE 9 — RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

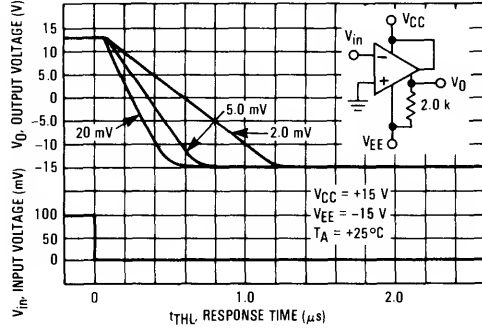


FIGURE 10 — OUTPUT SHORT CIRCUIT CURRENT CHARACTERISTICS AND POWER DISSIPATION

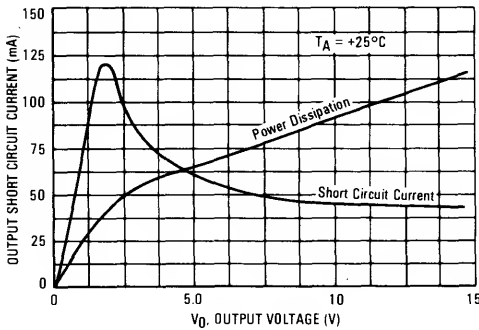
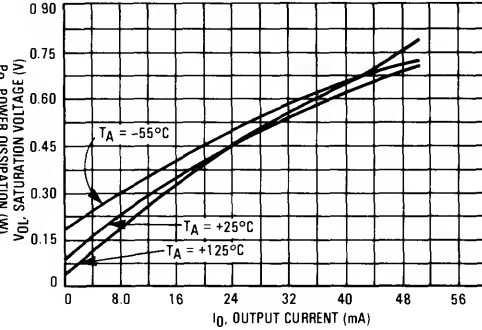


FIGURE 11 — OUTPUT SATURATION VOLTAGE versus OUTPUT CURRENT



LM111, LM211, LM311

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

FIGURE 12 — OUTPUT LEAKAGE CURRENT
versus TEMPERATURE

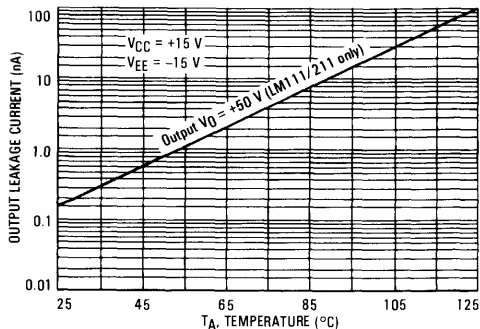


FIGURE 13 — POWER SUPPLY CURRENT
versus SUPPLY VOLTAGE

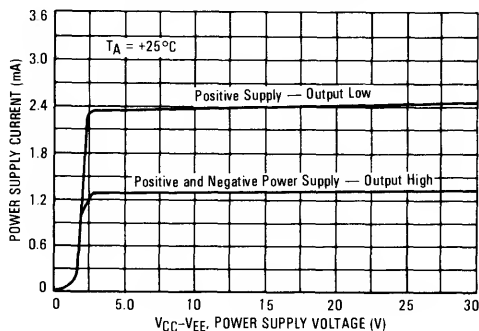
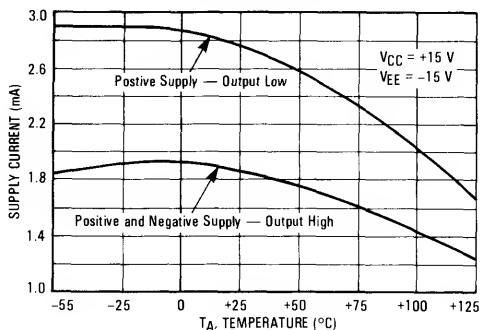


FIGURE 14 — POWER SUPPLY CURRENT versus
TEMPERATURE



APPLICATIONS INFORMATION

FIGURE 15 — IMPROVED METHOD OF ADDING
HYSTERESIS WITHOUT APPLYING POSITIVE
FEEDBACK TO THE INPUTS

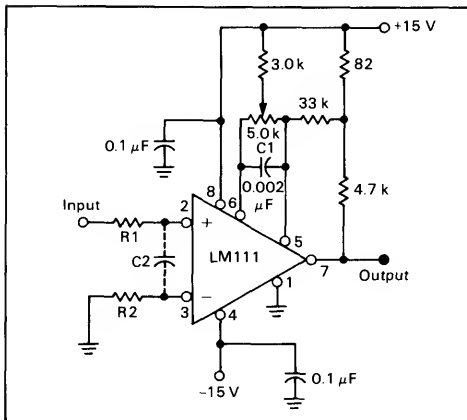
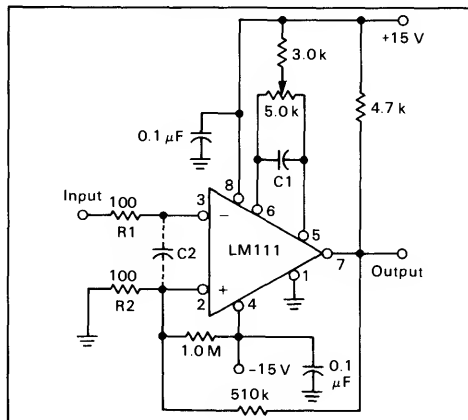


FIGURE 16 — CONVENTIONAL TECHNIQUE FOR
ADDING HYSTERESIS



APPLICATIONS INFORMATION

Techniques for Avoiding Oscillations in Comparator Applications

2

When a high-speed comparator such as the LM111 is used with high-speed input signals and low source impedances, the output response will normally be fast and stable, providing the power supplies have been bypassed (with 0.1 μF disc capacitors), and that the output signal is routed well away from the inputs (Pins 2 and 3) and also away from Pins 5 and 6.

However, when the input signal is a voltage ramp or a slow sine wave, or if the signal source impedance is high (1.0 k Ω to 100 k Ω), the comparator may burst into oscillation near the crossing-point. This is due to the high gain and wide bandwidth of comparators like the LM111 series. To avoid oscillation or instability in such a usage, several precautions are recommended, as shown in Figure 15.

The trim pins (Pins 5 and 6) act as unwanted auxiliary inputs. If these pins are not connected to a trim-pot, they should be shorted together. If they are connected to a trim-pot, a 0.01 μF capacitor (C1) between Pins 5 and 6 will minimize the susceptibility to ac coupling. A smaller capacitor is used if Pin 5 is used for positive feedback as in Figure 15.

Certain sources will produce a cleaner comparator output waveform if a 100 pF to 1000 pF capacitor (C2) is connected directly across the input pins. When the signal source is applied through a resistive network, R1, it is usually advantageous to choose R2 of the same value, both for dc and for dynamic (ac) considerations. Carbon, tin-oxide, and metal-film resistors have all been used with good results in comparator input circuitry, but inductive wirewound resistors should be avoided.

When comparator circuits use input resistors (e.g., summing resistors), their value and placement are particularly important. In all cases the body of the resistor should be close to the device or socket. In other words, there should be a very short lead length or printed-circuit foil run between comparator and resistor to radiate or pick up signals. The same applies to capacitors, pots, etc. For example, if R1 = 10 k Ω , as little as 5 inches of lead between the resistors and the input pins can result in oscillations that are very hard to dampen. Twisting these input leads tightly is the best alternative to placing resistors close to the comparator.

Since feedback to almost any pin of a comparator can result in oscillation, the printed-circuit layout should be engineered thoughtfully. Preferably there should be a groundplane under the LM111 circuitry (e.g., one side of a double layer printed circuit board). Ground, positive supply or negative supply foil should extend between the output and the inputs, to act as a guard. The foil connections for the inputs should be as small and compact as possible, and should be essentially surrounded by ground foil on all sides, to guard against capacitive coupling from any fast high-level signals (such as the output). If Pins 5 and 6 are not used, they should be shorted together. If they are connected to a trim-pot, the trim-pot should be located no more than a few inches away from the LM111, and a 0.01 μF capacitor should be installed across Pins 5 and 6. If this capacitor cannot be used, a shielding printed-circuit foil may be advisable between Pins 6 and 7. The power supply bypass capacitors should be located within a couple inches of the LM111.

A standard procedure is to add hysteresis to a comparator to prevent oscillation, and to avoid excessive noise on the output. In the circuit of Figure 16, the feedback resistor of 510 k Ω from the output to the positive input will cause about 3.0 mV of hysteresis. However, if R2 is larger than 100 Ω , such as 50 k Ω , it would not be practical to simply increase the value of the positive feedback resistor proportionally above 510 k Ω to maintain the same amount of hysteresis.

When both inputs of the LM111 are connected to active signals, or if a high-impedance signal is driving the positive input of the LM111 so that positive feedback would be disruptive, the circuit of Figure 15 is ideal. The positive feedback is applied to Pin 5 (one of the offset adjustment pins). This will be sufficient to cause 1.0 to 2.0 mV hysteresis and sharp transitions with input triangle waves from a few Hz to hundreds of kHz. The positive-feedback signal across the 82 Ω resistor swings 240 mV below the positive supply. This signal is centered around the nominal voltage at Pin 5, so this feedback does not add to the offset voltage of the comparator. As much as 8.0 mV of offset voltage can be trimmed out, using the 5.0 k Ω pot and 3.0 k Ω resistor as shown.

FIGURE 17 — ZERO-CROSSING DETECTOR DRIVING CMOS LOGIC

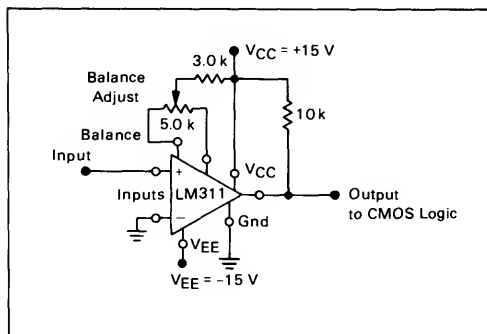
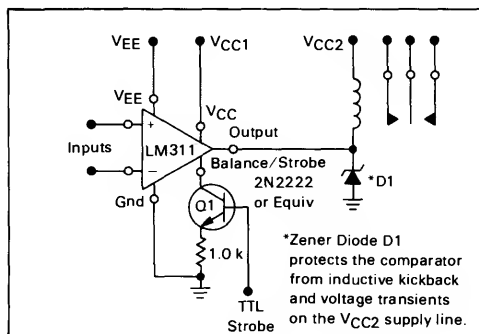


FIGURE 18 — RELAY DRIVER WITH STROBE CAPABILITY



QUAD LOW POWER OPERATIONAL AMPLIFIERS

The LM124 Series are low-cost, quad operational amplifiers with true differential inputs. These have several distinct advantages over standard operational amplifier types in single supply applications. The quad amplifier can operate at supply voltages as low as 3.0 Volts or as high as 32 Volts with quiescent currents about one fifth of those associated with the MC1741 (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

- Short Circuited Protected Outputs
- True Differential Input Stage
- Single Supply Operation: 3.0 to 32 Volts
- Low Input Bias Currents: 100 nA Max (LM324A)
- Four Amplifiers Per Package
- Internally Compensated
- Common Mode Range Extends to Negative Supply
- Industry Standard Pinouts

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	LM124 LM224 LM324A	LM2902	Unit
Power Supply Voltages				Vdc
Single Supply	V_{CC}	32	26	
Split Supplies	V_{CC}, V_{EE}	± 16	± 13	
Input Differential Voltage Range (1)	V_{IDR}	± 32	± 26	Vdc
Input Common Mode Voltage Range	V_{ICR}	-0.3 to 32	-0.3 to 26	Vdc
Input Forward Current (2)	I_{IF}	50	—	mA
		$(V_I < -0.3 \text{ V})$		
Output Short Circuit Duration	t_S	Continuous		
Junction Temperature	T_J			$^\circ\text{C}$
Ceramic Package		175		
Plastic Packages		150		
Storage Temperature Range	T_{stg}			$^\circ\text{C}$
Ceramic Package		-65 to +150		
Plastic Packages		-55 to +125		
Operating Ambient Temperature Range	T_A			$^\circ\text{C}$
LM124		-55 to +125	—	
LM224		-25 to +85	—	
LM324		0 to +70	—	
LM324A		0 to +70	—	
LM2902		—	-40 to +105	

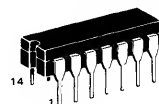
NOTES:

- (1) Split Power Supplies.
- (2) This input current will only exist when the voltage is negative at any of the input leads.
 Normal output states will reestablish when the input voltage returns to a voltage greater than -0.3 V.

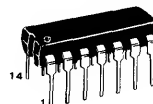
LM124, LM224, LM324, LM324A LM2902

QUAD DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUIT



J SUFFIX
 CERAMIC PACKAGE
 CASE 632

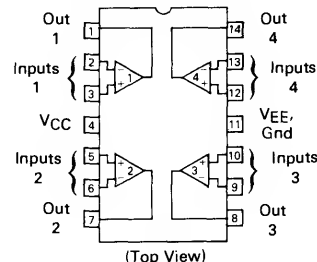


N SUFFIX
 PLASTIC PACKAGE
 CASE 646
 (LM224, LM324,
 LM2902 Only)



D SUFFIX
 PLASTIC PACKAGE
 CASE 751A
 (SO-14)

PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
LM124J	-55 to +125 $^\circ\text{C}$	Ceramic DIP
LM2902D	-40 to +105	SO-14
LM2902N		Plastic DIP
LM2902J	-40 to +85 $^\circ\text{C}$	Ceramic DIP
LM224D	-25 to +85 $^\circ\text{C}$	SO-14
LM224J		Ceramic DIP
LM224N	0 to +70 $^\circ\text{C}$	Plastic DIP
LM324AD		SO-14
LM324AN		Plastic DIP
LM324D		SO-14
LM324J		Ceramic DIP
LM324N		Plastic DIP

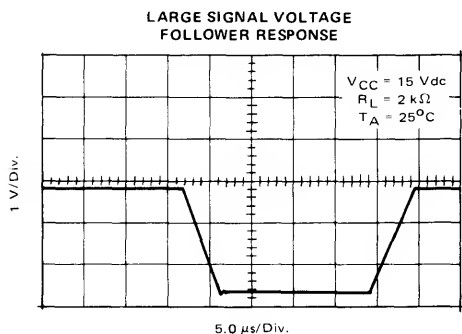
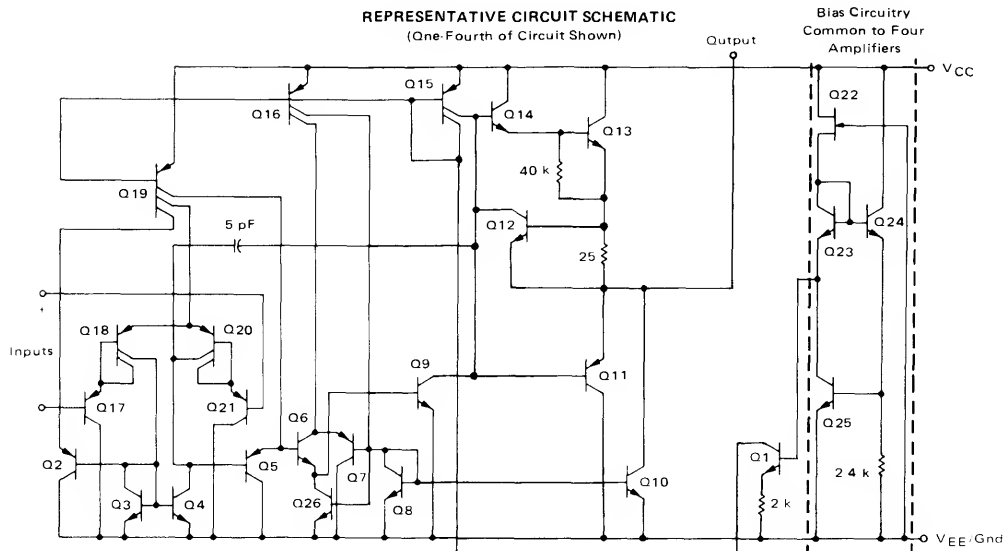
ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0\text{ V}$, $V_{EE} = \text{Gnd}$, $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	LM124/LM224		LM324A		LM324		LM2902		Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	
Input Offset Voltage $V_{CC} = 5.0\text{ V}$ to 30 V (26 V for LM2902), $V_{ICR} = 0\text{ V}$ to $V_{CC} - 1.7\text{ V}$, $V_O = 1.4\text{ V}$, $R_S = 0\ \Omega$ $T_A = 25^\circ\text{C}$ $T_A = T_{\text{High}}$ to T_{Low} (Note 1)	V_{IO}	—	2.0	5.0	—	2.0	3.0	—	2.0	mV
Average Temperature Coefficient of Input Offset Voltage $T_A = T_{\text{High}}$ to T_{Low} (Note 1)	$\Delta V_{IO}/\Delta T$	—	7.0	—	—	7.0	30	—	7.0	$\mu\text{V}/^\circ\text{C}$
Input Offset Current $T_A = T_{\text{High}}$ to T_{Low} (Note 1)	I_{IO}	—	3.0	30	—	5.0	30	—	5.0	nA
Average Temperature Coefficient of Input Offset Current $T_A = T_{\text{High}}$ to T_{Low} (Note 1)	$\Delta I_{IO}/\Delta T$	—	—	100	—	—	75	—	—	pA/ $^\circ\text{C}$
Input Bias Current $T_A = T_{\text{High}}$ to T_{Low} (Note 1)	I_{IB}	—	—90	—150	—	—45	—100	—	—90	nA
Input Common-Mode Voltage Range (Note 2) $V_{CC} = 30\text{ V}$ (26 V for LM2902) $V_{CC} = 30\text{ V}$ (26 V for LM2902), $T_A = T_{\text{High}}$ to T_{Low}	V_{ICR}	0	28.3	0	28.3	0	28.3	0	28.3	V
Differential Input Voltage Range Large Signal Open-Loop Voltage Gain $R_L = 2.0\text{ k}\Omega$, $V_{CC} = 15\text{ V}$, For Large V_O Swing, $T_A = T_{\text{High}}$ to T_{Low} (Note 1)	V_{IDR}	—	—	VCC	—	VCC	—	VCC	—	V
Channel Separation $1.0\text{ kHz} \leq f \leq 20\text{ kHz}$, Input Referenced	A_{VOL}	50	100	—	25	100	—	25	100	V/mV
Common-Mode Rejection Ratio $R_S \leq 10\text{ k}\Omega$	CMRR	70	85	—	65	70	—	65	70	dB
Power Supply Rejection Ratio	PSRR	65	100	—	65	100	—	65	100	dB
Output Voltage Range $R_L = 2.0\text{ k}\Omega$ ($R_L \geq 10\text{ k}\Omega$ for LM2902)	VOR	0	—	3.3	0	—	3.3	0	—	V
Output Voltage — High Limit ($T_A = T_{\text{High}}$ to T_{Low}) (Note 1) $V_{CC} = 30\text{ V}$ (26 V for LM2902), $R_L = 2.0\text{ k}\Omega$ $V_{CC} = 30\text{ V}$ (26 V for LM2902), $R_L = 10\text{ k}\Omega$	V_{OH}	26	—	—	26	—	—	26	—	V
Output Voltage — Low Limit $V_{CC} = 5.0\text{ V}$, $R_L = 10\text{ k}\Omega$, $T_A = T_{\text{High}}$ to T_{Low} (Note 1)	V_{OL}	—	5.0	20	—	5.0	20	—	5.0	mV
Output Source Current ($V_{ID} = +1.0\text{ V}$, $V_{CC} = 15\text{ V}$) $T_A = 25^\circ\text{C}$ $T_A = T_{\text{High}}$ to T_{Low} (Note 1)	I_{O+}	20	40	—	20	40	—	20	40	mA
Output Sink Current ($V_{ID} = -1.0\text{ V}$, $V_{CC} = 15\text{ V}$) $T_A = 25^\circ\text{C}$ $T_A = T_{\text{High}}$ to T_{Low} (Note 1) $V_{ID} = -1.0\text{ V}$, $V_O = 200\text{ mV}$, $T_A = 25^\circ\text{C}$	I_{O-}	10	20	—	10	20	—	10	20	mA
Output Short Circuit to Ground (Note 3) Power Supply Current ($T_A = T_{\text{High}}$ to T_{Low}) (Note 1) $V_{CC} = 30\text{ V}$ (26 V for LM2902), $V_O = 0\text{ V}$, $R_L = \infty$ $V_{CC} = 5.0\text{ V}$, $V_O = 0\text{ V}$, $R_L = \infty$	I_{OS}	—	40	60	—	40	60	—	40	mA
	I_{CC}	—	—	3.0	—	1.4	3.0	—	—	mA
		—	—	1.2	—	0.7	1.2	—	—	1.2

NOTES:

- (1) $T_{\text{Low}} = -55^\circ\text{C}$ for LM124
 $T_{\text{Low}} = -40^\circ\text{C}$ for LM2902
 $T_{\text{Low}} = -25^\circ\text{C}$ for LM224
 $T_{\text{Low}} = 0^\circ\text{C}$ for LM324,A
- $T_{\text{High}} = +125^\circ\text{C}$ for LM124
 $T_{\text{High}} = +85^\circ\text{C}$ for LM224
 $T_{\text{High}} = +70^\circ\text{C}$ for LM324,A
 $T_{\text{High}} = +105^\circ\text{C}$ for LM2902

- (2) The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V . The upper end of the common-mode voltage range is $V_{CC} - 1.7\text{ V}$.
- (3) Short circuits from the output to V_{CC} can cause excessive heating and eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

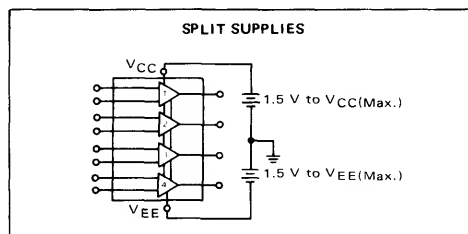
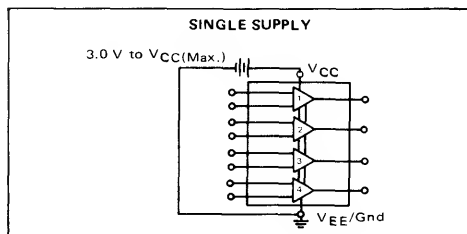


CIRCUIT DESCRIPTION

The LM124 Series is made using four internally compensated, two-stage operational amplifiers. The first stage

of each consists of differential input devices Q20 and Q18 with input buffer transistors Q21 and Q17 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance a smaller compensation capacitor (only 5 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q20 and Q18. Another feature of this input stage is that the input common-mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single-ended converter. The second stage consists of a standard current source load amplifier stage.

Each amplifier is biased from an internal-voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.



LM124, LM224, LM324,A, LM2902

TYPICAL PERFORMANCE CURVES

FIGURE 1 – INPUT VOLTAGE RANGE

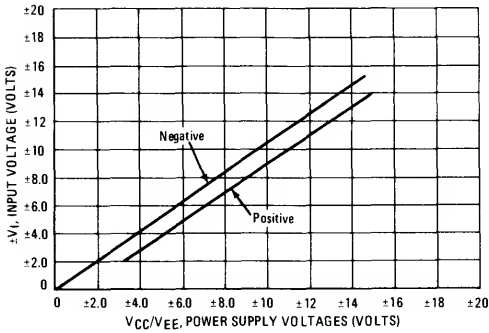


FIGURE 2 – OPEN LOOP FREQUENCY

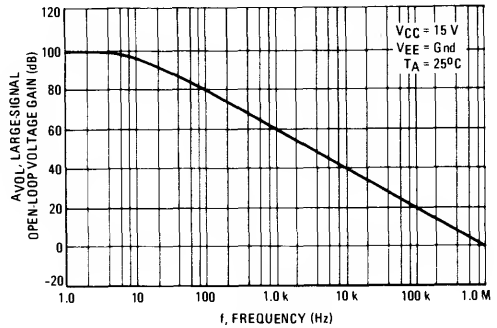


FIGURE 3 – LARGE-SIGNAL FREQUENCY RESPONSE

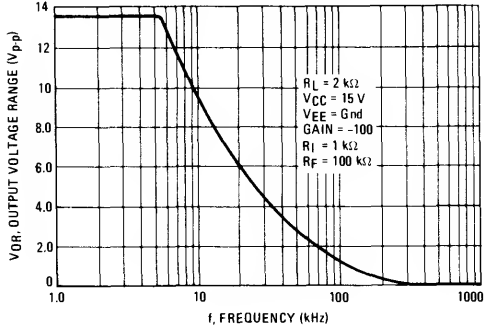


FIGURE 4 – SMALL-SIGNAL VOLTAGE FOLLOWER PULSE RESPONSE (Non-Inverting)

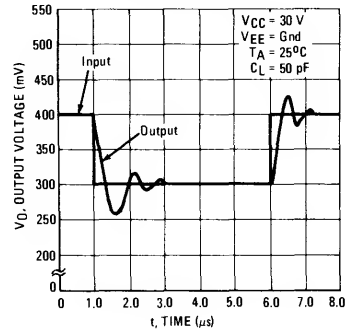


FIGURE 5 – POWER SUPPLY CURRENT versus POWER SUPPLY VOLTAGE

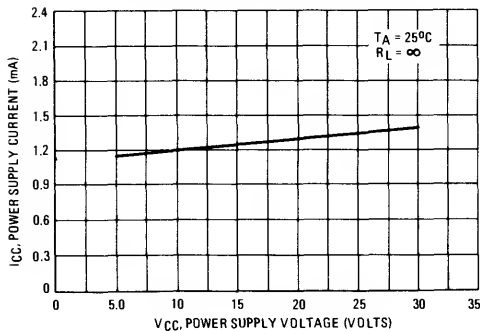
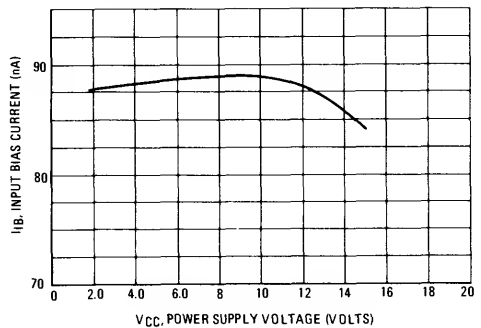


FIGURE 6 – INPUT BIAS CURRENT versus SUPPLY VOLTAGE



LM124, LM224, LM324,A, LM2902

APPLICATIONS INFORMATION

2

FIGURE 7 – VOLTAGE REFERENCE

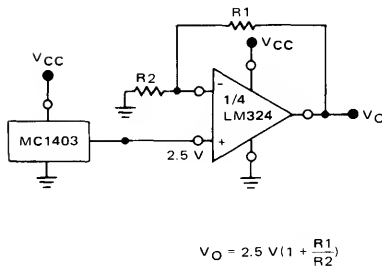


FIGURE 8 – WIEN BRIDGE OSCILLATOR

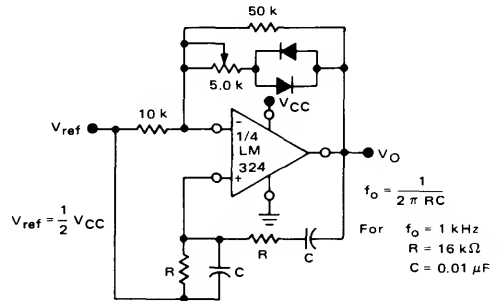


FIGURE 9 – HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER

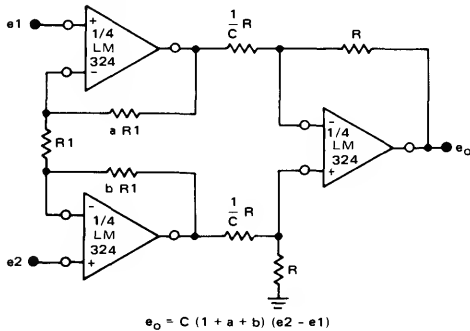


FIGURE 10 – COMPARATOR WITH HYSTERESIS

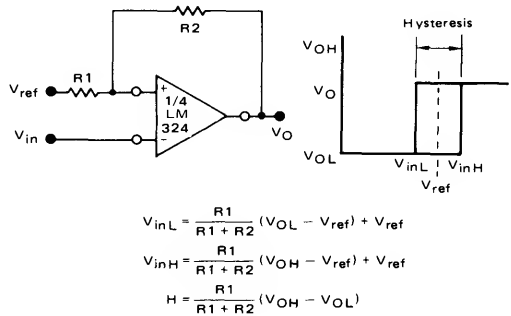
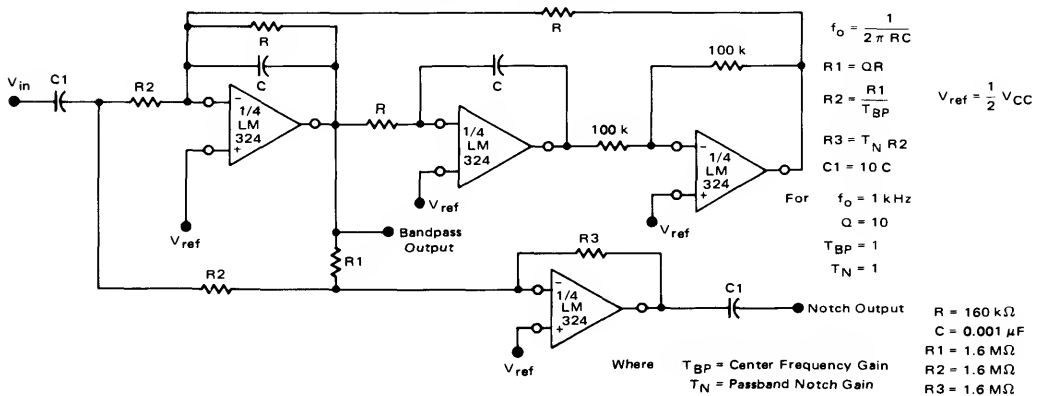


FIGURE 11 – BI-QUAD FILTER



LM124, LM224, LM324,A, LM2902

APPLICATIONS INFORMATION (continued)

FIGURE 12 – FUNCTION GENERATOR

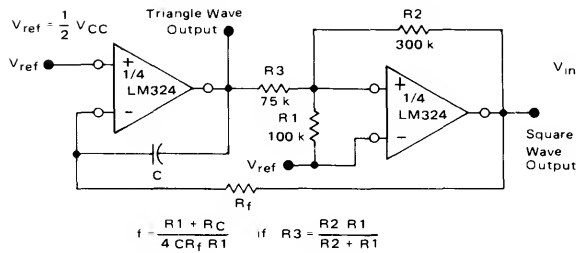
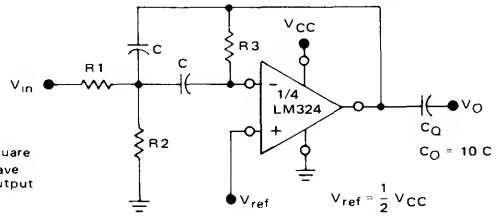


FIGURE 13 – MULTIPLE FEEDBACK BANDPASS FILTER



Given f_0 = Center Frequency
 $A(f_0)$ = Gain at Center Frequency

Choose Value f_0 , C
 Then

$$R_3 = \frac{Q}{\pi f_0 C}$$

$$R_1 = \frac{R_3}{2 A(f_0)}$$

$$R_2 = \frac{R_1 R_3}{4 Q^2 R_1 - R_3}$$

For less than 10% error from operational amplifier

$$\frac{Q_0 f_0}{BW} < 0.1 \quad \text{Where } f_0 \text{ and BW are expressed in Hz.}$$

If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

QUAD SINGLE SUPPLY COMPARATORS

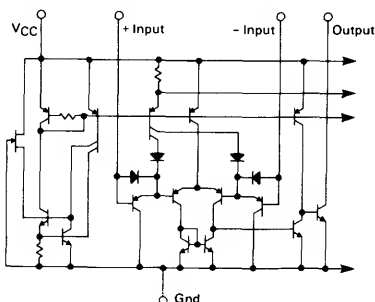
These comparators are designed for use in level detection, low-level sensing and memory applications in Consumer Automotive and Industrial electronic applications.

- Single or Split Supply Operation
- Low Input Bias Current — 25 nA (Typ)
- Low Input Offset Current — ± 5.0 nA (Typ)
- Low Input Offset Voltage — ± 1.0 mV (Typ LM139A Series)
- Input Common-Mode Voltage Range to Gnd
- Low Output Saturation Voltage — 130 mV (Typ) @ 4.0 mA
- TTL and CMOS Compatible

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage LM139, A/LM239, A/LM339A/LM2901 MC3302	V _{CC}	+36 or ± 18 +30 or ± 15	Vdc
Input Differential Voltage Range LM139, A/LM239, A/LM339, A/LM2901 MC3302	V _{IDR}	36 30	Vdc
Input Common Mode Voltage Range	V _{ICR}	-0.3 to V _{CC}	Vdc
Output Short-Circuit to Gnd (Note 1)	I _{SC}	Continuous	
Input Current (V _{in} < -0.3 Vdc) (Note 2)	I _{in}	50	mA
Power Dissipation @ T _A = 25°C	P _D	1.0	Watts
Ceramic Package		8.0	mW/°C
Plastic Package		1.0	Watts
Derate above 25°C		8.0	mW/°C
Junction Temperature	T _J	175	°C
Ceramic & Metal Package		150	
Operating Ambient Temperature Range	T _A	-55 to +125 -25 to +85 -40 to +85 -40 to +105 0 to +70	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

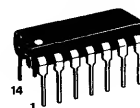
FIGURE 1 — CIRCUIT SCHEMATIC (Diagram shown is for 1 comparator)



LM139, A LM239, A LM2901 LM339, A MC3302

QUAD COMPARATORS

SILICON MONOLITHIC INTEGRATED CIRCUIT



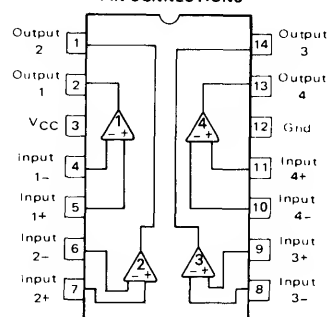
N, P SUFFIX
PLASTIC PACKAGE
CASE 646

J, L SUFFIX
CERAMIC PACKAGE
CASE 632



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
LM139J, AJ	-55°C to +125°C	Ceramic DIP
LM239D, AD		SO-14
LM239J, AJ	-25°C to +85°C	Ceramic DIP
LM239N, AN		Plastic DIP
LM339D, AD		SO-14
LM339J, AJ	0°C to +70°C	Ceramic DIP
LM339N, AN		Plastic DIP
LM2901D		SO-14
LM2901N	-40°C to +105°C	Plastic DIP
MC3302L		Ceramic DIP
MC3302P	-40°C to +85°C	Plastic DIP

ELECTRICAL CHARACTERISTICS ($V_{CC} = +5.0$ Vdc, $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	LM139A			LM239A/339A			LM139			LM239/339			LM2901			MC3302			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 4)	V_{IO}	—	+1.0	+2.0	—	+1.0	+2.0	—	+2.0	+5.0	—	+2.0	+5.0	—	+2.0	+7.0	—	+3.0	+20	mVdc
Input Bias Current (Notes 4, 5) (Output in Linear Range)	I_{IB}	—	25	100	—	25	250	—	25	100	—	25	250	—	25	250	—	25	500	nA
Input Offset Current (Note 4)	I_{IO}	—	+3.0	+25	—	+5.0	+50	—	+3.0	+25	—	+5.0	+50	—	+5.0	+50	—	+3.0	+100	nA
Input Common-Mode Voltage Range	V_{ICR}	0	—	$V_{CC} - 1.5$	0	—	$V_{CC} - 1.5$	0	—	$V_{CC} - 1.5$	0	—	$V_{CC} - 1.5$	0	—	$V_{CC} - 1.5$	0	—	$V_{CC} - 1.5$	V
Supply Current $R_L = \infty$ (For All Comparators) $R_L = \infty$, $V_{CC} = 30$ Vdc	I_{CC}	—	0.8	2.0	—	0.8	2.0	—	0.8	2.0	—	0.8	2.0	—	0.8	2.0	—	0.8	2.0	mA
Voltage Gain $R_L \geq 15$ k Ω , $V_{CC} = 15$ Vdc	A_V	50	200	—	50	200	—	200	—	—	200	—	—	25	100	—	2	30	—	V/mV
Large Signal Response Time $V_i = \text{TTL Logic Swing}$ $V_o = 1.4$ Vdc, $V_{RL} = 5.0$ Vdc, $R_L = 5.1$ k Ω	—	—	300	—	—	300	—	300	—	—	300	—	—	300	—	—	—	300	—	ns
Response Time (Note 6) $V_{RL} = 5.0$ Vdc, $R_L = 5.1$ k Ω	—	—	1.3	—	—	1.3	—	—	1.3	—	—	1.3	—	—	1.3	—	—	1.3	—	μs
Output Sink Current $V_i(-) \geq +1.0$ Vdc, $V_i(+)=0$, $V_O \leq 1.5$ Vdc	I_{sink}	6.0	16	—	6.0	18	—	6.0	18	—	6.0	16	—	6.0	16	—	6.0	16	—	mA
Saturation Voltage $V_i(+)=+1.0$ Vdc, $V_i(-)=0$, $I_{sink} \leq 4.0$ mA	V_{set}	—	130	400	—	130	400	—	130	400	—	130	400	—	130	400	—	130	500	mV
Output Leakage Current $V_i(+)=+1.0$ Vdc, $V_i(-)=0$, $V_O = +5.0$ Vdc	I_{OL}	—	0.1	—	—	0.1	—	—	0.1	—	—	0.1	—	—	0.1	—	—	0.1	—	nA

PERFORMANCE CHARACTERISTICS ($V_{CC} = +5.0$ Vdc, $T_A = T_{low}$ to T_{high} (Note 3))

Characteristic	Symbol	LM139A			LM239A/339A			LM139			LM239/339			LM2901			MC3302			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 4)	V_{IO}	—	—	+4.0	—	—	+4.0	—	—	+9.0	—	—	+9.0	—	—	+15	—	—	+40	mVdc
Input Bias Current (Notes 4, 5) (Output in Linear Range)	I_{IB}	—	—	300	—	—	400	—	—	300	—	—	400	—	—	500	—	—	1000	nA
Input Offset Current (Note 4)	I_{IO}	—	—	+100	—	—	+150	—	—	+100	—	—	+150	—	—	+200	—	—	+300	nA
Input Common-Mode Voltage Range	V_{ICR}	0	—	$V_{CC} - 2.0$	0	—	$V_{CC} - 2.0$	0	—	$V_{CC} - 2.0$	0	—	$V_{CC} - 2.0$	0	—	$V_{CC} - 2.0$	0	—	$V_{CC} - 2.0$	V
Saturation Voltage $V_i(-) \geq +1.0$ Vdc, $V_i(+)=0$, $I_{sink} \leq 4.0$ mA	V_{set}	—	—	700	—	—	700	—	—	700	—	—	700	—	—	700	—	—	700	mV
Output Leakage Current $V_i(+)=+1.0$ Vdc, $V_i(-)=0$, $V_O = 30$ Vdc	I_{OL}	—	—	1.0	—	—	1.0	—	—	1.0	—	—	1.0	—	—	1.0	—	—	1.0	μA
Differential Input Voltage All $V_i \geq 0$ Vdc	V_{ID}	—	—	V_{CC}	—	—	V_{CC}	—	—	V_{CC}	—	—	V_{CC}	—	—	V_{CC}	—	—	V_{CC}	Vdc

NOTES:

1. The maximum output current may be as high as 20 mA, independent of the magnitude of V_{CC} . Output short circuits to V_{CC} can cause excessive heating and eventual destruction.
2. The magnitude of input current will only occur if the leads are driven more negative than ground or the negative supply voltage. This is due to the input PNP collector-base junction becoming forward biased, acting as an input clamp diode. There is also a lateral PNP parasitic transistor action which can cause the output voltage of the comparators to go to the V_{CC} voltage level (or ground if overdrive is large) during the time that an input is driven negative. This will not destroy the device when limited to the max rating and normal output states will recover when the inputs become \geq ground or negative supply.
3. LM139/39A — $T_{low} = -55^\circ\text{C}$, $T_{high} = +125^\circ\text{C}$
LM239/239A — $T_{low} = -25^\circ\text{C}$, $T_{high} = +85^\circ\text{C}$
LM339/339A — $T_{low} = -40^\circ\text{C}$, $T_{high} = +105^\circ\text{C}$
LM2901 — $T_{low} = -40^\circ\text{C}$, $T_{high} = +105^\circ\text{C}$
MC3302 — $T_{low} = -25^\circ\text{C}$, $T_{high} = +85^\circ\text{C}$
4. At the output switch point, $V_O = 1.4$ Vdc, $R_S \leq 100 \Omega$, 5.0 Vdc $\leq V_{CC} \leq 30$ Vdc, with the inputs over the full common-mode range (0 Vdc to $V_{CC} - 1.5$ Vdc).
5. The bias current flows out of the inputs due to the PNP input stage. This current is virtually constant, independent of the output state.
6. The response time specified is for a 100 mV input step with 5.0 mV overdrive. For larger signals, 300 ns is typical.

LM139,A, LM239,A, LM339,A, LM2901, MC3302

2

FIGURE 2 — INVERTING COMPARATOR WITH HYSTERESIS

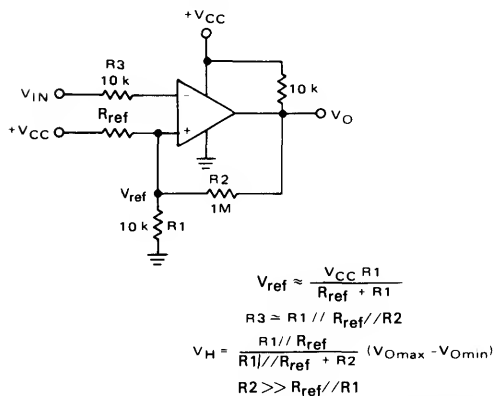
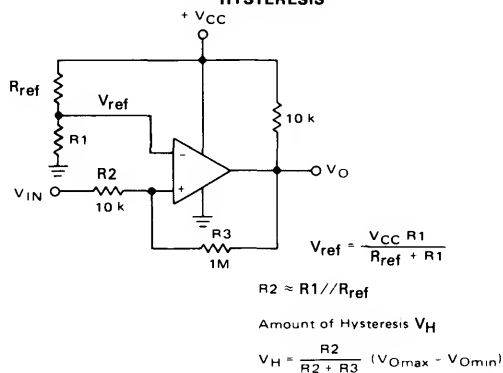


FIGURE 3 — NON-INVERTING COMPARATOR WITH HYSTERESIS



TYPICAL CHARACTERISTICS

($V_{CC} = +15$ Vdc, $T_A = +25^\circ\text{C}$ (each comparator) unless otherwise noted.)

FIGURE 4 — NORMALIZED INPUT OFFSET VOLTAGE

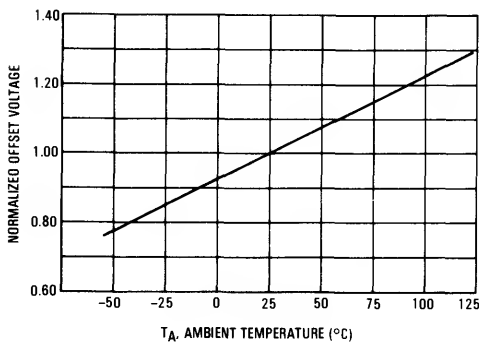


FIGURE 5 — INPUT BIAS CURRENT

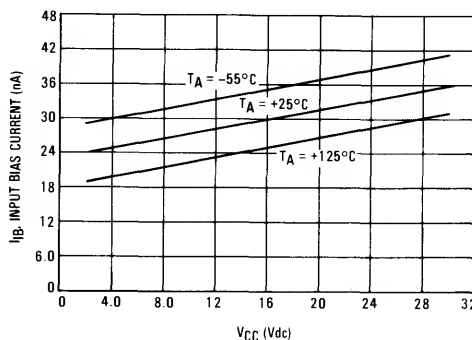


FIGURE 6 — OUTPUT SINK CURRENT versus OUTPUT SATURATION VOLTAGE

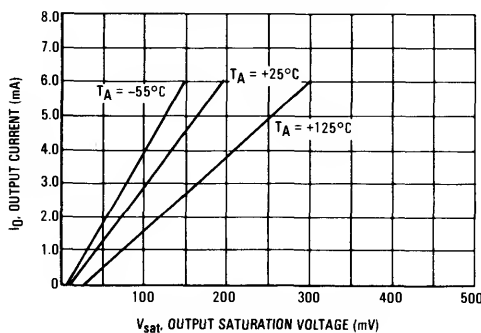
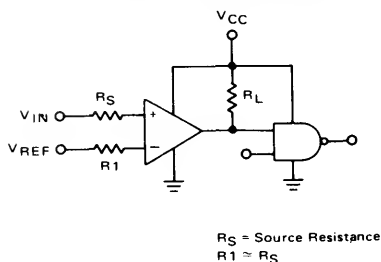
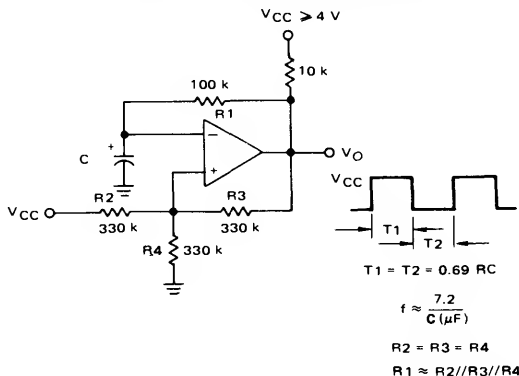


FIGURE 7 — DRIVING LOGIC



LOGIC	DEVICE	V _{CC} Volts	R _L k Ω
CMOS	1/4 MC14001	+15	100
TTL	1/4 MC7400	+5	10

FIGURE 8 — SQUAREWAVE OSCILLATOR



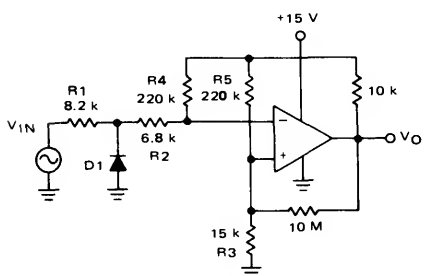
APPLICATIONS INFORMATION

These quad comparators feature high gain, wide bandwidth characteristics. This gives the device oscillation tendencies if the outputs are capacitively coupled to the inputs via stray capacitance. This oscillation manifests itself during output transistions (V_{OL} to V_{OH}). To alleviate this situation input resistors $< 10 \text{ k}\Omega$ should be used. The addition of positive feedback ($< 10 \text{ mV}$) is

also recommended.

It is good design practice to ground all unused input pins.

Differential input voltages may be larger than supply voltages without damaging the comparator's inputs. Voltages more negative than -300 mV should not be used.

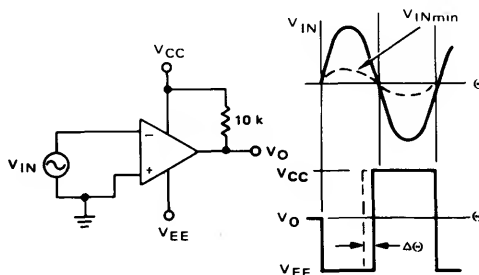
FIGURE 9 — ZERO CROSSING DETECTOR
(Single Supply)


D1 prevents input from going negative by more than 0.6 V.

$R_3 \leq \frac{R_5}{10}$ for small error in zero crossing

FIGURE 10 — ZERO CROSSING DETECTOR
(Split Supplies)

$V_{INmin} \approx 0.4 \text{ V peak for } 1\% \text{ phase distortion } (\Delta\theta)$.



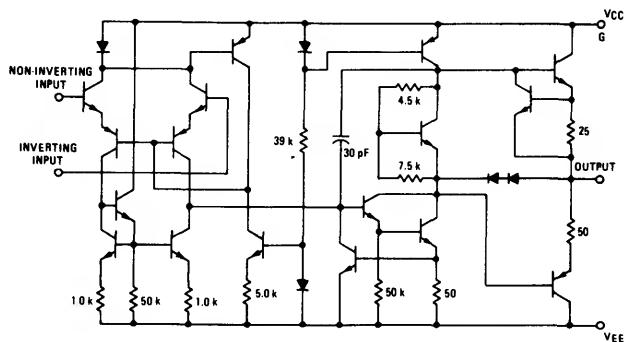
**(QUAD MC1741)
 OPERATIONAL AMPLIFIERS**

The LM148 series is a true quad MC1741. Integrated on a single monolithic chip are four independent, low power operational amplifiers which have been designed to provide operating characteristics identical to those of the industry standard MC1741, and can be applied with no change in circuit performance. In addition, the total supply current for all four amplifiers is comparable to the supply current of a single MC1741. Other features include input offset currents and input bias currents which are much less than the MC1741 industry standard.

The LM148 can be used in applications where amplifier matching or high packing density is important. Other applications include high impedance buffer amplifiers and active filter amplifiers.

- Each Amplifier is Functionally Equivalent to the MC1741
- Low Input Offset and Input Bias Currents
- Class AB Output Stage Eliminates Crossover Distortion
- Pin Compatible with MC3503 and LM124
- True Differential Inputs
- Internally Frequency Compensated
- Short Circuit Protection
- Low Power Supply Current (0.6 mA/Amplifier)

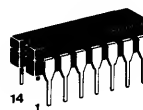
**EQUIVALENT CIRCUIT SCHEMATIC
 (1/4 of Circuit Shown)**



**LM148
 LM248
 LM348**

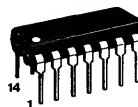
**(QUAD MC1741)
 DIFFERENTIAL INPUT
 OPERATIONAL AMPLIFIERS**

**SILICON MONOLITHIC
 INTEGRATED CIRCUIT**



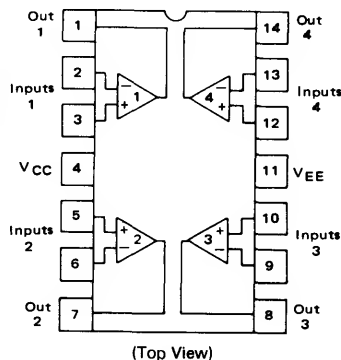
**J SUFFIX
 CERAMIC PACKAGE
 CASE 632**

**N SUFFIX
 PLASTIC PACKAGE
 CASE 646**



**D SUFFIX
 PLASTIC PACKAGE
 CASE 751A
 (SO-14)**

PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
LM148J	-55 to +125°C	Ceramic DIP
LM248J LM248N	-25 to +85°C	Ceramic DIP Plastic DIP
LM348D LM348J LM348N	0 to +70°C	SO-14 Ceramic DIP Plastic DIP

LM148, LM248, LM348

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	LM148	LM248/LM348			Unit
Power Supply Voltage	V _{CC}	+ 22	+ 18			V _{dc}
	V _{EE}	− 22	− 18			V _{dc}
Input Differential Voltage	V _{ID}	± 44	± 36			Volts
Input Common Mode Voltage	V _{ICM}	± 22	± 18			Volts
Output Short Circuit Duration	t _S	Continuous				
Operating Ambient Temperature Range	T _A	− 55 to + 125	− 25 to + 85	0 to + 70	°C	
Storage Temperature Range	T _{stg}	− 65 to + 150 − 55 to + 125				°C
Ceramic Package Plastic Package						
Junction Temperature	T _J	175 150				°C
Ceramic Package Plastic Package						

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = -15 V, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	LM148			LM248/LM348			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (R _S ≤ 10 k)	V _{IO}	—	1.0	5.0	—	1.0	6.0	mV
Input Offset Current	I _{IO}	—	4.0	25	—	4.0	50	nA
Input Bias Current	I _{IB}	—	30	100	—	30	200	nA
Input Resistance	r _i	0.8	2.5	—	0.8	2.5	—	MΩ
Common Mode Input Voltage Range	V _{ICR}	±12	—	—	±12	—	—	V
Large Signal Voltage Gain (R _L ≥ 2.0 k, V _O = ±10 V)	A _V	50	160	—	25	160	—	V/mV
Channel Separation (f = 1.0 Hz to 20 kHz)	—	—	-120	—	—	-120	—	dB
Common Mode Rejection Ratio (R _S ≤ 10 k)	CMRR	70	90	—	70	90	—	dB
Supply Voltage Rejection Ratio (R _S ≤ 10 k)	PSRR	77	96	—	77	96	—	dB
Output Voltage Swing (R _L ≥ 10 k) (R _L ≥ 2 k)	V _O	±12	±13	—	±12	±13	—	V
		±10	±12	—	±10	±12	—	
Output Short-Circuit Current	I _{OS}	—	25	—	—	25	—	mA
Supply Current — (All Amplifiers)	I _D	—	2.4	3.6	—	2.4	4.5	mA
Small Signal Bandwidth (A _V = 1)	BW	—	1.0	—	—	1.0	—	MHz
Phase Margin (A _V = 1)	φ _m	—	60	—	—	60	—	degrees
Slew Rate (A _V = 1)	SR	—	0.5	—	—	0.5	—	V/μs

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = -15 V, T_A = *T_{high} to T_{low} unless otherwise noted)

Input Offset Voltage (R _S ≤ 10 kΩ)	V _{IO}	—	—	6.0	—	—	7.5	mV
Input Offset Current LM148 LM248 LM348	I _{IO}	—	—	75	—	—	—	nA
		—	—	—	—	—	125	
		—	—	—	—	—	100	
		—	—	—	—	—	—	
Input Bias Current LM148 LM248 LM348	I _{IB}	—	—	325	—	—	—	nA
		—	—	—	—	—	500	
		—	—	—	—	—	400	
		—	—	—	—	—	—	
Common Mode Input Voltage Range	V _{ICR}	±12	—	—	±12	—	—	V
Large Signal Voltage Gain (R _L ≥ 2 k, V _O = ±10 V)	A _V	25	—	—	15	—	—	V/mV
Common Mode Rejection Ratio (R _S ≤ 10 k)	CMRR	70	90	—	70	90	—	dB
Supply Voltage Rejection Ratio (R _S ≤ 10 k)	PSRR	77	96	—	77	96	—	dB
Output Voltage Swing (R _L ≥ 10 k) (R _L ≥ 2 k)	V _O	±12	±13	—	±12	±13	—	V
		±10	±12	—	±10	±12	—	

*T_{high} = 125°C for LM148, 85°C for LM248, and 70°C for LM348. T_{low} = -55°C for LM148, -25°C for LM248, and 0°C for LM348.

NOTE: Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted or the maximum junction temperature will be exceeded.

LM148, LM248, LM348

2

TYPICAL CHARACTERISTICS

($V_{CC} = +15\text{ Vdc}$, $V_{EE} = -15\text{ Vdc}$, $T_A = +25^\circ\text{C}$ unless otherwise noted).

**FIGURE 1 – POWER BANDWIDTH
(LARGE SIGNAL SWING versus FREQUENCY)**

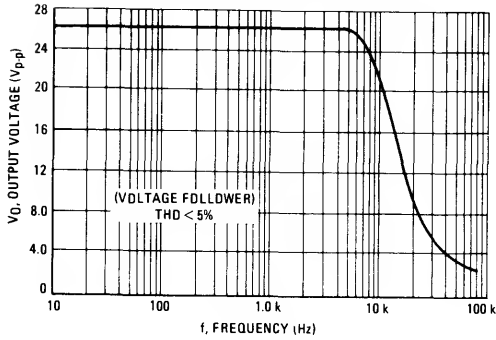
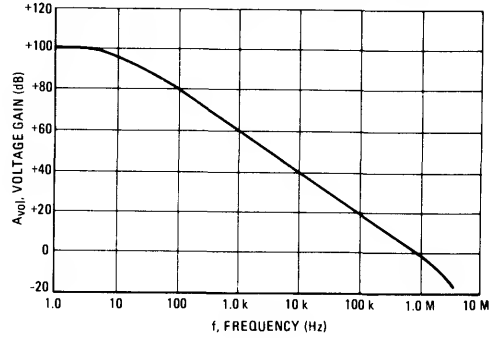
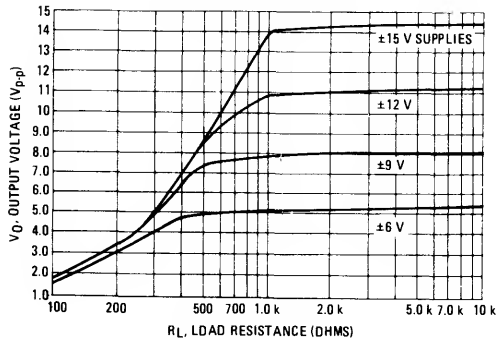


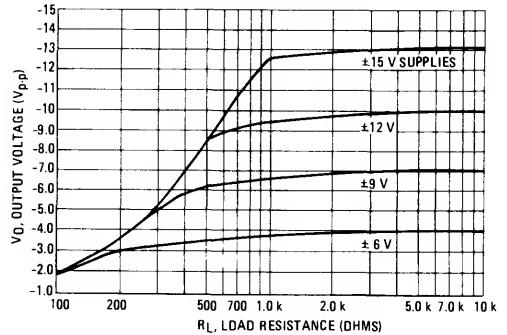
FIGURE 2 – OPEN LOOP FREQUENCY RESPONSE



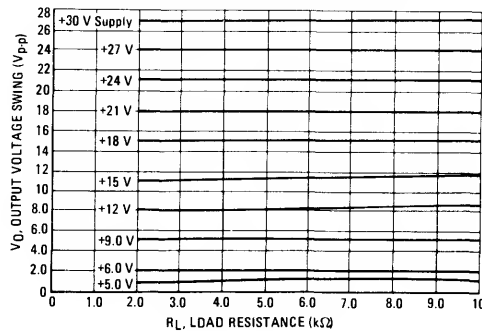
**FIGURE 3 – POSITIVE OUTPUT VOLTAGE SWING
versus LOAD RESISTANCE**



**FIGURE 4 – NEGATIVE OUTPUT VOLTAGE SWING
versus LOAD RESISTANCE**



**FIGURE 5 – OUTPUT VOLTAGE SWING versus
LOAD RESISTANCE (Single Supply Operation)**



LM148, LM248, LM348

FIGURE 6 — NONINVERTING PULSE RESPONSE

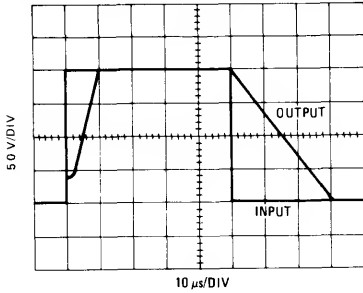
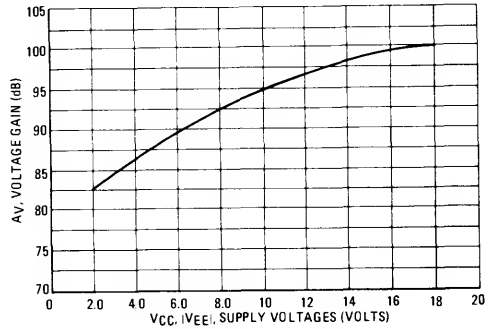


FIGURE 7 — OPEN LOOP VOLTAGE GAIN
versus SUPPLY VOLTAGE



APPLICATIONS INFORMATION

FIGURE 8 — VOLTAGE REFERENCE

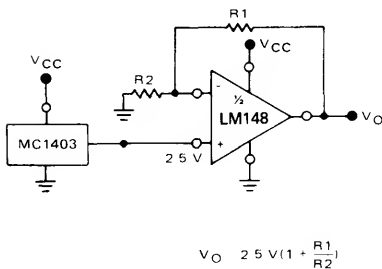


FIGURE 9 — WIEN BRIDGE OSCILLATOR

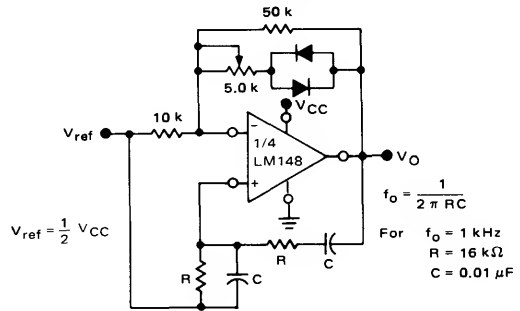


FIGURE 10 — HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER

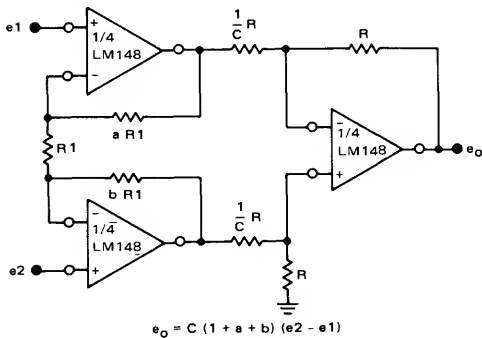
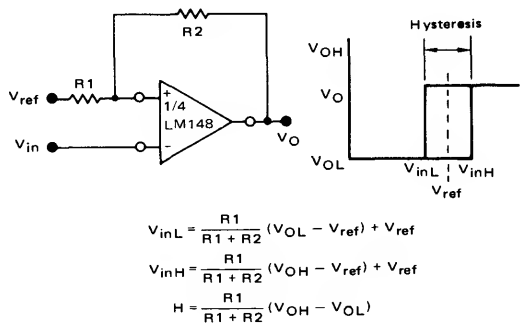


FIGURE 11 — COMPARATOR WITH HYSTERESIS



LM148, LM248, LM348

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FIGURE 12 – HIGH IMPEDANCE INSTRUMENTATION BUFFER/FILTER

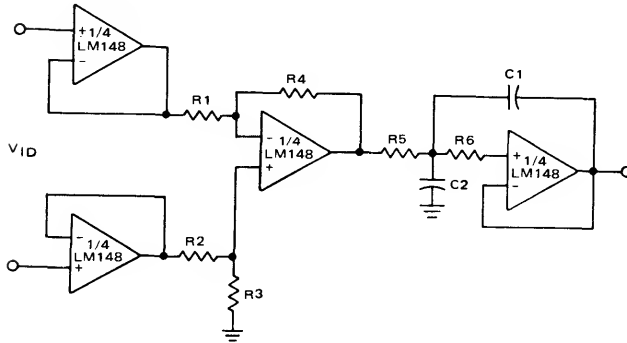


FIGURE 13 – FUNCTION GENERATOR

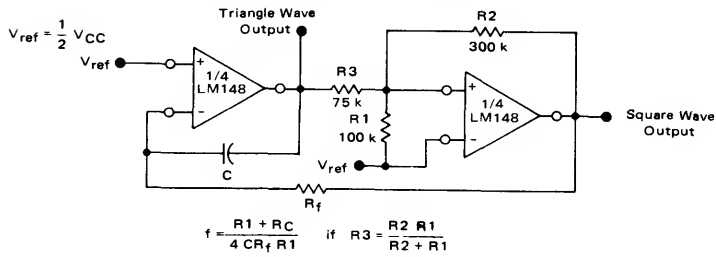
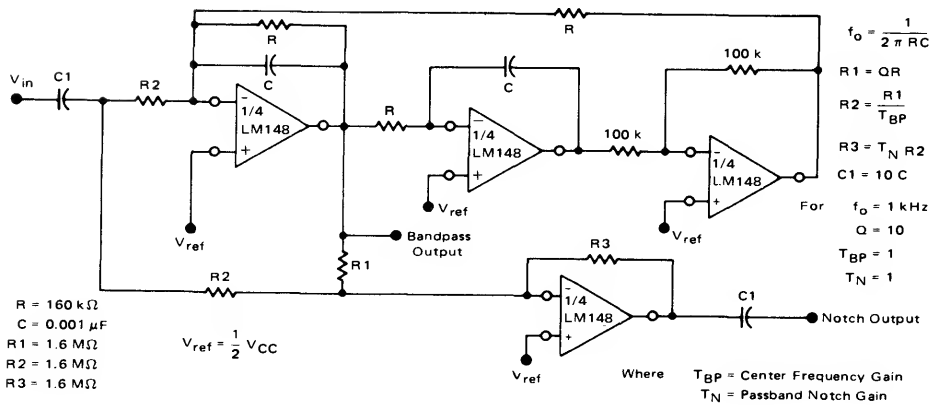
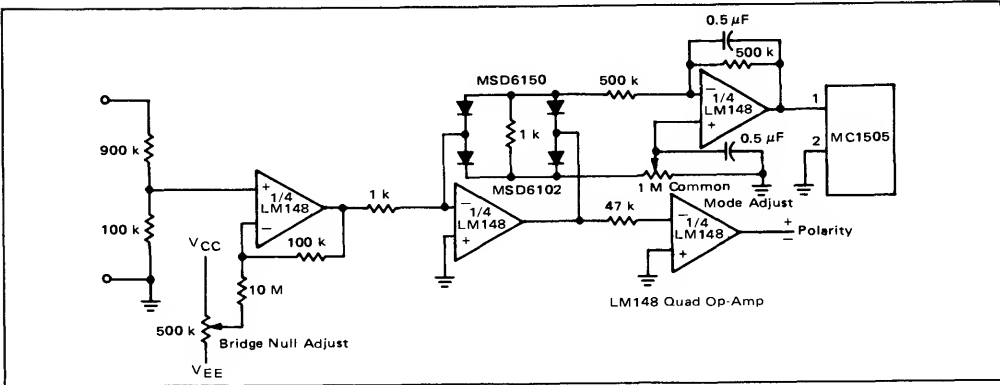


FIGURE 14 – BI-QUAD FILTER



LM148, LM248, LM348

FIGURE 15 — ABSOLUTE VALUE DVM FRONT END



2

DUAL LOW POWER OPERATIONAL AMPLIFIERS

Utilizing the circuit designs perfected for recently introduced Quad Operational Amplifiers, these dual operational amplifiers feature 1) low power drain, 2) a common mode input voltage range extending to ground/ V_{EE} , 3) Single Supply or Split Supply operation and 4) pin outs compatible with the popular MC1558 dual operational amplifier. The LM158 Series is equivalent to one-half of an LM124.

These amplifiers have several distinct advantages over standard operational amplifier types in single supply applications. They can operate at supply voltages as low as 3.0 Volts or as high as 32 Volts with quiescent currents about one-fifth of those associated with the MC1741 (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

- Short Circuit Protected Outputs
- True Differential Input Stage
- Single Supply Operation: 3.0 to 32 Volts
- Low Input Bias Currents
- Internally Compensated
- Common Mode Range Extends to Negative Supply
- Single and Split Supply Operation
- Similar Performance to the Popular MC1558

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	LM158 LM258 LM358	LM2904	Unit
Power Supply Voltages Single Supply Split Supplies	V_{CC} V_{CC}, V_{EE}	32 ± 16	26 ± 13	Vdc
Input Differential Voltage Range (1)	V_{IDR}	± 32	± 26	Vdc
Input Common Mode Voltage Range (2)	V_{ICR}	-0.3 to 32	-0.3 to 26	Vdc
Input Forward Current (3) ($V_I < -0.3\text{ V}$)	I_{IF}	50	—	mA
Output Short Circuit Duration	t_S	Continuous		
Junction Temperature	T_J	175 150		$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150 -55 to +125		$^\circ\text{C}$
Operating Ambient Temperature Range	T_A	-55 to +125 -25 to +85 0 to +70 —	— — — -40 to +105	$^\circ\text{C}$

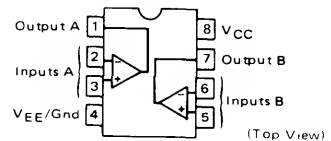
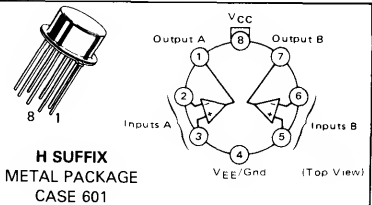
NOTES:

- (1) Split Power Supplies.
- (2) For Supply Voltages less than 32 V for the LM158/258/358 and 26 V for the LM2904, the absolute maximum input voltage is equal to the supply voltage.
- (3) This input current will only exist when the voltage is negative at any of the input leads. Normal output states will reestablish when the input voltage returns to a voltage greater than -0.3 V.

LM158, LM258, LM358, LM2904

DUAL DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUIT



ORDERING INFORMATION

Device	Temperature Range	Package
LM158H	-55 to +125 $^\circ\text{C}$	Metal Can
LM158J		Ceramic DIP
LM2904D	-40 to +105 $^\circ\text{C}$	SO-8
LM2904N		Plastic DIP
LM2904J	-40 to +85 $^\circ\text{C}$	Ceramic DIP
LM2904H		Metal Can
LM258D	-25 to +85 $^\circ\text{C}$	SO-8
LM258H		Metal Can
LM258J		Ceramic DIP
LM258N		Plastic DIP
LM358D	0 to +70 $^\circ\text{C}$	SO-8
LM358H		Metal Can
LM358J		Ceramic DIP
LM358N		Plastic DIP

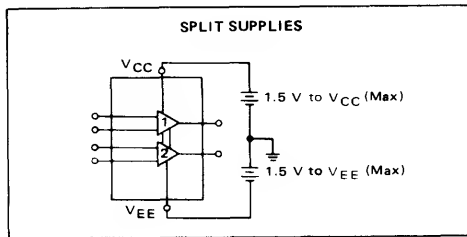
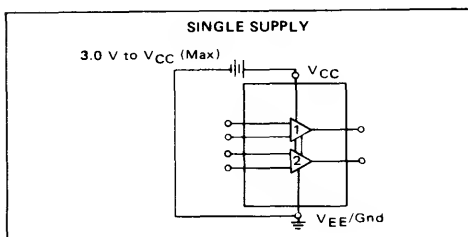
LM158, LM258, LM358, LM2904

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0 \text{ V}$, $V_{EE} = \text{Gnd}$, $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	LM158/LM258			LM358			LM2904			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage $V_{CC} = 5.0 \text{ V}$ to 30 V (26 V for LM2904), $V_{IC} = 0 \text{ V}$ to $V_{CC} - 1.7 \text{ V}$, $V_O = 1.4 \text{ V}$, $R_S = 0 \Omega$ $T_A = 25^\circ\text{C}$ $T_A = T_{\text{high}}$ to T_{low} (Note 1)	V_{IO}	—	2.0	5.0	—	2.0	7.0	—	2.0	7.0	mV
		—	—	7.0	—	—	9.0	—	—	10	
Average Temperature Coefficient of Input Offset Voltage $T_A = T_{\text{high}}$ to T_{low} (Note 1)	$\Delta V_{IO}/\Delta T$	—	7.0	—	—	7.0	—	—	7.0	—	$\mu\text{V}/^\circ\text{C}$
Input Offset Current $T_A = T_{\text{high}}$ to T_{low} (Note 1)	I_{IO}	—	3.0	30	—	5.0	50	—	5.0	50	nA
		—	—	100	—	—	150	—	45	200	
Average Temperature Coefficient of Input Offset Current $T_A = T_{\text{high}}$ to T_{low} (Note 1)	$\Delta I_{IO}/\Delta T$	—	10	—	—	10	—	—	10	—	$\text{pA}/^\circ\text{C}$
Input Bias Current $T_A = T_{\text{high}}$ to T_{low} (Note 1)	I_{IB}	—	-45	-150	—	-45	-250	—	-45	-250	nA
		—	-50	-300	—	-50	-500	—	-50	-500	
Input Common-Mode Voltage Range (Note 2) $V_{CC} = 30 \text{ V}$ (26 V for LM2904), $R_L = 2 \text{ k}\Omega$ $V_{CC} = 30 \text{ V}$ (26 V for LM2904), $T_A = T_{\text{high}}$ to T_{low}	V_{ICR}	0	—	28.3	0	—	28.3	0	—	24.3	V
		0	—	28	0	—	28	0	—	24	
Differential Input Voltage Range	V_{IDR}	—	—	V_{CC}	—	—	V_{CC}	—	—	V_{CC}	V
Large Signal Open-Loop Voltage Gain $R_L = 2.0 \text{ k}\Omega$, $V_{CC} = 15 \text{ V}$, For Large V_O Swing, $T_A = T_{\text{high}}$ to T_{low} (Note 1)	A_{VOL}	50	100	—	25	100	—	—	100	—	V/mV
		25	—	—	15	—	—	—	—	—	
Channel Separation 1.0 kHz $\leq f \leq 20 \text{ kHz}$, Input Referenced	—	—	-120	—	—	-120	—	—	-120	—	dB
Common-Mode Rejection Ratio $R_S \leq 10 \text{ k}\Omega$	CMRR	70	85	—	65	70	—	50	70	—	dB
Power Supply Rejection Ratio	PSRR	65	100	—	65	100	—	50	100	—	dB
Output Voltage Range $R_L = 2 \text{ k}\Omega$ ($R_L \geq 10 \text{ k}\Omega$ for LM2904)	V_{OR}	0	—	3.3	0	—	3.3	0	—	3.3	V
Output Voltage—High Limit ($T_A = T_{\text{high}}$ to T_{low}) (Note 1) $V_{CC} = 30 \text{ V}$ (26 V for LM2904), $R_L = 2 \text{ k}\Omega$ $V_{CC} = 30 \text{ V}$ (26 V for LM2904), $R_L = 10 \text{ k}\Omega$	V_{OH}	26	—	—	26	—	—	22	—	—	V
		27	28	—	27	28	—	23	24	—	
Output Voltage—Low Limit $V_{CC} = 5.0 \text{ V}$, $R_L = 10 \text{ k}\Omega$, $T_A = T_{\text{high}}$ to T_{low} (Note 1)	V_{OL}	—	5.0	20	—	5.0	20	—	5.0	20	mV
Output Source Current $V_{ID} = +1.0 \text{ V}$, $V_{CC} = 15 \text{ V}$	I_{O+}	20	40	—	20	40	—	20	40	—	mA
Output Sink Current $V_{ID} = -1.0 \text{ V}$, $V_{CC} = 15 \text{ V}$ $V_{ID} = -1.0 \text{ V}$, $V_O = 200 \text{ mV}$	I_{O-}	10	20	—	10	20	—	10	20	—	mA
		12	50	—	12	50	—	—	—	—	μA
Output Short Circuit to Ground (Note 3)	I_{OS}	—	40	60	—	40	60	—	40	60	mA
Power Supply Current ($T_A = T_{\text{high}}$ to T_{low}) (Note 1) $V_{CC} = 30 \text{ V}$ (26 V for LM2904), $V_O = 0 \text{ V}$, $R_L = \infty$ $V_{CC} = 5 \text{ V}$, $V_O = 0 \text{ V}$, $R_L = \infty$	I_{CC}	—	1.5	3.0	—	1.5	3.0	—	1.5	3.0	mA
		—	0.7	1.2	—	0.7	1.2	—	0.7	1.2	

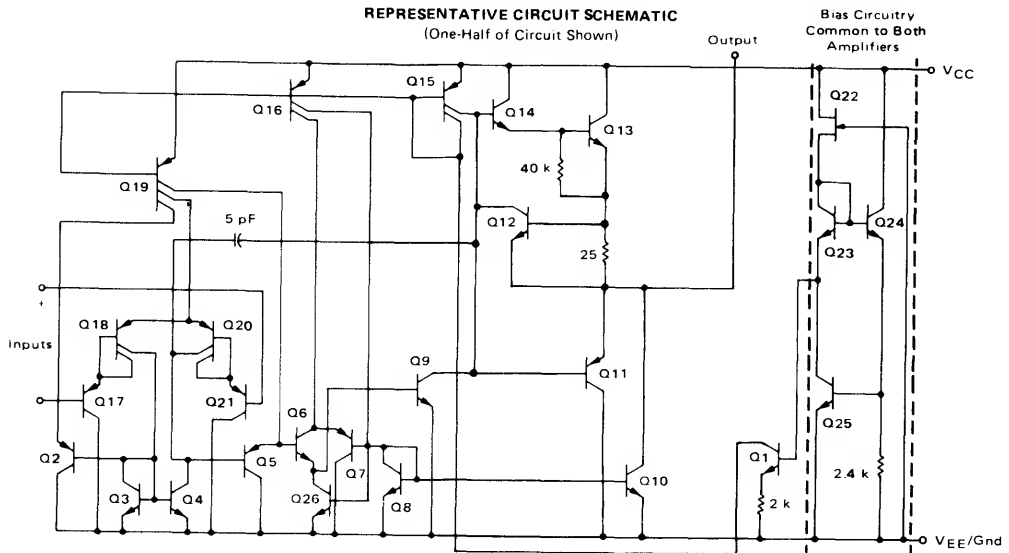
NOTES:

- $T_{\text{low}} = -55^\circ\text{C}$ for LM158
 $= -40^\circ\text{C}$ for LM2904
 $= -25^\circ\text{C}$ for LM258
 $= 0^\circ\text{C}$ for LM358
- $T_{\text{high}} = +125^\circ\text{C}$ for LM158
 $= +105^\circ\text{C}$ for LM2904
 $= +85^\circ\text{C}$ for LM258
 $= +70^\circ\text{C}$ for LM358
- The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is $V_{CC} - 1.7 \text{ V}$.
- Short circuits from the output to V_{CC} can cause excessive heating and eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

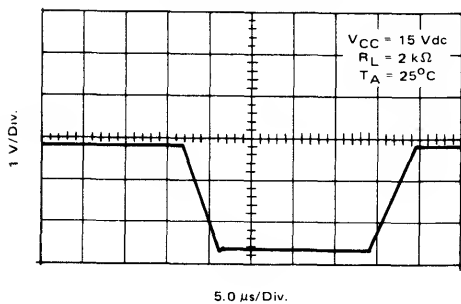


LM158, LM258, LM358, LM2904

2



**LARGE SIGNAL VOLTAGE
FOLLOWER RESPONSE**



CIRCUIT DESCRIPTION

The LM158 Series is made using two internally compensated, two-stage operational amplifiers. The first stage of each consists of differential input devices Q20 and Q18 with input buffer transistors Q21 and Q17 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance a smaller compensation capacitor (only 5 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q20 and Q18. Another feature of this input stage is that the input common-mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single-ended converter. The second stage consists of a standard current source load amplifier stage.

Each amplifier is biased from an internal-voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

TYPICAL PERFORMANCE CURVES

FIGURE 1 – INPUT VOLTAGE RANGE

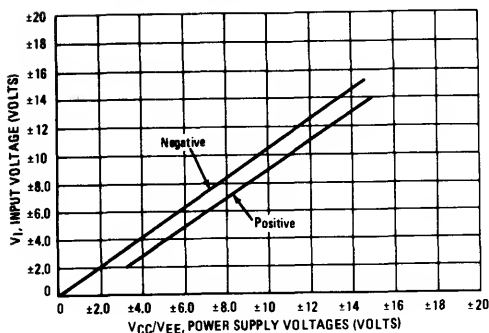


FIGURE 2 – OPEN LOOP FREQUENCY

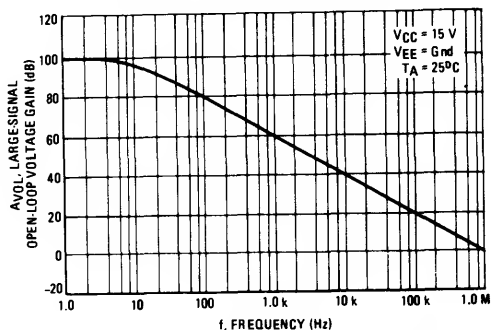


FIGURE 3 – LARGE-SIGNAL FREQUENCY RESPONSE

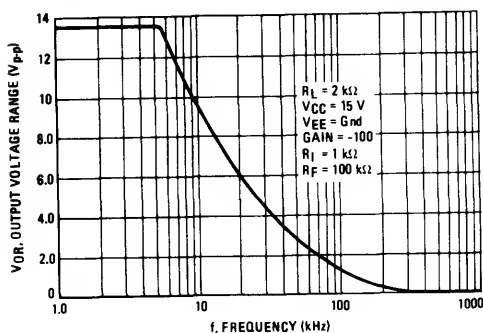


FIGURE 4 – SMALL-SIGNAL VOLTAGE FOLLOWER PULSE RESPONSE (Non-Inverting)

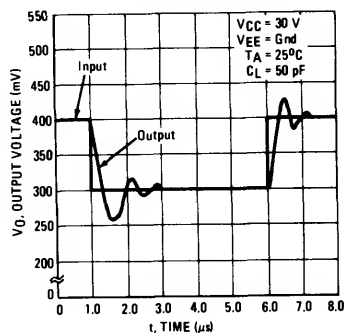


FIGURE 5 – POWER SUPPLY CURRENT versus POWER SUPPLY VOLTAGE

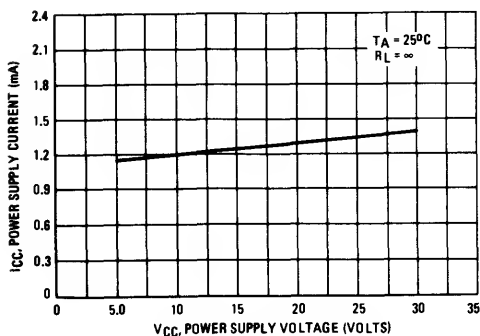
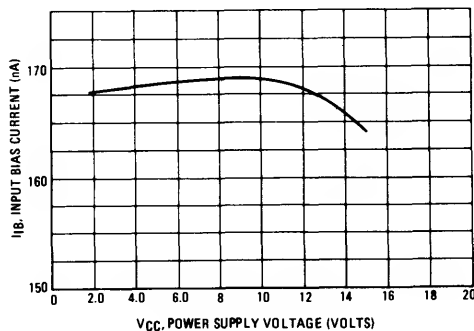


FIGURE 6 – INPUT BIAS CURRENT versus SUPPLY VOLTAGE



LM158, LM258, LM358, LM2904

APPLICATIONS INFORMATION

FIGURE 7 – VOLTAGE REFERENCE

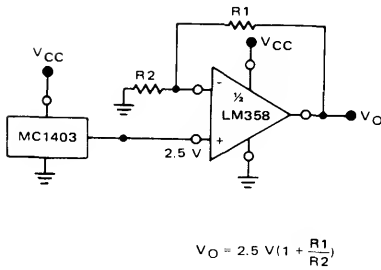


FIGURE 8 – WIEN BRIDGE OSCILLATOR

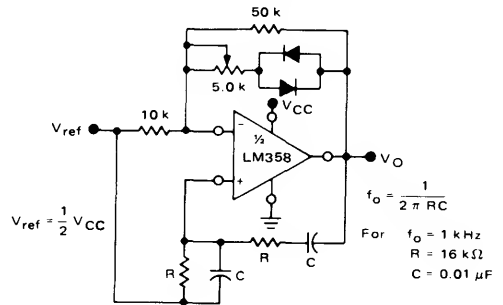


FIGURE 9 – HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER

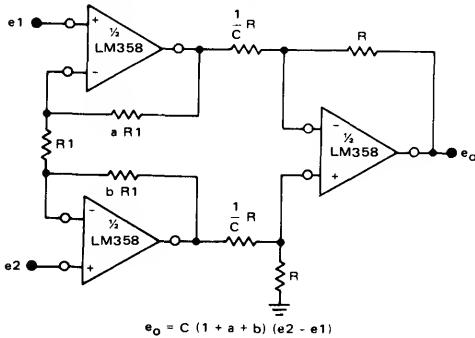


FIGURE 10 – COMPARATOR WITH HYSTERESIS

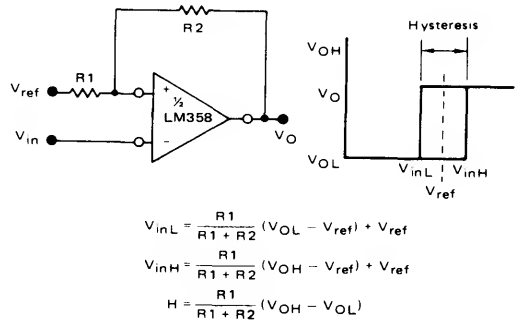
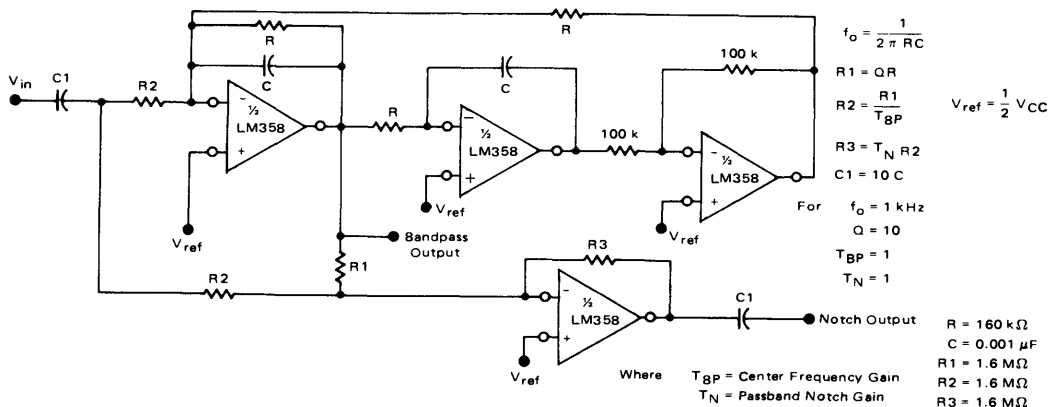


FIGURE 11 – BI-QUAD FILTER



APPLICATIONS INFORMATION (continued)

FIGURE 12 – FUNCTION GENERATOR

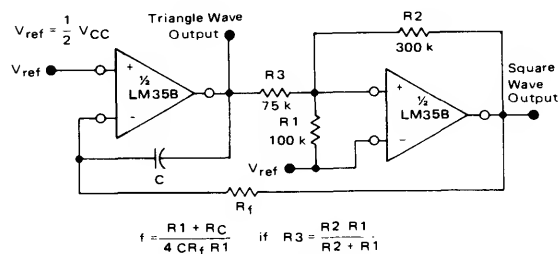
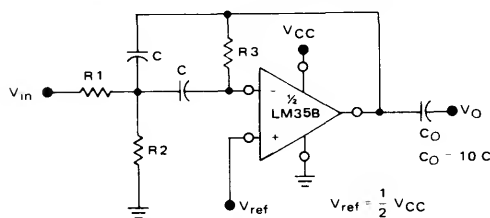


FIGURE 13 – MULTIPLE FEEDBACK BANDPASS FILTER



Given f_o = Center Frequency

$A(f_o)$ = Gain at Center Frequency

Choose Value f_o , C

Then

$$R_3 = \frac{Q}{\pi f_o C}$$

$$R_1 = \frac{R_3}{2 A(f_o)}$$

$$R_2 = \frac{R_1 R_3}{4 Q^2 R_1 - R_3}$$

For less than 10% error from operational amplifier

$$\frac{Q_o f_o}{BW} < 0.1 \quad \text{Where } f_o \text{ and } BW \text{ are expressed in Hz.}$$

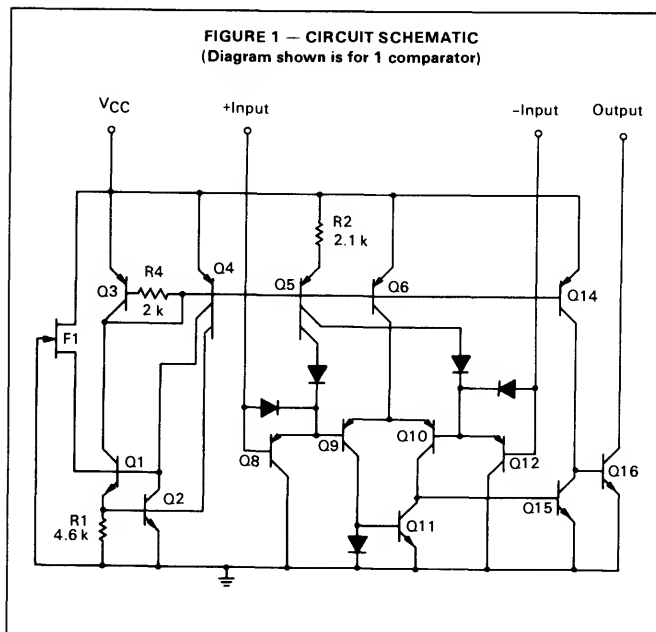
If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

**SINGLE SUPPLY, LOW POWER, LOW OFFSET VOLTAGE
DUAL COMPARATORS**

The LM193 series are dual independent precision voltage comparators capable of single- or split-supply operation. These devices are designed to permit a common mode range-to-ground level with single-supply operation. Input offset-voltage specifications as low as 2.0 mV make this device an excellent selection for many applications in consumer automotive, and industrial electronics.

- Wide Single-Supply Range — 2.0 Vdc to 36 Vdc
- Split-Supply Range — ± 1.0 Vdc to ± 18 Vdc
- Very Low Current Drain Independent of Supply Voltage — 0.4 mA
- Low Input Bias Current — 25 nA
- Low Input Offset Current — 5.0 nA
- Low Input Offset Voltage — 2.0 mV (max) LM193A/293A/393A
— 5.0 mV (max) LM193/293/393
- Input Common Mode Range to Ground Level
- Differential Input Voltage Range Equal to Power Supply Voltage
- Output Voltage Compatible with DTL, ECL, TTL, MOS and CMOS Logic Levels

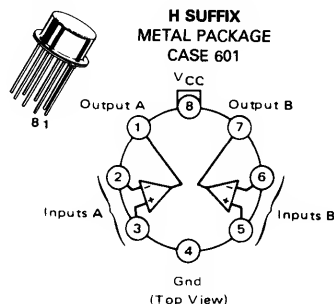
FIGURE 1 — CIRCUIT SCHEMATIC
(Diagram shown is for 1 comparator)



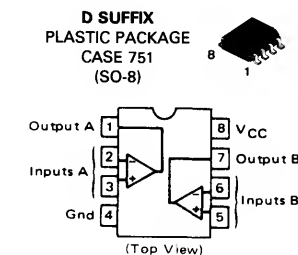
LM193 LM193A
LM293 LM293A
LM393 LM393A
LM2903

DUAL COMPARATORS

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**



N SUFFIX
PLASTIC PACKAGE
CASE 626



ORDERING INFORMATION

Device	Temperature Range	Package
LM193AH,H	-55 to +125°C	Metal Can
LM293AH,H	-25 to +85°C	Metal Can
LM293D		SO-8
LM393AH,H	0 to +70°C	Metal Can
LM393D		SO-8
LM393AN,N		Plastic DIP
LM2903D		SO-8
LM2903N	-40 to +105°C	Plastic DIP

LM193,A, LM293,A, LM393,A, LM2903

2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+36 or ± 18	Vdc
Input Differential Voltage Range	V_{IDR}	36	Vdc
Input Common Mode Voltage Range	V_{ICR}	-0.3 to +36	Vdc
Input Current (2) ($V_{in} < -0.3$ Vdc)	I_{in}	50	mA
Output Short Circuit-to-Ground Output Sink Current (1)	I_{SC} I_{sink}	Continuous 20	mA
Power Dissipation @ $T_A = 25^\circ\text{C}$ Plastic DIP Derate above 25°C Metal Can Derate above 25°C	P_D $1/R_{\theta JA}$ P_D $1/R_{\theta JA}$	570 5.7 830 6.64	mW mW/ $^\circ\text{C}$ mW mW/ $^\circ\text{C}$
Operating Ambient Temperature Range LM193, 193A LM293, 293A LM393, 393A LM2903	T_A	-55 to +125 -25 to +85 0 to +70 -40 to +105	$^\circ\text{C}$
Maximum Operating Junction Temperature LM393, 393A, 2903 LM193, 193A, 293, 293A	$T_{J(max)}$	125 150	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0$ Vdc; $*T_{low} \leq T_A \leq T_{high}$ unless otherwise stated.)

Characteristic	Symbol	LM193A			LM293A, LM393A			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (3) $T_A = 25^\circ\text{C}$ $T_{low} \leq T_A \leq T_{high}$	V_{IO}	— —	± 1.0 —	± 2.0 4.0	— —	± 1.0 —	± 2.0 4.0	mV
Input Offset Current $T_A = 25^\circ\text{C}$ $T_{low} \leq T_A \leq T_{high}$	I_{IO}	— —	± 3.0 —	± 25 ± 100	— —	± 5.0 —	± 50 ± 150	nA
Input Bias Current (4) $T_A = 25^\circ\text{C}$ $T_{low} \leq T_A \leq T_{high}$	I_{IB}	— —	25 —	100 300	— —	25 —	250 400	nA
Input Common Mode Voltage Range (5) $T_A = 25^\circ\text{C}$ $T_{low} \leq T_A \leq T_{high}$	V_{ICR}	0 0	— —	$V_{CC} - 1.5$ $V_{CC} - 2.0$	0 0	— —	$V_{CC} - 1.5$ $V_{CC} - 2.0$	Volts
Voltage Gain $R_L \geq 15$ k Ω , $V_{CC} = 15$ Vdc, $T_A = 25^\circ\text{C}$	A_{VOL}	50	200	—	50	200	—	V/mV
Large Signal Response Time $V_{in} = \text{TTL Logic Swing}$, $V_{ref} = 1.4$ Vdc $V_{RL} = 5.0$ Vdc, $R_L = 5.1$ k Ω , $T_A = 25^\circ\text{C}$	—	—	300	—	—	300	—	ns
Response Time (5) $V_{RL} = 5.0$ Vdc, $R_L = 5.1$ k Ω , $T_A = 25^\circ\text{C}$	t_{TLH}	—	1.3	—	—	1.3	—	μs
Input Differential Voltage (7) All $V_{in} \geq \text{Gnd}$ or V_- Supply (if used)	V_{ID}	—	—	V_{CC}	—	—	V_{CC}	V
Output Sink Current $V_{in-} \geq 1.0$ Vdc, $V_{in+} = 0$ Vdc, $V_O \leq 1.5$ Vdc $T_A = 25^\circ\text{C}$	I_{sink}	6.0	16	—	6.0	16	—	mA
Output Saturation Voltage $V_{in-} \geq 1.0$ Vdc, $V_{in+} = 0$, $I_{sink} \leq 4.0$ mA, $T_A = 25^\circ\text{C}$ $T_{low} \leq T_A \leq T_{high}$	V_{OL}	— —	150 —	400 700	— —	150 —	400 700	mV
Output Leakage Current $V_{in-} = 0$ V, $V_{in+} \geq 1.0$ Vdc, $V_O = 5.0$ Vdc, $T_A = 25^\circ\text{C}$ $V_{in-} = 0$ V, $V_{in+} \geq 1.0$ Vdc, $V_O = 30$ Vdc, $T_{low} \leq T_A \leq T_{high}$	I_{OL}	— —	0.1 —	— 1.0	— —	0.1 —	— 1.0	μA
Supply Current $R_L = \infty$ Both Comparators, $T_A = 25^\circ\text{C}$ $R_L = \infty$ Both Comparators, $V_{CC} = 30$ V	I_{CC}	— —	0.4 1.0	1.0 2.5	— —	0.4 1.0	1.0 2.5	mA

*LM193/193A — $T_{low} = -55^\circ\text{C}$, $T_{high} = +125^\circ\text{C}$

LM293/293A — $T_{low} = -25^\circ\text{C}$, $T_{high} = +85^\circ\text{C}$

LM393/393A — $T_{low} = 0^\circ\text{C}$, $T_{high} = +70^\circ\text{C}$

LM2903 — $T_{low} = -40^\circ\text{C}$, $T_{high} = +105^\circ\text{C}$

LM193,A, LM293,A, LM393,A, LM2903

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc; *T_{low} ≤ T_A ≤ T_{high} unless otherwise stated.)

Characteristic	Symbol	LM193			LM293, LM393			LM2903			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (3) T _A = 25°C T _{low} ≤ T _A ≤ T _{high}	V _{IO}	—	±1.0	±5.0 9.0	—	±1.0	±5.0 9.0	—	±2.0 9.0	±7.0 15	mV
Input Offset Current T _A = 25°C T _{low} ≤ T _A ≤ T _{high}	I _{IO}	—	±3.0	±25 ±100	—	±5.0	±50 ±150	—	±5.0 ±50	±50 ±200	nA
Input Bias Current (4) T _A = 25°C T _{low} ≤ T _A ≤ T _{high}	I _{IB}	—	25	100 300	—	25	250 400	—	25 200	250 500	nA
Input Common Mode Voltage Range (4) T _A = 25°C T _{low} ≤ T _A ≤ T _{high}	V _{ICR}	0 0	—	V _{CC} - 1.5 V _{CC} - 2.0	0 0	—	V _{CC} - 1.5 V _{CC} - 2.0	0 0	—	V _{CC} - 1.5 V _{CC} - 2.0	Volts
Voltage Gain R _L ≥ 15 kΩ, V _{CC} = 15 Vdc, T _A = 25°C	A _{VOL}	50	200	—	50	200	—	25	200	—	V/mV
Large Signal Response Time V _{in} = TTL Logic Swing, V _{ref} = 1.4 Vdc V _{RL} = 5.0 Vdc, R _L = 5.1 kΩ, T _A = 25°C	—	—	300	—	—	300	—	—	300	—	ns
Response Time (6) V _{RL} = 5.0 Vdc, R _L = 5.1 kΩ, T _A = 25°C	t _{TLH}	—	1.3	—	—	1.3	—	—	1.5	—	μs
Input Differential Voltage (7) All V _{in} ≥ Gnd or V- Supply (if used)	V _{ID}	—	—	V _{CC}	—	—	V _{CC}	—	—	V _{CC}	V
Output Sink Current V _{in} ≥ 1.0 Vdc, V _{in+} = 0 Vdc, V _O ≤ 1.5 Vdc T _A = 25°C	I _{sink}	6.0	16	—	6.0	16	—	6.0	16	—	mA
Output Saturation Voltage V _{in} ≥ 1.0 Vdc, V _{in+} = 0, I _{sink} ≤ 4.0 mA, T _A = 25°C T _{low} ≤ T _A ≤ T _{high}	V _{OL}	—	150	400 700	—	150	400 700	—	— 200	400 700	mV
Output Leakage Current V _{in} = 0 V, V _{in+} ≥ 1.0 Vdc, V _O = 5.0 Vdc, T _A = 25°C V _{in} = 0 V, V _{in+} ≥ 1.0 Vdc, V _O = 30 Vdc, T _{low} ≤ T _A ≤ T _{high}	I _{OL}	—	0.1	— 1000	—	0.1	— 1000	—	0.1	— 1000	nA
Supply Current R _L = ∞ Both Comparators, T _A = 25°C R _L = ∞ Both Comparators, V _{CC} = 30 V	I _{CC}	—	0.4	1.0 2.5	—	0.4	1.0 2.5	—	0.4	1.0 2.5	mA

*LM193/193A — T_{low} = -55°C, T_{high} = +125°C

LM293/293A — T_{low} = -25°C, T_{high} = +85°C

LM393/393A — T_{low} = 0°C, T_{high} = +70°C

NOTES:

- (1) The max. output current may be as high as 20 mA, independent of the magnitude of V_{CC}; output short circuits to V_{CC} can cause excessive heating and eventual destruction.
- (2) This magnitude of input current will only occur if the input leads are driven more negative than ground or the negative supply voltage. This is due to the input PNP collector base junction becoming forward biased, acting as an input clamp diode. There is also a lateral PNP parasitic transistor action on the IC chip. This phenomena can cause the output voltage of the comparators to go to the V_{CC} voltage level (or ground if overdrive is large) during the time the input is driven negative. This will not destroy the device and normal output states will recover when the inputs become > -0.3 V of ground or negative supply.
- (3) At output switch point, V_O = 1.4 Vdc, R_S = 0 Ω with V_{CC} from 5.0 Vdc to 30 Vdc, and over the full input common-mode range (0 volts to V_{CC} = -1.5 volts)
- (4) Due to the PNP transistor inputs, bias current will flow out of the inputs; this current is essentially constant independent of the output state, therefore, no loading changes will exist on the input lines.
- (5) Input common mode of either input should not be permitted to go more than 0.3 V negative of ground or minus supply. The upper limit of common mode range is V_{CC} - 1.5 V.
- (6) Response time is specified with a 100 mV step and 5.0 mV of overdrive. With larger magnitudes of overdrive faster response times are obtainable.
- (7) The comparator will exhibit proper output state if one of the inputs become greater than V_{CC}, the other input must remain within the common mode range. The low input state must not be less than -0.3 volts of ground of minus supply.

LM193,A, LM293,A, LM393,A, LM2903

TYPICAL PERFORMANCE CHARACTERISTICS

LM193,A/293,A/393,A

FIGURE 2 — INPUT BIAS CURRENT versus POWER SUPPLY VOLTAGE

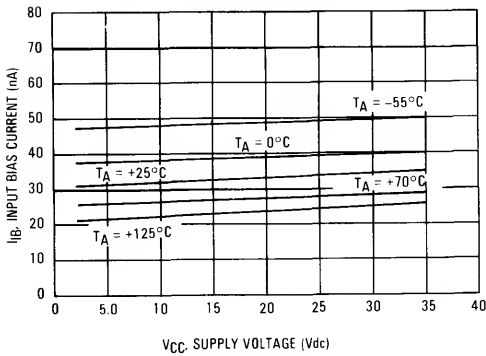


FIGURE 3 — OUTPUT SATURATION VOLTAGE versus OUTPUT SINK CURRENT

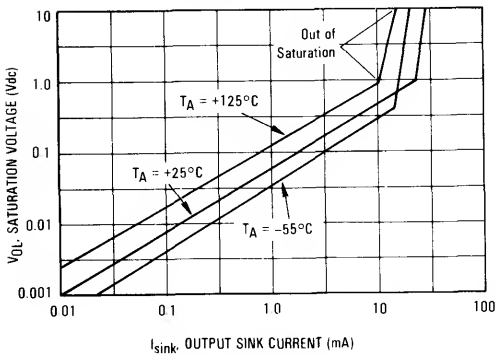
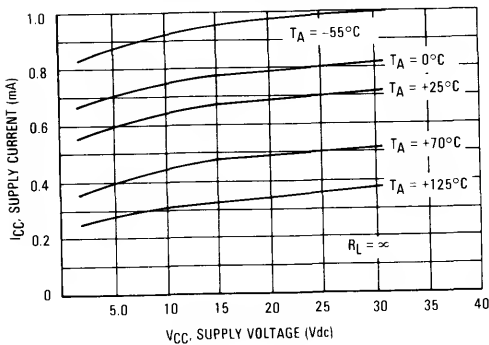


FIGURE 4 — POWER SUPPLY CURRENT versus POWER SUPPLY VOLTAGE



LM2903

FIGURE 5 — INPUT BIAS CURRENT versus POWER SUPPLY VOLTAGE

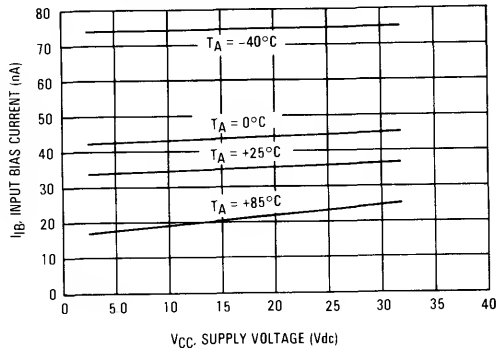


FIGURE 6 — OUTPUT SATURATION VOLTAGE versus OUTPUT SINK CURRENT

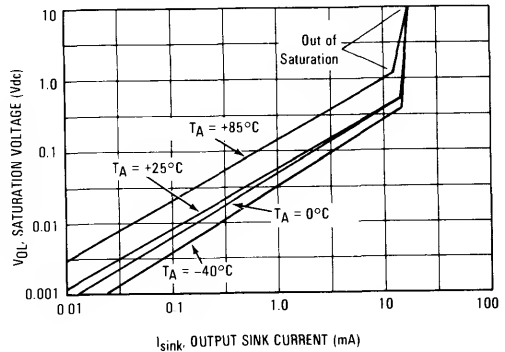
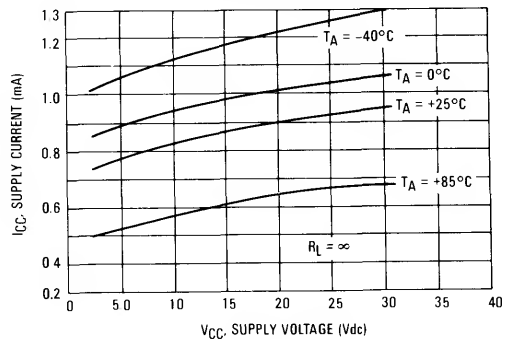


FIGURE 7 — POWER SUPPLY CURRENT versus POWER SUPPLY VOLTAGE

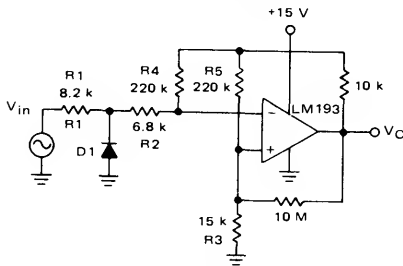


APPLICATIONS INFORMATION

These dual comparators feature high gain, wide bandwidth characteristics. This gives the device oscillation tendencies if the outputs are capacitively coupled to the inputs via stray capacitance. This oscillation manifests itself during output transitions (V_{OL} to V_{OH}). To alleviate this situation input resistors $< 10\text{ k}\Omega$ should be used. The addition of positive feedback ($< 10\text{ mV}$) is also recommended.

It is good design practice to ground all unused pins. Differential input voltages may be larger than supply voltage without damaging the comparator's inputs. Voltages more negative than -0.3 V should not be used.

FIGURE 8 — ZERO CROSSING DETECTOR
(Single Supply)

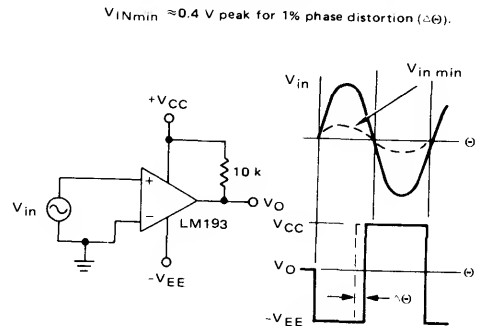


D1 prevents input from going negative by more than 0.6 V.

$$R1 + R2 = R3$$

$$R3 \leq \frac{R5}{10} \text{ for small error in zero crossing}$$

FIGURE 9 — ZERO CROSSING DETECTOR
(Split Supplies)



$$V_{INmin} \approx 0.4\text{ V peak for } 1\% \text{ phase distortion } (\approx \theta)$$

FIGURE 10 — FREE-RUNNING SQUARE-WAVE OSCILLATOR

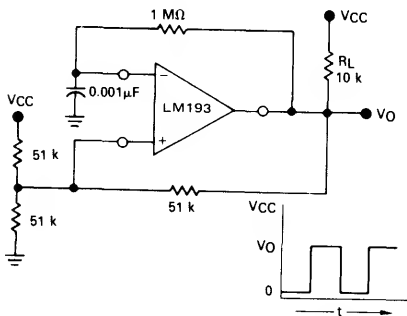


FIGURE 11 — TIME DELAY GENERATOR

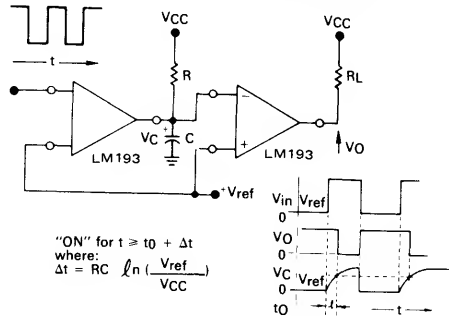
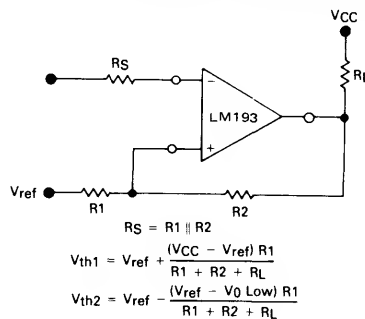


FIGURE 12 — COMPARATOR WITH HYSTERESIS

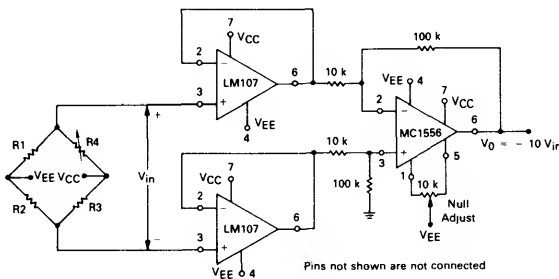


**INTERNALLY COMPENSATED
MONOLITHIC OPERATIONAL AMPLIFIER**

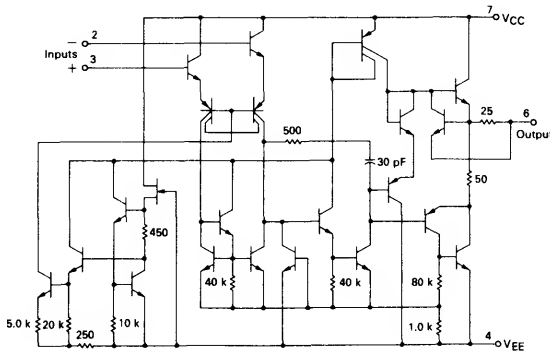
A general purpose operational amplifier series well suited for applications requiring lower input currents than are available with the popular MC1741. These improved input characteristics permit greater accuracy in sample and hold circuits and long interval integrators.

- Internally Compensated
- Low Offset Voltage: 7.5 mV max
- Low Input Offset Current: 50 nA max
- Low Input Bias Current: 250 nA max

**TYPICAL APPLICATION
HIGH IMPEDANCE BRIDGE AMPLIFIER**

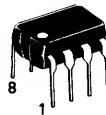


CIRCUIT SCHEMATIC



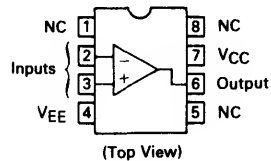
LM307

**OPERATIONAL AMPLIFIER
SILICON MONOLITHIC
INTEGRATED CIRCUIT**



N SUFFIX
PLASTIC PACKAGE
CASE 626

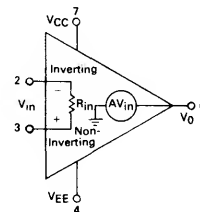
PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
LM307N	0°C to +70°C	Plastic DIP

EQUIVALENT CIRCUIT



**Pins 1, 5, and 8
no connection.**

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted.)

Rating	Symbol	LM307	Unit
Power Supply Voltages	V_{CC} V_{EE}	+ 18 – 18	Vdc
Differential Input Signal Voltage	V_{ID}	± 30	Volts
Common-Mode Input Swing (Note 1)	V_{ICR}	± 15	Volts
Output Short-Circuit Duration	t_s	Indefinite	
Power Dissipation (Package Limitation) (Note 2)	P_D	500	mW
Operating Temperature Range	T_A	0 to + 70	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	– 65 to + 150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted, see Note 3.)

Characteristics	Symbol	LM307			Unit
		Min	Typ	Max	
Input Offset Voltage $R_S \leq 50\text{ k}\Omega$, $T_A = +25^\circ\text{C}$ $R_S \leq 50\text{ k}\Omega$, $T_A = T_{low}$ to T_{high}	V_{IO}	— —	2.0 —	7.5 10	mV
Input Offset Current $T_A = +25^\circ\text{C}$ $T_A = T_{low}$ to T_{high}	I_{IO}	— —	3.0 —	50 70	nA
Input Bias Current $T_A = +25^\circ\text{C}$ $T_A = T_{low}$ to T_{high}	I_{IB}	— —	70 —	250 300	nA
Input Resistance	r_i	0.5	2.0	—	M Ω
Supply Current $V_S = \pm 15\text{ V}$, $T_A = +25^\circ\text{C}$	I_D	—	1.8	3.0	mA
Large-Signal Voltage Gain $V_S = \pm 15\text{ V}$, $V_O = \pm 10\text{ V}$, $R_L > 2.0\text{ k}\Omega$, $T_A = +25^\circ\text{C}$ $V_S = \pm 15\text{ V}$, $V_O = \pm 10\text{ V}$, $R_L \geq 2.0\text{ k}\Omega$, $T_A = T_{low}$	A_v	25 15	160 —	— —	V/mV
Average Temperature Coefficient of Input Offset Voltage $T_{low} \leq T_A \leq T_{high}$	TCV_{IO}	—	6.0	30	$\mu\text{V}/^\circ\text{C}$
Average Temperature Coefficient of Input Offset Current $+25^\circ\text{C} \leq T_A \leq T_{high}$ $T_{low} \leq T_A \leq +25^\circ\text{C}$	TCI_{IO}	— —	0.01 0.02	0.3 0.6	nA/ $^\circ\text{C}$
Output Voltage Swing ($T_A = T_{low}$ to T_{high}) $V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$ $R_L = 2.0\text{ k}\Omega$	V_O	± 12 ± 10	$+14$ ± 13	— —	V
Input Voltage Range ($T_A = T_{low}$ to T_{high}) $V_S = \pm 15\text{ V}$	V_{ICR}	± 12	—	—	V
Common-Mode Rejection Ratio ($T_A = T_{low}$ to T_{high}) $R_S \leq 50\text{ k}\Omega$	CMRR	70	90	—	dB
Supply-Voltage Rejection Ratio ($T_A = T_{low}$ to T_{high}) $R_S \leq 50\text{ k}\Omega$	PSRR	70	96	—	dB

Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.

NOTES:

- For supply voltages less than $\pm 15\text{ V}$, the absolute maximum input voltage is equal to the supply voltage.
- For operating at elevated temperatures, the device must be derated based on a maximum junction temperature of 100°C for the LM307.

The H package is derated based on a thermal resistance of $+150^\circ\text{C}/\text{W}$, junction to ambient, or $+45^\circ\text{C}/\text{W}$, junction to case.

- Unless otherwise noted, these specifications apply for:
 $\pm 5.0\text{ V} \leq V_{CC}/V_{EE} \leq \pm 15\text{ V}$, $T_{low} = 0^\circ\text{C}$, $T_{high} = +70^\circ\text{C}$

TYPICAL CHARACTERISTICS

(V_{CC} = +15 V, V_{EE} = -15 V, T_A = +25°C unless otherwise noted.)

FIGURE 1 — MINIMUM INPUT VOLTAGE RANGE

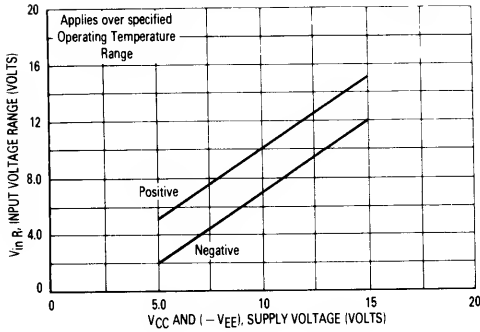


FIGURE 2 — MINIMUM OUTPUT VOLTAGE SWING

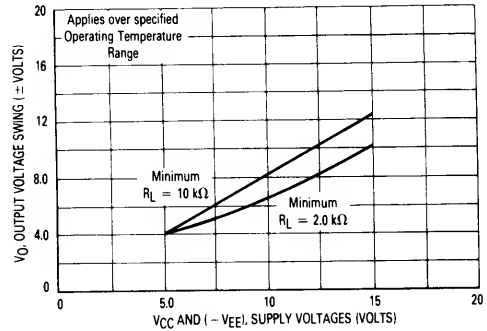


FIGURE 3 — MINIMUM VOLTAGE GAIN

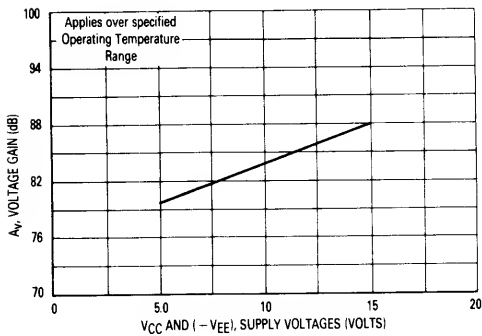


FIGURE 4 — TYPICAL SUPPLY CURRENTS

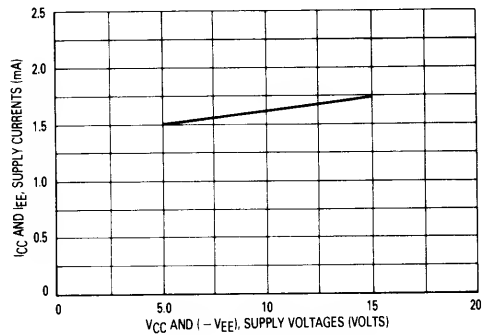


FIGURE 5 — OPEN-LOOP FREQUENCY RESPONSE

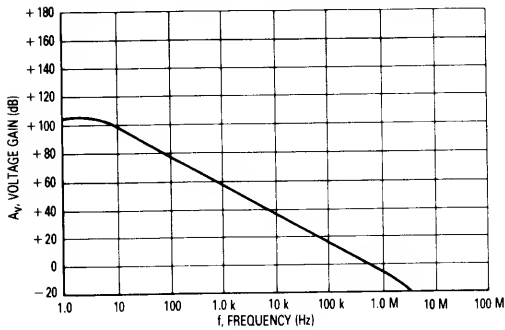
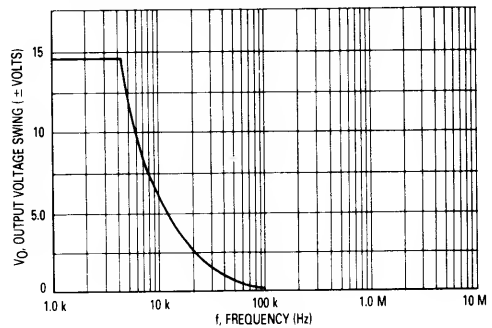
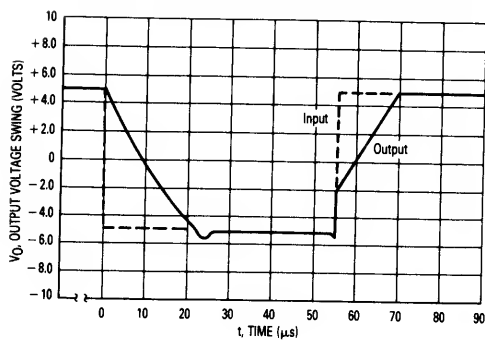


FIGURE 6 — LARGE-SIGNAL FREQUENCY RESPONSE



TYPICAL CHARACTERISTICS (continued)

FIGURE 7 — VOLTAGE FOLLOWER PULSE RESPONSE



**DUAL, LOW NOISE, AUDIO
 OPERATIONAL AMPLIFIER**

The LM833 is a standard low-cost monolithic dual general-purpose operational amplifier employing Bipolar technology with innovative high-performance concepts for audio systems applications. With high frequency PNP transistors, the LM833 offers low voltage noise (4.5 nV/√Hz), 15 MHz gain bandwidth product, 7.0 V/μs slew rate, 0.3 mV input offset voltage with 2.0 μV/°C temperature coefficient of input offset voltage. The LM833 output stage exhibits no deadband crossover distortion, large output voltage swing, excellent phase and gain margins, low open-loop high frequency output impedance and symmetrical source/sink ac frequency response.

The LM833 is specified over the vehicular temperature range and is available in the plastic DIP and SO-8 packages (P and D suffixes). For an improved performance dual/quad version, see the MC33079 family.

- Low Voltage Noise: 4.5 nV/√Hz
- High Gain Bandwidth Product: 15 MHz
- High Slew Rate: 7.0 V/μs
- Low Input Offset Voltage: 0.3 mV
- Low T.C. of Input Offset Voltage: 2.0 μV/°C
- Low Distortion: 0.002%
- Excellent Frequency Stability
- Dual Supply Operation

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V _{CC} to V _{EE})	V _S	+36	Volts
Input Differential Voltage Range	V _{IDR}	30 ⁽¹⁾	Volts
Input Voltage Range	V _{IR}	±15 ⁽¹⁾	Volts
Output Short-Circuit Duration ⁽²⁾	t _S	Indefinite	Seconds
Operating Ambient Temperature Range	T _A	-40 to +85	°C
Operating Junction Temperature	T _J	+150	°C
Storage Temperature	T _{stg}	-60 to +150	°C
Maximum Power Dissipation ⁽²⁾	P _D	500 ⁽³⁾	mW

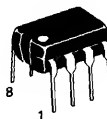
NOTES:

1. Either or both input voltages must not exceed the magnitude of V_{CC} or V_{EE}
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (See power dissipation performance characteristic).
3. Maximum value at T_A ≤ 85°C.

LM833

**DUAL OPERATIONAL
 AMPLIFIER**

**SILICON MONOLITHIC
 INTEGRATED CIRCUIT**

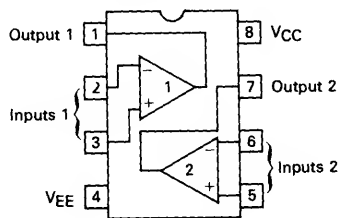


N SUFFIX
 PLASTIC PACKAGE
 CASE 626



D SUFFIX
 PLASTIC PACKAGE
 CASE 751
 (SO-8)

PIN ASSIGNMENTS



Dual, Top View

ORDERING INFORMATION

Device	Temperature Range	Package
LM833N	-40 to +85°C	Plastic DIP
LM833D		SO-8

LM833

2

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = 25^\circ\text{C}$ unless otherwise noted).

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S = 10\ \Omega$, $V_O = 0\text{ V}$)	V_{IO}	—	0.3	5.0	mV
Average Temperature Coefficient of Input Offset Voltage $R_S = 10\ \Omega$, $V_O = 0\text{ V}$, $T_A = T_{\text{low}}$ to T_{high}	$\Delta V_{IO}/\Delta T$	—	2.0	—	$\mu\text{V}/^\circ\text{C}$
Input Offset Current ($V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$)	I_{IO}	—	10	200	nA
Input Bias Current ($V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$)	I_{IB}	—	300	1000	nA
Common Mode Input Voltage Range	V_{ICR}	— -12	+14 -14	+12 —	V
Large Signal Voltage Gain ($R_L = 2.0\text{ k}\Omega$, $V_O = \pm 10\text{ V}$)	A_{VOL}	90	110	—	dB
Output Voltage Swing: $R_L = 2.0\text{ k}\Omega$, $V_{ID} = 1.0\text{ V}$ $R_L = 2.0\text{ k}\Omega$, $V_{ID} = 1.0\text{ V}$ $R_L = 10\text{ k}\Omega$, $V_{ID} = 1.0\text{ V}$ $R_L = 10\text{ k}\Omega$, $V_{ID} = 1.0\text{ V}$	V_{O+}	10	13.7	—	V
	V_{O-}	—	-14.1	-10	V
	V_{O+}	12	13.9	—	V
	V_{O-}	—	-14.7	-12	V
Common Mode Rejection ($V_{IN} = \pm 12\text{ V}$)	CMR	80	100	—	dB
Power Supply Rejection ($V_S = 15\text{ to }5.0\text{ V}$, $-15\text{ to }-5.0\text{ V}$)	PSR	80	115	—	dB
Power Supply Current ($V_O = 0\text{ V}$, Both Amplifiers)	I_D	—	4.0	8.0	mA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = 25^\circ\text{C}$ unless otherwise noted).

Characteristics	Symbol	Min	Typ	Max	Unit
Slew Rate ($V_{IN} = -10\text{ V to }+10\text{ V}$, $R_L = 2.0\text{ k}\Omega$, $A_V = +1.0$)	SR	5.0	7.0	—	$\text{V}/\mu\text{s}$
Gain Bandwidth Product ($f = 100\text{ kHz}$)	GBW	10	15	—	MHz
Unity Gain Frequency (Open Loop)	f_U	—	9.0	—	MHz
Unity Gain Phase Margin (Open Loop)	θ_m	—	60	—	Deg
Equivalent Input Noise Voltage ($R_S = 100\ \Omega$, $f = 1.0\text{ kHz}$)	e_n	—	4.5	—	$\text{nV}/\sqrt{\text{Hz}}$
Equivalent Input Noise Current ($f = 1.0\text{ kHz}$)	i_n	—	0.5	—	$\text{pA}/\sqrt{\text{Hz}}$
Power Bandwidth ($V_O = 27\text{ V}_{\text{p-p}}$, $R_L = 2.0\text{ k}\Omega$, $\text{THD} \leq 1.0\%$)	BWP	—	120	—	kHz
Distortion ($R_L = 2.0\text{ k}\Omega$, $f = 20\text{ Hz to }20\text{ kHz}$, $V_O = 3.0\text{ V}_{\text{rms}}$, $A_V = +1.0$)	THD	—	0.002	—	%
Channel Separation ($f = 20\text{ Hz to }20\text{ kHz}$)	—	—	-120	—	dB

FIGURE 1 — MAXIMUM POWER DISSIPATION
versus TEMPERATURE

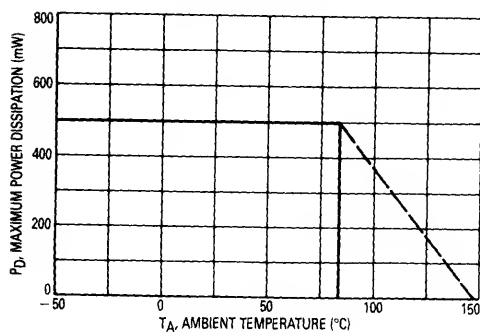


FIGURE 2 — INPUT BIAS CURRENT versus TEMPERATURE

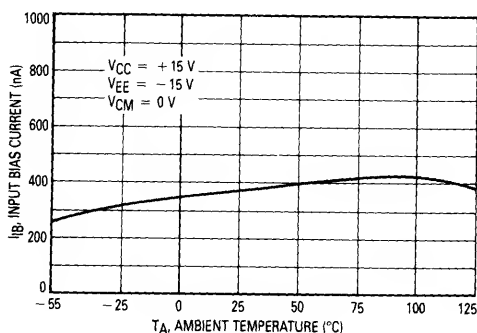


FIGURE 3 — INPUT BIAS CURRENT versus SUPPLY VOLTAGE

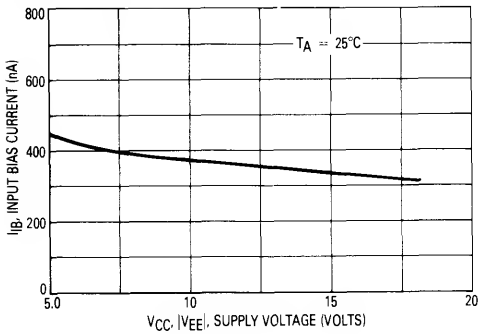


FIGURE 4 — SUPPLY CURRENT versus SUPPLY VOLTAGE

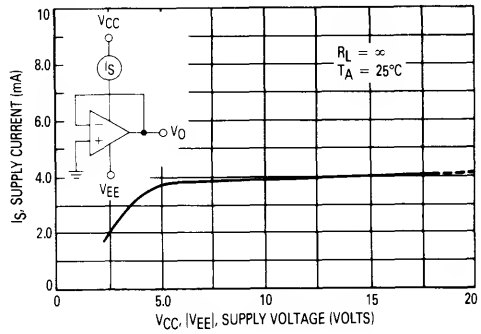


FIGURE 5 — DC VOLTAGE GAIN versus TEMPERATURE

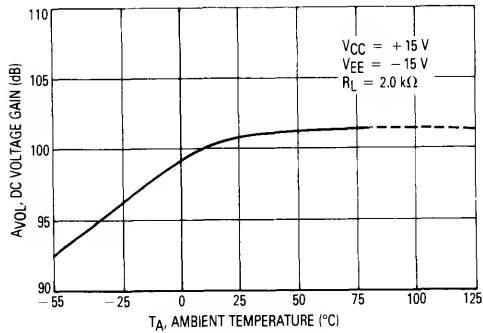


FIGURE 6 — DC VOLTAGE GAIN versus SUPPLY VOLTAGE

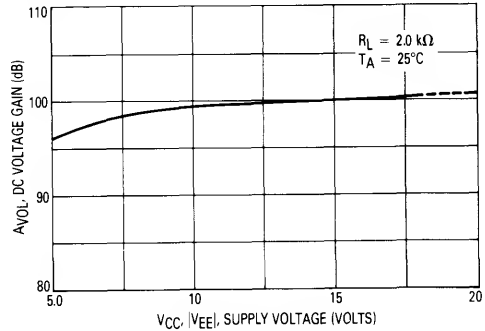


FIGURE 7 — OPEN-LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY

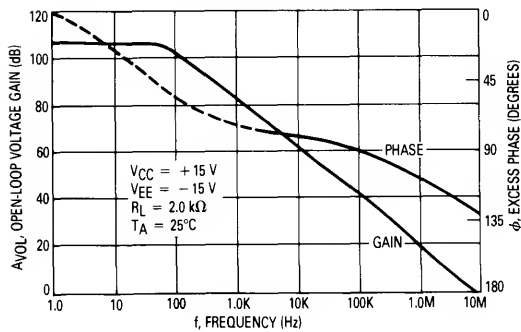


FIGURE 8 — GAIN BANDWIDTH PRODUCT versus TEMPERATURE

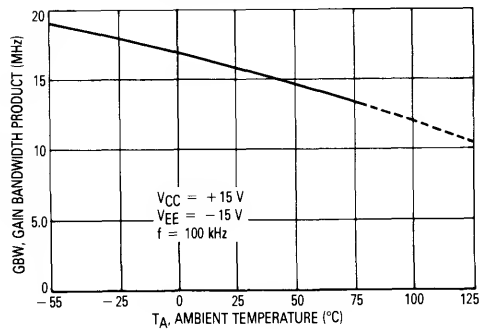


FIGURE 9 — GAIN BANDWIDTH PRODUCT versus SUPPLY VOLTAGE

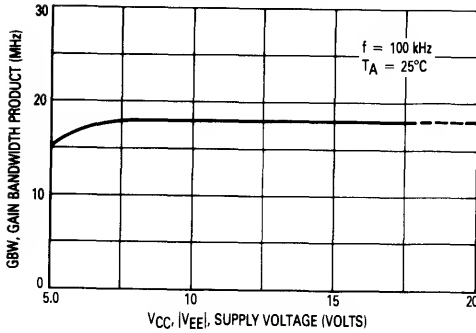


FIGURE 10 — SLEW RATE versus TEMPERATURE

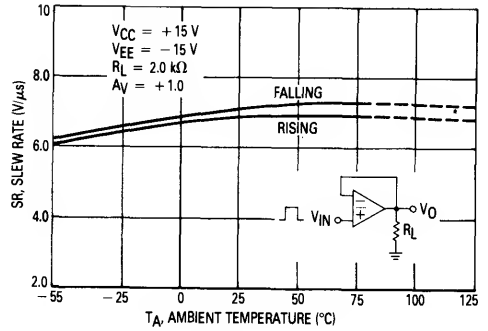


FIGURE 11 — SLEW RATE versus SUPPLY VOLTAGE

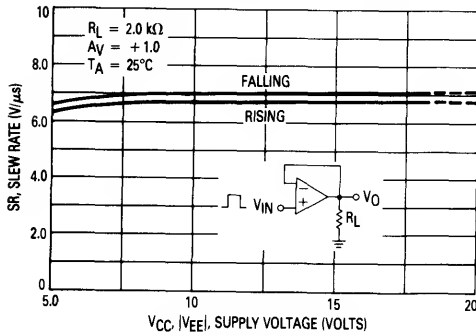


FIGURE 12 — OUTPUT VOLTAGE versus FREQUENCY

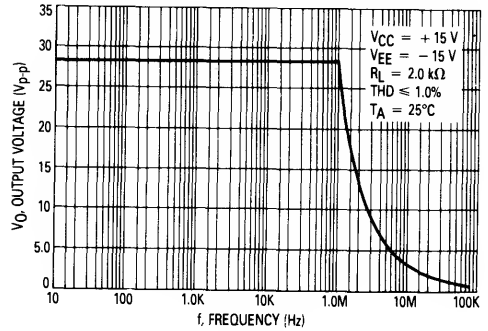


FIGURE 13 — MAXIMUM OUTPUT VOLTAGE versus SUPPLY VOLTAGE

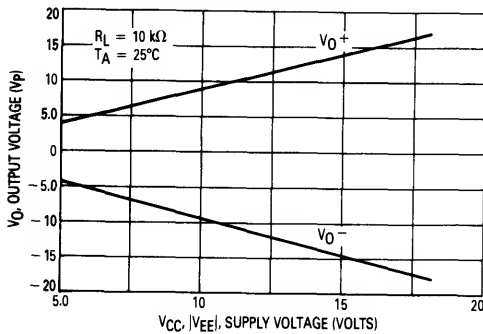
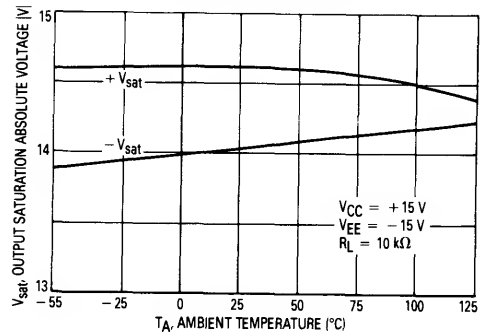
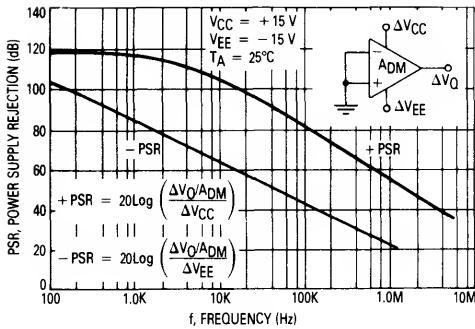


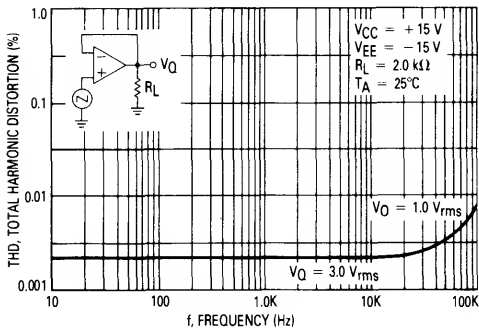
FIGURE 14 — OUTPUT SATURATION VOLTAGE versus TEMPERATURE



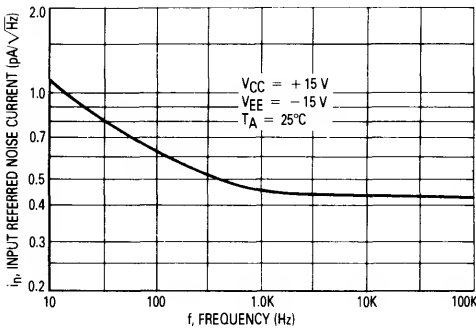
**FIGURE 15 — POWER SUPPLY REJECTION
versus FREQUENCY**



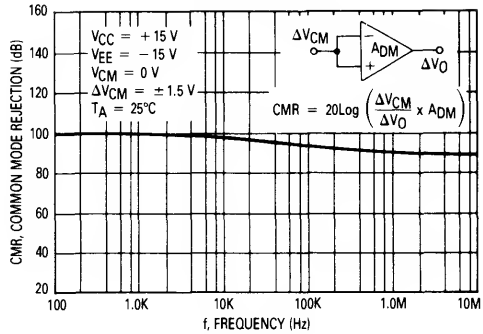
**FIGURE 17 — TOTAL HARMONIC DISTORTION
versus FREQUENCY**



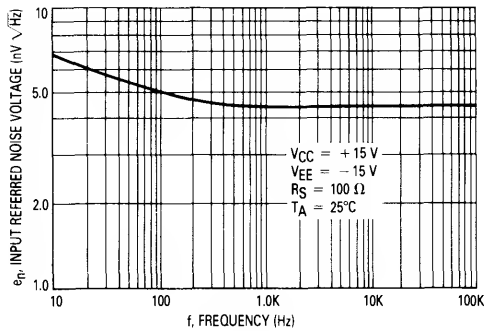
**FIGURE 19 — INPUT REFERRED NOISE CURRENT
versus FREQUENCY**



**FIGURE 16 — COMMON MODE REJECTION
versus FREQUENCY**



**FIGURE 18 — INPUT REFERRED NOISE VOLTAGE versus
FREQUENCY**



**FIGURE 20 — INPUT REFERRED NOISE VOLTAGE
versus SOURCE RESISTANCE**

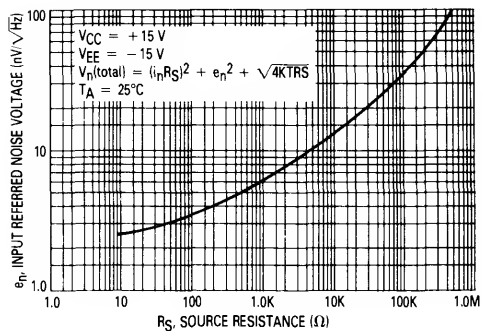


FIGURE 21 — INVERTING AMPLIFIER

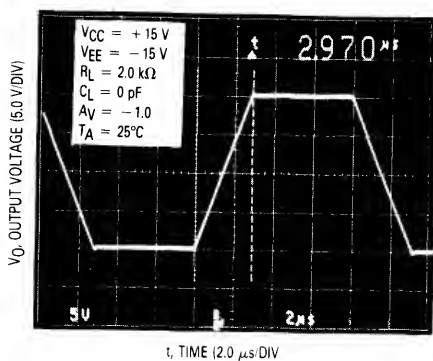


FIGURE 22 — NON-INVERTING AMPLIFIER SLEW RATE

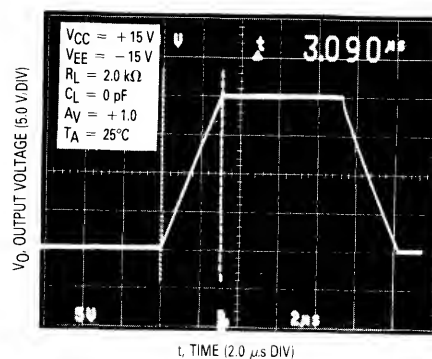
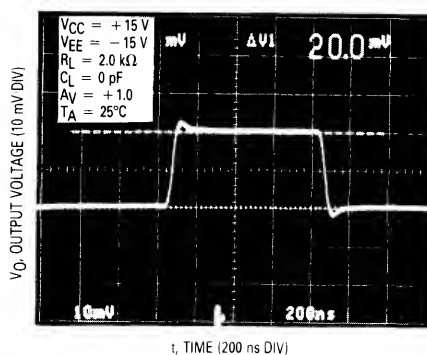


FIGURE 23 — NON-INVERTING AMPLIFIER OVERSHOOT



LM2900, LM3900 For Specifications, See MC3301 Data.
LM2901 For Specifications, See LM139 Data.
LM2902 For Specifications, See LM124 Data.
LM2903 For Specifications, See LM193
LM2904 For Specifications, See LM158

DUAL DIFFERENTIAL VOLTAGE COMPARATOR

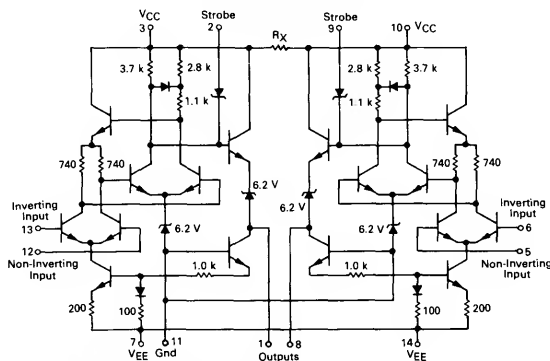
... designed for use in level detection, low-level sensing, and memory applications.

- Two Separate Outputs
- Strobe Capability
- High Output Sink Current
2.8 mA Minimum (Each Comparator) for MC1514
1.6 mA Minimum (Each Comparator) for MC1414
- Differential Input Characteristics
Input Offset Voltage = 1.0 mV for MC1514
= 1.5 mV for MC1414
Offset Voltage Drift = 3.0 $\mu\text{V}/^\circ\text{C}$ for MC1514
= 5.0 $\mu\text{V}/^\circ\text{C}$ for MC1414
- Short Propagation Delay Time — 40 ns Typical
- Output Compatible with All Saturating Logic Forms
 $V_O = +3.2\text{ V to } -0.5\text{ V Typical}$

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC} V_{EE}	+14 -7.0	Vdc
Differential Mode Input Voltage Range	V_{IDR}	± 5.0	Vdc
Common Mode Input Voltage Range	V_{ICR}	± 7.0	Vdc
Peak Load Current	I_L	10	mA
Power Dissipation (Package Limitation)	P_D		
Ceramic Dual In-Line Package		1000	mW
Derate above $T_A = 25^\circ\text{C}$		6.0	mW/ $^\circ\text{C}$
Plastic Dual In-Line Package		625	mW
Derate above $T_A = 25^\circ\text{C}$		5.0	mW/ $^\circ\text{C}$
Operating Temperature	T_A	-55 to +125 0 to +75	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

CIRCUIT SCHEMATIC



R_X = Low Resistance Value, usually < 100 Ω , not specified.

MC1414 MC1514

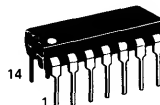
DUAL DIFFERENTIAL COMPARATOR

(DUAL MC1710)

SILICON MONOLITHIC
INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 632

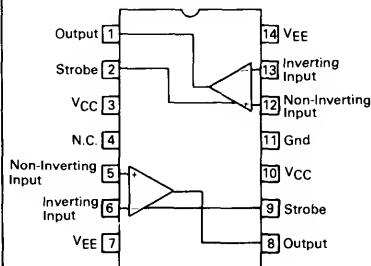


P SUFFIX
PLASTIC PACKAGE
CASE 646
(MC1414 Only)

D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)
(MC1414 Only)



PIN CONNECTIONS



MC1414, MC1514

ELECTRICAL CHARACTERISTICS ($V_{CC} = +12$ Vdc, $V_{EE} = -6.0$ Vdc, $T_A = 25^\circ\text{C}$ unless otherwise noted.) (Each Comparator)

Characteristic	Symbol	MC1514			MC1414			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($V_O = 1.4$ Vdc, $T_A = 25^\circ\text{C}$) ($V_O = 1.8$ Vdc, $T_A = T_{low}^*$) ($V_O = 1.0$ Vdc, $T_A = T_{high}^*$)	V_{IO}	—	1.0	2.0 3.0 3.0	—	1.5	5.0 6.5 6.5	mVdc
Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	—	3.0	—	—	5.0	—	$\mu\text{V}/^\circ\text{C}$
Input Offset Current ($V_O = 1.4$ Vdc, $T_A = 25^\circ\text{C}$) ($V_O = 1.8$ Vdc, $T_A = T_{low}$) ($V_O = 1.0$ Vdc, $T_A = T_{high}$)	I_{IO}	—	1.0	3.0 7.0 3.0	—	1.0	5.0 7.5 7.5	μAdc
Input Bias Current ($V_O = 1.4$ Vdc, $T_A = 25^\circ\text{C}$) ($V_O = 1.8$ Vdc, $T_A = T_{low}$) ($V_O = 1.0$ Vdc, $T_A = T_{high}$)	I_{IB}	—	12	20 45 20	—	15 18	25 40 40	μAdc
Open Loop Voltage Gain ($T_A = 25^\circ\text{C}$) ($T_A = T_{low}$ to T_{high})	A_{VOL}	1250 1000	1700	—	1000 800	1500	—	V/V
Output Resistance	R_O	—	200	—	—	200	—	Ohms
Differential Voltage Range	V_{IDR}	± 5.0	—	—	± 5.0	—	—	Vdc
High Level Output Voltage ($V_{ID} \geq 5.0$ mV, $0 \leq I_O \leq 5.0$ mA)	V_{OH}	2.5	3.2	4.0	2.5	3.2	4.0	Vdc
Low Level Output Voltage ($V_{ID} \geq -5.0$ mV, $I_{OS} = 2.8$ mA) ($V_{ID} \geq -5.0$ mV, $I_{OS} = 1.6$ mA)	V_{OL}	-1.0 —	-0.5 —	0 —	— -1.0	— -0.5	— 0	Vdc
Output Sink Current ($V_{ID} \geq -5.0$ mV, $V_{OL} \leq 0.4$ V, $T_A = T_{low}$ to T_{high})	I_{OS}	2.8	3.4	—	1.6	2.5	—	mAdc
Input Common Mode Voltage Range ($V_{EE} = -7.0$ Vdc)	V_{ICR}	± 5.0	—	—	± 5.0	—	—	Vdc
Common-Mode Rejection Ratio ($V_{EE} = -7.0$ Vdc, $R_S \leq 200$ Ω)	CMRR	80	100	—	70	100	—	dB
Strobe Low Level Current ($V_{IL} = 0$)	I_{IL}	—	—	2.5	—	—	2.5	mA
Strobe High Level Current ($V_{IH} = 5.0$ Vdc)	I_{IH}	—	—	1.0	—	—	1.0	μA
Strobe Disable Voltage ($V_{OL} \leq 0.4$ Vdc)	V_{IL}	—	—	0.4	—	—	0.4	Vdc
Strobe Enable Voltage ($V_{OH} \geq 2.4$ Vdc)	V_{IH}	3.5	—	6.0	3.5	—	6.0	Vdc
Propagation Delay Time (Figure 1)	t_{PLH} t_{PHL}	—	20 40	—	—	20 40	—	ns
Strobe Response Time (Figure 2)	t_{so} t_{sr}	—	15 6.0	—	—	15 6.0	—	ns
Total Power Supply Current, Both Comparators ($V_O \leq 0$)	I_{CC} I_{EE}	—	12.8 11	18 14	—	12.8 11	18 14	mAdc
Total Power Consumption, Both Comparators	P_D	—	230	300	—	230	300	mW

* $T_{low} = -55^\circ\text{C}$ for MC1514, 0°C for MC1414

$T_{high} = +125^\circ\text{C}$ for MC1514, $+75^\circ\text{C}$ for MC1414

FIGURE 1 — PROPAGATION DELAY TIME

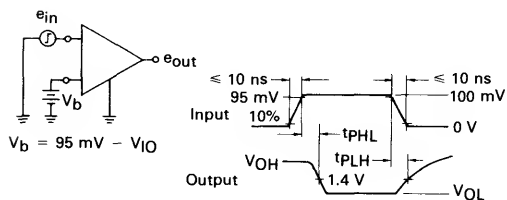
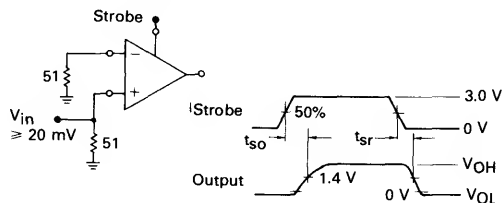


FIGURE 2 — STROBE RESPONSE TIME



MC1414, MC1514

TYPICAL CHARACTERISTICS (Each Comparator)

FIGURE 3 — VOLTAGE TRANSFER CHARACTERISTICS

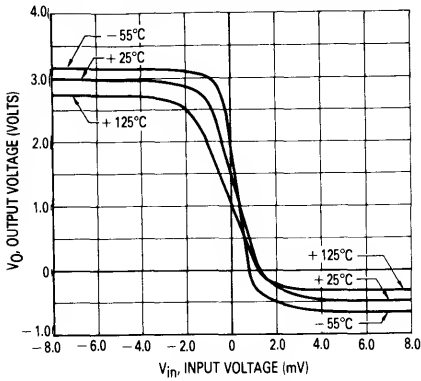


FIGURE 4 — INPUT OFFSET VOLTAGE versus TEMPERATURE

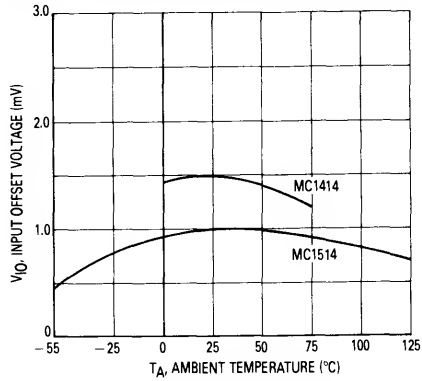


FIGURE 5 — INPUT OFFSET CURRENT versus TEMPERATURE

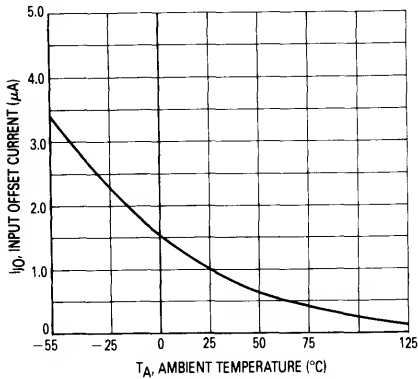


FIGURE 6 — INPUT BIAS CURRENT versus TEMPERATURE

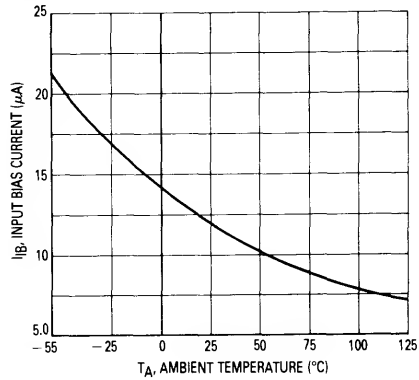


FIGURE 7 — GAIN VARIATION WITH POWER SUPPLY VOLTAGE

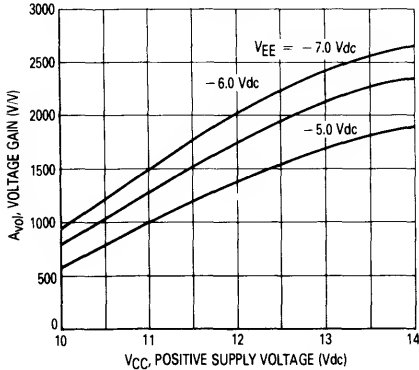
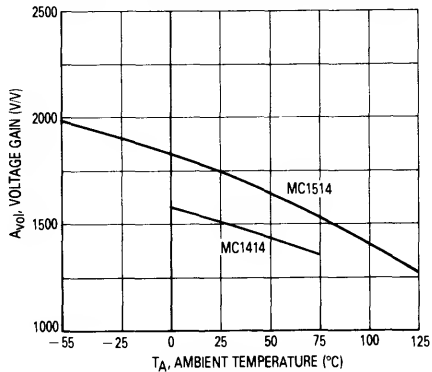


FIGURE 8 — VOLTAGE GAIN versus TEMPERATURE



MC1414, MC1514

2

FIGURE 9 — RESPONSE TIME

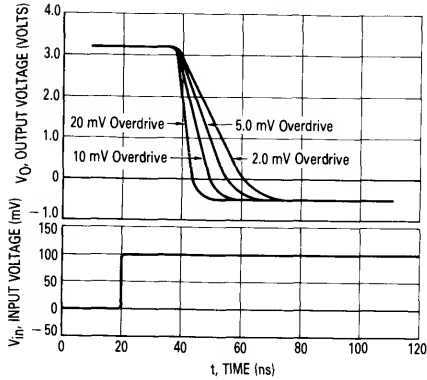


FIGURE 10 — POWER DISSIPATION versus TEMPERATURE

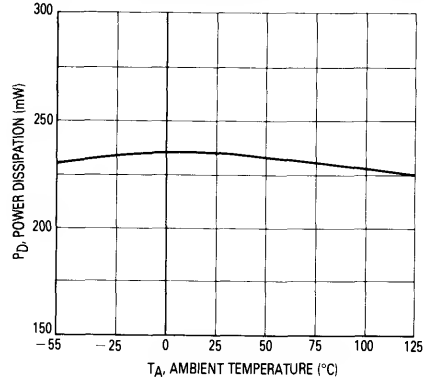


FIGURE 11 — RECOMMENDED SERIES RESISTANCE versus MRTL LOADS

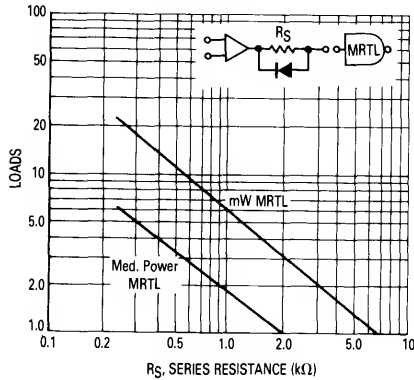


FIGURE 12 — SINK CURRENT versus TEMPERATURE

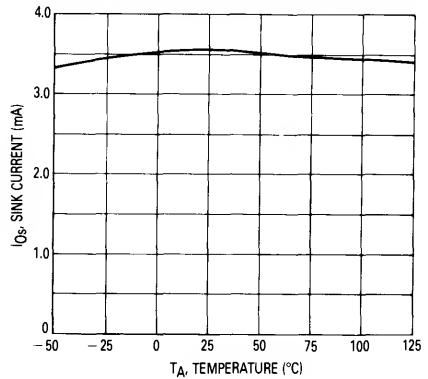
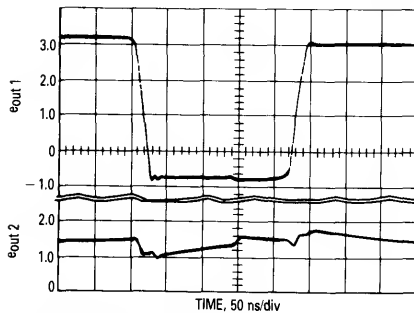
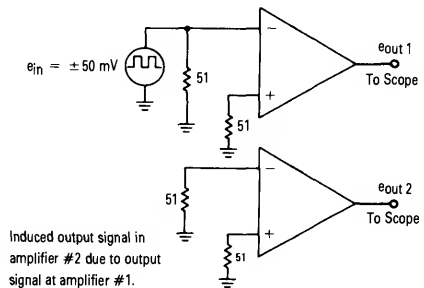


FIGURE 13 — CROSSTALK†



†Worst case condition shown — no load.



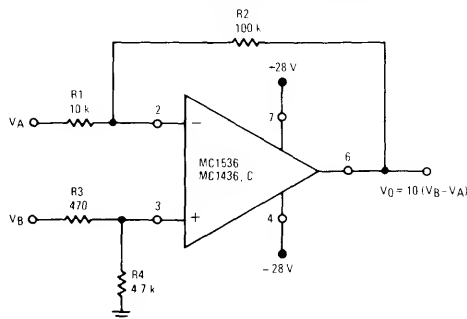
Induced output signal in amplifier #2 due to output signal at amplifier #1.

**HIGH VOLTAGE, INTERNALLY COMPENSATED
 OPERATIONAL AMPLIFIER**

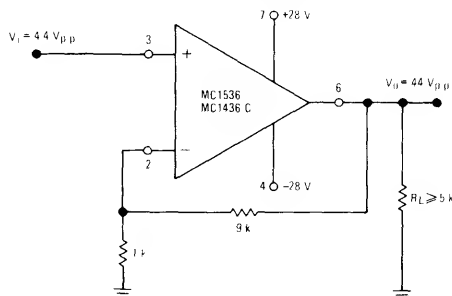
... designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- Maximum Supply Voltage — ± 40 Vdc (MC1536)
- Output Voltage Swing —
 ± 30 V_{pk(min)} ($V_{CC} = +36$ V, $V_{EE} = -36$ V) (MC1536)
 ± 22 V_{pk(min)} ($V_{CC} = +28$ V, $V_{EE} = -28$ V)
- Input Bias Current — 20 nA max (MC1536)
- Input Offset Current — 3.0 nA max (MC1536)
- Fast Slew Rate — 2.0 V/ μ s typ
- Internally Compensated
- Offset Voltage Null Capability
- Input Over-Voltage Protection
- A_{VOL} — 500,000 typ
- Characteristics Independent of Power Supply Voltages —
 (± 5.0 Vdc to ± 36 Vdc)

**FIGURE 1 — DIFFERENTIAL AMPLIFIER WITH ± 20 V
 COMMON MODE INPUT VOLTAGE RANGE**



**FIGURE 2 — TYPICAL NONINVERTING X10
 VOLTAGE AMPLIFIER**



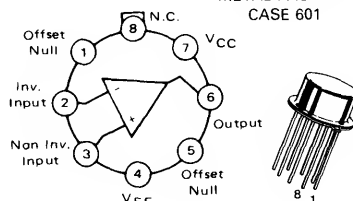
MC1436
MC1436C
MC1536

2

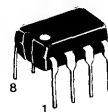
OPERATIONAL AMPLIFIER

**SILICON MONOLITHIC
 INTEGRATED CIRCUIT**

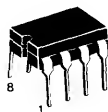
G SUFFIX
METAL PACKAGE
CASE 601



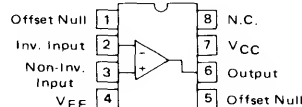
P1 SUFFIX
PLASTIC PACKAGE
CASE 626



U SUFFIX
CERAMIC PACKAGE
CASE 693



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)



ORDERING INFORMATION

Device	Temperature Range	Package
MC1436CD,D MC1436P1,CP1 MC1436CG,G MC1436CU,U	0°C to +70°C	SO-8 Plastic DIP Metal Can Ceramic DIP
MC1536G MC1536U	-55°C to +125°C	Metal Can Ceramic DIP

MC1436, MC1436C, MC1536

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	MC1536	MC1436	MC1436C	Unit
Power Supply Voltage	V_{CC} V_{EE}	+40 -40	+34 -34	+30 -30	Vdc
Input Differential Voltage Range	V_{IDR}	Note 3			Volts
Input Common-Mode Voltage Range	V_{ICR}	Note 3			Volts
Output Short Circuit Duration ($V_{CC} = V_{EE} = 28 \text{ Vdc}$, $V_O = 0$)	t_S	5.0			s
Power Dissipation (Package Limitation) Derate above $T_A = +25^\circ\text{C}$	P_D	680 4.6			mW/ $^\circ\text{C}$
Operating Ambient Temperature Range	T_A	-55 to +125			$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150			$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($V_{CC} = +28 \text{ Vdc}$, $V_{EE} = -28 \text{ Vdc}$, $T_A = +25^\circ\text{C}$ unless otherwise noted)

Characteristics	Symbol	MC1536			MC1436			MC1436C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Bias Current $T_A = +25^\circ\text{C}$ $T_A = T_{\text{low}} \text{ to } T_{\text{high}}$ (See Note 1)	I_{IB}	-	8.0	20 35	-	15	40 55	-	25	90	nAdc
Input Offset Current $T_A = +25^\circ\text{C}$ $T_A = +25^\circ\text{C} \text{ to } T_{\text{high}}$ $T_A = T_{\text{low}} \text{ to } +25^\circ\text{C}$	I_{IO}	-	1.0	3.0 4.5 7.0	-	5.0	10 14 14	-	10	25	nAdc
Input Offset Voltage $T_A = +25^\circ\text{C}$ $T_A = T_{\text{low}} \text{ to } T_{\text{high}}$	V_{IO}	-	2.0	5.0 7.0	-	5.0	10 14	-	5.0	12	mVdc
Differential Input Impedance (Open-Loop, $f \leq 5.0 \text{ Hz}$)											
Parallel Input Resistance	r_P	-	10	-	-	10	-	-	10	-	Meg ohms
Parallel Input Capacitance	C_P	-	2.0	-	-	2.0	-	-	2.0	-	pF
Common-Mode Input Impedance ($f \leq 5.0 \text{ Hz}$)	Z_{ic}	-	250	-	-	250	-	-	250	-	Meg ohms
Input Common Mode Voltage Range	V_{ICR}	± 24	± 25	-	± 22	± 25	-	± 18	± 20	-	Vpk
Equivalent Input Noise Voltage ($A_V = 100$, $R_S = 10 \text{ k ohms}$, $f = 1.0 \text{ kHz}$, $8W = 1.0 \text{ Hz}$)	e_n	-	50	-	-	50	-	-	50	-	nV/(Hz) $^{1/2}$
Common-Mode Rejection Ratio (dc)	CMRR	80	110	-	70	110	-	50	90	-	dB
Large Signal dc Open Loop Voltage Gain ($V_O = \pm 10 \text{ V}$, $R_L = 100 \text{ k ohms}$) $\left\{ \begin{array}{l} T_A = +25^\circ\text{C} \\ T_A = T_{\text{low}} \text{ to } T_{\text{high}} \end{array} \right.$ ($V_O = \pm 10 \text{ V}$, $R_L = 10 \text{ k ohms}$, $T_A = +25^\circ\text{C}$)	A_{VOL}	100,000 50,000	500,000 -	- -	70,000 50,000	500,000 -	- -	50,000 -	500,000 -	- -	V/V
Power Bandwidth (Voltage Follower) ($A_V = 1$, $R_L = 5.0 \text{ k ohms}$, $THD \leq 5\%$, $V_O = 40 \text{ Vp-p}$)	8Wp	-	23	-	-	23	-	-	23	-	kHz
Unity Gain Crossover Frequency (open-loop)	f_c	-	1.0	-	-	1.0	-	-	1.0	-	MHz
Phase Margin (open-loop, unity gain)	ϕ_m	-	50	-	-	50	-	-	50	-	degrees
Gain Margin	A_M	-	18	-	-	18	-	-	18	-	dB
Slew Rate (Unity Gain)	SR	-	2.0	-	-	2.0	-	-	2.0	-	V/ μs
Output Impedance ($f \leq 5.0 \text{ Hz}$)	Z_O	-	1.0	-	-	1.0	-	-	1.0	-	k ohms
Short-Circuit Output Current	I_{OS}	-	± 17	-	-	± 17	-	-	± 19	-	mA
Output Voltage Range ($R_L = 5.0 \text{ k ohms}$) $V_{CC} = +28 \text{ Vdc}$, $V_{EE} = -28 \text{ Vdc}$ $V_{CC} = +36 \text{ Vdc}$, $V_{EE} = -36 \text{ Vdc}$	V_{OR}	± 22 ± 30	± 23 ± 32	- -	± 20	± 22	- -	± 20	± 22	-	Vpk
Power Supply Sensitivity (dc) V_{EE} - constant, $R_S \leq 10 \text{ k ohms}$ V_{CC} - constant, $R_S \leq 10 \text{ k ohms}$	PSS+ PSS-	-	15 15	100 100	-	35 35	200 200	-	50 50	-	$\mu\text{V/V}$
Power Supply Current (See Note 2)	I_{CC} I_{EE}	-	2.2 2.2	4.0 4.0	-	2.6 2.6	5.0 5.0	-	2.6 2.6	5.0 5.0	mA
DC Quiescent Power Consumption ($V_O = 0$)	P_C	-	124	224	-	146	280	-	146	280	mW

Note 1 $T_{\text{low}} = 0^\circ\text{C}$ for MC1436C
-55 $^\circ\text{C}$ for MC1536
 $T_{\text{high}} = +70^\circ\text{C}$ for MC1436C
+125 $^\circ\text{C}$ for MC1536

Note 2 $V_{CC} = V_{EE} = 5.0 \text{ Vdc}$ to 36 Vdc for MC1536
 $V_{CC} = V_{EE} = 5.0 \text{ Vdc}$ to 30 Vdc for MC1436
 $V_{CC} = V_{EE} = 5.0 \text{ Vdc}$ to 28 Vdc for MC1436C

Note 3: Either or both input voltages must not exceed the magnitude of V_{CC} or $V_{EE} + 3.0$ volts.

MC1436, MC1436C, MC1536

FIGURE 3 — LOW-DRIFT SAMPLE AND HOLD

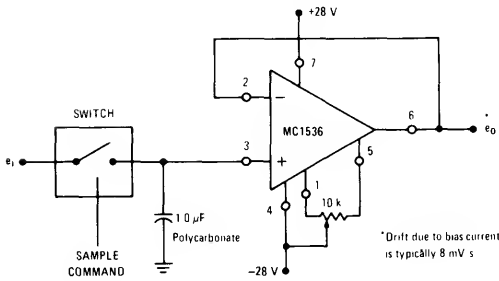


FIGURE 4 — POWER BANDWIDTH

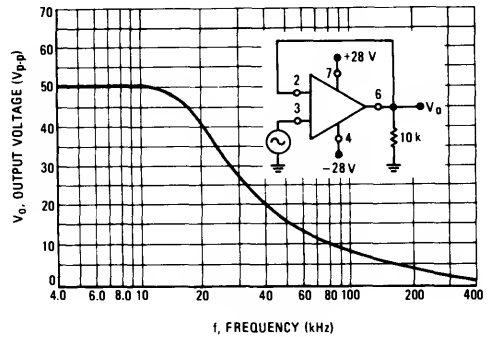


FIGURE 5 — PEAK OUTPUT VOLTAGE SWING versus POWER SUPPLY VOLTAGE

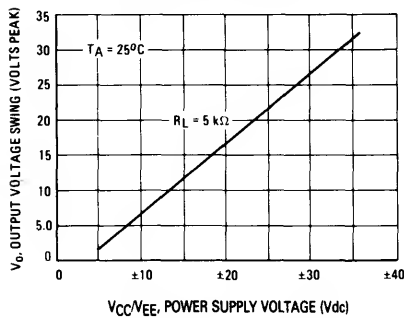


FIGURE 6 — OPEN-LOOP FREQUENCY RESPONSE

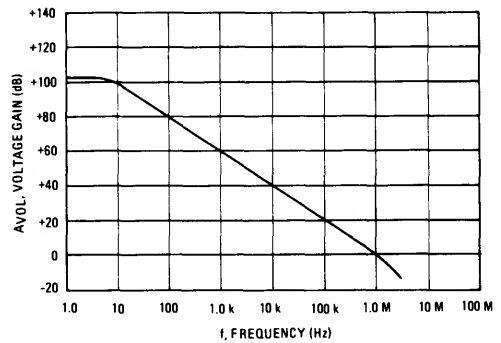


FIGURE 7 — OUTPUT SHORT-CIRCUIT CURRENT versus TEMPERATURE

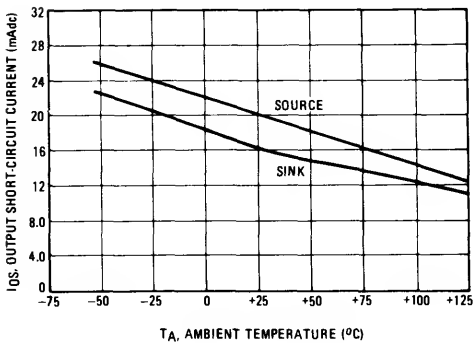
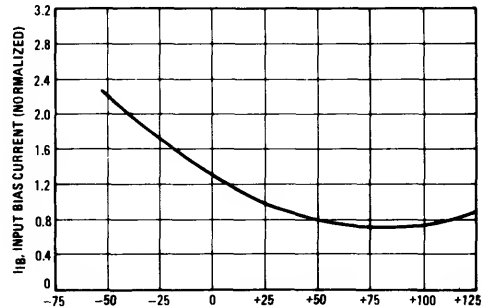


FIGURE 8 — INPUT BIAS CURRENT versus TEMPERATURE



MC1436, MC1436C, MC1536

FIGURE 9 — INVERTING FEEDBACK MODEL

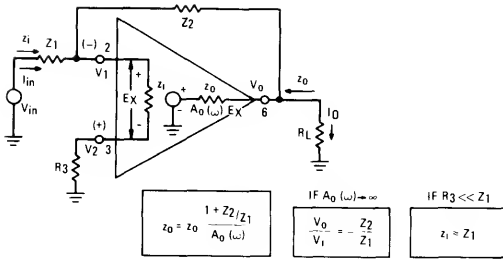


FIGURE 10 — NON-INVERTING FEEDBACK MODEL

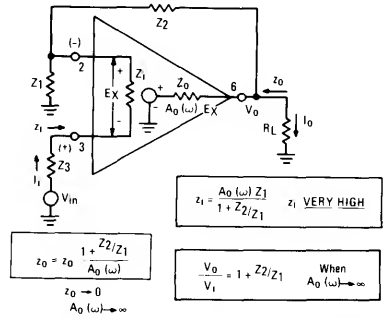


FIGURE 11 — AUDIO AMPLIFIER

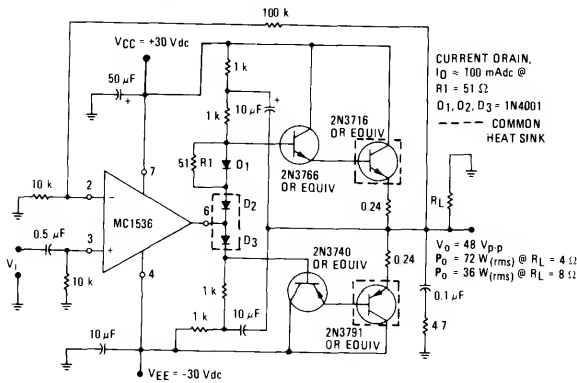


FIGURE 12 — VOLTAGE CONTROLLED CURRENT SOURCE OR TRANSCONDUCTANCE AMPLIFIER WITH 0 TO 40 V COMPLIANCE

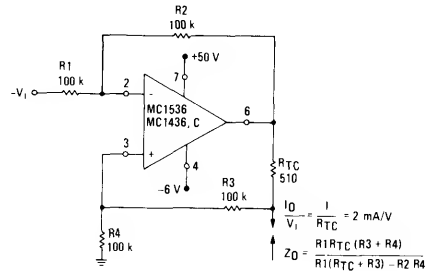


FIGURE 13 — REPRESENTATIVE CIRCUIT SCHEMATIC

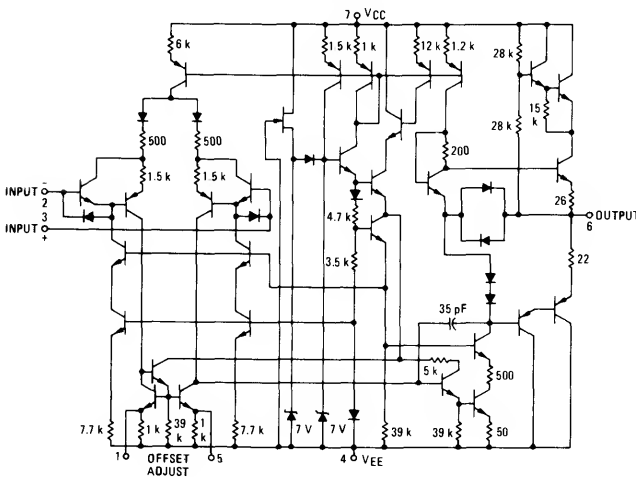
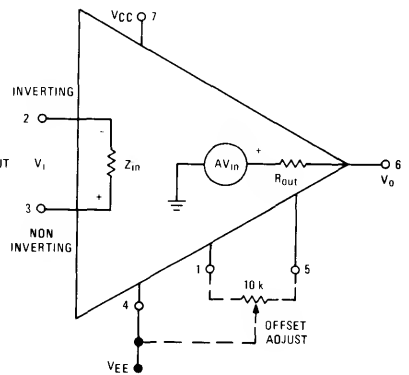


FIGURE 14 — EQUIVALENT CIRCUIT



MATCHED DUAL OPERATIONAL AMPLIFIERS

... designed for use as summing amplifiers, integrators, or amplifiers with operating characteristics as a function of the external feedback components. Ideal for chopper stabilized applications where extremely high gain is required with excellent stability.

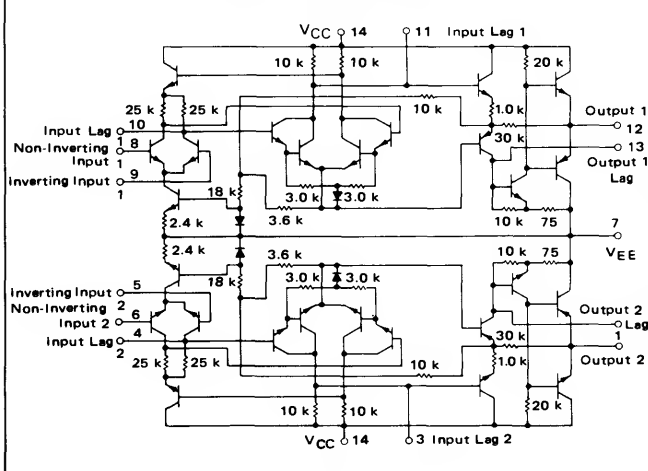
Typical Amplifier Features:

- High-Performance Open Loop Gain Characteristics – $AVOL = 45,000$ typical
- Low Temperature Drift – $\pm 3 \mu V/^{\circ}C$
- Large Output Voltage Swing – $\pm 14 V$ typical @ $\pm 15 V$ Supply

MAXIMUM RATINGS ($T_A = +25^{\circ}C$)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+18	Vdc
	V_{EE}	-18	Vdc
Differential Input Voltage Range	V_{IDR}	± 5.0	Volts
Common-Mode Input Voltage Range	V_{ICR}	$\pm V_{CC}$	Volts
Output Short Circuit Duration	t_S	5.0	s
Power Dissipation (Package Limitation)	P_D		
Ceramic Package		750	mW
Derate above $T_A = +25^{\circ}C$		6.0	mW/ $^{\circ}C$
Plastic Package MC1437P		625	mW
Derate above $T_A = +25^{\circ}C$		5.0	mW/ $^{\circ}C$
Operating Ambient Temperature Range	T_A	-55 to +125 0 to +70	$^{\circ}C$
Storage Temperature Range	T_{stg}	-65 to +150	$^{\circ}C$

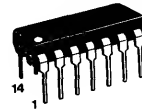
FIGURE 1 – CIRCUIT SCHEMATIC



MC1437 MC1537

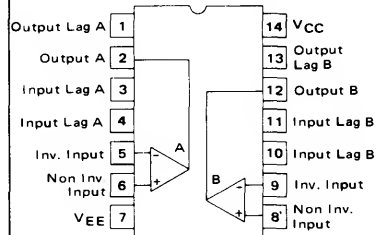
DUAL MC1709 OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 646
(MC1437P Only)

PIN CONNECTIONS



L SUFFIX
CERAMIC PACKAGE
CASE 632

ORDERING INFORMATION

Device	Temperature Range	Package
MC1437L	$0^{\circ}C$ to $+70^{\circ}C$	Ceramic DIP
MC1437P	$0^{\circ}C$ to $+70^{\circ}C$	Plastic DIP
MC1537L	$-55^{\circ}C$ to $+125^{\circ}C$	Ceramic DIP

MC1437, MC1537

ELECTRICAL CHARACTERISTICS – Each Amplifier ($V_{CC} = +15\text{ Vdc}$, $V_{EE} = -15\text{ Vdc}$, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	MC1537			MC1437			Unit
		Min	Typ	Max	Min	Typ	Max	
Open Loop Voltage Gain ($R_L = 5.0\text{ k}\Omega$, $V_O = \pm 10\text{ V}$, $T_A = T_{\text{low}} \textcircled{1}$ to $T_{\text{high}} \textcircled{2}$)	A_{VOL}	25,000	45,000	70,000	15,000	45,000	—	—
Output Impedance ($f = 20\text{ Hz}$)	z_o	—	30	—	—	30	—	Ω
Input Impedance ($f = 20\text{ Hz}$)	z_i	150	400	—	50	150	—	$\text{k}\Omega$
Output Voltage Range ($R_L = 10\text{ k}\Omega$) ($R_L = 2.0\text{ k}\Omega$)	V_{OR}	± 12 ± 10	± 14 ± 13	— —	± 12 —	± 14 —	— —	V_{peak}
Input Common-Mode Voltage Range	V_{ICR}	± 8.0	± 10	—	± 8.0	± 10	—	V_{peak}
Common-Mode Rejection Ratio	CMRR	70	100	—	65	100	—	dB
Input Bias Current ($I_{IB} = \frac{I_1 + I_2}{2}$) ($T_A = +25^\circ\text{C}$) ($T_A = T_{\text{low}} \textcircled{1}$)	I_{IB}	— —	0.2 0.5	0.5 1.5	— —	0.4 —	1.5 2.0	μA
Input Offset Current ($I_{IO} = I_1 - I_2$) ($I_{IO} = I_1 - I_2$, $T_A = T_{\text{low}} \textcircled{1}$) ($I_{IO} = I_1 - I_2$, $T_A = T_{\text{high}} \textcircled{2}$)	I_{IO}	— — —	0.05 — —	0.2 0.5 0.2	— — —	0.05 — —	0.5 0.75 0.75	μA
Input Offset Voltage ($T_A = +25^\circ\text{C}$) ($T_A = T_{\text{low}} \textcircled{1}$ to $T_{\text{high}} \textcircled{2}$)	V_{IO}	— —	1.0 —	5.0 6.0	— —	1.0 —	7.5 10	mV
Step Response { Gain = 100, 5% overshoot, $R_1 = 1\text{ k}\Omega$, $R_2 = 100\text{ k}\Omega$, $R_3 = 1.5\text{ k}\Omega$, $C_1 = 100\text{ pF}$, $C_2 = 3.0\text{ pF}$ }	t_{TLH} t_{PLH} - t_{PHL} SR	— — —	0.8 0.38 12	— — —	— 0.38 12	0.8 — —	— — —	μs μs $\text{V}/\mu\text{s}$
{ Gain = 10, 10% overshoot, $R_1 = 1\text{ k}\Omega$, $R_2 = 10\text{ k}\Omega$, $R_3 = 1.5\text{ k}\Omega$, $C_1 = 500\text{ pF}$, $C_2 = 20\text{ pF}$ }	t_{TLH} t_{PLH} - t_{PHL} SR	— — —	0.6 0.34 1.7	— — —	— 0.34 1.7	0.6 — —	— — —	μs μs $\text{V}/\mu\text{s}$
{ Gain = 1, 5% overshoot, $R_1 = 10\text{ k}\Omega$, $R_2 = 10\text{ k}\Omega$, $R_3 = 1.5\text{ k}\Omega$, $C_1 = 5000\text{ pF}$, $C_2 = 200\text{ pF}$ }	t_{TLH} t_{PLH} - t_{PHL} SR	— — —	2.2 1.3 0.25	— — —	— 1.3 0.25	2.2 — —	— — —	μs μs $\text{V}/\mu\text{s}$
Average Temperature Coefficient of Input Offset Voltage ($R_S \leq 50\text{ }\Omega$, $T_A = T_{\text{low}} \textcircled{1}$ to $T_{\text{high}} \textcircled{2}$) ($R_S \leq 10\text{ k}\Omega$, $T_A = T_{\text{low}} \textcircled{1}$ to $T_{\text{high}} \textcircled{2}$)	$\Delta V_{IO}/\Delta T$	— —	1.5 3.0	— —	— —	1.5 3.0	— —	$\mu\text{V}/^\circ\text{C}$
Average Temperature Coefficient of Input Offset Voltage ($T_A = T_{\text{low}} \textcircled{1}$ to $+25^\circ\text{C}$) ($T_A = +25^\circ\text{C}$ to $T_{\text{high}} \textcircled{2}$)	$\Delta I_{IO}/\Delta T$	— —	0.7 0.7	— —	— —	0.7 0.7	— —	nA/ $^\circ\text{C}$
DC Power Consumption (Total) (Power Supply = $\pm 15\text{ V}$, $V_O = 0$)	P_C	—	160	225	—	160	225	mW
Positive Supply Sensitivity (V_{EE} constant)	PSS+	—	10	150	—	10	200	$\mu\text{V}/\text{V}$
Negative Supply Sensitivity (V_{CC} constant)	PSS-	—	10	150	—	10	200	$\mu\text{V}/\text{V}$

$\textcircled{1} T_{\text{low}} = 0^\circ\text{C}$ for MC1437
= -55°C for MC1537

$\textcircled{2} T_{\text{high}} = +70^\circ\text{C}$ for MC1437
= $+125^\circ\text{C}$ for MC1537

MATCHING CHARACTERISTICS

Open Loop Voltage Gain	$A_{VOL1}-A_{VOL2}$	—	± 1.0	—	—	± 1.0	—	dB
Input Bias Current	$I_{IB1}-I_{IB2}$	—	± 0.15	—	—	± 0.15	—	μA
Input Offset Current	$I_{IO1}-I_{IO2}$	—	± 0.02	—	—	± 0.02	—	μA
Average Temperature Coefficient	$\left \frac{\Delta I_{IO1}}{\Delta T} \right - \left \frac{\Delta I_{IO2}}{\Delta T} \right $	—	± 0.2	—	—	± 0.2	—	nA/ $^\circ\text{C}$
Input Offset Voltage	$V_{IO1}-V_{IO2}$	—	± 0.2	—	—	± 0.2	—	mV
Average Temperature Coefficient	$\left \frac{\Delta V_{IO1}}{\Delta T} \right - \left \frac{\Delta V_{IO2}}{\Delta T} \right $	—	± 0.5	—	—	± 0.5	—	$\mu\text{V}/^\circ\text{C}$
Channel Separation ($f = 10\text{ kHz}$)	ϵ_{o1} ϵ_{o2}	—	90	—	—	90	—	dB

MC1437, MC1537

TYPICAL OUTPUT CHARACTERISTICS

FIGURE 3 – TEST CIRCUIT
 $V_{CC} = +15 \text{ Vdc}$, $V_{EE} = 15 \text{ Vdc}$, $T_A = 25^\circ\text{C}$

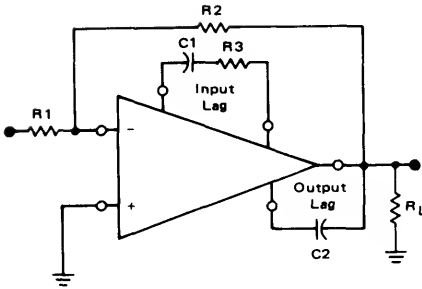


FIGURE NO.	CURVE NO.	VOLTAGE GAIN	TEST CONDITIONS					OUTPUT NOISE (mV/√Hz)
			$R_1(\Omega)$	$R_2(\Omega)$	$R_3(\Omega)$	$C_1(\mu\text{F})$	$C_2(\mu\text{F})$	
4	1	1	10 k	10 k	1.5 k	5.0 k	200	0.10
	2	10	10 k	100 k	1.5 k	500	20	0.14
	3	100	10 k	1.0 M	1.5 k	100	3.0	0.7
	4	1000	1.0 k	1.0 M	0	10	3.0	5.2
5	1	1	10 k	10 k	1.5 k	5.0 k	200	0.10
	2	10	10 k	100 k	1.5 k	500	20	0.14
	3	100	10 k	1.0 M	1.5 k	100	3.0	0.7
	4	1000	1.0 k	1.0 M	0	10	3.0	5.2
6	1	A_{VOL}	0	∞	1.5 k	5.0 k	200	5.5
	2	A_{VOL}	0	∞	1.5 k	500	20	10.5
	3	A_{VOL}	0	∞	1.5 k	100	3.0	21.0
	4	A_{VOL}	0	∞	0	10	3.0	39.0
	5	A_{VOL}	0	∞	∞	0	3.0	—

FIGURE 4 – LARGE SIGNAL SWING versus FREQUENCY

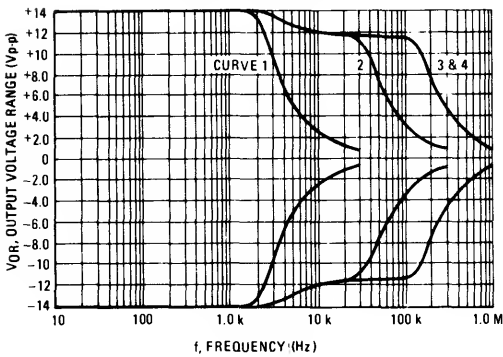


FIGURE 5 – VOLTAGE GAIN versus FREQUENCY

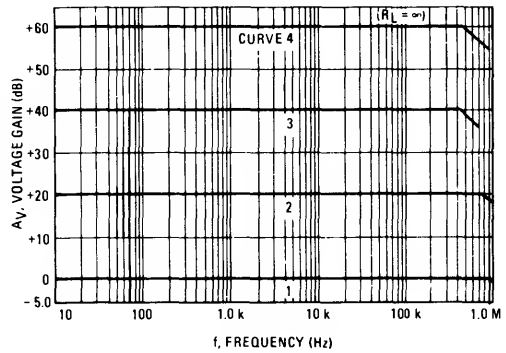


FIGURE 6 – OPEN LOOP VOLTAGE GAIN versus FREQUENCY

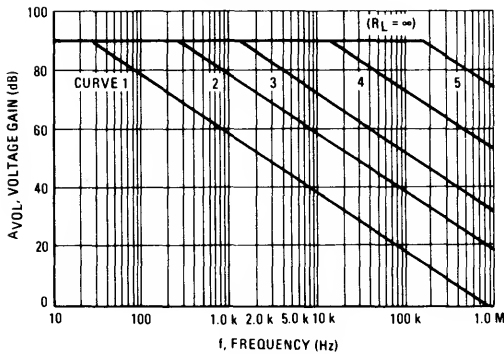
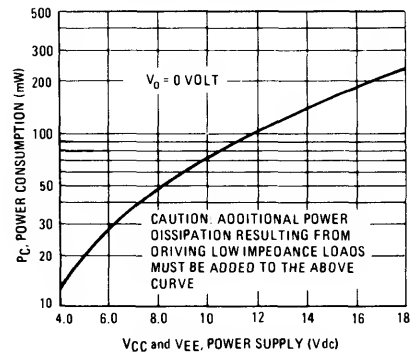


FIGURE 7 – TOTAL POWER CONSUMPTION versus POWER SUPPLY VOLTAGE



TYPICAL CHARACTERISTICS (continued)

2

FIGURE 8 — VOLTAGE GAIN versus POWER SUPPLY VOLTAGE

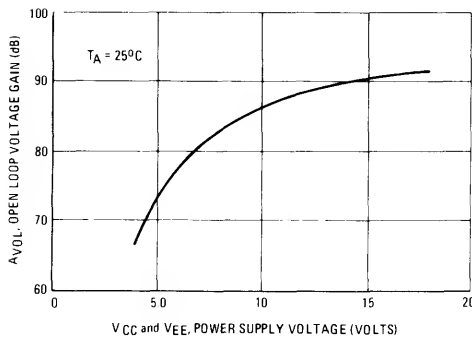


FIGURE 9 — COMMON INPUT SWING versus POWER SUPPLY VOLTAGE

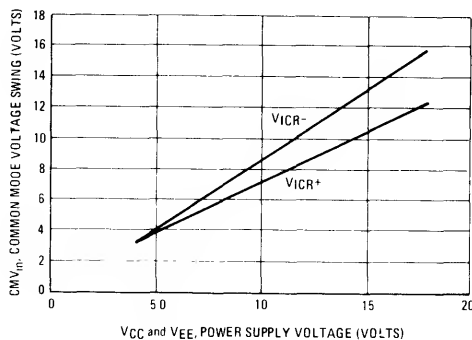


FIGURE 10 — INPUT OFFSET VOLTAGE versus TEMPERATURE

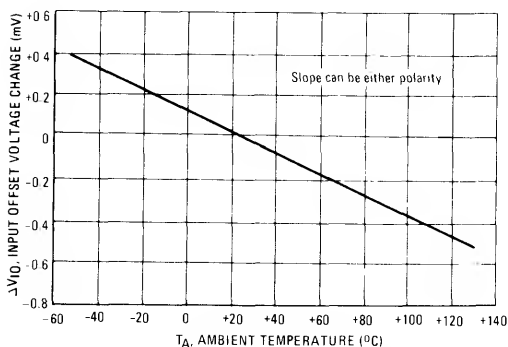


FIGURE 11 — OUTPUT NOISE VOLTAGE versus SOURCE RESISTANCE

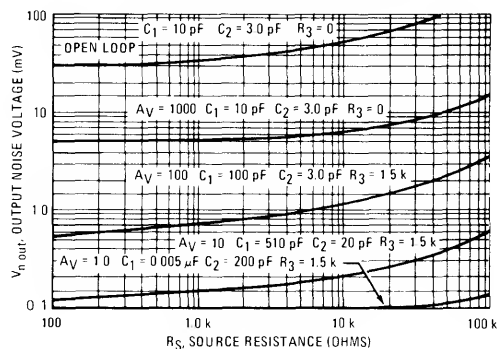
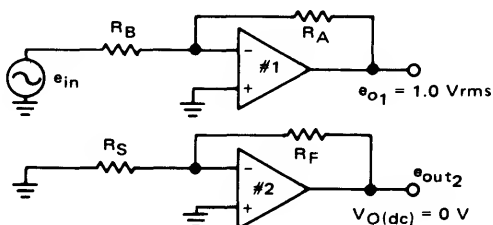
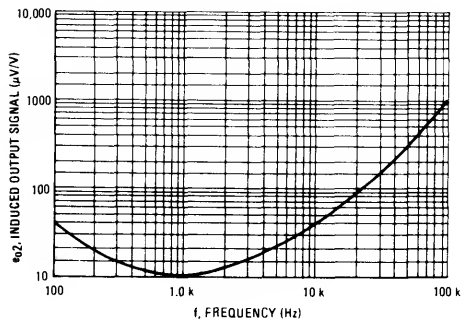


FIGURE 12 — INDUCED OUTPUT SIGNAL (CHANNEL SEPARATION) versus FREQUENCY



Induced output signal (μV of induced output signal in amplifier #2 per volt of output signal at amplifier #1).

UNCOMPENSATED OPERATIONAL AMPLIFIER

... designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- Low Input Offset Voltage — 3.0 mV max
- Low Input Offset Current — 60 nA max
- Large Power-Bandwidth — 20 Vp-p Output Swing at 20 kHz min
- Output Short-Circuit Protection
- Input Over-Voltage Protection
- Class AB Output for Excellent Linearity
- High Slew Rate — 34 V/ μ s typ

FIGURE 1 — HIGH SLEW-RATE INVERTER

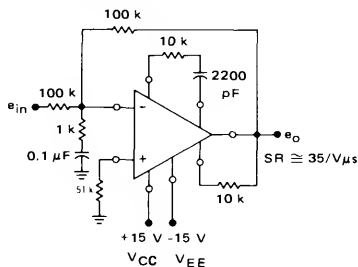


FIGURE 2 — OUTPUT NULLING CIRCUIT

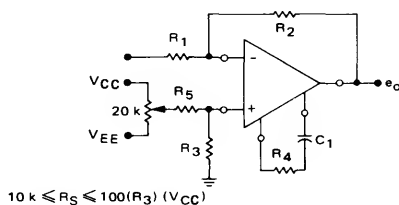
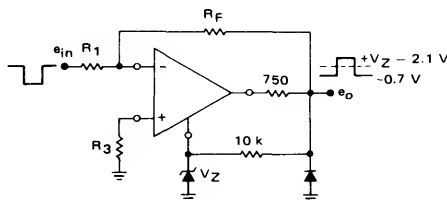


FIGURE 3 — OUTPUT LIMITING CIRCUIT

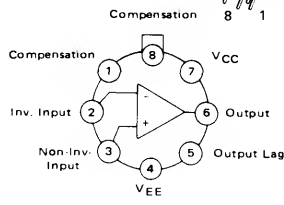


MC1439 MC1539

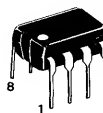
OPERATIONAL AMPLIFIER

SILICON MONOLITHIC
 INTEGRATED CIRCUIT

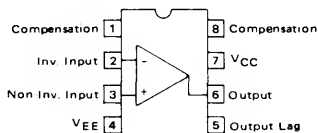
G SUFFIX
 METAL PACKAGE
 CASE 601



(Top View)



P1 SUFFIX
 PLASTIC PACKAGE
 CASE 626
 (MC1439 Only)



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC1439G	0°C to +70°C	Metal Can
MC1439P1		Plastic DIP
MC1539G	-55°C to +125°C	Metal Can

MC1439, MC1539

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC1539			MC1439			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Bias Current (T _A = +25°C) (T _A = T _{low} ①)	I _{IB}	—	0.20 0.23	0.50 0.70	—	0.20 0.23	1.0 1.5	μA
Input Offset Current (T _A = T _{low}) (T _A = +25°C) (T _A = T _{high} ①)	I _{IO}	— — —	— 20 —	75 60 75	— — —	— 20 —	150 100 150	nA
Input Offset Voltage (T _A = +25°C) (T _A = T _{low} , T _{high})	V _{IO}	— —	1.0 —	3.0 4.0	— —	2.0 —	7.5 —	mV
Average Temperature Coefficient of Input Offset Voltage (T _A = T _{low} to T _{high}) (R _S = 50 Ω) (R _S ≤ 10 kΩ)	TCV _{IO}	— —	3.0 5.0	— —	— —	3.0 5.0	— —	μV/°C
Input Impedance (f = 20 Hz)	z _{in}	150	300	—	100	300	—	kΩ
Input Common-Mode Voltage Range	V _{ICR}	±11	±12	—	±11	±12	—	V _{pk}
Equivalent Input Noise Voltage (R _S = 10 kΩ, Noise Bandwidth = 1.0 Hz, f = 1.0 kHz)	e _n	—	30	—	—	30	—	nV/(Hz) ^{1/2}
Common-Mode Rejection Ratio (f = 1.0 kHz)	CMRR	80	110	—	80	110	—	dB
Open-Loop Voltage Gain (V _O = ±10 V, R _L = 10 kΩ, R _S = ∞) (T _A = +25°C to T _{high}) (T _A = T _{low})	A _{VOL}	50,000 25,000	120,000 100,000	— —	15,000 15,000	100,000 100,000	— —	—
Power Bandwidth (A _v = 1, THD ≤ 5%, V _O = 20 V _{p-p}) (R _L = 2.0 kΩ) (R _L = 1.0 kΩ, R _S = 10 k)	PBW	— 20	— 50	— —	10 —	50 —	— —	kHz
Step Response { Gain = 1000, no overshoot, R1 = 1.0 kΩ, R2 = 1.0 MΩ, R3 = 1.0 kΩ, R4 = 30 kΩ, R5 = 10 kΩ, C1 = 1000 pF } { Gain = 1000, 15% overshoot, R1 = 1.0 kΩ, R2 = 1.0 MΩ, R3 = 1.0 kΩ, R4 = 0, R5 = 10 kΩ, C1 = 10 pF } { Gain = 100, no overshoot, R1 = 1.0 kΩ, R2 = 100 kΩ, R3 = 1.0 kΩ, R4 = 10 kΩ, R5 = 10 kΩ, C1 = 2200 pF } { Gain = 10, 15% overshoot, R1 = 1.0 kΩ, R2 = 10 kΩ, R3 = 1.0 kΩ, R4 = 1.0 kΩ, R5 = 10 kΩ, C1 = 2200 pF } { Gain = 1, 15% overshoot, R1 = 10 kΩ, R2 = 10 kΩ, R3 = 5.0 kΩ, R4 = 390 Ω, R5 = 10 kΩ, C1 = 2200 pF }	t _{THL}	—	130	—	—	130	—	ns
	t _{pd}	—	190	—	—	190	—	ns
	SR	—	6.0	—	—	6.0	—	V/μs
	t _{THL}	—	80	—	—	80	—	ns
	t _{pd}	—	100	—	—	100	—	ns
	SR	—	14	—	—	14	—	V/μs
	t _{THL}	—	60	—	—	60	—	ns
	t _{pd}	—	100	—	—	100	—	ns
	SR	—	34	—	—	34	—	V/μs
	t _{THL}	—	120	—	—	120	—	ns
	t _{pd}	—	80	—	—	80	—	ns
	SR	—	6.25	—	—	6.25	—	V/μs
Output Impedance (f = 20 Hz)	z _O	—	4.0	—	—	4.0	—	kΩ
	V _O	— ±10	— ±13	— —	±10 —	±13 —	— —	V _{pk}
	V _O	—	—	—	—	—	—	V _{pk}
Output Voltage Swing (R _L = 2.0 kΩ, f = 1.0 kHz) (R _L = 1.0 kΩ, f = 1.0 kHz)	V _O	— ±10	— ±13	— —	±10 —	±13 —	— —	V _{pk}
Positive Supply Rejection Ratio (V _{EE} constant, R _S = ∞)	PSRR+	—	50	150	—	50	200	μV/V
Negative Supply Rejection Ratio (V _{CC} constant, R _S = ∞)	PSRR-	—	50	150	—	50	200	μV/V
Power Supply Current (V _O = 0)	I _{CC} I _{EE}	— —	3.0 3.0	5.0 5.0	— —	3.0 3.0	6.7 6.7	mAdc

① T_{low} = 0°C for MC1439
— 55°C for MC1539
T_{high} = +70°C for MC1439
+125°C for MC1539

MC1439, MC1539

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 +18	Vdc
Differential Input Voltage Range	V_{IDR}	$\pm(V_{CC} + V_{EE})$	Vdc
Common-Mode Input Voltage Range	V_{ICR}	$+V_{CC} - V_{EE} $	Vdc
Load Current	I_L	15	mA
Output Short-Circuit Duration	t_S	Continuous	
Power Dissipation (Package Limitation)	P_D		
Metal Package		680	mW
Derate above $T_A = +25^\circ\text{C}$		4.6	mW/ $^\circ\text{C}$
Plastic Dual In-Line Packages MC1439		625	mW
Derate above $T_A = +25^\circ\text{C}$		5.0	mW/ $^\circ\text{C}$
Operating Temperature Range	T_A	-55 to +125 0 to +70	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150 -55 to +125	$^\circ\text{C}$

FIGURE 4 – EQUIVALENT CIRCUIT SCHEMATIC

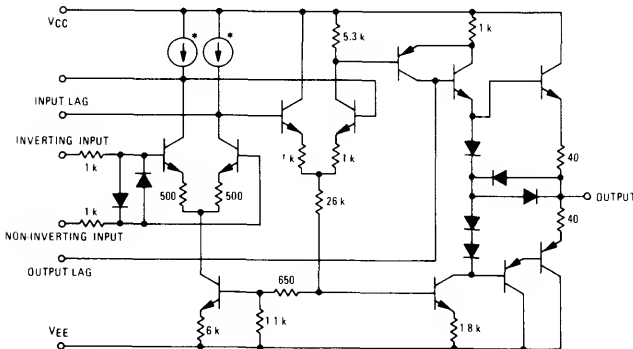


FIGURE 5 – EQUIVALENT CIRCUIT

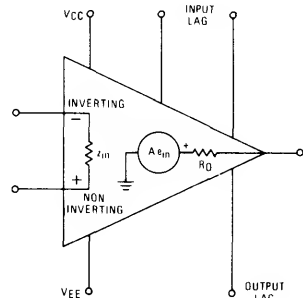
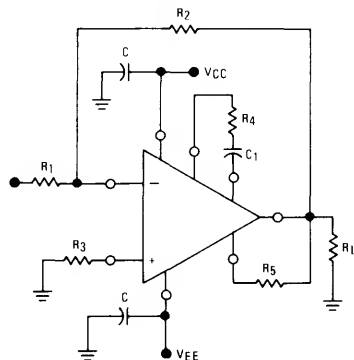


FIGURE 6 – TEST CIRCUIT



TYPICAL OUTPUT CHARACTERISTICS

$V_{CC} = +15\text{ Vdc}$, $V_{EE} = -15\text{ Vdc}$, $T_A = +25^\circ\text{C}$

FIGURE NO.	CURVE NO.	VOLTAGE GAIN	TEST CONDITIONS (FIGURE 6)					
			$R_1 (\Omega)$	$R_2 (\Omega)$	$R_3 (\Omega)$	$R_4 (\Omega)$	$R_5 (\Omega)$	$C_1 (\text{pF})$
7, 10, 12	1	A_{vcl}	0	∞	0	∞	∞	0
	2	1	10 k	10 k	50 k	390	10 k	2200
	3	10	10 k	10 k	10 k	10 k	10 k	2200
	4	100	10 k	100 k	10 k	10 k	10 k	2200
	5	1000	10 k	1.0 M	10 k	30 k	10 k	1000
	6	1000	10 k	1.0 k	1.0 M	10 k	0	10
8	1	A_{vcl}	0	∞	0	∞	∞	0
	2	1	10 k	10 k	50 k	390	10 k	2200
	3	10	10 k	10 k	10 k	10 k	10 k	2200
	4	100	10 k	100 k	10 k	10 k	10 k	2200
	5	1000	10 k	1.0 M	10 k	30 k	10 k	1000
	6	1000	10 k	1.0 k	1.0 M	10 k	0	10
13	ALL	1	10 k	10 k	50 k	390	10 k	2200
14	ALL	10	10 k	10 k	10 k	10 k	10 k	2200
15	ALL	100	10 k	100 k	10 k	10 k	10 k	2200
16	ALL	1000	10 k	1.0 M	10 k	30 k	10 k	2200

MC1439, MC1539

TYPICAL CHARACTERISTICS (continued)

($V_{CC} = +15$ Vdc, $V_{EE} = -15$ Vdc, $T_A = +25^\circ\text{C}$, unless otherwise noted.)

FIGURE 7 — LARGE-SIGNAL SWING versus FREQUENCY

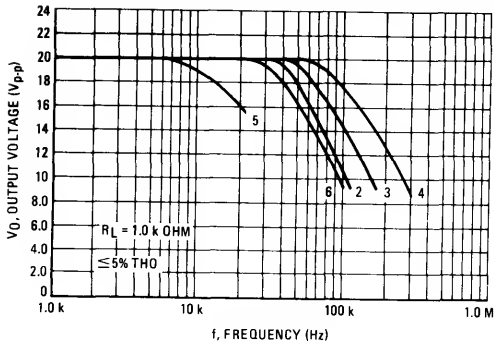


FIGURE 8 — OPEN-LOOP VOLTAGE GAIN versus FREQUENCY

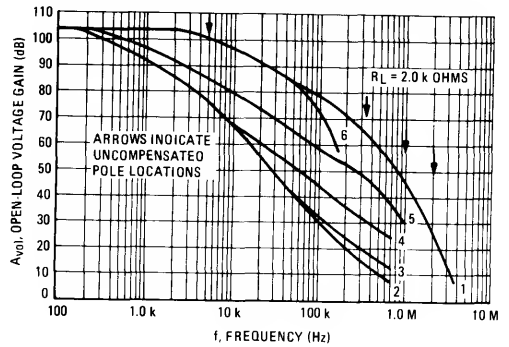


FIGURE 9 — OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

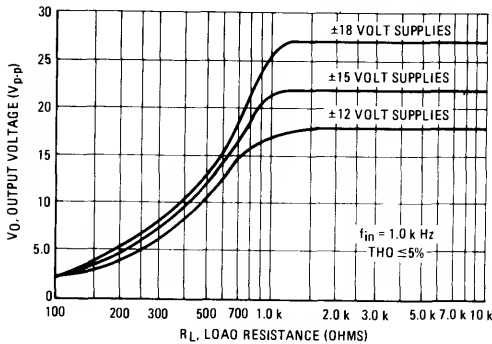


FIGURE 10 — OPEN-LOOP PHASE-SHIFT versus FREQUENCY

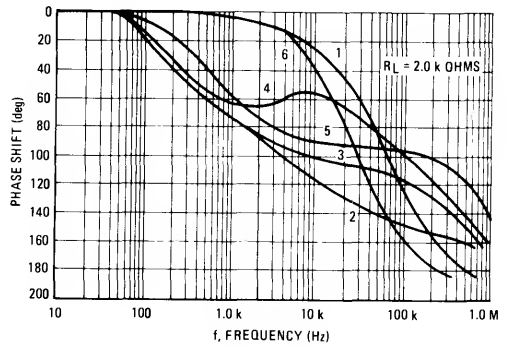


FIGURE 11 — OUTPUT VOLTAGE SWING (to clipping) versus SUPPLY

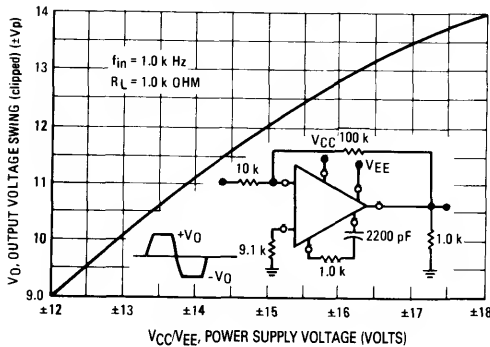
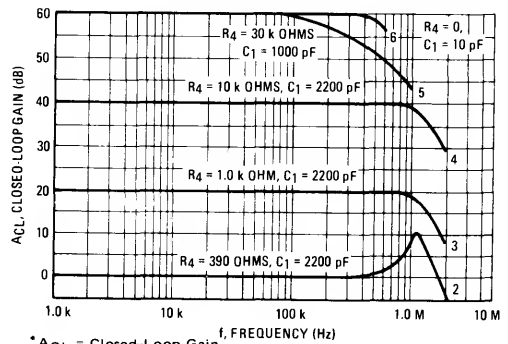


FIGURE 12 — CLOSED-LOOP GAIN versus FREQUENCY



* A_{CL} = Closed-Loop Gain

MC1439, MC1539

TYPICAL CHARACTERISTICS (continued)

($V_{CC} = +15$ Vdc, $V_{EE} = -15$ Vdc, $T_A = +25^\circ\text{C}$, unless otherwise noted.)

FIGURE 13 – $A_{CL} = 1$ RESPONSE versus TEMPERATURE

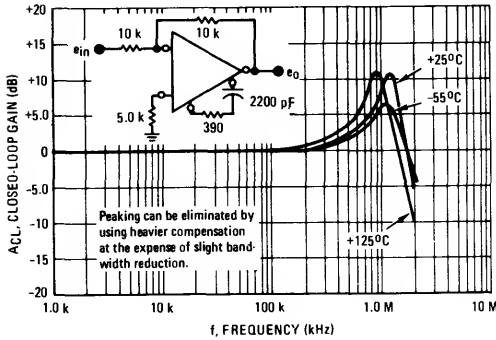


FIGURE 14 – $A_{CL} = 10$ RESPONSE versus TEMPERATURE

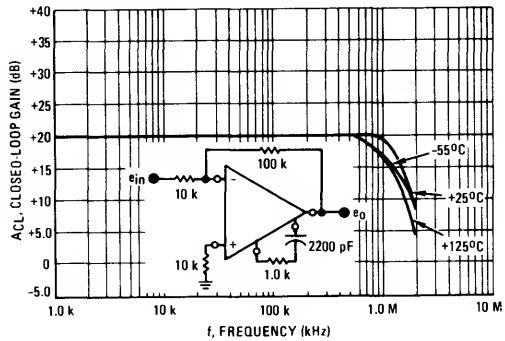


FIGURE 15 – $A_{CL} = 100$ RESPONSE versus TEMPERATURE

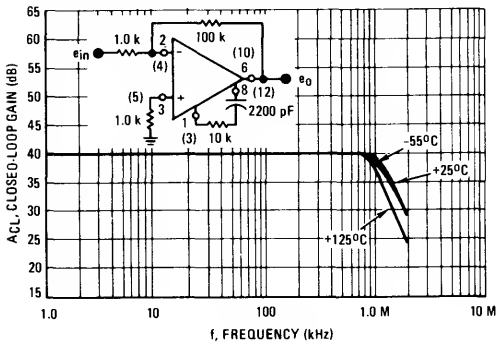


FIGURE 16 – $A_{CL} = 1000$ RESPONSE versus TEMPERATURE

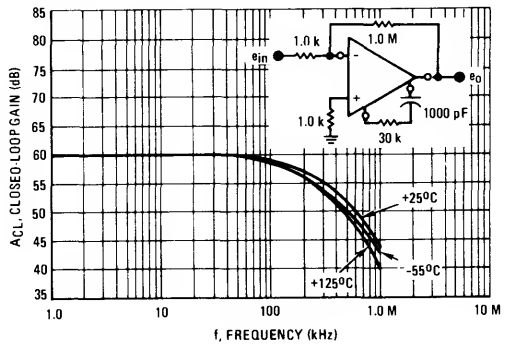
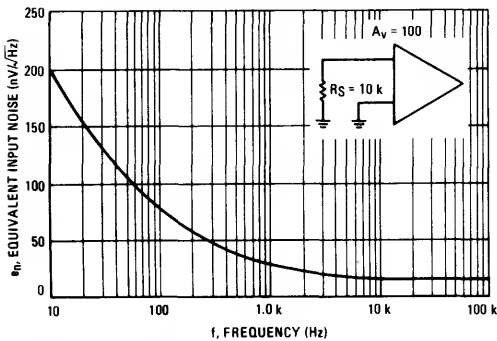
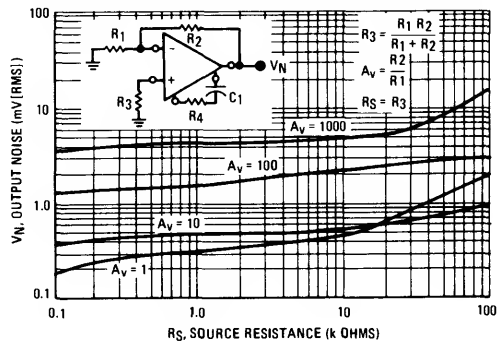


FIGURE 17 – SPECTRAL NOISE DENSITY



* A_{CL} = Closed-Loop Gain

FIGURE 18 – OUTPUT NOISE versus SOURCE RESISTANCE



MC1439, MC1539

TYPICAL CHARACTERISTICS (continued)

($V_{CC} = +15$ Vdc, $V_{EE} = -15$ Vdc, $T_A = +25^\circ\text{C}$, unless otherwise noted.)

2

FIGURE 19 — POWER DISSIPATION versus TEMPERATURE

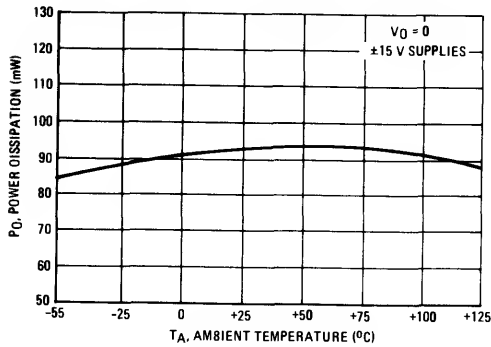


FIGURE 20 — POWER DISSIPATION versus POWER SUPPLY VOLTAGE

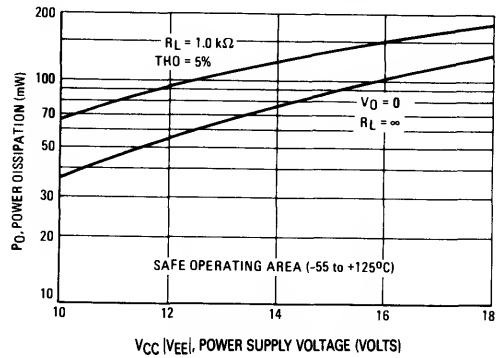


FIGURE 21 — POWER BANDWIDTH (LARGE-SIGNAL SWING versus FREQUENCY)

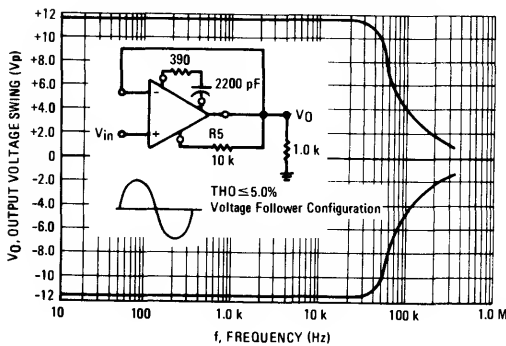


FIGURE 22 — COMMON-MODE INPUT VOLTAGE versus SUPPLY VOLTAGE

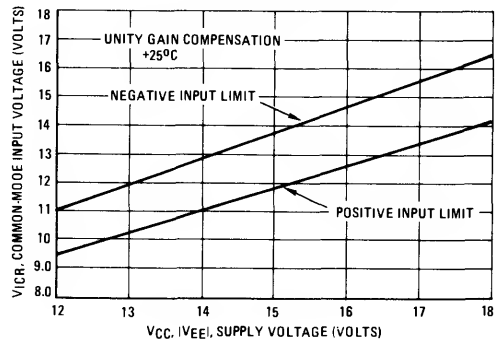


FIGURE 23 — COMMON-MODE REJECTION RATIO versus FREQUENCY

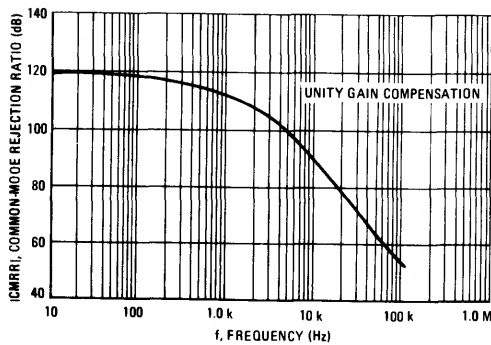
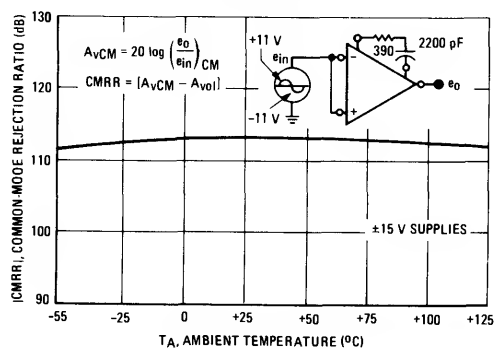
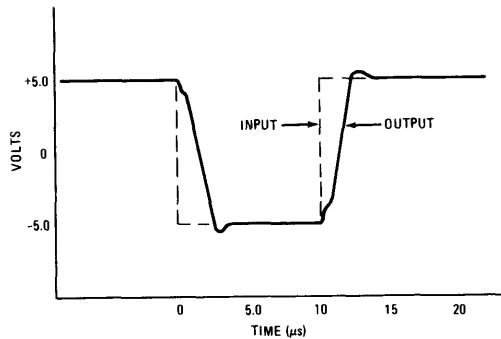


FIGURE 24 — COMMON-MODE REJECTION RATIO versus TEMPERATURE



MC1439, MC1539

FIGURE 25 – VOLTAGE-FOLLOWER PULSE RESPONSE



TYPICAL APPLICATIONS

FIGURE 26 – VOLTAGE FOLLOWER

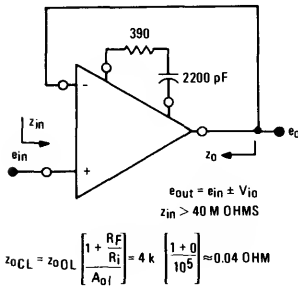


FIGURE 27 – DIFFERENTIAL AMPLIFIER

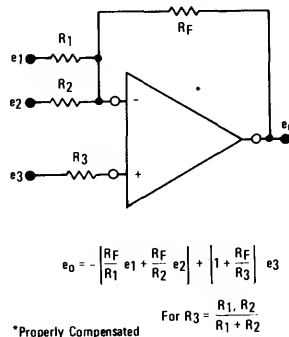


FIGURE 28 – SUMMING AMPLIFIER

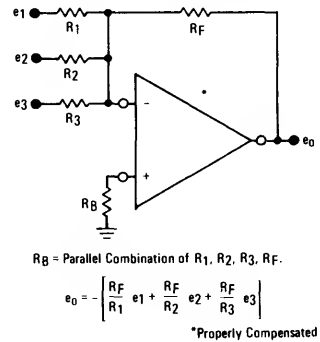
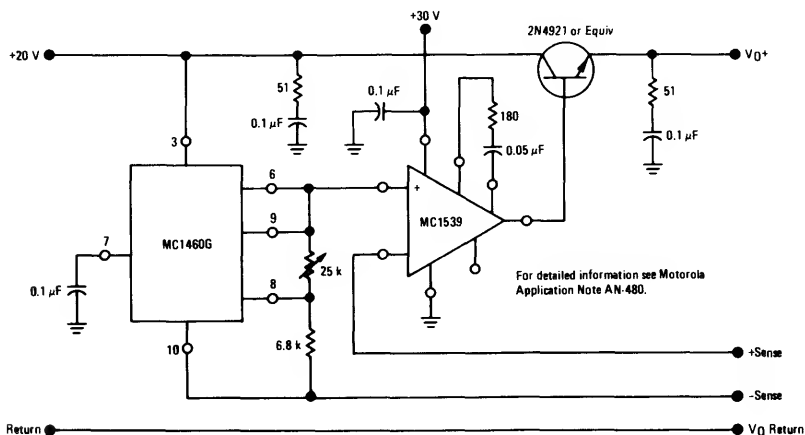
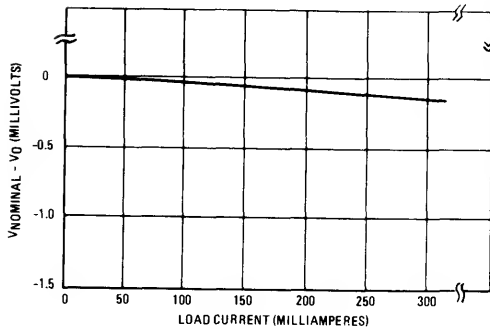
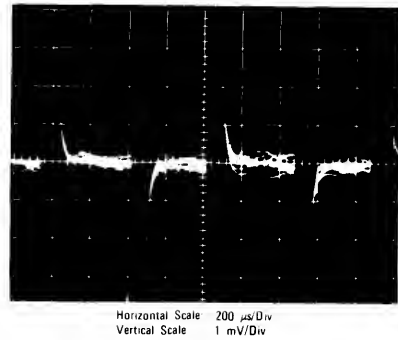


FIGURE 29 – +15 VOLT REGULATOR



TYPICAL APPLICATIONS (continued)

FIGURE 30 – LOAD REGULATION FOR
CIRCUIT OF FIGURE 29FIGURE 31 – REGULATOR OUTPUT VOLTAGE
(under pulsed load condition)

MC1445
MC1545

2

**GATE CONTROLLED TWO CHANNEL INPUT
WIDEBAND AMPLIFIER**

... designed for use as a general purpose gated wideband amplifier, video switch, sense amplifier, multiplexer, modulator, FSK circuit, limiter, AGC circuit, or pulse amplifier.

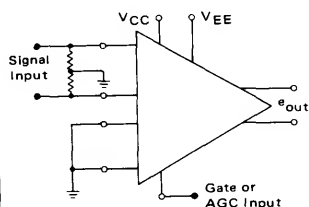
- Large Bandwidth; 50 MHz Typical
- Channel-Select Time of 20 ns Typical
- Differential Inputs and Differential Output

**GATE CONTROLLED
TWO CHANNEL INPUT
WIDEBAND AMPLIFIER**

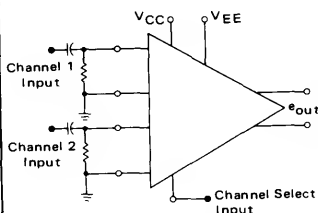
**SILICON MONOLITHIC
INTEGRATED CIRCUIT**

TYPICAL APPLICATIONS

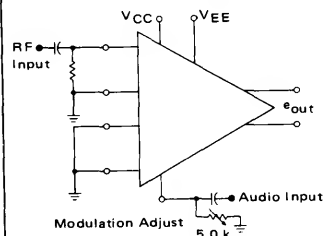
**VIDEO SWITCH OR
DIFFERENTIAL AMPLIFIER WITH AGC**



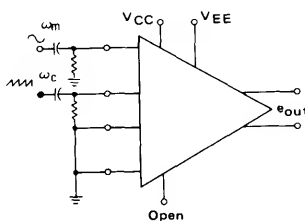
MULTIPLEX OR FSK



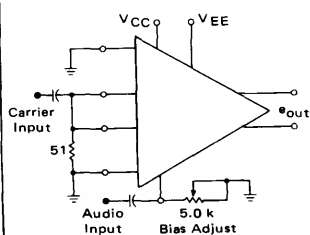
AMPLITUDE MODULATOR



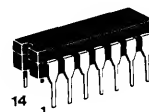
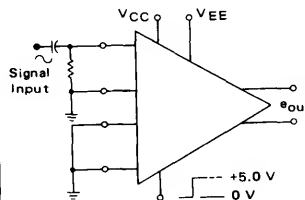
PULSE-WIDTH MODULATOR



BALANCED MODULATOR

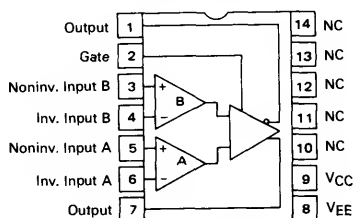


ANALOG SWITCH



**L SUFFIX
CERAMIC PACKAGE
CASE 632**

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC1445L	0°C to +75°C	Ceramic DIP
MC1545L	-55°C to +125°C	Ceramic DIP

MC1445, MC1545

2

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+12 -12	Vdc
Input Differential Voltage Range	V_{IDR}	± 5.0	Volts
Load Current	I_L	25	mA
Power Dissipation (Package Limitation)	P_D		
Ceramic Dual In-Line Package		625	mW
Derate above $T_A = +25^\circ\text{C}$		5.0	mW/ $^\circ\text{C}$
Metal Can		680	mW
Derate above $T_A = +25^\circ\text{C}$		4.6	mW/ $^\circ\text{C}$
Operating Ambient Temperature Range MC1445 MC1545	T_A	0 to +75 -55 to +125	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($V_{CC} = +5.0\text{ Vdc}$, $V_{EE} = -5.0\text{ Vdc}$, at $T_A = +25^\circ\text{C}$, specifications apply to both input channels unless otherwise noted.)

Characteristic	Fig. No.	Symbol	MC1545			MC1445			Unit
			Min	Typ	Max	Min	Typ	Max	
Single-Ended Voltage Gain	1,12	A_{VS}	16	19	21	16	19.5	23	dB
Bandwidth	1,12	BW	40	50	—	—	50	—	MHz
Input Impedance ($f = 50\text{ kHz}$)	5,14	z_i	4.0	10	—	3.0	10	—	k ohms
Output Impedance ($f = 50\text{ kHz}$)	6,15	z_o	—	25	—	—	25	—	Ohms
Output Differential Voltage Range ($R_L = 1.0\text{ k ohm}$, $f = 50\text{ kHz}$)	4,13	V_{ODR}	1.5	2.5	—	1.5	2.5	—	Vp-p
Input Bias Current	16	I_{IB}	—	15	25	—	15	30	μAdc
Input Offset Current	16	I_{IO}	—	2.0	—	—	2.0	—	μAdc
Input Offset Voltage	17	V_{IO}	—	1.0	5.0	—	—	7.5	mVdc
Quiescent Output dc Level	17	V_O	—	0.1	—	—	0.1	—	Vdc
Output dc Level Change (Gate Input Voltage Change: +5.0 V to 0 V)	17	ΔV_O	—	± 15	—	—	± 15	—	mV
Common-Mode Rejection Ratio ($f = 50\text{ kHz}$)	9,18	CMRR	—	85	—	—	85	—	dB
Input Common-Mode Voltage Range	18	V_{ICR}	—	± 2.5	—	—	± 2.5	—	Vp
Gate Characteristics	8								
Gate Input Voltage — Low Logic State (Note 1)		$V_{IL(G)}$	0.40	0.70	—	0.2	0.4	—	Vdc
Gate Input Voltage — High Logic State (Note 2)		$V_{IH(G)}$	—	1.5	2.2	—	1.3	3.0	
Gate Input Current — Low Logic State ($V_{IL(G)} = 0\text{ V}$)	18	$I_{IL(G)}$	—	—	2.5	—	—	4.0	mA
Gate Input Current — High Logic State ($V_{IH(G)} = +5.0\text{ V}$)	18	$I_{IH(G)}$	—	—	2.0	—	—	4.0	μA
Step Response ($e_{in} = 20\text{ mV}$)	19								
		t_{PLH}	—	6.5	10	—	6.5	—	ns
		t_{PHL}	—	6.3	10	—	6.3	—	
		t_{TLH}	—	6.5	15	—	6.5	—	
		t_{THL}	—	7.0	15	—	7.0	—	
Wideband Input Noise (5.0 Hz — 10 MHz, $R_S = 50\text{ ohms}$)	10,20	e_n	—	25	—	—	25	—	$\mu\text{V(rms)}$
DC Power Consumption	11,20	P_C	—	70	110	—	70	150	mW

Note 1. $V_{IL(G)}$ is the gate voltage which results in channel A gain of unity or less and channel B gain of 16 dB or greater.

Note 2. $V_{IH(G)}$ is the gate voltage which results in channel B gain of unity or less and channel A gain of 16 dB or greater.

FIGURE 1 – SINGLE-ENDED
VOLTAGE GAIN versus FREQUENCY

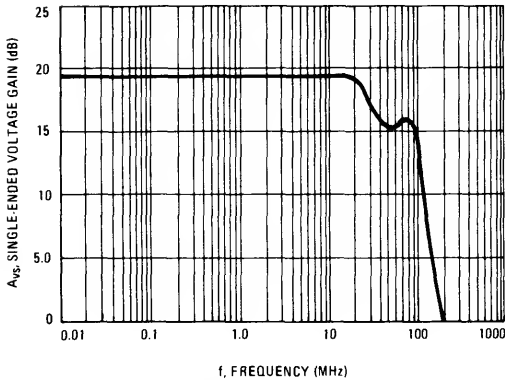


FIGURE 3 – VOLTAGE GAIN
versus POWER SUPPLY VOLTAGES

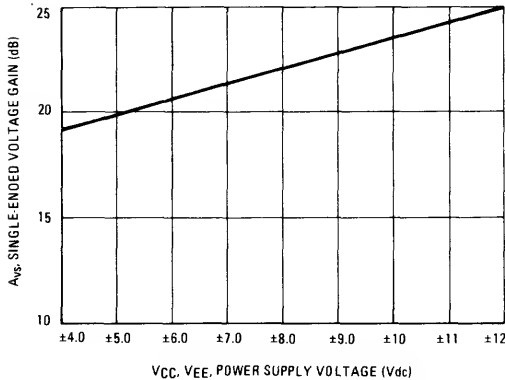


FIGURE 5 – INPUT C_p AND R_p versus FREQUENCY
(BOTH CHANNELS)

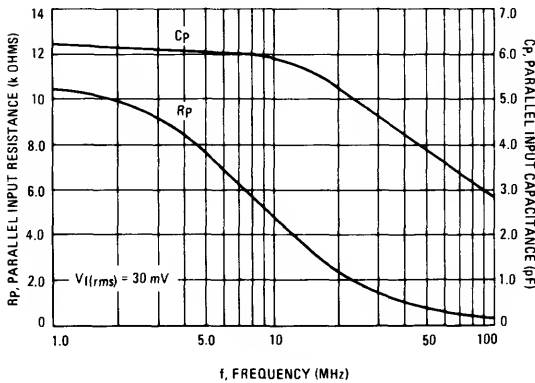


FIGURE 2 – SINGLE-ENDED
VOLTAGE GAIN versus TEMPERATURE

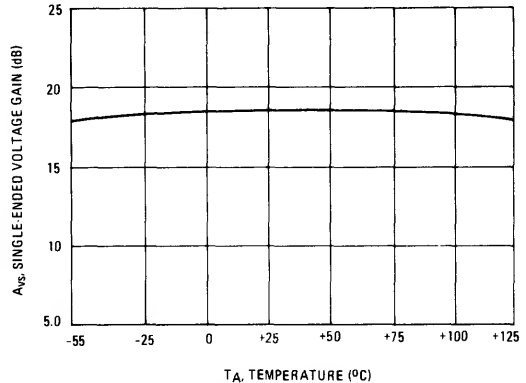


FIGURE 4 – OUTPUT VOLTAGE SWING
versus LOAD RESISTANCE

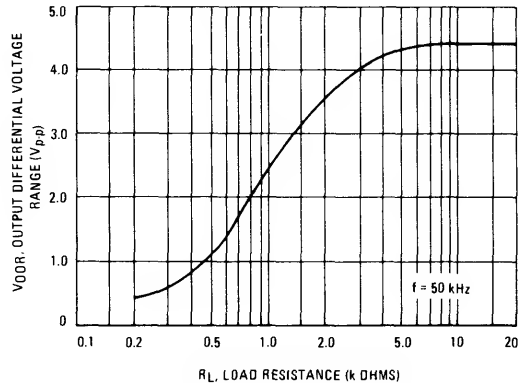


FIGURE 6 – OUTPUT IMPEDANCE versus FREQUENCY

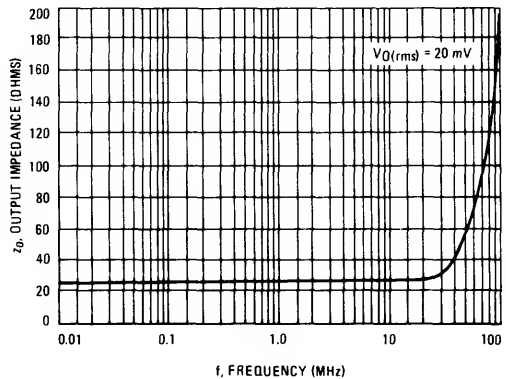


FIGURE 7 – CHANNEL SEPARATION versus FREQUENCY

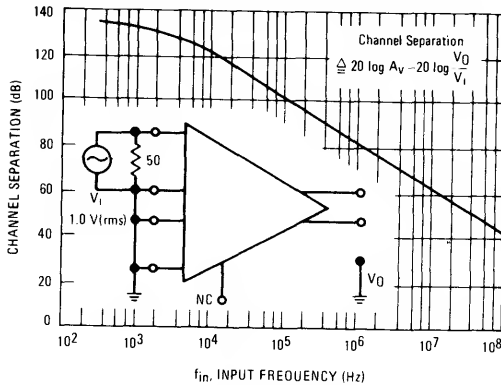


FIGURE 9 – COMMON MODE REJECTION RATIO versus FREQUENCY

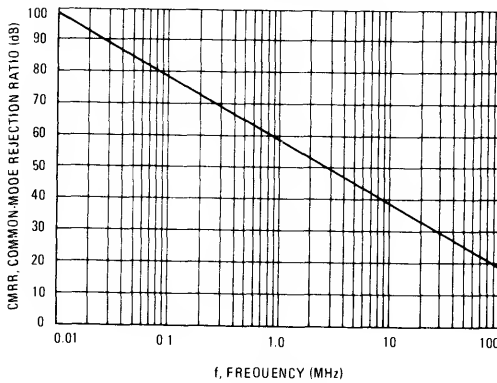


FIGURE 11 – CIRCUIT SCHEMATIC

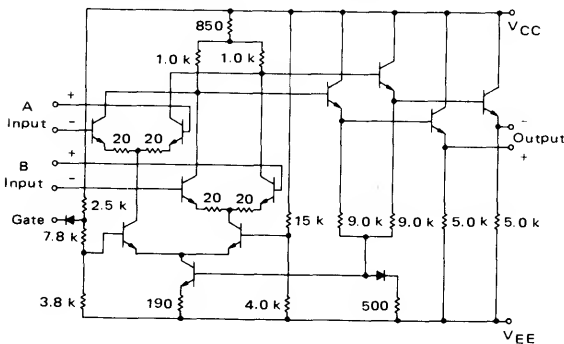


FIGURE 8 – GATE CHARACTERISTICS

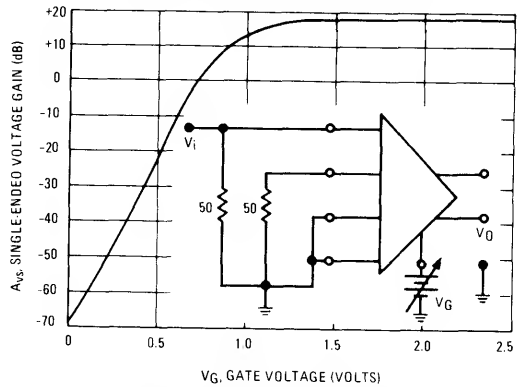


FIGURE 10 – INPUT WIDEBAND NOISE versus SOURCE RESISTANCE

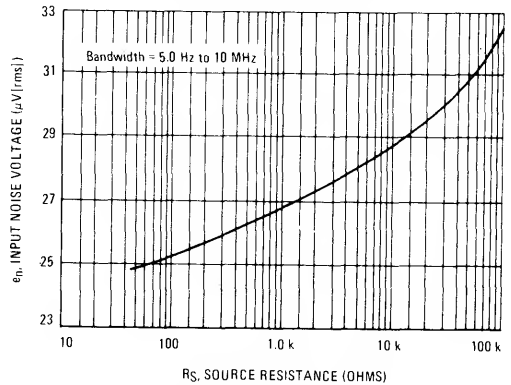
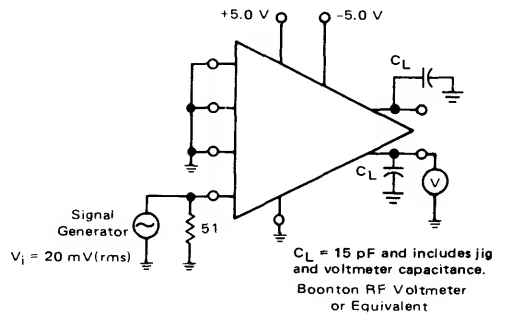


FIGURE 12 – SINGLE-ENDED VOLTAGE GAIN AND BANDWIDTH TEST CIRCUIT



MC1445, MC1545

2

FIGURE 13 – OUTPUT VOLTAGE SWING TEST CIRCUIT

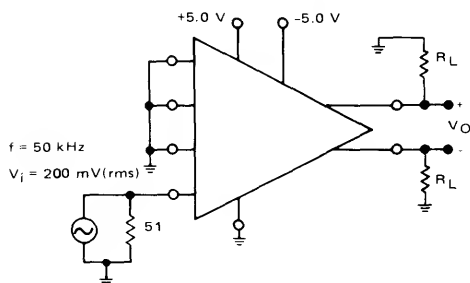


FIGURE 14 – INPUT IMPEDANCE TEST CIRCUIT

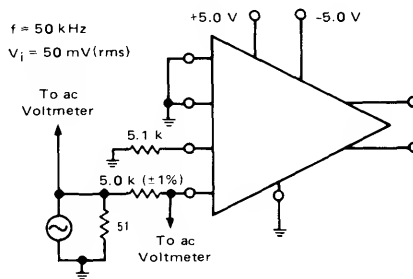


FIGURE 15 – OUTPUT IMPEDANCE TEST CIRCUIT

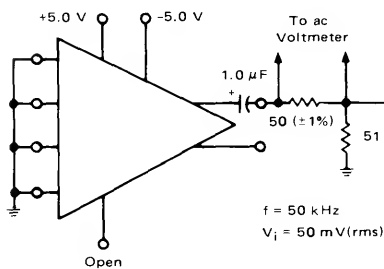


FIGURE 16 – INPUT BIAS CURRENT AND INPUT OFFSET CURRENT TEST CIRCUIT

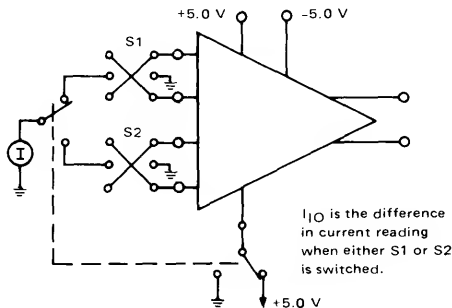


FIGURE 17 – INPUT OFFSET VOLTAGE AND QUIESCENT OUTPUT LEVEL TEST CIRCUIT

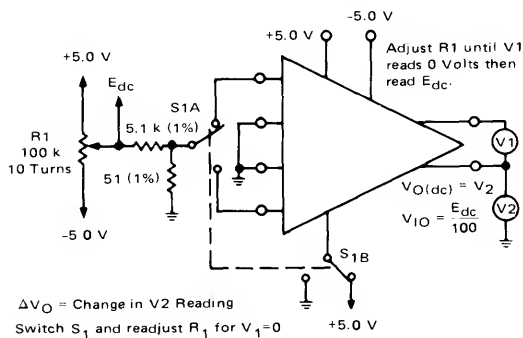


FIGURE 18 – GATE CURRENT (HIGH AND LOW), COMMON-MODE REJECTION AND COMMON-MODE INPUT RANGE TEST CIRCUIT

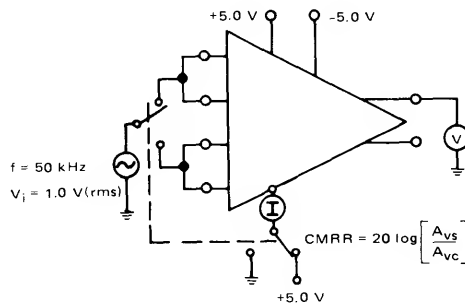
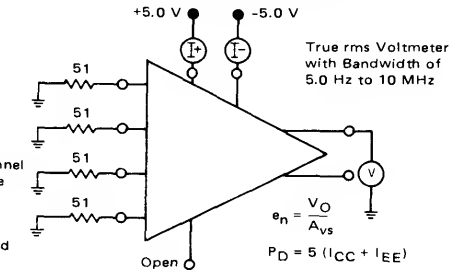


FIGURE 20 – POWER DISSIPATION AND WIDEBAND INPUT NOISE TEST CIRCUIT



MC1454G
MC1554G

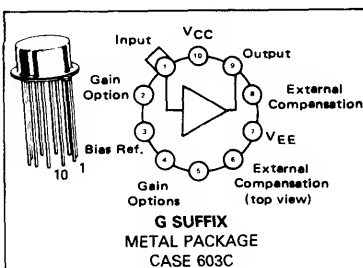
2

1-WATT POWER AMPLIFIERS

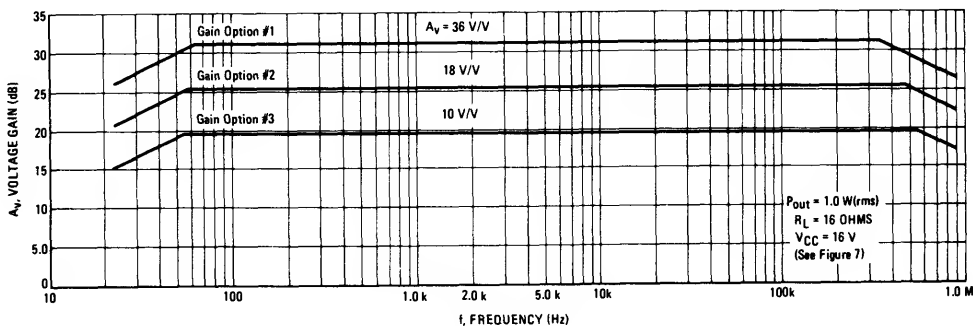
... designed to amplify signals to 300-kHz with 1-Watt delivered to a direct coupled or capacitively coupled load.

- Low Total Harmonic Distortion — 0.4% (Typ) @ 1 Watt
- Low Output Impedance — 0.2 Ohm
- Excellent Gain — Temperature Stability

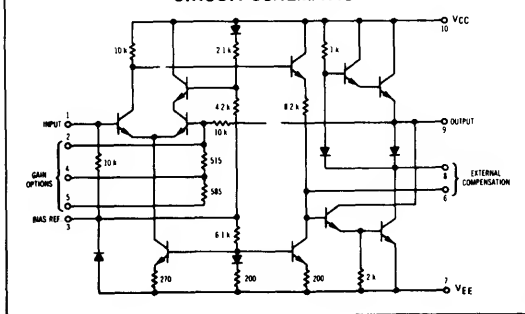
**1-WATT
POWER AMPLIFIER
INTEGRATED CIRCUIT
SILICON MONOLITHIC
EPITAXIAL PASSIVATED**



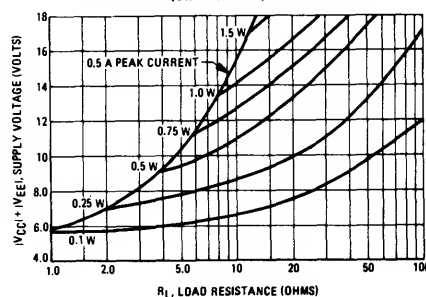
VOLTAGE GAIN versus FREQUENCY ($R_L = 16 \text{ OHMS}$)



CIRCUIT SCHEMATIC



**MAXIMUM AVAILABLE OUTPUT POWER
(SINE WAVE)**



MC1454G, MC1554G

ELECTRICAL CHARACTERISTICS ($T_C = +25^\circ\text{C}$ unless otherwise noted)
Frequency compensation shown in Figures 6 and 7.

Characteristic	Figure	R_L (Ohms)	Gain Option*	Symbol	MC1554 (-55 to +125°C)			MC1454 (0 to +70°C)			Unit
					Min	Typ	Max	Min	Typ	Max	
Output Power (for $e_{out} < 5.0\%$ THD)	1	16	—	P_{out}	1.0	1.1	—	—	1.0	—	Watt
Power Dissipation (@ $P_{out} = 1.0$ W)	1	16	—	P_D	—	0.9	1.2	—	0.9	—	Watt
Voltage Gain	1	16	10	A_v	8.0	10	12	—	10	—	V/V
		16	18		—	18	—	—	18	—	
		16	36		—	36	—	—	36	—	
Input Impedance	1	—	10	z_{in}	7.0	10	—	3.0	10	—	k Ω
Output Impedance	1	—	10	z_o	—	0.2	—	—	0.4	—	Ω
Power Bandwidth (for $e_{out} < 5.0\%$ THD)	2	16	10	BW	—	270	—	—	270	—	kHz
		16	18		—	250	—	—	250	—	
		16	36		—	210	—	—	210	—	
Total Harmonic Distortion (for $e_{in} < 0.05\%$ THD, $f = 20$ Hz to 20 kHz)	2	—	—	THD	—	—	—	—	—	—	%
		16	10		—	0.4	—	—	0.4	—	
		16	10		—	0.5	—	—	0.5	—	
$P_{out} = 1.0$ Watt (sinewave)											
$P_{out} = 0.1$ Watt (sinewave)											
Zero Signal Current Drain	3	∞	—	I_D	—	11	15	—	11	20	mAdc
Output Noise Voltage	3	16	10	V_n	—	0.3	—	—	0.3	—	mV(rms)
Output Quiescent Voltage (Split Supply Operation)	4	16	—	V_O (dc)	—	± 10	± 30	—	± 10	—	mVdc
Positive Supply Sensitivity (V_{EE} constant)	5	∞	—	S^+	—	-40	—	—	-40	—	mV/V
Negative Supply Sensitivity (V_{CC} constant)	5	∞	—	S^-	—	-40	—	—	-40	—	mV/V

*To obtain the voltage gain characteristic desired, use the following pin connections: Voltage Gain

Pin Connection

10 Pins 2 and 4 open, Pin 5 to ac ground
18 Pins 2 and 5 open, Pin 4 to ac ground
36 Pin 2 connected to Pin 5, Pin 4 to ac ground

Characteristic Definitions (Linear Operation)

FIGURE 1

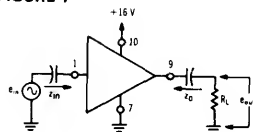


FIGURE 3

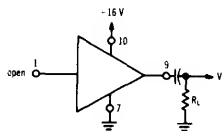


FIGURE 4

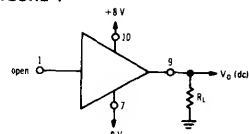


FIGURE 2

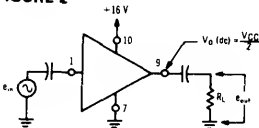
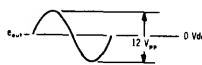
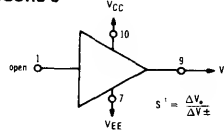


FIGURE 5



MC1454G, MC1554G

2

MAXIMUM RATINGS ($T_C = +25^{\circ}\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Total Power Supply Voltage	$ V_{CC} + V_{EE} $	18	Vdc
Peak Load Current	I_{out}	0.5	Ampere
Audio Output Power	P_{out}	1.8	Watts
Power Dissipation (package limitation) $T_A = +25^{\circ}C$ Derate above $25^{\circ}C$	P_D $1/\theta_{JA}$	600 4.8	mW mW/ $^{\circ}C$
$T_C = +25^{\circ}C$ Derate above $25^{\circ}C$	P_D $1/\theta_{JC}$	1.8 14.4	Watts mW/ $^{\circ}C$
Operating Temperature Range MC1454 MC1554	T_A	0 to $+70$ -55 to $+125$	$^{\circ}C$
Storage Temperature Range	T_{stg}	-55 to $+150$	$^{\circ}C$

TYPICAL CONNECTIONS

FIGURE 6 – SPLIT SUPPLY OPERATION VOLTAGE
GAIN (A_V) = 10, $f_{LOW} \approx 25$ Hz

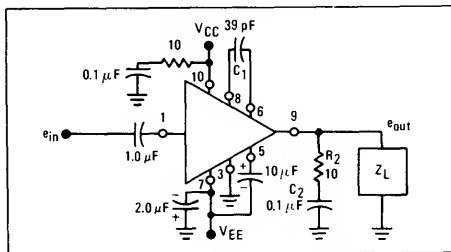
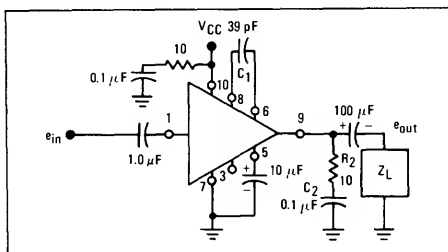


FIGURE 7 – SINGLE SUPPLY OPERATION VOLTAGE
GAIN (A_V) = 10, $f_{LOW} \approx 100$ Hz



RECOMMENDED OPERATING CONDITIONS

In order to avoid local VHF instability, the following set of rules must be adhered to:

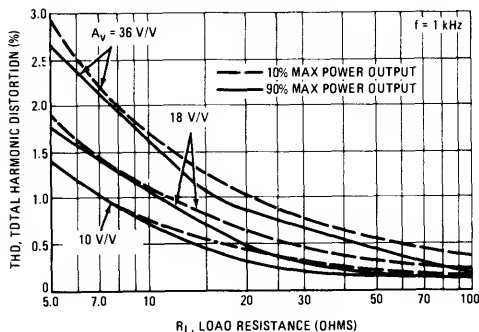
1. An R-C stabilizing network ($0.1 \mu\text{F}$ in series with 10 ohms) should be placed directly from pin 9 to ground, as shown in Figures 6 and 7, using short leads, to eliminate local VHF instability caused by lead inductance to the load.
2. Excessive lead inductance from the V_{CC} supply to pin 10 can cause high frequency instability. To prevent this, the V_{CC} -by-pass capacitor should be connected with short leads from the V_{CC} pin to ground. If this capacitor is remotely located a series R-C network ($0.1 \mu\text{F}$ and 10 ohms) should be used directly from pin 10 to ground as shown in Figures 6 and 7.

3. Lead lengths from the external components to pins 7, 9, and 10 of the package should be as short as possible to insure good VHF grounding for these points.

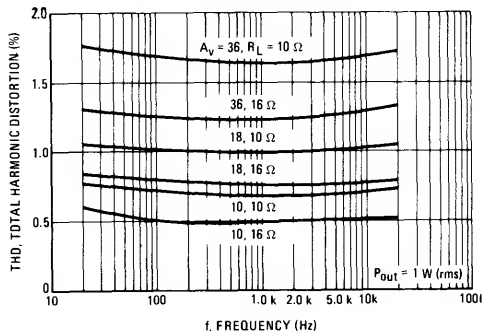
Due to the large bandwidth of the amplifier, coupling must be avoided between the output and input leads. This can be assured by either (a) use of short leads which are well isolated, (b) narrow-banding the overall amplifier by placing a capacitor from pin 1 to ground to form a low-pass filter in combination with the source impedance, or (c) use of a shielded input cable. In applications which require upper band-edge control the input low-pass filter is recommended.

TYPICAL CHARACTERISTICS

**FIGURE 8 – TOTAL HARMONIC DISTORTION
versus LOAD RESISTANCE**



**FIGURE 9 – TOTAL HARMONIC DISTORTION
versus FREQUENCY**



MC1454G, MC1554G

TYPICAL CHARACTERISTICS (continued)

FIGURE 10 – VOLTAGE GAIN versus TEMPERATURE

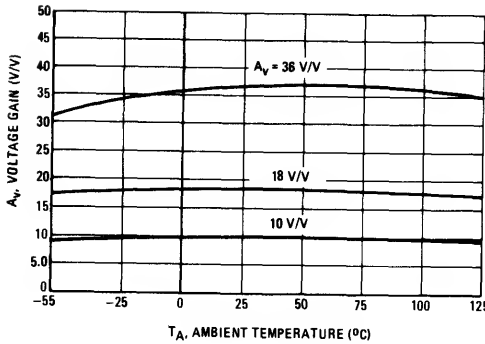


FIGURE 11 – OUTPUT VOLTAGE CHANGE

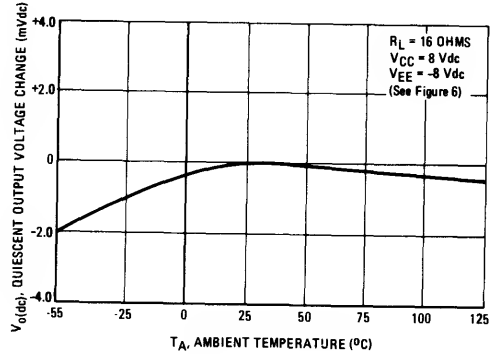


FIGURE 12 – VOLTAGE GAIN versus FREQUENCY ($R_L = \infty$)

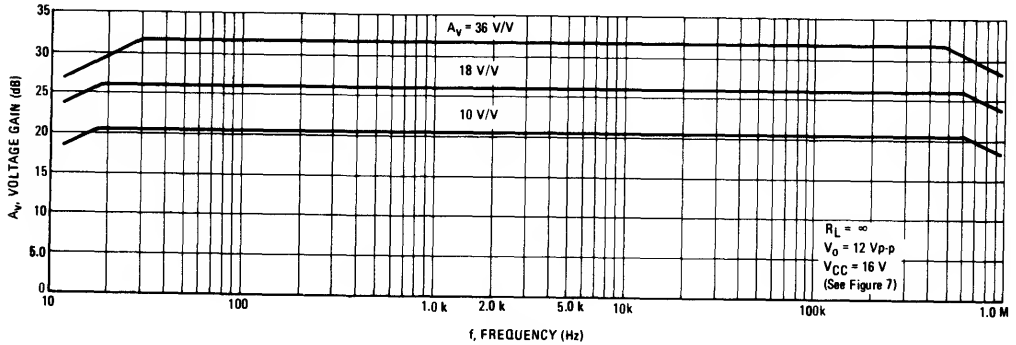
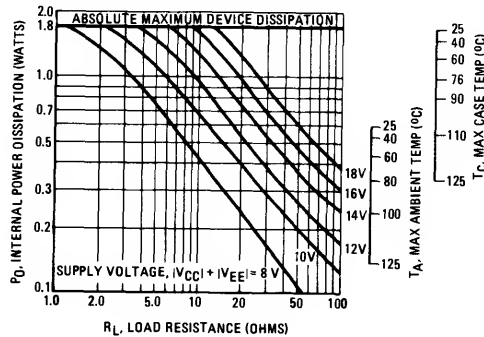


FIGURE 13 – MAXIMUM DEVICE DISSIPATION (SINE WAVE)

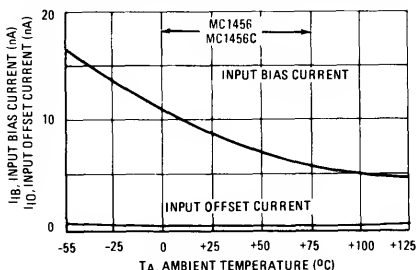


**INTERNALLY COMPENSATED, HIGH PERFORMANCE
 OPERATIONAL AMPLIFIER**

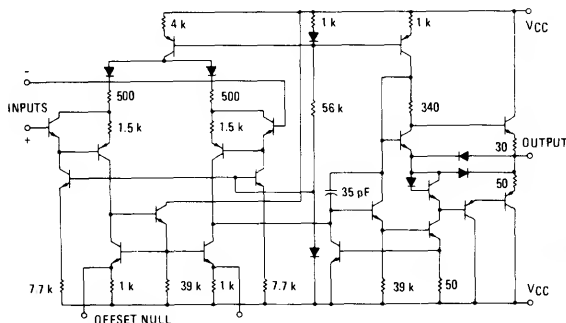
... designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- Low Input Bias Current — 15 nA max
- Low Input Offset Current — 2.0 nA max
- Low Input Offset Voltage — 4.0 mV max
- Fast Slew Rate — 2.5 V/ μ s typ
- Large Power Bandwidth — 40 kHz typ
- Low Power Consumption — 45 mW max
- Offset Voltage Null Capability
- Output Short-Circuit Protection
- Input Over-Voltage Protection

**TYPICAL INPUT BIAS CURRENT AND INPUT
 OFFSET CURRENT versus TEMPERATURE for MC1556**



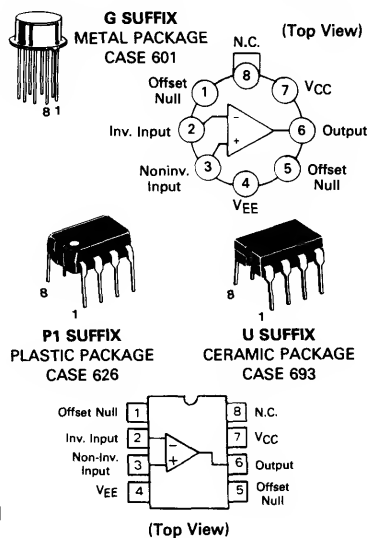
REPRESENTATIVE CIRCUIT SCHEMATIC



**MC1456
 MC1456C
 MC1556**

OPERATIONAL AMPLIFIER

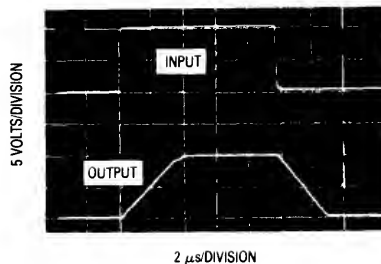
SILICON MONOLITHIC
 INTEGRATED CIRCUIT



ORDERING INFORMATION

Device	Temperature Range	Package
MC1456G,CG MC1456CP1,P1	0°C to +70°C	Metal Can Plastic DIP
MC1556G MC1556U	-55°C to +125°C	Metal Can Ceramic DIP

VOLTAGE-FOLLOWER PULSE RESPONSE



MC1456, MC1456C, MC1556

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	MC1556	MC1456 MC1456C	Unit
Power Supply Voltage	V_{CC} V_{EE}	+22 -22	+18 -18	Vdc
Differential Input Voltage Range	V_{IDR}	$\pm V_{CC}$		Volts
Common-Mode Voltage Range	V_{ICR}	$\pm V_{CC}$		Volts
Load Current	I_L	20		mA
Output Short Circuit Duration	t_S	Continuous		
Power Dissipation (Package Limitation) Derate above $T_A = +25^\circ\text{C}$	P_D	680 4.6		mW mW/ $^\circ\text{C}$
Operating Temperature Range	T_A	-55 to +125	0 to +70	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ Vdc}$, $V_{EE} = -15\text{ Vdc}$, $T_A = +25^\circ\text{C}$ unless otherwise noted).

Characteristic	Fig.	Symbol	MC1556			MC1456			MC1456C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Bias Current $T_A = +25^\circ\text{C}$ $T_A = T_{low}$ to T_{high} (See Note 1)		I_{IB}	—	8.0	15	—	15	30	—	15	90	nAdc
Input Offset Current $T_A = +25^\circ\text{C}$ $T_A = +25^\circ\text{C}$ to T_{high} $T_A = T_{low}$ to $+25^\circ\text{C}$		I_{IO}	—	1.0	2.0	—	5.0	10	—	5.0	30	nAdc
Input Offset Voltage $T_A = +25^\circ\text{C}$ $T_A = T_{low}$ to T_{high}		V_{IO}	—	2.0	4.0	—	5.0	10	—	5.0	12	mVdc
Differential Input Impedance (Open-Loop, $f = 20\text{ Hz}$)												
Parallel Input Resistance		r_p	—	5.0	—	—	3.0	—	—	3.0	—	Megohms
Parallel Input Capacitance		C_p	—	6.0	—	—	6.0	—	—	6.0	—	pF
Common-Mode Input Impedance ($f = 20\text{ Hz}$)		Z_i	—	250	—	—	250	—	—	250	—	Megohms
Common-Mode Input Voltage Range	1	V_{ICR}	± 12	± 13	—	$+11$	± 12	—	± 10.5	± 12	—	V _{pk}
Equivalent Input Noise Voltage ($A_V = 100$, $R_s = 10\text{ k ohms}$, $f = 1.0\text{ kHz}$, $BW = 1.0\text{ Hz}$)	2	e_n	—	45	—	—	45	—	—	45	—	nV/(Hz) ^{1/2}
Common-Mode Rejection Ratio ($f = 100\text{ Hz}$)	3	CMRR	80	110	—	70	110	—	—	110	—	dB
Open-Loop Voltage Gain, ($V_O = \pm 10\text{ V}$, $R_L = 2.0\text{ k ohms}$) $T_A = +25^\circ\text{C}$ $T_A = T_{low}$ to T_{high}	4,5,6	A_{VOL}	100,000 40,000	200,000 —	— 70,000 40,000	100,000 —	—	25,000 —	100,000 —	—	—	V/V
Power Bandwidth ($A_V = 1$, $R_L = 2.0\text{ k ohms}$, $\text{THD} \leq 5\%$, $V_O = 20\text{ Vpp}$)	9	BW _p	—	40	—	—	40	—	—	40	—	kHz
Unity Gain Crossover Frequency (open-loop)	5	BW	—	1.0	—	—	1.0	—	—	1.0	—	MHz
Phase Margin (open-loop, unity gain)	5,7		—	70	—	—	70	—	—	70	—	degrees
Gain Margin	5,7		—	18	—	—	18	—	—	18	—	dB
Slew Rate (Unity Gain)		SR	—	2.5	—	—	2.5	—	—	2.5	—	V/ μs
Output Impedance ($f = 20\text{ Hz}$)		z_o	—	1.0	2.0	—	1.0	2.5	—	1.0	—	kohms
Short-Circuit Output Current	8	I_{OS}	—	-17, +9.0	—	—	-17, +9.0	—	—	-17, +9.0	—	mA _{dc}
Output Voltage Swing ($R_L = 2.0\text{ k ohms}$)	10	V_{OR}	± 12	± 13	—	$+11$	± 12	—	± 10	± 12	—	V _{pk}
Power Supply Rejection Ratio $V_{CC} = \text{constant}$, $R_S \leq 10\text{ k ohms}$ $V_{EE} = \text{constant}$, $R_S \leq 10\text{ k ohms}$		PSRR+ PSRR-	—	50 50	100 100	—	75 75	200 200	—	75 75	—	$\mu\text{V/V}$
Power Supply Current		I_{CC} I_{EE}	—	1.0 1.0	1.5 1.5	—	1.3 1.3	3.0 3.0	—	1.3 1.3	4.0 4.0	mA _{dc}
DC Quiescent Power Dissipation ($V_O = 0$)	11	P_D	—	30	45	—	40	90	—	40	120	mW

Note 1: T_{low} : 0° for MC1456 and MC1456C
 -55°C for MC1556
 T_{high} : $+70^\circ\text{C}$ for MC1456 and MC1456C
 $+125^\circ\text{C}$ for MC1556

MC1456, MC1456C, MC1556

TYPICAL CHARACTERISTICS

($V_{CC} = +15$ Vdc, $V_{EE} = -15$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted).

FIGURE 1 — INPUT COMMON-MODE SWING versus POWER SUPPLY VOLTAGE

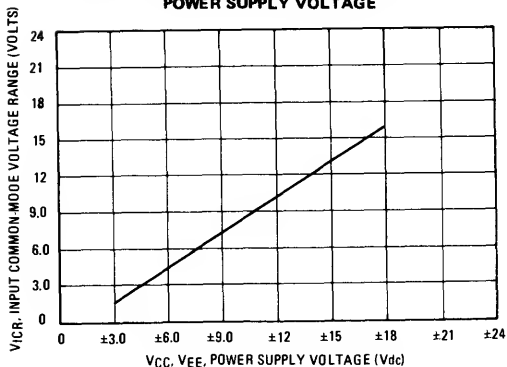


FIGURE 2 — SPECTRAL NOISE DENSITY

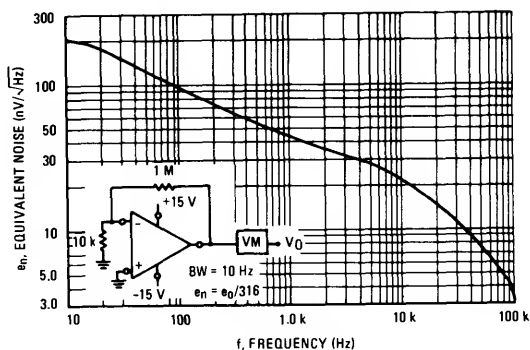


FIGURE 3 — COMMON-MODE REJECTION RATIO versus FREQUENCY

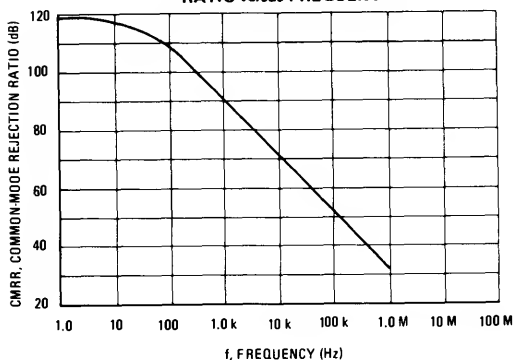


FIGURE 4 — OPEN-LOOP VOLTAGE GAIN versus TEMPERATURE

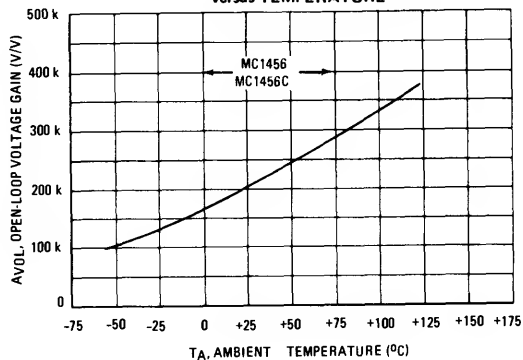


FIGURE 5 — OPEN-LOOP FREQUENCY RESPONSE

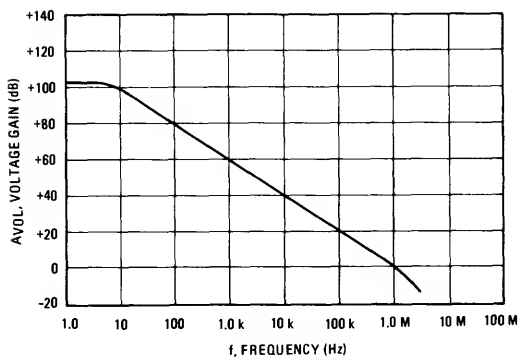
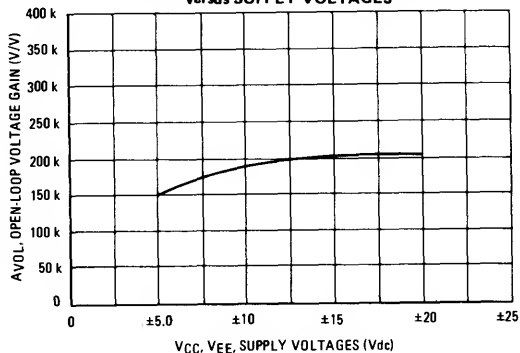


FIGURE 6 — OPEN-LOOP VOLTAGE GAIN versus SUPPLY VOLTAGES



MC1456, MC1456C, MC1556

TYPICAL CHARACTERISTICS (continued)

FIGURE 7 – OPEN-LOOP PHASE SHIFT

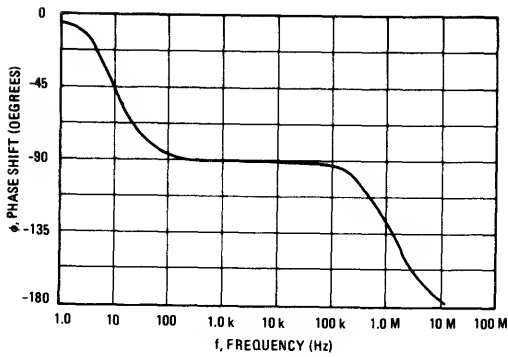


FIGURE 8 – OUTPUT SHORT-CIRCUIT CURRENT
versus TEMPERATURE

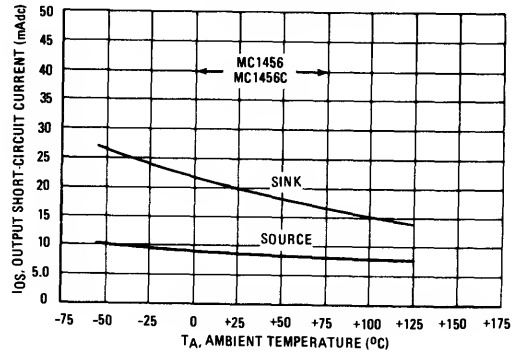


FIGURE 9 – POWER BANDWIDTH

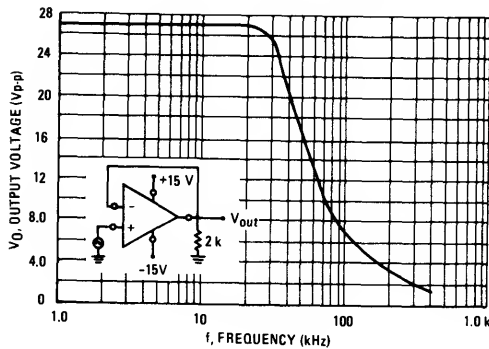


FIGURE 10 – OUTPUT VOLTAGE SWING versus
LOAD RESISTANCE

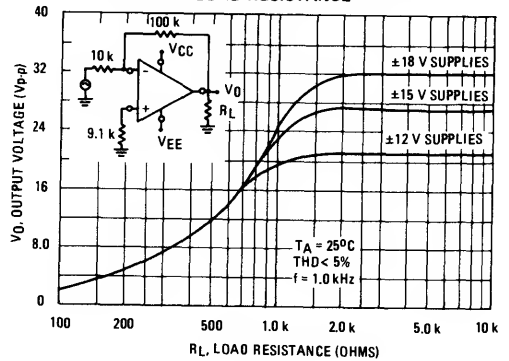
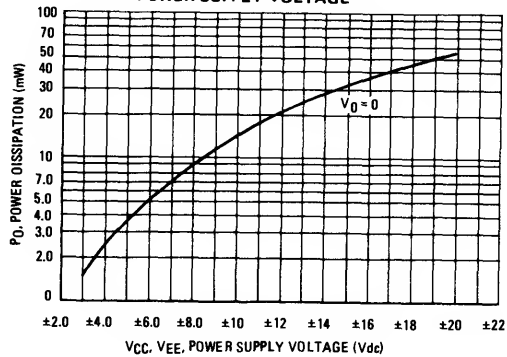


FIGURE 11 – POWER DISSIPATION versus
POWER SUPPLY VOLTAGE



MC1456, MC1456C, MC1556

TYPICAL APPLICATIONS

Where values are not given for external components they must be selected by the designer to fit the requirements of the system.

FIGURE 12 — INVERTING FEEDBACK MODEL

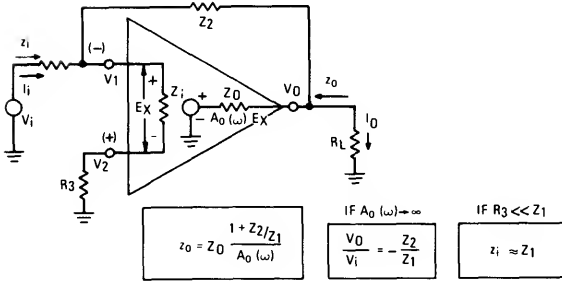


FIGURE 13 — NONINVERTING FEEDBACK MODEL

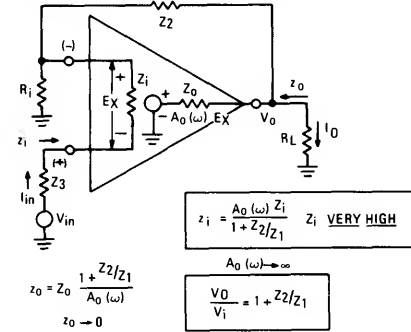


FIGURE 14 — LOW-DRIFT SAMPLE AND HOLD

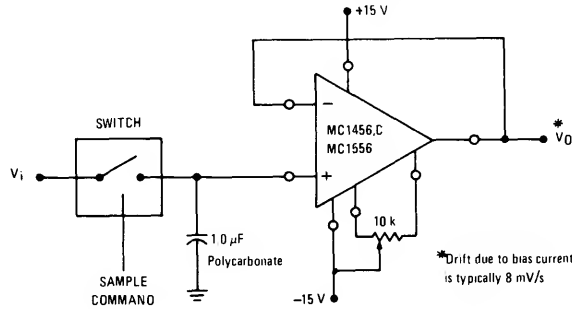
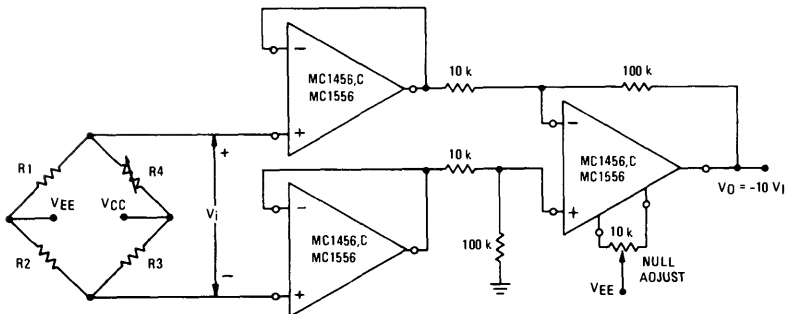


FIGURE 15 — HIGH IMPEDANCE BRIDGE AMPLIFIER



TYPICAL APPLICATIONS (continued)

FIGURE 16 – LOGARITHMIC AMPLIFIER

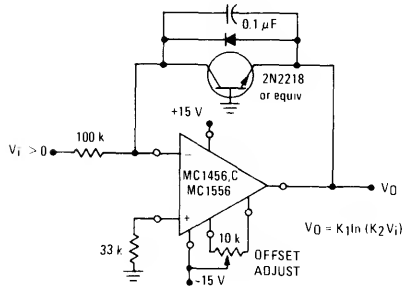
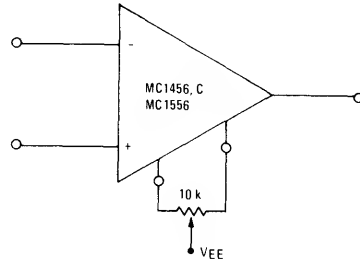


FIGURE 17 – VOLTAGE OFFSET NULL CIRCUIT



(DUAL MC1741)

**INTERNALLY COMPENSATED,
HIGH PERFORMANCE
DUAL OPERATIONAL AMPLIFIERS**

... designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- No Frequency Compensation Required
- Short Circuit Protection
- Wide Common Mode and Differential Voltage Ranges
- Low Power Consumption
- No Latch Up

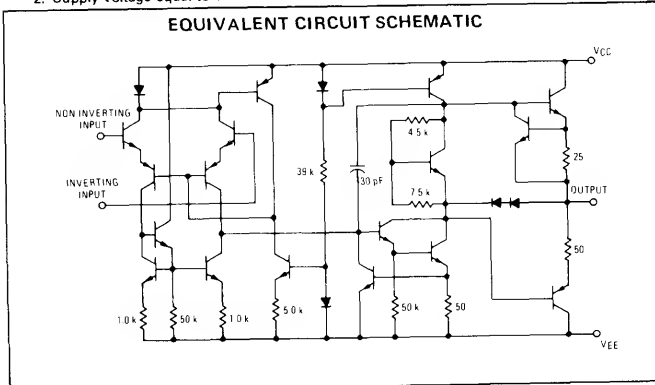
MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	MC1458	MC1558	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 -18	+22 -22	Vdc Vdc
Input Differential Voltage	V_{ID}	± 30		Volts
Input Common Mode Voltage(1)	V_{ICM}	+15		Volts
Output Short Circuit Duration(2)	t_S	Continuous		
Operating Ambient Temperature Range	T_A	0 to +70	-55 to +125	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150		$^\circ\text{C}$
Metal and Ceramic Packages		-55 to +125		
Plastic Package				
Junction Temperature	T_J	175		$^\circ\text{C}$
Metal and Ceramic Packages		150		
Plastic Package				

NOTES:

1. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.
2. Supply voltage equal to or less than 15 V.

EQUIVALENT CIRCUIT SCHEMATIC



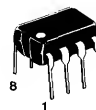
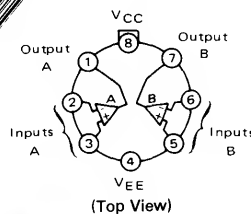
**MC1458
MC1458C
MC1558**

**(DUAL MC1741)
DUAL
OPERATIONAL AMPLIFIERS**

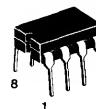
**SILICON MONOLITHIC
INTEGRATED CIRCUIT**



**G SUFFIX
METAL PACKAGE
CASE 601**



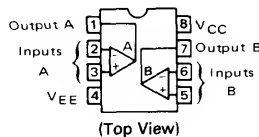
**P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MC1458, MC1458C)**



**U SUFFIX
CERAMIC PACKAGE
CASE 693**



**D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)**



ORDERING INFORMATION

Device	Temperature Range	Package
MC1458CD,D MC1458CG,G MC1458CP1,P1 MC1458CU,U	0° to $+70^\circ\text{C}$	SO-8 Metal Can Plastic DIP Ceramic DIP
MC1558G MC1558U	-55°C to $+125^\circ\text{C}$	Metal Can Ceramic DIP

MC1458, MC1458C, MC1558

ELECTRICAL CHARACTERISTICS — Note 1. ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = 25^\circ\text{C}$ unless otherwise noted).

Characteristic	Symbol	MC1558			MC1458			MC1458C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10\text{ k}$)	V_{IO}	—	1.0	5.0	—	2.0	6.0	—	2.0	10	mV
Input Offset Current	I_{IO}	—	20	200	—	20	200	—	20	300	nA
Input Bias Current	I_{IB}	—	80	500	—	80	500	—	80	700	nA
Input Resistance	r_i	0.3	2.0	—	0.3	2.0	—	—	2.0	—	M Ω
Input Capacitance	C_i	—	1.4	—	—	1.4	—	—	1.4	—	pF
Offset Voltage Adjustment Range	V_{IOR}	—	± 15	—	—	± 15	—	—	± 15	—	mV
Common Mode Input Voltage Range	V_{ICR}	± 12	± 13	—	± 12	± 13	—	± 11	± 13	—	V
Large Signal Voltage Gain ($V_O = \pm 10\text{ V}$, $R_L = 2.0\text{ k}$) ($V_O = \pm 10\text{ V}$, $R_L = 10\text{ k}$)	A_v	50 —	200 —	— —	20 —	200 —	— —	— 20	— 200	— —	V/mV
Output Resistance	r_o	—	75	—	—	75	—	—	75	—	Ω
Common Mode Rejection Ratio ($R_S \leq 10\text{ k}$)	CMRR	70	90	—	70	90	—	60	90	—	dB
Supply Voltage Rejection Ratio ($R_S \leq 10\text{ k}$)	PSRR	—	30	150	—	30	150	—	30	—	$\mu\text{V/V}$
Output Voltage Swing ($R_L \geq 10\text{ k}$) ($R_L \geq 2\text{ k}$)	V_O	± 12 ± 10	± 14 ± 13	— —	± 12 ± 10	± 14 ± 13	— —	± 11 ± 9.0	± 14 ± 13	— —	V
Output Short-Circuit Current	I_{os}	—	20	—	—	20	—	—	20	—	mA
Supply Currents (Both Amplifiers)	I_D	—	2.3	5.0	—	2.3	5.6	—	2.3	8.0	mA
Power Consumption	P_C	—	70	150	—	70	170	—	70	240	mW
Transient Response (Unity Gain) ($V_i = 20\text{ mV}$, $R_L \geq 2\text{ k}\Omega$, $C_L \leq 100\text{ pF}$) Rise Time ($V_i = 20\text{ mV}$, $R_L \geq 2\text{ k}\Omega$, $C_L \leq 100\text{ pF}$) Overshoot ($V_i = 10\text{ V}$, $R_L \geq 2\text{ k}\Omega$, $C_L \leq 100\text{ pF}$) Slew Rate	t_{RLH} os SR	— — —	0.3 15 0.5	— — —	— — —	0.3 15 0.5	— — —	— — —	0.3 15 0.5	— — —	μs % V/ μs

ELECTRICAL CHARACTERISTICS Note 1 ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = *T_{\text{high}}$ to T_{low} unless otherwise noted).

Characteristic	Symbol	MC1558			MC1458			MC1458C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10\text{ k}\Omega$)	V_{IO}	—	1.0	6.0	—	—	7.5	—	—	12	mV
Input Offset Current ($T_A = 125^\circ\text{C}$) ($T_A = -55^\circ\text{C}$) ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$)	I_{IO}	— — —	7.0 85 —	200 500 —	— — —	— — —	— — 300	— — —	— — —	400	nA
Input Bias Current ($T_A = 125^\circ\text{C}$) ($T_A = -55^\circ\text{C}$) ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$)	I_{IB}	— — —	30 300 —	500 1500 —	— — —	— — —	— — 800	— — —	— — 1000	—	nA
Common Mode Input Voltage Range	V_{ICR}	± 12	± 13	—	—	—	—	—	—	—	V
Common Mode Rejection Ratio ($R_S \leq 10\text{ k}$)	CMRR	70	90	—	—	—	—	—	—	—	dB
Supply Voltage Rejection Ratio ($R_S \leq 10\text{ k}$)	PSRR	—	30	150	—	—	—	—	—	—	$\mu\text{V/V}$
Output Voltage Swing ($R_L \geq 10\text{ k}$) ($R_L \geq 2\text{ k}$)	V_O	± 12 ± 10	± 14 ± 13	— —	± 12 ± 10	± 14 ± 13	— —	± 9.0 ± 13	— —	— —	V
Large Signal Voltage Gain ($V_O = \pm 10\text{ V}$, $R_L = 2\text{ k}$) ($V_O = \pm 10\text{ V}$, $R_L = 10\text{ k}$)	A_v	25 —	— —	— —	15 —	— —	— —	— 15	— —	— —	V/mV
Supply Currents (Both Amplifiers) ($T_A = 125^\circ\text{C}$) ($T_A = -55^\circ\text{C}$)	I_D	— —	— —	4.5 6.0	— —	— —	— —	— —	— —	— —	mA
Power Consumption ($T_A = 125^\circ\text{C}$) ($T_A = -55^\circ\text{C}$)	P_C	— —	— —	135 180	— —	— —	— —	— —	— —	— —	mW

* $T_{\text{high}} = 125^\circ\text{C}$ for MC1558 and 70°C for MC1458, MC1458C
 $T_{\text{low}} = -55^\circ\text{C}$ for MC1558 and 0°C for MC1458, MC1458C

Note 1. Input pins of an unused amplifier must be grounded for split supply operation or biased at least 3.0 V above V_{EE} for single supply operation.

MC1458, MC1458C, MC1558

FIGURE 1 – BURST NOISE versus SOURCE RESISTANCE

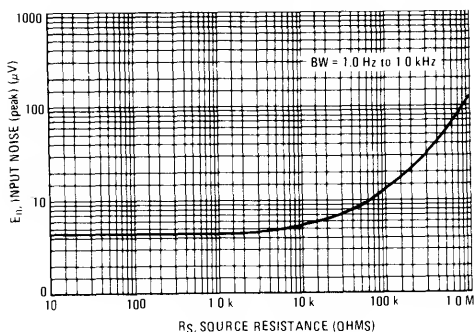
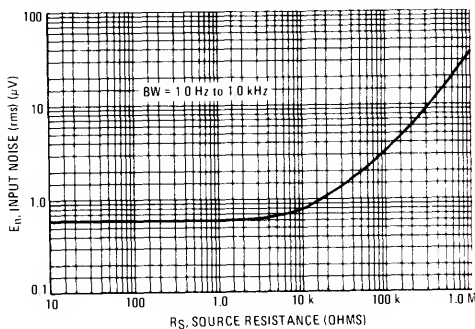


FIGURE 2 – RMS NOISE versus SOURCE RESISTANCE



2

FIGURE 3 – OUTPUT NOISE versus SOURCE RESISTANCE

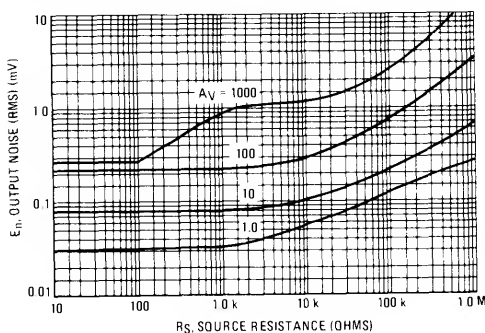


FIGURE 4 – SPECTRAL NOISE DENSITY

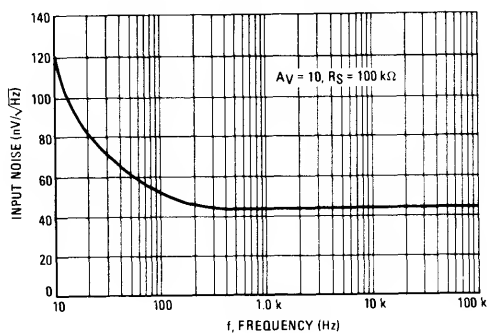
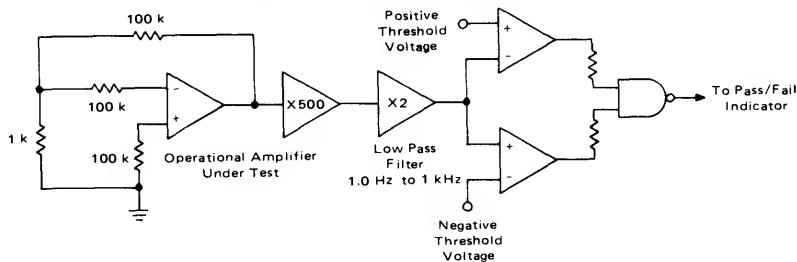


FIGURE 5 – BURST NOISE TEST CIRCUIT



Unlike conventional peak reading or RMS meters, this system was especially designed to provide the quick response time essential to burst (popcorn) noise testing.

The test time employed is 10 seconds and the 20 μ V peak limit refers to the operational amplifier input thus eliminating errors in the closed-loop gain factor of the operational amplifier under test.

MC1458, MC1458C, MC1558

TYPICAL CHARACTERISTICS

($V_{CC} = +15$ Vdc, $V_{EE} = -15$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted).

**FIGURE 6 – POWER BANDWIDTH
(LARGE SIGNAL SWING versus FREQUENCY)**

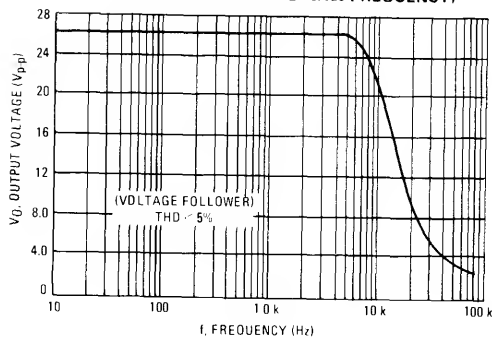
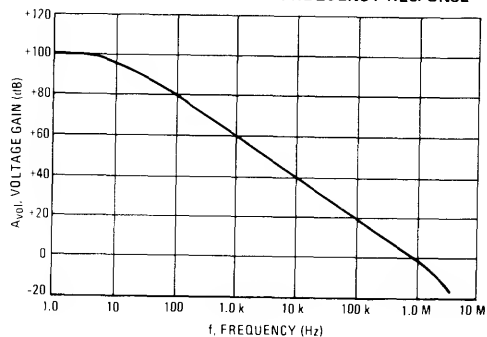
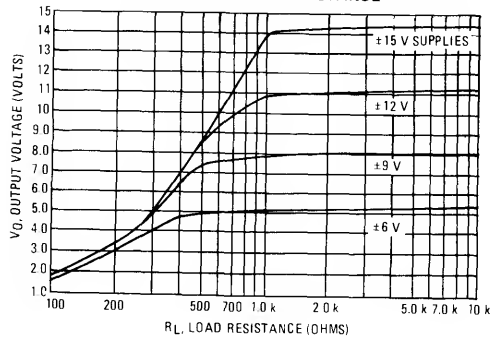


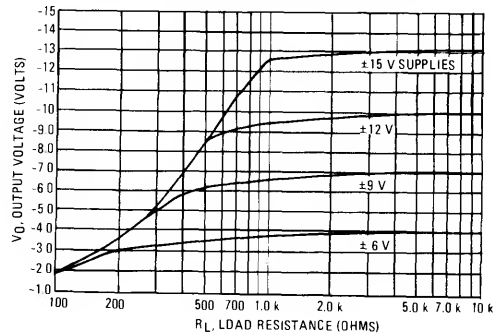
FIGURE 7 – OPEN LOOP FREQUENCY RESPONSE



**FIGURE 8 – POSITIVE OUTPUT VOLTAGE SWING
versus LOAD RESISTANCE**



**FIGURE 9 – NEGATIVE OUTPUT VOLTAGE SWING
versus LOAD RESISTANCE**



**FIGURE 10 – OUTPUT VOLTAGE SWING versus
LOAD RESISTANCE (Single Supply Operation)**

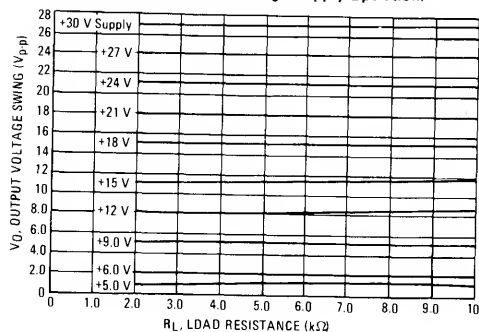


FIGURE 11 – SINGLE SUPPLY INVERTING AMPLIFIER

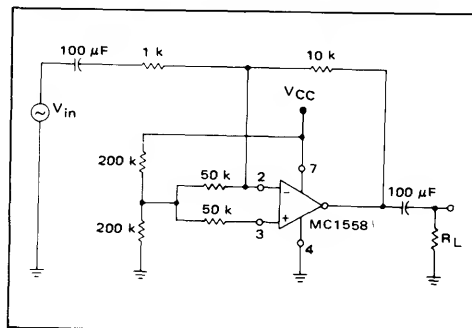


FIGURE 12 — NONINVERTING PULSE RESPONSE

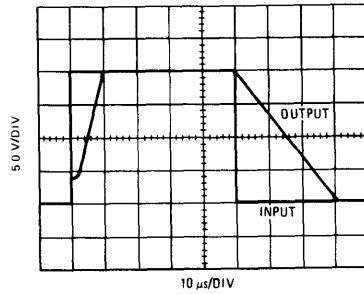


FIGURE 13 — TRANSIENT RESPONSE TEST CIRCUIT

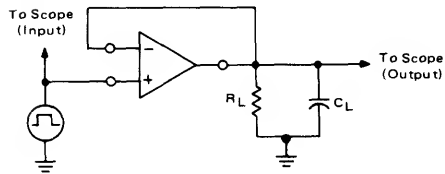
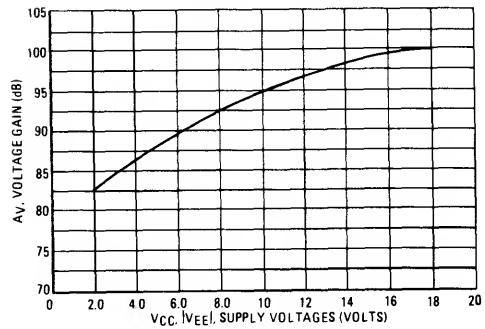


FIGURE 14 — OPEN LOOP VOLTAGE GAIN
versus SUPPLY VOLTAGE

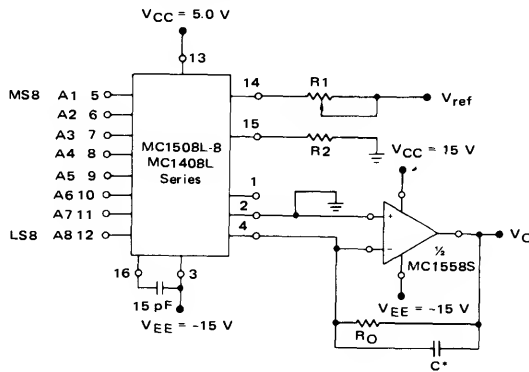


**DUAL HIGH SLEW RATE, INTERNALLY
COMPENSATED OPERATIONAL AMPLIFIERS**

The MC1558S is functionally equivalent, pin compatible, and possesses the same ease of use as the popular MC1558 circuit, yet offers 20 times higher slew rate and power bandwidth. This device is ideally suited for D/A converters due to its fast settling time and high slew rate.

- High Slew Rate — 10 V/μs Guaranteed Minimum (for inverting unity gain only)
- No Frequency Compensation Required
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low Power Consumption
- No Latch-Up

**TYPICAL APPLICATION OUTPUT CURRENT TO
VOLTAGE TRANSFORMATION FOR A D-TO-A CONVERTER**



Settling time to within 1/2 LS8 (±19.5 mV) is approximately 4.0 μs from the time that all bits are switched.

*The value of C may be selected to minimize overshoot and ringing (C ≈ 68 pF).

Theoretical V_O

$$V_O = \frac{V_{ref}}{R_1} (R_O) \left[\frac{A_1}{2} + \frac{A_2}{4} + \frac{A_3}{8} + \frac{A_4}{16} + \frac{A_5}{32} + \frac{A_6}{64} + \frac{A_7}{128} + \frac{A_8}{256} \right]$$

Adjust V_{ref} , R_1 or R_O so that V_O with all digital inputs at high level is equal to 9.961 volts.

$$\begin{aligned} V_{ref} &= 2.0 \text{ Vdc} \\ R_1 &= R_2 \approx 1.0 \text{ k}\Omega \\ R_O &= 5.0 \text{ k}\Omega \end{aligned}$$

$$V_O = \frac{2 \text{ V}}{1 \text{ k}} (5 \text{ k}) \left[\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256} \right] = 10 \text{ V} \left[\frac{255}{256} \right] = 9.961 \text{ V}$$

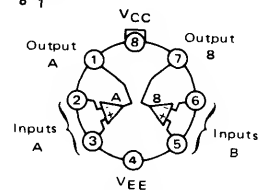
MC1458S
MC1558S

**DUAL
OPERATIONAL AMPLIFIERS**

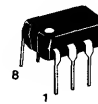
**SILICON MONOLITHIC
INTEGRATED CIRCUIT**



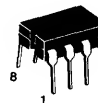
G SUFFIX
METAL PACKAGE
CASE 601



(Top View)



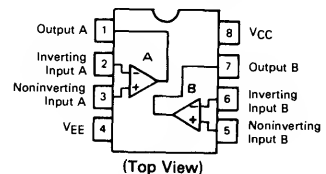
P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MC1458S Only)



U SUFFIX
CERAMIC PACKAGE
CASE 693



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)
(MC1458S Only)



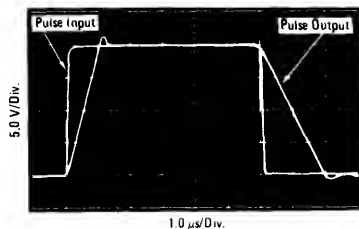
(Top View)

ORDERING INFORMATION

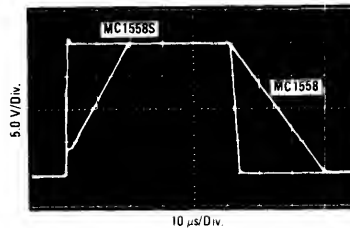
Device	Temperature Range	Package
MC1458SD	0°C to +70°C	SO-8
MC1458SG		Metal Can
MC1458SP1		Plastic DIP
MC1458SU		Ceramic DIP
MC1558SG	-55°C to +125°C	Metal Can
MC1558SU		

MC1458S, MC1558S

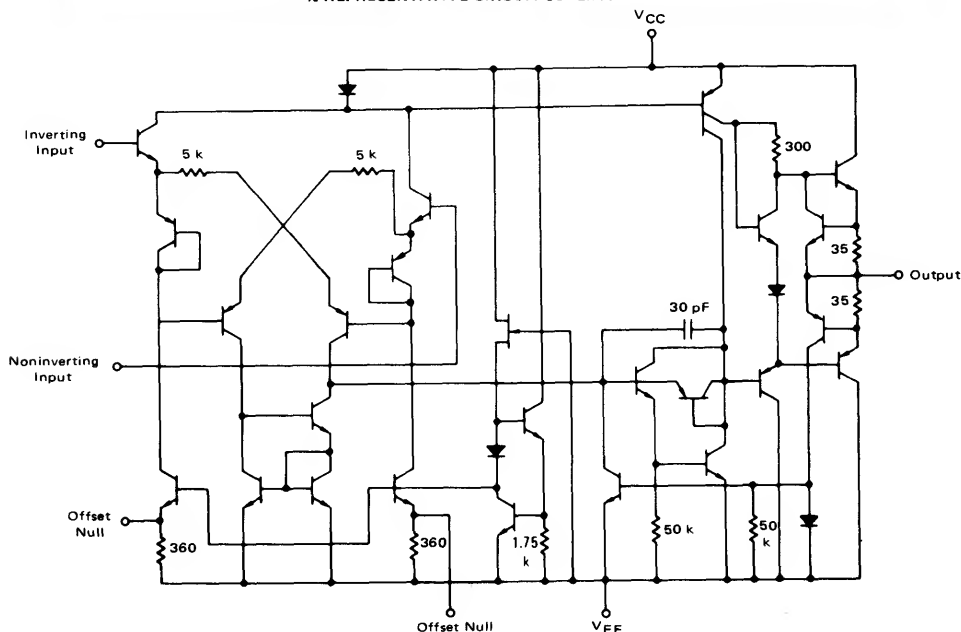
**MC1558S LARGE-SIGNAL TRANSIENT RESPONSE
(Inverting Mode)**



**STANDARD MC1558 versus MC1558S RESPONSE COMPARISON
(Inverting Mode)**



¼ REPRESENTATIVE CIRCUIT SCHEMATIC



MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted.)

Rating	Symbol	MC1558S	MC1458S	Unit
Power Supply Voltage	V_{CC} V_{EE}	+22 -22	+18 -18	Vdc
Input Differential Voltage Range ①	V_{IDR}	± 30		Volts
Input Common-Mode Voltage Range ②	V_{ICR}	± 15		Volts
Output Short Circuit Duration	t_S	Continuous		
Operating Ambient Temperature Range	T_A	-55 to +125	0 to +70	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	$^\circ\text{C}$
Junction Temperature	T_J	175	175	$^\circ\text{C}$
		150	150	$^\circ\text{C}$

Note 1. For supply voltages less than ± 15 Vdc, the absolute maximum input voltage is equal to the supply voltage.

Note 2. Supply voltage equal to or less than 15 Vdc.

MC1458S, MC1558S

ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ Vdc}$, $V_{EE} = -15\text{ Vdc}$, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	MC1558S			MC1458S			Unit
		Min	Typ	Max	Min	Typ	Max	
Power Bandwidth (See Figure 3) $A_v = 1$, $R_L = 2.0\text{ k}\Omega$, $\text{THD} = 5\%$, $V_O = 20\text{ V(p-p)}$	BW_p	150	200	—	150	200	—	kHz
Large-Signal Transient Response								
Slew Rate (Figures 10 and 11) $V(-)$ to $V(+)$ $V(+)$ to $V(-)$	SR	10 10	20 12	— —	10 10	20 12	— —	V/ μs
Settling Time (Figures 10 and 11) (to within 0.1%)	t_{settlg}	—	3.0	—	—	3.0	—	μs
Small-Signal Transient Response (Gain = 1, $E_{in} = 20\text{ mV}$, see Figures 7 and 8)								
Rise Time	t_{TLH}	—	0.25	—	—	0.25	—	μs
Fall Time	t_{THL}	—	0.25	—	—	0.25	—	μs
Propagation Delay Time	$t_{\text{PLH}}, t_{\text{PHL}}$	—	0.25	—	—	0.25	—	μs
Overshoot	OS	—	20	—	—	20	—	%
Short-Circuit Output Currents	I_{OS}	± 10	—	± 45	± 10	—	± 45	mA
Open-Loop Voltage Gain ($R_L = 2.0\text{ k}\Omega$) (See Figure 4) $V_O = \pm 10\text{ V}$	A_{VOL}	50,000	200,000	—	20,000	100,000	—	—
Output Impedance ($f = 20\text{ Hz}$)	z_o	—	75	—	—	75	—	Ω
Input Impedance ($f = 20\text{ Hz}$)	z_i	0.3	1.0	—	0.3	1.0	—	M Ω
Output Voltage Swing $R_L = 10\text{ k}\Omega$ $R_L = 2.0\text{ k}\Omega$	V_O	± 12 ± 10	± 14 ± 13	— —	± 12 ± 10	± 14 ± 13	— —	V _{pk}
Input Common-Mode Voltage Swing	V_{ICR}	± 12	± 13	—	± 12	± 13	—	V _{pk}
Common-Mode Rejection Ratio ($f = 20\text{ Hz}$)	CMRR	70	90	—	70	90	—	dB
Input Bias Current (See Figure 2)	I_{IB}	—	200	500	—	200	500	nA
Input Offset Current	$ I_{IO} $	—	30	200	—	30	200	nA
Input Offset Voltage ($R_S = \leq 10\text{ k}\Omega$)	$ V_{IO} $	—	1.0	5.0	—	2.0	6.0	mV
DC Power Consumption (See Figure 9) (Power Supply = $\pm 15\text{ V}$, $V_O = 0$)	P_C	—	70	150	—	70	170	mW
Positive Voltage Supply Sensitivity (V_{EE} constant)	PSS+	—	2.0	150	—	2.0	150	$\mu\text{V/V}$
Negative Voltage Supply Sensitivity (V_{CC} constant)	PSS-	—	10	150	—	10	150	$\mu\text{V/V}$

** Plastic package offered in limited temperature range device only.

ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ Vdc}$, $V_{EE} = -15\text{ Vdc}$, $T_A = -55$ to $+125^\circ\text{C}$ for MC1558S and $T_A = 0$ to 70°C for MC1458S, unless otherwise noted.)

Characteristic	Symbol	MC1558S			MC1458S			Unit
		Min	Typ	Max	Min	Typ	Max	
Open Loop Voltage Gain $V_O = \pm 10\text{ V}$	A_{VOL}	25,000	—	—	15,000	—	—	V/V
Output Voltage Swing $R_L = 10\text{ k}\Omega$ $R_L = 2\text{ k}\Omega$	V_O	± 12 ± 10	— —	— —	± 12 ± 10	— —	— —	V _{pk}
Input Common-Mode Voltage Range	V_{ICR}	± 12	—	—	—	—	—	V _{pk}
Common-Mode Rejection Ratio ($f = 20\text{ Hz}$)	CMRR	70	—	—	—	—	—	dB
Input Bias Current $T_A = 125^\circ\text{C}$ $T_A = -55^\circ\text{C}$ $T_A = 0$ to 70°C	I_{IB}	— — —	200 500 —	500 1500 —	— — —	— — —	— — 800	nA
Input Offset Current $T_A = 125^\circ\text{C}$ $T_A = -55^\circ\text{C}$ $T_A = 0$ to 70°C	I_{IO}	— — —	30 — —	200 500 —	— — —	— — —	— — 300	nA
Input Offset Voltage $R_S \leq 10\text{ k}\Omega$	V_{IO}	—	—	6.0	—	—	7.5	mV
DC Power Consumption $V_O = 0\text{ V}$	P_C	—	—	200	—	—	—	mW
Positive Power Supply Sensitivity $V_{EE} = -15\text{ V}$	PSS+	—	—	150	—	—	—	$\mu\text{V/V}$
Negative Power Supply Sensitivity $V_{CC} = 15\text{ V}$	PSS-	—	—	150	—	—	—	$\mu\text{V/V}$

MC1458S, MC1558S

TYPICAL CHARACTERISTICS

($V_{CC} = +15$ Vdc, $V_{EE} = -15$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 1 – OFFSET ADJUST CIRCUIT

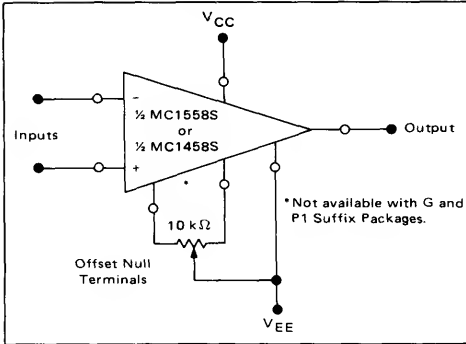


FIGURE 2 – INPUT BIAS CURRENT versus TEMPERATURE

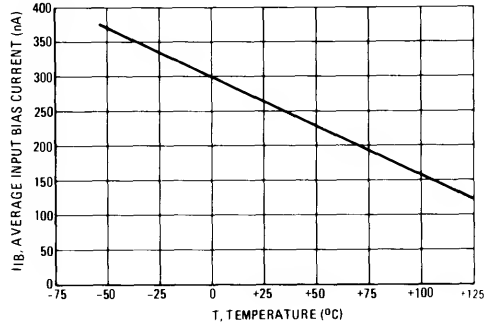


FIGURE 3 – POWER BANDWIDTH – NONDISTORTED OUTPUT VOLTAGE versus FREQUENCY

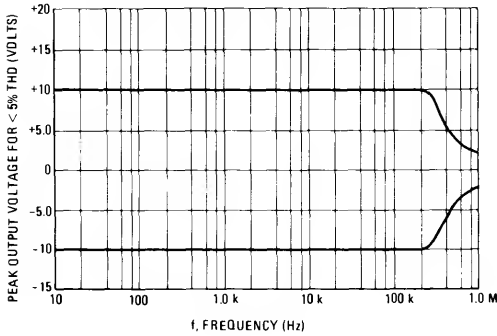


FIGURE 4 – OPEN-LOOP FREQUENCY RESPONSE

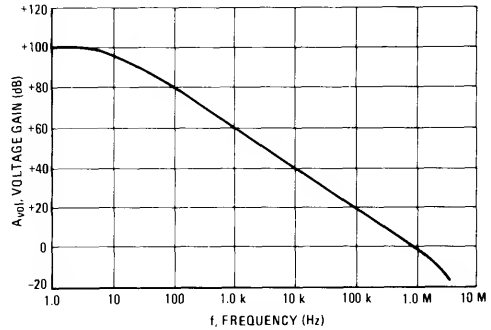
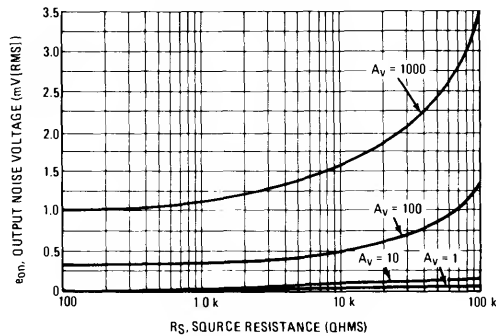


FIGURE 5 – OUTPUT NOISE versus SOURCE RESISTANCE



SETTLING TIME

In order to properly utilize the high slew rate and fast settling time of an operational amplifier, a number of system considerations must be observed. Capacitance at the summing node and at the amplifier output must be minimal and circuit board layout should be consistent with common high-frequency considerations. Both power supply connections should be adequately bypassed as close as possible to the device pins. In bypassing, both low and high-frequency components should be considered to avoid the possibility of excessive ringing. In order to achieve optimum damping, the selection of a capacitor in parallel with the feedback resistor may be necessary. A value too small could result in excessive ringing while a value too large will degrade slew rate and settling time.

SETTLING TIME MEASUREMENT

In order to accurately measure the settling time of an operational amplifier, it is suggested that the "false" summing junction approach be taken as shown in Figure 11. This is necessary since it is difficult to determine when the waveform at the output of the operational amplifier settles to within 0.1% of its final value. Because the output and input voltages are effectively subtracted from each other at the amplifier inverting input, this seems like an ideal node for the measurement. However, the probe capacitance at this critical node can greatly affect the accuracy of the actual measurement.

FIGURE 11 — WAVEFORM AT FALSE SUMMING NODE
(Inverting Mode)

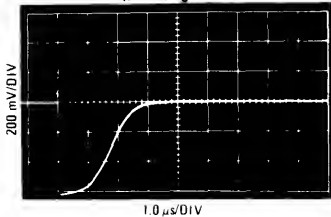
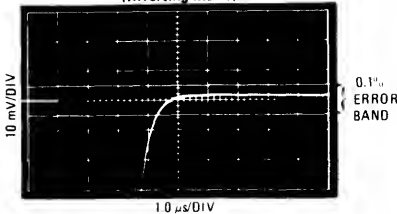


FIGURE 12 — EXPANDED WAVEFORM AT FALSE SUMMING NODE
(Inverting Mode)



The solution to these problems is the creation of a second or "false" summing node. The addition of two diodes at this node clamps the error voltage to limit the voltage excursion to the oscilloscope. Because of the voltage divider effect, only one-half of the actual error appears at this node. For extremely critical measurements, the capacitance of the diodes and the oscilloscope, and the settling time of the oscilloscope must be considered. The expression

$$t_{\text{setlg}} = \sqrt{x^2 + y^2 + z^2}$$

can be used to determine the actual amplifier settling time, where

t_{setlg} = observed settling time

x = amplifier settling time (to be determined)

y = false summing junction settling time

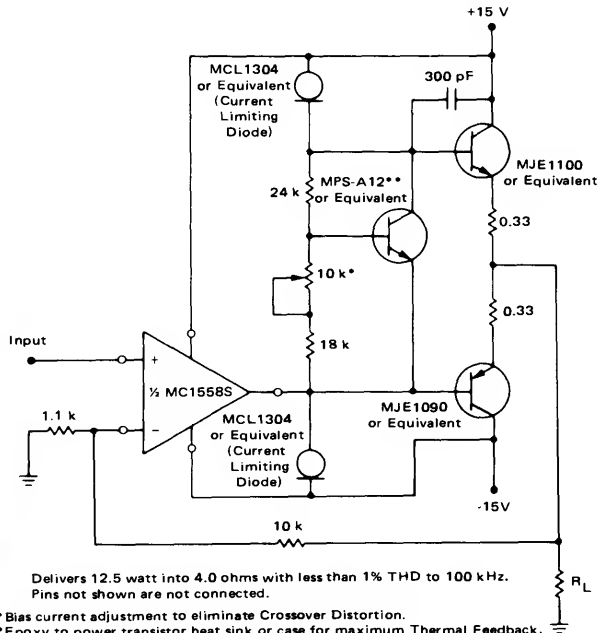
z = oscilloscope settling time

It should be remembered that to settle within $\pm 0.1\%$ requires $7RC$ time constants.

The $\pm 0.1\%$ factor was chosen for the MC1558S settling time as it is compatible with the $\pm 1/2$ LSB accuracy of the MC1508L-8 digital-to-analog converter. This D-to-A converter features $\pm 0.19\%$ maximum error.

TYPICAL APPLICATION

FIGURE 13 — 12.5-WATT WIDEBAND POWER AMPLIFIER



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

RF/IF/AUDIO AMPLIFIER

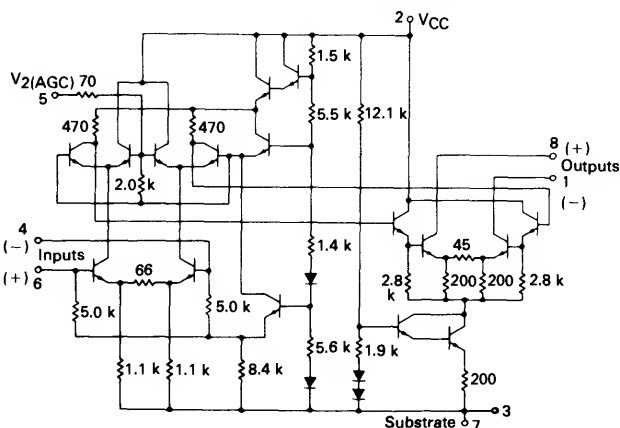
... an integrated circuit featuring wide-range AGC for use in RF/IF amplifiers and audio amplifiers over the temperature range, -40 to +85°C. See Motorola Application Note AN513 for design details.

- High Power Gain — 50 dB Typ at 10 MHz
45 dB Typ at 60 MHz
35 dB Typ at 100 MHz
- Wide-Range AGC — 60 dB Min, dc to 60 MHz
- 6.0 to 15 V Operation, Single-Polarity Power Supply

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+18	Vdc
Output Supply	V_O	+18	Vdc
AGC Supply	$V_2(\text{AGC})$	V_{CC}	Vdc
Differential Input Voltage	V_I	5.0	Vdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Junction Temperature	T_J	+150	°C

REPRESENTATIVE CIRCUIT SCHEMATIC

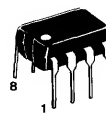


Pins 3 and 7 should both be connected to circuit ground.

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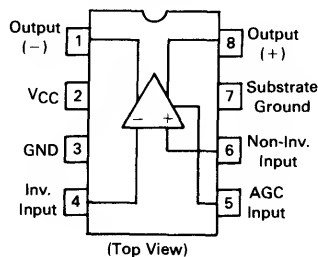
WIDEBAND AMPLIFIER WITH AGC

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 626

PIN CONNECTIONS



SCATTERING PARAMETERS ($V_{CC} = +12 \text{ Vdc}$, $T_A = +25^\circ\text{C}$, $Z_0 = 50 \Omega$)

Parameter	Symbol	f = MHz Typ		Unit
		30	60	
Input Reflection Coefficient	$ S_{11} $ θ_{11}	0.95 -7.3	0.93 -16	— °C
Output Reflection Coefficient	$ S_{22} $ θ_{22}	0.99 -3.0	0.98 -5.5	— °C
Forward Transmission Coefficient	$ S_{21} $ θ_{21}	16.8 128	14.7 64.3	— °C
Reverse Transmission Coefficient	S_{12} θ_{12}	0.00048 84.9	0.00092 79.2	— °C

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ELECTRICAL CHARACTERISTICS ($V_{CC} = 12 \text{ Vdc}$, $f = 60 \text{ MHz}$, $BW = 1.0 \text{ MHz}$, $T_A = 25^\circ\text{C}$)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Power Supply Current Drain	—	I_{CC}	—	—	17	mA
AGC Range (AGC) 5.0 V Min to 7.0 V Max	19	MAGC	-60	—	—	dB
Output Stage Current (Sum of Pins 1 and 8)	—	I_O	4.0	—	7.5	mA
Single Ended Power Gain $R_S = R_L = 50 \text{ Ohms}$	19	G_P	40	—	—	dB
Noise Figure $R_S = 50 \text{ Ohms}$	19	NF	—	6.0	—	dB
Power Dissipation	—	P_D	—	168	204	mW

TYPICAL CHARACTERISTICS

($V_2 \text{ (AGC)} = 0$, $V_{CC} = 12 \text{ Vdc}$, $T_A = +25^\circ\text{C}$ unless otherwise noted)

FIGURE 1 — UNNEUTRALIZED POWER GAIN versus FREQUENCY (Tuned Amplifier, See Figure 19)

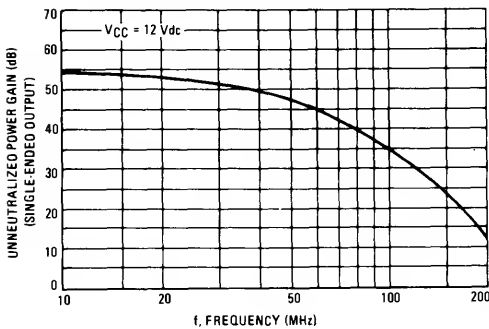


FIGURE 2 — VOLTAGE GAIN versus FREQUENCY (Video Amplifier, See Figure 21)

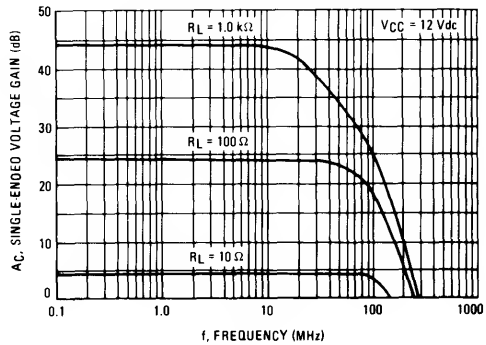


FIGURE 3 — DYNAMIC RANGE: OUTPUT VOLTAGE versus INPUT VOLTAGE (Video Amplifier, See Figure 21)

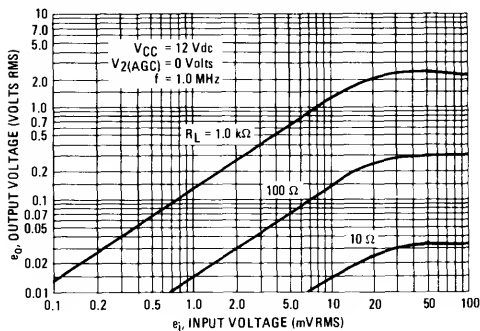


FIGURE 4 — VOLTAGE GAIN versus FREQUENCY (Video Amplifier, See Figure 21)

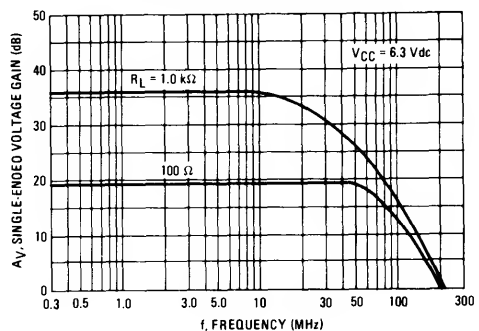


FIGURE 5 — VOLTAGE GAIN AND SUPPLY CURRENT versus SUPPLY VOLTAGE (Video Amplifier, See Figure 21)

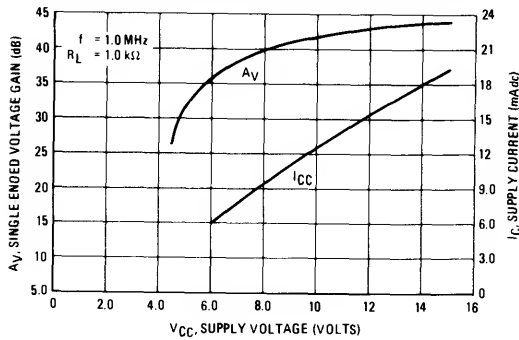


FIGURE 6 — TYPICAL GAIN REDUCTION versus AGC VOLTAGE

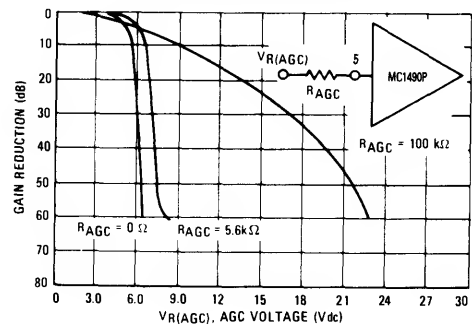


FIGURE 7 — TYPICAL GAIN REDUCTION versus AGC CURRENT

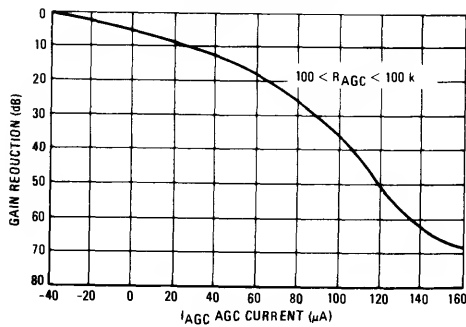


FIGURE 8 — FIXED TUNED POWER GAIN REDUCTION versus TEMPERATURE (See Test Circuit, Figure 19)

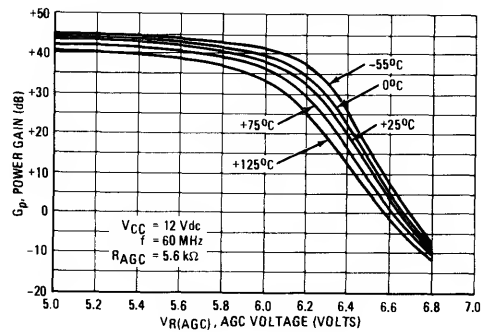


FIGURE 9 — POWER GAIN versus SUPPLY VOLTAGE (See Test Circuit, Figure 19)

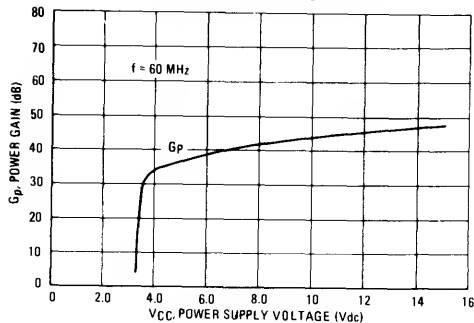
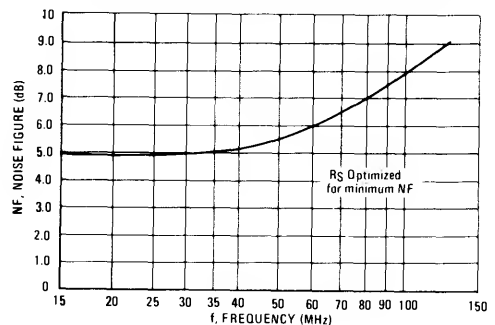


FIGURE 10 — NOISE FIGURE versus FREQUENCY



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FIGURE 11 — NOISE FIGURE versus SOURCE RESISTANCE

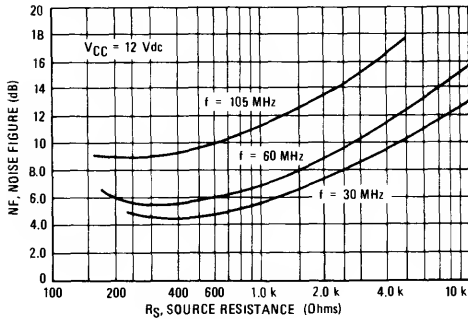


FIGURE 12 — NOISE FIGURE versus AGC GAIN REDUCTION

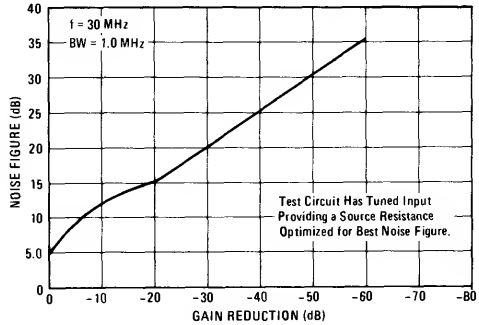


FIGURE 13 — HARMONIC DISTORTION versus AGC GAIN REDUCTION FOR AM CARRIER (For Test Circuit, See Figure 14)

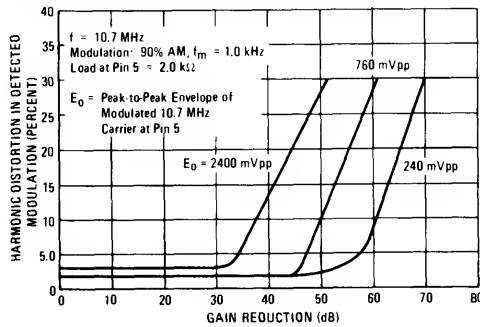
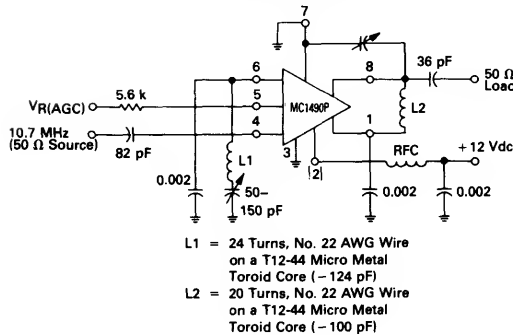


FIGURE 14 — 10.7 MHz AMPLIFIER
Gain $\approx 55 \text{ dB}$, BW $\approx 100 \text{ kHz}$



TYPICAL CHARACTERISTICS (continued)

2

FIGURE 15 — S_{11} AND S_{22} , INPUT AND OUTPUT REFLECTION COEFFICIENT

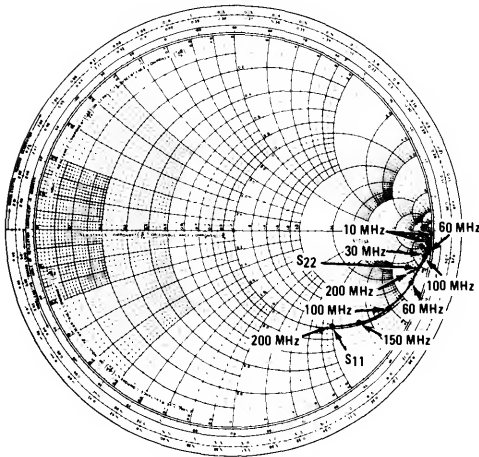


FIGURE 16 — S_{11} AND S_{22} , INPUT AND OUTPUT REFLECTION COEFFICIENT

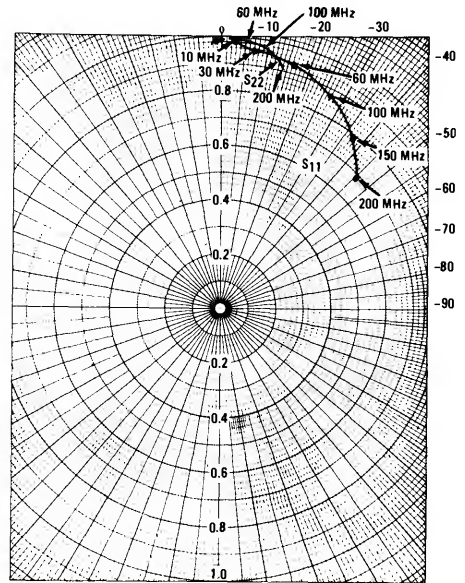


FIGURE 17 — S_{21} , FORWARD TRANSMISSION COEFFICIENT (GAIN)

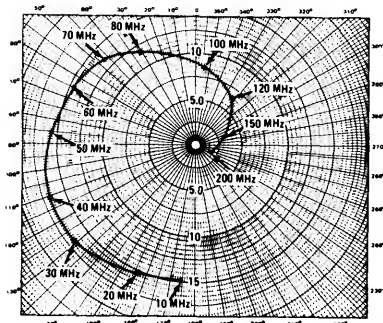
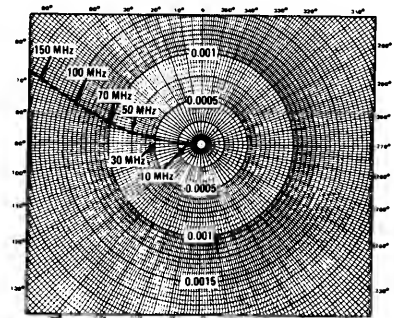


FIGURE 18 — S_{12} , REVERSE TRANSMISSION COEFFICIENT (FEEDBACK)



MC1490P

TYPICAL APPLICATIONS

FIGURE 19 — 60 MHz POWER GAIN TEST CIRCUIT

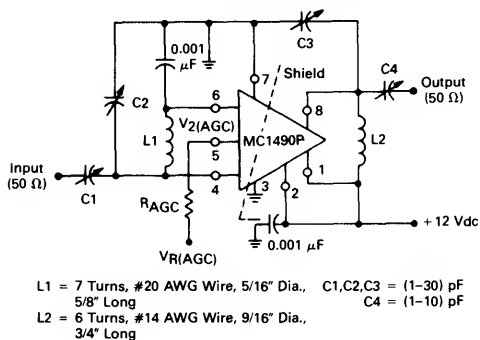


FIGURE 20 — PROCEDURE FOR SETUP USING FIGURE 19

Test	e_{in}	$V_2(AGC)$	$R_{AGC}(k\Omega)$
MAGC	2.23 mV (-40 dBm)	5-7 V	0
Gp	1.0 mV (-47 dBm)	≤ 5.0 V	5.6
NF	1.0 mV (-47 dBm)	≤ 5.0 V	5.6

FIGURE 21 — VIDEO AMPLIFIER

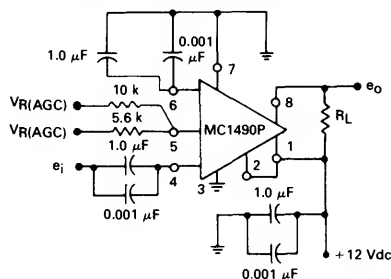


FIGURE 22 — 30 MHz AMPLIFIER
(Power Gain = 50 dB, BW ≈ 1.0 MHz)

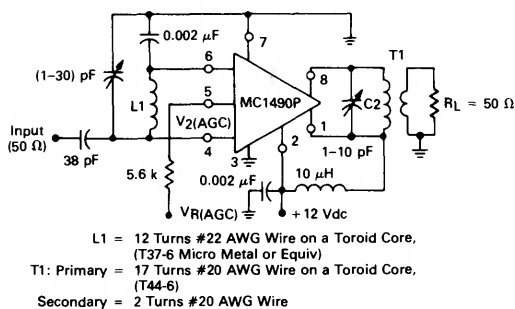
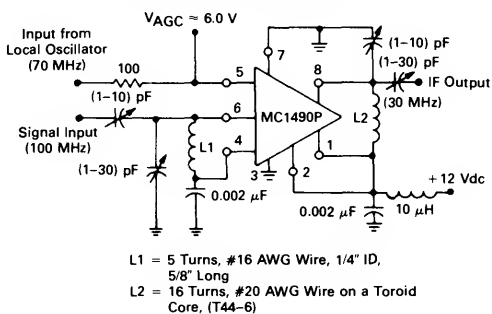


FIGURE 23 — 100 MHz MIXER



RF/IF/AUDIO AMPLIFIER

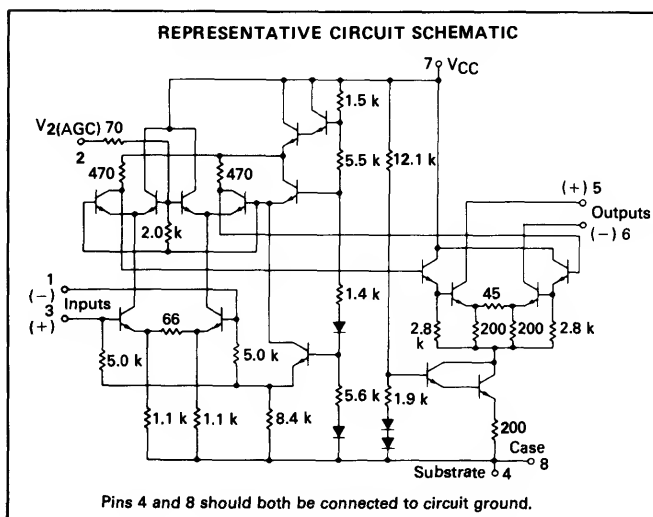
... an integrated circuit featuring wide-range AGC for use in RF/IF amplifiers and audio amplifiers over the temperature range, -55 to +125°C.

- High Power Gain — 50 dB Typ at 10 MHz
45 dB Typ at 60 MHz
35 dB Typ at 100 MHz
- Wide-Range AGC — 60 dB min, dc to 60 MHz
- Low Reverse Transfer Admittance — <10 μ mhos Typ at 60 MHz
- 6.0 to 15-Volt Operation, Single-Polarity Power Supply

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol*	Value	Unit
Power Supply Voltage	V_{CC}	+18	Vdc
Output Supply	V_O	+18	Vdc
AGC Supply	$V_2(\text{AGC})$	V_{CC}	Vdc
Differential Input Voltage	V_I	5.0	Vdc
Operating Temperature Range	T_A	-55 to +125	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Junction Temperature	T_J	+175	$^\circ\text{C}$

REPRESENTATIVE CIRCUIT SCHEMATIC

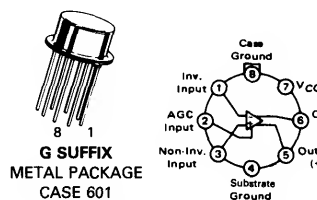


MC1590G

**WIDEBAND AMPLIFIER
WITH AGC**

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**

PIN CONNECTIONS



ADMITTANCE PARAMETERS
($V_{CC} = +12 \text{ Vdc}$, $T_A = +25^\circ\text{C}$)

Parameter	Symbol	f = MHz Typ		Unit
		30	60	
Single-Ended Input Admittance	g_{11} b_{11}	0.4 1.2	0.6 -3.0	mmhos
Single-Ended Output Admittance	g_{22} b_{22}	0.05 0.5	0.1 1.0	mmhos
Forward Transfer Admittance (Pin 1 to Pin 5)	Y_{21} θ_{21} (Polar)	175 -30	150 -105	mmhos $^\circ\text{C}$
Reverse Transfer Admittance*	g_{12} b_{12}	-0 -5.0	-0 -10	μ mhos

*The value of Reverse Transfer Admittance includes the feedback admittance of the test circuit used in the measurement. The total feedback capacitance (including test circuit) is 0.025 pF and is a more practical value for design calculations than the internal feedback of the device alone. (See Figure 10.)

SCATTERING PARAMETERS ($V_{CC} = +12 \text{ Vdc}$,
 $T_A = +25^\circ\text{C}$, $Z_0 = 50 \Omega$)

Parameter	Symbol	f = MHz Typ		Unit
		30	60	
Input Reflection Coefficient	S_{11} θ_{11}	0.95 -7.3	0.93 -16	$^\circ\text{C}$
Output Reflection Coefficient	S_{22} θ_{22}	0.99 -3.0	0.98 -5.5	$^\circ\text{C}$
Forward Transmission Coefficient	S_{21} θ_{21}	16.8 128	14.7 64.3	$^\circ\text{C}$
Reverse Transmission Coefficient	S_{12} θ_{12}	0.00048 84.9	0.00092 79.2	$^\circ\text{C}$

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ELECTRICAL CHARACTERISTICS ($V_{CC} = +12$ Vdc, $f = 60$ MHz, BW = 1.0 MHz, $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ unless otherwise noted)

Characteristic	Fig.	Symbol	Min	Typ	Max	Unit
AGC Range ($V_2(\text{AGC}) = 5.0$ V to 7.0 V) ($V_2(\text{AGC}) = 5.0$ V to 7.0 V, $T_A = 25^\circ\text{C}$)	24	M_{AGC}	58 60	— 68	— —	dB
Single-Ended Power Gain ($T_A = 25^\circ\text{C}$)	24	G_p	37 40	— 45	— —	dB
Noise Figure (R_s optimized for best NF) ($T_A = 25^\circ\text{C}$)	24	NF	—	6.0	7.0	dB
Output Stage Current (Sum of Pins 5 and 6) ($T_A = 25^\circ\text{C}$)	32	I_O	3.5 4.0	— 5.6	8.0 7.5	mA
Output Current Matching (Magnitude of Difference of Output Currents) ($I_5 - I_6$) ($T_A = 25^\circ\text{C}$)	32	ΔI_O	—	0.7	—	mA
Power Supply Current ($V_O = 0$ V) ($V_O = 0$ V, $T_A = 25^\circ\text{C}$)	32	I_{CC}	— —	— 14	20 17	mA
Power Consumption ($12 \times I_{CC}$) ($V_I = 0$ V) ($V_I = 0$ V, $T_A = 25^\circ\text{C}$)	—	P_C	— —	— 168	240 204	mW

FIGURE 1 – UNNEUTRALIZED POWER GAIN versus FREQUENCY
(Tuned Amplifier, See Figure 24)

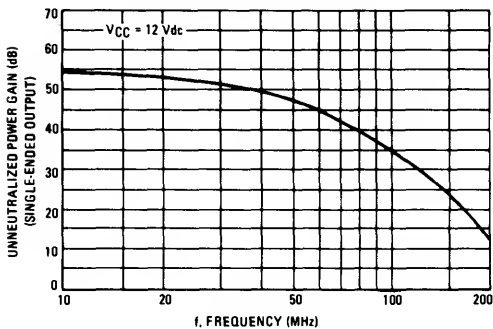
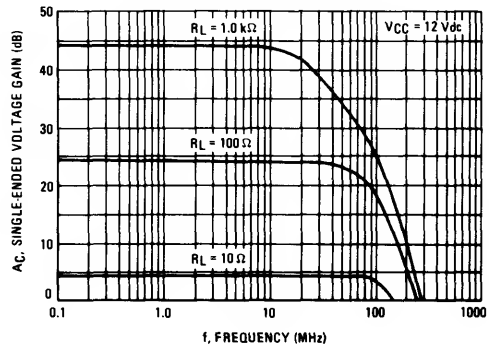


FIGURE 2 – VOLTAGE GAIN versus FREQUENCY
(Video Amplifier, See Figure 26)



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TYPICAL CHARACTERISTICS

(V_2 (AGC) = 0, V_{CC} = 12 Vdc, T_A = +25°C unless otherwise noted)

FIGURE 3 – DYNAMIC RANGE: OUTPUT VOLTAGE versus INPUT VOLTAGE (Video Amplifier, See Figure 26)

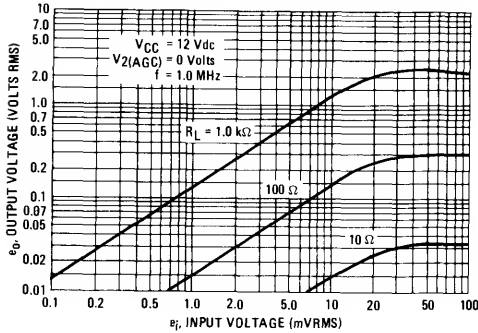


FIGURE 4 – VOLTAGE GAIN versus FREQUENCY (Video Amplifier, See Figure 26)

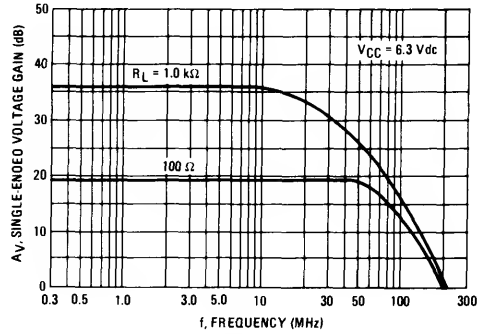


FIGURE 5 – VOLTAGE GAIN AND SUPPLY CURRENT versus SUPPLY VOLTAGE (Video Amplifier, See Figure 26)

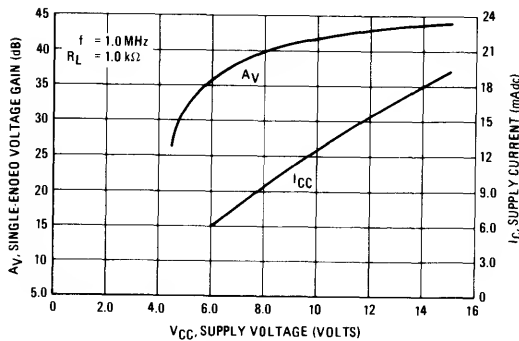


FIGURE 6 – TYPICAL GAIN REDUCTION versus AGC VOLTAGE

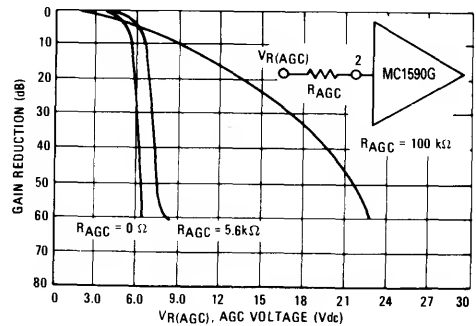


FIGURE 7 – TYPICAL GAIN REDUCTION versus AGC CURRENT

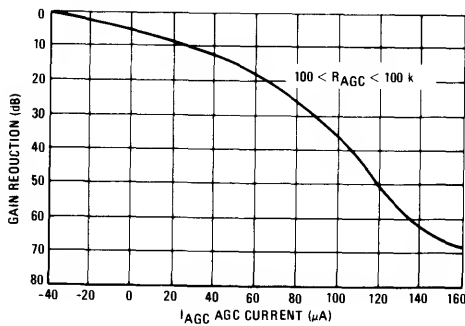
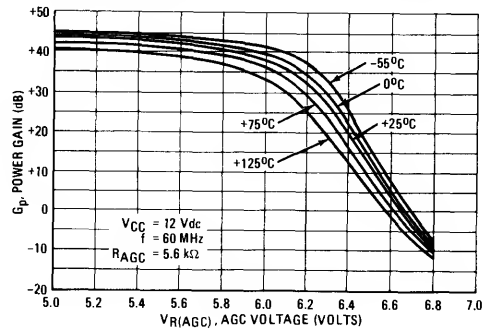


FIGURE 8 – FIXED TUNED POWER GAIN REDUCTION versus TEMPERATURE (See Test Circuit, Figure 24)



TYPICAL CHARACTERISTICS (continued)

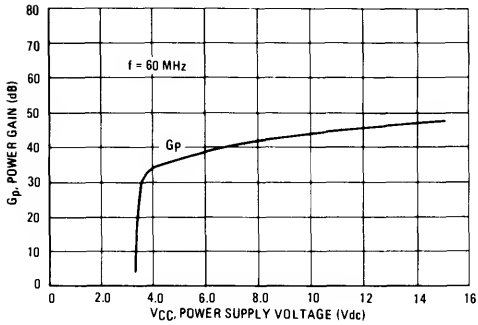
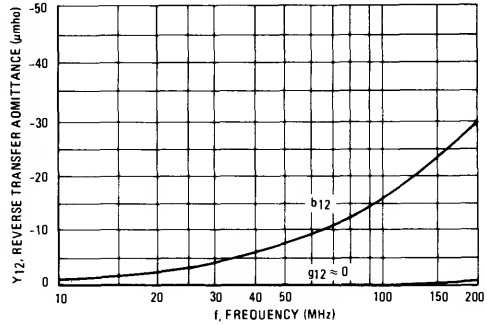
FIGURE 9 – POWER GAIN versus SUPPLY VOLTAGE
(See Test Circuit, Figure 24)FIGURE 10 – REVERSE TRANSFER ADMITTANCE versus FREQUENCY
(See Parameter Table, Page 1)

FIGURE 11 – NOISE FIGURE versus FREQUENCY

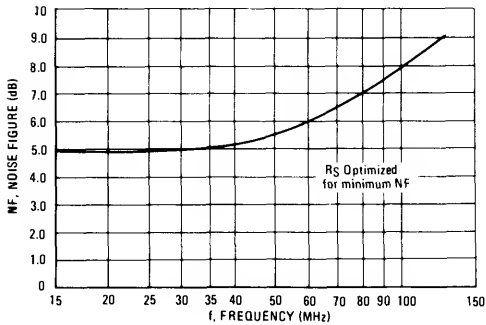


FIGURE 12 – NOISE FIGURE versus SOURCE RESISTANCE

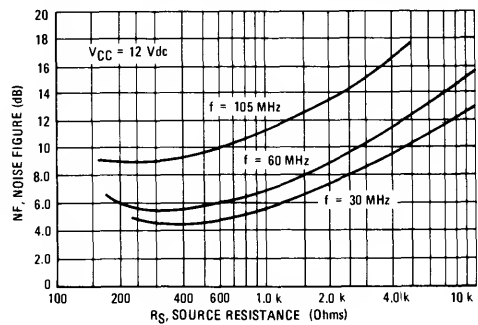
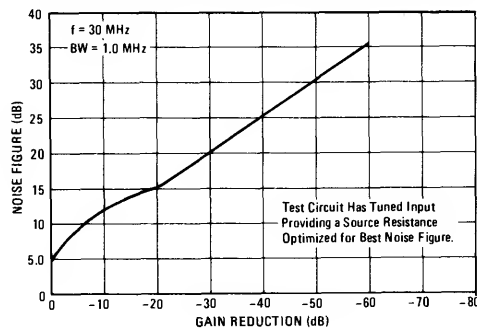


FIGURE 13 – NOISE FIGURE versus AGC GAIN REDUCTION



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TYPICAL CHARACTERISTICS (continued)

2

FIGURE 14 – SINGLE-ENDED OUTPUT ADMITTANCE

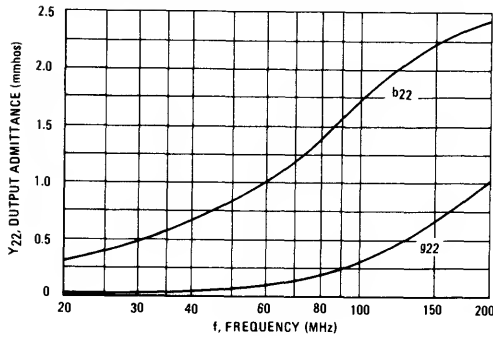


FIGURE 15 – SINGLE-ENDED INPUT ADMITTANCE

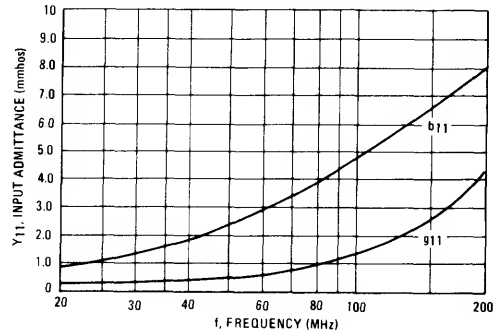


FIGURE 16 – HARMONIC DISTORTION versus AGC GAIN REDUCTION FOR AM CARRIER (For Test Circuit, See Figure 17)

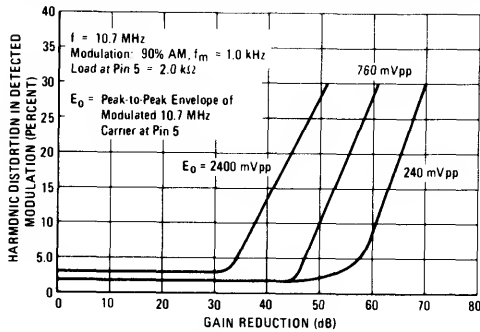


FIGURE 17 – 10.7 MHz AMPLIFIER
Gain ≈ 55 dB, BW ≈ 100 kHz

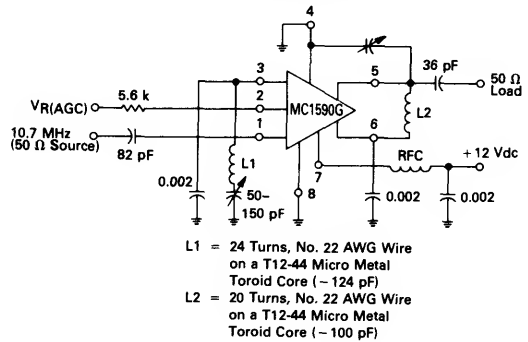


FIGURE 18 – Y₂₁, FORWARD TRANSFER ADMITTANCE
RECTANGULAR FORM

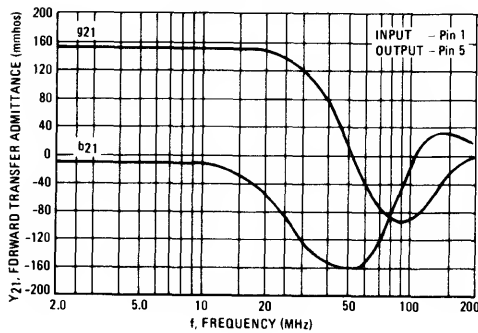
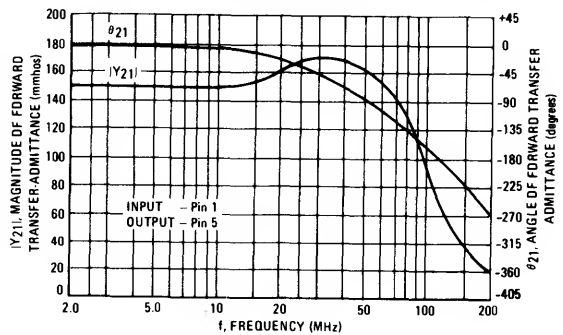


FIGURE 19 – Y₂₁, FORWARD TRANSFER ADMITTANCE
POLAR FORM



TYPICAL CHARACTERISTICS (continued)

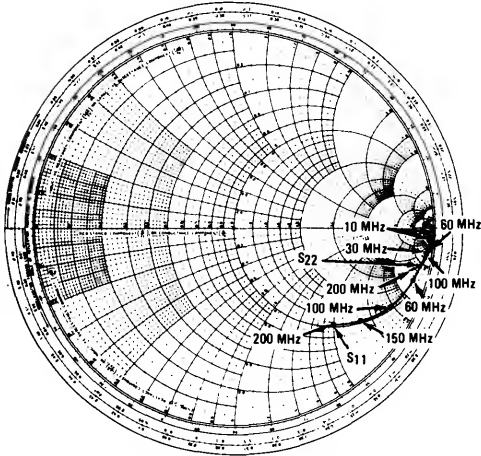
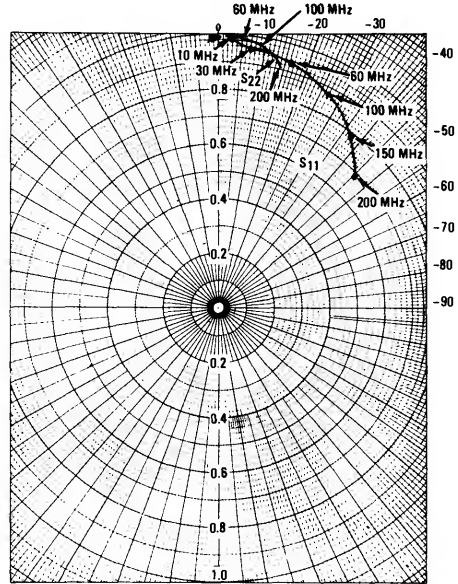
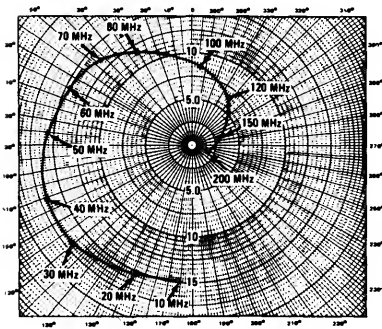
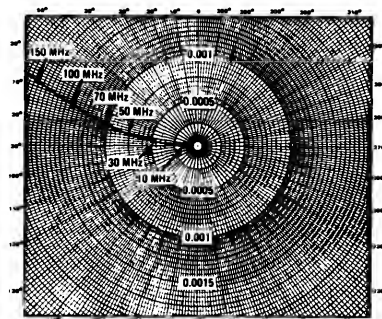
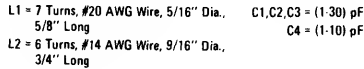
FIGURE 20 — S_{11} AND S_{22} . INPUT AND OUTPUT REFLECTION COEFFICIENTFIGURE 21 — S_{11} AND S_{22} . INPUT AND OUTPUT REFLECTION COEFFICIENTFIGURE 22 — S_{21} . FORWARD TRANSMISSION COEFFICIENT (GAIN)FIGURE 23 — S_{12} . REVERSE TRANSMISSION COEFFICIENT (FEEDBACK)

FIGURE 24 — 60 MHz POWER GAIN TEST CIRCUIT



Input (50 Ω)

38 pF

(1.30) pF

0.002 μ F

3

4

MC1590G

2

1

5.6 k

0.002 μ F

V_R(AGC)

5

6

7

8

10 μ H

1-10 pF

10 μ H

+12 Vdc

T1

R_L = 50 Ω

L1 = 12 Turns #22 AWG Wire on a Toroid Core, (T37-6 Micro Metal or Equiv)

T1: Primary = 17 Turns #20 AWG Wire on a Toroid Core, (T44-6 Micro Metal or Equiv)

Secondary = 2 Turns #20 AWG Wire

Input from Local Oscillator (70 MHz)

Signal Input (100 MHz)

VAGC = 6.0 V

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IF Output (30 MHz)

+12 Vdc

L1 = 5 Turns, #16 AWG Wire, 1/4" ID, 5/8" Long

L2 = 16 Turns, #20 AWG Wire on a Toroid Core, (T44-6 Micro Metal or Equiv)

VR (AGC)

Input (50 Ω)

24 pF

5.1 k

200 μ H

(1-10) pF

0.002 μ F

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Shield

1

2

3

4

5

6

7

8

+12 Vdc

(1-10) pF

10 μ H

RFC

10 k

T1

0.002 μ F

39 pF

0.002 μ F

0.001 μ F

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Shield

1

2

3

4

5

6

7

8

10 μ H

RFC

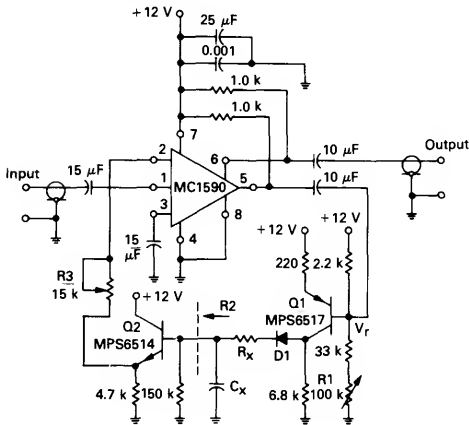
Output (50 Ω)

T1: Primary Winding = 15 Turns, #22 AWG Wire, 1/4" ID Air Core
Secondary Winding = 4 Turns, #22 AWG Wire,
Coefficient of Coupling \approx 1.0

T2: Primary Winding = 10 Turns, #22 AWG Wire, 1/4" ID Air Core
Secondary Winding = 2 Turns, #22 AWG Wire,
Coefficient of Coupling \approx 1.0

TYPICAL APPLICATIONS (continued)

FIGURE 30 — SPEECH COMPRESSOR



DESCRIPTION OF SPEECH COMPRESSOR

The amplifier drives the base of a PNP MPS6517 operating common-emitter with a voltage gain of approximately 20. The control R1 varies the quiescent Q point of this transistor so that varying amounts of signal exceed the level V_r . Diode D1 rectifies the positive peaks of Q1's output only when these peaks are greater than $V_r \approx 7.0$ Volts. The resulting output is filtered by C_x , R_x .

R_x controls the charging time constant or attack time. C_x is involved in both charge and discharge. R2 (the 150 kΩ and input resistance of the emitter-follower Q2) controls the decay time. Making the decay long and attack short is accomplished by making R_x small and R2 large. (A Darlington emitter-follower may be needed if extremely slow decay times are required.)

The emitter-follower Q2 drives the AGC Pin 2 of the MC1590G and reduces the gain. R3 controls the slope of signal compression. The following graph (Figure 31) details performance with R3 set to 15 kΩ.

FIGURE 31 — OUTPUT VOLTAGE versus INPUT VOLTAGE

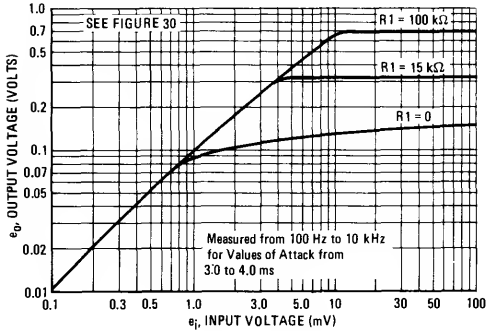
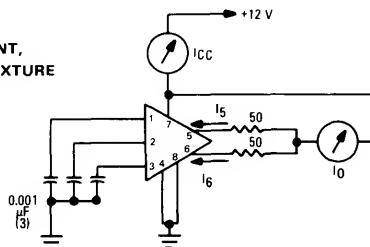


TABLE 1 — DISTORTION versus FREQUENCY

FREQUENCY	DISTORTION		DISTORTION	
	10 mV e_i	100 mV e_i	10 mV e_i	100 mV e_i
100 Hz	3.5%	12%	15%	27%
300 Hz	2%	10%	6%	20%
1.0 kHz	1.5%	8%	3%	9%
10 kHz	1.5%	8%	1%	3%
100 kHz	1.5%	8%	1%	3%
Notes 1 and 2		Notes 3 and 4		

- Note: (1) Decay = 300 ms
Attack = 20 ms
(2) $C_x = 7.5 \mu F$
 $R_x = 0$ (Short)
(3) Decay = 20 ms
Attack = 3 ms
(4) $C_x = 0.68 \mu F$
 $R_x = 1.5 k\Omega$

FIGURE 32 — OUTPUT CURRENT, CURRENT MATCH AND I_{CC} FIXTURE



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

2

MONOLITHIC OPERATIONAL AMPLIFIER

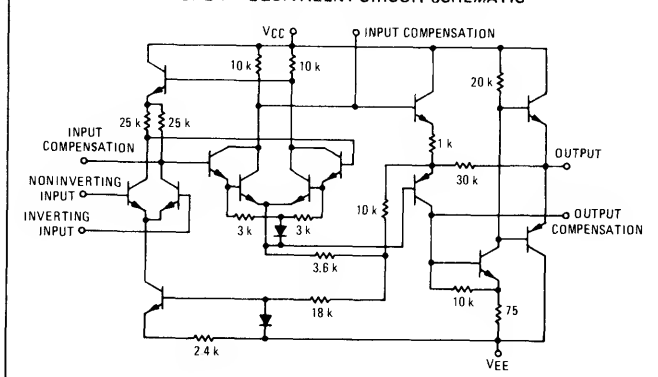
... designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- High-Performance Open Loop Gain Characteristics
 $A_{VOL} = 45,000$ typical
- Low Temperature Drift — $\pm 3.0 \mu V/^{\circ}C$ typical (MC1709)
- Large Output Voltage Swing — ± 14 V typical @ ± 15 V Supply
- Low Output Impedance — $z_o = 150$ ohms typical

MAXIMUM RATINGS ($T_A = +25^{\circ}C$ unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 -18	Vdc
Input Differential Voltage Range	V_{IDR}	± 5.0	Volts
Input Common-Mode Range	V_{ICR}	± 10	Volts
Output Load Current	I_L	10	mA
Output Short-Circuit Duration	t_S	5.0	s
Power Dissipation (Package Limitation)	P_D		
Metal Can		680	mW
Derate above $T_A = +25^{\circ}C$		4.6	mW/ $^{\circ}C$
Plastic Dual In-Line Packages (MC1709C only)		625	mW
Derate above $T_A = +25^{\circ}C$		5.0	mW/ $^{\circ}C$
Ceramic Dual In-Line Package		750	mW/ $^{\circ}C$
Derate above $T_A = +25^{\circ}C$		6.0	mW/ $^{\circ}C$
Operating Ambient Temperature Range	T_A	-55 to +125 0 to +70	$^{\circ}C$
Storage Temperature Range	T_{stg}	-65 to +150 -55 to +125	$^{\circ}C$
Metal and Ceramic Packages			
Plastic Packages			

FIGURE 1 — EQUIVALENT CIRCUIT SCHEMATIC

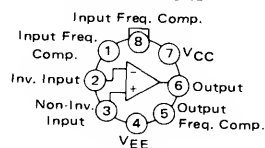


**MC1709
MC1709A
MC1709C**

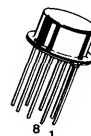
OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

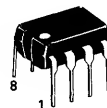
PIN CONNECTIONS



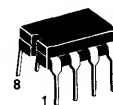
(Top View)



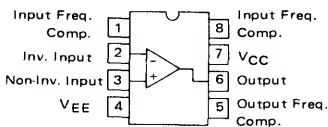
**G SUFFIX
METAL PACKAGE
CASE 601**



**P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MC1709C Only)**



**U SUFFIX
CERAMIC PACKAGE
CASE 693**



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC1709CG MC1709CU MC1709CP1	0 $^{\circ}C$ to +70 $^{\circ}C$	Metal Can Ceramic DIP Plastic DIP
MC1709G,AG MC1709AU	-55 $^{\circ}C$ to +125 $^{\circ}C$	Metal Can Ceramic DIP

MC1709, MC1709A, MC1709C

2

ELECTRICAL CHARACTERISTICS (unless otherwise noted, $+9.0\text{ V} \leq V_{CC} \leq 15\text{ V}$, $-9.0\text{ V} \geq V_{EE} \geq -15\text{ V}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	MC1709A			MC1709			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10\text{ k}\Omega$)	V_{IO}	—	0.6	2.0	—	1.0	5.0	mV
Input Offset Current	I_{IO}	—	10	50	—	50	200	nA
Input Bias Current	I_{IB}	—	100	200	—	200	500	nA
Input Resistance	r_i	350	700	—	150	400	—	k Ω
Output Resistance	r_o	—	150	—	—	150	—	Ω
Power Supply Currents ($V_{CC} = 15\text{ V}$, $V_{EE} = -15\text{ V}$)	I_{CC}, I_{EE}	—	2.5	3.6	—	—	—	mA
Power Consumption ($V_{CC} = 15\text{ V}$, $V_{EE} = -15\text{ V}$)	P_C	—	75	108	—	80	165	mW
Transient Response ($V_{CC} = 15\text{ V}$, $V_{EE} = -15\text{ V}$) See Figure 8	Risetime	—	—	1.5	—	0.3	1.0	μs
	Overshoot	—	—	30	—	10	30	%

ELECTRICAL CHARACTERISTICS (unless otherwise noted, $+9.0\text{ V} \leq V_{CC} \leq 15\text{ V}$, $-9.0\text{ V} \geq V_{EE} \geq -15\text{ V}$, $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$)

Characteristic	Symbol	MC1709A			MC1709			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10\text{ k}\Omega$)	V_{IO}	—	—	3.0	—	—	6.0	mV
Average Temperature Coefficient of Input Offset Voltage ($R_S = 50\text{ }\Omega$, $T_A = 25^\circ\text{C}$ to 125°C) ($R_S = 50\text{ }\Omega$, $T_A = -55^\circ\text{C}$ to 25°C) ($R_S = 50\text{ }\Omega$, $T_A = -55^\circ\text{C}$ to 125°C) ($R_S = 10\text{ k}\Omega$, $T_A = 25^\circ\text{C}$ to 125°C) ($R_S = 10\text{ k}\Omega$, $T_A = -55^\circ\text{C}$ to 25°C) ($R_S = 10\text{ k}\Omega$, $T_A = -55^\circ\text{C}$ to 125°C)	$\Delta V_{IO}/\Delta T$	—	1.8	10	—	—	—	$\mu\text{V}/^\circ\text{C}$
		—	1.8	10	—	—	—	
		—	—	—	—	3.0	—	
		—	2.0	15	—	—	—	
		—	4.8	25	—	—	—	
		—	—	—	—	6.0	—	
Input Offset Current ($T_A = -55^\circ\text{C}$) ($T_A = 125^\circ\text{C}$)	I_{IO}	—	40	250	—	100	500	nA
		—	3.5	50	—	20	200	
Average Temperature Coefficient of Input Offset Current ($T_A = -55^\circ\text{C}$ to 25°C) ($T_A = 25^\circ\text{C}$ to 125°C)	$\Delta I_{IO}/\Delta T$	—	0.45	2.8	—	—	—	nA/ $^\circ\text{C}$
		—	0.08	0.5	—	—	—	
Input Bias Current ($T_A = -55^\circ\text{C}$)	I_{IB}	—	300	600	—	500	1500	nA
Input Resistance ($T_A = -55^\circ\text{C}$)	r_i	85	170	—	40	100	—	k Ω
Input Common-Mode Voltage Range ($V_{CC} = 15\text{ V}$, $V_{EE} = -15\text{ V}$)	V_{ICR}	± 8.0	± 10	—	± 8.0	± 10	—	V
Common Mode Rejection Ratio ($R_S \leq 10\text{ k}\Omega$)	CMRR	80	110	—	70	90	—	dB
Supply Voltage Rejection Ratio ($V_{CC} = 15\text{ V}$, $V_{EE} = -15\text{ V}$, $R_S \leq 10\text{ k}\Omega$)	PSRR	—	40	100	—	25	150	$\mu\text{V}/\text{V}$
Large Signal Voltage Gain ($V_{CC} = 15\text{ V}$, $V_{EE} = -15\text{ V}$, $R_L \geq 2.0\text{ k}\Omega$, $V_O \geq \pm 15\text{ V}$)	A_V	25	45	70	25	45	70	V/mV
Output Voltage Range ($V_{CC} = 15\text{ V}$, $V_{EE} = -15\text{ V}$) ($R_L \geq 10\text{ k}\Omega$) ($R_L \geq 2.0\text{ k}\Omega$)	V_{OR}	—	—	—	—	—	—	V
		± 12	± 14	—	± 12	± 14	—	
		± 10	± 13	—	± 10	± 13	—	
Power Supply Currents ($V_{CC} = 15\text{ V}$, $V_{EE} = -15\text{ V}$) ($T_A = -55^\circ\text{C}$) ($T_A = 125^\circ\text{C}$)	I_{CC}/I_{EE}	—	2.7	4.5	—	—	—	mA
		—	2.1	3.0	—	—	—	
Power Consumption ($V_{CC} = 15\text{ V}$, $V_{EE} = -15\text{ V}$) ($T_A = -55^\circ\text{C}$) ($T_A = 125^\circ\text{C}$)	P_C	—	81	135	—	—	—	mW
		—	63	90	—	—	—	

MC1709, MC1709A, MC1709C

ELECTRICAL CHARACTERISTICS (unless otherwise noted, $V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	MC1709C			Unit
		Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10\text{ k}\Omega$, $9.0\text{ V} \leq V_{CC} \leq 15\text{ V}$, $-9.0\text{ V} \geq V_{EE} \geq -15\text{ V}$)	V_{IO}	—	2.0	7.5	mV
Input Offset Current	I_{IO}	—	100	500	nA
Input Bias Current	I_{IB}	—	300	1500	nA
Input Resistance	r_i	50	250	—	k Ω
Output Resistance	r_o	—	150	—	Ω
Power Consumption	P_C	—	80	200	mW
Large Signal Voltage Gain ($R_L \geq 2.0\text{ k}\Omega$, $V_O = \pm 10\text{ V}$)	A_V	15	45	—	V/mV
Output Voltage Range ($R_L \geq 10\text{ k}\Omega$) ($R_L \geq 2.0\text{ k}\Omega$)	V_{OR}	± 12 ± 10	± 14 ± 13	—	V
Input Common-Mode Voltage Range	V_{ICR}	± 8.0	± 10	—	V
Common Mode Rejection Ratio ($R_S \leq 10\text{ k}\Omega$)	CMRR	65	90	—	dB
Supply Voltage Rejection Ratio ($R_S \leq 10\text{ k}\Omega$)	PSRR	—	25	200	$\mu\text{V/V}$
Transient Response See Figure 8 Rise Time Overshoot	t_{TLH} OS	— —	0.3 10	— —	μs %

ELECTRICAL CHARACTERISTICS (unless otherwise specified, $V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = 0^\circ\text{C}$ to 70°C)

Parameter	Symbol	MC1709C			Unit
		Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10\text{ k}\Omega$, $9.0\text{ V} \leq V_{CC} \leq 15\text{ V}$, $-9.0\text{ V} \geq V_{EE} \geq -15\text{ V}$)	V_{IO}	—	—	10	mV
Input Offset Current	I_{IO}	—	—	750	nA
Input Bias Current	I_{IB}	—	—	2.0	μA
Large Signal Voltage Gain ($R_L \geq 2.0\text{ k}\Omega$, $V_O = \pm 10\text{ V}$)	A_V	12	—	—	V/mV
Input Resistance	r_i	35	—	—	k Ω

TYPICAL CHARACTERISTICS

FIGURE 2 – TEST CIRCUIT
($V_{CC} = +15\text{ Vdc}$, $V_{EE} = -15\text{ Vdc}$, $T_A = +25^\circ\text{C}$)

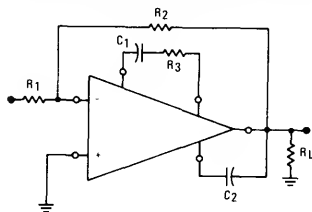


Fig. No.	Curve No.	Test Conditions				
		$R_1(\Omega)$	$R_2(\Omega)$	$R_3(\Omega)$	$C_1(\text{pF})$	$C_2(\text{pF})$
3	1	10 k	10 k	1.5 k	5.0 k	200
	2	10 k	100 k	1.5 k	500	20
	3	10 k	1.0 M	1.5 k	100	3.0
	4	1.0 k	1.0 M	0	10	3.0
4	1	1.0 k	1.0 M	0	10	3.0
	2	10 k	1.0 M	1.5 k	100	3.0
	3	10 k	100 k	1.5 k	500	20
	4	10 k	10 k	1.5 k	5.0 k	200
5	1	0	∞	1.5 k	5.0 k	200
	2	0	∞	1.5 k	500	20
	3	0	∞	1.5 k	100	3.0
	4	0	∞	0	10	3.0

MC1709, MC1709A, MC1709C

FIGURE 3 – LARGE SIGNAL SWING versus FREQUENCY

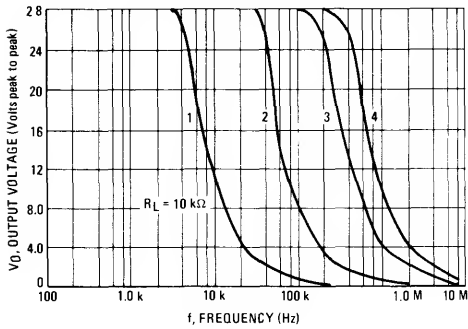


FIGURE 4 – CLOSED LOOP VOLTAGE GAIN versus FREQUENCY

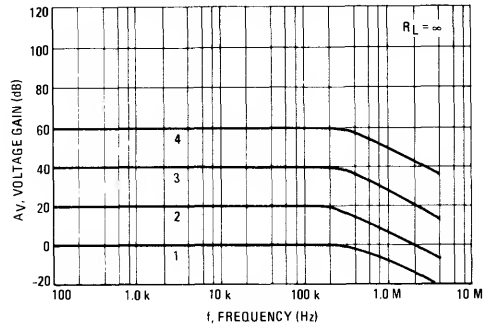


FIGURE 5 – OPEN LOOP VOLTAGE GAIN versus FREQUENCY

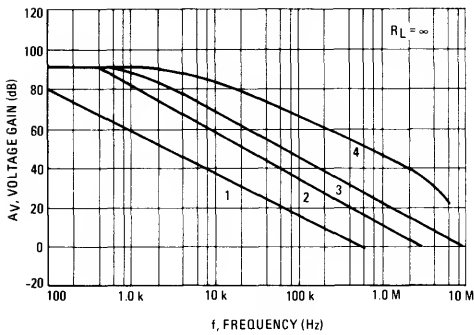


FIGURE 6 – VOLTAGE GAIN versus POWER SUPPLY VOLTAGE

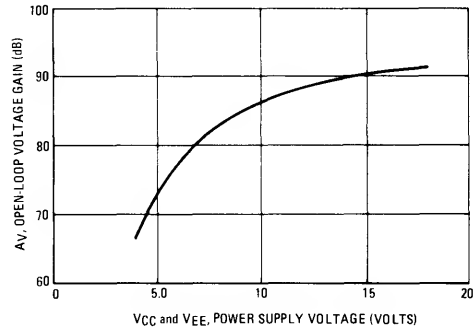


FIGURE 7 – SLEW RATE versus CLOSED LOOP GAIN USING RECOMMENDED COMPENSATION NETWORKS

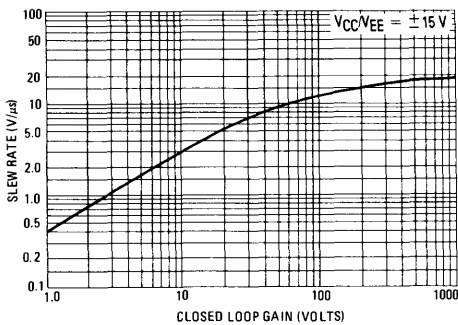
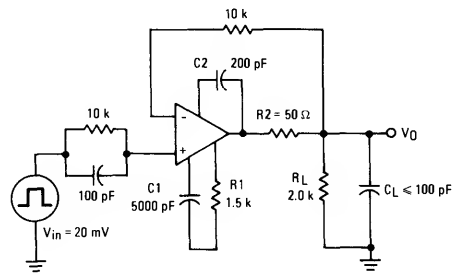


FIGURE 8 – TRANSIENT RESPONSE TEST CIRCUIT



DIFFERENTIAL VIDEO AMPLIFIER

... a wideband amplifier with differential input and differential output. Gain is fixed at 10, 100, or 400 without external components or, with the addition of one external resistor, gain becomes adjustable from 10 to 400.

- Bandwidth — 120 MHz typical @ $A_{vd} = 10$
- Rise Time — 2.5 ns typical @ $A_{vd} = 10$
- Propagation Delay Time — 3.6 ns typical @ $A_{vd} = 10$

FIGURE 1 — BASIC CIRCUIT

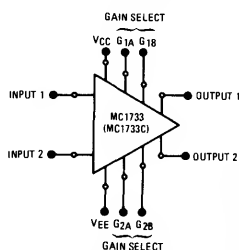


FIGURE 2 — VOLTAGE GAIN ADJUST CIRCUIT

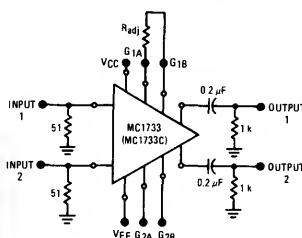
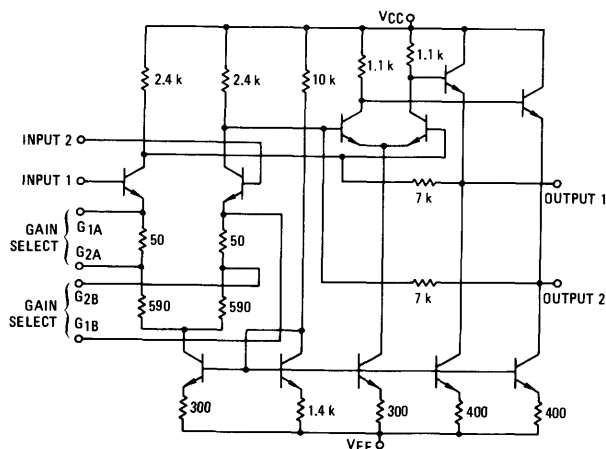


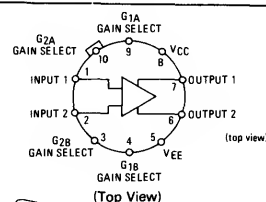
FIGURE 3 — EQUIVALENT CIRCUIT SCHEMATIC



MC1733 MC1733C

DIFFERENTIAL VIDEO WIDEBAND AMPLIFIER

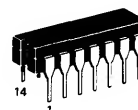
SILICON MONOLITHIC INTEGRATED CIRCUIT



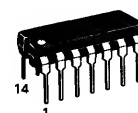
G SUFFIX
METAL PACKAGE
CASE 603



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

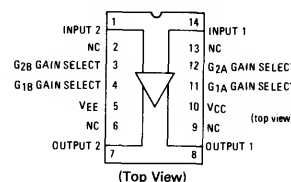


L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
MC1733G MC1733L	-55°C to +125°C	Metal Can Ceramic DIP
MC1733CD MC1733CG MC1733CL MC1733CP	0°C to +70°C	SO-14 Metal Can Ceramic DIP Plastic DIP

MC1733, MC1733C

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V _{CC} V _{EE}	+8.0 -8.0	Volts
Differential Input Voltage	V _{in}	±5.0	Volts
Common-Mode Input Voltage	V _{ICM}	±6.0	Volts
Output Current	I _O	10	mA
Internal Power Dissipation (Note 1) Metal Can Package Ceramic Dual In-Line Package	P _D	500 500	mW
Operating Temperature Range MC1733C MC1733	T _A	0 to +70 -55 to +125	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

2

ELECTRICAL CHARACTERISTICS (V_{CC} = +6.0 Vdc, V_{EE} = -6.0 Vdc, at T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC1733			MC1733C			Units
		Min	Typ	Max	Min	Typ	Max	
Differential Voltage Gain Gain 1 (Note 2) Gain 2 (Note 3) Gain 3 (Note 4)	A _{vd}	300 90 9.0	400 100 10	500 110 11	250 80 8.0	400 100 10	600 120 12	V/V
Bandwidth (R _s = 50 Ω) Gain 1 Gain 2 Gain 3	BW	— — —	40 90 120	— — —	— — —	40 90 120	— — —	MHz
Rise Time (R _s = 50 Ω, V _O = 1 Vp-p) Gain 1 Gain 2 Gain 3	t _{TLH} t _{THL}	— — —	10.5 4.5 2.5	— 10 —	— — —	10.5 4.5 2.5	— 12 —	ns
Propagation Delay (R _s = 50 Ω, V _O = 1 Vp-p) Gain 1 Gain 2 Gain 3	t _{PLH} t _{PHL}	— — —	7.5 6.0 3.6	— 10 —	— — —	7.5 6.0 3.6	— 10 —	ns
Input Resistance Gain 1 Gain 2 Gain 3	R _{in}	— 20 —	4.0 30 250	— — —	— 10 —	4.0 30 250	— — —	kΩ
Input Capacitance (Gain 2)	C _{in}	—	2.0	—	—	2.0	—	pF
Input Offset Current (Gain 3)	I _{IO}	—	0.4	3.0	—	0.4	5.0	μA
Input Bias Current (Gain 3)	I _{IB}	—	9.0	20	—	9.0	30	μA
Input Noise Voltage (R _s = 50 Ω, BW = 1 kHz to 10 MHz)	V _n	—	12	—	—	12	—	μV(rms)
Input Voltage Range (Gain 2)	V _{in}	±1.0	—	—	±1.0	—	—	V
Common-Mode Rejection Ratio Gain 2 (V _{CM} = ±1 V, f ≤ 100 kHz) Gain 2 (V _{CM} = ±1 V, f = 5 MHz)	CMRR	60 —	86 60	— —	60 —	86 60	— —	dB
Supply Voltage Rejection Ratio Gain 2 (ΔV _S = ±0.5 V)	PSRR	50	70	—	50	70	—	dB
Output Offset Voltage Gain 1 Gain 2 and Gain 3	V _{OO}	— — —	0.6 0.35 —	1.5 1.0 —	— — —	0.6 0.35 —	1.5 1.5 —	V
Output Common-Mode Voltage (Gain 3)	V _{CMO}	2.4	2.9	3.4	2.4	2.9	3.4	V
Output Voltage Swing (Gain 2)	V _O	3.0	4.0	—	3.0	4.0	—	Vp-p
Output Sink Current (Gain 2)	I _O	2.5	3.6	—	2.5	3.6	—	mA
Output Resistance	R _{out}	—	20	—	—	20	—	Ω
Power Supply Current (Gain 2)	I _D	—	18	24	—	18	24	mA

MC1733, MC1733C

ELECTRICAL CHARACTERISTICS ($V_{CC} = +6.0$ Vdc, $V_{EE} = -6.0$ Vdc, at $T_A = T_{high}$ to T_{low} unless otherwise noted.)*

Characteristic	Symbol	MC1733			MC1733C			Units
		Min	Typ	Max	Min	Typ	Max	
Differential Voltage Gain	A_{vd}							V/V
Gain 1 (Note 2)		200	—	600	250	—	600	
Gain 2 (Note 3)		80	—	120	80	—	120	
Gain 3 (Note 4)		8.0	—	12	8.0	—	12	
Input Resistance	R_{in}							k Ω
Gain 2		8.0	—	—	8.0	—	—	
Input Offset Current (Gain 3)	$ I_{IO} $	—	—	5.0	—	—	6.0	μ A
Input Bias Current (Gain 3)	I_{IB}	—	—	40	—	—	40	μ A
Input Voltage Range (Gain 2)	V_{in}	± 1.0	—	—	± 1.0	—	—	V
Common-Mode Rejection Ratio	CMRR							dB
Gain 2 ($V_{CM} = \pm 1$ V, $f \leq 100$ kHz)		50	—	—	50	—	—	
Supply Voltage Rejection Ratio	PSRR							dB
Gain 2 ($\Delta V_S = \pm 0.5$ V)		50	—	—	50	—	—	
Output Offset Voltage	V_{OO}							V
Gain 1		—	—	1.5	—	—	1.5	
Gain 2 and Gain 3		—	—	1.2	—	—	1.5	
Output Voltage Swing (Gain 2)	V_O	2.5	—	—	2.5	—	—	V _{p-p}
Output Sink Current (Gain 2)	I_O	2.2	—	—	2.5	—	—	mA
Power Supply Current (Gain 2)	I_D	—	—	27	—	—	27	mA

* $T_{low} = 0^\circ\text{C}$ for MC1733C, -55°C for MC1733

$T_{high} = +70^\circ\text{C}$ for MC1733C, $+125^\circ\text{C}$ for MC1733.

NOTES

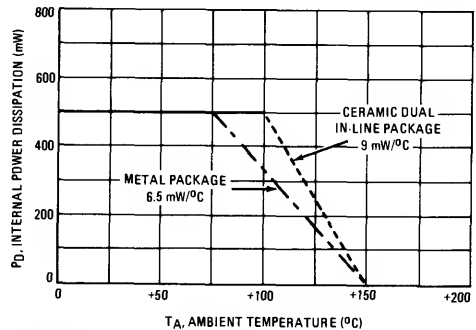
Note 1: Derate metal package at 6.5 mW/ $^\circ\text{C}$ for operation at ambient temperatures above 75°C and dual in-line package at 9 mW/ $^\circ\text{C}$ for operation at ambient temperatures above 100°C (see Figure 4). If operation at high ambient temperatures is required (MC1733) a heatsink may be necessary to limit maximum junction temperature to 150°C . Thermal resistance, junction-to-case, for the metal package is 69.4 $^\circ\text{C}$ per Watt.

Note 2: Gain Select pins G_{1A} and G_{1B} connected together.

Note 3: Gain Select pins G_{2A} and G_{2B} connected together.

Note 4: All Gain Select pins open.

FIGURE 4 – MAXIMUM ALLOWABLE POWER DISSIPATION



TYPICAL CHARACTERISTICS

($V_{CC} = +6.0$ Vdc, $V_{EE} = -6.0$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 5 – SUPPLY CURRENT versus TEMPERATURE

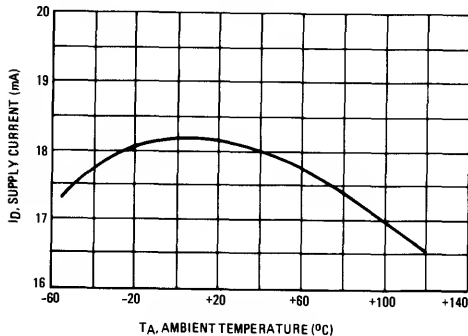
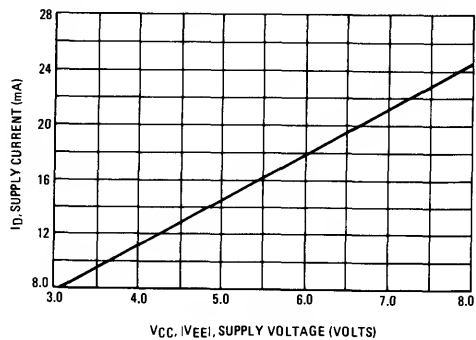


FIGURE 6 – SUPPLY CURRENT versus SUPPLY VOLTAGE



MC1733, MC1733C

TYPICAL CHARACTERISTICS (continued)

($V_{CC} = +6.0$ Vdc, $V_{EE} = -6.0$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 7 – GAIN versus TEMPERATURE

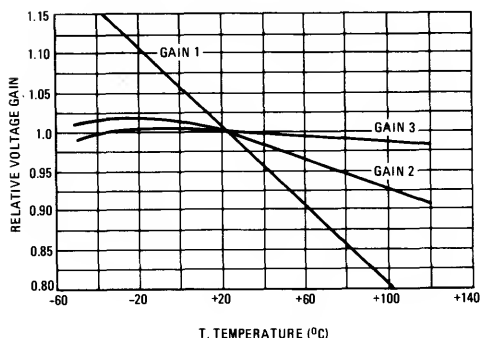


FIGURE 8 – GAIN versus FREQUENCY

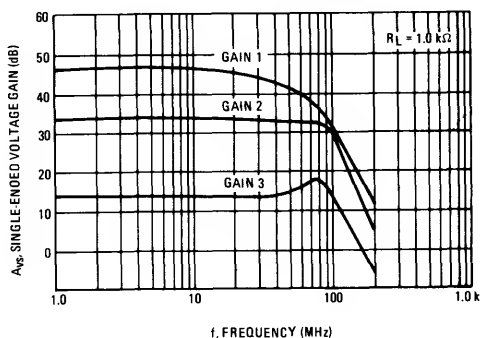


FIGURE 9 – GAIN versus SUPPLY VOLTAGE

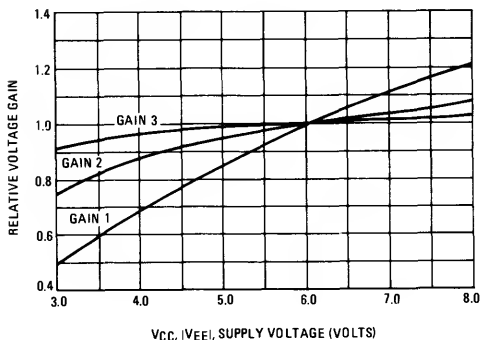


FIGURE 10 – GAIN versus R_{ADJ}

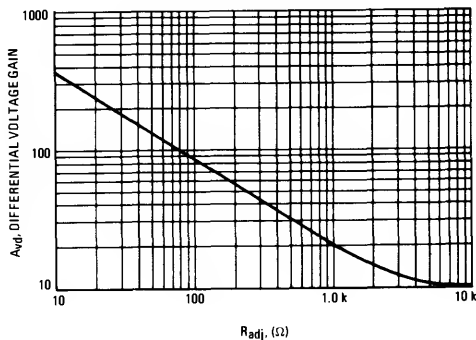


FIGURE 11 – GAIN versus FREQUENCY and SUPPLY VOLTAGE

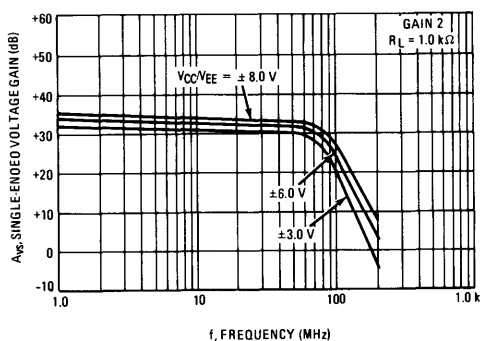
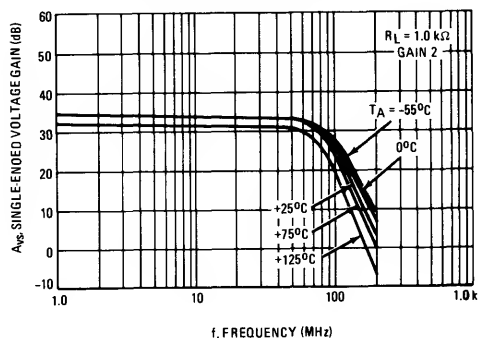


FIGURE 12 – GAIN versus FREQUENCY and TEMPERATURE



MC1733, MC1733C

TYPICAL CHARACTERISTICS (continued)

($V_{CC} = +6.0$ Vdc, $V_{EE} = -6.0$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 13 – PULSE RESPONSE versus GAIN

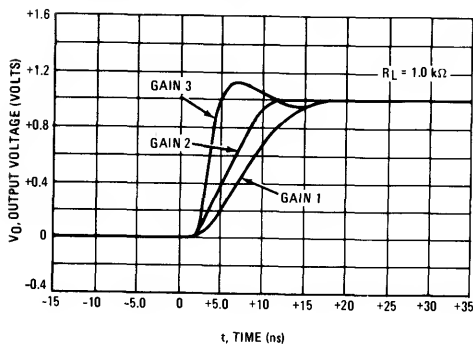


FIGURE 14 – PULSE RESPONSE versus SUPPLY VOLTAGE

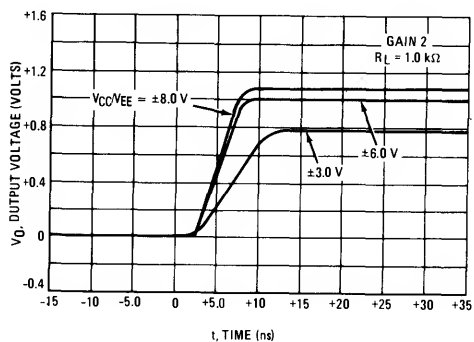


FIGURE 15 – PULSE RESPONSE versus TEMPERATURE

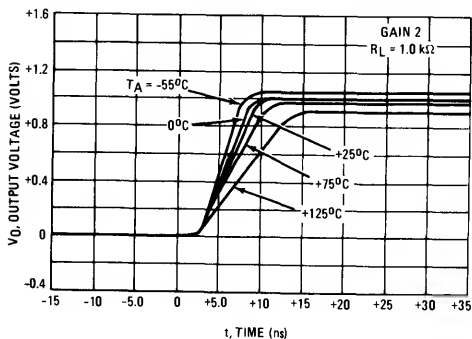


FIGURE 16 – DIFFERENTIAL OVERDRIVE RECOVERY TIME

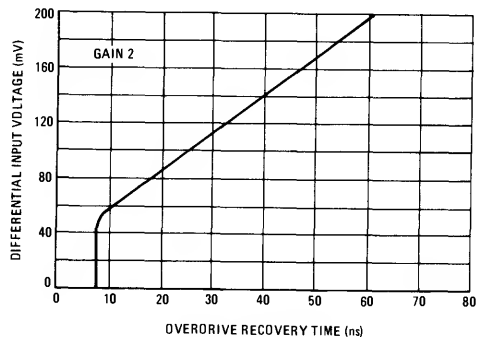


FIGURE 17 – PHASE SHIFT versus FREQUENCY

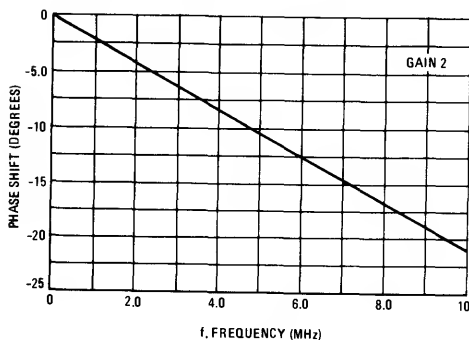
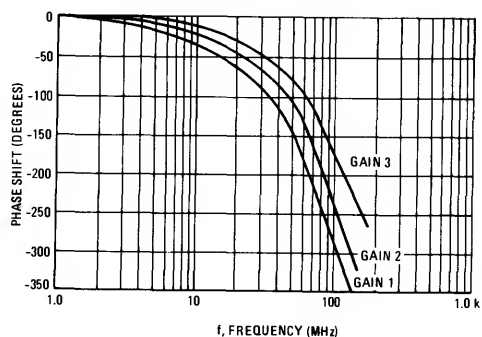


FIGURE 18 – PHASE SHIFT versus FREQUENCY



MC1733, MC1733C

TYPICAL CHARACTERISTICS (Continued)

($V_{CC} = +6.0$ Vdc, $V_{EE} = -6.0$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 19 – INPUT RESISTANCE versus TEMPERATURE

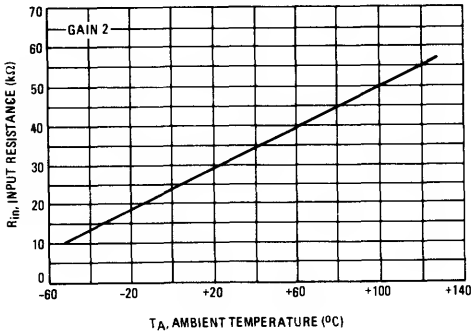


FIGURE 20 – INPUT NOISE VOLTAGE

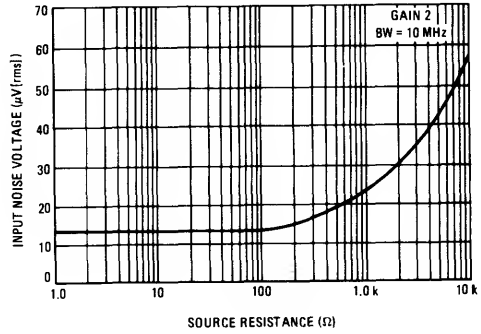


FIGURE 21 – OUTPUT VOLTAGE SWING and SINK CURRENT versus SUPPLY VOLTAGE

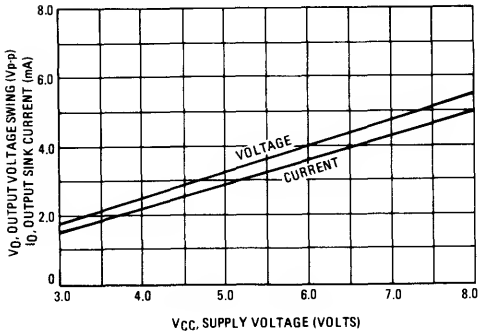


FIGURE 22 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

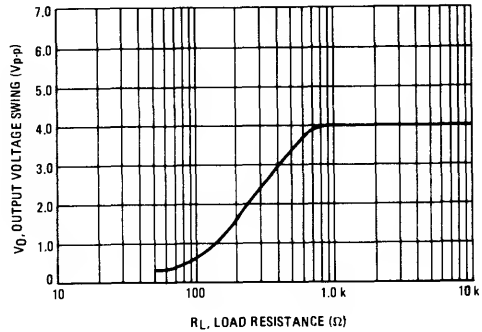


FIGURE 23 – OUTPUT VOLTAGE SWING versus FREQUENCY

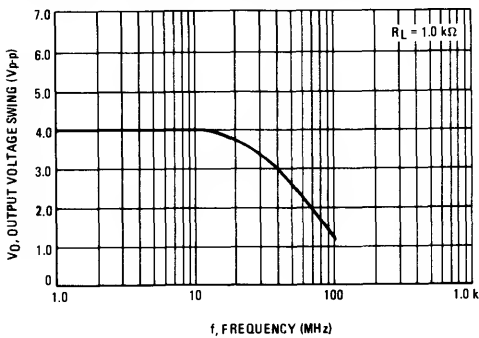
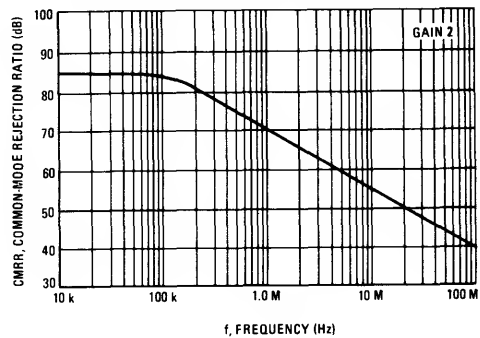


FIGURE 24 – COMMON-MODE REJECTION RATIO



APPLICATIONS INFORMATION

FIGURE 25 — VOLTAGE CONTROLLED OSCILLATOR

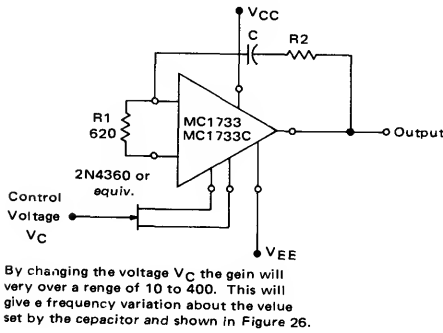
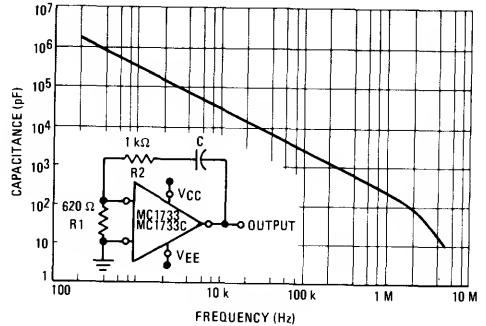


FIGURE 26 — OSCILLATOR FREQUENCY FOR VARIOUS CAPACITOR VALUES



TAPE, DRUM OR DISC MEMORY READ AMPLIFIERS

The first of several methods to be discussed is shown in Figure 27. This block diagram describes a simple Read circuit with no threshold circuitry. Each block represents a basic function that must be performed by the Read circuit. The first block, referred to as "amplification", increases the level of the signal available from the Read head to a level adequate to drive the peak detector. Obviously, these signal levels will vary depending on factors such as tape speed, whether the system used is disc or tape, and the type of head and the circuitry used. For a representative tape system, levels of 7 to 25 mV for the signal from the Read head and 2 V for the signal to the peak detector are typical. These signal levels are "peak-to-peak" unless otherwise specified. On the basis of the signal levels mentioned above, the overall amplification required is 38 to 49 dB.

How the overall gain requirement is implemented will depend somewhat on the system used. For instance, a tape cassette system with variable tape speed may utilize a first stage for gain and a second stage primarily for gain control. Thus, a typical circuit would utilize 35 dB in the first stage and 10 to 15 dB in the second stage.

Devices suitable for use as amplifiers fall into one of two categories, operational amplifiers or wideband video amplifiers. Lower speed equipment with low transfer rates commonly uses low cost operational amplifiers. Examples of these are the MC1741, MC1458, MC1709, and MLM301. Equipment requiring higher transfer rates, such as disc systems normally use wideband amplifiers such as the MC1733. The actual cross-over point where wideband amplifiers are used exclusively varies with equipment de-

sign. For purposes of comparison, the MLM301 has slightly less than a 40 dB open-loop gain at 100 kHz; the MC1741, a compensated op-amp, has approximately 20 dB open loop gain at 100 kHz; the MC1733 has approximately 33 dB of gain out to 100 MHz (depending on gain option and loading).

There are a number of ways to implement the peak detector function. However, the simplest and most widely used method is a passive differentiator that generates "zero-crossings" for each of the data peaks in the Read signal.

The actual circuitry used to differentiate the Read signal varies from a differential LC type in disc systems to a simple RC type in reel and cassette systems. Either type, of course, attenuates the signal by an amount depending on the circuit used and system specifications. A good approximation of attenuation using the RC type is 20 dB. Thus, the 2 V signal going into the differentiator is reduced to 200 mV.

The next block in Figure 27 to be discussed is the zero-crossing detector. In most cases detection of the zero-crossings is combined with the limiter. These functions serve to generate a TTL compatible pulse waveform with "edges" corresponding to zero-crossings. For low transfer rates, the circuit often used consists of an operational amplifier with series or shunt limiting. For higher transfer rates (greater than 100K B/S) comparators are used.

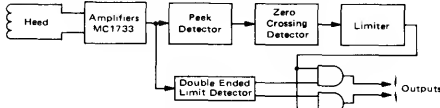
The method described above is often modified to include threshold sensing. In Figure 28, the function called "double-ended, limit-detector" enables the output NAND gate when either the negative or positive data peaks of the Read signal exceed a predetermined threshold. This function can be implemented in either of two ways. One method first rectifies the signal before it is applied to a comparator with a set threshold. The other method utilizes two comparators, one comparator for positive-going peaks and the other for negative-going peaks. These comparator outputs are then combined in the output logic gates.

FIGURE 27 — TYPICAL READ CIRCUIT (METHOD 1)



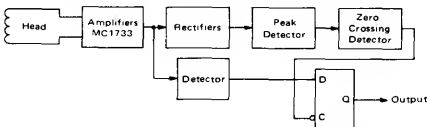
APPLICATIONS INFORMATION (continued)

FIGURE 28 — READ CIRCUIT (METHOD 2)



Another common technique is shown in Figure 29. The branch labeled rectifiers, peak detector, etc., provides a clock transition of the D flip-flop that corresponds to the peak of both the positive and negative-going data peaks. This branch may include threshold circuitry prior to the peak detector. The detector in the lower path detects whether the signal peaks are positive or negative and feeds this data to the flip-flop. This detector can be implemented using a comparator with pre-set threshold.

FIGURE 29 — READ CIRCUIT (METHOD 3)



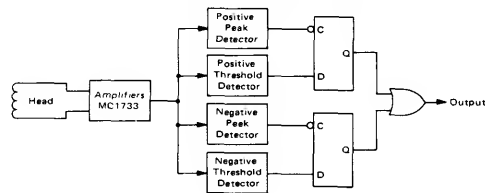
The technique shown in Figure 30 uses separate circuits with threshold provisions for both negative and positive peaks. The peak detectors and threshold detectors

may be implemented with two comparators and two passive differentiators.

Each of the methods shown offer certain intrinsic advantages or disadvantages. The overall decision as to which method to use however often involves other important considerations. These could include cost and system requirements or circuitry other than simply the Read circuitry. For instance, if cost is the predominate overall factor, then approach one may be the only feasible alternative.

Method four was included as a design example because it illustrates several unique advantages. First, it uses threshold sensing to reduce noise peak errors. Second, it may be implemented using only integrated circuits. Third, it offers separate, direct threshold sensing for both positive and negative peaks.

FIGURE 30 — READ CIRCUIT (Method 4)



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

2

INTERNALLY COMPENSATED, HIGH PERFORMANCE OPERATIONAL AMPLIFIERS

... designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- No Frequency Compensation Required
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up

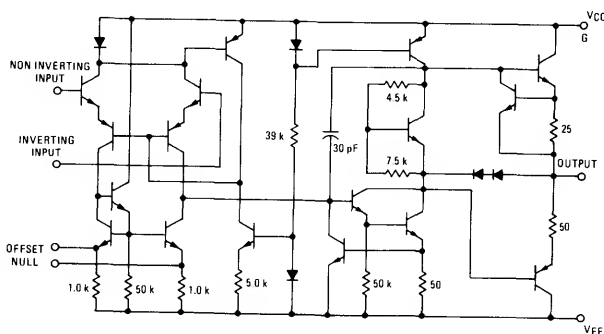
MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	MC1741C	MC1741	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 -18	+22 -22	Vdc Vdc
Input Differential Voltage	V_{ID}	± 30		Volts
Input Common Mode Voltage (Note 1)	V_{ICM}	± 15		Volts
Output Short Circuit Duration (Note 2)	t_S	Continuous		
Operating Ambient Temperature Range	T_A	0 to +70	-55 to +125	$^\circ\text{C}$
Storage Temperature Range Metal and Ceramic Packages Plastic Packages	T_{stg}	-65 to +150 -55 to +125		$^\circ\text{C}$

NOTES:

1. For supply voltages less than +15 V, the absolute maximum input voltage is equal to the supply voltage.
2. Supply voltage equal to or less than 15 V.

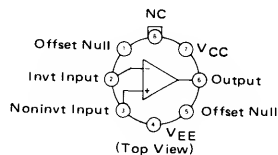
EQUIVALENT CIRCUIT SCHEMATIC



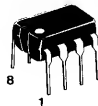
MC1741 MC1741C

OPERATIONAL AMPLIFIER

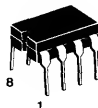
SILICON MONOLITHIC INTEGRATED CIRCUIT



G SUFFIX
METAL PACKAGE
CASE 601



P1 SUFFIX
PLASTIC PACKAGE
CASE 626

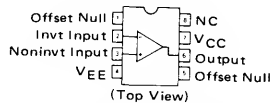


U SUFFIX
CERAMIC PACKAGE
CASE 693



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

PIN CONNECTIONS



ORDERING INFORMATION

Device	Alternate	Temperature Range	Package
MC1741CD	—	0°C to +70°C	SO-8
MC1741CG	LM741CH, $\mu\text{A}741\text{HC}$		Metal Can
MC1741CP1	LM741CN, $\mu\text{A}741\text{TC}$	-55°C to +125°C	Plastic DIP
MC1741CU	—		Ceramic DIP
MC1741G	—	-55°C to +125°C	Metal Can
MC1741U	—		Ceramic DIP

MC1741, MC1741C

ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = 25^\circ\text{C}$ unless otherwise noted).

Characteristic	Symbol	MC1741			MC1741C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10\text{ k}$)	V_{IO}	—	1.0	5.0	—	2.0	6.0	mV
Input Offset Current	I_{IO}	—	20	200	—	20	200	nA
Input Bias Current	I_{IB}	—	80	500	—	80	500	nA
Input Resistance	r_i	0.3	2.0	—	0.3	2.0	—	M Ω
Input Capacitance	C_i	—	1.4	—	—	1.4	—	pF
Offset Voltage Adjustment Range	V_{IOR}	—	± 15	—	—	± 15	—	mV
Common Mode Input Voltage Range	V_{ICR}	± 12	± 13	—	± 12	± 13	—	V
Large Signal Voltage Gain ($V_O = \pm 10\text{ V}$, $R_L \geq 2.0\text{ k}$)	A_v	50	200	—	20	200	—	V/mV
Output Resistance	r_o	—	75	—	—	75	—	Ω
Common Mode Rejection Ratio ($R_S \leq 10\text{ k}$)	CMRR	70	90	—	70	90	—	dB
Supply Voltage Rejection Ratio ($R_S \leq 10\text{ k}$)	PSRR	—	30	150	—	30	150	$\mu\text{V/V}$
Output Voltage Swing ($R_L \geq 10\text{ k}$) ($R_L \geq 2\text{ k}$)	V_O	± 12 ± 10	± 14 ± 13	—	± 12 ± 10	± 14 ± 13	—	V
Output Short-Circuit Current	I_{os}	—	20	—	—	20	—	mA
Supply Current	I_D	—	1.7	2.8	—	1.7	2.8	mA
Power Consumption	P_C	—	50	85	—	50	85	mW
Transient Response (Unity Gain – Non-Inverting) ($V_i = 20\text{ mV}$, $R_L \geq 2\text{ k}$, $C_L \leq 100\text{ pF}$) Rise Time ($V_i = 20\text{ mV}$, $R_L \geq 2\text{ k}$, $C_L \leq 100\text{ pF}$) Overshoot ($V_i = 10\text{ V}$, $R_L \geq 2\text{ k}$, $C_L \leq 100\text{ pF}$) Slew Rate	t_{TLH} os SR	— — —	0.3 15 0.5	— — —	— — —	0.3 15 0.5	— — —	μs % V/ μs

ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = T_{low}$ to T_{high} unless otherwise noted).

Characteristic	Symbol	MC1741			MC1741C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10\text{ k}\Omega$)	V_{IO}	—	1.0	6.0	—	—	7.5	mV
Input Offset Current ($T_A = 125^\circ\text{C}$) ($T_A = -55^\circ\text{C}$) ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$)	I_{IO}	— — —	7.0 85 —	200 500 —	— — —	— — —	— — 300	nA
Input Bias Current ($T_A = 125^\circ\text{C}$) ($T_A = -55^\circ\text{C}$) ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$)	I_{IB}	— — —	30 300 —	500 1500 —	— — —	— — —	— — 800	nA
Common Mode Input Voltage Range	V_{ICR}	± 12	± 13	—	—	—	—	V
Common Mode Rejection Ratio ($R_S \leq 10\text{ k}$)	CMRR	70	90	—	—	—	—	dB
Supply Voltage Rejection Ratio ($R_S \leq 10\text{ k}$)	PSRR	—	30	150	—	—	—	$\mu\text{V/V}$
Output Voltage Swing ($R_L \geq 10\text{ k}$) ($R_L \geq 2\text{ k}$)	V_O	± 12 ± 10	± 14 ± 13	— —	— ± 10	— ± 13	— —	V
Large Signal Voltage Gain ($R_L \geq 2\text{ k}$, $V_{out} = \pm 10\text{ V}$)	A_v	25	—	—	15	—	—	V/mV
Supply Currents ($T_A = 125^\circ\text{C}$) ($T_A = -55^\circ\text{C}$)	I_D	— —	1.5 2.0	2.5 3.3	— —	— —	— —	mA
Power Consumption ($T_A = +125^\circ\text{C}$) ($T_A = -55^\circ\text{C}$)	P_C	— —	45 60	75 100	— —	— —	— —	mW

* $T_{high} = 125^\circ\text{C}$ for MC1741 and 70°C for MC1741C

$T_{low} = -55^\circ\text{C}$ for MC1741 and 0°C for MC1741C

MC1741, MC1741C

2

FIGURE 1 – BURST NOISE versus SOURCE RESISTANCE

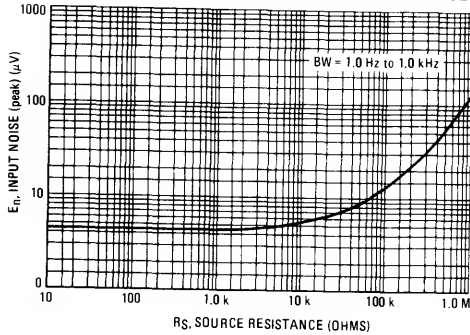


FIGURE 2 – RMS NOISE versus SOURCE RESISTANCE

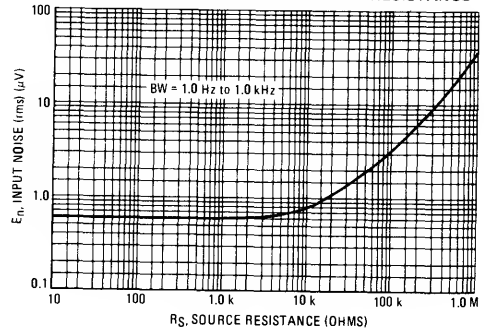


FIGURE 3 – OUTPUT NOISE versus SOURCE RESISTANCE

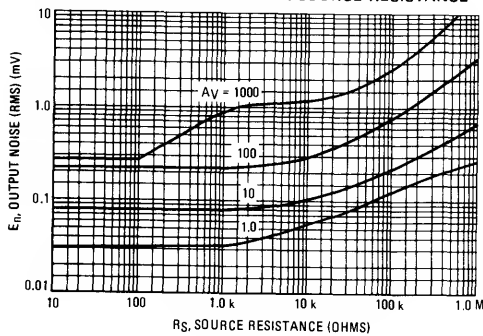


FIGURE 4 – SPECTRAL NOISE DENSITY

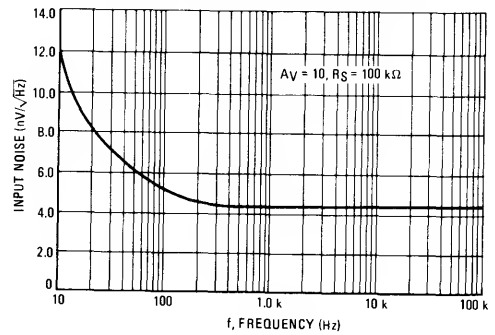
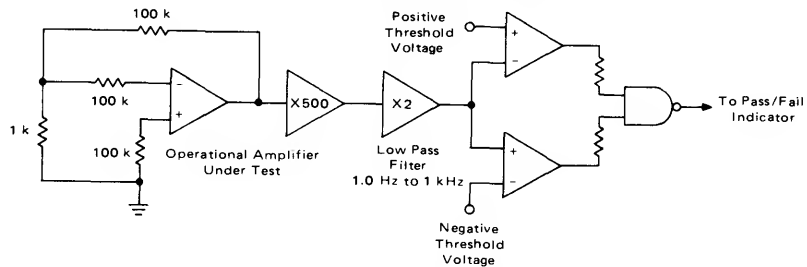


FIGURE 5 – BURST NOISE TEST CIRCUIT



Unlike conventional peak reading or RMS meters, this system was especially designed to provide the quick response time essential to burst (popcorn) noise testing.

The test time employed is 10 seconds and the 20 μ V peak limit refers to the operational amplifier input thus eliminating errors in the closed-loop gain factor of the operational amplifier under test.

MC1741, MC1741C

TYPICAL CHARACTERISTICS

($V_{CC} = +15$ Vdc, $V_{EE} = -15$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted)

**FIGURE 6 – POWER BANDWIDTH
(LARGE SIGNAL SWING versus FREQUENCY)**

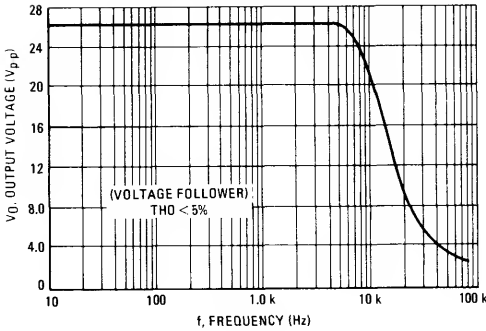
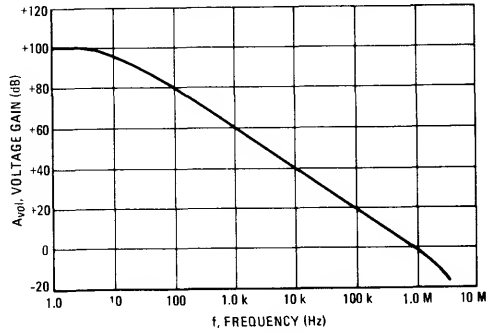
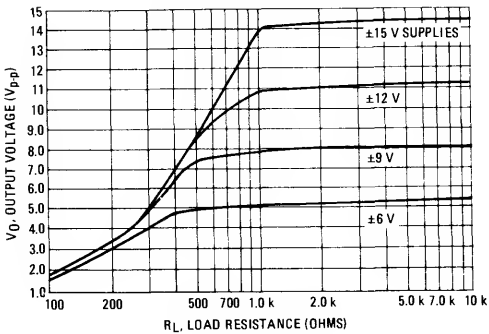


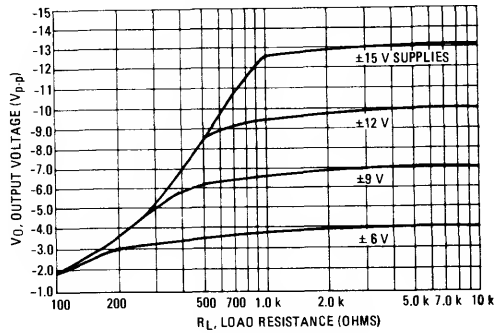
FIGURE 7 – OPEN LOOP FREQUENCY RESPONSE



**FIGURE 8 – POSITIVE OUTPUT VOLTAGE SWING
versus LOAD RESISTANCE**



**FIGURE 9 – NEGATIVE OUTPUT VOLTAGE SWING
versus LOAD RESISTANCE**



**FIGURE 10 – OUTPUT VOLTAGE SWING versus
LOAD RESISTANCE (Single Supply Operation)**

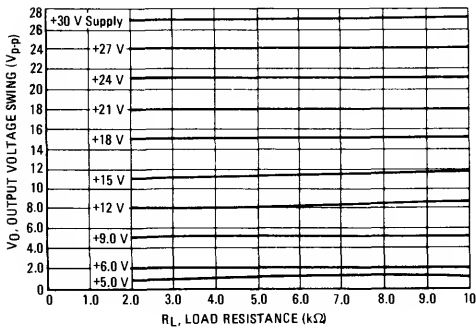


FIGURE 11 – SINGLE SUPPLY INVERTING AMPLIFIER

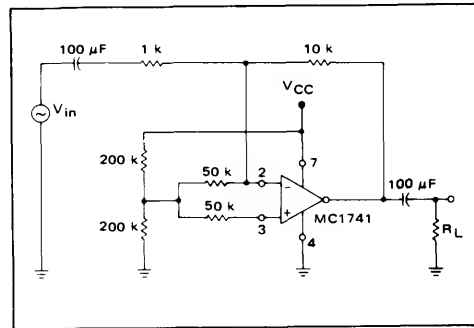


FIGURE 12 — NONINVERTING PULSE RESPONSE

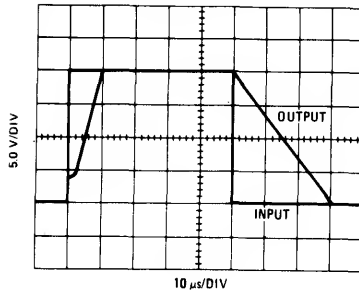


FIGURE 13 — TRANSIENT RESPONSE TEST CIRCUIT

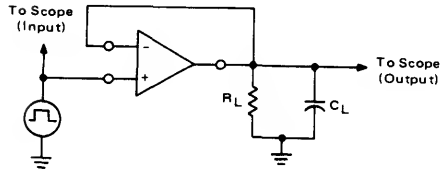
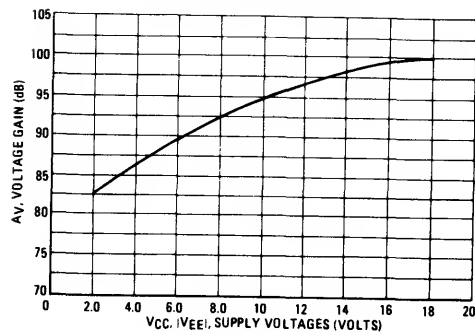


FIGURE 14 — OPEN LOOP VOLTAGE GAIN
versus SUPPLY VOLTAGE

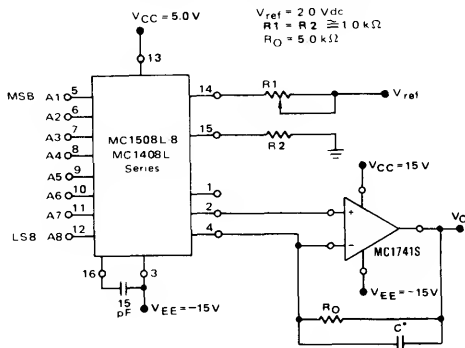


HIGH SLEW RATE, INTERNALLY COMPENSATED OPERATIONAL AMPLIFIER

The MC1741S/MC1741SC is functionally equivalent, pin compatible, and possesses the same ease of use as the popular MC1741 circuit, yet offers 20 times higher slew rate and power bandwidth. This device is ideally suited for D-to-A converters due to its fast settling time and high slew rate.

- High Slew Rate — 10 V/ μ s Guaranteed Minimum (for unity gain only)
- No Frequency Compensation Required
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low Power Consumption
- No Latch-Up

TYPICAL APPLICATION OF OUTPUT CURRENT TO VOLTAGE TRANSFORMATION FOR A D-TO-A CONVERTER



Pins not shown are not connected.

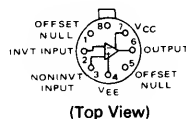
Settling time to within 1/2 LSB (± 19.5 mV) is approximately 4.0 μ s from the time that all bits are switched.

*The value of C may be selected to minimize overshoot and ringing ($C \approx 150$ pF).

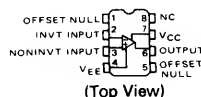
MC1741S MC1741SC

OPERATIONAL AMPLIFIER

SILICON MONOLITHIC
 INTEGRATED CIRCUIT



G SUFFIX
 METAL PACKAGE
 CASE 601



P1 SUFFIX
 PLASTIC PACKAGE
 CASE 626

D SUFFIX
 PLASTIC PACKAGE
 CASE 751
 (SO-8)

ORDERING INFORMATION

Device	Temperature Range	Package
MC1741SG	-55°C to +125°C	Metal Can
MC1741SCD		SO-8
MC1741SCG	0°C to +70°C	Metal Can
MC1741SCP1		Plastic DIP

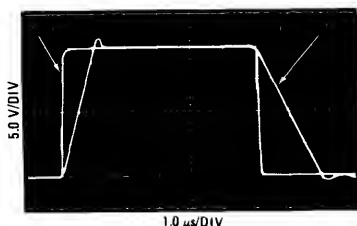
Theoretical V_0

$$V_0 = \frac{V_{ref}}{R_1} (R_0) \left[\frac{A_1}{2} + \frac{A_2}{4} + \frac{A_3}{8} + \frac{A_4}{16} + \frac{A_5}{32} + \frac{A_6}{64} + \frac{A_7}{128} + \frac{A_8}{256} \right]$$

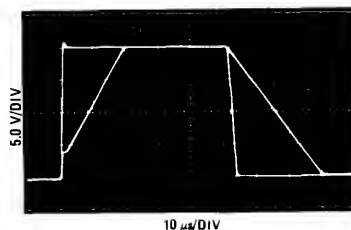
Adjust V_{ref} , R_1 or R_0 so that V_0 with all digital inputs at high level is equal to 9.961 volts.

$$V_0 = \frac{2V}{1k} (5k) \left[\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256} \right] = 10V \left[\frac{255}{256} \right] = 9.961V$$

MC1741S LARGE-SIGNAL TRANSIENT RESPONSE

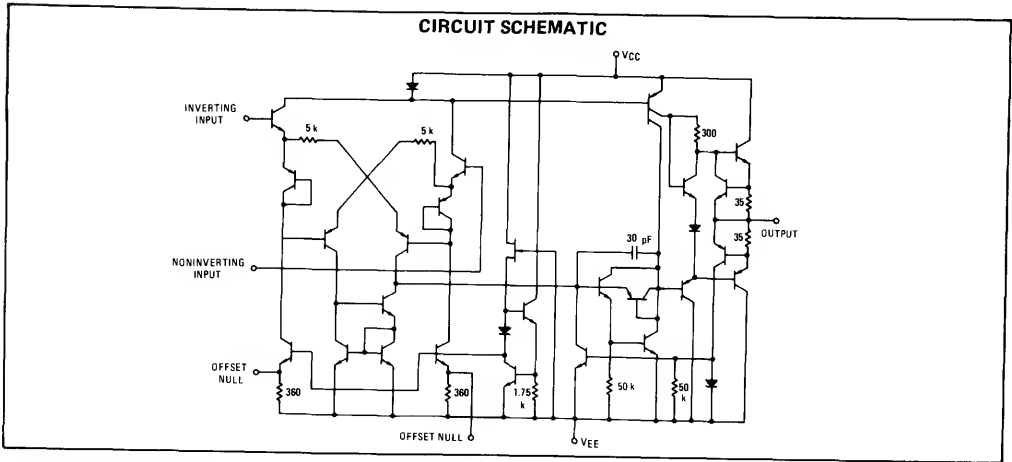


STANDARD MC1741 versus MC1741S RESPONSE COMPARISON



MC1741S, MC1741SC

2

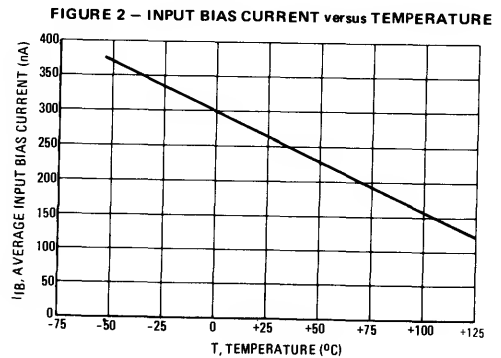
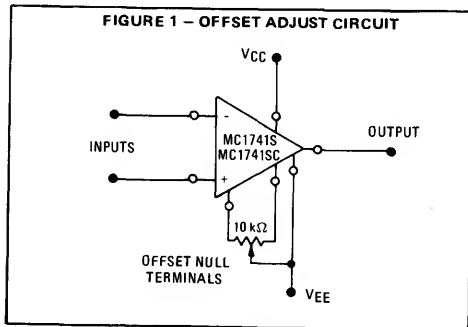


MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted.)

Rating	Symbol	Value		Unit
		MC1741SC	MC1741S	
Power Supply Voltage	V_{CC} V_{EE}	+18 -18	+22 -22	Vdc
Differential Input Signal Voltage	V_{ID}	± 30		Volts
Common-Mode Input Voltage Swing (See Note 1)	V_{ICR}	± 15		Volts
Output Short-Circuit Duration (See Note 2)	t_s	Continuous		
Power Dissipation (Package Limitation)	P_D			
Metal Package		680		mW
Derate above $T_A = +25^\circ\text{C}$		4.6		mW/ $^\circ\text{C}$
Plastic Dual In-Line Package		625		mW
Derate above $T_A = +25^\circ\text{C}$		5.0		mW/ $^\circ\text{C}$
Operating Ambient Temperature Range	T_A	0 to +75	-55 to +125	$^\circ\text{C}$
Storage Temperature Range	T_{stg}			$^\circ\text{C}$
Metal Package		-65 to +150		
Plastic Package		-55 to +125		

Note 1. For supply voltages less than ± 15 Vdc, the absolute maximum input voltage is equal to the supply voltage.

Note 2. Supply voltage equal to or less than 15 Vdc.



MC1741S, MC1741SC

ELECTRICAL CHARACTERISTICS ($V_{CC} = +15$ Vdc, $V_{EE} = -15$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	MC1741S			MC1741SC			Unit
		Min	Typ	Max	Min	Typ	Max	
Power Bandwidth (See Figure 3) $A_V = 1$, $R_L = 2.0$ k Ω , THD = 5%, $V_O = 20$ V(p-p)	BW _p	150	200	—	150	200	—	kHz
Large-Signal Transient Response								
Slew Rate (Figures 10 and 11) V(–) to V(+) V(+) to V(–)	SR	10 10	20 12	— —	10 10	20 12	— —	V/ μ s
Settling Time (Figures 10 and 11) (to within 0.1%)	t_{settlg}	—	3.0	—	—	3.0	—	μ s
Small-Signal Transient Response (Gain = 1, $E_{in} = 20$ mV, see Figures 7 and 8)								
Rise Time	t_{TLH}	—	0.25	—	—	0.25	—	μ s
Fall Time	t_{THL}	—	0.25	—	—	0.25	—	μ s
Propagation Delay Time	t_{PLH}, t_{PHL}	—	0.25	—	—	0.25	—	μ s
Overshoot	OS	—	20	—	—	20	—	%
Short-Circuit Output Currents	I_{OS}	± 10	—	± 35	± 10	—	± 35	mA
Open-Loop Voltage Gain ($R_L = 2.0$ k Ω) (See Figure 4) $V_O = \pm 10$ V, $T_A = +25^\circ\text{C}$ $V_O = \pm 10$ V, $T_A = T_{low}^*$ to T_{high}^*	A_{vol}	50,000 25,000	200,000 —	— —	20,000 15,000	100,000 —	— —	—
Output Impedance ($f = 20$ Hz)	z_o	—	75	—	—	75	—	Ω
Input Impedance ($f = 20$ Hz)	z_i	0.3	1.0	—	0.3	1.0	—	M Ω
Output Voltage Swing $R_L = 10$ k Ω , $T_A = T_{low}$ to T_{high} (MC1741S only) $R_L = 2.0$ k Ω , $T_A = +25^\circ\text{C}$ $R_L = 2.0$ k Ω , $T_A = T_{low}$ to T_{high}	V_O	± 12 ± 10 ± 10	± 14 ± 13 —	— — —	± 12 ± 10 ± 10	± 14 ± 13 —	— — —	V_{pk}
Input Common-Mode Voltage Range $T_A = T_{low}$ to T_{high} (MC1741S)	V_{ICR}	± 12	± 13	—	± 12	± 13	—	V_{pk}
Common-Mode Rejection Ratio ($f = 20$ Hz) $T_A = T_{low}$ to T_{high} (MC1741S)	CMRR	70	90	—	70	90	—	dB
Input Bias Current (See Figure 2) $T_A = +25^\circ\text{C}$ and T_{high} $T_A = T_{low}$	I_{IB}	— —	200 500	500 1500	— —	200 —	500 800	nA
Input Offset Current $T_A = +25^\circ\text{C}$ and T_{high} $T_A = T_{low}$	$ I_{IO} $	— —	30 —	200 500	— —	30 —	200 300	nA
Input Offset Voltage ($R_S = \leq 10$ k Ω) $T_A = +25^\circ\text{C}$ $T_A = T_{low}$ to T_{high}	$ V_{IO} $	— —	1.0 —	5.0 6.0	— —	2.0 —	6.0 7.5	mV
DC Power Consumption (See Figure 9) (Power Supply = ± 15 V, $V_O = 0$) $T_A = T_{low}$ to T_{high}	P_C	—	50	85	—	50	85	mW
Positive Voltage Supply Sensitivity (V_{EE} constant) $T_A = T_{low}$ to T_{high} on MC1741S	PSS+	—	2.0	100	—	2.0	150	μ V/V
Negative Voltage Supply Sensitivity (V_{CC} constant)	PSS–	—	10	150	—	10	150	μ V/V

* $T_{low} = 0$ for MC1741SC
= -55°C for MC1741S

$T_{high} = +70^\circ\text{C}$ for MC1741SC
= $+125^\circ\text{C}$ for MC1741S

MC1741S, MC1741SC

TYPICAL CHARACTERISTICS

($V_{CC} = +15\text{ Vdc}$, $V_{EE} = -15\text{ Vdc}$, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 3 – POWER BANDWIDTH – NONDISTORTED OUTPUT VOLTAGE versus FREQUENCY

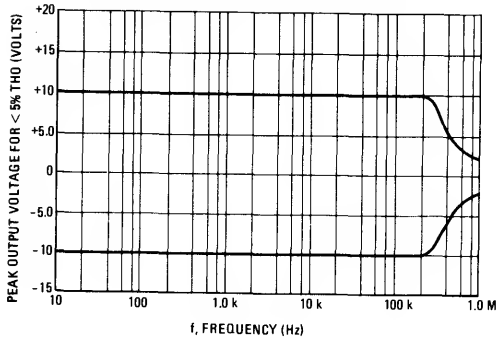


FIGURE 4 – OPEN-LOOP FREQUENCY RESPONSE

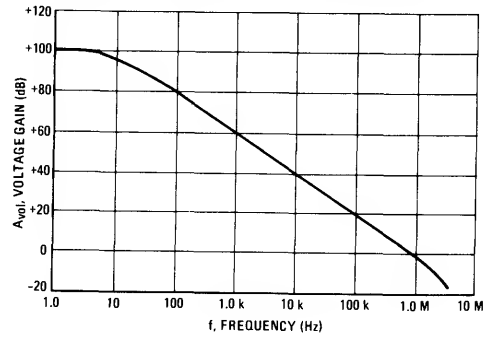


FIGURE 5 – NOISE versus FREQUENCY

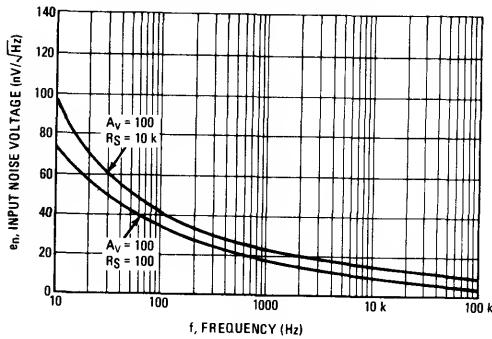


FIGURE 6 – OUTPUT NOISE versus SOURCE RESISTANCE

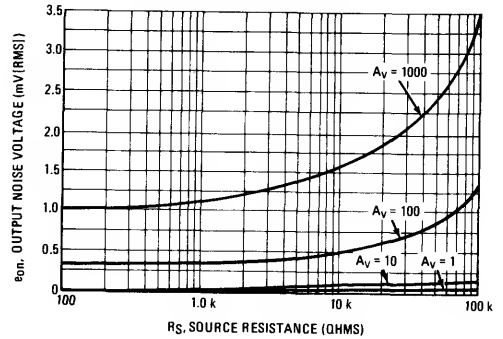


FIGURE 7 – SMALL-SIGNAL TRANSIENT RESPONSE DEFINITIONS

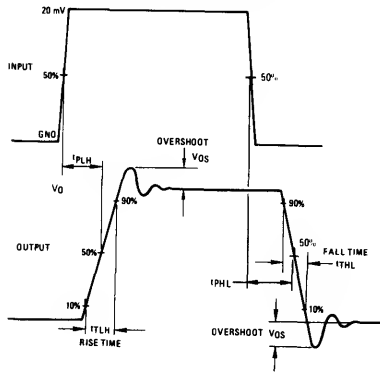
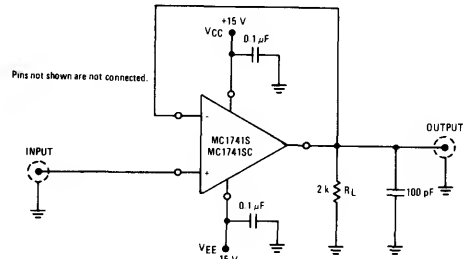


FIGURE 8 – SMALL-SIGNAL TRANSIENT RESPONSE TEST CIRCUIT



2

FIGURE 12 – WAVEFORM AT FALSE SUMMING NODE

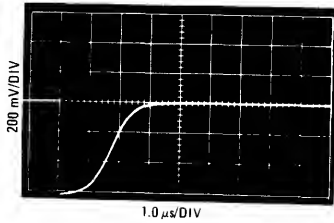
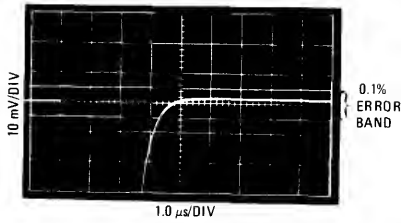
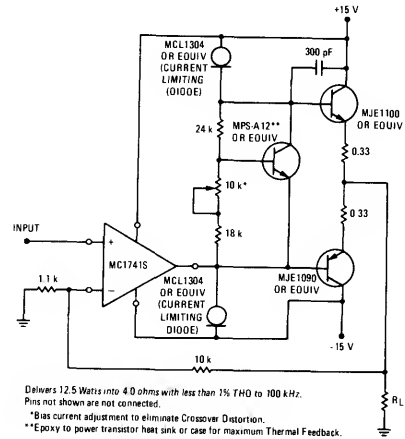


FIGURE 13 – EXPANDED WAVEFORM AT FALSE SUMMING NODE



TYPICAL APPLICATION

FIGURE 14 – 12.5-WATT WIDEBAND POWER AMPLIFIER



MC1747 MC1747C

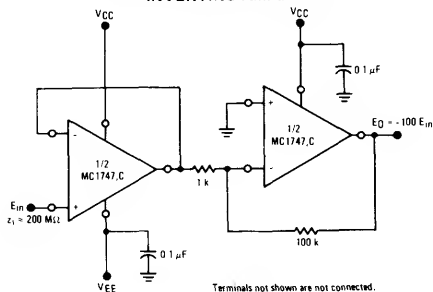
2

(DUAL MC1741)
**INTERNALLY COMPENSATED,
 HIGH PERFORMANCE
 OPERATIONAL AMPLIFIER**

... designed for use as summing amplifiers, integrators, or amplifiers with operating characteristics as a function of the external feedback components. The MC1747L and MC1747CL are functionally and electrically equivalent to the μ A747 and μ A747C respectively.

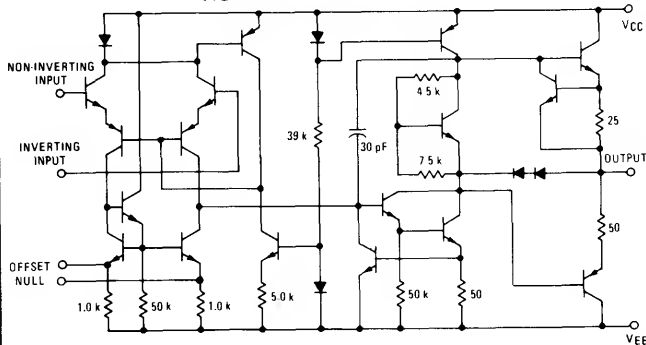
- No Frequency Compensation Required
- Short-Circuit Protection
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up
- Offset Voltage Null Capability

**FIGURE 1 — HIGH-IMPEDANCE, HIGH-GAIN
 INVERTING AMPLIFIER**



Terminals not shown are not connected.

FIGURE 2 — CIRCUIT SCHEMATIC

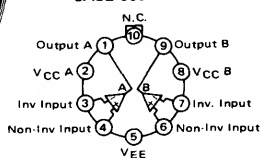


(DUAL MC1741)
**DUAL
 OPERATIONAL AMPLIFIER**

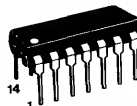
**SILICON MONOLITHIC
 INTEGRATED CIRCUIT**



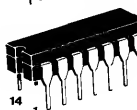
**G SUFFIX
 METAL PACKAGE
 CASE 603**



**D SUFFIX
 PLASTIC PACKAGE
 CASE 751A
 (SO-14)**

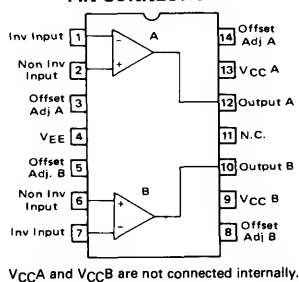


**P2 SUFFIX
 PLASTIC PACKAGE
 CASE 646**



**L SUFFIX
 CERAMIC PACKAGE
 CASE 632**

PIN CONNECTIONS



VCC A and VCC B are not connected internally.

ORDERING INFORMATION

Device	Temperature Range	Package
MC1747G MC1747L	-55°C to +125°C	Metal Can Ceramic DIP
MC1747CD MC1747CG MC1747CL MC1747CP2	0°C to +70°C	SO-14 Metal Can Ceramic DIP Plastic DIP

MC1747, MC1747C

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted.)

Rating	Symbol	MC1747	MC1747C	Unit
Power Supply Voltages	V_{CC}	+22	+18	Vdc
	V_{EE}	-22	-18	
Differential Input Signal Voltage ①	V_{ID}	± 30		Volts
Common-Mode Input Swing Voltage ②	V_{ICR}	± 15		Volts
Output Short-Circuit Duration	t_{OS}	Continuous		
Voltage (Measurement between Offset Null and V_{EE})		± 0.5		Volts
Operating Ambient Temperature Range	T_A	-55 to +125	0 to +70	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	$^\circ\text{C}$
Junction Temperature	T_J	175		$^\circ\text{C}$
Ceramic end Metal Package		150		
Plastic Package		150		

ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ Vdc}$, $V_{EE} = -15\text{ Vdc}$, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

Characteristics	Symbol	MC1747			MC1747C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Bias Current $T_A = +25^\circ\text{C}$ $T_A = T_{high}$ ③ $T_A = T_{low}$ ③	I_{IB}	—	80 30 300	500 500 1500	—	80 30 30	500 800 800	nAdc
Input Offset Current $T_A = +25^\circ\text{C}$ $T_A = T_{high}$ $T_A = T_{low}$	I_{IO}	—	20 7.0 85	200 200 500	—	20 7.0 7.0	200 300 300	nAdc
Input Offset Voltage ($R_S \leq 10\text{ k}\Omega$) $T_A = +25^\circ\text{C}$ $T_A = T_{low}$ to T_{high}	V_{IO}	—	1.0 1.0	5.0 6.0	—	1.0 1.0	6.0 7.5	mVdc
Offset Voltage Adjustment Range		—	± 15	—	—	± 15	—	mV
Differential Input Impedance (Open-loop, $f = 20\text{ Hz}$)								
Parallel Input Resistance	r_i	0.3	2.0	—	0.3	2.0	—	M Ω
Parallel Input Capacitance	C_i	—	1.4	—	—	1.4	—	pF
Common-Mode Input Voltage Swing $T_{low} \leq T_A \leq T_{high}$	V_{ICR}	± 12	± 13	—	± 12	± 13	—	Volts
Common-Mode Rejection Ratio ($R_S = 10\text{ k}\Omega$) $T_{low} \leq T_A \leq T_{high}$	CMRR	70	90	—	70	90	—	dB
Open-Loop Voltage Gain $T_A = +25^\circ\text{C}$ $T_A = T_{low}$ to T_{high} } ($V_O = \pm 10\text{ V}$, $R_L = 2.0\text{ k}\Omega$)	A_{vol}	50,000 25,000	200,000 —	— —	25,000 15,000	200,000 —	— —	Volts
Transient Response (Unity Gain) ($V_{in} = 20\text{ mV}$, $R_L = 2.0\text{ k}\Omega$, $C_L \leq 100\text{ pF}$)								
Rise Time	t_{PLH}	—	0.3 5.0	— —	— —	0.3 5.0	— —	μs %
Overshoot Percentage		—	—	—	—	—	—	
Slew Rate (Unity Gain)	SR	—	0.5	—	—	0.5	—	V/ μs
Output Impedance	z_o	—	75	—	—	75	—	ohms
Short-Circuit Output Current	I_{OS}	—	25	—	—	25	—	mAdc
Channel Separation		—	120	—	—	120	—	dB
Output Voltage Swing ($T_{low} \leq T_A \leq T_{high}$) $R_L = 10\text{ k}\Omega$ $R_L = 2.0\text{ k}\Omega$	V_{OR}	± 12 ± 10	± 14 ± 13	—	± 12 ± 10	± 14 ± 13	—	V _{pk}
Power Supply Sensitivity (T_{low} to T_{high}) $V_{EE} = \text{Constant}$, $R_S \leq 10\text{ k}\Omega$ $V_{CC} = \text{Constant}$, $R_S \leq 10\text{ k}\Omega$	PSS+ PSS-	— —	30 30	150 150	— —	30 30	150 150	$\mu\text{V/V}$
Power Supply Current (each amplifier) $T_A = +25^\circ\text{C}$ $T_A = T_{low}$ $T_A = T_{high}$	$I_{CC/EE}$	— — —	1.7 2.0 1.5	2.8 3.3 2.5	— — —	1.7 2.0 2.0	2.8 3.3 3.3	mAdc
DC Power Consumption (each amplifier) $T_A = +25^\circ\text{C}$ $T_A = T_{low}$ $T_A = T_{high}$	P_C	— — —	50 60 45	85 100 75	— — —	50 60 60	85 100 100	mW

① For supply voltages of less than $\pm 15\text{ V}$, the maximum differential input voltage is equal to $\pm (V_{CC} + |V_{EE}|)$.

② For supply voltages of less than $\pm 15\text{ V}$, the maximum input voltage is equal to the supply voltage ($+V_{CC}$, $-|V_{EE}|$).

③ T_{low} : 0°C for MC1747CL

— 55°C for MC1747L

T_{high} : $+70^\circ\text{C}$ for MC1747CL

+ 125°C for MC1747L

MC1747, MC1747C

FIGURE 3 – TYPICAL FREQUENCY-SHIFT KEYER TONE GENERATOR TEST CIRCUIT

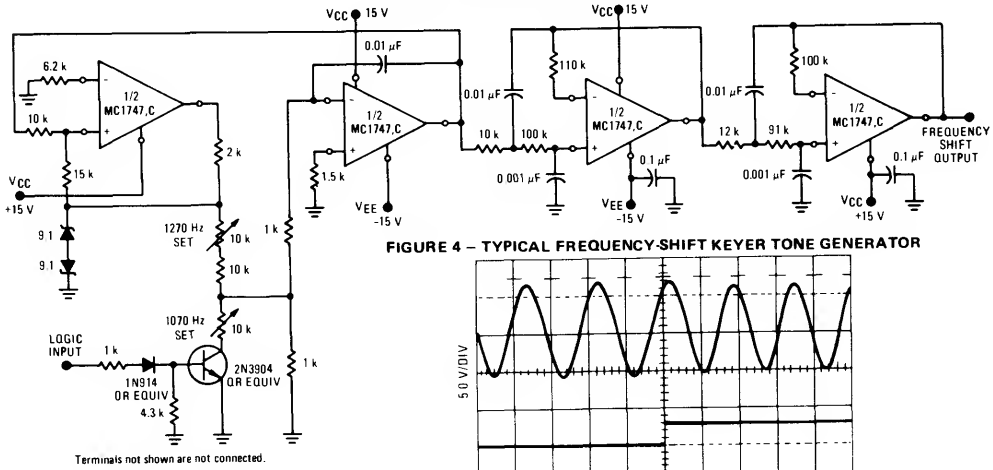
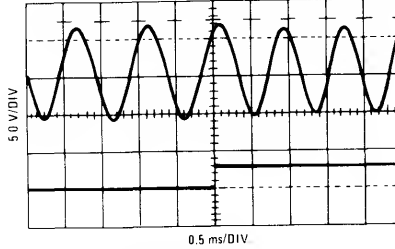


FIGURE 4 – TYPICAL FREQUENCY-SHIFT KEYER TONE GENERATOR



TYPICAL CHARACTERISTICS

($V_{CC} = +15$ Vdc, $V_{EE} = -15$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 5 – OPEN-LOOP VOLTAGE GAIN versus POWER-SUPPLY VOLTAGE

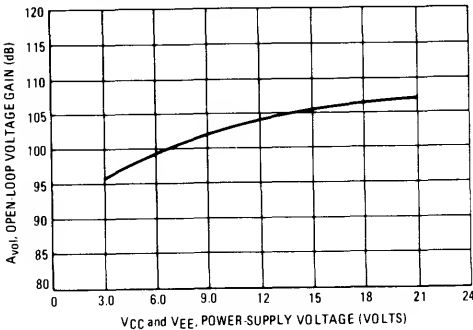


FIGURE 6 – OPEN-LOOP FREQUENCY RESPONSE

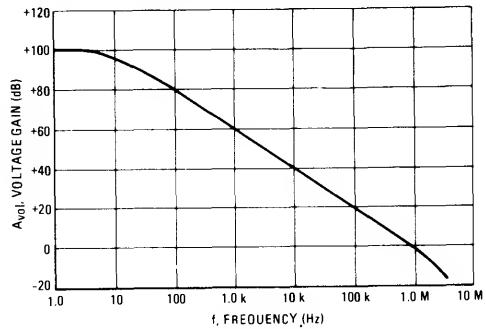


FIGURE 7 – POWER BANDWIDTH (LARGE SIGNAL SWING versus FREQUENCY)

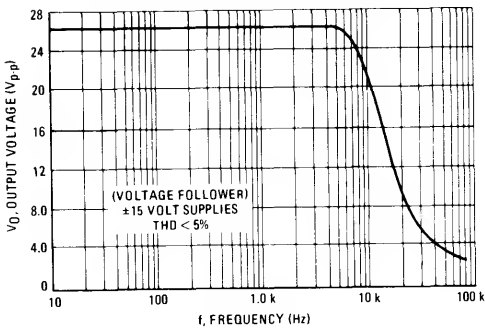
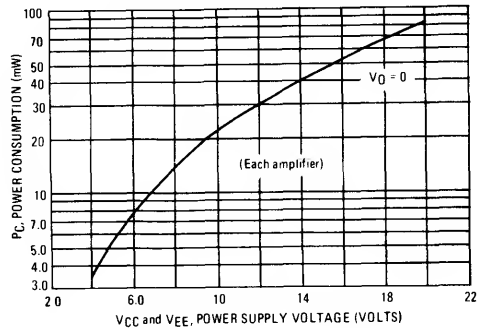


FIGURE 8 – POWER CONSUMPTION versus POWER SUPPLY VOLTAGE



TYPICAL CHARACTERISTICS (continued)

($V_{CC} = +15$ Vdc, $V_{EE} = -15$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 9 — OUTPUT VOLTAGE SWING
versus LOAD RESISTANCE

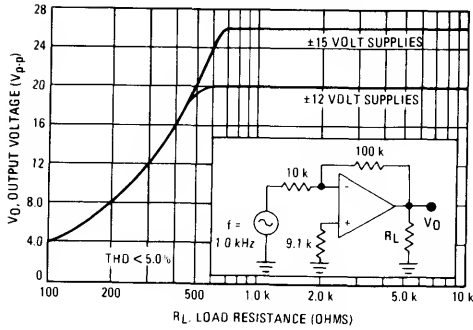
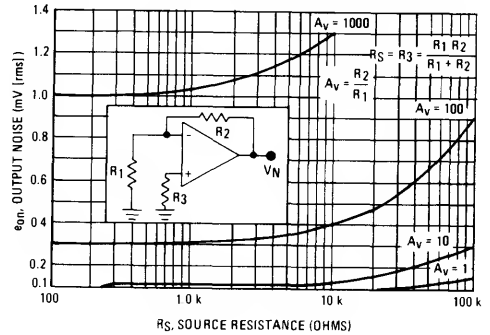


FIGURE 10 — OUTPUT NOISE versus SOURCE RESISTANCE

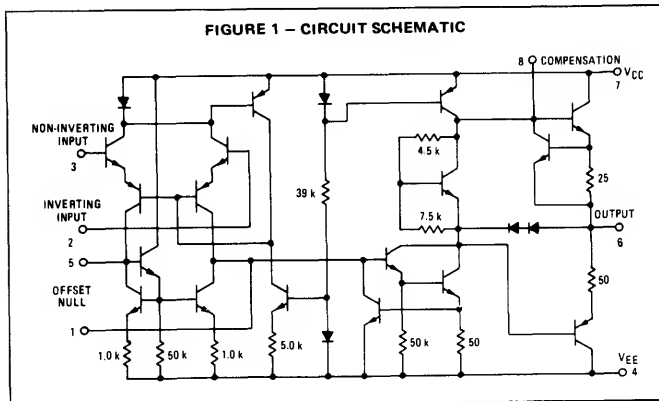


**HIGH PERFORMANCE
 OPERATIONAL AMPLIFIER**

The MC1748 is designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- Noncompensated MC1741
- Single 30 pF Capacitor Compensation Required For Unity Gain
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up

FIGURE 1 — CIRCUIT SCHEMATIC



TYPICAL COMPENSATION CIRCUITS

FIGURE 2 — OFFSET ADJUST AND FREQUENCY COMPENSATION

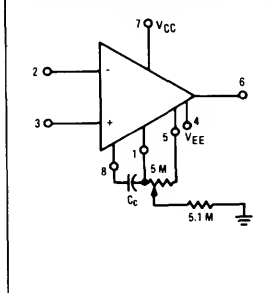


FIGURE 3 — SINGLE-POLE COMPENSATION

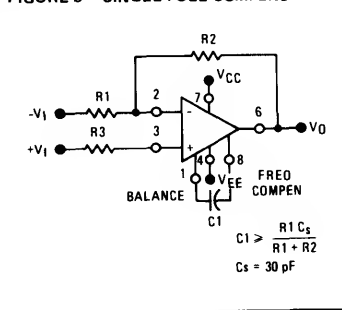
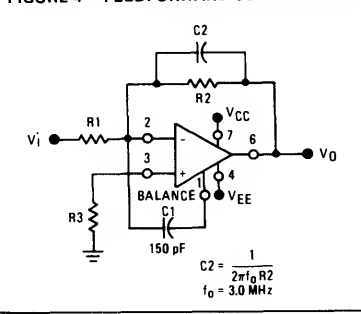


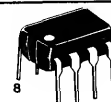
FIGURE 4 — FEEDFORWARD COMPENSATION



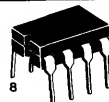
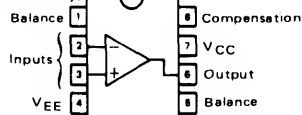
**MC1748
 MC1748C**

OPERATIONAL AMPLIFIER

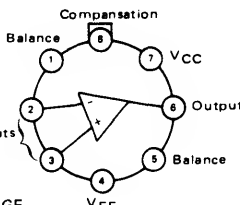
**SILICON MONOLITHIC
 INTEGRATED CIRCUIT**



**P1 SUFFIX
 PLASTIC PACKAGE
 CASE 626
 (MC1748C Only)**



**U SUFFIX
 CERAMIC PACKAGE
 CASE 693**



**G SUFFIX
 METAL PACKAGE
 CASE 601**

ORDERING INFORMATION

Device	Temperature Range	Package
MC1748G MC1748U	-55°C to +125°C	Metal Can Ceramic DIP
MC1748CG MC1748CP1 MC1748CU	0°C to +70°C	Metal Can Plastic DIP

MC1748, MC1748C

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	MC1748	MC1748C	Unit
Power Supply Voltage	V_{CC} V_{EE}	+22 -22	+18 -18	Vdc
Differential Input Signal	V_{in}	± 30		Volts
Common-Mode Input Swing ^①	V_{ICR}	± 15		Volts
Output Short Circuit Duration	t_s	Continuous		
Power Dissipation (Package Limitation) Derate above $T_A = +25^\circ\text{C}$	P_D	680 4.6		mW mW/ $^\circ\text{C}$
Operating Temperature Range	T_A	-55 to +125	0 to +70	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ Vdc}$, $V_{EE} = -15\text{ Vdc}$, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

Characteristics	Symbol	MC1748			MC1748C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Bias Current $T_A = +25^\circ\text{C}$ $T_A = T_{low}$ to T_{high} ^②	I_{IB}	—	0.08	0.5	—	0.08	0.5	μAdc
Input Offset Current $T_A = +25^\circ\text{C}$ $T_A = T_{low}$ to T_{high}	$ I_{IO} $	—	0.02	0.2	—	0.02	0.2	μAdc
Input Offset Voltage ($R_S \leq 10\text{ k}\Omega$) $T_A = +25^\circ\text{C}$ $T_A = T_{low}$ to T_{high}	$ V_{IO} $	—	1.0	5.0	—	1.0	6.0	mVdc
Differential Input Impedance (Open-Loop, $f = 20\text{ Hz}$)								
Parallel Input Resistance	R_p	0.3	2.0	—	0.3	2.0	—	Megohm
Parallel Input Capacitance	C_p	—	1.4	—	—	1.4	—	pF
Common-Mode Input Impedance ($f = 20\text{ Hz}$)	Z_{in}	—	200	—	—	200	—	Megohms
Common-Mode Input Voltage Swing	V_{ICR}	± 12	± 13	—	± 12	± 13	—	Vpk
Common-Mode Rejection Ratio ($f = 100\text{ Hz}$)	CMRR	70	90	—	70	90	—	dB
Open-Loop Voltage Gain, ($V_O = \pm 10\text{ V}$, $R_L = 2.0\text{ k}\Omega$) $T_A = +25^\circ\text{C}$ $T_A = T_{low}$ to T_{high}	A_{vol}	50,000 25,000	200,000 —	— —	20,000 15,000	200,000 —	— —	V/V
Step Response ($V_{in} = 20\text{ mV}$, $C_c = 30\text{ pF}$, $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$)								
Rise Time	t_r	—	0.3	—	—	0.3	—	μs
Overshoot Percentage		—	5.0	—	—	5.0	—	%
Slew Rate	dV_{out}/dt	—	0.8	—	—	0.8	—	V/ μs
Output Impedance ($f = 20\text{ Hz}$)	Z_O	—	75	—	—	75	—	ohms
Short-Circuit Output Current	I_{sc}	—	25	—	—	25	—	mAdc
Output Voltage Swing ($R_L = 10\text{ k}\Omega$) $R_L = 2\text{ k}\Omega$ ($T_A = T_{low}$ to t_{high})	V_O	± 12 ± 10	± 14 ± 13	— —	± 12 ± 10	± 14 ± 13	— —	Vpk
Power Supply Sensitivity $V_{EE} = \text{constant}$, $R_S \leq 10\text{ k}\Omega$ $V_{CC} = \text{constant}$, $R_S \leq 10\text{ k}\Omega$	S^+ S^-	— —	30 30	150 150	— —	30 30	150 150	$\mu\text{V/V}$
Power Supply Current	I_{D^+} I_{D^-}	— —	1.67 1.67	2.83 2.83	— —	1.67 1.67	2.83 2.83	mAdc
DC Quiescent Power Dissipation ($V_O = 0$)	P_D	—	50	85	—	50	85	mW

^① For supply voltages less than $\pm 15\text{ V}$, the Maximum Input Voltage is equal to the Supply Voltage.

^② T_{low} : 0°C for MC1748C
 -55°C for MC1748
 T_{high} : $+70^\circ\text{C}$ for MC1748C
 $+125^\circ\text{C}$ for MC1748

MC1748, MC1748C

TYPICAL CHARACTERISTICS

($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 5 – MINIMUM INPUT VOLTAGE RANGE

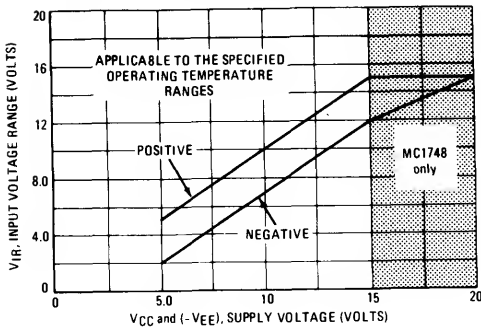


FIGURE 6 – MINIMUM OUTPUT VOLTAGE SWING

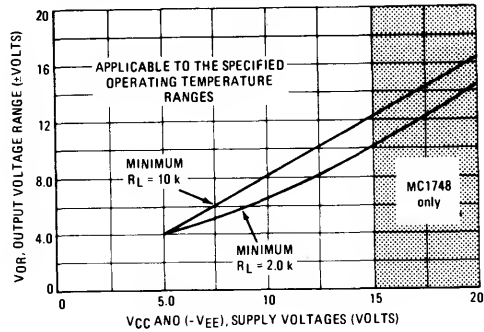


FIGURE 7 – MINIMUM VOLTAGE GAIN

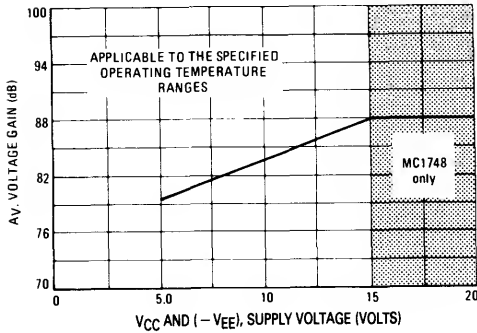


FIGURE 8 – TYPICAL SUPPLY CURRENTS

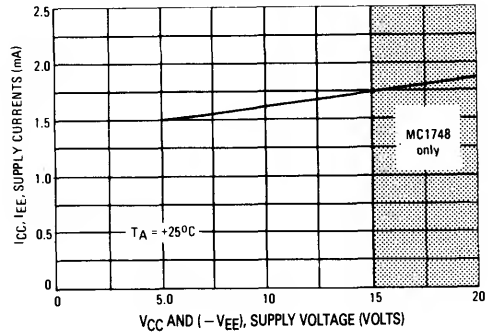


FIGURE 9 – OPEN-LOOP FREQUENCY RESPONSE

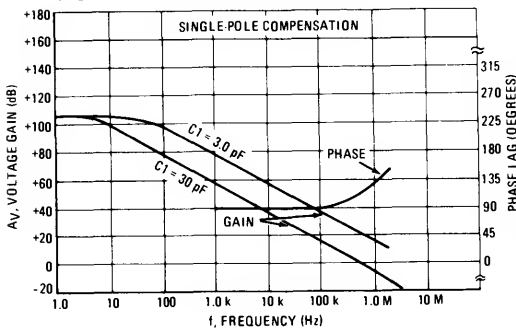
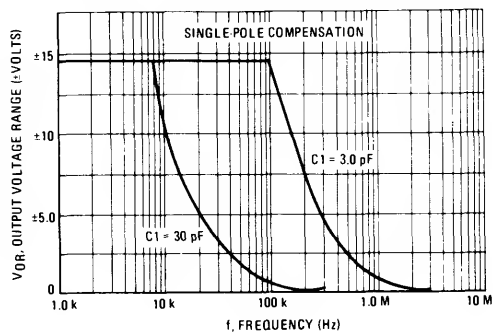


FIGURE 10 – LARGE-SIGNAL FREQUENCY RESPONSE



TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +15 V, V_{EE} = -15 V, T_A = +25°C unless otherwise noted.)

FIGURE 11 – VOLTAGE FOLLOWER PULSE RESPONSE

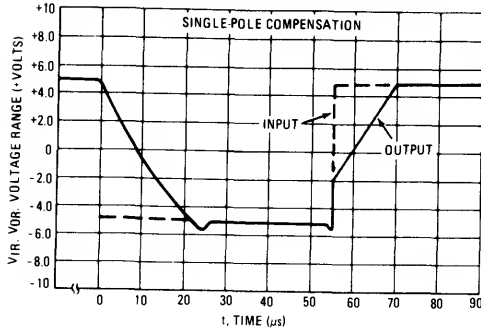


FIGURE 12 – OPEN-LOOP FREQUENCY RESPONSE

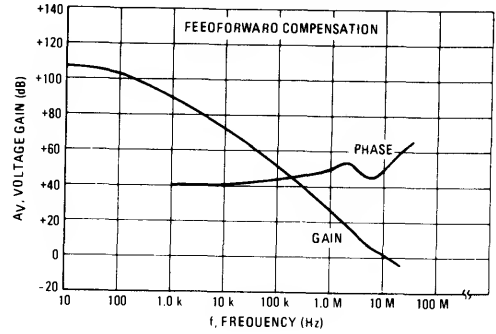


FIGURE 13 – LARGE-SIGNAL FREQUENCY RESPONSE

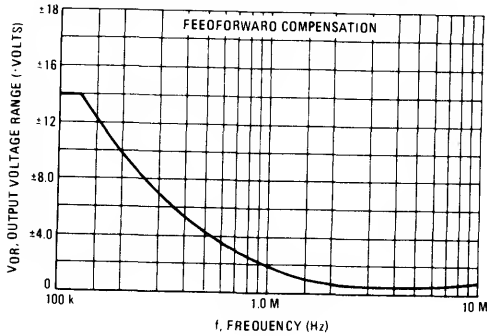
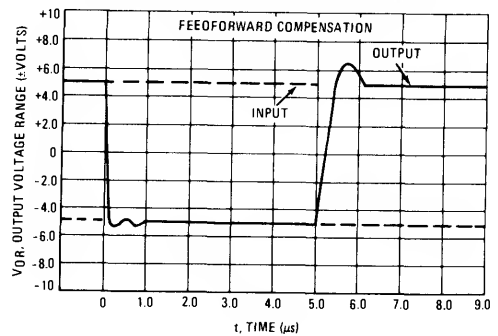


FIGURE 14 – INVERTER PULSE RESPONSE



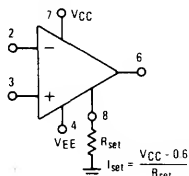
**MICROPOWER PROGRAMMABLE
 OPERATIONAL AMPLIFIER**

This extremely versatile operational amplifier features low power consumption and high input impedance. In addition, the quiescent currents within the device may be programmed by the choice of an external resistor value or current source applied to the I_{set} input. This allows the amplifier's characteristics to be optimized for input current and power consumption despite wide variations in operating power supply voltages.

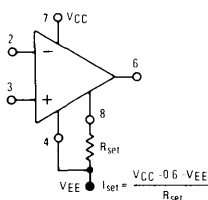
- ± 1.2 V to ± 18 V Operation
- Wide Programming Range
- Offset Null Capability
- No Frequency Compensation Required
- Low Input Bias Currents
- Short-Circuit Protection

RESISTIVE PROGRAMMING (See Figure 1.)

R_{set} to GROUND



R_{set} to NEGATIVE SUPPLY
 (Recommended for supply voltage less than ± 6.0 V)



Typical R_{set} Values

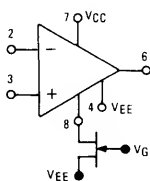
V_{CC}, V_{EE}	$I_{set} = 1.5 \mu A$	$I_{set} = 15 \mu A$
$\pm 6.0V$	3.6 M Ω	360 k Ω
$\pm 10V$	6.2 M Ω	620 k Ω
$\pm 12V$	7.5 M Ω	750 k Ω
$\pm 15V$	10 M Ω	1.0 M Ω

Typical R_{set} Values

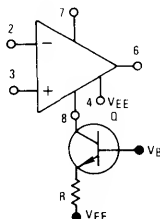
V_{CC}, V_{EE}	$I_{set} = 1.5 \mu A$	$I_{set} = 15 \mu A$
$\pm 1.5V$	1.6 M Ω	160 k Ω
$\pm 3.0V$	3.6 M Ω	360 k Ω
$\pm 6.0V$	7.5 M Ω	750 k Ω
$\pm 15 V$	20 M Ω	2.0 M Ω

ACTIVE PROGRAMMING

FET CURRENT SOURCE



BIPOLAR CURRENT SOURCE



Pins not shown are not connected.

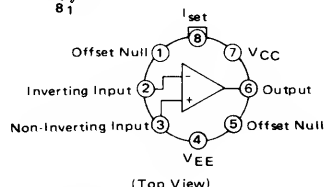
**MC1776
 MC1776C**

**PROGRAMMABLE
 OPERATIONAL AMPLIFIER**

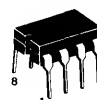
**SILICON MONOLITHIC
 INTEGRATED CIRCUIT**



G SUFFIX
 METAL PACKAGE
 CASE 601



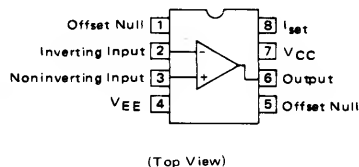
P1 SUFFIX
 PLASTIC PACKAGE
 CASE 626
 (MC1776C Only)



U SUFFIX
 CERAMIC PACKAGE
 CASE 693



D SUFFIX
 PLASTIC PACKAGE
 CASE 751
 (SO-8)



ORDERING INFORMATION

Device	Temperature Range	Package
MC1776G	-55 to +125°C	Metal Can
MC1776U		Ceramic DIP
MC1776CD	0 to +70°C	SO-8
MC1776CG		Metal Can
MC1776CP1		Plastic DIP
MC1776CU		Ceramic DIP

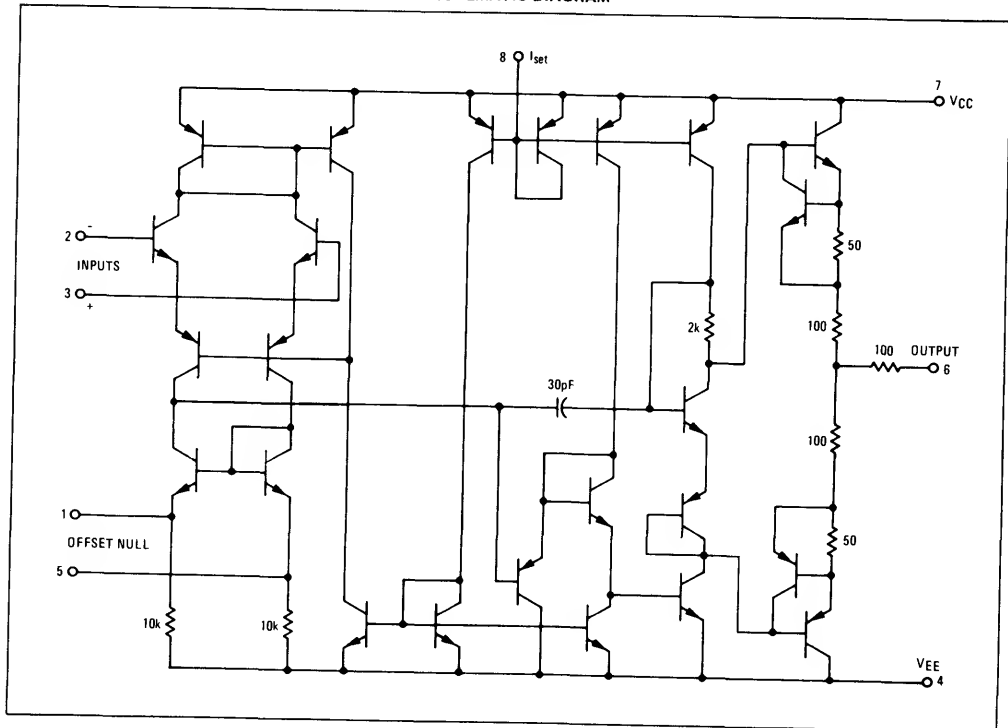
MC1776, MC1776C

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC}, V_{EE}	± 18	Vdc
Differential Input Voltage	V_{ID}	± 30	Vdc
Common-Mode Input Voltage V_{CC} and $ V_{EE} < 15\text{ V}$ V_{CC} and $ V_{EE} \geq 15\text{ V}$	V_{ICM}	V_{CC}, V_{EE} ± 15	Vdc
Offset Null to VEE Voltage	$V_{off-V_{EE}}$	± 0.5	Vdc
Programming Current	I_{set}	500	μA
Programming Voltage (Voltage from I_{set} terminal to ground)	V_{set}	$(V_{CC} - 2.0\text{ V})$ to V_{CC}	Vdc
Output Short-Circuit Duration*	t_s	Indefinite	s
Operating Temperature Range MC1776 MC1776C	T_A	-55 to +125 0 to +70	$^\circ\text{C}$
Storage Temperature Range Metal and Ceramic Packages Plastic Package	T_{stg}	-65 to +150 -55 to +125	$^\circ\text{C}$
Junction Temperature Metal and Ceramic Packages Plastic Package	T_J	175 150	$^\circ\text{C}$

*May be to ground or either Supply Voltage. Rating applies up to a case temperature of $+125^\circ\text{C}$ or ambient temperature of $+70^\circ\text{C}$ and $I_{set} \leq 30\text{ }\mu\text{A}$.

SCHEMATIC DIAGRAM



MC1776, MC1776C

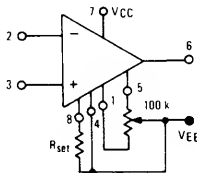
ELECTRICAL CHARACTERISTICS ($V_{CC} = +3.0\text{ V}$, $V_{EE} = -3.0\text{ V}$, $I_{set} = 1.5\text{ }\mu\text{A}$, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	MC1776			MC1776C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10\text{ k}\Omega$) $T_A = +25^\circ\text{C}$ $T_{low}^* \leq T_A \leq T_{high}^*$	V_{IO}	—	2.0	5.0	—	2.0	6.0	mV
		—	—	6.0	—	—	7.5	
Offset Voltage Adjustment Range	V_{IOR}	—	9.0	—	—	9.0	—	mV
Input Offset Current $T_A = +25^\circ\text{C}$ $T_A = T_{high}$ $T_A = T_{low}$	I_{IO}	—	0.7	3.0	—	0.7	6.0	nA
		—	—	5.0	—	—	6.0	
		—	—	10	—	—	10	
Input Bias Current $T_A = +25^\circ\text{C}$ $T_A = T_{high}$ $T_A = T_{low}$	I_{IB}	—	2.0	7.5	—	2.0	10	nA
		—	—	7.5	—	—	10	
		—	—	20	—	—	20	
Input Resistance	r_i	—	50	—	—	50	—	$M\Omega$
Input Capacitance	c_i	—	2.0	—	—	2.0	—	pF
Input Voltage Range $T_{low} \leq T_A \leq T_{high}$	V_{ID}	± 1.0	—	—	± 1.0	—	—	V
Large Signal Voltage Gain $R_L \geq 75\text{ k}\Omega$, $V_O = \pm 1.0\text{ V}$, $T_A = +25^\circ\text{C}$ $R_L \geq 75\text{ k}\Omega$, $V_O = \pm 1.0\text{ V}$, $T_{low} \leq T_A \leq T_{high}$	AV_{OL}	50 k 25 k	200 k —	— —	25 k 25 k	200 k —	— —	V/V
Output Voltage Swing $R_L \geq 75\text{ k}\Omega$, $T_{low} \leq T_A \leq T_{high}$	V_O	± 2.0	± 2.4	—	± 2.0	± 2.4	—	V
Output Resistance	r_o	—	5.0	—	—	5.0	—	$k\Omega$
Output Short-Circuit Current	I_{OS}	—	3.0	—	—	3.0	—	mA
Common-Mode Rejection Ratio $R_S \leq 10\text{ k}\Omega$, $T_{low} \leq T_A \leq T_{high}$	CMRR	70	86	—	70	86	—	dB
Supply Voltage Rejection Ratio $R_S \leq 10\text{ k}\Omega$, $T_{low} \leq T_A \leq T_{high}$	PSRR	—	25	150	—	25	200	$\mu\text{V/V}$
Supply Current $T_A = +25^\circ\text{C}$ $T_{low} \leq T_A \leq T_{high}$	I_{CC} , I_{EE}	—	13	20	—	13	20	μA
		—	—	25	—	—	25	
Power Dissipation $T_A = +25^\circ\text{C}$ $T_{low} \leq T_A \leq T_{high}$	P_D	—	78	120	—	78	120	μW
		—	—	150	—	—	150	
Transient Response (Unity Gain) $V_{in} = 20\text{ mV}$, $R_L \geq 5.0\text{ k}\Omega$, $C_L = 100\text{ pF}$ Rise Time Overshoot	t_{TLH} OS	— —	3.0 0	— —	— —	3.0 0	— —	μs %
Slew Rate ($R_L \geq 5.0\text{ k}\Omega$)	S_R	—	0.03	—	—	0.03	—	$\text{V}/\mu\text{s}$

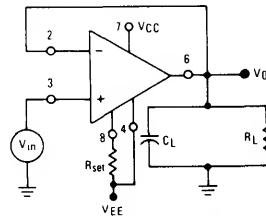
* $T_{low} = -55^\circ\text{C}$ for MC1776
0°C for MC1776C

$T_{high} = +125^\circ\text{C}$ for MC1776
+70°C for MC1776C

**VOLTAGE OFFSET
NULL CIRCUIT**



**TRANSIENT-RESPONSE
TEST CIRCUIT**



Pins not shown are not connected.

MC1776, MC1776C

2

ELECTRICAL CHARACTERISTICS — continued ($V_{CC} = +3.0\text{ V}$, $V_{EE} = -3.0\text{ V}$, $I_{set} = 15\text{ }\mu\text{A}$, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	MC1776			MC1776C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10\text{ k}\Omega$) $T_A = +25^\circ\text{C}$ $T_{low}^* \leq T_A \leq T_{high}^*$	V_{IO}	—	2.0	5.0	—	2.0	6.0	mV
Offset Voltage Adjustment Range	V_{IOR}	—	18	—	—	18	—	mV
Input Offset Current $T_A = +25^\circ\text{C}$ $T_A = T_{high}$ $T_A = T_{low}$	I_{IO}	—	2.0	15	—	2.0	25	nA
		—	—	15	—	—	25	
		—	—	40	—	—	40	
Input Bias Current $T_A = +25^\circ\text{C}$ $T_A = T_{high}$ $T_A = T_{low}$	I_{IB}	—	15	50	—	15	50	nA
		—	—	50	—	—	50	
		—	—	120	—	—	100	
Input Resistance	r_i	—	5.0	—	—	5.0	—	M Ω
Input Capacitance	c_i	—	2.0	—	—	2.0	—	pF
Input Voltage Range $T_{low} \leq T_A \leq T_{high}$	V_{ID}	± 1.0	—	—	± 1.0	—	—	V
Large Signal Voltage Gain $R_L \geq 5.0\text{ k}\Omega$, $V_O = \pm 1.0\text{ V}$, $T_A = +25^\circ\text{C}$ $R_L \geq 5.0\text{ k}\Omega$, $V_O = \pm 1.0\text{ V}$, $T_{low} \leq T_A \leq T_{high}$	A_{VOL}	50 k	200 k	—	25 k	200 k	—	V/V
		25 k	—	—	25k	—	—	
Output Voltage Swing $R_L \geq 5.0\text{ k}\Omega$, $T_{low} \leq T_A \leq T_{high}$	V_O	± 1.9	± 2.1	—	± 2.0	± 2.1	—	V
Output Resistance	r_o	—	1.0	—	—	1.0	—	k Ω
Output Short-Circuit Current	I_{OS}	—	5.0	—	—	5.0	—	mA
Common-Mode Rejection Ratio $R_S \leq 10\text{ k}\Omega$, $T_{low} \leq T_A \leq T_{high}$	CMRR	70	86	—	70	86	—	dB
Supply Voltage Rejection Ratio $R_S \leq 10\text{ k}\Omega$, $T_{low} \leq T_A \leq T_{high}$	PSRR	—	25	150	—	25	200	$\mu\text{V/V}$
Supply Current $T_A = +25^\circ\text{C}$ $T_{low} \leq T_A \leq T_{high}$	I_{CC} , I_{EE}	—	130	160	—	130	170	μA
		—	—	180	—	—	180	
Power Dissipation $T_A = +25^\circ\text{C}$ $T_{low} \leq T_A \leq T_{high}$	P_D	—	780	960	—	780	1020	μW
		—	—	1080	—	—	1080	
Transient Response (Unity Gain) $V_{in} = 20\text{ mV}$, $R_L \geq 5.0\text{ k}\Omega$, $C_L = 100\text{ pF}$ Rise Time Overshoot	t_{TLH} OS	—	0.6	—	—	0.6	—	μs %
		—	5.0	—	—	5.0	—	
Slew Rate ($R_L \geq 5.0\text{ k}\Omega$)	SR	—	0.35	—	—	0.35	—	V/ μs

* $T_{low} = -55^\circ\text{C}$ for MC1776
0 $^\circ\text{C}$ for MC1776C

$T_{high} = +125^\circ\text{C}$ for MC1776
+70 $^\circ\text{C}$ for MC1776C

MC1776, MC1776C

2

ELECTRICAL CHARACTERISTICS — continued ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $I_{set} = 1.5\text{ }\mu\text{A}$, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	MC1776			MC1776C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10\text{ k}\Omega$) $T_A = +25^\circ\text{C}$ $T_{low}^* \leq T_A \leq T_{high}^*$	V_{IO}	—	2.0	5.0	—	2.0	6.0	mV
		—	—	6.0	—	—	7.5	
Offset Voltage Adjustment Range	V_{IOR}	—	9.0	—	—	9.0	—	mV
Input Offset Current $T_A = +25^\circ\text{C}$ $T_A = T_{high}$ $T_A = T_{low}$	I_{IO}	—	0.7	3.0	—	0.7	6.0	nA
		—	—	5.0	—	—	6.0	
		—	—	10	—	—	10	
Input Bias Current $T_A = +25^\circ\text{C}$ $T_A = T_{high}$ $T_A = T_{low}$	I_{IB}	—	2.0	7.5	—	2.0	10	nA
		—	—	7.5	—	—	10	
		—	—	20	—	—	20	
Input Resistance	r_i	—	50	—	—	50	—	M Ω
Input Capacitance	c_i	—	2.0	—	—	2.0	—	pF
Input Voltage Range $T_{low} \leq T_A \leq T_{high}$	V_{ID}	± 10	—	—	± 10	—	—	V
Large Signal Voltage Gain $R_L \geq 75\text{ k}\Omega$, $V_O = \pm 10\text{ V}$, $T_A = +25^\circ\text{C}$ $R_L \geq 75\text{ k}\Omega$, $V_O = \pm 10\text{ V}$, $T_{low} \leq T_A \leq T_{high}$	$AVOL$	200 k 100 k	400 k —	— —	50 k 50 k	400 k —	— —	V/V
Output Voltage Swing $R_L \geq 75\text{ k}\Omega$, $T_A = +25^\circ\text{C}$ $R_L \geq 75\text{ k}\Omega$, $T_{low} \leq T_A \leq T_{high}$	V_O	± 12 ± 10	± 14 —	— —	± 12 ± 10	± 14 —	— —	V
Output Resistance	r_o	—	5.0	—	—	5.0	—	k Ω
Output Short-Circuit Current	I_{os}	—	3.0	—	—	3.0	—	mA
Common-Mode Rejection Ratio $R_S \leq 10\text{ k}\Omega$, $T_{low} \leq T_A \leq T_{high}$	CMRR	70	90	—	70	90	—	dB
Supply Voltage Rejection Ratio $R_S \leq 10\text{ k}\Omega$, $T_{low} \leq T_A \leq T_{high}$	PSRR	—	25	150	—	25	200	$\mu\text{V/V}$
Supply Current $T_A = +25^\circ\text{C}$ $T_{low} \leq T_A \leq T_{high}$	I_{CC} , I_{EE}	—	20	25	—	20	30	μA
		—	—	30	—	—	35	
Power Dissipation $T_A = +25^\circ\text{C}$ $T_{low} \leq T_A \leq T_{high}$	P_D	—	—	0.75 0.9	—	—	0.9 1.05	mW
Transient Response (Unity Gain) $V_{in} = 20\text{ mV}$, $R_L \geq 5.0\text{ k}\Omega$, $C_L = 100\text{ pF}$ Rise Time Overshoot	t_{TLH} t_{OS}	— —	1.6 0	— —	— —	1.6 0	— —	μs %
Slew Rate ($R_L \geq 5.0\text{ k}\Omega$)	S_R	—	0.1	—	—	0.1	—	V/ μs

* $T_{low} = -55^\circ\text{C}$ for MC1776
0 $^\circ\text{C}$ for MC1776C

$T_{high} = +125^\circ\text{C}$ for MC1776
+70 $^\circ\text{C}$ for MC1776C

MC1776, MC1776C

ELECTRICAL CHARACTERISTICS — continued ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $I_{set} = 15\text{ }\mu\text{A}$, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	MC1776			MC1776C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10\text{ k}\Omega$) $T_A = +25^\circ\text{C}$ $T_{low}^* \leq T_A \leq T_{high}^*$	V_{IO}	—	2.0	5.0	—	2.0	6.0	mV
		—	—	6.0	—	—	7.5	
Offset Voltage Adjustment Range	V_{IOR}	—	18	—	—	18	—	mV
Input Offset Current $T_A = +25^\circ\text{C}$ $T_A = T_{high}$ $T_A = T_{low}$	I_{IO}	—	2.0	15	—	2.0	25	nA
		—	—	15	—	—	25	
		—	—	40	—	—	40	
Input Bias Current $T_A = +25^\circ\text{C}$ $T_A = T_{high}$ $T_A = T_{low}$	I_{IB}	—	15	50	—	15	50	nA
		—	—	50	—	—	50	
		—	—	120	—	—	100	
Input Resistance	r_i	—	5.0	—	—	5.0	—	M Ω
Input Capacitance	c_i	—	2.0	—	—	2.0	—	pF
Input Voltage Range $T_{low} \leq T_A \leq T_{high}$	V_{ID}	± 10	—	—	± 10	—	—	V
Large Signal Voltage Gain $R_L \geq 5.0\text{ k}\Omega$, $V_O = \pm 10\text{ V}$, $T_A = +25^\circ\text{C}$ $R_L \geq 75\text{ k}\Omega$, $V_O = \pm 10\text{ V}$, $T_{low} \leq T_A \leq T_{high}$	A_{VOL}	100 k 75 k	400 k —	— —	50 k 50 k	400 k —	— —	V/V
Output Voltage Swing $R_L \geq 5.0\text{ k}\Omega$, $T_A = +25^\circ\text{C}$ $R_L \geq 75\text{ k}\Omega$, $T_{low} \leq T_A \leq T_{high}$	V_O	± 10 ± 10	± 13 —	— —	± 10 ± 10	± 13 —	— —	V
Output Resistance	r_o	—	1.0	—	—	1.0	—	k Ω
Output Short-Circuit Current	I_{OS}	—	12	—	—	12	—	mA
Common-Mode Rejection Ratio $R_S \leq 10\text{ k}\Omega$, $T_{low} \leq T_A \leq T_{high}$	CMRR	70	90	—	70	90	—	dB
Supply Voltage Rejection Ratio $R_S \leq 10\text{ k}\Omega$, $T_{low} \leq T_A \leq T_{high}$	PSRR	—	25	150	—	25	200	$\mu\text{V/V}$
Supply Current $T_A = +25^\circ\text{C}$ $T_{low} \leq T_A \leq T_{high}$	I_{CC}, I_{EE}	— —	160 —	180 200	— —	160 —	190 200	μA
Power Dissipation $T_A = +25^\circ\text{C}$ $T_{low} \leq T_A \leq T_{high}$	P_D	— —	— —	5.4 6.0	— —	— —	5.7 6.0	mW
Transient Response (Unity Gain) $V_{in} = 20\text{ mV}$, $R_L \geq 5.0\text{ k}\Omega$, $C_L = 100\text{ pF}$ Rise Time Overshoot	t_{TLH} OS	— —	0.35 10	— —	— —	0.35 10	— —	μs %
Slew Rate ($R_L \geq 5.0\text{ k}\Omega$)	SR	—	0.8	—	—	0.8	—	V/ μs

* $T_{low} = -55^\circ\text{C}$ for MC1776
0 $^\circ\text{C}$ for MC1776C

$T_{high} = +125^\circ\text{C}$ for MC1776
+70 $^\circ\text{C}$ for MC1776C

MC1776, MC1776C

TYPICAL CHARACTERISTICS

($T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 1 – SET CURRENT versus SET RESISTOR

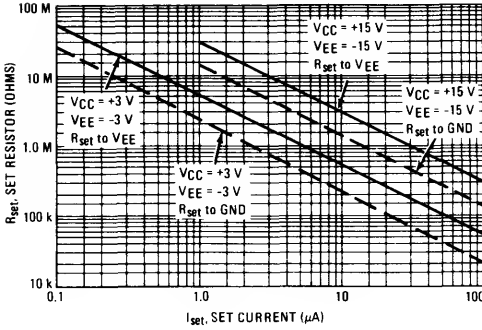


FIGURE 2 – POSITIVE STANDBY SUPPLY CURRENT versus SET CURRENT

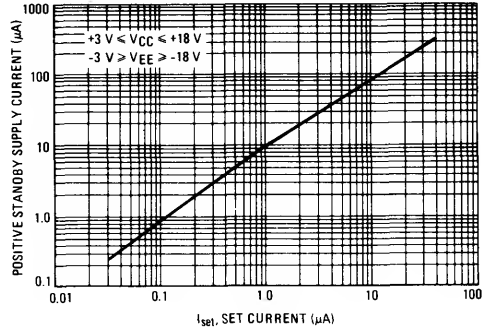


FIGURE 3 – OPEN-LOOP GAIN versus SET CURRENT

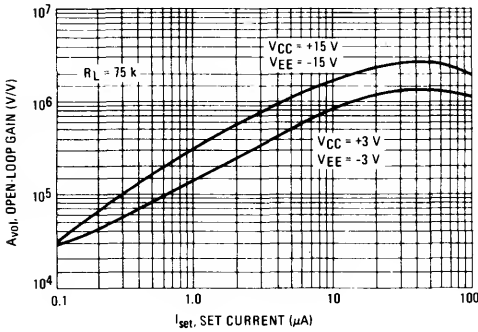


FIGURE 4 – INPUT BIAS CURRENT versus SET CURRENT

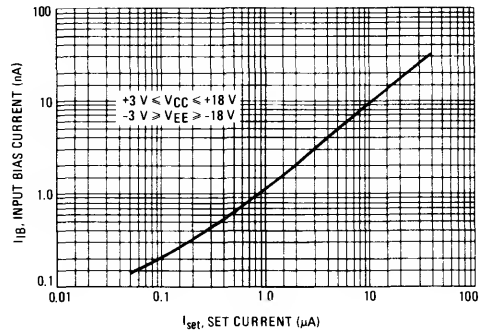


FIGURE 5 – INPUT BIAS CURRENT versus AMBIENT TEMPERATURE

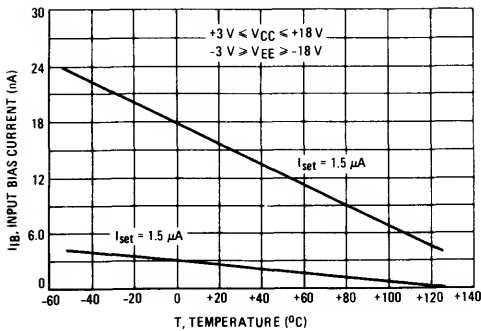
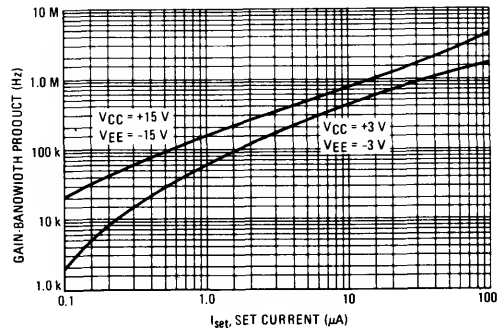
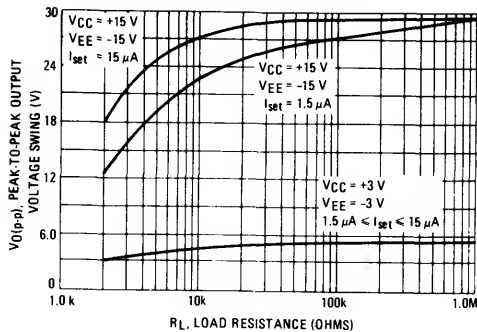
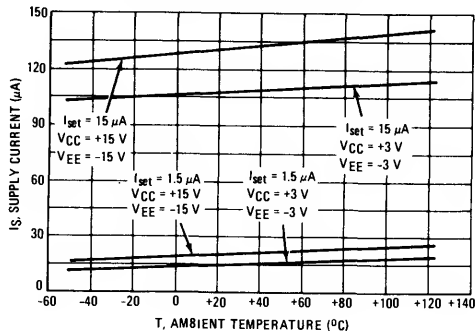
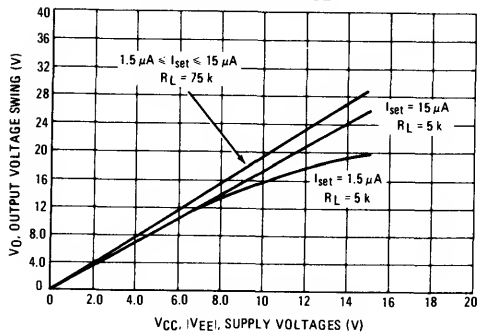
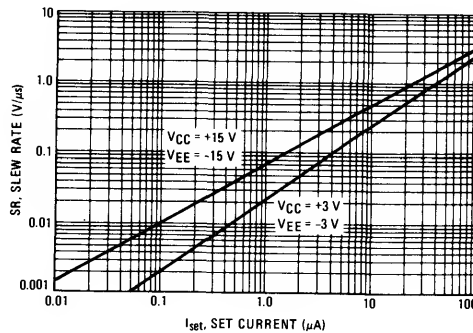
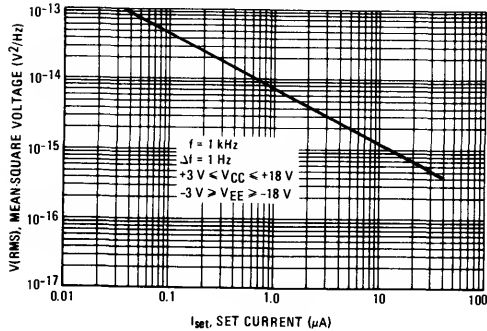
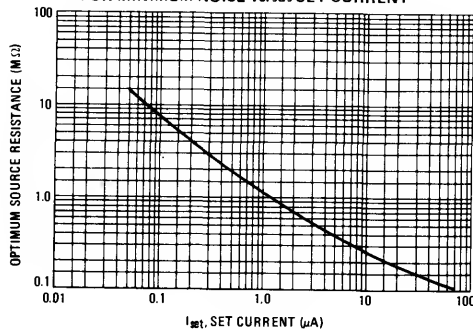


FIGURE 6 – GAIN-BANDWIDTH PRODUCT (GBW) versus SET CURRENT



TYPICAL CHARACTERISTICS (continued)

 $(T_A = +25^\circ\text{C}$ unless otherwise noted.)FIGURE 7 – OUTPUT VOLTAGE SWING
versus LOAD RESISTANCEFIGURE 8 – SUPPLY CURRENT
versus AMBIENT TEMPERATUREFIGURE 9 – OUTPUT VOLTAGE SWING
versus SUPPLY VOLTAGEFIGURE 10 – SLEW RATE
versus SET CURRENTFIGURE 11 – INPUT NOISE VOLTAGE
versus SET CURRENTFIGURE 12 – OPTIMUM SOURCE RESISTANCE
FOR MINIMUM NOISE versus SET CURRENT

APPLICATIONS INFORMATION

FIGURE 13 – WIEN BRIDGE OSCILLATOR

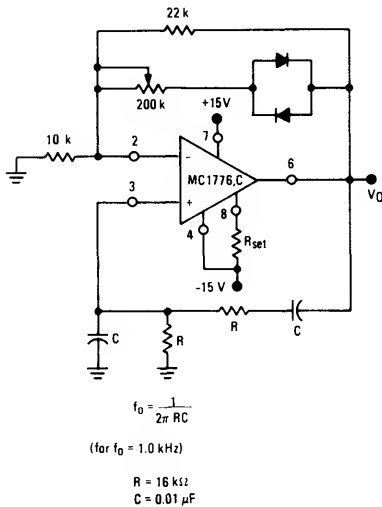
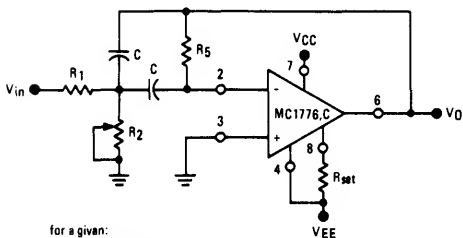


FIGURE 14 – MULTIPLE FEEDBACK BANDPASS FILTER



for a given:
 f_0 = center frequency
 $A(f_0)$ = Gain at center frequency
 Q = quality factor
 Choose a value for C , then

$$R_5 = \frac{Q}{\pi f_0 C}$$

$$R_1 = \frac{R_5}{2A(f_0)}$$

$$R_2 = \frac{R_1 R_5}{4Q^2 R_1 - R_5}$$

To obtain less than 10% error from the operational amplifier:

$$\frac{Q f_0}{GBW} < 0.1$$

where f_0 and GBW are expressed in Hz. GBW is available from Figure 6 as a function of Sat Current, I_{sat} .

FIGURE 15 – MULTIPLE FEEDBACK BANDPASS FILTER
(1.0 kHz)

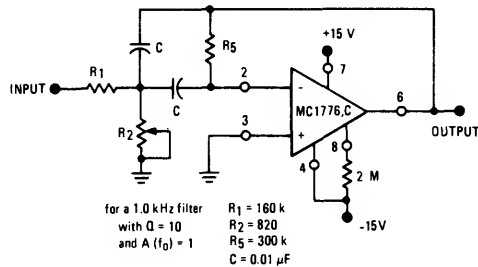


FIGURE 16 – GATED AMPLIFIER

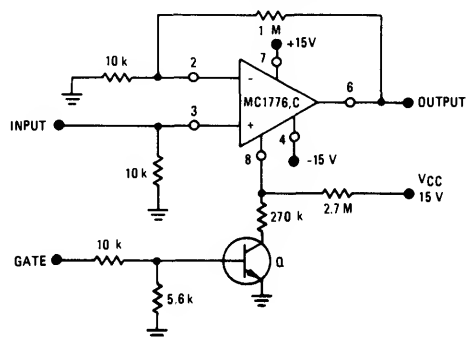
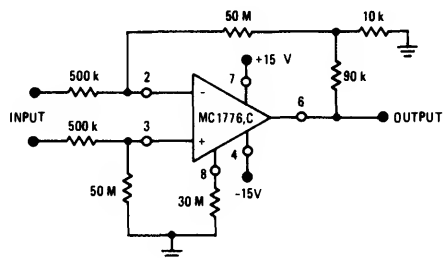


FIGURE 17 – HIGH INPUT IMPEDANCE AMPLIFIER



QUAD SINGLE SUPPLY OPERATIONAL AMPLIFIER

These internally compensated Norton operational amplifiers are designed specifically for single positive power supply applications found in industrial control systems and automotive electronics. Each device contains four independent amplifiers — making it ideal for applications such as active filters, multi-channel amplifiers, tachometers, oscillators and other similar usages.

- Single-Supply Operation
- Internally Compensated
- Wide Unity Gain Bandwidth: 4.0 MHz Typical
- Low Input Bias Current: 50 nA Typical
- High Open-Loop Gain: 1000 V/V Minimum
- Large Output Voltage Swing: ($V_{CC} - 1$) V_{p-p}

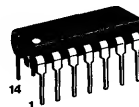
MAXIMUM RATINGS

Rating	Symbol	LM2900/ LM3900	MC3301	MC3401	Unit
Supply Voltage	V_{CC}	+32	+28	+18	V
Input Currents (I_{in}^+ or I_{in}^-)	I_{in}	5.0	5.0	5.0	mA
Output Current	I_O	50	50	50	mA
Power Dissipation ($T_A = +25^\circ\text{C}$) Derate above $T_A = +25^\circ\text{C}$	P_D $1/R_{\theta JA}$	625 5.0	625 5.0	625 5.0	mW mW/°C
Operating Ambient Temperature Range LM2900	T_A	— -40 to +85	-40 to +85	0 to +70	°C
LM3900		0 to +70	—	—	
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	-65 to +150	°C

MC3301 LM2900
MC3401 LM3900

QUAD OPERATIONAL AMPLIFIER

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**

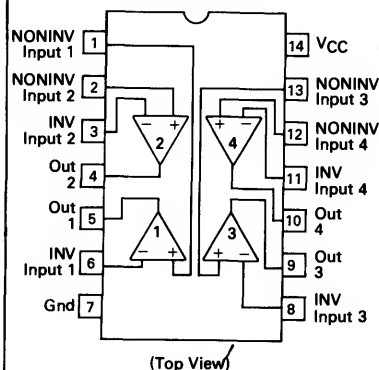


N, P SUFFIX
PLASTIC PACKAGE
CASE 646

D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)



PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
LM3900D MC3401D	0°C to +70°C	SO-14
LM3900N MC3401P		Plastic DIP
LM2900N MC3301P	-40°C to +85°C	

MC3301, MC3401, LM2900, LM3900

2

ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $T_A = +25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	LM2900			LM3900			MC3301			MC3401			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Open-Loop Voltage Gain $f = 100\text{ Hz}$, $R_L = 5.0\text{ k}$ $T_A = T_{\text{low}}$ to T_{high} (Notes 1, 2)	A_{VOL}	1.2	2.0	—	1.2	2.0	—	1.2	2.0	—	1.2	2.0	—	V/mV
Input Resistance (Inverting Input)	r_i	—	1.0	—	—	1.0	—	—	1.0	—	0.1	1.0	—	M Ω
Output Resistance	r_O	—	8.0	—	—	8.0	—	—	8.0	—	—	8.0	—	k Ω
Input Bias Current (Inverting Input) $T_A = T_{\text{low}}$ to T_{high} (Note 1)	I_B	—	50	200	—	50	200	—	50	300	—	50	300	nA
Slew Rate ($C_L = 100\text{ pF}$, $R_L = 2.0\text{ k}$) Positive Output Swing Negative Output Swing	SR	—	0.5	—	—	0.5	—	—	0.5	—	—	0.5	—	V/ μs
Unity Gain Bandwidth	BW	—	4.0	—	—	4.0	—	—	4.0	—	—	4.0	—	MHz
Output Voltage Swing (Note 7) $V_{CC} = +15\text{ V}$, $R_L = 2.0\text{ k}$ $V_{\text{out High}} (I_{\text{in}}^- = 0, I_{\text{in}}^+ = 0)$ $V_{\text{out Low}} (I_{\text{in}}^- = 10\text{ }\mu\text{A}, I_{\text{in}}^+ = 0)$ $V_{CC} = \text{Maximum Rating}$, $R_L = \infty$ $V_{\text{out High}} (I_{\text{in}}^- = 0, I_{\text{in}}^+ = 0)$	V_{OH} V_{OL} V_{OH}	13.5 — —	14.2 0.03 29.5	— 0.2 —	13.5 — —	14.2 0.03 29.5	— 0.2 —	13.5 — —	14.2 0.03 25.5	— 0.2 —	13.5 — —	14.2 0.03 15.5	— 0.2 —	V
Output Current Source Sink (Note 3) Low Level Output Current $I_{\text{in}}^- = 5.0\text{ }\mu\text{A}$, $V_{OL} = 1.0\text{ V}$	I_{source} I_{sink} I_{OL}	6.0 0.5 —	10 0.87 5.0	— — —	6.0 0.5 —	10 0.87 5.0	— — —	5.0 0.5 —	10 0.87 5.0	— — —	5.0 0.5 —	10 0.87 5.0	— — —	mA
Supply Current (All Four Amplifiers) Noninverting Inputs Open Noninverting Inputs Grounded	I_{DO} I_{DG}	— —	6.9 7.8	10 14	— —	6.9 7.8	10 14	— —	6.9 7.8	10 14	— —	6.9 7.8	10 14	mA
Power Supply Rejection ($f = 100\text{ Hz}$)	PSRR	—	55	—	—	55	—	—	55	—	—	55	—	dB
Mirror Gain ($T_A = T_{\text{low}}$ to T_{high} ; Notes 1, 4) $I_{\text{in}}^+ = 20\text{ }\mu\text{A}$ $I_{\text{in}}^+ = 200\text{ }\mu\text{A}$	A_i	0.90 0.90	1.0 1.0	1.1 1.1	0.90 0.90	1.0 1.0	1.1 1.1	0.90 0.90	1.0 1.0	1.1 1.1	0.90 0.90	1.0 1.0	1.1 1.0	μA
Δ Mirror Gain ($T_A = T_{\text{low}}$ to T_{high} ; Notes 1, 4) $20\text{ }\mu\text{A} \leq I_{\text{in}}^+ \leq 200\text{ }\mu\text{A}$	ΔA_i	—	2.0	5.0	—	2.0	5.0	—	2.0	5.0	—	2.0	5.0	%
Mirror Current ($T_A = T_{\text{low}}$ to T_{high} ; Notes 1, 5)		—	10	500	—	10	500	—	10	500	—	10	500	μA
Negative Input Current (Note 6)		—	1.0	—	—	1.0	—	—	1.0	—	—	1.0	—	mA

NOTES:

- $T_{\text{low}} = -40^\circ\text{C}$ for LM2900, MC3301
 $= 0^\circ\text{C}$ for LM3900, MC3401
 $T_{\text{high}} = +85^\circ\text{C}$ for LM2900, MC3301
 $= +70^\circ\text{C}$ for LM3900, MC3401
- Open-loop voltage gain is defined as voltage gain from the inverting input to the output.
- Sink current is specified for linear operation. When the device is used as a comparator (non-linear operation) where the inverting input is overdriven, the sink current (low level output current) capability is typically 5.0 mA.
- This specification indicates the current gain of the current mirror which is used as the noninverting input.
- Input V_{BE} match between the noninverting and inverting inputs occurs for a mirror current (noninverting input current) of approximately $10\text{ }\mu\text{A}$.
- Clamp transistors are included to prevent the input voltages from swinging below ground more than approximately -0.3 volts . The negative input currents that may result from large signal overdrive with capacitive input coupling must be limited externally to values of approximately 1.0 mA . Negative input currents in excess of 4.0 mA will cause the output to drop to a low voltage. These values apply for any one of the input terminals. If more than one of the input terminals are simultaneously driven negative, maximum currents are reduced. Common-mode biasing can be used to prevent negative input voltages.
- When used as a noninverting amplifier, the minimum output voltage is the V_{BE} of the inverting input transistor.

TYPICAL CHARACTERISTICS

($V_{CC} = +15\text{ Vdc}$, $R_L = 5.0\text{ k}\Omega$, $T_A = +25^\circ\text{C}$
[each amplifier] unless otherwise noted.)

FIGURE 1 — OPEN-LOOP VOLTAGE GAIN versus FREQUENCY

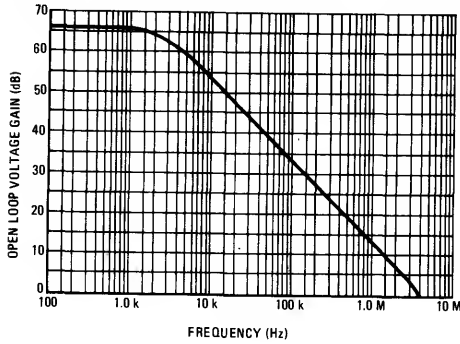


FIGURE 2 — OPEN-LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE

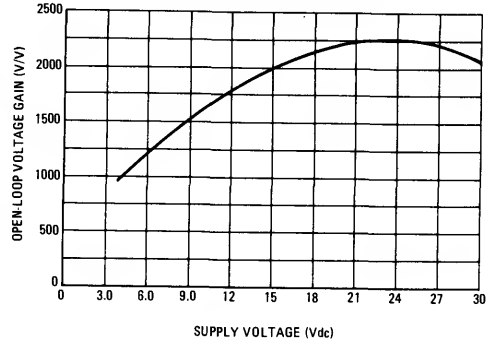


FIGURE 3 — OUTPUT RESISTANCE versus FREQUENCY

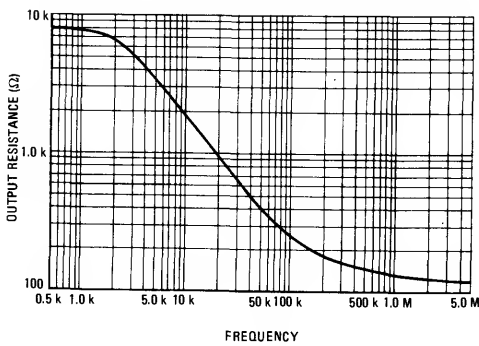


FIGURE 4 — SUPPLY CURRENT versus SUPPLY VOLTAGE

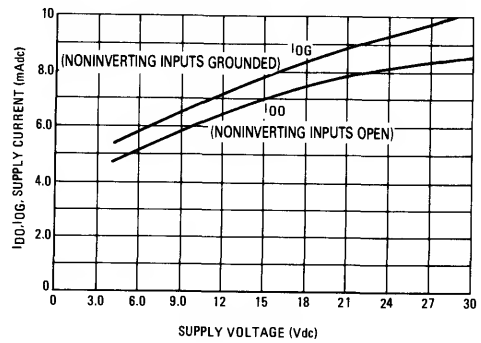


FIGURE 5 — LINEAR SOURCE CURRENT versus SUPPLY VOLTAGE

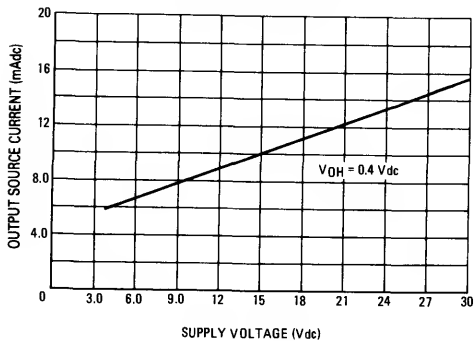
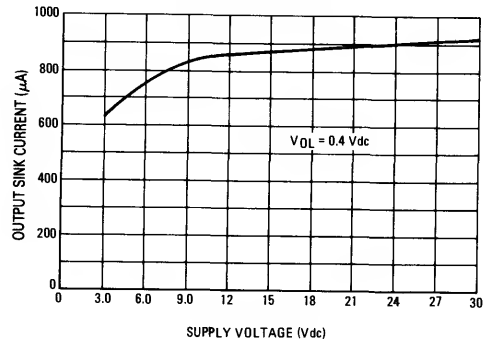


FIGURE 6 — LINEAR SINK CURRENT versus SUPPLY VOLTAGE



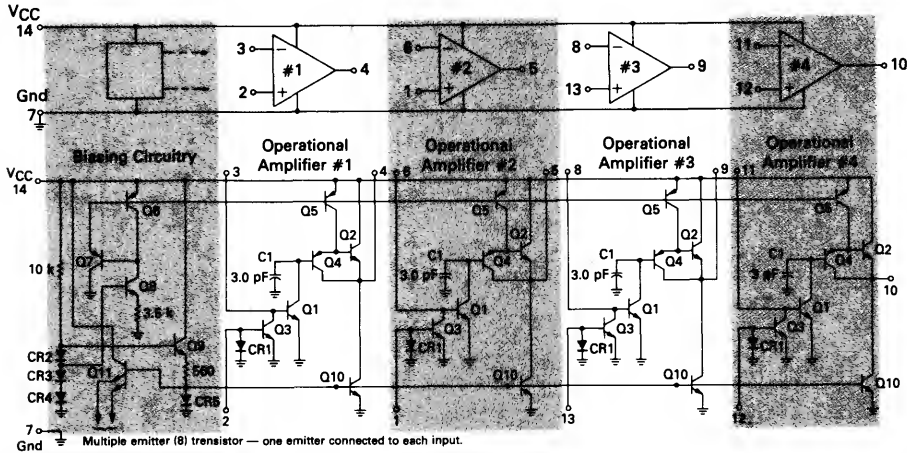
OPERATION AND APPLICATIONS

BASIC AMPLIFIER

The basic amplifier is the common emitter stage shown in Figures 7 and 8. The active load I_1 is buffered from the input transistor by a PNP transistor, Q4, and from the output by an NPN transistor, Q2. Q2 is biased Class A by the current source I_2 . The magnitude of I_2 (specified I_{sink}) is a limiting factor in capacitively cou-

pled linear operation at the output. The sink current of the device can be forced to exceed the specified level by keeping the output dc voltage above ≈ 1.0 volt resulting in an increase in the distortion appearing at the output. Closed-loop stability is maintained by an on-the-chip 3-pF capacitor shown in Figure 10 on the following page. No external compensation is required.

FIGURE 7 — BLOCK DIAGRAM



A noninverting input is obtained by adding a current mirror as shown in Figure 9. Essentially all current which enters the noninverting input, I_{in}^+ , flows through the diode CR1. The voltage drop across CR1 corresponds to this input current magnitude and this same voltage is applied to a matched device, Q3. Thus Q3 is biased to conduct an emitter current equal to I_{in}^+ . Since the alpha current gain of Q3 ≈ 1 , its collector current is

approximately equal to I_{in}^+ also. In operation this current flows through an external feedback resistor which generates the output voltage signal. For inverting applications, the noninverting input is often used to set the dc quiescent level at the output. Techniques for doing this are discussed in the "Normal Design Procedure" section.

FIGURE 8 — A BASIC GAIN STAGE

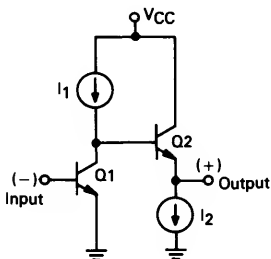
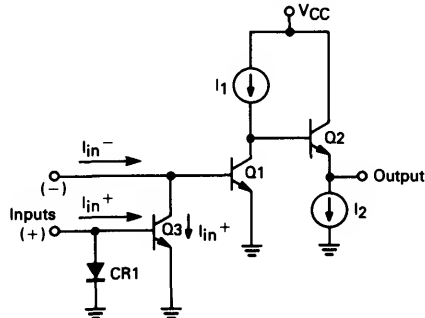


FIGURE 9 — OBTAINING A NONINVERTING INPUT



OPERATION AND APPLICATIONS (continued)

2

BIASING CIRCUITRY

The circuitry common to all four amplifiers is shown in Figure 11. The purpose of this circuitry is to provide biasing voltage for the PNP and NPN current sources used in the amplifiers.

The voltage drops across diodes CR2, CR3 and CR4 are used as references. The voltage across resistor R1 is the sum of the drops across CR4 and CR3 minus the V_{BE} of Q8. The PNP current sources (Q5, etc.) are set to the magnitude $V_{BE}/R1$ by transistor Q6. Transistor

Q7 reduces base current loading. The voltage across resistor R2 is the sum of the voltage drops across CR2, CR3 and CR4, minus the V_{BE} drops of transistor Q9 and diode CR5 thus the current set is established by CR5 in all the NPN current sources (Q10, etc.). This technique results in current source magnitudes which are relatively independent of the supply voltage. Q11 (Figure 7) provides circuit protection from signals that are negative with respect to ground.

FIGURE 10 — A BASIC OPERATIONAL AMPLIFIER

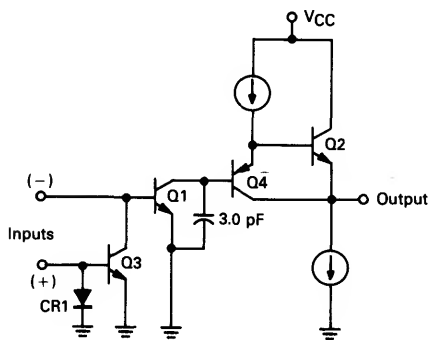
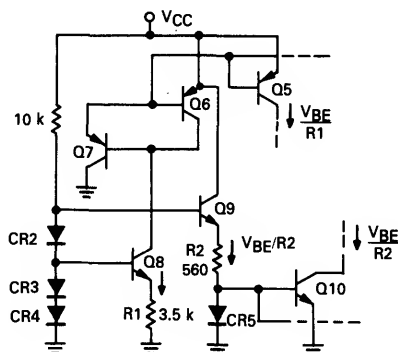


FIGURE 11 — BIASING CIRCUITRY



NORMAL DESIGN PROCEDURE

1. Output Q-Point Biasing

A. A number of techniques may be devised to bias the quiescent output voltage to an acceptable level. However, in terms of loop gain considerations it is usually desirable to use the noninverting input to effect the biasing; as shown in Figures 12 and 13 (see the first page of this specification). The high impedance of the collector of the noninverting "current mirror" transistor helps to achieve the maximum loop gain for any particular configuration. It is desirable that the noninverting input current be in the 10 μ A to 200 μ A range.

B. V_{CC} Reference Voltage (see Figures 12 and 13)

The noninverting input is normally returned to the V_{CC} voltage (which should be well filtered) through a resistor, R_f , allowing the input current, I_{in}^+ , to be within the range of 10 μ A to 200 μ A.

Choosing the feedback resistor, R_f , to be equal to $\frac{1}{2} R_f$ will now bias the amplifier output dc level to approximately $\frac{V_{CC}}{2}$. This allows the maximum dynamic range of the output voltage.

C. Reference Voltage other than V_{CC} (see Figure 14)

The biasing resistor R_f may be returned to a voltage (V_r) other than V_{CC} . By setting $R_f = R_r$ (still keeping I_{in}^+ between 10 μ A and 200 μ A) the output dc level will be equal to V_r . The expression for determining V_{Odc} is:

$$V_{Odc} = \frac{(A_i)(V_r)(R_f)}{R_r} + \left(1 - \frac{R_f}{R_r} A_i\right) \phi$$

where ϕ is the V_{BE} drop of the input transistors (approximately 0.6 Vdc @ +25°C and assumed equal). A_i is the current mirror gain.

FIGURE 12 — INVERTING AMPLIFIER

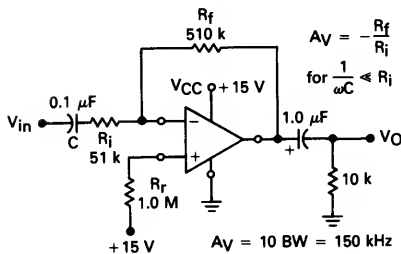
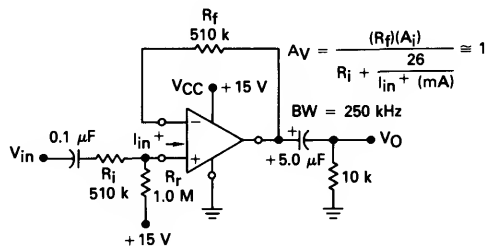


FIGURE 13 — NONINVERTING AMPLIFIER



2. Gain Determination

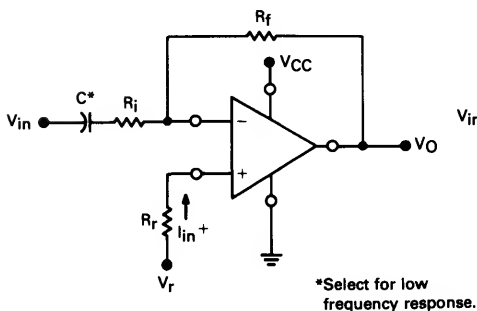
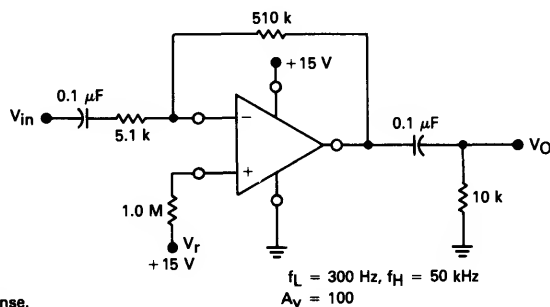
A. Inverting Amplifier

The amplifier is normally used in the inverting mode. The input may be capacitively coupled to avoid upsetting the dc bias and the output is normally capacitively coupled to eliminate the dc voltage across the load. Note that when the output is capacitively coupled to the load, the value of I_{sink} becomes a limitation with respect to the load driving capabilities of the device. The limitation is less severe if the device is direct coupled. In this configuration, the ac gain is determined by the ratio of R_f to R_i , in the same manner as for a conventional operational amplifier:

$$A_V = \frac{R_f}{R_i}$$

The lower corner frequency is determined by the coupling capacitors to the input and load resistors. The upper corner frequency will usually be determined by the amplifier internal compensation. The amplifier unity gain bandwidth is typically 4.0 MHz and with the gain roll-off at 20 dB per decade, bandwidth will typically be 400 kHz with 20 dB of closed-loop gain or 40 kHz with 40 dB of closed-loop gain. The exception to this occurs at low gains where the input resistor selected is large. The pole formed by the amplifier input capacitance, stray capacitance and the input resistor may occur before the closed-loop gain intercepts the open-loop response curve. The inverting input capacity is typically 3.0 pF.

FIGURE 14 — INVERTING AMPLIFIER WITH ARBITRARY REFERENCE


FIGURE 15 — INVERTING AMPLIFIER WITH $A_V = 100$ AND $V_r = V_{CC}$


2

B. Noninverting Amplifier

These devices may be used in the noninverting mode (see Figure 13). The amplifier gain in this configuration is subject to the current mirror gain. In addition, the resistance of the input diode must be included in the value of the input resistor. This resistance is approximately $\frac{26}{I_{in}^+}$ ohms, where I_{in}^+ is input current in milliamperes. The non-inverting ac gain expression is given by:

$$A_v = \frac{(R_f)(A_i)}{R_i + \frac{26}{I_{in}^+ (mA)}}$$

The bandwidth of the noninverting configuration for a given R_f value is essentially independent of the gain chosen. For $R_f = 510 \text{ k}\Omega$ the bandwidth will be in excess of 200 kHz for noninverting gains of 1, 10, or 100. This is a result of the loop gain remaining constant for these gains since the input resistor is effectively isolated from the feedback loop.

TYPICAL APPLICATIONS

FIGURE 16 — TACHOMETER CIRCUIT

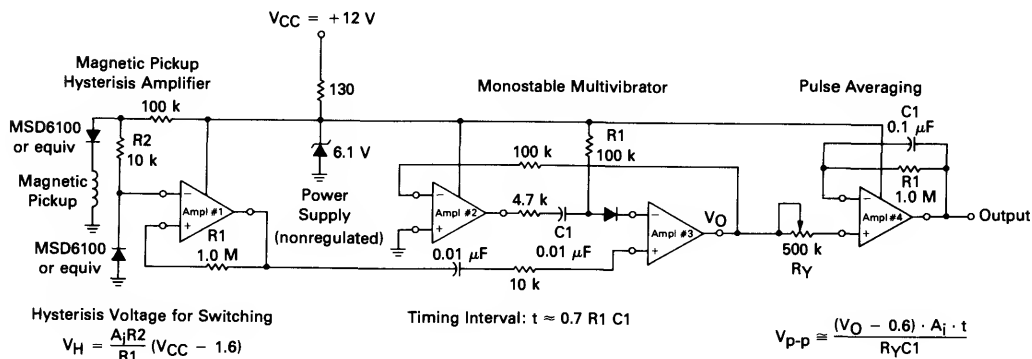
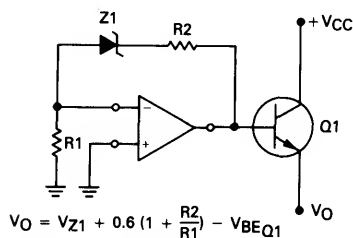
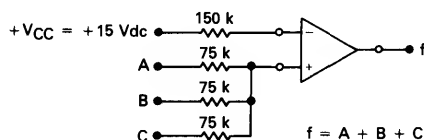


FIGURE 17 — VOLTAGE REGULATOR



NOTE:
For positive T_C zeners R2 and R1 can be selected to give T_C output.

FIGURE 18 — LOGIC "OR" GATE



TYPICAL APPLICATIONS (continued)

FIGURE 19 — LOGIC "NAND" GATE (Large Fan-In)

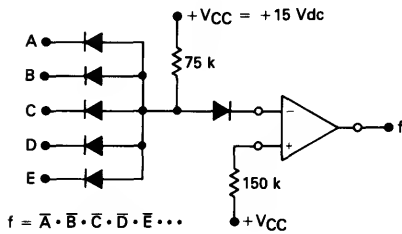


FIGURE 20 — LOGIC "NOR" GATE

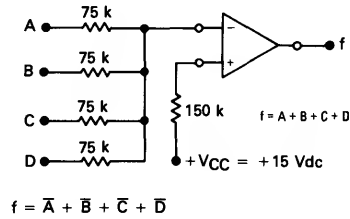


FIGURE 21 — R-S FLIP-FLOP

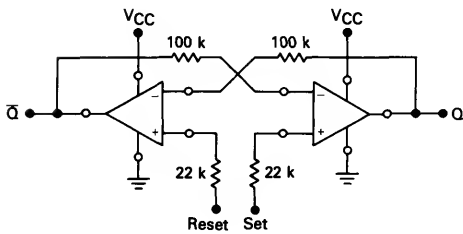


FIGURE 23 — POSITIVE-EDGE DIFFERENTIATOR

Output Rise Time ≈ 0.22 ms
Input Change Time Constant ≈ 1.0 ms

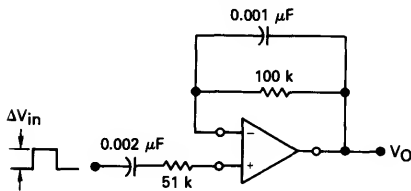


FIGURE 22 — ASTABLE MULTIVIBRATOR

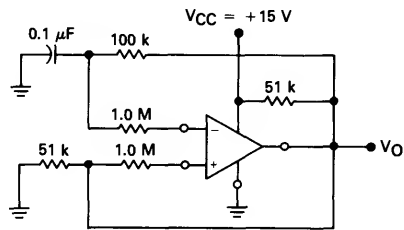


FIGURE 24 — NEGATIVE-EDGE DIFFERENTIATOR

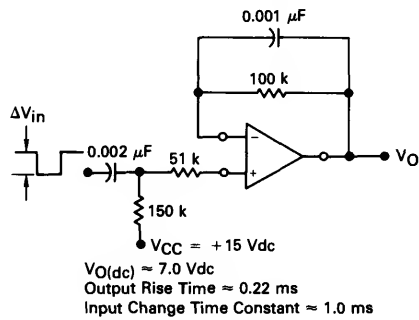


FIGURE 25 — AMPLIFIER AND DRIVER FOR A 50-OHM LINE

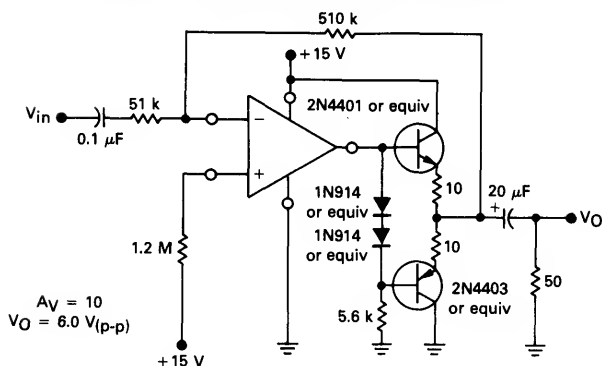


FIGURE 26 — BASIC BANDPASS AND NOTCH FILTER

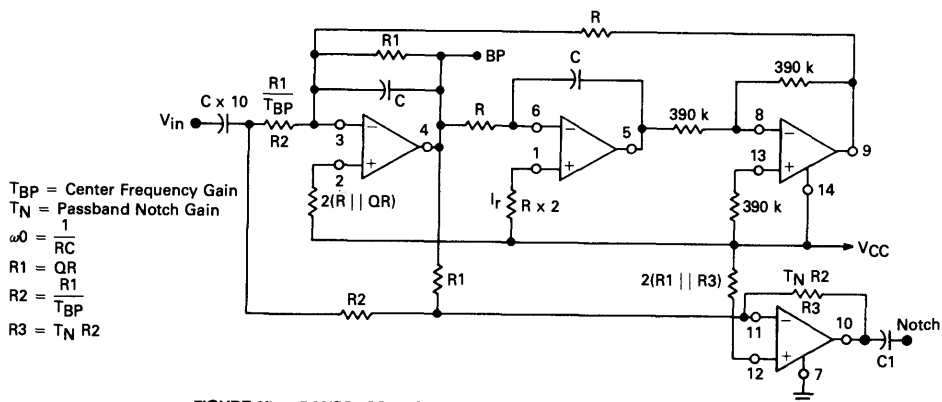
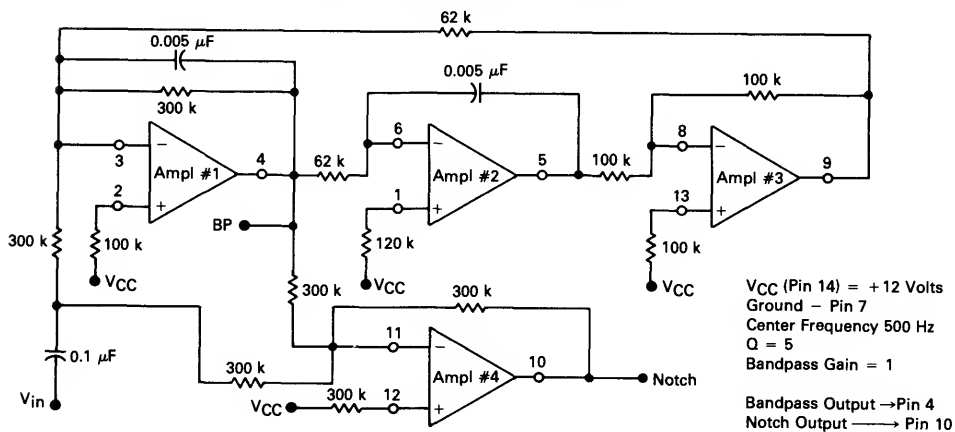
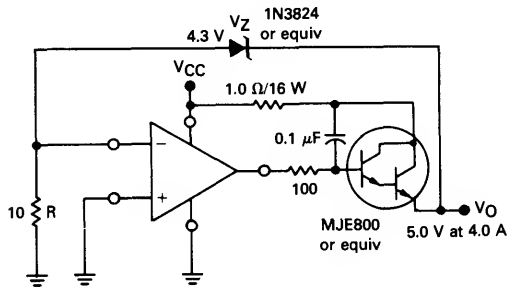


FIGURE 27 — BANDPASS AND NOTCH FILTER



TYPICAL APPLICATIONS (continued)

FIGURE 28 — VOLTAGE REGULATOR

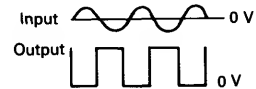
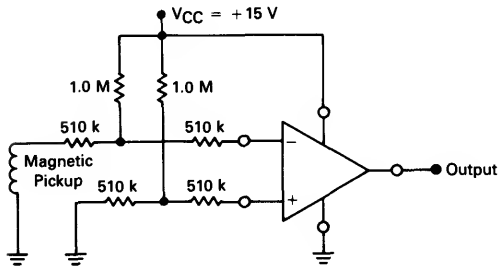


$$V_O = V_Z + 0.6 \text{ Vdc}$$

NOTE 1: R is used to bias the zener.

NOTE 2: If the Zener TC is positive, and equal in magnitude to the negative TC of the input to the operational amplifier ($\approx 2.0 \text{ mV}/^\circ\text{C}$), the output is zero-TC. A 7.0 Volt Zener will give approximately zero-TC.

FIGURE 29 — ZERO CROSSING DETECTOR



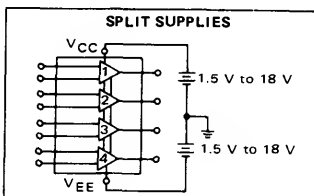
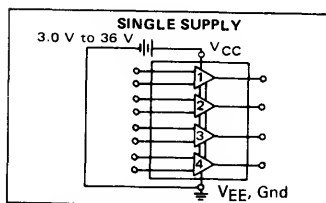
MOTOROLA SEMICONDUCTOR TECHNICAL DATA

2

QUAD LOW POWER OPERATIONAL AMPLIFIERS

The MC3503 is a low-cost, quad operational amplifier with true differential inputs. The device has electrical characteristics similar to the popular MC1741. However, the MC3503 has several distinct advantages over standard operational amplifier types in single supply applications. The quad amplifier can operate at supply voltages as low as 3.0 Volts or as high as 36 Volts with quiescent currents about one third of those associated with the MC1741 (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

- Short Circuit Protected Outputs
- Class AB Output Stage for Minimal Crossover Distortion
- True Differential Input Stage
- Single Supply Operation: 3.0 to 36 Volts
- Split Supply Operation: ± 1.5 to ± 18 Volts
- Low Input Bias Currents: 500 nA Max
- Four Amplifiers Per Package
- Internally Compensated
- Similar Performance to Popular MC1741
- Industry Standard Pinouts



MAXIMUM RATINGS

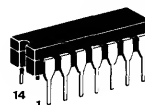
Rating	Symbol	Value	Unit
Power Supply Voltages			Vdc
Single Supply	VCC	36	
Split Supplies	VCC	+18	
	VEE	-18	
Input Differential Voltage Range (1)	V _{IDR}	± 36	Vdc
Input Common Mode Voltage Range (1) (2)	V _{ICR}	± 18	Vdc
Storage Temperature Range	T _{stg}	-65 to +150	°C
		-55 to +125	
Operating Ambient Temperature Range	T _A	-55 to +125	°C
		0 to +70	
		-40 to +85	
Junction Temperature	T _J	175	°C
		150	

(1) Split Power Supplies.
(2) For Supply Voltages less than ± 18 V, the absolute maximum input voltage is equal to the supply voltage.

MC3403
MC3503
MC3303

QUAD DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

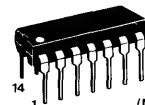
SILICON MONOLITHIC
INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 632

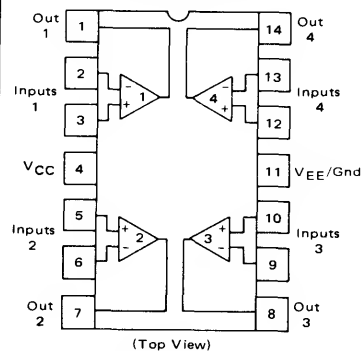


D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)



P SUFFIX
PLASTIC PACKAGE
CASE 646
(MC3403 and MC3303 Only)

PIN CONNECTIONS



ORDERING INFORMATION

Type	Temperature Range	Package
MC3303D	-40°C to +85°C	SO-14
MC3303L		Ceramic DIP
MC3303P		Plastic DIP
MC3403D	0°C to +70°C	SO-14
MC3403L		Ceramic DIP
MC3403P		Plastic DIP
MC3503L	-55°C to +125°C	Ceramic DIP

MC3403, MC3503, MC3303

ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$ for MC3503, MC3403; $V_{CC} = +14\text{ V}$, $V_{EE} = \text{Gnd}$ for MC3303.
 $T_A = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	MC3503			MC3403			MC3303			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage $T_A = T_{\text{high}} \text{ to } T_{\text{low}} \text{ (1)}$	V_{IO}	—	2.0	5.0	—	2.0	10	—	2.0	8.0	mV
Input Offset Current $T_A = T_{\text{high}} \text{ to } T_{\text{low}}$	I_{IO}	—	30	50	—	30	50	—	30	75	nA
Large Signal Open-Loop Voltage Gain $V_O = \pm 10\text{ V}$, $R_L = 2.0\text{ k}\Omega$, $T_A = T_{\text{high}} \text{ to } T_{\text{low}}$	A_{VOL}	50	200	—	20	200	—	20	200	—	V/mV
Input Bias Current $T_A = T_{\text{high}} \text{ to } T_{\text{low}}$	I_{IB}	—	-200	-500	—	-200	-500	—	-200	-500	nA
Output Impedance $f = 20\text{ Hz}$	z_o	—	75	—	—	75	—	—	75	—	Ω
Input Impedance $f = 20\text{ Hz}$	z_i	0.3	1.0	—	0.3	1.0	—	0.3	1.0	—	M Ω
Output Voltage Range $R_L = 10\text{ k}\Omega$, $R_L = 2.0\text{ k}\Omega$, $R_L = 2.0\text{ k}\Omega$, $T_A = T_{\text{high}} \text{ to } T_{\text{low}}$	V_{OR}	± 12 ± 10 ± 10	± 13.5 ± 13 —	— — —	± 12 ± 10 ± 10	± 13.5 ± 13 —	— — —	+12 +10 +10	+12.5 +12 —	— — —	V
Input Common-Mode Voltage Range	V_{ICR}	+13 V - V_{EE}	+13.5 V - V_{EE}	—	+13 V - V_{EE}	+13.5 V - V_{EE}	—	+12 V - V_{EE}	+12.5 V - V_{EE}	—	V
Common-Mode Rejection Ratio $R_S < 10\text{ k}\Omega$	CMRR	70	90	—	70	90	—	70	90	—	dB
Power Supply Current ($V_O = 0$) $R_L = \infty$	I_{CC}, I_{EE}	—	2.8	4.0	—	2.8	7.0	—	2.8	7.0	mA
Individual Output Short-Circuit Current (2)	I_{OS+}	± 10	± 30	± 45	± 10	± 20	± 45	± 10	± 30	± 45	mA
Positive Power Supply Rejection Ratio	PSRR+	—	30	150	—	30	150	—	30	150	$\mu\text{V/V}$
Negative Power Supply Rejection Ratio	PSRR-	—	30	150	—	30	150	—	—	—	$\mu\text{V/V}$
Average Temperature Coefficient of Input Offset Current $T_A = T_{\text{high}} \text{ to } T_{\text{low}}$	$\Delta I_{IO}/\Delta T$	—	50	—	—	50	—	—	50	—	$\text{pA}/^\circ\text{C}$
Average Temperature Coefficient of Input Offset Voltage $T_A = T_{\text{high}} \text{ to } T_{\text{low}}$	$\Delta V_{IO}/\Delta T$	—	10	—	—	10	—	—	10	—	$\mu\text{V}/^\circ\text{C}$
Power Bandwidth $A_V = 1$, $R_L = 2.0\text{ k}\Omega$, $V_O = 20\text{ V(p-p)}$, THD = 5%	BWp	—	9.0	—	—	9.0	—	—	9.0	—	kHz
Small-Signal Bandwidth $A_V = 1$, $R_L = 10\text{ k}\Omega$, $V_O = 50\text{ mV}$	BW	—	1.0	—	—	1.0	—	—	1.0	—	MHz
Slew Rate $A_V = 1$, $V_i = -10\text{ V to } +10\text{ V}$	SR	—	0.6	—	—	0.6	—	—	0.6	—	V/ μs
Rise Time $A_V = 1$, $R_L = 10\text{ k}\Omega$, $V_O = 50\text{ mV}$	t_{RLH}	—	0.35	—	—	0.35	—	—	0.35	—	μs
Fall Time $A_V = 1$, $R_L = 10\text{ k}\Omega$, $V_O = 50\text{ mV}$	t_{RHL}	—	0.35	—	—	0.35	—	—	0.35	—	μs
Overshoot $A_V = 1$, $R_L = 10\text{ k}\Omega$, $V_O = 50\text{ mV}$	OS	—	20	—	—	20	—	—	20	—	%
Phase Margin $A_V = 1$, $R_L = 2.0\text{ k}\Omega$, $C_L = 200\text{ pF}$	ϕ_m	—	60	—	—	60	—	—	60	—	degrees
Crossover Distortion ($V_{in} = 30\text{ mVp-p}$, $V_{out} = 2.0\text{ Vp-p}$, $f = 10\text{ kHz}$)	—	—	1.0	—	—	1.0	—	—	1.0	—	%

(1) $T_{\text{high}} = 125^\circ\text{C}$ for MC3503, 70°C for MC3403, 85°C for MC3303

$T_{\text{low}} = -55^\circ\text{C}$ for MC3503, 0°C for MC3403, -40°C for MC3303

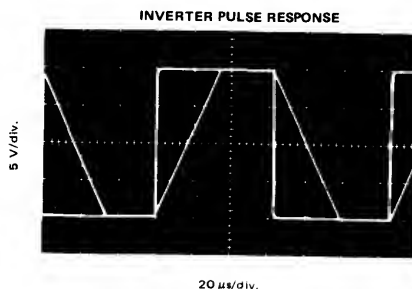
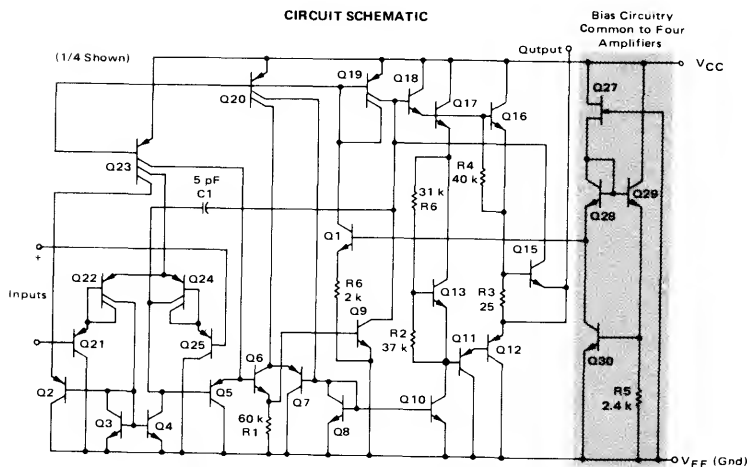
ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0\text{ V}$, $V_{EE} = \text{Gnd}$, $T_A = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	MC3503			MC3403			MC3303			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	—	2.0	5.0	—	2.0	10	—	—	10	mV
Input Offset Current	I_{IO}	—	30	50	—	30	50	—	—	75	nA
Input Bias Current	I_{IB}	—	-200	-500	—	-200	-500	—	—	-500	nA
Large-Signal Open-Loop Voltage Gain $R_L = 2.0\text{ k}\Omega$	A_{VOL}	10	200	—	10	200	—	10	200	—	V/mV
Power Supply Rejection Ratio	PSRR	—	—	150	—	—	150	—	—	150	$\mu\text{V/V}$
Output Voltage Range (3) $R_L = 10\text{ k}\Omega$, $V_{CC} = 5.0\text{ V}$, $R_L = 10\text{ k}\Omega$, $5.0\text{ V} < V_{CC} < 30\text{ V}$	V_{OR}	3.3 $V_{CC} - 2.0$	3.5 $V_{CC} - 1.7$	—	3.3 $V_{CC} - 2.0$	3.5 $V_{CC} - 1.7$	—	3.3 $V_{CC} - 2.0$	3.5 $V_{CC} - 1.7$	—	Vp-p
Power Supply Current	I_{CC}	—	2.5	4.0	—	2.5	7.0	—	2.5	7.0	mA
Channel Separation $f = 1.0\text{ kHz to } 20\text{ kHz}$ (Input Referenced)	—	—	-120	—	—	-120	—	—	-120	—	dB

(2) Not to exceed maximum package power dissipation.

(3) Output will swing to ground

2



CIRCUIT DESCRIPTION

The MC3503/3403/3303 is made using four internally compensated, two-stage operational amplifiers. The first stage of each consists of differential input devices Q24 and Q22 with input buffer transistors Q25 and Q21 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance a smaller compensation capacitor (only 5 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q24 and Q22. Another feature of this input stage is that the input common-mode range can include

the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single-ended converter. The second stage consists of a standard current source load amplifier stage.

The output stage is unique because it allows the output to swing to ground in single supply operation and yet does not exhibit any crossover distortion in split supply operation. This is possible because class AB operation is utilized.

Each amplifier is biased from an internal-voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

MC3403, MC3503, MC3303

TYPICAL PERFORMANCE CURVES

FIGURE 1 – SINE WAVE RESPONSE

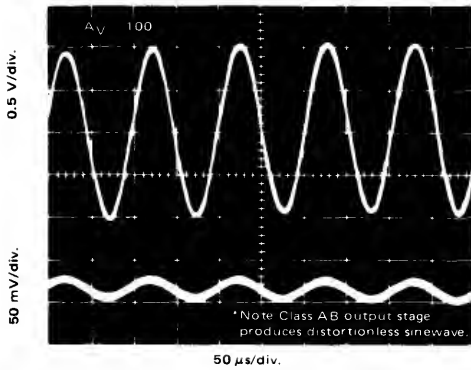


FIGURE 2 – OPEN LOOP FREQUENCY RESPONSE

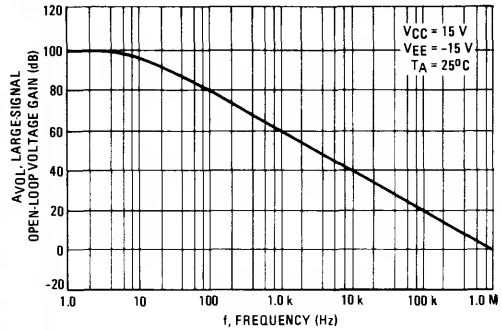


FIGURE 3 – POWER BANDWIDTH

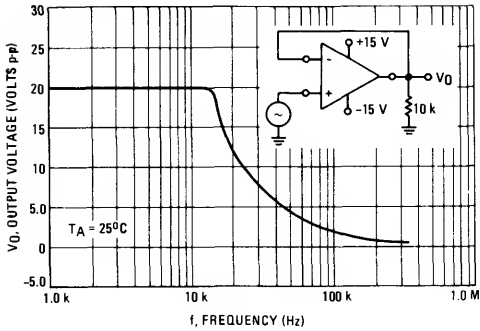


FIGURE 4 – OUTPUT SWING versus SUPPLY VOLTAGE

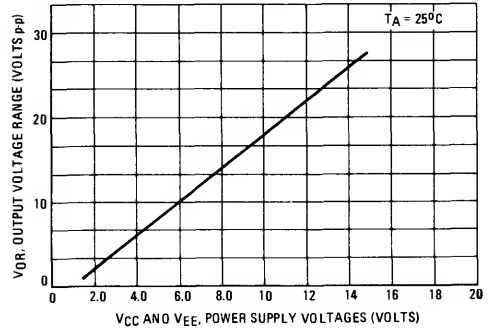


FIGURE 5 – INPUT BIAS CURRENT versus TEMPERATURE

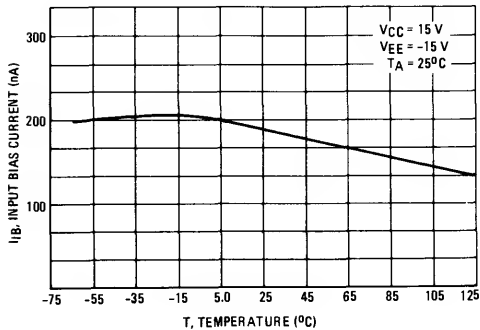
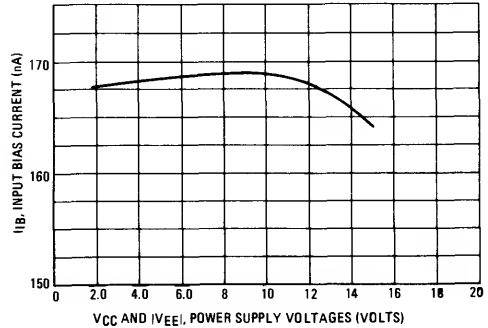


FIGURE 6 – INPUT BIAS CURRENT versus SUPPLY VOLTAGE



MC3403, MC3503, MC3303

APPLICATIONS INFORMATION

2

FIGURE 7 - VOLTAGE REFERENCE

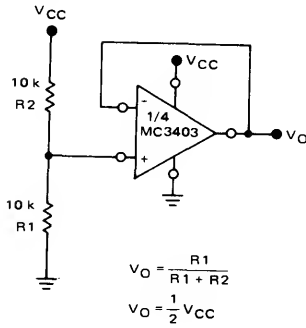


FIGURE 8 - WIEN BRIDGE OSCILLATOR

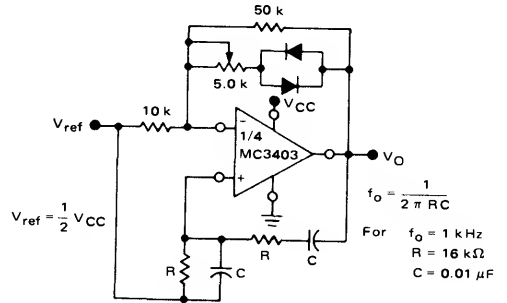


FIGURE 9 - HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER

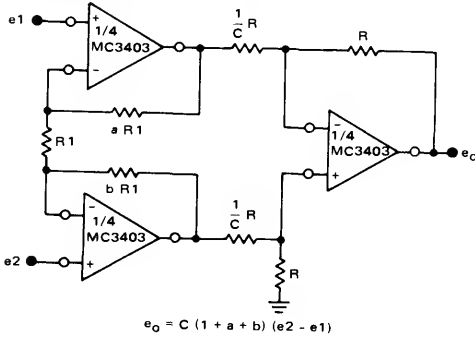


FIGURE 10 - COMPARATOR WITH HYSTERESIS

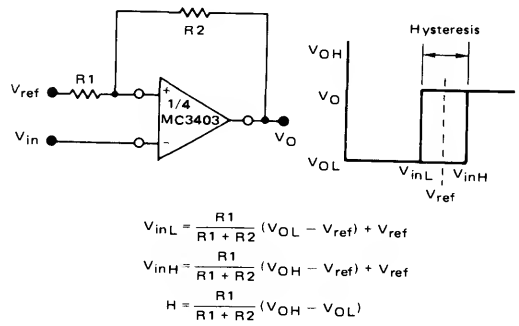
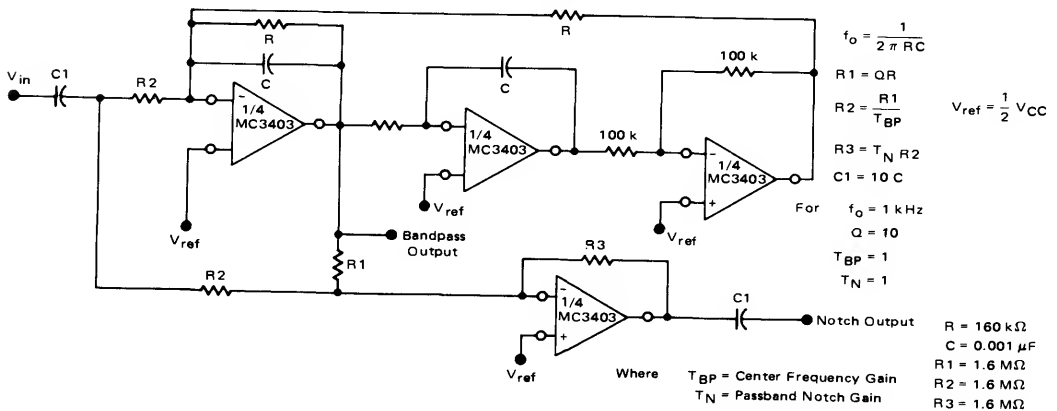


FIGURE 11 - BI-QUAD FILTER



MC3403, MC3503, MC3303

FIGURE 12 – FUNCTION GENERATOR

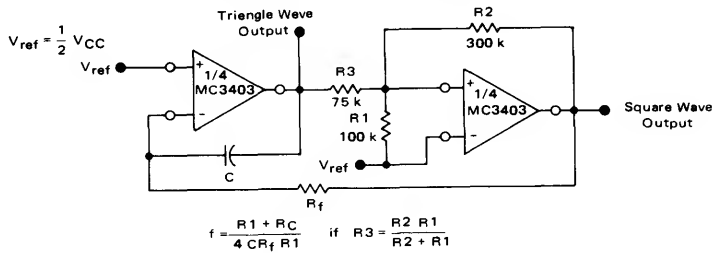
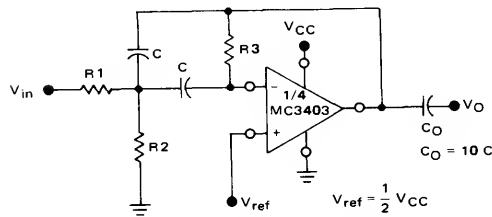


FIGURE 13 – MULTIPLE FEEDBACK BANDPASS FILTER



Given f_0 = Center Frequency
 $A(f_0)$ = Gain at Center Frequency

Choose Value f_0, C

Then:

$$R3 = \frac{O}{\pi f_0 C}$$

$$R1 = \frac{R3}{2 A(f_0)}$$

$$R2 = \frac{R1 R5}{4Q^2 R1 - R5}$$

For less than 10% error from operational amplifier

$$\frac{Q_0 f_0}{BW} < 0.1 \quad \text{Where } f_0 \text{ and } BW \text{ are expressed in Hz.}$$

If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

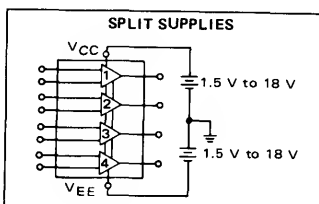
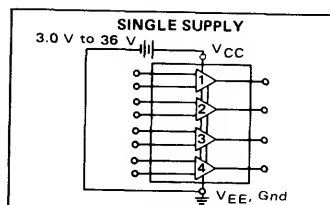
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DUAL OPERATIONAL AMPLIFIER AND DUAL COMPARATOR

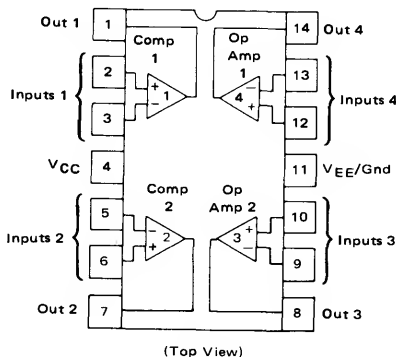
The MC3405/3505 contains two differential-input operational amplifiers and two comparators, each set capable of single supply operation. This operational amplifier-comparator circuit fulfills its applications as a general purpose product for automotive and consumer circuits as well as an industrial building block.

The MC3405 is specified over the commercial operating temperature range of 0 to +70°C, while the MC3505 is specified over the military operating range of -55 to +125°C.

- Operational Amplifiers Equivalent in Performance to MC3403/3503
- Comparators Similar in Performance to LM339/139
- Single Supply Operation: 3.0 to 36 Volts
- Split Supply Operation: ± 1.5 to ± 18 Volts
- Low Supply Current Drain
- Operational Amplifiers Are Internally Frequency Compensated
- Comparators TTL and CMOS Compatible



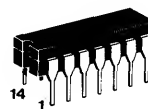
PIN CONNECTIONS



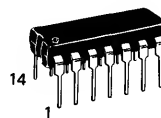
**MC3405
MC3505**

DUAL OPERATIONAL AMPLIFIER AND DUAL VOLTAGE COMPARATOR

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

Device	Temperature Range	Package
MC3405L	0 to +70°C	Ceramic DIP
MC3405P	0 to +70°C	Plastic DIP
MC3505L	-55 to +125°C	Ceramic DIP

MC3405, MC3505

OPERATIONAL AMPLIFIER SECTION

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage—Single Supply Split Supplies	V_{CC} V_{CC}, V_{EE}	36 ± 18	Vdc
Input Differential Voltage Range	V_{IDR}	± 36	Vdc
Input Common Mode Voltage Range	V_{ICR}	± 18	Vdc
Operating Ambient Temperature Range—MC3505 MC3405	T_A	-55 to +125 0 to +70	$^{\circ}\text{C}$
Storage Temperature Range—Ceramic Package Plastic Package	T_{stg}	-65 to +150 -55 to +125	$^{\circ}\text{C}$
Operating Junction Temperature Range—Ceramic Package Plastic Package	T_J	175 150	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0\text{ V}$, $V_{EE} = \text{Gnd}$, $T_A = 25^{\circ}\text{C}$ unless otherwise noted)

Characteristic	Symbol	MC3505			MC3405			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	—	2.0	5.0	—	2.0	10	mV
Input Offset Current	I_{IO}	—	30	50	—	30	50	nA
Input Bias Current	I_{IB}	—	-200	-500	—	-200	-500	nA
Large-Signal Open-Loop Voltage Gain ($R_L = 2.0\text{ k}\Omega$)	A_{VOL}	20	200	—	20	200	—	V/mV
Power Supply Rejection Ratio	PSRR	—	—	150	—	—	150	$\mu\text{V/V}$
Output Voltage Range (Note 1) ($R_L = 10\text{ k}\Omega$, $V_{CC} = 5.0\text{ V}$) ($R_L = 10\text{ k}\Omega$, $5.0\text{ V} < V_{CC} \leq 30\text{ V}$)	V_{OR}	3.3 $V_{CC} - 2.0$	3.5 $V_{CC} - 1.7$	—	3.3 $V_{CC} - 2.0$	3.5 $V_{CC} - 1.7$	—	Vp-p
Power Supply Current (Notes 2 and 3)	I_{CC}	—	2.5	4.0	—	2.5	7.0	mA
Channel Separation $f = 1.0\text{ kHz}$ to 20 kHz (Input Referenced)	—	—	-120	—	—	-120	—	dB

ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = 25^{\circ}\text{C}$ unless otherwise noted)

Input Offset Voltage ($T_A = T_{\text{low}}$ to T_{high}) (Note 4)	V_{IO}	—	2.0	5.0	—	2.0	10	mV
Average Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	—	15	—	—	15	—	$\mu\text{V}/^{\circ}\text{C}$
Input Offset Current ($T_A = T_{\text{low}}$ to T_{high}) (Note 4)	I_{IO}	—	—	50	—	—	50	nA
Input Bias Current ($T_A = T_{\text{low}}$ to T_{high}) (Note 4)	I_{IB}	—	-200	-500	—	-200	-500	nA
Input Common Mode Voltage Range	V_{ICR}	+13 - V_{EE}	—	—	+13 - V_{EE}	—	—	Vdc
Large Signal Open Loop Voltage Gain ($V_O = \pm 10\text{ V}$, $R_L = 2.0\text{ k}\Omega$) ($T_A = T_{\text{low}}$ to T_{high}) (Note 4)	A_{VOL}	50 25	200 100	—	20 15	200 100	—	V/mV
Common Mode Rejection Ratio	CMRR	70	90	—	70	90	—	dB
Power Supply Rejection Ratio	PSRR	—	30	150	—	30	150	$\mu\text{V/V}$
Output Voltage ($R_L = 10\text{ k}\Omega$) ($R_L = 2.0\text{ k}\Omega$) ($R_L = 2.0\text{ k}\Omega$, $T_A = T_{\text{low}}$ to T_{high}) (Note 4)	V_O	± 12 ± 10 ± 10	± 13.5 ± 13 —	—	± 12 ± 10 ± 10	± 13.5 ± 13 —	—	Vdc
Output Short-Circuit Current	I_{OS}	± 10	± 30	± 45	± 10	± 20	± 45	mA
Power Supply Current (Notes 2 and 3)	I_{CC}, I_{EE}	—	2.8	4.0	—	2.8	7.0	mA
Phase Margin	ϕ_m	—	60	—	—	60	—	Degrees
Small-Signal Bandwidth ($A_V = 1$, $R_L = 10\text{ k}\Omega$, $V_O = 50\text{ mV}$)	BW	—	1.0	—	—	1.0	—	MHz
Power Bandwidth ($A_V = 1$, $R_L = 2.0\text{ k}\Omega$, $V_O = 20\text{ V}$ (p-p), THD = 5%)	BWp	—	9.0	—	—	9.0	—	kHz
Rise Time/Fall Time	t_{RLH}, t_{FHL}	—	0.35	—	—	0.35	—	μs
Overshoot ($A_V = 1$, $R_L = 10\text{ k}\Omega$, $V_O = 50\text{ mV}$)	OS	—	20	—	—	20	—	%
Slew Rate	SR	—	0.6	—	—	0.6	—	V/ μs

- NOTES: 1. Output will swing to ground.
2. Not to exceed maximum package power dissipation.
3. For Operational Amplifier and Comparator.

4. $T_{\text{low}} = -55^{\circ}\text{C}$ for MC3505 $T_{\text{high}} = +125^{\circ}\text{C}$ for MC3505
 $= 0^{\circ}\text{C}$ for MC3405 $= +70^{\circ}\text{C}$ for MC3405

MC3405, MC3505

COMPARATOR SECTION

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage—Single Supply	V_{CC}	36	Vdc
Split Supplies	V_{CC}, V_{EE}	± 18	
Input Differential Voltage Range	V_{IDR}	± 36	Vdc
Input Common Mode Voltage Range	V_{ICR}	-0.3 to +36	Vdc
Sink Current	I_{sink}	20	mA
Operating Ambient Temperature Range—MC3505 MC3405	T_A	-55 to +125 0 to +70	$^{\circ}C$
Storage Temperature Range—Ceramic Package Plastic Package	T_{stg}	-65 to +150 -55 to +125	$^{\circ}C$
Operating Junction Temperature Range—Ceramic Package Plastic Package	T_J	175 150	$^{\circ}C$

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0$ V, $V_{EE} = \text{Gnd}$, $T_A = 25^{\circ}C$ unless otherwise noted)

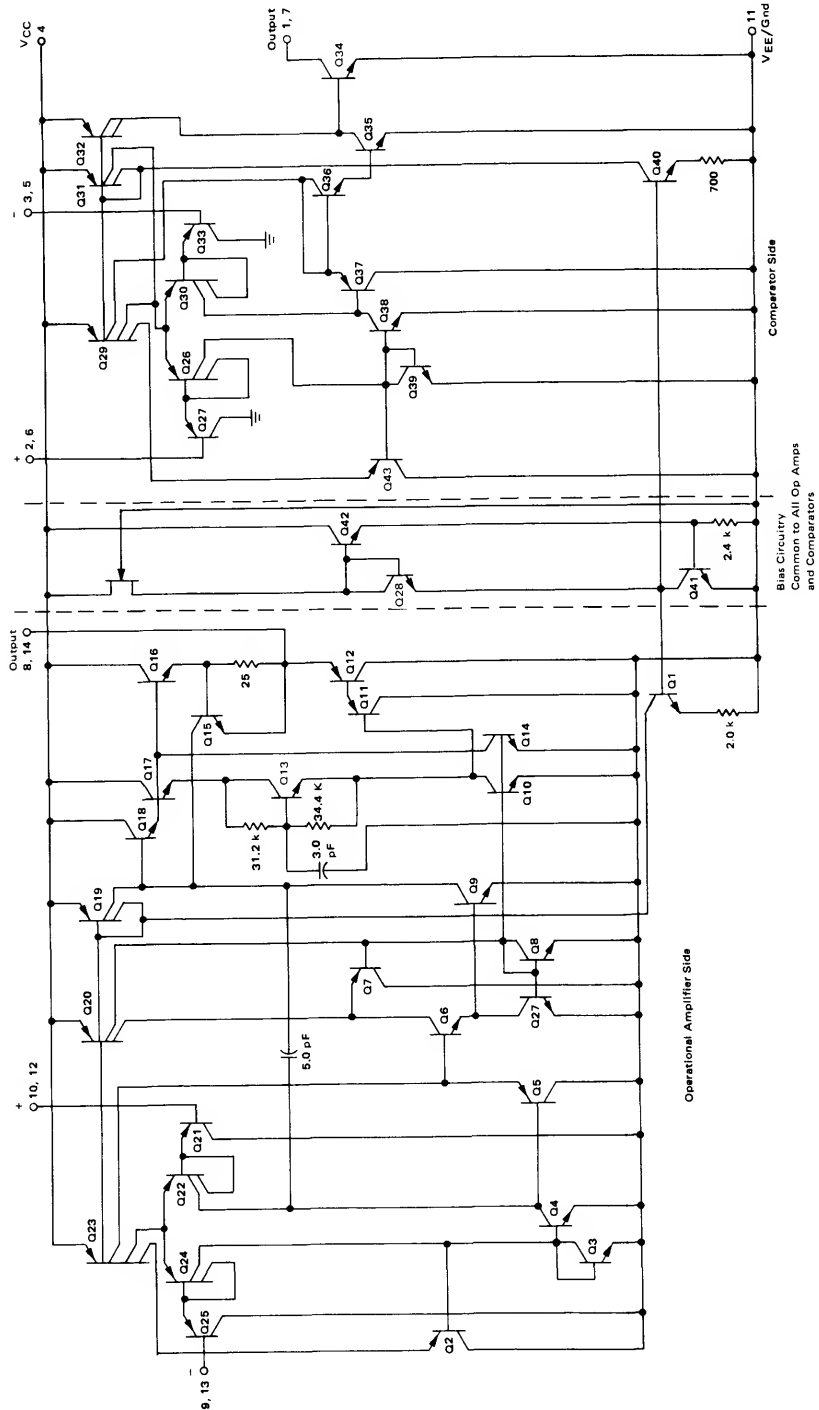
Characteristic	Symbol	MC3505			MC3405			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($T_A = T_{low}$ to T_{high}) (Notes 1 and 2)	V_{IO}	—	2.0	5.0 9.0	—	2.0	10 12	mV
Average Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	—	15	—	—	15	—	$\mu V/^{\circ}C$
Input Offset Current ($T_A = T_{low}$ to T_{high}) (Note 1)	I_{IO}	—	50	75 150	—	50	100 200	nA
Input Bias Current ($T_A = T_{low}$ to T_{high}) (Note 1)	I_{IB}	—	-125	-500 -1500	—	-125	-500 -800	nA
Input Common Mode Voltage Range ($T_A = T_{low}$ to T_{high}) (Note 1)	V_{ICR}	0	$V_{CC} - 1.5$ $V_{CC} - 1.7$	$V_{CC} - 1.7$ $V_{CC} - 2.0$	0	$V_{CC} - 1.5$ $V_{CC} - 1.7$	$V_{CC} - 1.7$ $V_{CC} - 2.0$	Vp-p
Input Differential Voltage (All $V_{in} \geq 0$ Vdc)	V_{ID}	—	—	36	—	—	36	V
Large-Signal Open-Loop Voltage Gain ($R_L = 15$ k Ω)	A_{VOL}	—	200	—	—	200	—	V/mV
Output Sink Current ($V_{in} (-) \geq 1.0$ Vdc, $V_{in} (+) = 0$, $V_O \leq 1.5$ V)	I_{sink}	6.0	16	—	6.0	16	—	mA
Low Level Output Voltage ($V_{in} (+) = 0$ V, $V_{in} (-) = 1.0$ V, $I_{sink} = 4.0$ mA) ($T_A = T_{low}$ to T_{high}) (Note 1)	V_{OL}	—	350	500 700	—	350	500 700	mV
Output Leakage Current ($V_{in} (+) \geq 1.0$ Vdc, $V_{in} (-) = 0$, $V_O = 5.0$ Vdc) ($T_A = T_{low}$ to T_{high}) (Note 1)	I_{OL}	—	0.1 0.1	1.0 1.0	—	0.1 0.1	1.0 1.0	μA
Large-Signal Response	—	—	300	—	—	300	—	ns
Response Time (Note 3) ($V_{RL} = 5.0$ Vdc, $R_L = 5.1$ k Ω)	—	—	1.3	—	—	1.3	—	μs

NOTES: 1. $T_{low} = -55^{\circ}C$ for MC3505 $T_{high} = +125^{\circ}C$ for MC3505
 $= 0^{\circ}C$ for MC3405 $= +70^{\circ}C$ for MC3405

- $V_O \geq 1.4$ V, $R_S = 0$ Ω with V_{CC} from 5.0 Vdc to 30 Vdc, and over the input common mode range 0 to $V_{CC} - 1.7$ V.
- The response time specified is for a 100 mV input step with 5.0 mV overdrive. For larger signals 300 ns is typical.

MC3405, MC3505

CIRCUIT SCHEMATIC
(1/2 OF CIRCUIT SHOWN)



MC3405, MC3505

OPERATIONAL AMPLIFIER SECTION TYPICAL PERFORMANCE CURVES

2

FIGURE 1 — SINE WAVE RESPONSE

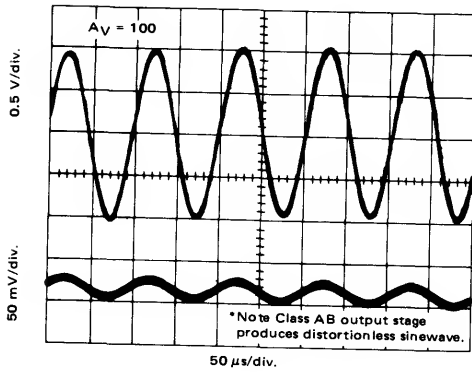


FIGURE 2 — OPEN LOOP FREQUENCY RESPONSE

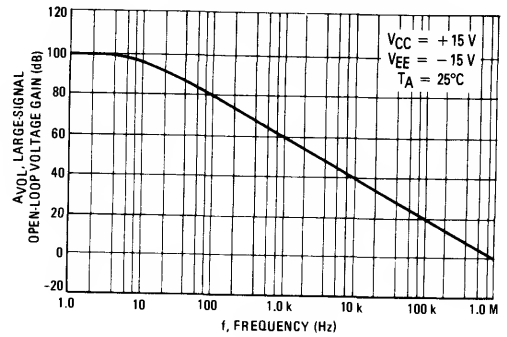


FIGURE 3 — POWER BANDWIDTH

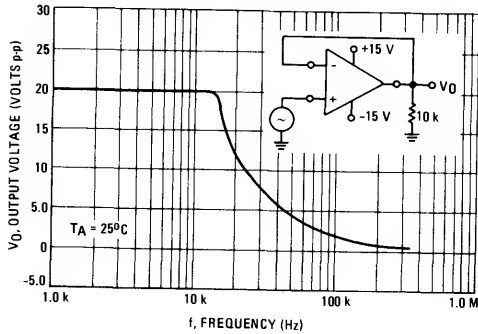


FIGURE 4 — OUTPUT SWING versus SUPPLY VOLTAGE

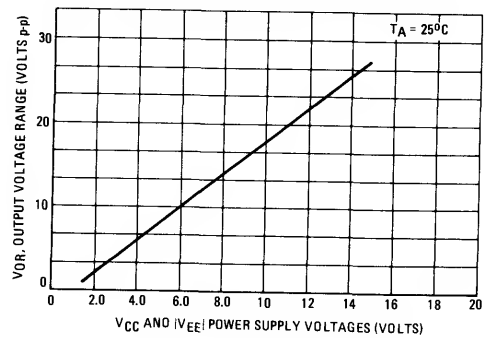


FIGURE 5 — INPUT BIAS CURRENT versus TEMPERATURE

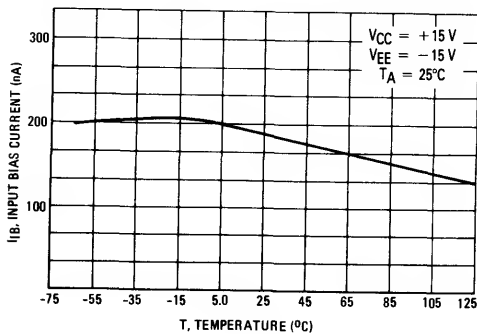


FIGURE 6 — INPUT BIAS CURRENT versus SUPPLY VOLTAGE

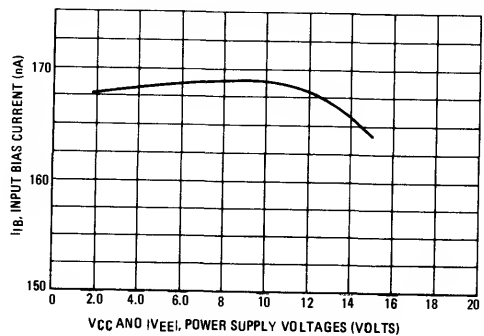


FIGURE 12 – WINDOW COMPARATOR

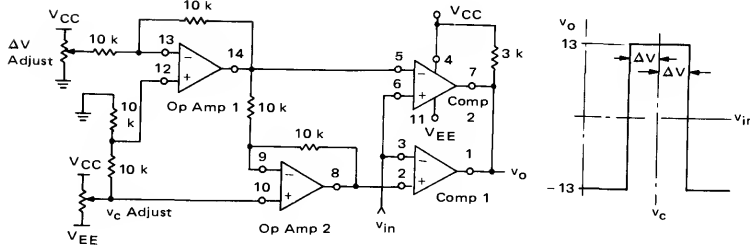


FIGURE 13 – SQUELCH CIRCUIT FOR AM OR FM

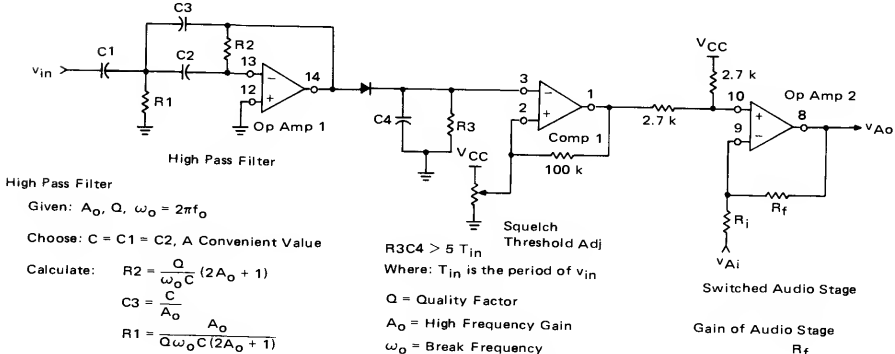


FIGURE 14 – HIGH/LOW LIMIT ALARM

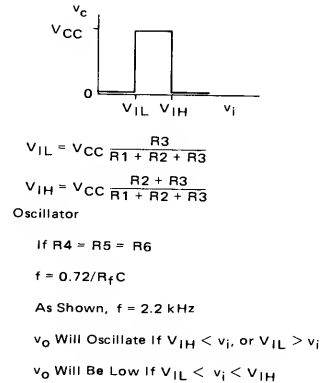
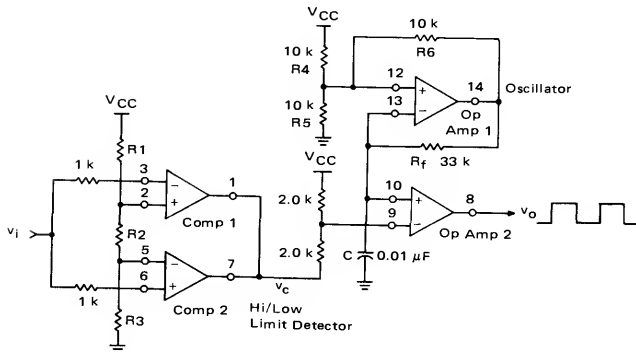


FIGURE 15 – ZERO CROSSING DETECTOR WITH TEMPERATURE SENSOR

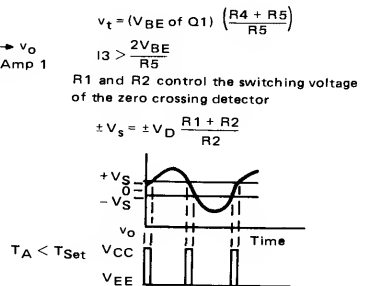
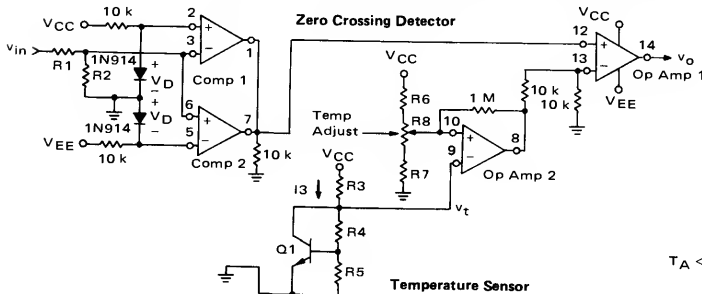
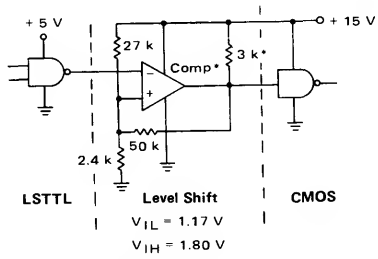
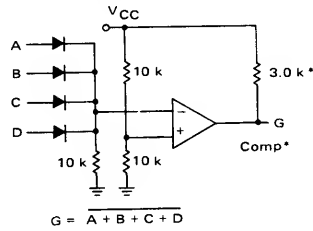


FIGURE 16 – LSTTL to CMOS INTERFACE WITH HYSTERESIS



*The same configuration may be used with an Op Amp if the 3 k resistor is removed.

FIGURE 17 – "NOR" GATE



*The same configuration may be used with an Op Amp if the 3 k resistor is removed.

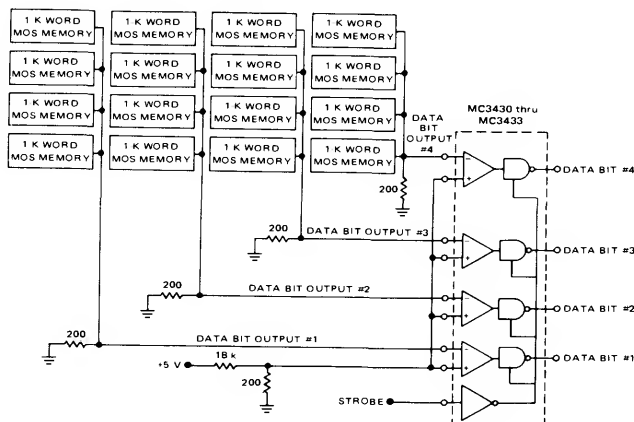
QUAD DIFFERENTIAL VOLTAGE COMPARATOR/SENSE AMPLIFIERS

The MC3430 thru MC3433 high-speed comparators are ideal for application as sense amplifiers in MOS memory systems. They are specified in a unique way which combines the effects of input offset voltage, input offset current, voltage gain, temperature variations and input common-mode range into a single functional parameter. This parameter, called Input Sensitivity, specifies a minimum differential input voltage which will guarantee a given logic state. Four variations are offered in the comparator series.

The MC3430 and MC3431 versions feature a three-state strobe input common to all four channels which can be used to place the four outputs in a high-impedance state. These two devices use active-pull-up MTTL compatible outputs. The MC3432 and MC3433 are open-collector types which permit the implied AND connection. The MC3430 and MC3432 versions are specified for a ± 7.0 mV input sensitivity over the 0 to 70°C temperature range, while the MC3431 and MC3433 are specified for ± 12 mV.

- Propagation Delay Time – 40 ns
- Outputs Specified for a Fanout of 10 (MC7400 type loads)
- Specified for all conditions of $\pm 5\%$ Power Supply Variations, Operating Temperature Range, Input Common-Mode Voltage Swing from -3.0 V to 3.0 V, and $R_S \leq 200$ ohms.

**FIGURE 1 – A TYPICAL MOS MEMORY SENSING APPLICATION FOR A
4-K WORD BY 4-BIT MEMORY ARRANGEMENT EMPLOYING
1103 TYPE MEMORY DEVICES**



Only four devices are required for a
4-k word by 16-bit memory system.

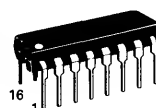
MC3430 thru MC3433

QUAD HIGH SPEED VOLTAGE COMPARATORS

SILICON MONOLITHIC
INTEGRATED CIRCUITS

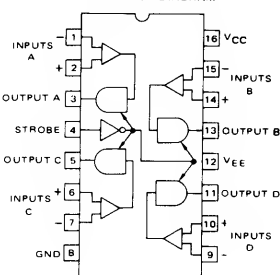


L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

CONNECTION DIAGRAM



TRUTH TABLE
MC3430 and MC3432

Input	Strobe	Output	Device
$V_{ID} \geq 7.0$ mV	L	H	MC3430
	H	Z	
$T_A = 0$ to 70°C	L	Off	MC3432
	H	Off	
-7.0 mV $\leq V_{ID}$	L	L	MC3430
≤ 7.0 mV	L	I	MC3432
$T_A = 0$ to 70°C	L	Off	MC3430
	H	Z	
$V_{ID} \leq -7.0$ mV	L	On	MC3432
$T_A = 0$ to 70°C	H	Off	

TRUTH TABLE
MC3431 and MC3433

Input	Strobe	Output	Device
$V_{ID} \geq 12$ mV	L	H	MC3431
	H	Z	
$T_A = 0$ to 70°C	L	Off	MC3433
	H	Off	
-12 mV $\leq V_{ID}$	L	L	MC3431
$\leq +12$ mV	L	Z	
$T_A = 0$ to 70°C	H	Off	MC3433
	L	L	
$V_{ID} \leq -12$ mV	L	L	MC3431
	H	Z	
$T_A = 0$ to 70°C	L	On	MC3433
	H	Off	

L = Low Logic State Z = Third (High Impedance)
H = High Logic State I = Indeterminate State
 $R_S \leq 200 \Omega$

MC3430 thru MC3433

2

MAXIMUM RATINGS ($T_A = 0$ to $+70^\circ\text{C}$ unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}, V_{EE}	± 7.0	Vdc
Differential Mode Input Signal Voltage Range	V_{IDR}	± 6.0	Vdc
Common-Mode Input Voltage Range	V_{ICR}	± 5.0	Vdc
Strobe Input Voltage	$V_{I(S)}$	5.5	Vdc
Output Voltage (MC3432 — 33 versions)	V_O	+7.0	Vdc
Junction Temperature	T_J	175	$^\circ\text{C}$
Ceramic Package		150	
Plastic Package			
Operating Temperature Range	T_A	0 to +70	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS ($T_A = 0$ to $+70^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltages	V_{CC}, V_{EE}	+4.75 -4.75	+5.0 -5.0	+5.25 -5.25	Vdc
Output Load Current	I_{OL}	—	—	16	mA
Differential-Mode Input Voltage Range	V_{IDR}	-5.0	—	+5.0	Vdc
Common-Mode Input Voltage Range	V_{ICR}	-3.0	—	+3.0	Vdc
Input Voltage Range (any input to Ground)	V_{IR}	-5.0	—	+3.0	Vdc

ELECTRICAL CHARACTERISTICS ($V_{CC} = +5.0$ Vdc, $V_{EE} = -5.0$ Vdc, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ unless otherwise noted.) Typical Values are Measured at $T_A = 25^\circ\text{C}$

Characteristic	Symbol	MC3430, MC3431			MC3432, MC3433			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Sensitivity (See Discussion on Page 3) ($R_S \leq 200$ Ohms) (Common Mode Voltage Range = $-3.0\text{ V} \leq V_{in} \leq 3.0\text{ V}$) $4.75 \leq V_{CC} \leq 5.25\text{ V}$ } MC3430, MC3432 $-4.75 \geq V_{EE} \geq -5.25\text{ V}$ } MC3431, MC3433 $T_A = 25^\circ\text{C}$ (Common Mode Voltage Range = $-3.0\text{ V} \leq V_{in} \leq 3.0\text{ V}$) $4.75 \leq V_{CC} \leq 5.25\text{ V}$ } MC3430, MC3432 $-4.75 \geq V_{EE} \geq -5.25\text{ V}$ } MC3431, MC3433 $T_A = 0$ to 70°C	V_{IS}	—	—	± 6.0 ± 10	—	—	± 6.0 ± 10	mV
Input Offset Voltage ($R_S \leq 200$ Ohms)	V_{IO}	—	2.0	—	—	2.0	—	mV
Input Bias Current ($V_{CC} = 5.25\text{ V}$, $V_{EE} = -5.25\text{ V}$)	I_{IB}	—	20	40	—	20	40	μA
Input Offset Current	I_{IO}	—	1.0	—	—	1.0	—	μA
Voltage Gain	A_{vol}	—	1200	—	—	1200	—	V/V
Strobe Input Voltage (Low State)	$V_{IL(S)}$	—	—	0.8	—	—	0.8	V
Strobe Input Voltage (High State)	$V_{IH(S)}$	2.0	—	—	2.0	—	—	V
Strobe Current (Low State) ($V_{CC} = 5.25\text{ V}$, $V_{EE} = -5.25\text{ V}$, $V_{in} = 0.4\text{ V}$)	$I_{IL(S)}$	—	—	-1.6	—	—	-1.6	mA
Strobe Current (High State) ($V_{CC} = 5.25\text{ V}$, $V_{EE} = -5.25\text{ V}$, $V_{in} = 2.4\text{ V}$) ($V_{CC} = 5.25\text{ V}$, $V_{EE} = -5.25\text{ V}$, $V_{in} = 5.25\text{ V}$)	$I_{IH(S)}$	—	—	40 1.0	—	—	40 1.0	μA mA
Output Voltage (High State) ($I_O = -400\text{ }\mu\text{A}$, $V_{CC} = 4.75\text{ V}$, $V_{EE} = -4.75\text{ V}$)	V_{OH}	2.4	—	—	—	—	—	V
Output Voltage (Low State) ($I_O = 16\text{ mA}$, $V_{CC} = 4.75\text{ V}$, $V_{EE} = 4.75\text{ V}$)	V_{OL}	—	—	0.4	—	—	0.4	V
Output Leakage Current ($V_{CC} = 4.75\text{ V}$, $V_{EE} = -4.75\text{ V}$, $V_O = 5.25\text{ V}$)	I_{CEX}	—	—	—	—	—	250	μA
Output Current Short Circuit ($V_{CC} = 5.25\text{ V}$, $V_{EE} = -5.25\text{ V}$)	I_{os}	-18	—	-70	—	—	—	mA
Output Disable Leakage Current ($V_{CC} = 5.25\text{ V}$, $V_{EE} = -5.25\text{ V}$)	I_{off}	—	—	40	—	—	—	μA
High Logic Level Supply Currents ($V_{CC} = 5.25\text{ V}$, $V_{EE} = -5.25\text{ V}$)	I_{CC} I_{EE}	— —	45 -17	60 -30	— —	45 -17	60 -30	mA mA

A UNIQUE FUNCTIONAL PARAMETER FOR COMPARATORS

2

A unique approach is used in specifying the MC3430-33 quad comparators. Previously, comparators have been specified as linear devices with common operational amplifier type parameters such as voltage gain (A_{VOL}), input offset voltage (V_{IO}), input offset current (I_{IO}) and common-mode rejection ratio (CMRR). This is true despite the fact that most comparators are seldom operated in their linear region because it is difficult to hold a high gain comparator in this narrow region. Comparators are normally used to "detect" when an unknown voltage level exceeds a given reference voltage.

The most desirable comparator parameter is what minimum differential input voltage is required at the comparator's input terminals to guarantee a given output logic state. This new and important parameter has been called input sensitivity (V_{IS}) and is analogous to the input threshold voltage specification on a core memory sense amplifier. The input sensitivity specification includes the effects of voltage gain, input offset voltage and input offset current and eliminates the need for specifying these three parameters.

In order to make this parameter as inclusive as possible on the MC3430-33 series quad comparators, the input sensitivity is specified within the following conditions:

Commercial Temperature Range — 0 to 70°C
Power Supply Variations — $\pm 5\%$ (all conditions)
Input Source Resistance — ≤ 200 Ohms
Common-Mode Voltage Range — -3.0 V to +3.0 V

Note: Typical values have been included on the omitted parameters for applications where the offset voltages are externally nulled.

Voltage gain is defined as the ratio of the resulting ΔV_O to a change in the V_{IDR} using conditions at which the V_{IO} and I_{IO} are nulled. Thus, for worst case M TTL logic levels, the required output voltage change is 2.0 V (V_{OHmin} — V_{OLmax} = 2.4 V —

0.4 V). If 2.0 mV are required at the input terminals to induce this change in logic state, the voltage gain would be 1000 V/V.

Gain however is not the only factor affecting the logic transition. Normally input offset voltages, that are not externally nulled, can add an appreciable error that drastically overshadows the comparator gain. Therefore, the 2.0 mV for example, required to cause the logic transition is often masked. An input offset voltage of up to 7.5 mV might be required to reach the linear region. A further consideration is the input offset current of up to ± 10 μA flowing through the matched 200-Ohm source resistors at the input terminals which can create an additional error of ± 2.0 mV. In order to determine a worst case input sensitivity, it must be assumed that minimum specified gain and maximum specified offset voltage and current conditions exist. Also it must be assumed that these three factors are cumulative, requiring a worst case input of:

Logic Transition = 2.0 mV

V_{IO} = 7.5 mV

I_{IO} of ± 10 μA thru 200-Ohm resistor = 2.0 mV

Therefore, $2 + 7.5 + 2 = 11.5$ mV.

The effects of power supply voltage variations, temperature changes and common-mode input voltage conditions have not been considered, as they are not present in the gain and offset specifications on most comparators.

Thus, the input sensitivity specification greatly reduces the effort required in determining the worst case differential voltage required by a given comparator type.

Table I compares the worst case input sensitivity of three popular comparator types at both room temperature and over the specified commercial temperature range (0 to 70°C). This sensitivity was computed from the specified voltage gain, offset voltage and offset current limits.

TABLE I — WORST CASE COMPARISONS

Type Number	$T_A = 25^{\circ}\text{C}$						$T_A = 0 \text{ to } 70^{\circ}\text{C}$					
	V_{IO} mV Max	A_{vol}^* V/V Typ	Differential Input Voltage Required for 3.0 V Output Change	I_{IO} μA Max	Error Voltage Generated into 200 Ω Source Resistors	Total Sensitivity mV	V_{IO} mV Max	A_{vol}^* V/V Typ	Differential Input Voltage Required for 3.0 V Output Change	I_{IO} μA Max	Error Voltage Generated into 200 Ω Source Resistors	Total Sensitivity mV
MC3430, MC3432	—	—	—	—	—	6.0	—	—	—	—	—	7.0
MC3431, MC3433	—	—	—	—	—	10	—	—	—	—	—	12
MC1711C	5.0	1500	2.0 mV	15	3.0 mV	10	5.0	1000	3.0 mV	25	5.0 mV	13
LM311	7.5	200 k	0.015 mV	6.0**	0.0012 mV	7.516	10	100 k	0.030 mV	70**	0.014 mV	10.04

*Typical values given, as minimum gain not always specified

** I_{IO} measured in nA

FIGURE 2 — GUARANTEED OUTPUT STATE versus DIFFERENTIAL INPUT VOLTAGE

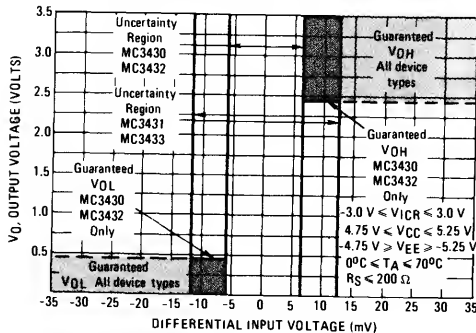
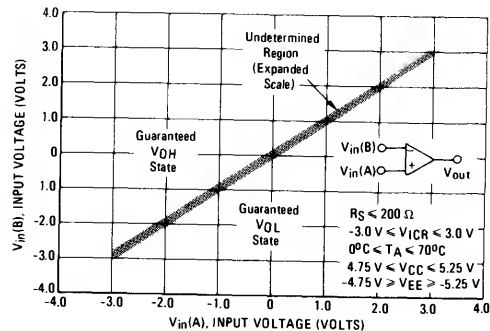


FIGURE 3 — GUARANTEED OUTPUT STATE versus INPUT VOLTAGE



MC3430 thru MC3433

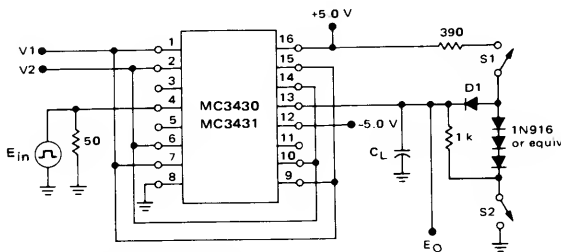
2

SWITCHING CHARACTERISTICS ($V_{CC} = +5.0$ Vdc, $V_{EE} = -5.0$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Fig.	MC3430, MC3431			MC3432, MC3433			Unit
			Min	Typ	Max	Min	Typ	Max	
High to Low Logic Level Propagation Delay Time (Differential Inputs) $5.0\text{ mV} + V_{IS}$	$t_{PHL}(D)$	6,8-11	—	20	45	—	27	50	ns
Low to High Logic Level Propagation Delay Time (Differential Inputs) $5.0\text{ mV} + V_{IS}$	$t_{PLH}(D)$	6,8-11	—	33	55	—	40	65	ns
Open State to High Logic Level Propagation Delay Time (Strobe)	$t_{PZH}(S)$	4	—	—	35	—	—	—	ns
High Logic Level to Open State Propagation Delay Time (Strobe)	$t_{PHZ}(S)$	4	—	—	35	—	—	—	ns
Open State to Low Logic Level Propagation Delay Time (Strobe)	$t_{PZL}(S)$	4	—	—	40	—	—	—	ns
Low Logic Level to Open State Propagation Delay Time (Strobe)	$t_{PLZ}(S)$	4	—	—	35	—	—	—	ns
High Logic to Low Logic Level Propagation Delay Time (Strobe)	$t_{PHL}(S)$	5	—	—	—	—	—	40	ns
Low Logic to High Logic Level Propagation Delay Time (Strobe)	$t_{PLH}(S)$	5	—	—	—	—	—	35	ns

TEST CIRCUITS

FIGURE 4 — STROBE PROPAGATION DELAY TIMES $t_{PLZ}(S)$, $t_{PZL}(S)$, $t_{PHZ}(S)$, and $t_{PZH}(S)$



Output of Channel 8 shown under test, other channels are tested similarly.

	V1	V2	S1	S2	C_L
$t_{PLZ}(S)$	100 mV	GND	Closed	Closed	15 pF
$t_{PZL}(S)$	100 mV	GND	Closed	Open	50 pF
$t_{PHZ}(S)$	GND	100 mV	Closed	Closed	15 pF
$t_{PZH}(S)$	GND	100 mV	Open	Closed	50 pF

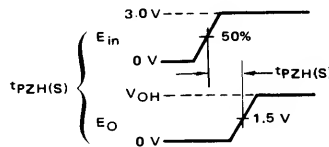
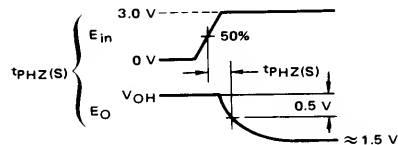
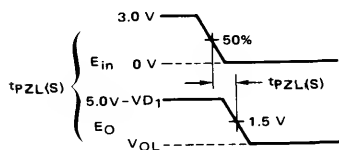
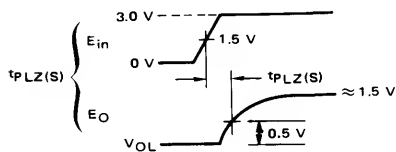
C_L includes jig and probe capacitance.

E_{in} waveform characteristics

t_{PLH} and $t_{PHL} \leq 10$ ns measured 10% to 90%.

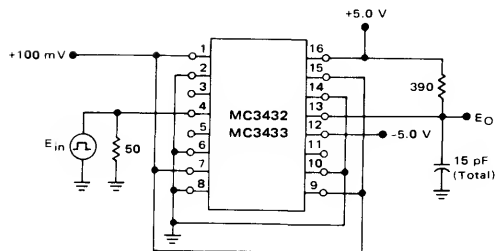
PRR = 1.0 MHz

Duty Cycle = 50%

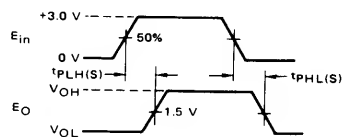


MC3430 thru MC3433

FIGURE 5 – STROBE PROPAGATION DELAY $t_{PLH(S)}$ AND $t_{PHL(S)}$

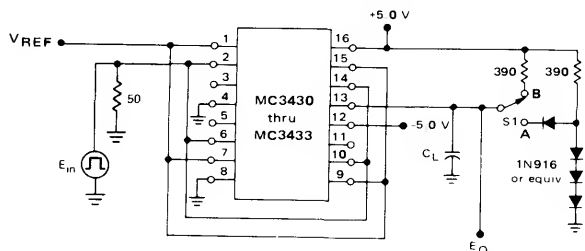


Output of Channel B shown under test, other channels are tested similarly.



E_{in} waveform characteristics:
 t_{PLH} and $t_{PHL} \leq 10$ ns measured 10% to 90%.
 PRR = 1.0 MHz
 Duty Cycle = 50%

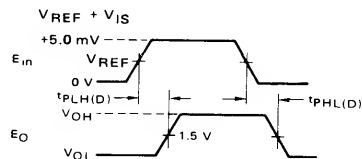
FIGURE 6 – DIFFERENTIAL INPUT PROPAGATION DELAY $t_{PLH(D)}$ AND $t_{PHL(D)}$



Output of Channel B shown under test, other channels are tested similarly

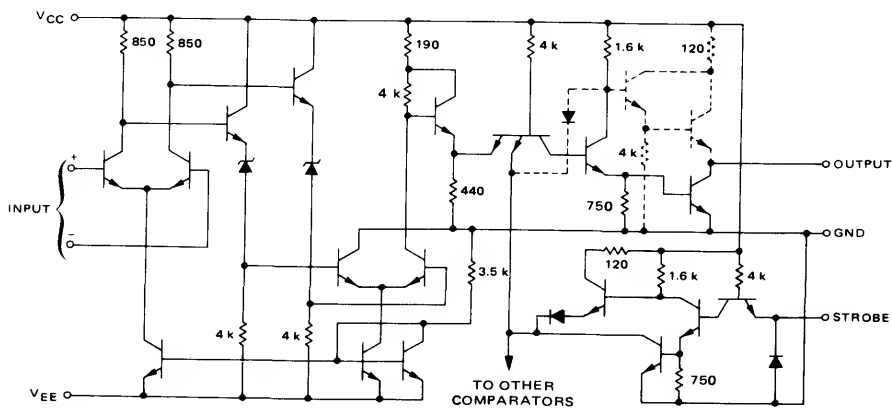
S1 at "A" for MC3430, MC3431
 S1 at "B" for MC3432, MC3433
 $C_L = 50$ pF total for MC3430, MC3431
 $C_L = 15$ pF total for MC3432, MC3433

Device	V_{REF} mV
MC3430	11
MC3431	15
MC3432	11
MC3433	15



E_{in} waveform characteristics:
 t_{PLH} and $t_{PHL} \leq 10$ ns measured 10% to 90%.
 PRR = 1.0 MHz
 Duty Cycle = 50%

FIGURE 7 – CIRCUIT SCHEMATIC
 (1/4 Circuit Shown)



Dashed components apply to the MC3430 and MC3431 circuits only.

MC3430 thru MC3433

TYPICAL PERFORMANCE CURVES

RESPONSE TIME versus OVERDRIVE – MC3430, MC3431

FIGURE 8 – OUTPUT LOW TO HIGH

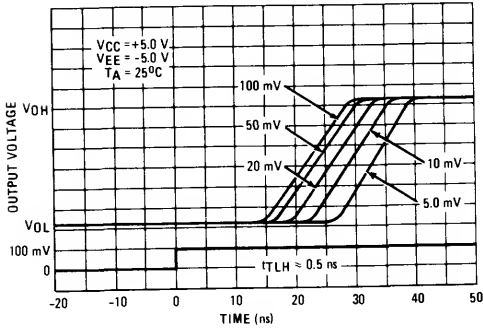
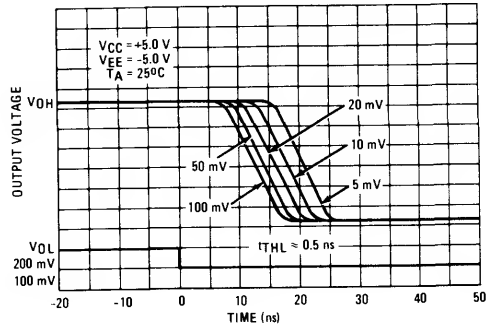


FIGURE 9 – OUTPUT HIGH TO LOW



RESPONSE TIME versus OVERDRIVE – MC3432, MC3433

FIGURE 10 – OUTPUT LOW TO HIGH

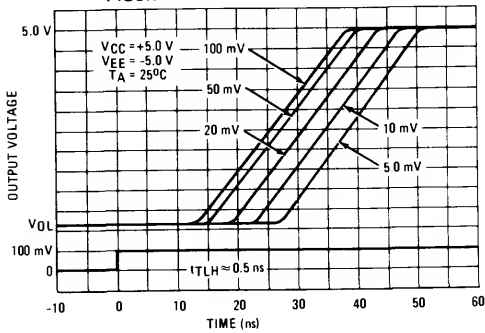


FIGURE 11 – OUTPUT HIGH TO LOW

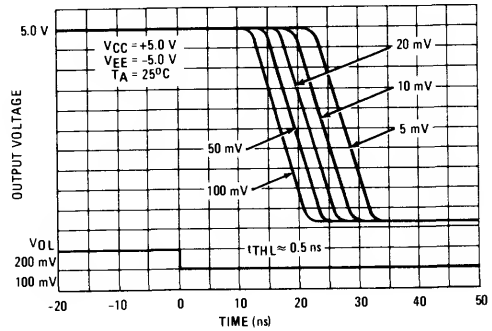


FIGURE 12 – AVERAGE INPUT OFFSET VOLTAGE versus TEMPERATURE

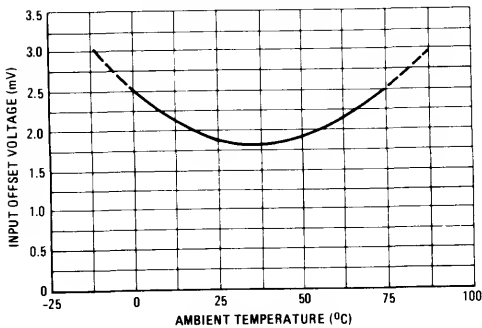
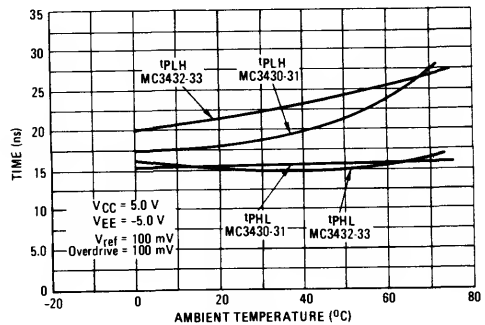


FIGURE 13 – RESPONSE TIME versus TEMPERATURE



APPLICATIONS INFORMATION

FIGURE 14 – 4-BIT PARALLEL A/D CONVERTER

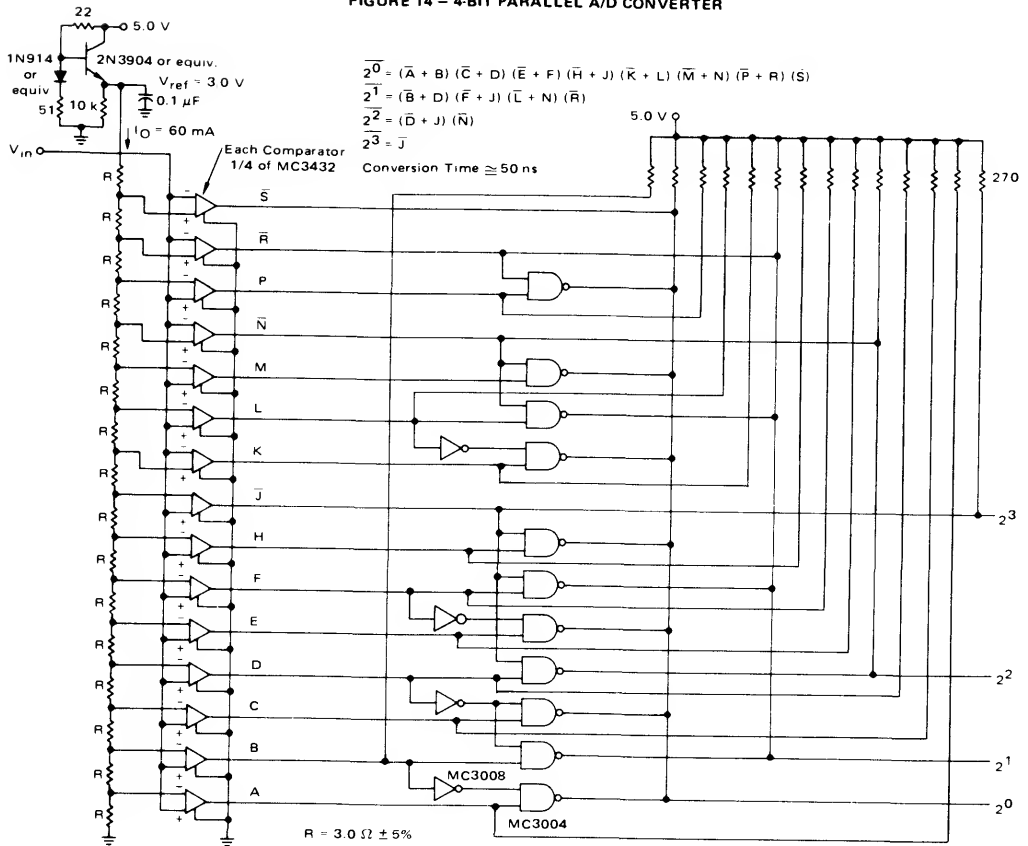


FIGURE 15 – LEVEL DETECTOR WITH HYSTERESIS

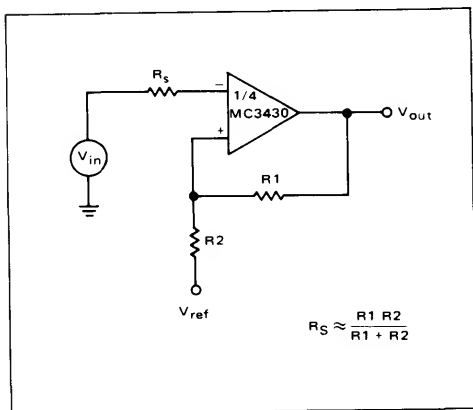


FIGURE 16 – TRANSFER CHARACTERISTICS AND EQUATIONS FOR FIGURE 15

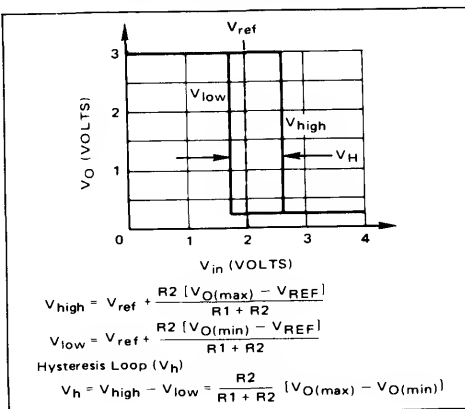


FIGURE 17 – DOUBLE ENDED LIMIT DETECTOR

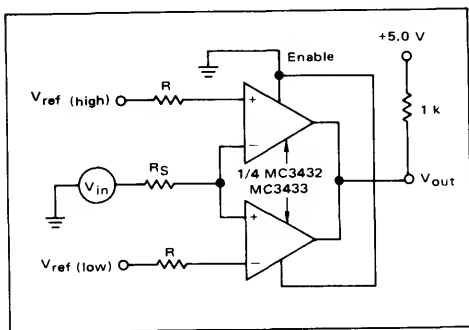
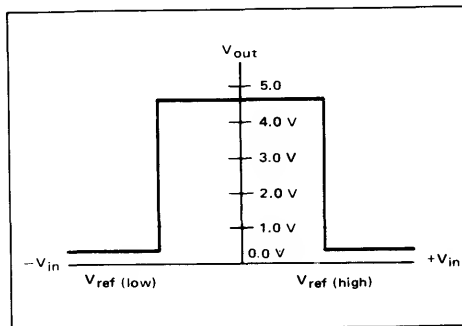


FIGURE 18 – VOLTAGE TRANSFER FUNCTION



DUAL LOW POWER OPERATIONAL AMPLIFIERS

Utilizing the circuit designs perfected for recently introduced Quad Operational Amplifiers, these dual operational amplifiers feature 1) low power drain, 2) a common mode input voltage range extending to ground/V_{EE}, 3) Single Supply or Split Supply operation and 4) pin outs compatible with the popular MC1558 dual operational amplifier. The MC3558 Series is equivalent to one-half of a MC3503.

These amplifiers have several distinct advantages over standard operational amplifier types in single supply applications. They can operate at supply voltages as low as 3.0 Volts or as high as 36 Volts with quiescent currents about one-fifth of those associated with the MC1741 (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

- Short Circuit Protected Outputs
- True Differential Input Stage
- Single Supply Operation: 3.0 to 36 Volts
- Low Input Bias Currents
- Internally Compensated
- Common Mode Range Extends to Negative Supply
- Class AB Output Stage for Minimum Crossover Distortion
- Single and Split Supply Operations Available
- Similar Performance to the Popular MC1558

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltages Single Supply Split Supplies	V _{CC} V _{CC} V _{EE}	36 +18 -18	V _{dc}
Input Differential Voltage Range (1)	V _{IDR}	±30	V _{dc}
Input Common Mode Voltage Range (2)	V _{ICR}	±15	V _{dc}
Input Forward Current (V _I < -0.3 V)	I _{IF}	50	mA
Junction Temperature Ceramic and Metal Packages Plastic Package	T _J	175 150	°C
Storage Temperature Range Ceramic and Metal Packages Plastic Package	T _{stg}	-65 to +150 -55 to +125	°C
Operating Ambient Temperature Range MC3558 MC3458 MC3358	T _A	-55 to +125 0 to +70 -40 to +85	°C

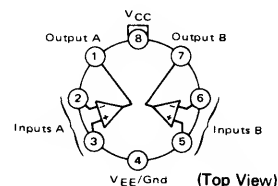
NOTES:

- (1) Split Power Supplies.
- (2) For Supply Voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

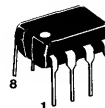
MC3458
MC3558
MC3358

DUAL DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

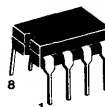
**SILICON MONOLITHIC
INTEGRATED CIRCUIT**



G SUFFIX
METAL PACKAGE
CASE 601



P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MC3458, MC3358 Only)

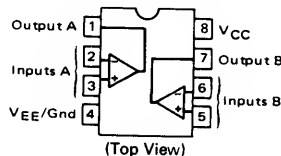


U SUFFIX
CERAMIC PACKAGE
CASE 693



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
MC3358P1	-40°C to +85°C	Plastic DIP
MC3458D	0°C to +70°C	SO-8
MC3458G		Metal Can
MC3458P1		Plastic DIP
MC3458U	-55°C to +125°C	Ceramic DIP
MC3558G		Metal Can
MC3558U		Ceramic DIP

MC3458, MC3558, MC3358

(For MC3558, MC3458, $V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = 25^\circ\text{C}$ unless otherwise noted.) (For MC3358, $V_{CC} = +14\text{ V}$, $V_{EE} = \text{Gnd}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	MC3558			MC3458			MC3358			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage $T_A = \text{High to T}_{\text{low}}$ (1)	V_{IO}	—	2.0	5.0	—	2.0	10	—	2.0	8.0	mV
Input Offset Current $T_A = \text{High to T}_{\text{low}}$	I_{IO}	—	30	50	—	30	50	—	30	75	nA
Input Bias Current $T_A = \text{High to T}_{\text{low}}$	I_{IB}	—	—	200	—	—	200	—	—	250	nA
Large Signal Open-Loop Voltage Gain $V_O = \pm 10\text{ V}$, $R_L = 2.0\text{ k}\Omega$, $T_A = \text{High to T}_{\text{low}}$	A_{VOL}	50	200	—	20	200	—	20	200	—	V/mV
Input Bias Current $T_A = \text{High to T}_{\text{low}}$	I_{IB}	—	—200	—500	—	—200	—500	—	—200	—500	nA
Output Impedance $f = 20\text{ Hz}$	z_o	—	75	—	—	75	—	—	75	—	Ω
Input Impedance $f = 20\text{ Hz}$	z_i	0.3	1.0	—	0.3	1.0	—	0.3	1.0	—	M Ω
Output Voltage Range $R_L = 10\text{ k}\Omega$, $R_L = 2.0\text{ k}\Omega$, $R_L = 2.0\text{ k}\Omega$, $T_A = \text{High to T}_{\text{low}}$	V_{OR}	+12	+13.5	—	+12	+13.5	—	12	12.5	—	V
Input Common-Mode Voltage Range	V_{ICR}	+13 V - V_{EE}	+13.5 V - V_{EE}	—	+13 V - V_{EE}	+13.5 V - V_{EE}	—	+12 V - V_{EE}	+12.5 V - V_{EE}	—	V
Common-Mode Rejection Ratio $R_S \leq 10\text{ k}\Omega$	CMRR	70	90	—	70	90	—	70	90	—	dB
Power Supply Current ($V_O = 0$) $R_L = \infty$	$I_{CC,IEE}$	—	1.6	2.2	—	1.6	3.7	—	1.6	3.7	mA
Individual Output Short-Circuit Current (2)	I_{OS+}	+10	+30	+45	+10	+20	+45	+10	+30	+45	mA
Positive Power Supply Rejection Ratio	PSRR+	—	30	150	—	30	150	—	30	150	$\mu\text{V/V}$
Negative Power Supply Rejection Ratio	PSRR-	—	30	150	—	30	150	—	—	—	$\mu\text{V/V}$
Average Temperature Coefficient of Input Offset Current $T_A = \text{High to T}_{\text{low}}$	I_{IO}/T	—	50	—	—	50	—	—	50	—	pA/ $^\circ\text{C}$
Average Temperature Coefficient of Input Offset Voltage $T_A = \text{High to T}_{\text{low}}$	V_{IO}/T	—	10	—	—	10	—	—	10	—	$\mu\text{V}/^\circ\text{C}$
Power Bandwidth $A_V = 1$, $R_L = 2.0\text{ k}\Omega$, $V_O = 20\text{ V(p-p)}$, THD = 5%	BWp	—	9.0	—	—	9.0	—	—	9.0	—	kHz
Small-Signal Bandwidth $A_V = 1$, $R_L = 10\text{ k}\Omega$, $V_O = 50\text{ mV}$	BW	—	1.0	—	—	1.0	—	—	1.0	—	MHz
Slew Rate $A_V = 1$, $V_i = -10\text{ V to }+10\text{ V}$	SR	—	0.6	—	—	0.6	—	—	0.6	—	V/ μs
Rise Time $A_V = 1$, $R_L = 10\text{ k}\Omega$, $V_O = 50\text{ mV}$	t_{RLH}	—	0.35	—	—	0.35	—	—	0.35	—	μs
Fall Time $A_V = 1$, $R_L = 10\text{ k}\Omega$, $V_O = 50\text{ mV}$	t_{RHL}	—	0.35	—	—	0.35	—	—	0.35	—	μs
Overshoot $A_V = 1$, $R_L = 10\text{ k}\Omega$, $V_O = 50\text{ mV}$	OS	—	20	—	—	20	—	—	20	—	%
Phase Margin $A_V = 1$, $R_L = 2.0\text{ k}\Omega$, $C_L = 200\text{ pF}$	ϕ_m	—	60	—	—	60	—	—	60	—	Degrees
Crossover Distortion ($V_{in} = 30\text{ mV(p-p)}$, $V_{out} = 2.0\text{ V(p-p)}$, $f = 10\text{ kHz}$)	—	—	1.0	—	—	1.0	—	—	1.0	—	%

(1) $T_{\text{High}} = 125^\circ\text{C}$ for MC3558, 70°C for MC3458, 85°C for MC3358
 $T_{\text{low}} = -55^\circ\text{C}$ for MC3558, 0°C for MC3458, -40°C for MC3358

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0\text{ V}$, $V_{EE} = \text{Gnd}$, $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	MC3558			MC3458			MC3358			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	—	2.0	5.0	—	2.0	10	—	2.0	10	mV
Input Offset Current	I_{IO}	—	30	50	—	30	50	—	—	75	nA
Input Bias Current	I_{IB}	—	—200	—500	—	—200	—500	—	—	—500	nA
Large Signal Open-Loop Voltage Gain $R_L = 2.0\text{ k}\Omega$	A_{VOL}	20	200	—	20	200	—	20	200	—	V/mV
Power Supply Rejection Ratio	PSRR	—	—	150	—	—	150	—	—	150	$\mu\text{V/V}$
Output Voltage Range (3) $R_L = 10\text{ k}\Omega$, $V_{CC} = 5.0\text{ V}$, $R_L = 10\text{ k}\Omega$, $5.0\text{ V} < V_{CC} < 30\text{ V}$	V_{OR}	3.3	3.5	—	3.3	3.5	—	3.3	3.5	—	Vp-p
Power Supply Current	I_{CC}	—	2.5	4.0	—	2.5	7.0	—	2.5	4.0	mA
Channel Separation $f = 1.0\text{ kHz to }20\text{ kHz}$ (Input Referenced)	—	—	—120	—	—	—120	—	—	—120	—	dB

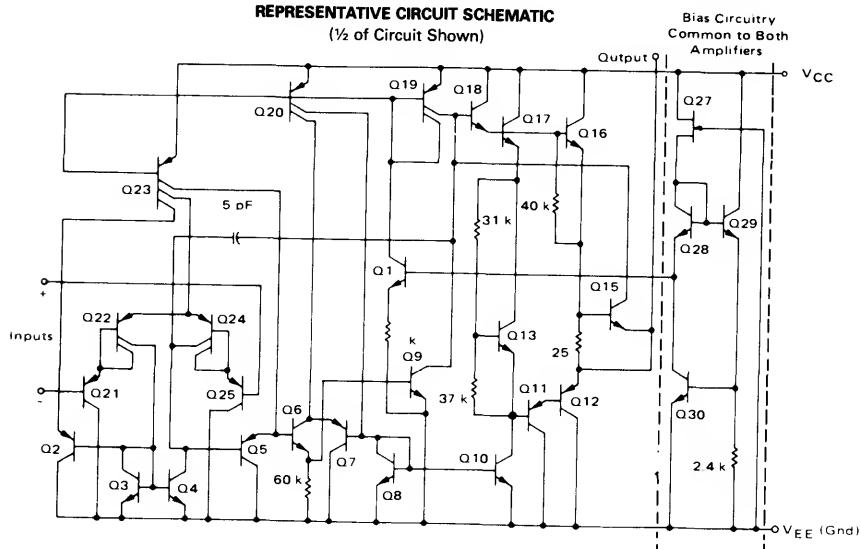
(2) Not to exceed maximum package power dissipation.

(3) Output will swing to ground

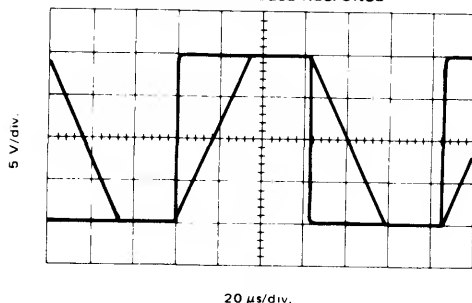
MC3458, MC3558, MC3358

2

REPRESENTATIVE CIRCUIT SCHEMATIC
(½ of Circuit Shown)



INVERTER PULSE RESPONSE



CIRCUIT DESCRIPTION

The MC3558 Series is made using two internally compensated, two-stage operational amplifiers. The first stage of each consists of differential input devices Q24 and Q22 with input buffer transistors Q25 and Q21 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance a smaller compensation capacitor (only 5 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q24 and Q22. Another feature of this input stage is that the input common-mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single-ended converter. The second stage consists of a standard current source load amplifier stage.

The output stage is unique because it allows the output to swing to ground in single supply operation and yet does not exhibit any crossover distortion in split supply operation. This is possible because class AB operation is utilized.

Each amplifier is biased from an internal-voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

TYPICAL PERFORMANCE CURVES

FIGURE 1 – SINE WAVE RESPONSE

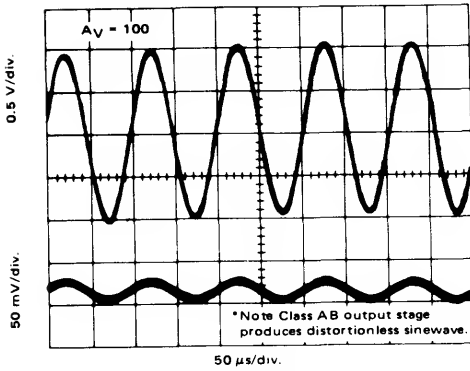


FIGURE 2 – OPEN LOOP FREQUENCY RESPONSE

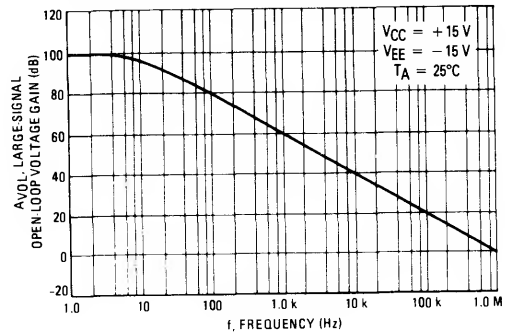


FIGURE 3 – POWER BANDWIDTH

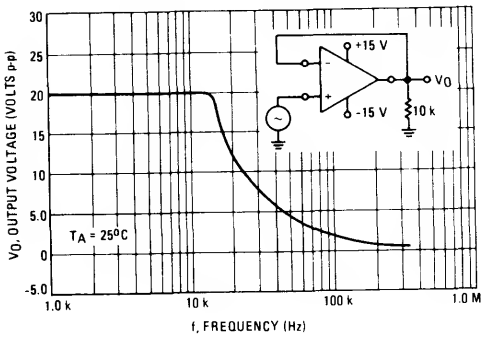


FIGURE 4 – OUTPUT SWING versus SUPPLY VOLTAGE

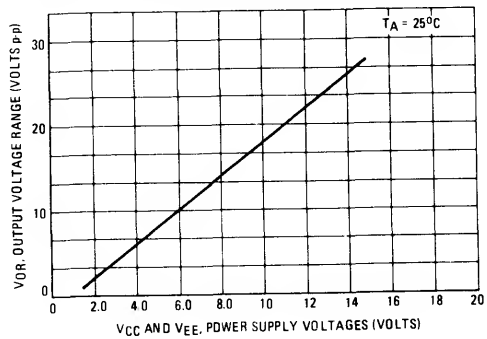


FIGURE 5 – INPUT BIAS CURRENT versus TEMPERATURE

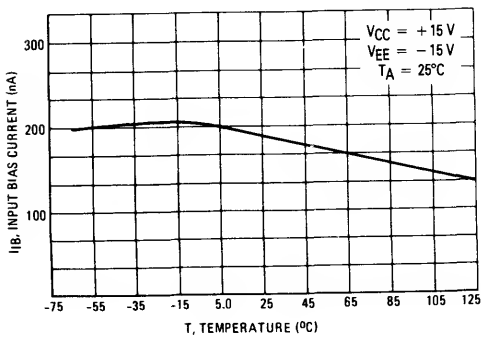
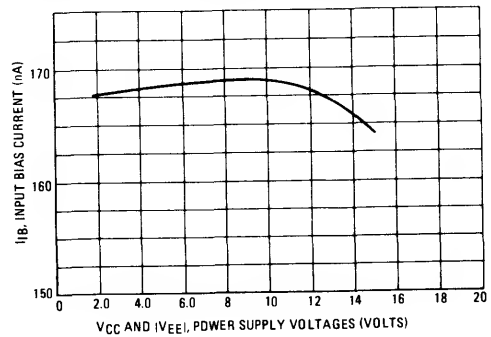


FIGURE 6 – INPUT BIAS CURRENT versus SUPPLY VOLTAGE



2

FIGURE 7 – VOLTAGE REFERENCE



APPLICATIONS INFORMATION (continued)

FIGURE 12 – FUNCTION GENERATOR

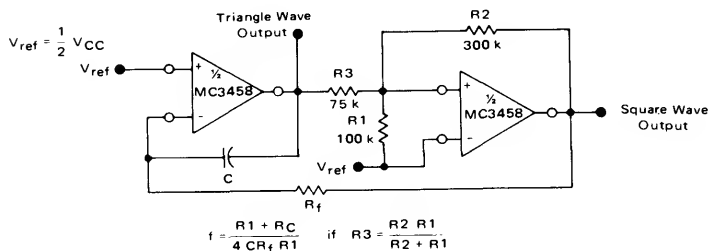
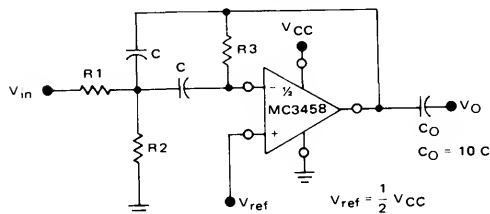


FIGURE 13 – MULTIPLE FEEDBACK BANDPASS FILTER



Given f_o = Center Frequency
 $A(f_o)$ = Gain at Center Frequency

Choose Value f_o , C

Then

$$R3 = \frac{Q}{\pi f_o C}$$

$$R1 = \frac{R3}{2 A(f_o)}$$

$$R2 = \frac{R1 R3}{4Q^2 R1 - R3}$$

For less than 10% error from operational amplifier

$$\frac{Q_o f_o}{BW} < 0.1 \quad \text{Where } f_o \text{ and BW are expressed in Hz.}$$

If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

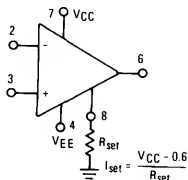
**LOW COST PROGRAMMABLE
OPERATIONAL AMPLIFIER**

The MC3476 is a low cost selection of the popular, industry-standard MC1776 programmable operational amplifier. This extremely versatile operational amplifier features low power consumption and high input impedance. In addition, the quiescent currents within the device may be programmed by the choice of an external resistor value or current source applied to the I_{set} input. This allows the amplifier's characteristics to be optimized for input current and power consumption despite wide variations in operating power supply voltages.

- ± 6.0 V to ± 18 V Operation
- Wide Programming Range
- Offset Null Capability
- No Frequency Compensation Required
- Low Input Bias Currents
- Short-Circuit Protection

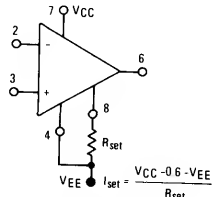
RESISTIVE PROGRAMMING (See Figure 1.)

R_{set} to GROUND



Typical R_{set} Values		
V_{CC}, V_{EE}	$I_{set} = 10 \mu A$	$I_{set} = 15 \mu A$
± 6.0 V	560 k Ω	360 k Ω
± 9.0 V	820 k Ω	560 k Ω
± 12 V	1.0 M Ω	750 k Ω
± 15 V	1.5 M Ω	1.0 M Ω

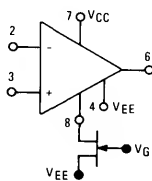
R_{set} to NEGATIVE SUPPLY



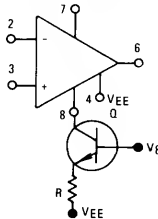
Typical R_{set} Values		
V_{CC}, V_{EE}	$I_{set} = 10 \mu A$	$I_{set} = 15 \mu A$
± 6.0 V	1.0 M Ω	820 k Ω
± 9.0 V	1.8 M Ω	1.2 M Ω
± 12 V	2.2 M Ω	1.5 M Ω
± 15 V	2.7 M Ω	2.0 M Ω

ACTIVE PROGRAMMING

FET CURRENT SOURCE



BIPOLAR CURRENT SOURCE



Pins not shown are not connected.

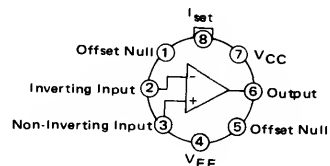
MC3476

**LOW COST
PROGRAMMABLE
OPERATIONAL AMPLIFIER**

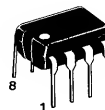
**SILICON MONOLITHIC
INTEGRATED CIRCUIT**



G SUFFIX
METAL PACKAGE
CASE 601

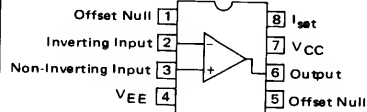
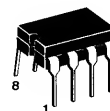


(Top View)



P1 SUFFIX
PLASTIC PACKAGE
CASE 626

U SUFFIX
CERAMIC PACKAGE
CASE 693



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC3476G	0 to +70°C	Metal Can
MC3476P1	0 to +70°C	Plastic DIP
MC3476U	0 to +70°C	Ceramic DIP

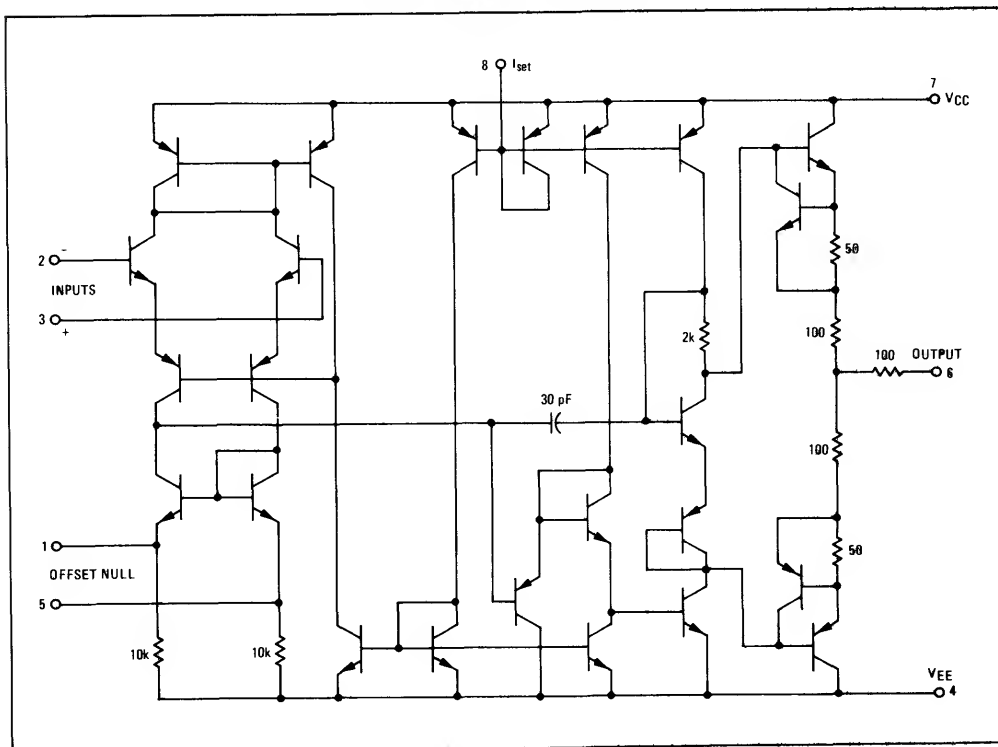
MC3476

MAXIMUM RATINGS ($T_A = +25^{\circ}\text{C}$ unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC}, V_{EE}	± 18	Vdc
Input Differential Voltage Range	V_{IDR}	± 30	Vdc
Input Common-Mode Voltage Range	V_{ICR}	V_{CC}, V_{EE}	Vdc
Offset Null to VEE Voltage	$V_{off-V_{EE}}$	± 0.5	Vdc
Programming Current	I_{set}	200	μA
Programming Voltage (Voltage from I_{set} terminal to ground)	V_{set}	$(V_{CC} - 0.6 \text{ V})$ to V_{CC}	Vdc
Output Short-Circuit Duration*	t_S	Indefinite	s
Operating Ambient Temperature Range	T_A	0 to 70	$^{\circ}\text{C}$
Storage Temperature Range Metal and Ceramic Packages Plastic Package	T_{stg}	-65 to +150 -55 to +125	$^{\circ}\text{C}$
Junction Temperature Metal and Ceramic Packages Plastic Package	T_J	175 150	$^{\circ}\text{C}$

*Short-Circuit to ground with $I_{set} \leq 15 \mu\text{A}$. Rating applies up to ambient temperature of $+70^{\circ}\text{C}$.

EQUIVALENT SCHEMATIC DIAGRAM

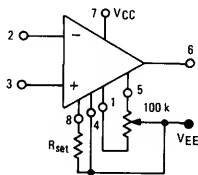


MC3476

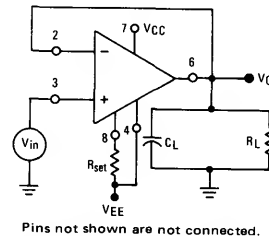
ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $I_{set} = 15\text{ }\mu\text{A}$, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S \leq 10\text{ k}\Omega$) $T_A = +25^\circ\text{C}$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	V_{IO}	—	2.0	6.0	mV
Offset Voltage Adjustment Range	V_{IOR}	—	18	—	mV
Input Offset Current $T_A = +25^\circ\text{C}$ $T_A = 70^\circ\text{C}$ $T_A = 0^\circ\text{C}$	I_{IO}	—	2.0	25	nA
Input Bias Current $T_A = +25^\circ\text{C}$ $T_A = 70^\circ\text{C}$ $T_A = 0^\circ\text{C}$	I_{IB}	—	15	50	nA
Input Resistance	r_i	—	5.0	—	M Ω
Input Capacitance	C_i	—	2.0	—	pF
Input Common-Mode Voltage Range $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	V_{ICR}	± 10	—	—	V
Large Signal Voltage Gain $R_L \geq 10\text{ k}\Omega$, $V_O = \pm 10\text{ V}$, $T_A = +25^\circ\text{C}$ $R_L \geq 10\text{ k}\Omega$, $V_O = \pm 10\text{ V}$, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	A_{VOL}	50 k 25 k	400 k —	— —	V/V
Output Voltage Range $R_L \geq 10\text{ k}\Omega$, $T_A = +25^\circ\text{C}$ $R_L \geq 10\text{ k}\Omega$, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	V_{OR}	± 12 ± 12	± 13 —	— —	V
Output Resistance	r_o	—	1.0	—	k Ω
Output Short-Circuit Current	I_{os}	—	12	—	mA
Common-Mode Rejection Ratio $R_S \leq 10\text{ k}\Omega$, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	CMRR	70	90	—	dB
Supply Voltage Rejection Ratio $R_S \leq 10\text{ k}\Omega$, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	PSRR	—	25	200	$\mu\text{V/V}$
Supply Current $T_A = +25^\circ\text{C}$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	I_{CC} , I_{EE}	— —	160 —	200 225	μA
Power Dissipation $T_A = +25^\circ\text{C}$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	P_D	— —	4.8 —	6.0 6.75	mW
Transient Response (Unity Gain) $V_{in} = 20\text{ mV}$, $R_L \geq 10\text{ k}\Omega$, $C_L = 100\text{ pF}$ Rise Time Overshoot	t_{TLH} OS	— —	0.35 10	— —	μs %
Slew Rate ($R_L \geq 10\text{ k}\Omega$)	SR	—	0.8	—	V/ μs

**VOLTAGE OFFSET
NULL CIRCUIT**



**TRANSIENT-RESPONSE
TEST CIRCUIT**



MC3476

TYPICAL CHARACTERISTICS

($T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 1 — SET CURRENT versus SET RESISTOR

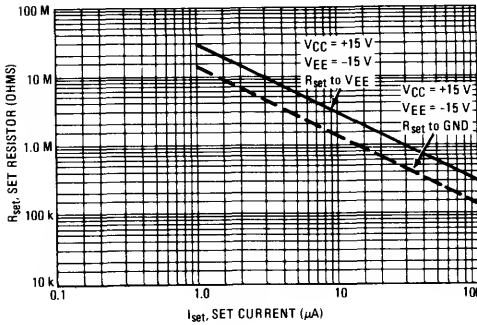


FIGURE 2 — POSITIVE STANDBY SUPPLY CURRENT versus SET CURRENT

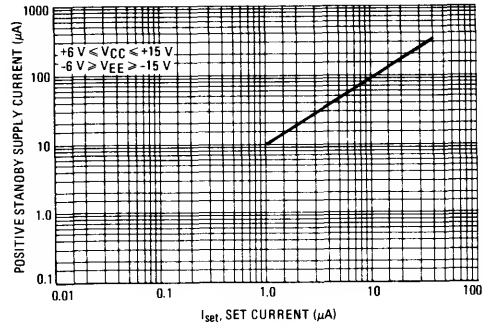


FIGURE 3 — OPEN-LOOP GAIN versus SET CURRENT

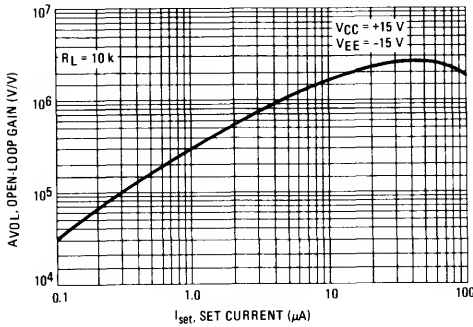


FIGURE 4 — INPUT BIAS CURRENT versus SET CURRENT

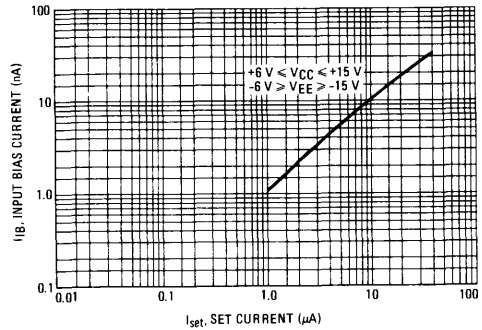


FIGURE 5 — SLEW RATE versus SET CURRENT

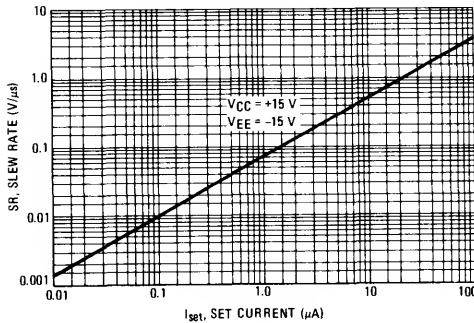
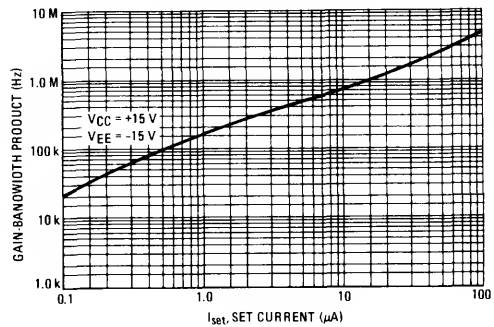
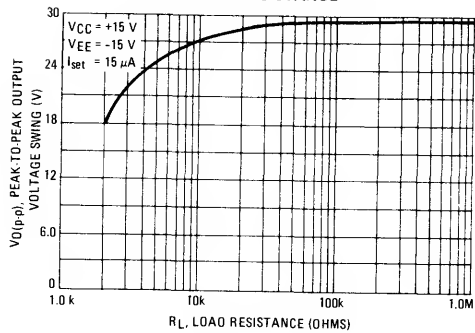
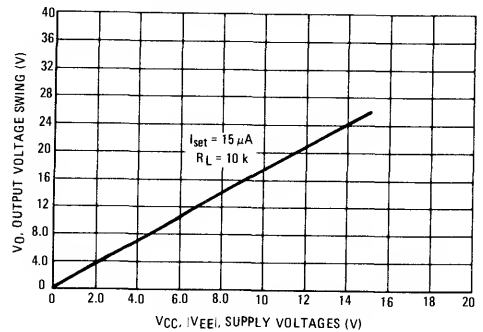


FIGURE 6 — GAIN-BANDWIDTH PRODUCT (GBW) versus SET CURRENT



TYPICAL CHARACTERISTICS (continued)

 $(T_A = +25^\circ\text{C unless otherwise noted.})$ FIGURE 7 – OUTPUT VOLTAGE SWING
versus LOAD RESISTANCEFIGURE 8 – OUTPUT SWING
versus SUPPLY VOLTAGE

MC4558, MC4558AC, MC4558C

2

DUAL WIDEBAND OPERATIONAL AMPLIFIER

The MC4558, MC4558AC, and MC4558C combine all the outstanding features of the MC1458 and, in addition, possess three times the unity gain bandwidth of the industry standard.

- 2.5 MHz Unity Gain Bandwidth Guaranteed on MC4558 and MC4558AC
- 2 MHz Unity Gain Bandwidth Guaranteed on MC4558C
- Internally Compensated
- Short-Circuit Protection
- Gain and Phase Match between Amplifiers
- Low Power Consumption

DUAL WIDE BANDWIDTH OPERATIONAL AMPLIFIER

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**

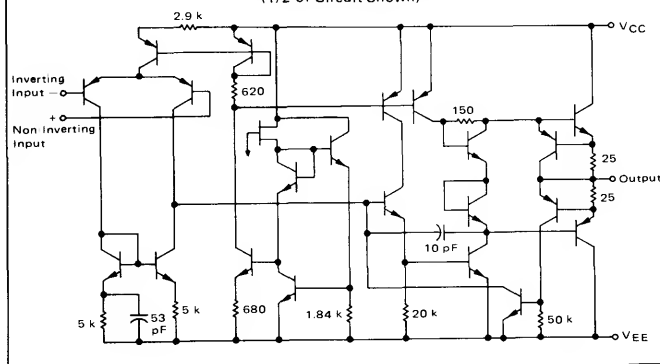
MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	MC4558 MC4558AC	MC4558C	Unit
Power Supply Voltage	V_{CC} V_{EE}	+22 -22	+18 -18	Vdc
Input Differential Voltage	V_{ID}	± 30		Volts
Input Common Mode Voltage (Note 1)	V_{ICM}	± 15		Volts
Output Short-Circuit Duration (Note 2)	t_S	Continuous		
Operating Ambient Temperature Range	T_A	See Ordering Information Below		
Storage Temperature Range	T_{stg}	-65 to +150		$^\circ\text{C}$
Junction Temperature	T_J	175		$^\circ\text{C}$
Metal and Ceramic Packages		-55 to +125		
Plastic Package		150		

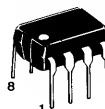
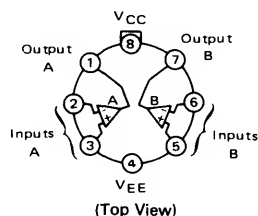
NOTES:

1. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.
2. Short circuit may be to ground or either supply.

EQUIVALENT CIRCUIT SCHEMATIC (1/2 of Circuit Shown)

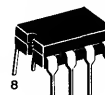


G SUFFIX
METAL PACKAGE
CASE 601

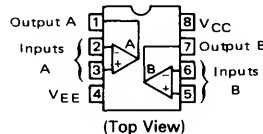


P1 SUFFIX
PLASTIC PACKAGE
CASE 626

U SUFFIX
CERAMIC PACKAGE
CASE 693



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)



ORDERING INFORMATION

Device	Temperature Range	Package
MC4558G	-55 to +125 $^\circ\text{C}$	Metal Can
MC4558U		Ceramic DIP
MC4558CD		SO-8
MC4558CG	0 to +70 $^\circ\text{C}$	Metal Can
MC4558ACP1, CP1		Plastic DIP
MC4558CU		Ceramic DIP

MC4558, MC4558AC, MC4558C

FREQUENCY CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	MC4558, MC4558AC			MC4558C			Unit
		Min	Typ	Max	Min	Typ	Max	
Unity Gain Bandwidth	BW	2.5	2.8	—	2.0	2.8	—	MHz

ELECTRICAL CHARACTERISTICS ($V_{CC} = 15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = 25^\circ\text{C}$ unless otherwise noted.)

Input Offset Voltage ($R_S \leq 10\text{ k}\Omega$)	V_{IO}	—	1.0	5.0	—	2.0	6.0	mV
Input Offset Current	I_{IO}	—	20	200	—	20	200	nA
Input Bias Current†	I_{IB}	—	80	500	—	80	500	nA
Input Resistance	r_i	0.3	2.0	—	0.3	2.0	—	$M\Omega$
Input Capacitance	C_i	—	1.4	—	—	1.4	—	pF
Common Mode Input Voltage Range	V_{ICR}	± 12	± 13	—	± 12	± 13	—	V
Large Signal Voltage Gain ($V_O = \pm 10\text{ V}$, $R_L = 2.0\text{ k}\Omega$)	A_v	50	200	—	20	200	—	V/mV
Output Resistance	r_o	—	75	—	—	75	—	Ω
Common Mode Rejection Ratio ($R_S \leq 10\text{ k}\Omega$)	CMRR	70	90	—	70	90	—	dB
Supply Voltage Rejection Ratio ($R_S \leq 10\text{ k}\Omega$)	PSRR	—	30	150	—	30	150	$\mu\text{V/V}$
Output Voltage Swing ($R_L \geq 10\text{ k}\Omega$) ($R_L \geq 2\text{ k}\Omega$)	V_O	± 12 ± 10	± 14 ± 13	—	± 12 ± 10	± 14 ± 13	—	V
Output Short-Circuit Current	I_{os}	10	20	40	10	20	40	mA
Supply Currents (Both Amplifiers)	I_D	—	2.3	5.0	—	2.3	5.6	mA
Power Consumption (Both Amplifiers)	P_C	—	70	150	—	70	170	mW
Transient Response (Unity Gain) ($V_i = 20\text{ mV}$, $R_L \geq 2\text{ k}\Omega$, $C_L \leq 100\text{ pF}$) Rise Time ($V_i = 20\text{ mV}$, $R_L \geq 2\text{ k}\Omega$, $C_L \leq 100\text{ pF}$) Overshoot ($V_i = 10\text{ V}$, $R_L \geq 2\text{ k}\Omega$, $C_L \leq 100\text{ pF}$) Slew Rate	t_{TLH} t_{os} SR	— — 1.5	0.3 15 1.6	— — —	— — 1.0	0.3 15 1.6	— — —	μs % V/ μs

ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = *T_{high}$ to T_{low} unless otherwise noted).

Input Offset Voltage ($R_S \leq 10\text{ k}\Omega$)	V_{IO}	—	1.0	6.0	—	—	7.5	mV
Input Offset Current ($T_A = T_{high}$) ($T_A = T_{low}$) ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$)	I_{IO}	— — —	7.0 85 —	200 500 —	— — —	— — —	— — 300	nA
Input Bias Current ($T_A = T_{high}$) ($T_A = T_{low}$) ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$)	I_{IB}	— — —	30 300 —	500 1500 —	— — —	— — —	— — 800	nA
Common Mode Input Voltage Range	V_{ICR}	± 12	± 13	—	—	—	—	V
Large Signal Voltage Gain ($V_O = \pm 10\text{ V}$, $R_L = 2\text{ k}\Omega$)	A_v	25	—	—	15	—	—	V/mV
Common Mode Rejection Ratio ($R_S \leq 10\text{ k}\Omega$)	CMRR	70	90	—	—	—	—	dB
Supply Voltage Rejection Ratio ($R_S \leq 10\text{ k}\Omega$)	PSRR	—	30	150	—	—	—	$\mu\text{V/V}$
Output Voltage Swing ($R_L \geq 10\text{ k}\Omega$) ($R_L \geq 2\text{ k}\Omega$)	V_O	± 12 ± 10	± 14 ± 13	—	± 12 ± 10	± 14 ± 13	—	V
Supply Currents (Both Amplifiers) ($T_A = T_{high}$) ($T_A = T_{low}$)	I_D	— —	— —	4.5 6.0	— —	— —	5.0 6.7	mA
Power Consumption (Both Amplifiers) ($T_A = T_{high}$) ($T_A = T_{low}$)	P_C	— —	— —	135 180	— —	— —	150 200	mW

* $T_{high} = 125^\circ\text{C}$ for MC4558 and 70°C for MC4558C and MC4558AC.

$T_{low} = -55^\circ\text{C}$ for MC4558 and 0°C for MC4558C and MC4558AC.

† I_{IB} is out of the amplifier due to PNP input transistors.

MC4558, MC4558AC, MC4558C

FIGURE 1 – BURST NOISE versus SOURCE RESISTANCE

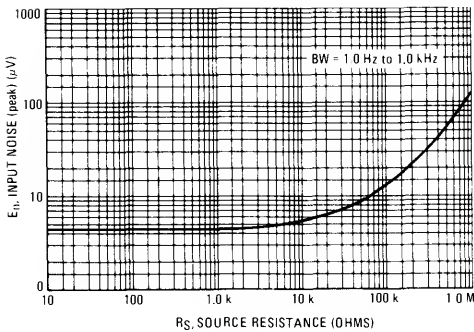


FIGURE 2 – RMS NOISE versus SOURCE RESISTANCE

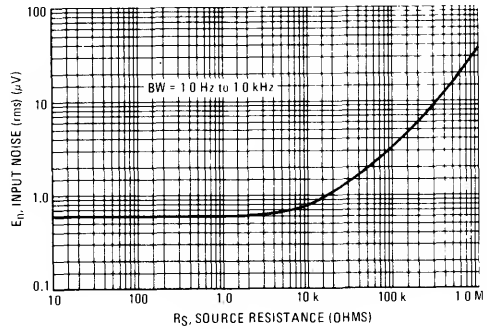


FIGURE 3 – OUTPUT NOISE versus SOURCE RESISTANCE

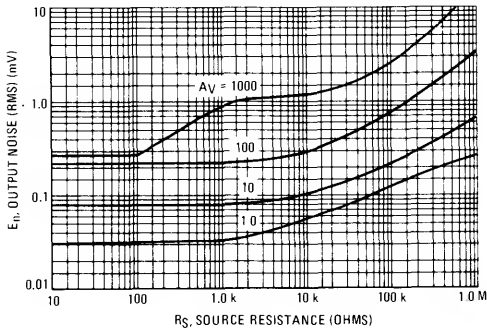


FIGURE 4 – SPECTRAL NOISE DENSITY

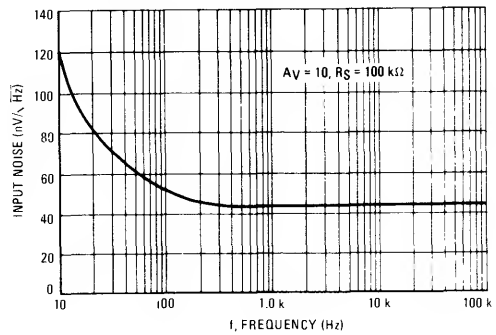
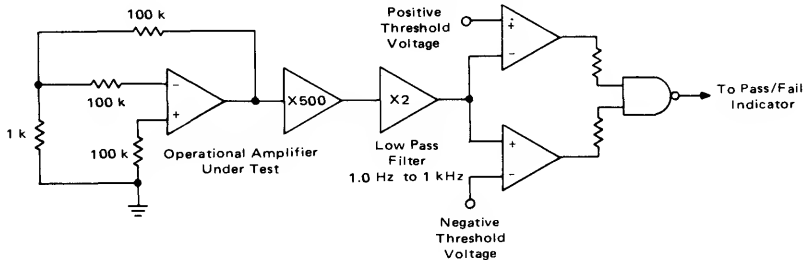


FIGURE 5 – BURST NOISE TEST CIRCUIT



Unlike conventional peak reading or RMS meters, this system was especially designed to provide the quick response time essential to burst (popcorn) noise testing.

The test time employed is 10 seconds and the 20 μ V peak limit refers to the operational amplifier input thus eliminating errors in the closed-loop gain factor of the operational amplifier under test.

FIGURE 6 – OPEN LOOP FREQUENCY RESPONSE

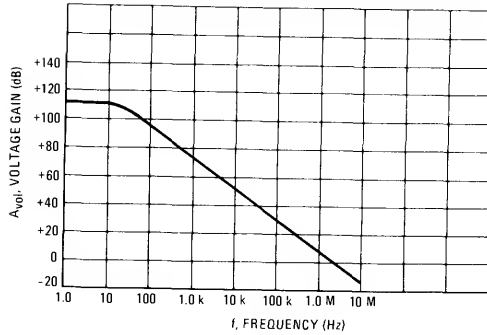


FIGURE 7 – PHASE MARGIN versus FREQUENCY

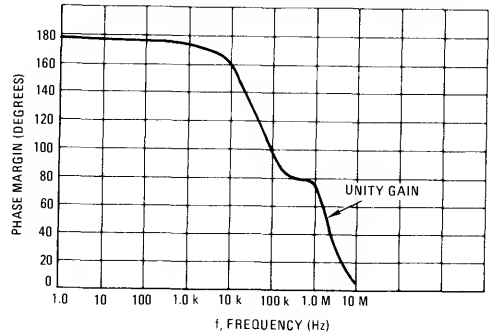


FIGURE 8 – POSITIVE OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

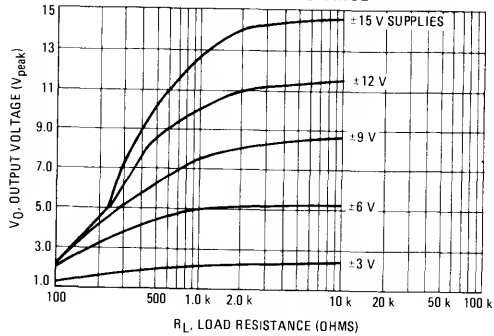


FIGURE 9 – NEGATIVE OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

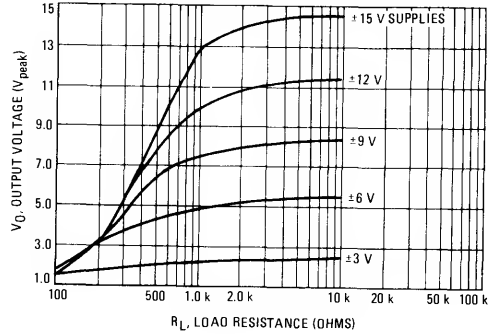


FIGURE 10 – POWER BANDWIDTH (LARGE SIGNAL SWING versus FREQUENCY)

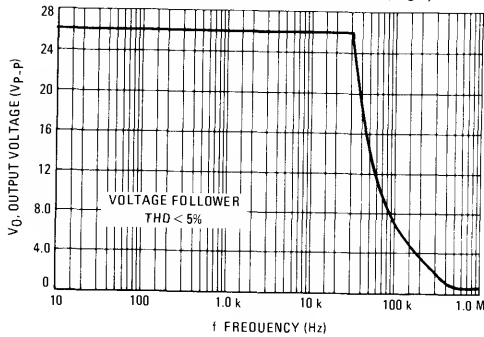
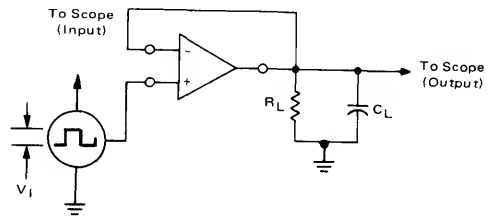


FIGURE 11 – TRANSIENT RESPONSE TEST CIRCUIT



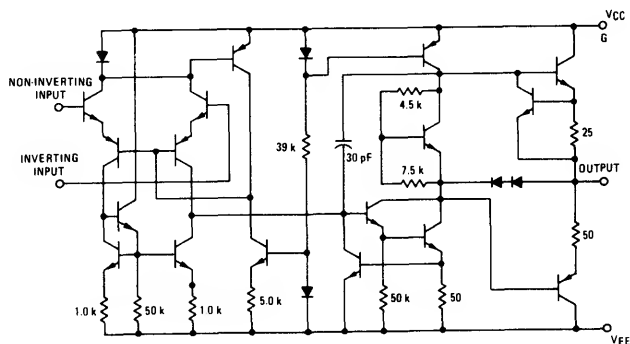
**(QUAD MC1741)
 OPERATIONAL AMPLIFIERS**

The MC4741 series is a true quad MC1741. Integrated on a single monolithic chip are four independent, low-power operational amplifiers which have been designed to provide operating characteristics identical to those of the industry standard MC1741, and can be applied with no change in circuit performance.

The MC4741 can be used in applications where amplifier matching or high packing density is important. Other applications include high impedance buffer amplifiers and active filter amplifiers.

- Each Amplifier is Functionally Equivalent to the MC1741
- Class AB Output Stage Eliminates Crossover Distortion
- True Differential Inputs
- Internally Frequency Compensated
- Short Circuit Protection
- Low Power Supply Current (0.6 mA/Amplifier)

**EQUIVALENT CIRCUIT SCHEMATIC
 (1/4 of Circuit Shown)**



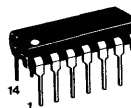
**MC4741
 MC4741C**

**(QUAD MC1741)
 DIFFERENTIAL INPUT
 OPERATIONAL AMPLIFIERS**

**SILICON MONOLITHIC
 INTEGRATED CIRCUIT**



**L SUFFIX
 CERAMIC PACKAGE
 CASE 632**

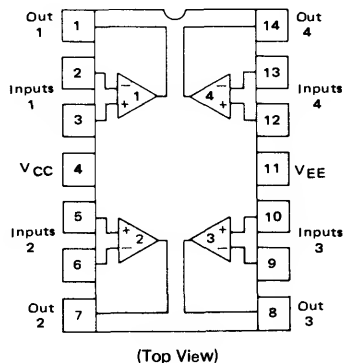


**P SUFFIX
 PLASTIC PACKAGE
 CASE 646**



**D SUFFIX
 PLASTIC PACKAGE
 CASE 751A
 (SO-14)**

PIN CONNECTIONS

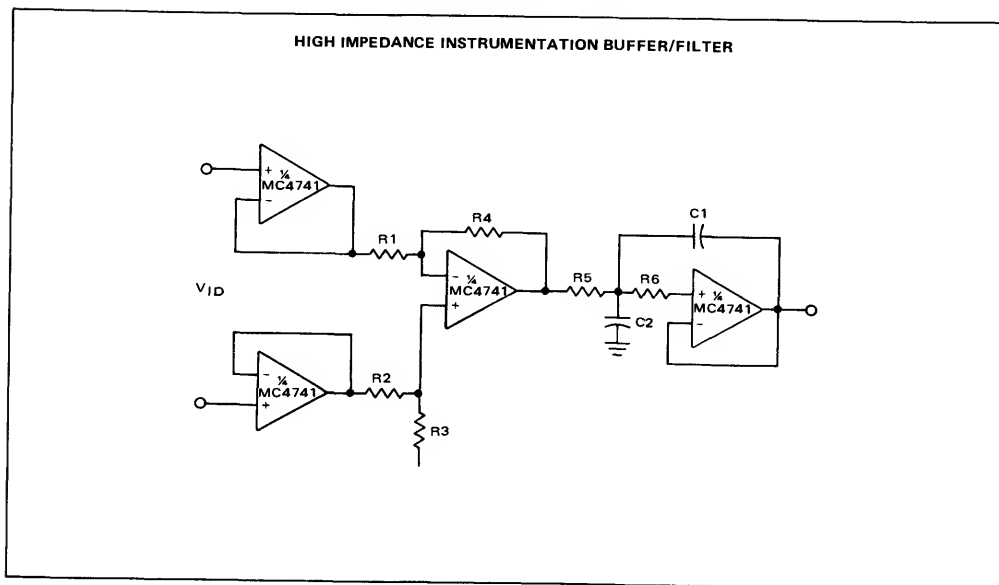


ORDERING INFORMATION

Device	Temperature Range	Package
MC4741L	-55°C to +125°C	Ceramic DIP
MC4741CD	0°C to +70°C	SO-14
MC4741CL		Ceramic DIP
MC4741CP		Plastic DIP

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted).

Rating	Symbol	MC4741	MC4741C	Unit
Power Supply Voltage	V_{CC} V_{EE}	+22 -22	+18 -18	Vdc Vdc
Input Differential Voltage	V_{ID}	+44	+36	Volts
Input Common Mode Voltage	V_{ICM}	+22	+18	Volts
Output Short Circuit Duration	t_S	Continuous		
Operating Ambient Temperature Range	T_A	-55 to +125	0 to +70	$^\circ\text{C}$
Storage Temperature Range	T_{stg}			
Ceramic Package		-65 to +150		
Plastic Package		-55 to +125		
Junction Temperature	T_J			
Ceramic Package		175		
Plastic Package		150		

TYPICAL APPLICATION

MC4741, MC4741C

2

ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = 25^\circ\text{C}$ unless otherwise noted).

Characteristic	Symbol	MC4741			MC4741C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10\text{ k}$)	V_{IO}	—	1.0	5.0	—	2.0	6.0	mV
Input Offset Current	I_{IO}	—	20	200	—	20	200	nA
Input Bias Current	I_{IB}	—	80	500	—	80	500	nA
Input Resistance	r_i	0.3	2.0	—	0.3	2.0	—	M Ω
Input Capacitance	C_i	—	1.4	—	—	1.4	—	pF
Offset Voltage Adjustment Range	V_{IOR}	—	± 15	—	—	± 15	—	mV
Common Mode Input Voltage Range	V_{ICR}	± 12	± 13	—	± 12	± 13	—	V
Large Signal Voltage Gain ($V_O = \pm 10\text{ V}$, $R_L \geq 2.0\text{ k}$)	A_v	50	200	—	20	200	—	V/mV
Output Resistance	r_o	—	75	—	—	75	—	Ω
Common Mode Rejection Ratio ($R_S \leq 10\text{ k}$)	CMRR	70	90	—	70	90	—	dB
Supply Voltage Rejection Ratio ($R_S \leq 10\text{ k}$)	PSRR	—	30	150	—	30	150	$\mu\text{V/V}$
Output Voltage Swing ($R_L \geq 10\text{ k}$) ($R_L \geq 2\text{ k}$)	V_O	± 12 ± 10	± 14 ± 13	— —	± 12 ± 10	± 14 ± 13	— —	V
Output Short-Circuit Current	I_{OS}	—	20	—	—	20	—	mA
Supply Current — (All Amplifiers)	I_D	—	2.4	4.0	—	3.5	7.0	mA
Power Consumption (All Amplifiers)	P_C	—	72	120	—	105	210	mW
Transient Response (Unity Gain — Non-Inverting) ($V_I = 20\text{ mV}$, $R_L \geq 2\text{ k}$, $C_L \leq 100\text{ pF}$) Rise Time ($V_I = 20\text{ mV}$, $R_L \geq 2\text{ k}$, $C_L \leq 100\text{ pF}$) Overshoot ($V_I = 10\text{ V}$, $R_L \geq 2\text{ k}$, $C_L \leq 100\text{ pF}$) Slew Rate	t_{TLH} os SR	— — —	0.3 15 0.5	— — —	— — —	0.3 15 0.5	— — —	μs % V/ μs

ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = *T_{\text{high}}$ to T_{low} unless otherwise noted.)

Characteristic	Symbol	MC4741			MC4741C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10\text{ k}\Omega$)	V_{IO}	—	1.0	6.0	—	—	7.5	mV
Input Offset Current ($T_A = 125^\circ\text{C}$) ($T_A = -55^\circ\text{C}$) ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$)	I_{IO}	— — —	7.0 85 —	200 500 —	— — —	— — —	— — 300	nA
Input Bias Current ($T_A = 125^\circ\text{C}$) ($T_A = -55^\circ\text{C}$) ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$)	I_{IB}	— — —	30 300 —	500 1500 —	— — —	— — —	— — 800	nA
Common Mode Input Voltage Range	V_{ICR}	± 12	± 13	—	—	—	—	V
Large Signal Voltage Gain ($R_L \geq 2\text{ k}$, $V_{out} = \pm 10\text{ V}$)	A_v	25	—	—	15	—	—	V/mV
Common Mode Rejection Ratio ($R_S \leq 10\text{ k}$)	CMRR	70	90	—	—	—	—	dB
Supply Voltage Rejection Ratio ($R_S \leq 10\text{ k}$)	PSRR	—	30	150	—	—	—	$\mu\text{V/V}$
Output Voltage Swing ($R_L \geq 10\text{ k}$) ($R_L \geq 2\text{ k}$)	V_O	± 12 ± 10	± 14 ± 13	— —	— ± 10	— ± 13	— —	V
Supply Currents — (All Amplifiers) ($T_A = 125^\circ\text{C}$) ($T_A = -55^\circ\text{C}$)	I_D	— —	2.4 3.6	3.4 5.0	— —	— —	— —	mA
Power Consumption ($T_A = +125^\circ\text{C}$) (All Amplifiers) ($T_A = -55^\circ\text{C}$)	P_C	— —	72 108	102 150	— —	— —	— —	mW

* $T_{\text{high}} = 125^\circ\text{C}$ for MC4741 and 70°C for MC4741C

$T_{\text{low}} = -55^\circ\text{C}$ for MC4741 and 0°C for MC4741C

MC4741, MC4741C

TYPICAL CHARACTERISTICS

($V_{CC} = +15$ Vdc, $V_{EE} = -15$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted).

**FIGURE 1 – POWER BANDWIDTH
(LARGE SIGNAL SWING versus FREQUENCY)**

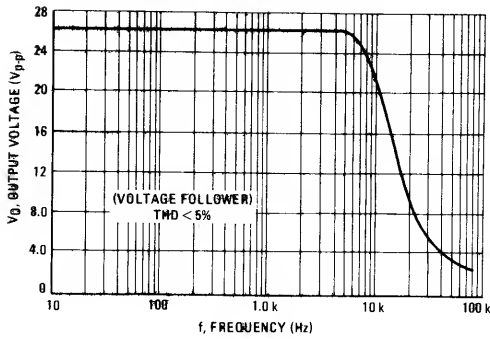
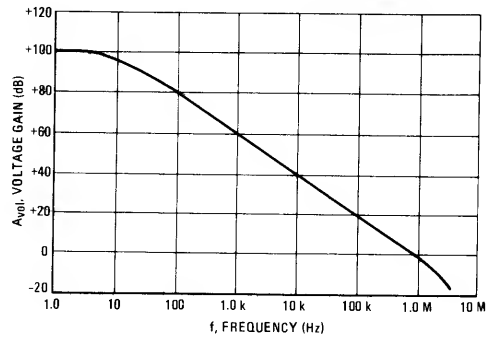
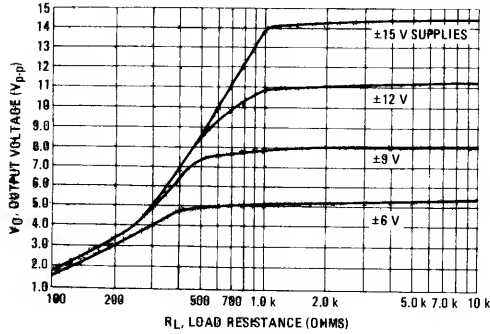


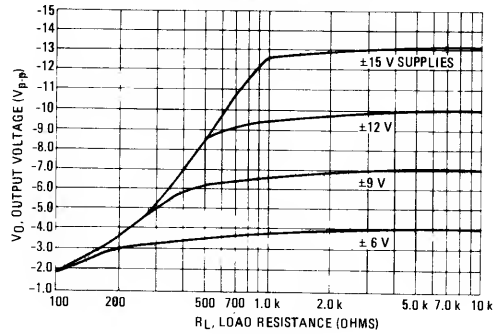
FIGURE 2 – OPEN LOOP FREQUENCY RESPONSE



**FIGURE 3 – POSITIVE OUTPUT VOLTAGE SWING
versus LOAD RESISTANCE**



**FIGURE 4 – NEGATIVE OUTPUT VOLTAGE SWING
versus LOAD RESISTANCE**



**FIGURE 5 – OUTPUT VOLTAGE SWING versus
LOAD RESISTANCE (Single Supply Operation)**

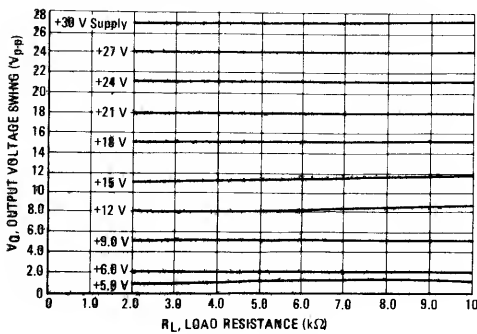
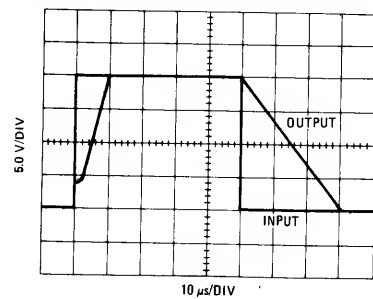


FIGURE 6 – NONINVERTING PULSE RESPONSE



MC4741, MC4741C

FIGURE 7 — BI-QUAD FILTER

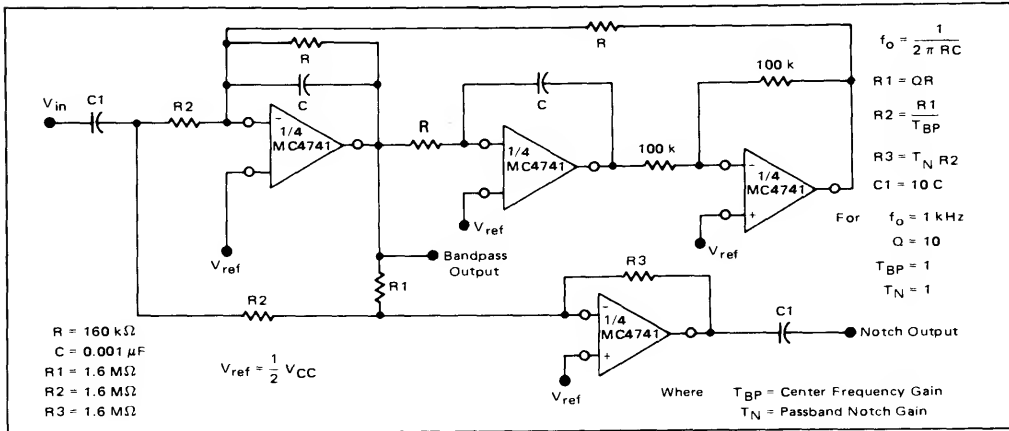


FIGURE 8 — OPEN LOOP VOLTAGE GAIN
versus SUPPLY VOLTAGE

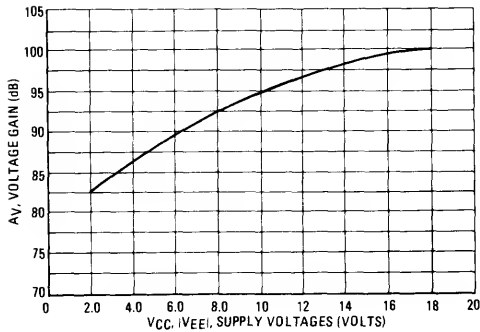


FIGURE 9 — TRANSIENT RESPONSE TEST CIRCUIT

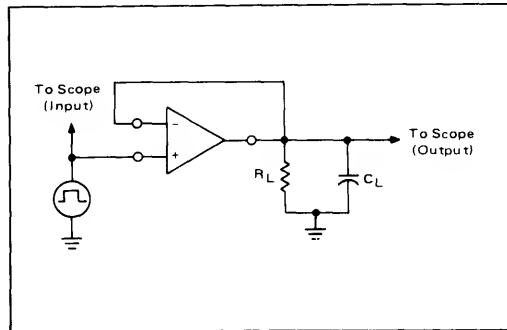
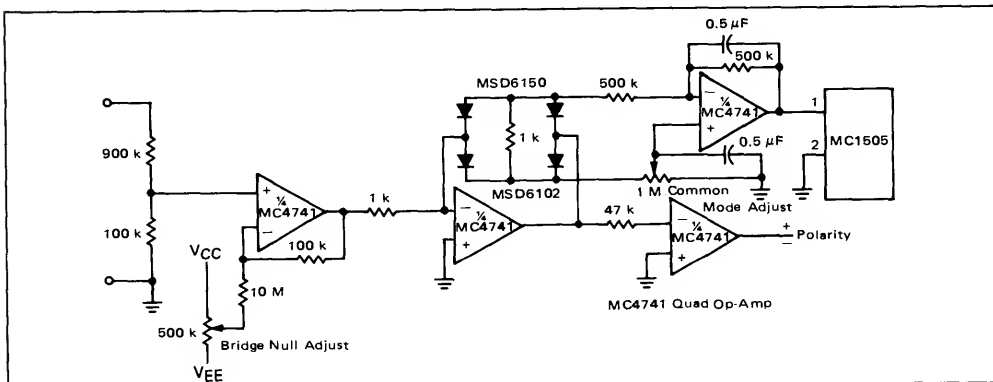


FIGURE 10 — ABSOLUTE VALUE DVM FRONT END



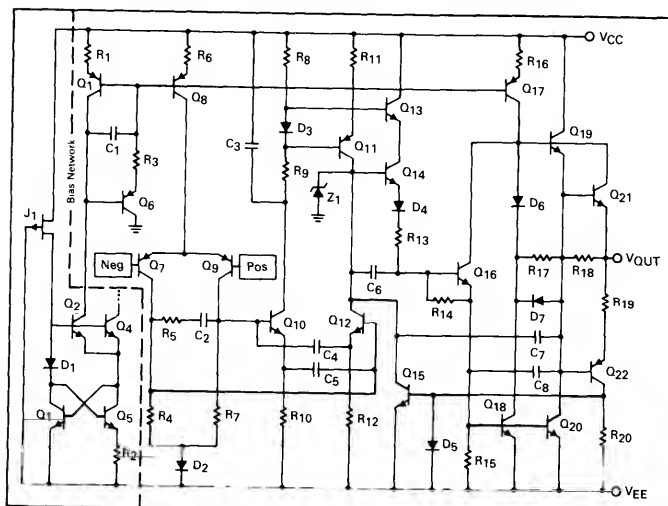
**DUAL, LOW NOISE
 OPERATIONAL AMPLIFIER**

The MC33077 is a precision high quality, high frequency, low noise monolithic dual operational amplifier employing innovative bipolar design techniques. Precision matching coupled with a unique analog resistor trim technique is used to obtain low input offset voltages. Dual-doublet frequency compensation techniques are used to enhance the gain bandwidth product of the amplifier. In addition, the MC33077 offers low input noise voltage, low temperature coefficient of input offset voltage, high slew rate, high ac and dc open-loop voltage gain and low supply current drain. The all NPN transistor output stage exhibits no deadband cross-over distortion, large output voltage swing, excellent phase and gain margins, low open-loop output impedance and symmetrical source and sink ac frequency performance.

The MC33077 is tested over the vehicular temperature range and is available in plastic DIP and SO-8 package (P and D suffixes).

- Low Voltage Noise: 4.4 nV/√Hz @ 1.0 kHz
- Low Input Offset Voltage: 0.2 mV
- Low TC of Input Offset Voltage: 2.0 μV/°C
- High Gain Bandwidth Product: 37 MHz @ 100 kHz
- High AC Voltage Gain: 370 @ 100 kHz
1850 @ 20 kHz
- Unity Gain Stable: with Capacitance Loads to 500 pF
- High Slew Rate: 11 V/μs
- Low Total Harmonic Distortion: 0.0007%
- Large Output Voltage Swing: +14 V to -14.7 V
- High DC Open-Loop Voltage Gain: 400 k (112 dB)
- High Common Mode Rejection: 107 dB
- Low Power Supply Drain Current: 3.5 mA
- Dual Supply Operation: ±2.5 V to ±18 V

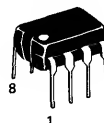
EQUIVALENT CIRCUIT SCHEMATIC (EACH AMPLIFIER)



MC33077

**DUAL, LOW NOISE
 OPERATIONAL AMPLIFIER**

**SILICON MONOLITHIC
 INTEGRATED CIRCUIT**

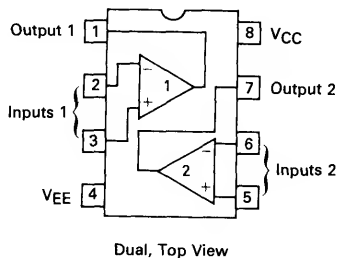


P SUFFIX
 PLASTIC PACKAGE
 CASE 626



D SUFFIX
 PLASTIC PACKAGE
 CASE 751
 (SO-8)

PIN ASSIGNMENTS



ORDERING INFORMATION

Op Amp Function	Device	Ambient Test Temperature Range	Package
Dual	MC33077D MC33077P	-40°C to +85°C	SO-8 Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+36	Volts
Input Differential Voltage Range	V_{IDR}	(Note 1)	Volts
Input Voltage Range	V_{IR}	(Note 1)	Volts
Output Short Circuit Duration (Note 2)	t_S	Indefinite	Seconds
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	-60 to +150	°C
Maximum Power Dissipation	P_D	(Note 2)	mW

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = 25^\circ\text{C}$ unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S = 10\ \Omega$, $V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	$ V_{IO} $	— —	0.13 —	1.0 1.5	mV
Average Temperature Coefficient of Input Offset Voltage $R_S = 10\ \Omega$, $V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	$\Delta V_{IO}/\Delta T$	—	2.0	—	$\mu\text{V}/^\circ\text{C}$
Input Bias Current ($V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	I_{IB}	— —	280 —	1000 1200	nA
Input Offset Current ($V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	I_{IO}	— —	15 —	180 240	nA
Common Mode Input Voltage Range ($\Delta V_{IO} = 5.0\text{ mV}$, $V_O = 0\text{ V}$)	V_{ICR}	± 13.5	± 14	—	V
Large Signal Voltage Gain ($V_O = \pm 10\text{ V}$, $R_L = 2.0\text{ k}\Omega$) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	A_{VOL}	150 k 125 k	400 k —	— —	V/V
Output Voltage Swing ($V_{ID} = \pm 1.0\text{ V}$) $R_L = 2.0\text{ k}\Omega$ $R_L = 2.0\text{ k}\Omega$ $R_L = 10\text{ k}\Omega$ $R_L = 10\text{ k}\Omega$	V_{O+} V_{O-} V_{O+} V_{O-}	13 — 13.4 —	13.6 -14.1 14 -14.7	— -13.5 — -14.3	V
Common Mode Rejection ($V_{in} = \pm 13\text{ V}$)	CMR	85	107	—	dB
Power Supply Rejection (Note 3) $V_{CC}/V_{EE} = +15\text{ V}/-15\text{ V}$ to $+5.0\text{ V}/-5.0\text{ V}$	PSR	80	90	—	dB
Output Short Circuit Current ($V_{ID} = \pm 1.0\text{ V}$, Output to Ground) Source Sink	I_{SC}	+10 -20	+26 -33	60 60	mA
Power Supply Current ($V_O = 0\text{ V}$, All Amplifiers) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	I_D	— —	3.5 —	4.5 4.8	mA

Notes:

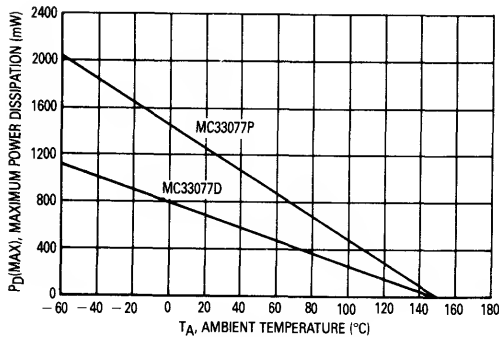
1. Either or both input voltages should not exceed V_{CC} or V_{EE} (See Applications Information).
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (See power dissipation performance characteristic, Figure 1).
3. Measured with V_{CC} and V_{EE} simultaneously varied.

MC33077

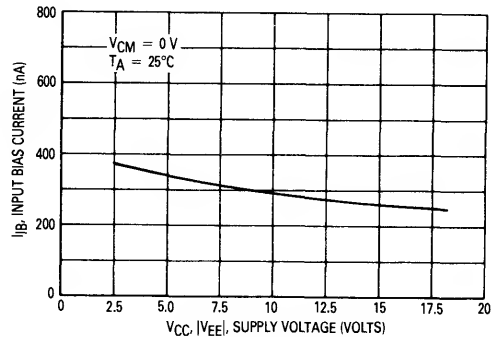
AC ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = 25^\circ\text{C}$ unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Slew Rate ($V_{in} = -10\text{ V}$ to $+10\text{ V}$, $R_L = 2.0\text{ k}\Omega$, $C_L = 100\text{ pF}$, $A_V = +1.0$)	SR	8.0	11	—	V/ μs
Gain Bandwidth Product ($f = 100\text{ kHz}$)	GBW	25	37	—	MHz
AC Voltage Gain ($R_L = 2.0\text{ k}\Omega$, $V_O = 0\text{ V}$) $f = 100\text{ kHz}$ $f = 20\text{ kHz}$	A_{VO}	— —	370 1850	— —	V/V
Unity Gain Frequency (Open-Loop)	f_U	—	7.5	—	MHz
Gain Margin ($R_L = 2.0\text{ k}\Omega$, $C_L = 0\text{ pF}$)	A_m	—	10	—	dB
Phase Margin ($R_L = 2.0\text{ k}\Omega$, $C_L = 0\text{ pF}$)	ϕ_m	—	55	—	Deg
Channel Separation ($f = 20\text{ Hz}$ to 20 kHz , $R_L = 2.0\text{ k}\Omega$, $V_O = 10\text{ V}_{p-p}$)	CS	—	-120	—	dB
Power Bandwidth ($V_O = 27\text{ V}_{p-p}$, $R_L = 2.0\text{ k}\Omega$, THD $\leq 1\%$)	BWP	—	200	—	kHz
Distortion ($R_L = 2.0\text{ k}\Omega$) $A_V = +1.0$, $f = 20\text{ Hz}$ to 20 kHz $V_O = 3.0\text{ V}_{rms}$ $A_V = 2000$, $f = 20\text{ kHz}$ $V_O = 2.0\text{ V}_{p-p}$ $V_O = 10\text{ V}_{p-p}$ $A_V = 4000$, $f = 100\text{ kHz}$ $V_O = 2.0\text{ V}_{p-p}$ $V_O = 10\text{ V}_{p-p}$	THD	— — — — — —	0.0007 0.215 0.242 0.319 0.316	— — — — —	%
Open-Loop Output Impedance ($V_O = 0\text{ V}$, $f = f_U$)	$ Z_O $	—	36	—	Ω
Differential Input Resistance ($V_{CM} = 0\text{ V}$)	R_{IN}	—	270	—	$\text{k}\Omega$
Differential Input Capacitance ($V_{CM} = 0\text{ V}$)	C_{IN}	—	15	—	pF
Equivalent Input Noise Voltage ($R_S = 100\text{ }\Omega$) $f = 10\text{ Hz}$ $f = 1.0\text{ kHz}$	e_n	— —	6.7 4.4	— —	$\text{nV}/\sqrt{\text{Hz}}$
Equivalent Input Noise Current ($f = 1.0\text{ kHz}$) $f = 10\text{ Hz}$ $f = 1.0\text{ kHz}$	i_n	— —	1.3 0.6	— —	$\text{pA}/\sqrt{\text{Hz}}$

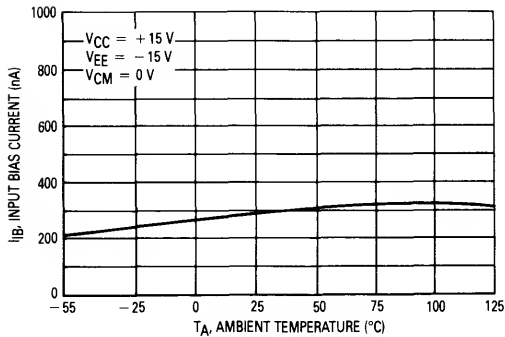
**FIGURE 1 — MAXIMUM POWER DISSIPATION
versus TEMPERATURE**



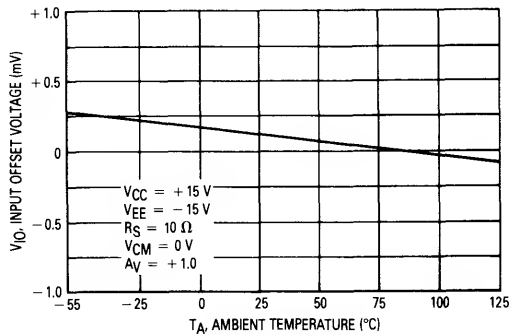
**FIGURE 2 — INPUT BIAS CURRENT
versus SUPPLY VOLTAGE**



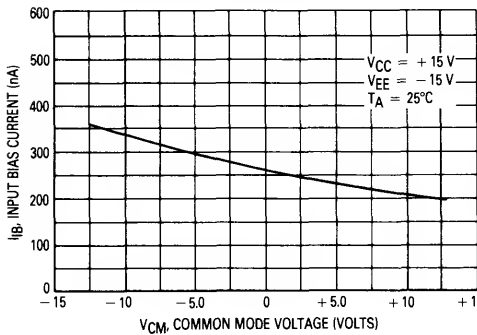
**FIGURE 3 — INPUT BIAS CURRENT
versus TEMPERATURE**



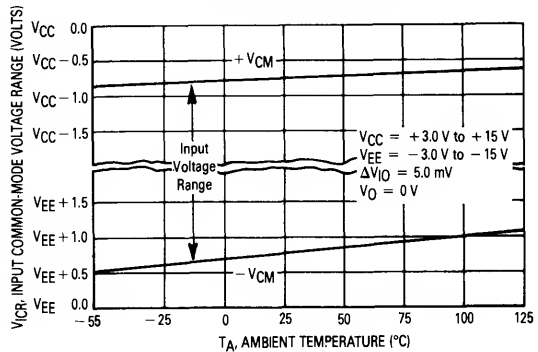
**FIGURE 4 — INPUT OFFSET VOLTAGE
versus TEMPERATURE**



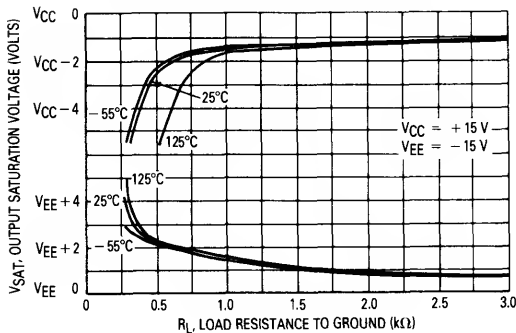
**FIGURE 5 — INPUT BIAS CURRENT
versus COMMON MODE VOLTAGE**



**FIGURE 6 — INPUT COMMON MODE VOLTAGE RANGE
versus TEMPERATURE**



**FIGURE 7 — OUTPUT SATURATION VOLTAGE
versus LOAD RESISTANCE TO GROUND**



**FIGURE 8 — OUTPUT SHORT CIRCUIT CURRENT
versus TEMPERATURE**

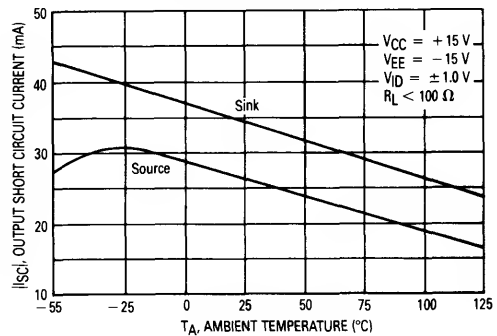
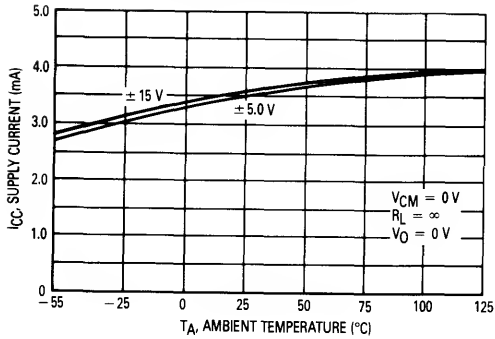
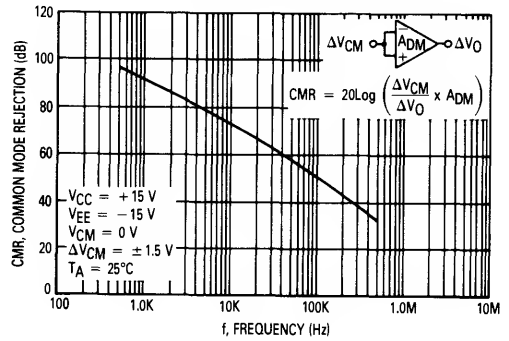
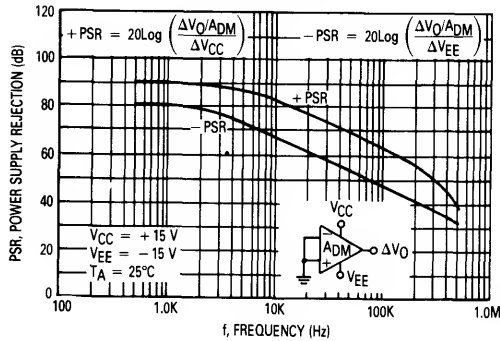
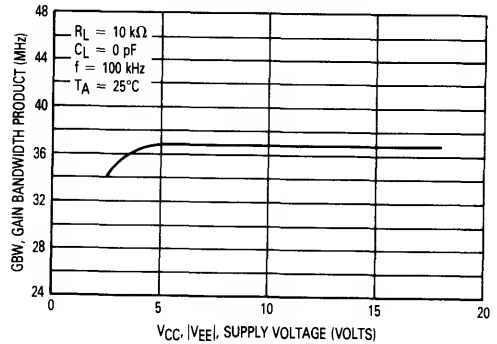
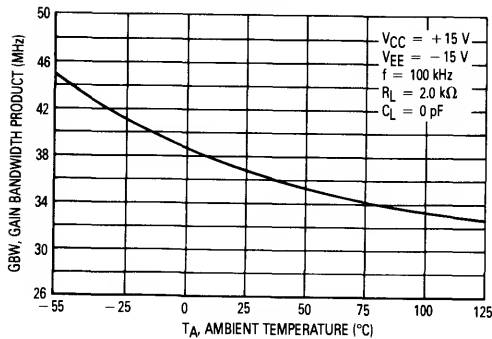
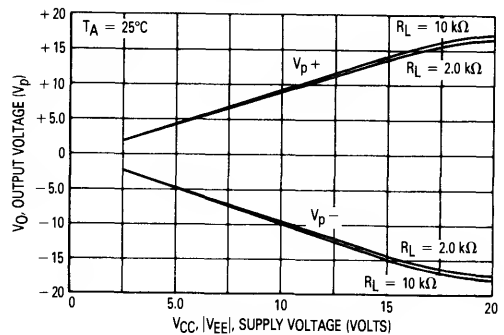


FIGURE 9 — SUPPLY CURRENT
versus TEMPERATUREFIGURE 10 — COMMON MODE REJECTION
versus FREQUENCYFIGURE 11 — POWER SUPPLY REJECTION
versus FREQUENCYFIGURE 12 — GAIN BANDWIDTH PRODUCT
versus SUPPLY VOLTAGEFIGURE 13 — GAIN BANDWIDTH PRODUCT
versus TEMPERATUREFIGURE 14 — MAXIMUM OUTPUT VOLTAGE
versus SUPPLY VOLTAGE

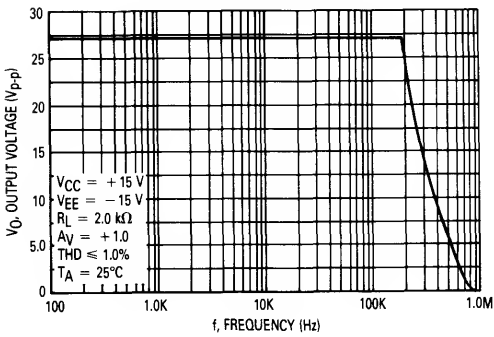
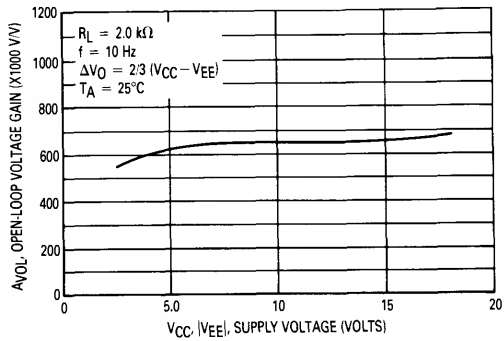
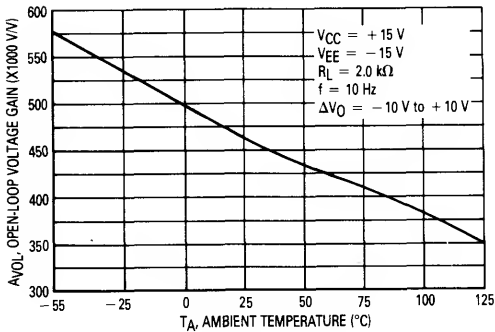
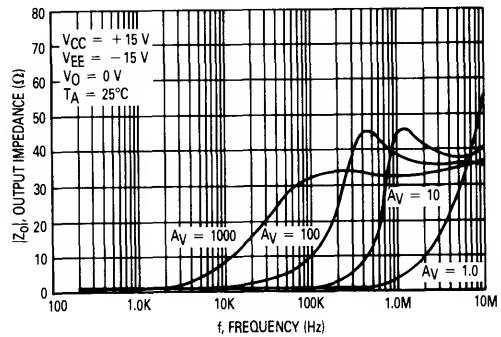
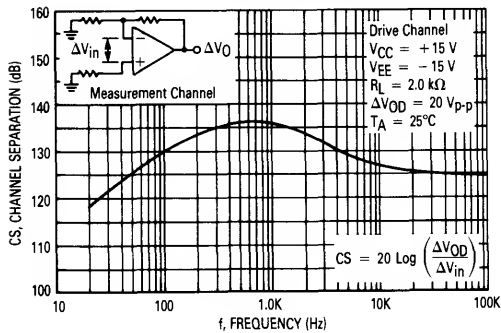
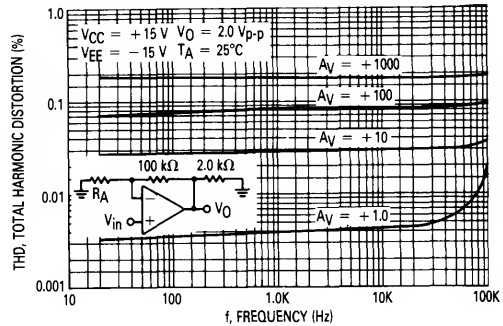
**FIGURE 15 — OUTPUT VOLTAGE
versus FREQUENCY**

**FIGURE 16 — OPEN-LOOP VOLTAGE GAIN
versus SUPPLY VOLTAGE**

**FIGURE 17 — OPEN-LOOP VOLTAGE GAIN
versus TEMPERATURE**

**FIGURE 18 — OUTPUT IMPEDANCE
versus FREQUENCY**

**FIGURE 19 — CHANNEL SEPARATION
versus FREQUENCY**

**FIGURE 20 — TOTAL HARMONIC DISTORTION
versus FREQUENCY**


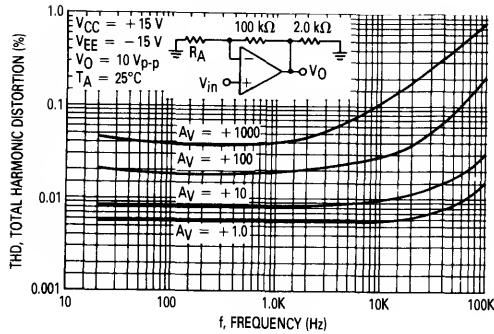
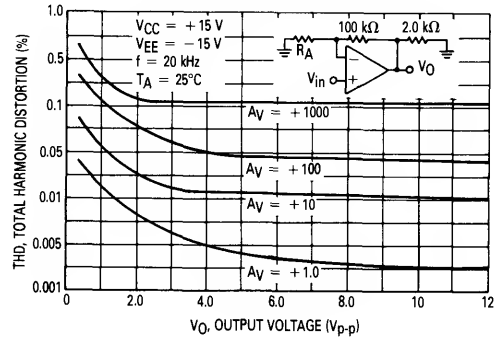
FIGURE 21 — TOTAL HARMONIC DISTORTION
versus FREQUENCYFIGURE 22 — TOTAL HARMONIC DISTORTION
versus OUTPUT VOLTAGE

FIGURE 23 — SLEW RATE versus SUPPLY VOLTAGE

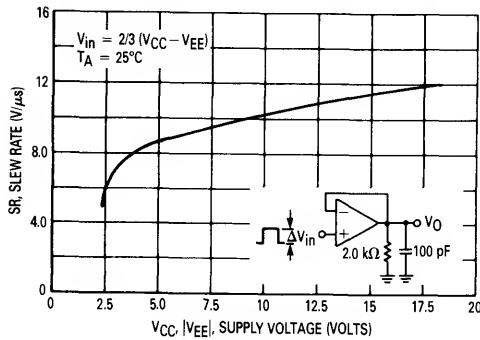


FIGURE 24 — SLEW RATE versus TEMPERATURE

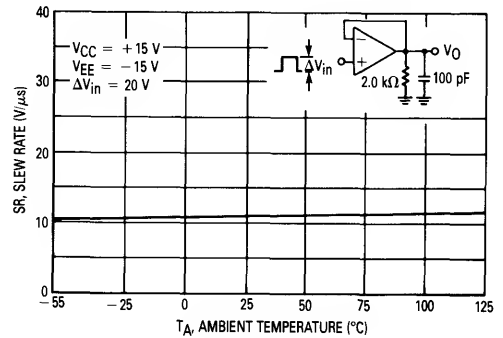
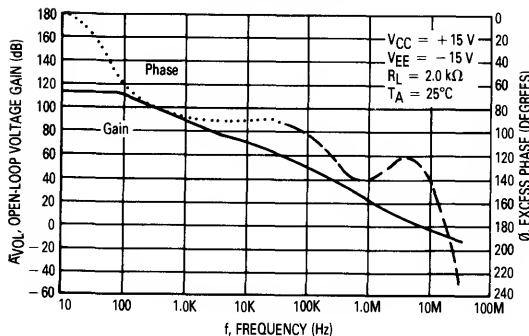
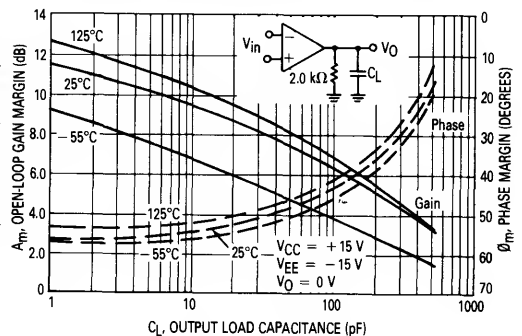
FIGURE 25 — VOLTAGE GAIN and PHASE
versus FREQUENCYFIGURE 26 — OPEN-LOOP GAIN MARGIN and PHASE
MARGIN versus OUTPUT LOAD CAPACITANCE

FIGURE 27 — PHASE MARGIN versus OUTPUT VOLTAGE

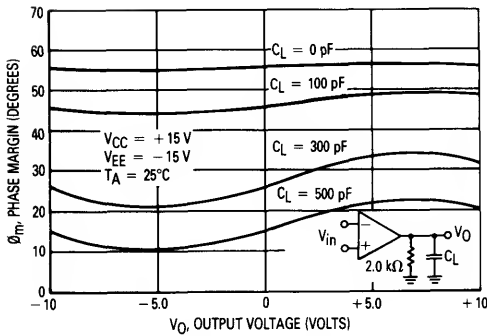


FIGURE 28 — OVERSHOOT versus OUTPUT LOAD CAPACITANCE

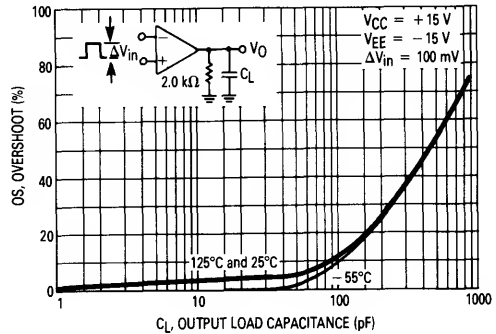


FIGURE 29 — INPUT REFERRED NOISE VOLTAGE and CURRENT versus FREQUENCY

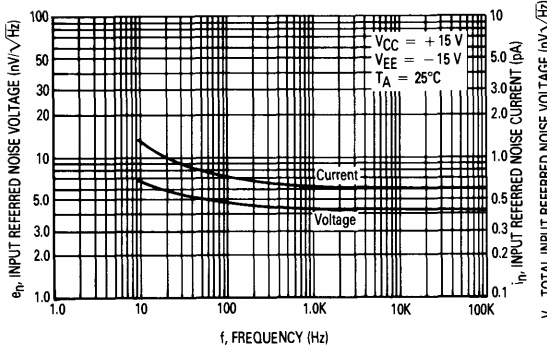


FIGURE 30 — TOTAL INPUT REFERRED NOISE VOLTAGE versus SOURCE RESISTANCE

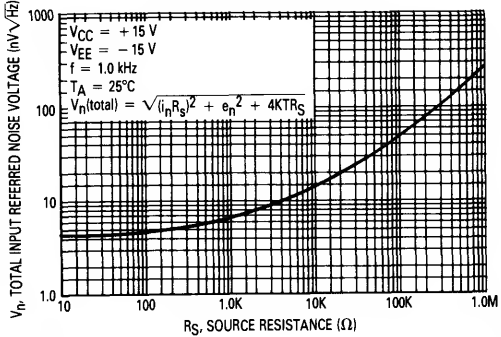


FIGURE 31 — PHASE MARGIN AND GAIN MARGIN versus DIFFERENTIAL SOURCE RESISTANCE

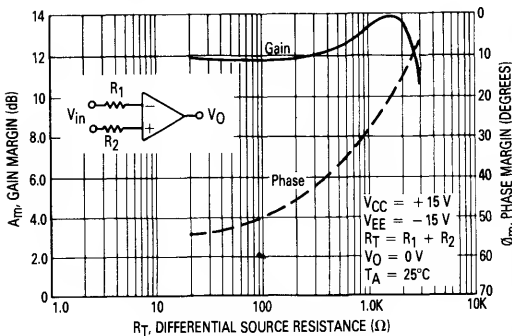


FIGURE 32 — INVERTING AMPLIFIER SLEW RATE

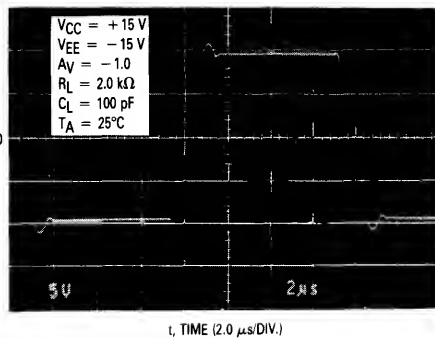


FIGURE 33 — NON-INVERTING AMPLIFIER SLEW RATE

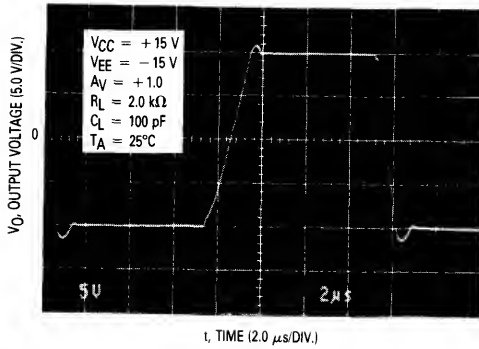
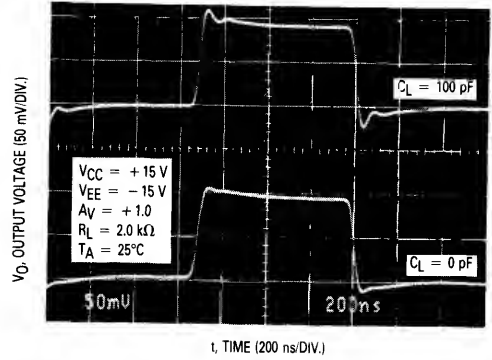
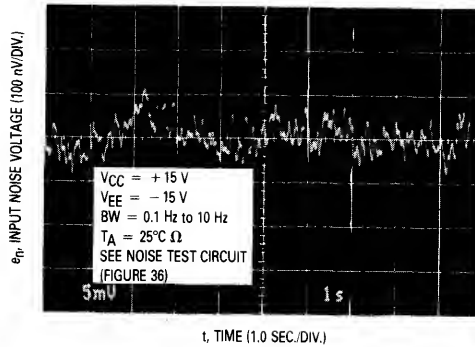


FIGURE 34 — NON-INVERTING AMPLIFIER OVERSHOOT

FIGURE 35 — LOW FREQUENCY NOISE VOLTAGE
versus TIME

APPLICATIONS INFORMATION

The MC33077 is designed primarily for its low noise, low offset voltage, high gain bandwidth product and large output swing characteristics. Its outstanding high frequency gain/phase performance make it a very attractive amplifier for high quality pre-amps, instrumentation amps, active filters and other applications requiring precision quality characteristics.

The MC33077 utilizes high frequency lateral PNP input transistors in a low noise bipolar differential stage driving a compensated Miller integration amplifier. Dual-doublet frequency compensation techniques are used to enhance the gain bandwidth product. The output stage uses an all NPN transistor design which provides greater output voltage swing and improved frequency performance over more conventional stages by using both PNP and NPN transistors (Class AB). This combination produces an amplifier with superior characteristics.

Through precision component matching and innovative current mirror design, a lower than normal temperature coefficient of input offset voltage ($2.0 \mu\text{V}/^\circ\text{C}$ as opposed to $10 \mu\text{V}/^\circ\text{C}$), as well as low input offset voltage, is accomplished.

The minimum common mode input range is from 1.5 volts below the positive rail (V_{CC}) to 1.5 volts above the negative rail (V_{EE}). The inputs will typically common mode to within 1.0 volt of both negative and positive rails though degradation in offset voltage and gain will be experienced as the common mode voltage nears either supply rail. In practice, though not recommended, the input voltage may exceed V_{CC} by approximately 30 volts and decrease below the V_{EE} rail by approximately 0.6 volts without causing permanent damage to the device. If the input voltage on either or both inputs is less than approximately 0.6 volts, excessive current may flow, if not limited, causing permanent damage to the device.

The amplifier will not latch with input source currents up to 20 mA, though in practice, source currents should be limited to 5.0 mA so as to avoid any parametric damage to the device. If both inputs exceed V_{CC} , the output will be in the high state and phase reversal may occur. No phase reversal will occur if the voltage on one input is within the common mode range and the voltage on the other input exceeds V_{CC} . Phase reversal may occur if the input voltage on either or both inputs is less than 1.0 volt above the negative rail. Phase reversal will be experienced if the voltage on either or both inputs is less than V_{EE} .

Through the use of dual-doublet frequency compensation techniques, the gain bandwidth product has been greatly enhanced over other amplifiers using the conventional single pole compensation. The phase and gain error of the amplifier remains low to higher frequencies for fixed amplifier gain configurations.

With the all NPN output stage, there is minimal swing loss to the supply rails, producing superior output swing, no crossover distortion and improved output phase symmetry with output voltage excursions. Output phase symmetry being the amplifiers ability to maintain a constant phase relation independent of its output voltage swing. Output phase symmetry degradation in the more conventional PNP and NPN transistor output stage was primarily due to the inherent cut-off frequency mismatch of the PNP and NPN transistors (typically 10 MHz and 300 MHz respectively) used causing considerable phase change to occur as the output voltage changes. By eliminating the PNP in the output, such phase change has been avoided and a very significant improvement in output phase symmetry as well as output swing has been accomplished.

The output swing improvement is most noticeable when operation is with lower supply voltages (typically 30% with $\pm 5.0 \text{ V}$ supplies). With a 10 k load, the output of the amplifier can typically swing to within 1.0 V of the positive rail (V_{CC}), and to within 0.3 V of the negative rail (V_{EE}), producing a $28.7 V_{D-P}$ signal from $\pm 15 \text{ V}$ supplies. Output voltage swing can be further improved by using an output pull-up resistor referenced to the V_{CC} . Where output signals are referenced to the positive supply rail, the pull-up resistor will pull the output to V_{CC} during the positive swing and during the negative swing, the NPN output transistor collector will pull the output very near V_{EE} . This configuration will produce the maximum attainable output signal from given supply voltages. The value of load resistance used should be much less than any feedback resistance so as to avoid excess loading and allow easy pull-up of the output.

Output impedance of the amplifier is typically less than 50 ohms at frequencies less than the unity gain cross-over frequency (see Output Impedance versus Frequency curve). The amplifier is unity gain stable with output capacitance loads up to 500 pF at full output swing over the -55°C to $+125^\circ\text{C}$ temperature range. Output phase symmetry is excellent with typically 4° total phase change over a 20 volt output excursion at 25°C with a 2.0 k Ω and 100 pF load. With a 2.0 k Ω resistive load and no capacitance loading the total phase change is approximately one degree for the same 20 volt output excursion. With a 2.0 k Ω and 500 pF load at 125°C the total phase change is typically only 10° for a 20 volt output excursion (see Phase Margin versus Output Voltage curve).

As with all amplifiers, care should be exercised so as to insure that one does not create a pole at the input of the amplifier which is near the closed loop corner frequency. This becomes a greater concern when using high frequency amplifiers since it is very easy to create such a pole with relatively small values of resistance on the inputs. If this does occur, the amplifiers phase will

degrade severely causing the amplifier to become unstable. Effective source resistances, acting in conjunction with the input capacitance of the amplifier, should be kept to a minimum so as to avoid creating such a pole at the input (see Phase Margin and Gain Margin versus Differential Source Resistance curve). There is minimal effect on stability where the created input pole is much greater than the closed loop corner frequency. Where amplifier stability is affected as a result of a negative feedback resistor in conjunction with the amplifier's input capacitance, creating a pole near the closed loop corner frequency, lead capacitor compensation techniques (lead capacitor in parallel with the feedback resistor) can be employed to improve stability. The feedback resistor and lead capacitor RC time constant should be larger than that of the uncompensated input pole frequency. Having a high resistance connected to the non-inverting input of the amplifier can create a like instability problem. Compensation for this condition can be accomplished by adding a lead capacitor in parallel with the non-inverting input resistor of such a value as to make the RC time constant larger than the RC time constant of the uncompensated input resistor acting in conjunction with the amplifiers input capacitance.

For optimum frequency performance and stability careful component placement and printed circuit board layout should be exercised. For example, long unshielded input or output leads may result in unwanted input-output coupling. In order to reduce the input capacitance, the body of resistors connected to the input pins should be physically close to the input pins. This not only minimizes the input pole creation for optimum frequency response, but also min-

imizes extraneous signal "pickup" at this node. Power supplies should be decoupled with adequate capacitance as close as possible to the device supply pin.

In addition to amplifier stability considerations, input source resistance values should be low so as to take full advantage of the low noise characteristics of the amplifier. Thermal noise (Johnson noise) of a resistor is generated by thermally-charged carriers randomly moving within the resistor creating a voltage. The rms thermal noise voltage in a resistor can be calculated from:

$$E_{nr} = \sqrt{4kTR \times BW}$$

where:

k = Boltzmann's constant (1.38×10^{-23} joules/K)

T = Kelvin temperature

R = Resistance in ohms

BW = Upper and lower frequency limit in hertz.

By way of reference, a $1.0 \text{ k}\Omega$ resistor, at 25°C , will produce $4.0 \text{ nV}/\sqrt{\text{Hz}}$ of rms noise voltage. If this resistor is connected to the input of the amplifier, the noise voltage will be gained up in accordance to the amplifiers gain configuration. For this reason the selection of input source resistance for low noise circuit applications warrants serious consideration. The total noise of the amplifier, as referred to its inputs, is typically only $4.4 \text{ nV}/\sqrt{\text{Hz}}$ at 1.0 kHz .

The output of any one amplifier is current limited and thus protected from a direct short to ground. However, under such conditions, it is important to not allow the amplifier to exceed the maximum junction temperature rating. Typically for ± 15 volt supplies, any one output can be shorted continuously to ground without exceeding the temperature rating.

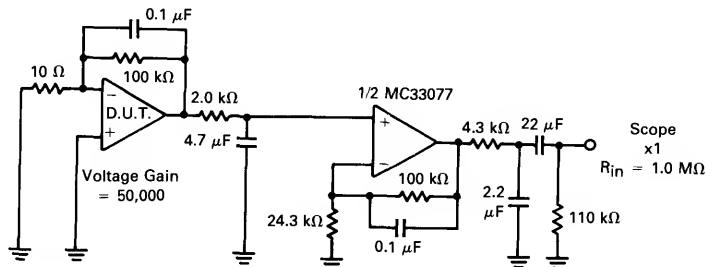


FIGURE 36 — VOLTAGE NOISE TEST CIRCUIT
(0.1 Hz-to-10 Hz_{p-p})

Note: All capacitors are non-polarized.

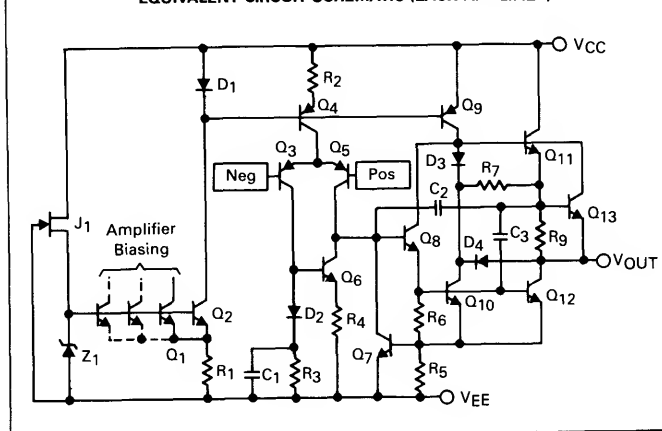
**LOW NOISE
 OPERATIONAL AMPLIFIER**

The MC33078/9 series is a family of high quality monolithic amplifiers employing Bipolar technology with innovative high-performance concepts for quality audio and data signal processing applications. This family incorporates the use of high frequency PNP input transistors to produce amplifiers exhibiting low input voltage noise with high gain bandwidth product and slew rate. The all NPN output stage exhibits no deadband crossover distortion, large output voltage swing, excellent phase and gain margins, low open-loop high frequency output impedance and symmetrical source and sink ac frequency performance.

The MC33078/9 family offers both dual and quad amplifier versions, tested over the vehicular temperature range and available in the plastic DIP and SOIC packages (P and D suffixes).

- Dual Supply Operation: ± 18 V (Max)
- Low Voltage Noise: 4.5 nV/ $\sqrt{\text{Hz}}$
- Low Input Offset Voltage: 0.15 mV
- Low T.C. of Input Offset Voltage: 2.0 $\mu\text{V}/^\circ\text{C}$
- Low Total Harmonic Distortion: 0.002%
- High Gain Bandwidth Product: 16 MHz
- High Slew Rate: 7.0 V/ μs
- High Open-Loop ac Gain: 800 @ 20 kHz
- Excellent Frequency Stability
- Large Output Voltage Swing: +14.1 V/-14.6 V

EQUIVALENT CIRCUIT SCHEMATIC (EACH AMPLIFIER)

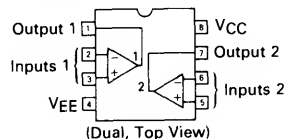
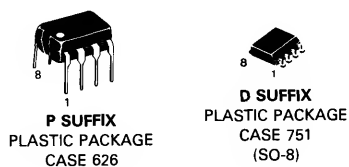


**MC33078
 MC33079**

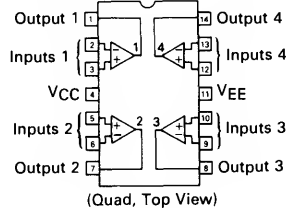
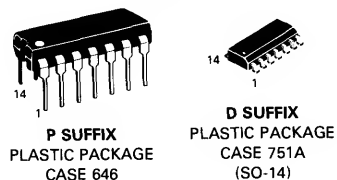
**DUAL/QUAD
 LOW NOISE
 OPERATIONAL AMPLIFIERS**

**SILICON MONOLITHIC
 INTEGRATED CIRCUIT**

MC33078



MC33079



ORDERING INFORMATION

Op Amp Function	Device	Test Temp. Range	Package
Dual	MC33078D MC33078P	-40°C to +85°C	SO-8 Plastic DIP
Quad	MC33079D MC33079P	-40°C to +85°C	SO-14 Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+36	Volts
Input Differential Voltage Range	V_{IDR}	(Note 1)	Volts
Input Voltage Range	V_{IR}	(Note 1)	Volts
Output Short-Circuit Duration (Note 2)	t_S	Indefinite	Seconds
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	-60 to +150	°C
Maximum Power Dissipation	P_D	(Note 2)	mW

Notes:

1. Either or both input voltages must not exceed the magnitude of V_{CC} or V_{EE} .
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (See power dissipation performance characteristic, Figure 1).
3. Measured with V_{CC} and V_{EE} differentially varied simultaneously.

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S = 10\ \Omega$, $V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$) MC33078 $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ MC33079 $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	$ V_{IO} $	— — —	0.15 — 0.15	2.0 3.0 2.5 3.5	mV
Average Temperature Coefficient of Input Offset Voltage $R_S = 10\ \Omega$, $V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$, $T_A = T_{low}$ to T_{high}	$\Delta V_{IO}/\Delta T$	—	2.0	—	$\mu\text{V}/^\circ\text{C}$
Input Bias Current ($V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	I_{IB}	— —	300 —	750 800	nA
Input Offset Current ($V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	I_{IO}	— —	25 —	150 175	nA
Common Mode Input Voltage Range ($\Delta V_{IO} = 5.0\text{ mV}$, $V_O = 0\text{ V}$)	V_{ICR}	± 13	± 14	—	V
Large Signal Voltage Gain ($V_O = \pm 10\text{ V}$, $R_L = 2.0\text{ k}\Omega$) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	A_{VOL}	90 85	110 —	— —	dB
Output Voltage Swing ($V_{ID} = \pm 1.0\text{ V}$) $R_L = 600\ \Omega$ $R_L = 600\ \Omega$ $R_L = 2.0\text{ k}\Omega$ $R_L = 2.0\text{ k}\Omega$ $R_L = 10\text{ k}\Omega$ $R_L = 10\text{ k}\Omega$	V_{O+} V_{O-} V_{O+} V_{O-} V_{O+} V_{O-}	— — 13.2 — 13.5 —	10.7 -11.9 13.8 -13.7 14.1 -14.6	— — — -13.2 — -14	V
Common Mode Rejection ($V_{IN} = \pm 13\text{ V}$)	CMR	80	100	—	dB
Power Supply Rejection (Note 3) $V_{CC}/V_{EE} = +15\text{ V}/-15\text{ V}$ to $+5.0\text{ V}/-5.0\text{ V}$	PSR	80	105	—	dB
Output Short Circuit Current ($V_{ID} = 1.0\text{ V}$, Output to Ground) Source Sink	I_{SC}	+15 -20	+29 -37	— —	mA
Power Supply Current ($V_O = 0\text{ V}$, All Amplifiers) MC33078 $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ MC33079 $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	I_D	— — — —	4.1 — 8.4 —	5.0 5.5 10 11	mA

MC33078, MC33079

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
Slew Rate ($V_{in} = -10\text{ V to } +10\text{ V}$, $R_L = 2.0\text{ k}\Omega$, $C_L = 100\text{ pF}$, $A_v = +1.0$)	SR	5.0	7.0	—	V/ μs
Gain BAndwidth Product ($f = 100\text{ kHz}$)	GBW	10	16	—	MHz
Unity Gain Frequency (Open-Loop)	f_U	—	9.0	—	MHz
Gain Margin ($R_L = 2.0\text{ k}\Omega$)	A_m	—	-11	—	dB
		—	-6.0	—	dB
Phase Margin ($R_L = 2.0\text{ k}\Omega$)	ϕ_m	—	55	—	Deg
		—	40	—	Deg
Channel Separation ($f = 20\text{ Hz to } 20\text{ kHz}$)	CS	—	-120	—	dB
Power Bandwidth ($V_O = 27\text{ V}_{p-p}$, $R_L = 2.0\text{ k}\Omega$, $\text{THD} \leq 1.0\%$)	BW_P	—	120	—	kHz
Distortion ($R_L = 2.0\text{ k}\Omega$, $f = 20\text{ Hz to } 20\text{ kHz}$, $V_O = 3.0\text{ V}_{rms}$, $A_v = +1.0$)	THD	—	0.002	—	%
Open-Loop Output Impedance ($V_O = 0\text{ V}$, $f = 9.0\text{ MHz}$)	$ Z_O $	—	37	—	Ω
Differential Input Resistance ($V_{CM} = 0\text{ V}$)	R_{IN}	—	175	—	$\text{k}\Omega$
Differential Input Capacitance ($V_{CM} = 0\text{ V}$)	C_{IN}	—	12	—	pF
Equivalent Input Noise Voltage ($R_S = 100\text{ }\Omega$, $f = 1.0\text{ kHz}$)	e_n	—	4.5	—	$\text{nV}/\sqrt{\text{Hz}}$
Equivalent Input Noise Current ($f = 1.0\text{ kHz}$)	i_n	—	0.5	—	$\text{pA}/\sqrt{\text{Hz}}$

TYPICAL CHARACTERISTICS

FIGURE 1 — MAXIMUM POWER DISSIPATION versus TEMPERATURE

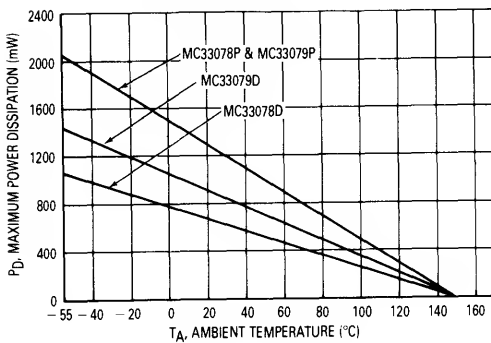


FIGURE 2 — INPUT BIAS CURRENT versus SUPPLY VOLTAGE

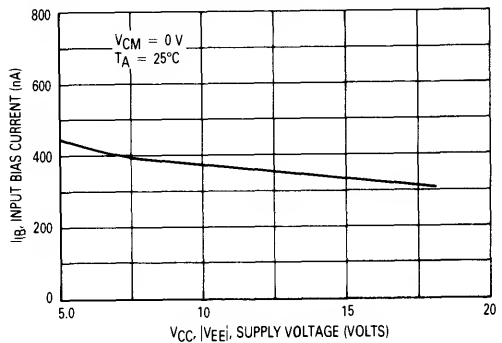


FIGURE 3 — INPUT BIAS CURRENT versus TEMPERATURE

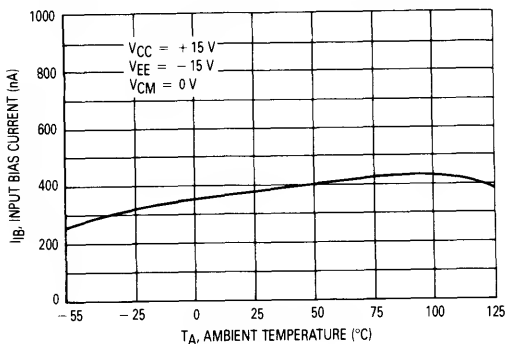
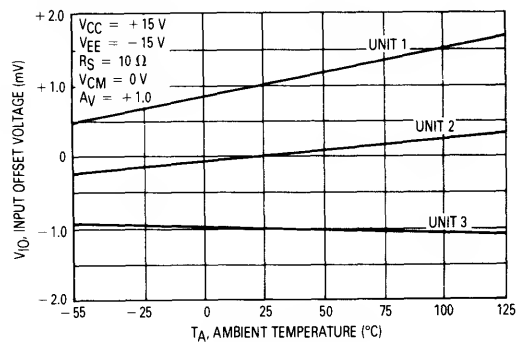


FIGURE 4 — INPUT OFFSET VOLTAGE versus TEMPERATURE



TYPICAL CHARACTERISTICS — continued

2

FIGURE 5 — INPUT BIAS CURRENT versus COMMON MODE VOLTAGE

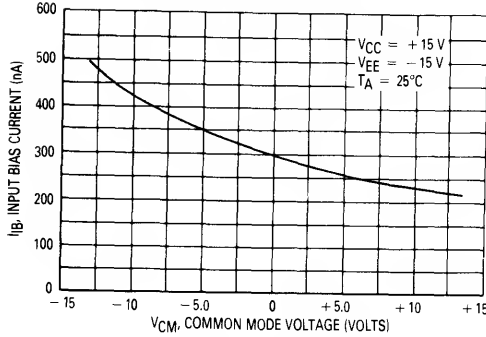


FIGURE 6 — INPUT COMMON-MODE VOLTAGE RANGE versus TEMPERATURE

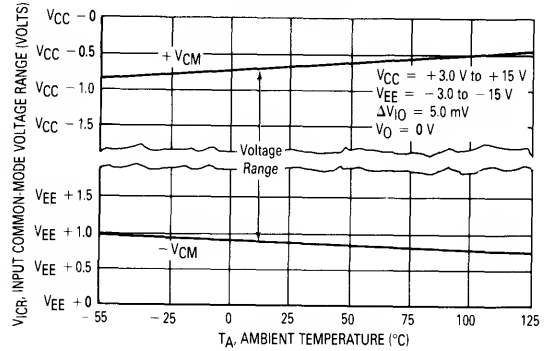


FIGURE 7 — OUTPUT SATURATION VOLTAGE versus LOAD RESISTANCE TO GROUND

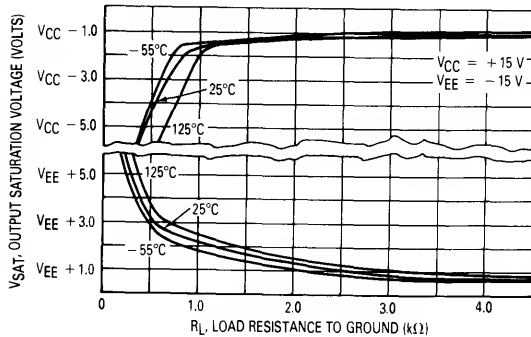


FIGURE 8 — OUTPUT SHORT CIRCUIT CURRENT versus TEMPERATURE

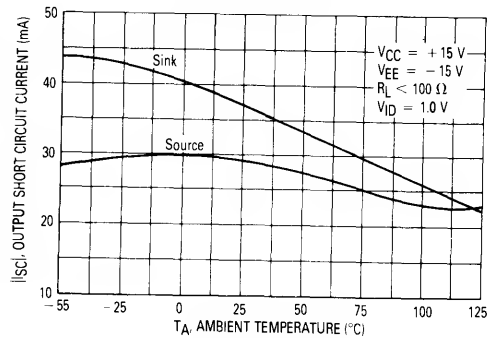


FIGURE 9 — SUPPLY CURRENT versus TEMPERATURE

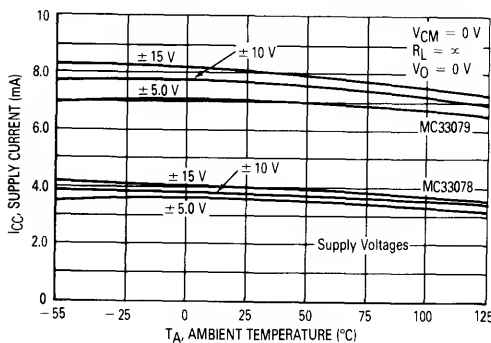


FIGURE 10 — COMMON MODE REJECTION versus FREQUENCY

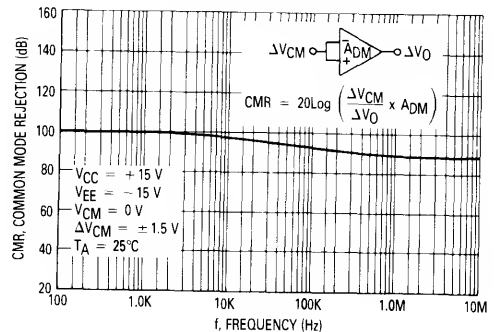


FIGURE 11 — POWER SUPPLY REJECTION
versus FREQUENCY

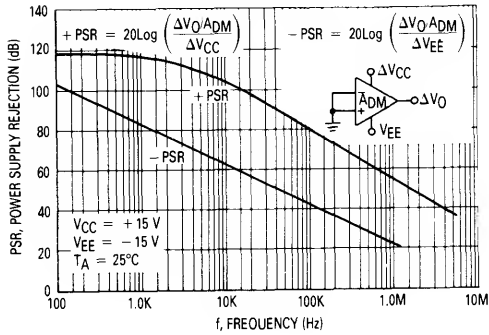


FIGURE 12 — GAIN BANDWIDTH PRODUCT versus
SUPPLY VOLTAGE

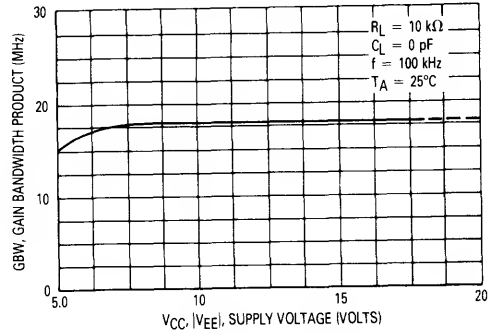


FIGURE 13 — GAIN BANDWIDTH PRODUCT
versus TEMPERATURE

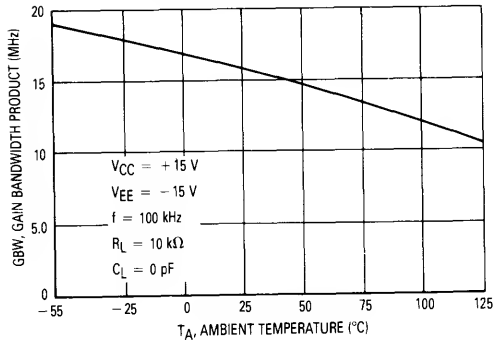


FIGURE 14 — MAXIMUM OUTPUT VOLTAGE
versus SUPPLY VOLTAGE

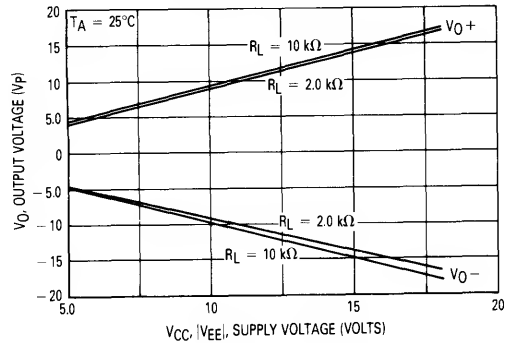


FIGURE 15 — OUTPUT VOLTAGE versus FREQUENCY

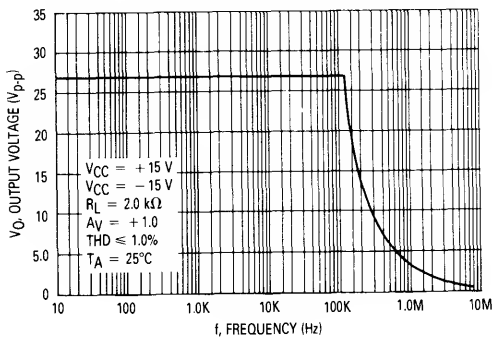
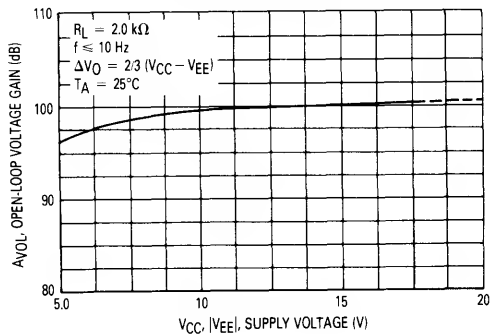


FIGURE 16 — OPEN-LOOP VOLTAGE GAIN versus
SUPPLY VOLTAGE



TYPICAL CHARACTERISTICS — continued

2

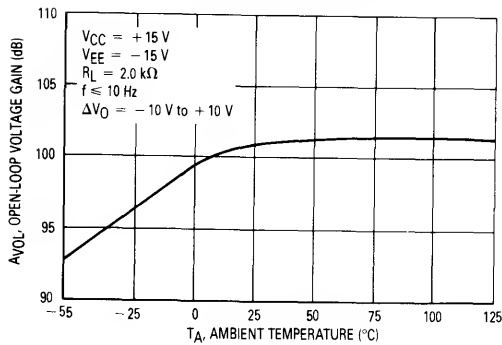
FIGURE 17 — OPEN-LOOP VOLTAGE GAIN
versus TEMPERATURE

FIGURE 18 — OUTPUT IMPEDANCE versus FREQUENCY

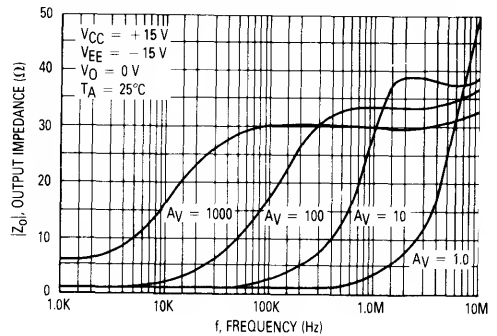


FIGURE 19 — CHANNEL SEPARATION versus FREQUENCY

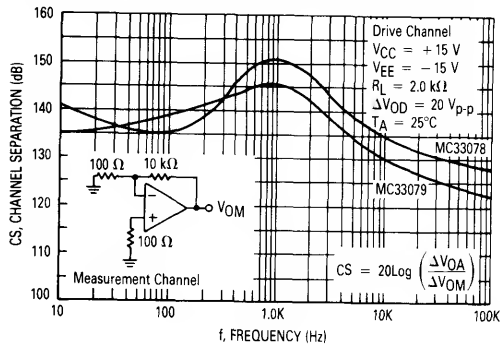
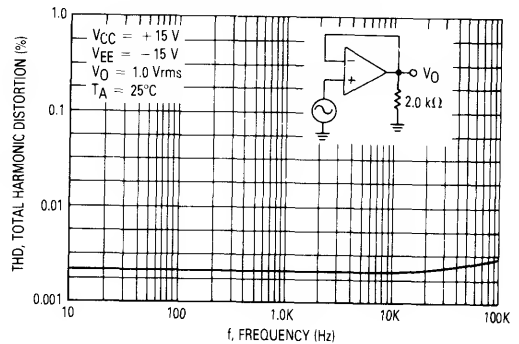
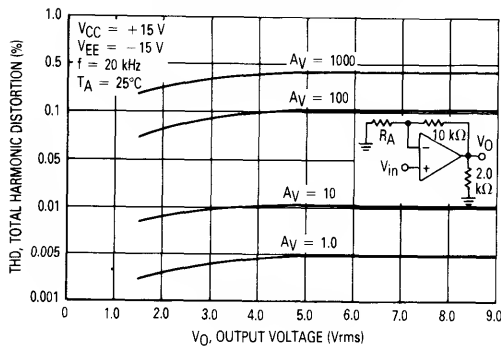
FIGURE 20 — TOTAL HARMONIC DISTORTION
versus FREQUENCYFIGURE 21 — TOTAL HARMONIC DISTORTION
versus OUTPUT VOLTAGE

FIGURE 22 — SLEW RATE versus SUPPLY VOLTAGE

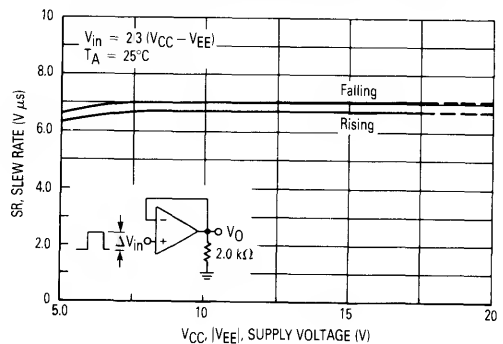


FIGURE 23 — SLEW RATE versus TEMPERATURE

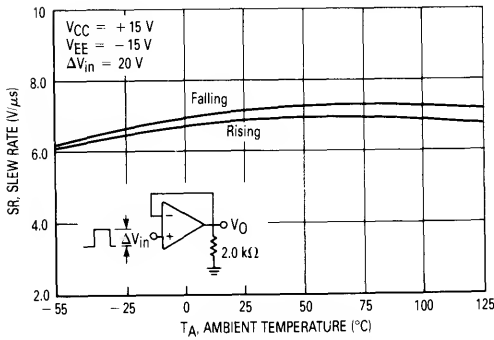


FIGURE 24 — VOLTAGE GAIN AND PHASE versus FREQUENCY

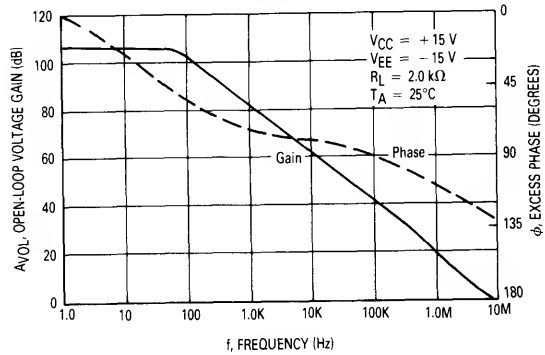


FIGURE 25 — OPEN-LOOP GAIN MARGIN AND PHASE MARGIN versus LOAD CAPACITANCE

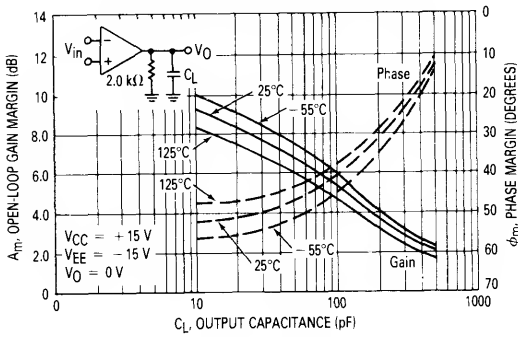


FIGURE 26 — OVERSHOOT versus OUTPUT LOAD CAPACITANCE

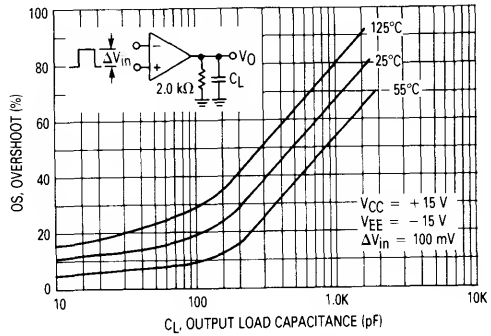


FIGURE 27 — INPUT REFERRED NOISE VOLTAGE AND CURRENT versus FREQUENCY

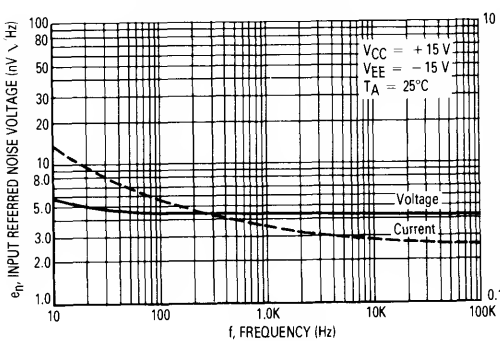
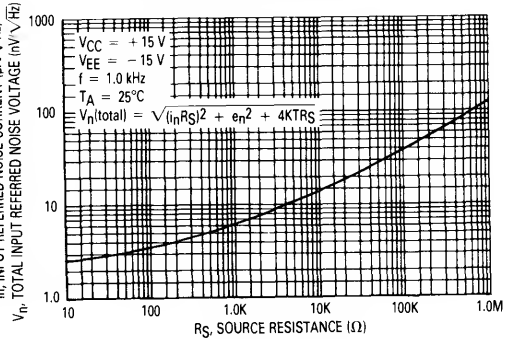


FIGURE 28 — TOTAL INPUT REFERRED NOISE VOLTAGE versus SOURCE RESISTANCE



TYPICAL CHARACTERISTICS — continued

FIGURE 29 — PHASE MARGIN AND GAIN MARGIN versus DIFFERENTIAL SOURCE RESISTANCE

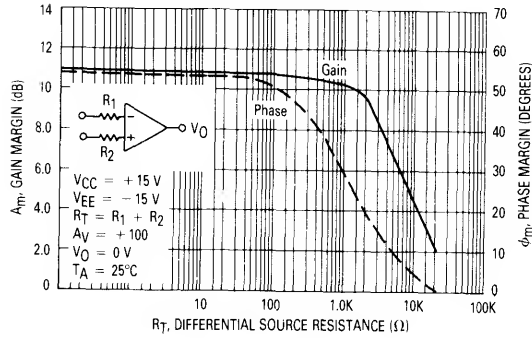


FIGURE 30 — INVERTING AMPLIFIER SLEW RATE

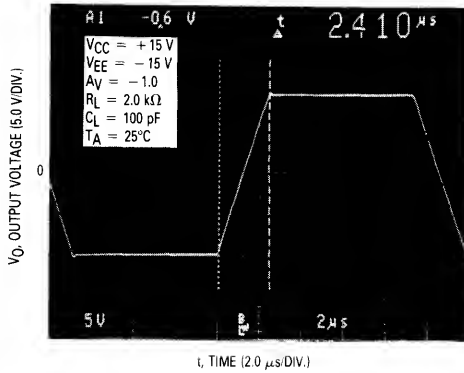


FIGURE 31 — NON-INVERTING AMPLIFIER SLEW RATE

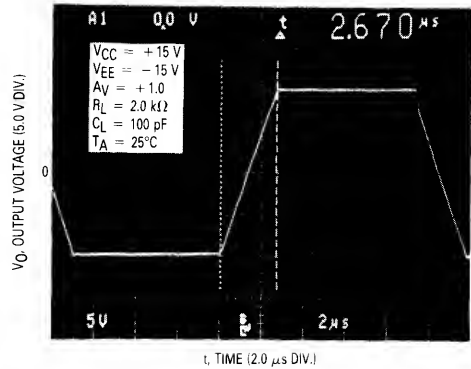


FIGURE 32 — NON-INVERTING AMPLIFIER OVERSHOOT

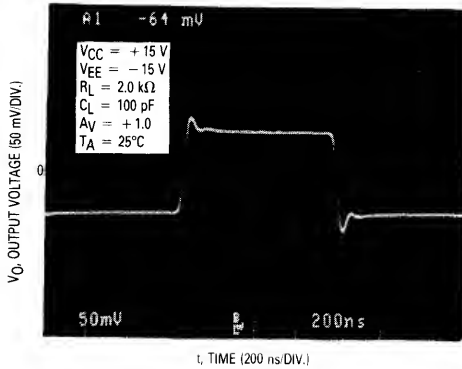
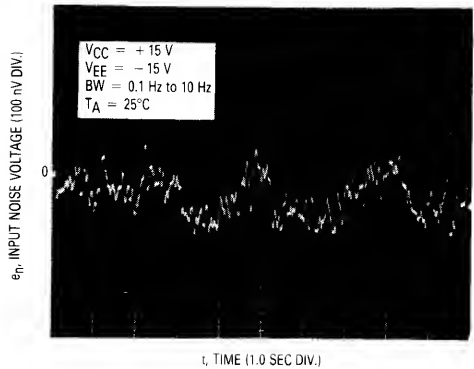
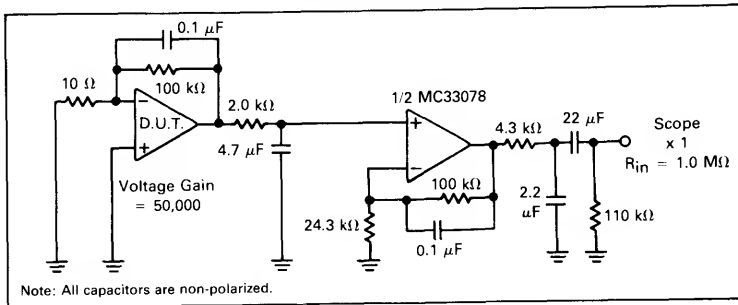


FIGURE 33 — LOW FREQUENCY NOISE VOLTAGE versus TIME



MC33078, MC33079

FIGURE 34 — VOLTAGE NOISE TEST CIRCUIT
(0.1 Hz-TO-10 Hz_{p-p})



2

**LOW POWER, SINGLE SUPPLY
OPERATIONAL AMPLIFIERS**

Quality bipolar fabrication with innovative design concepts are employed for the MC33171/2/4, MC35171/2/4 series of monolithic operational amplifiers. This series of operational amplifiers operates at 180 μ A per amplifier and offers 1.8 MHz of gain bandwidth product and 2.1 V/ μ s slew rate without the use of JFET device technology. Although this series can be operated from split supplies, it is particularly suited for single supply operation, since the common mode input voltage range includes ground potential (V_{EE}). With a Darlington input stage, this series exhibits high input resistance, low input offset voltage and high gain. The all NPN output stage, characterized by no deadband crossover distortion and large output voltage swing, provides high capacitance drive capability, excellent phase and gain margins, low open-loop high frequency output impedance and symmetrical source/sink AC frequency response.

The MC33171/2/4, MC35171/2/4 series of devices are specified over the industrial/vehicular or military temperature ranges. The complete series of single, dual and quad operational amplifiers are available in the plastic and ceramic DIP as well as the SOIC surface mount packages.

- Low Supply Current: 180 μ A (Per Amplifier)
- Wide Supply Operating Range: +3.0 V to +44 V or ± 1.5 V to ± 22 V
- Wide Input Common Mode Range Including Ground (V_{EE})
- Wide Bandwidth: 1.8 MHz
- High Slew Rate: 2.1 V/ μ s
- Low Input Offset Voltage: 2.0 mV
- Large Output Voltage Swing: -14.2 V to $+14.2$ V (with ± 15 V Supplies)
- Large Capacitance Drive Capability: 0 to 500 pF
- Low Total Harmonic Distortion: 0.03%
- Excellent Phase Margin: 60°
- Excellent Gain Margin: 15 dB
- Output Short Circuit Protection

ORDERING INFORMATION


Op Amp Function	Device	Temperature Range	Package
Single	MC33171D	-40 to +85°C	SO-8
	MC35171U	-55 to +125°C	Ceramic DIP
	MC33171P	-40 to +85°C	Plastic DIP
Dual	MC33172D	-40 to +85°C	SO-8
	MC35172U	-55 to +125°C	Ceramic DIP
	MC33172P	-40 to +85°C	Plastic DIP
Quad	MC33174D	-40 to +85°C	SO-14
	MC35174L	-55 to +125°C	Ceramic DIP
	MC33174P	-40 to +85°C	Plastic DIP

**MC33171, MC35171
MC33172, MC35172
MC33174, MC35174**

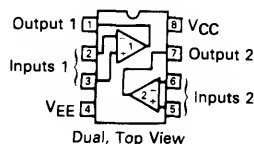
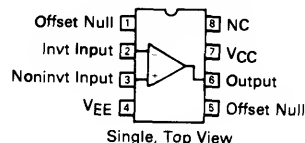
**LOW POWER, SINGLE SUPPLY
OPERATIONAL AMPLIFIERS**


P SUFFIX
PLASTIC PACKAGE
CASE 626


U SUFFIX
CERAMIC PACKAGE
CASE 693



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

PIN ASSIGNMENTS

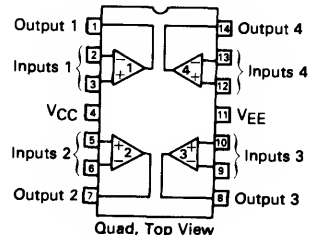



P SUFFIX
PLASTIC PACKAGE
CASE 646


L SUFFIX
CERAMIC PACKAGE
CASE 632


D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

PIN ASSIGNMENTS



MC33171, MC33172, MC33174, MC35171, MC35172, MC35174

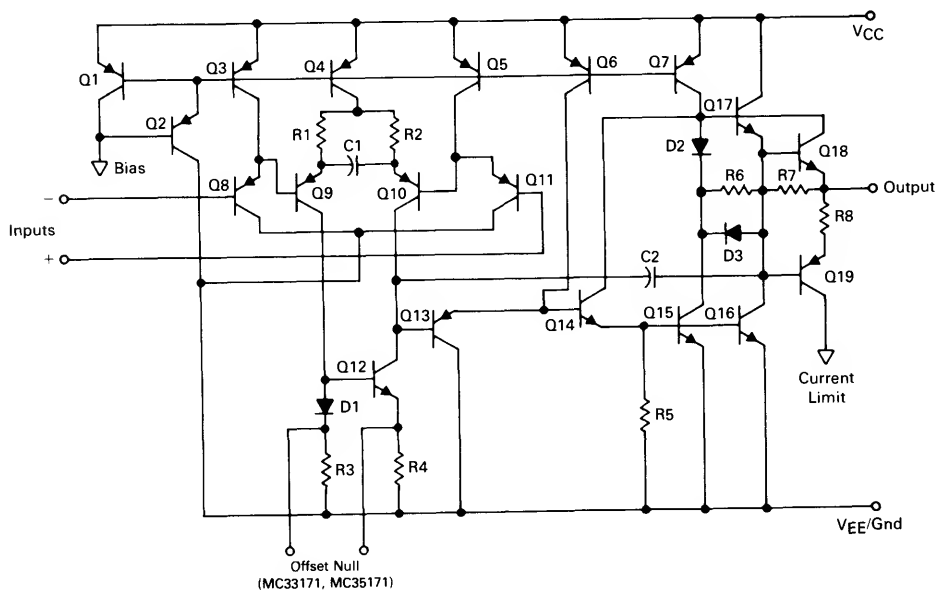
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}/V_{EE}	± 22	Volts
Input Differential Voltage Range	V_{IDR}	(Note 1)	Volts
Input Voltage Range	V_{IR}	(Note 1)	Volts
Output Short Circuit Duration (Note 2)	t_S	Indefinite	Seconds
Operating Ambient Temperature Range MC35171/MC35172/MC35174 MC33171/MC33172/MC33174	T_A	-55 to $+125$ -40 to $+85$	$^{\circ}\text{C}$
Operating Junction Temperature	T_J	$+150$	$^{\circ}\text{C}$
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}	-65 to $+150$ -55 to $+125$	$^{\circ}\text{C}$

Notes: 1. Either or both input voltages must not exceed the magnitude of V_{CC} or V_{EE} .

2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded.

EQUIVALENT CIRCUIT SCHEMATIC (EACH AMPLIFIER)



MC33171, MC33172, MC33174, MC35171, MC35172, MC35174

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, R_L connected to ground, $T_A = T_{\text{low}}$ to T_{high} [Note 3] unless otherwise noted.)

unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($V_{CM} = 0\text{ V}$) $V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = +25^\circ\text{C}$ $V_{CC} = +5\text{ V}$, $V_{EE} = 0\text{ V}$, $T_A = +25^\circ\text{C}$ $V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = T_{\text{low}}$ to T_{high}	V_{IO}	— — —	2.0 2.5 —	4.5 5.0 6.5	mV
Average Temperature Coefficient of Offset Voltage	$\Delta V_{IO}/\Delta T$	—	10	—	$\mu\text{V}/^\circ\text{C}$
Input Bias Current ($V_{CM} = 0\text{ V}$) $T_A = +25^\circ\text{C}$ $T_A = T_{\text{low}}$ to T_{high}	I_{IB}	— —	20 —	100 200	nA
Input Offset Current ($V_{CM} = 0\text{ V}$) $T_A = +25^\circ\text{C}$ $T_A = T_{\text{low}}$ to T_{high}	I_{IO}	— —	5.0 —	20 40	nA
Large Signal Voltage Gain ($V_O = \pm 10\text{ V}$, $R_L = 10\text{ k}$) $T_A = +25^\circ\text{C}$ $T_A = T_{\text{low}}$ to T_{high}	A_{VOL}	50 25	500 —	— —	V/mV
Output Voltage Swing $V_{CC} = +5.0\text{ V}$, $V_{EE} = 0\text{ V}$, $R_L = 10\text{ k}$, $T_A = +25^\circ\text{C}$ $V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $R_L = 10\text{ k}$, $T_A = +25^\circ\text{C}$ $V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $R_L = 10\text{ k}$, $T_A = T_{\text{low}}$ to T_{high} $V_{CC} = +5.0\text{ V}$, $V_{EE} = 0\text{ V}$, $R_L = 10\text{ k}$, $T_A = +25^\circ\text{C}$ $V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $R_L = 10\text{ k}$, $T_A = +25^\circ\text{C}$ $V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $R_L = 10\text{ k}$, $T_A = T_{\text{low}}$ to T_{high}	V_{OH}	3.5 13.6 13.3	4.3 14.2 —	— — —	V
	V_{OL}	— — —	0.05 -14.2 —	0.15 -13.6 -13.3	
Output Short Circuit Current ($T_A = +25^\circ\text{C}$) Input Overdrive = 1.0 V, Output to Ground Source Sink	I_{SC}	3.0 15	5.0 27	— —	mA
Input Common Mode Voltage Range $T_A = +25^\circ\text{C}$ $T_A = T_{\text{low}}$ to T_{high}	V_{ICR}	V_{EE} to ($V_{CC} - 1.8$) V_{EE} to ($V_{CC} - 2.2$)			V
Common Mode Rejection Ratio ($R_S \leq 10\text{ k}$)	CMRR	80	90	—	dB
Power Supply Rejection Ratio ($R_S = 100\ \Omega$)	PSRR	80	100	—	dB
Power Supply Current (Per Amplifier) $V_{CC} = +5.0\text{ V}$, $V_{EE} = 0\text{ V}$, $T_A = +25^\circ\text{C}$ $V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = +25^\circ\text{C}$ $V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = T_{\text{low}}$ to T_{high}	I_D	— — —	180 220 —	250 250 300	μA

Notes: (continued)

3. $T_{\text{low}} = -55^\circ\text{C}$ for MC35171/MC35172/MC35174
 $= -40^\circ\text{C}$ for MC33171/MC33172/MC33174

$T_{\text{high}} = +125^\circ\text{C}$ for MC35171/MC35172/MC35174
 $= +85^\circ\text{C}$ for MC33171/MC33172/MC33174

MC33171, MC33172, MC33174, MC35171, MC35172, MC35174

2

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, R_L connected to ground, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Slew Rate ($V_{in} = -10\text{ V to } +10\text{ V}$, $R_L = 10\text{ k}$, $C_L = 100\text{ pF}$) $A_V + 1$ $A_V - 1$	SR	1.6 —	2.1 2.1	— —	$\text{V}/\mu\text{s}$
Gain Bandwidth Product ($f = 100\text{ kHz}$)	GBW	1.4	1.8	—	MHz
Power Bandwidth $A_V = +1.0$, $R_L = 10\text{ k}$, $V_O = 20\text{ V}_{p-p}$, THD = 5%	BWp	—	35	—	kHz
Phase Margin $R_L = 10\text{ k}$ $R_L = 10\text{ k}$, $C_L = 100\text{ pF}$	ϕ_m	— —	60 45	—	Degrees
Gain Margin $R_L = 10\text{ k}$ $R_L = 10\text{ k}$, $C_L = 100\text{ pF}$	A_m	— —	15 5.0	—	dB
Equivalent Input Noise Voltage $R_S = 100\ \Omega$, $f = 1.0\text{ kHz}$	e_n	—	32	—	$\text{nV}/\sqrt{\text{Hz}}$
Equivalent Input Noise Current ($f = 1.0\text{ kHz}$)	i_n	—	0.2	—	$\text{pA}/\sqrt{\text{Hz}}$
Differential Input Resistance $V_{CM} = 0\text{ V}$	R_{IN}	—	300	—	$\text{M}\Omega$
Input Capacitance	C_i	—	0.8	—	pF
Total Harmonic Distortion $A_V = +10$, $R_L = 10\text{ k}$, $2.0\text{ V}_{p-p} \leq V_O \leq 20\text{ V}_{p-p}$, $f = 10\text{ kHz}$	THD	—	0.03	—	%
Channel Separation ($f = 10\text{ kHz}$)	—	—	120	—	dB
Open-Loop Output Impedance ($f = 1.0\text{ MHz}$)	z_o	—	100	—	Ω

TYPICAL PERFORMANCE CURVES

FIGURE 1 — INPUT COMMON-MODE VOLTAGE RANGE versus TEMPERATURE

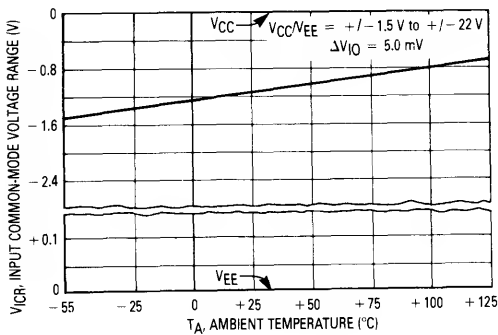
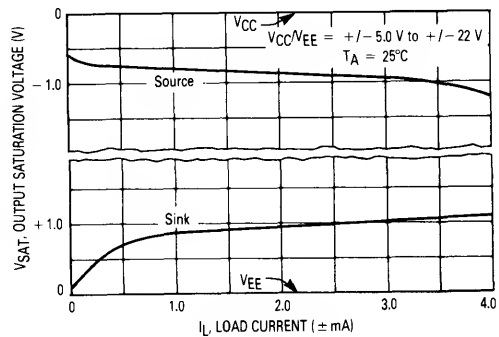


FIGURE 2 — SPLIT SUPPLY OUTPUT SATURATION versus LOAD CURRENT



2

FIGURE 3 — OPEN-LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY

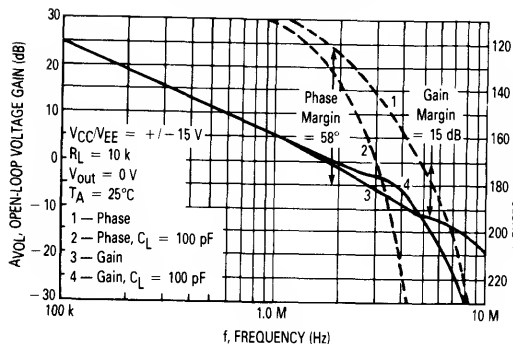


FIGURE 4 — PHASE MARGIN AND PERCENT OVERSHOOT versus LOAD CAPACITANCE

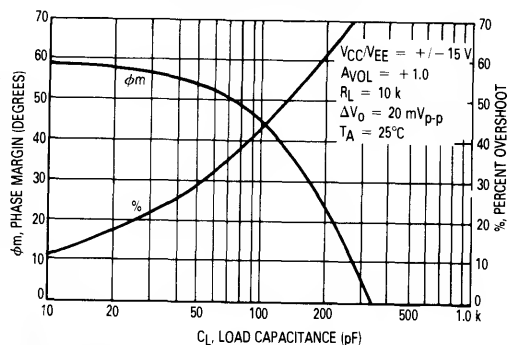


FIGURE 5 — NORMALIZED GAIN BANDWIDTH PRODUCT AND SLEW RATE versus TEMPERATURE

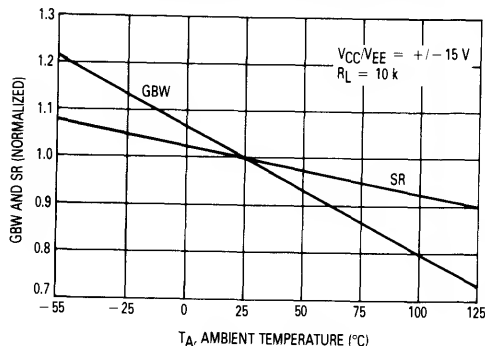


FIGURE 6 — SMALL AND LARGE SIGNAL TRANSIENT RESPONSE

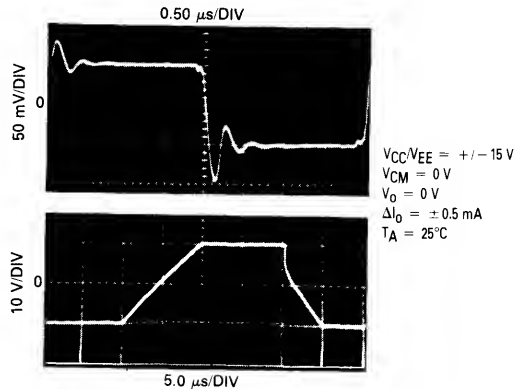


FIGURE 7 — OUTPUT IMPEDANCE versus FREQUENCY

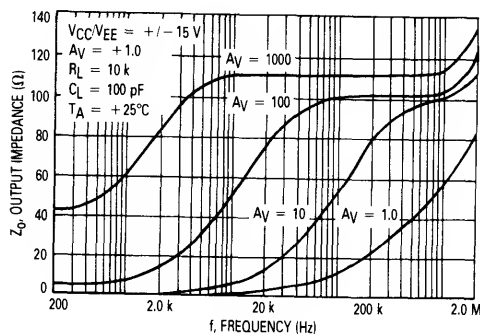
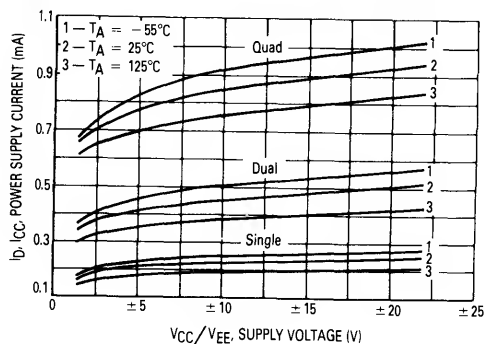


FIGURE 8 — SUPPLY CURRENT versus SUPPLY VOLTAGE



APPLICATIONS INFORMATION

CIRCUIT DESCRIPTION/PERFORMANCE FEATURES

Although the bandwidth, slew rate, and settling time of the MC33171/72/74 amplifier family is similar to low power op amp products utilizing JFET input devices, these amplifiers offer additional advantages as a result of the PNP transistor differential inputs and an all NPN transistor output stage.

Because the input common mode voltage range of this input stage includes the V_{EE} potential, single supply operation is feasible to as low as 3.0 volts with the common mode input voltage at ground potential.

The input stage also allows differential input voltages up to ± 44 volts, provided the maximum input voltage range is not exceeded. Specifically, the input voltages must range between V_{CC} and V_{EE} supply voltages as shown by the maximum rating table. In practice, although *not recommended*, the input voltages can exceed the V_{CC} voltage by approximately 3.0 volts and decrease below the V_{EE} voltage by 0.3 volts without causing product damage, although output phase reversal may occur. It is also possible to source up to 5.0 mA of current from V_{EE} through either input's clamping diode without damage or latching, but phase reversal may again occur. If at least one input is within the common mode input voltage range and the other input is within the maximum input voltage range, no phase reversal will occur. If both inputs exceed the upper common mode input voltage limit, the output will be forced to its lowest voltage state.

Since the input capacitance associated with the small geometry input device is substantially lower (0.8 pF) than that of a typical JFET (3.0 pF), the frequency response for a given input source resistance is greatly enhanced. This becomes evident in D-to-A current to voltage conversion applications where the feedback resistance can form a pole with the input capacitance of the op amp. This input pole creates a 2nd order system with the single pole op amp and is therefore detrimental to its settling time. In this context, lower input capacitance is desirable especially for higher values of feedback resistances (lower current DAC's). This input pole can be compensated for by creating a feedback zero with a capacitance across the feedback resistance, if necessary, to reduce overshoot. For 10 k Ω of feedback resistance, the MC33171/72/74 family can typically settle to within 1/2 LSB of 8 bits in 4.2 μ s, and within 1/2 LSB of 12 bits in 4.8 μ s for a 10 volt step. In a standard inverting unity gain fast settling configuration, the symmetrical slew rate is typically ± 2.1 volts/ μ s. In the classic noninverting unity gain configuration the typical output positive slew rate is also 2.1 volts/ μ s, and the corresponding negative slew rate will usually exceed the positive slew rate as a function of the fall time of the input waveform.

The all NPN output stage, shown in its basic form on the equivalent circuit schematic, offers unique advantages over the more conventional NPN/PNP transistor Class AB output stage. A 10 k Ω load resistance can typically swing within 0.8 volt of the positive rail (V_{CC}) and negative rail (V_{EE}), providing a 28.4 Vp-p swing from ± 15 volt supplies. This large output swing becomes most noticeable at lower supply voltages.

The positive swing is limited by the saturation voltage of the current source transistor Q7, the V_{BE} of the NPN pull up transistor Q17, and the voltage drop associated with the short circuit resistance, R_5 . For sink currents less than 0.4 mA, the negative swing is limited by the saturation voltage of the pull-down transistor Q15, and the voltage drop across R_4 and R_5 . For small valued sink currents, the above voltage drops are negligible, allowing the negative swing voltage to approach within millivolts

of V_{EE} . For sink currents (> 0.4 mA), diode D3 clamps the voltage across R_4 . Thus the negative swing is limited by the saturation voltage of Q15, plus the forward diode drop of D3 ($\approx V_{EE} + 1.0$ V). Therefore an unprecedented peak-to-peak output voltage swing is possible for a given supply voltage as indicated by the output swing specifications.

If the load resistance is referenced to V_{CC} instead of ground for single supply applications, the maximum possible output swing can be achieved for a given supply voltage. For light load currents, the load resistance will pull the output to V_{CC} during the positive swing and the output will pull the load resistance near ground during the negative swing. The load resistance value should be much less than that of the feedback resistance to maximize pull up capability.

Because the PNP output emitter follower transistor has been eliminated, the MC33171/72/74 family offers a 15 mA minimum current sink capability, typically to an output voltage of ($V_{EE} + 1.8$ V). In single supply applications the output can directly source or sink base current from a common emitter NPN transistor for high current switching applications.

In addition, the all NPN transistor output stage is inherently faster than PNP types, contributing to the bipolar amplifier's improved gain bandwidth products. The associated high frequency low output impedance (200 Ω typ @ 1.0 MHz) allows capacitive drive capability from 0 to 400 pF without oscillation in the noninverting unity gain configuration. The 60° phase margin and 15 dB gain margin as well as the general gain and phase characteristics are virtually independent of the source/sink output swing conditions. This allows easier system phase compensation, since output swing will not be a phase consideration. The ac characteristics of the MC33171/72/74 family also allow excellent active filter capability, especially for low voltage single supply applications.

Although the single supply specification is defined at 5.0 volts, these amplifiers are functional to at least 3.0 volts @ 25°C. However slight changes in parametrics such as bandwidth, slew rate, and dc gain may occur.

If power to this integrated circuit is applied in reverse polarity or if the IC is installed backwards in a socket, large unlimited current surges will occur through the device that may result in device destruction.

As usual with most high frequency amplifiers, proper lead dress, component placement and PC board layout should be exercised for optimum frequency performance. For example, long unshielded input or output leads may result in unwanted input output coupling. In order to preserve the relatively low input capacitance associated with these amplifiers, resistors connected to the inputs should be immediately adjacent to the input pin to minimize additional stray input capacitance. This not only minimizes the input pole for optimum frequency response, but also minimizes extraneous "pick up" at this node. Supply decoupling with adequate capacitance immediately adjacent to the supply pin is also important, particularly over temperature, since many types of decoupling capacitors exhibit great impedance changes over temperature.

The output of any one amplifier is current limited and thus protected from a direct short to ground. However, under such conditions, it is important not to allow the device to exceed the maximum junction temperature rating. Typically for ± 15 volt supplies, any one output can be shorted continuously to ground without exceeding the maximum temperature rating.

FIGURE 9 — AC COUPLED NONINVERTING AMPLIFIER WITH SINGLE +5.0 V SUPPLY

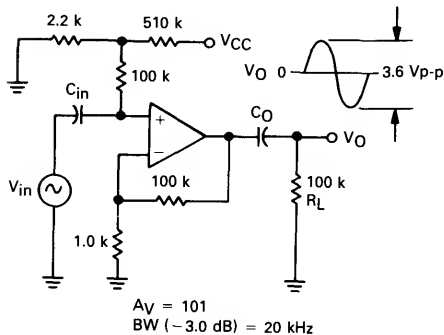


FIGURE 10 — AC COUPLED INVERTING AMPLIFIER WITH SINGLE +5.0 V SUPPLY

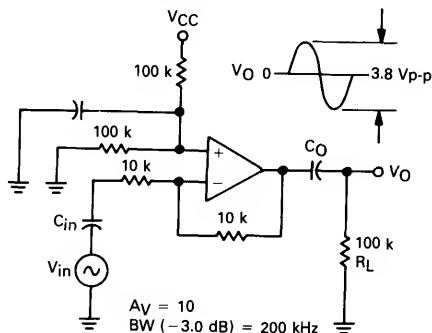


FIGURE 11 — DC COUPLED INVERTING AMPLIFIER MAXIMUM OUTPUT SWING WITH SINGLE +5.0 V SUPPLY

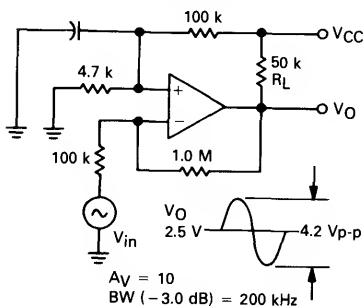
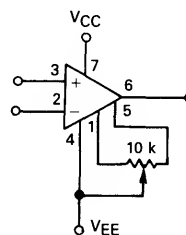


FIGURE 12 — OFFSET NULLING CIRCUIT



Offset Nulling range is approximately $\pm 80 \text{ mV}$ with a 10 k potentiometer, MC33171/MC35171 only.

FIGURE 13 — ACTIVE HIGH-Q NOTCH FILTER

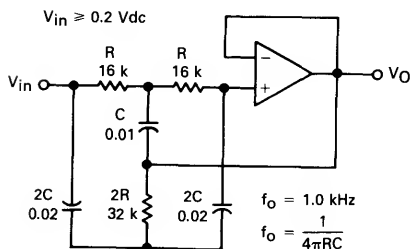
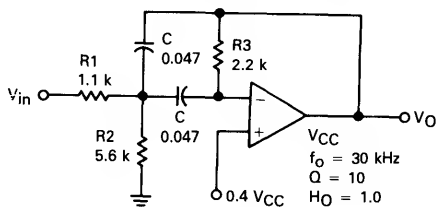


FIGURE 14 — ACTIVE BANDPASS FILTER



Given f_o = Center Frequency

A_o = Gain at Center Frequency

Choose Value f_o , Q , A_o , C

Then

For less than 10% error from operational amplifier
 Where f_o and GBW are expressed in Hz.

$$R1 = \frac{R3}{2 H_o} \quad R2 = \frac{R1 R3}{4 Q^2 R1 - R3}$$

$$R3 = \frac{Q}{\pi f_o C} \quad \frac{Q_o f_o}{GBW} < 0.1$$

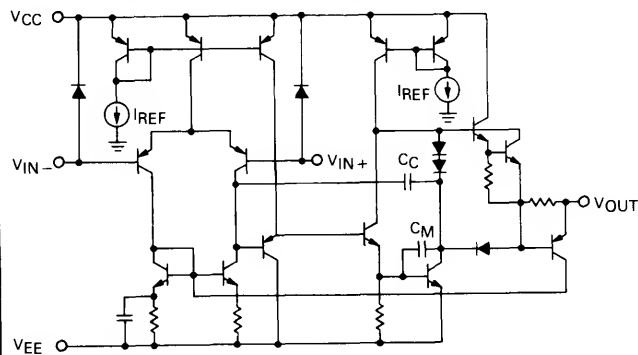
**HIGH OUTPUT CURRENT
 LOW POWER, LOW NOISE
 BIPOLAR OPERATIONAL AMPLIFIERS**

The MC33178/9 series is a family of high quality monolithic amplifiers employing Bipolar technology with innovative high performance concepts for quality audio and data signal processing applications. This device family incorporates the use of high frequency PNP input transistors to produce amplifiers exhibiting low input offset voltage, noise and distortion. In addition, the amplifier provides high output current drive capability while consuming only 420 μ A of drain current per amplifier. The NPN output stage used, exhibits no deadband crossover distortion, large output voltage swing, excellent phase and gain margins, low open-loop high frequency output impedance, symmetrical source and sink ac frequency performance.

The MC33178/9 family offers both dual and quad amplifier versions, tested over the vehicular temperature range. These devices are available in DIP and SOIC packages.

- 600 Ω Output Drive Capability
- Large Output Voltage Swing
- Low Offset Voltage: 0.15 mV (Mean)
- Low T.C. of Input Offset Voltage: 2.0 μ V/ $^{\circ}$ C
- Low Total Harmonic Distortion: 0.0024%
 (@ 1.0 kHz w/600 Ω Load)
- High Gain Bandwidth: 5.0 MHz
- High Slew Rate: 2.0 V/ μ s
- Dual Supply Operation: \pm 2.0 V to \pm 18 V

EQUIVALENT CIRCUIT SCHEMATIC (EACH AMPLIFIER)

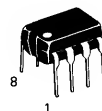


ORDERING INFORMATION

Op Amp Function	Fully Compensated	Temperature Range	Package
Dual	MC33178D MC33178P	-40 $^{\circ}$ C to +85 $^{\circ}$ C	SO-8 Plastic DIP
Quad	MC33179D MC33179P		SO-14 Plastic DIP

**MC33178
 MC33179**

**HIGH OUTPUT CURRENT
 LOW POWER, LOW NOISE
 OPERATIONAL AMPLIFIERS**

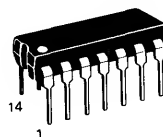
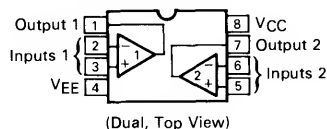


P SUFFIX
 PLASTIC PACKAGE
 CASE 626



D SUFFIX
 PLASTIC PACKAGE
 CASE 751
 (SO-8)

PIN ASSIGNMENTS

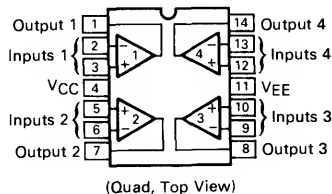


P SUFFIX
 PLASTIC PACKAGE
 CASE 646



D SUFFIX
 PLASTIC PACKAGE
 CASE 751A
 (SO-14)

PIN ASSIGNMENTS



MC33178, MC33179

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+36	Volts
Input Differential Voltage Range	V_{IDR}	(Note 1)	Volts
Input Voltage Range	V_{IR}	(Note 1)	Volts
Output Short Circuit Duration (Note 2)	t_S	Indefinite	Seconds
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	-60 to +150	°C
Maximum Power Dissipation	P_D	(Note 2)	mW

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = 25^\circ\text{C}$ unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S = 50\ \Omega$, $V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$) ($V_{CC} = +2.5\text{ V}$, $V_{EE} = -2.5\text{ V}$ to $V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	2	$ V_{IO} $	— —	0.15 —	3.0 4.0	mV
Average Temperature Coefficient of Input Offset Voltage ($R_S = 50\ \Omega$, $V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$) $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	2	$\Delta V_{IO}/\Delta T$	—	2.0	—	$\mu\text{V}/^\circ\text{C}$
Input Bias Current ($V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	3, 4	I_{IB}	— —	100 —	500 600	nA
Input Offset Current ($V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		$ I_{IO} $	— —	5.0 —	50 60	nA
Common Mode Input Voltage Range ($\Delta V_{IO} = 5.0\text{ mV}$, $V_O = 0\text{ V}$)	5	V_{ICR}	-13 —	-14 +14	— +13	V
Large Signal Voltage Gain ($V_O = -10\text{ V}$ to $+10\text{ V}$, $R_L = 600\ \Omega$) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	6, 7	A_{VOL}	50 k 25 k	200 k —	— —	V/V
Output Voltage Swing ($V_{ID} = \pm 1.0\text{ V}$) ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$) $R_L = 300\ \Omega$ $R_L = 300\ \Omega$ $R_L = 600\ \Omega$ $R_L = 600\ \Omega$ $R_L = 2.0\text{ k}\Omega$ $R_L = 2.0\text{ k}\Omega$ ($V_{CC} = +2.5\text{ V}$, $V_{EE} = -2.5\text{ V}$) $R_L = 600\ \Omega$ $R_L = 600\ \Omega$	8, 9, 10	V_{O+} V_{O-} V_{O+} V_{O-} V_{O+} V_{O-} V_{O+} V_{O-}	— — +12 — +13 — +13 —	+12 -12 +13.6 -13 +14 -13.8	— — — -12 — -13	V
Common Mode Rejection ($V_{in} = \pm 13\text{ V}$)	11	CMR	80	110	—	dB
Power Supply Rejection $V_{CC}/V_{EE} = +15\text{ V}/-15\text{ V}$, $+5.0\text{ V}/-15\text{ V}$, $+15\text{ V}/-5.0\text{ V}$	12	PSR	80	110	—	dB
Output Short Circuit Current ($V_{ID} = \pm 1.0\text{ V}$, Output to Ground) Source ($V_{CC} = 2.5\text{ V}$ to 15 V) Sink ($V_{EE} = -2.5\text{ V}$ to -15 V)	13, 14	I_{SC}	+50 -50	+80 -100	— —	mA
Power Supply Current ($V_O = 0\text{ V}$) ($V_{CC} = 2.5\text{ V}$, $V_{EE} = -2.5\text{ V}$ to $V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$) MC33178 (Dual) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ MC33179 (Quad) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	15	I_D	— — — —	— — 1.7 —	1.4 1.6 2.4 2.8	mA

NOTES:

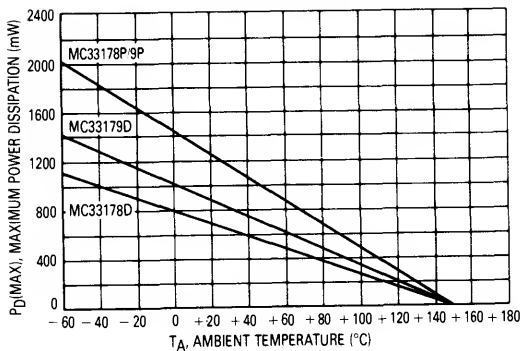
- Either or both input voltages should not exceed V_{CC} or V_{EE} .
- Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded. (See power dissipation performance characteristic, Figure 1.)

MC33178, MC33179

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = 25^\circ\text{C}$ unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Slew Rate ($V_{in} = -10\text{ V}$ to $+10\text{ V}$, $R_L = 2.0\text{ k}\Omega$, $C_L = 100\text{ pF}$, $A_V = +1.0\text{ V}$)	16, 31	SR	1.2	2.0	—	$\text{V}/\mu\text{s}$
Gain Bandwidth Product ($f = 100\text{ kHz}$)	17	GBW	2.5	5.0	—	MHz
AC Voltage Gain ($R_L = 600\ \Omega$, $V_O = 0\text{ V}$, $f = 20\text{ kHz}$)	18, 19	A_{VO}	—	50	—	dB
Unity Gain Frequency (Open-Loop) ($R_L = 600\ \Omega$, $C_L = 0\text{ pF}$)		f_U	—	3.0	—	MHz
Gain Margin ($R_L = 600\ \Omega$, $C_L = 0\text{ pF}$)	20, 22, 23	A_m	—	15	—	dB
Phase Margin ($R_L = 600\ \Omega$, $C_L = 0\text{ pF}$)	21, 22, 23	ϕ_m	—	60	—	Deg.
Channel Separation ($f = 100\text{ Hz}$ to 20 kHz)	24	CS	—	-120	—	dB
Power Bandwidth ($V_O = 20\text{ V}_{p-p}$, $R_L = 600\ \Omega$, $\text{THD} \leq 1.0\%$)		BWp	—	32	—	kHz
Distortion ($R_L = 600\ \Omega$, $V_O = 2.0\text{ V}_{p-p}$, $A_V = +1.0\text{ V}$) ($f = 1.0\text{ kHz}$) ($f = 10\text{ kHz}$) ($f = 20\text{ kHz}$)	25	THD	—	0.0024 0.014 0.024	—	%
Open Loop Output Impedance ($V_O = 0\text{ V}$, $f = 3.0\text{ MHz}$, $A_V = 10\text{ V}$)	26	$ Z_O $	—	150	—	Ω
Differential Input Resistance ($V_{CM} = 0\text{ V}$)		R_{IN}	—	200	—	$\text{k}\Omega$
Differential Input Capacitance ($V_{CM} = 0\text{ V}$)		C_{IN}	—	10	—	pF
Equivalent Input Noise Voltage ($R_S = 100\ \Omega$) $f = 10\text{ Hz}$ $f = 1.0\text{ kHz}$	27	e_n	—	8.0 7.5	—	$\text{nV}/\sqrt{\text{Hz}}$
Equivalent Input Noise Current $f = 10\text{ Hz}$ $f = 1.0\text{ kHz}$	28	i_n	—	0.33 0.15	—	$\text{pA}/\sqrt{\text{Hz}}$

**FIGURE 1 — MAXIMUM POWER DISSIPATION
versus TEMPERATURE**



**FIGURE 2 — INPUT OFFSET VOLTAGE versus
TEMPERATURE FOR 3 TYPICAL UNITS**

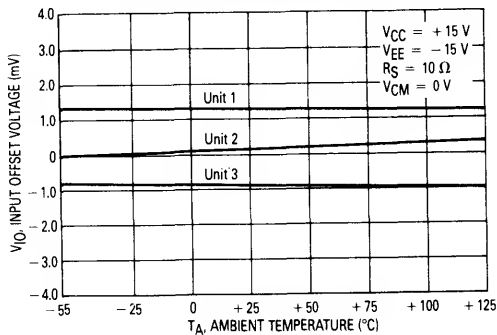


FIGURE 3 — INPUT BIAS CURRENT
versus COMMON MODE VOLTAGE

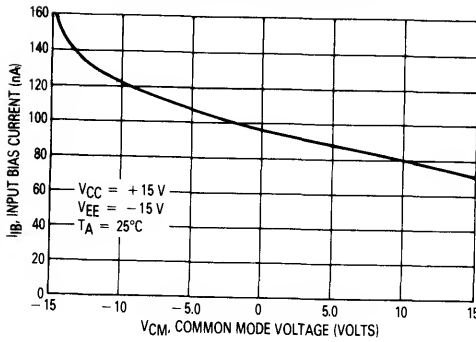


FIGURE 4 — INPUT BIAS CURRENT
versus TEMPERATURE

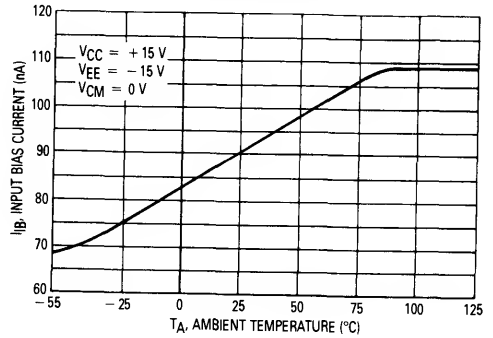


FIGURE 5 — INPUT COMMON MODE VOLTAGE
RANGE versus TEMPERATURE

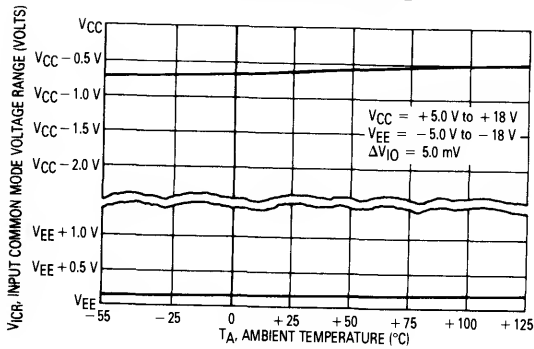


FIGURE 6 — OPEN LOOP VOLTAGE GAIN
versus TEMPERATURE

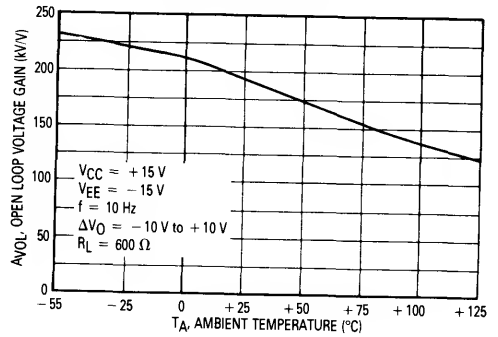


FIGURE 7 — VOLTAGE GAIN AND PHASE
versus FREQUENCY

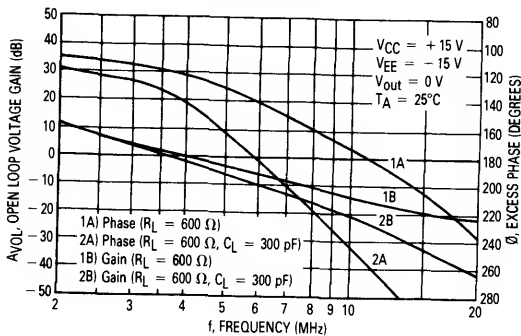


FIGURE 8 — OUTPUT VOLTAGE SWING
versus SUPPLY VOLTAGE

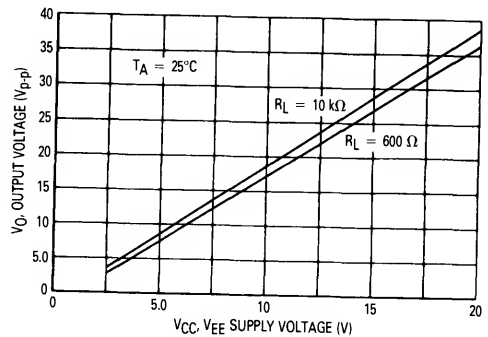


FIGURE 9 — OUTPUT SATURATION VOLTAGE
versus LOAD CURRENT

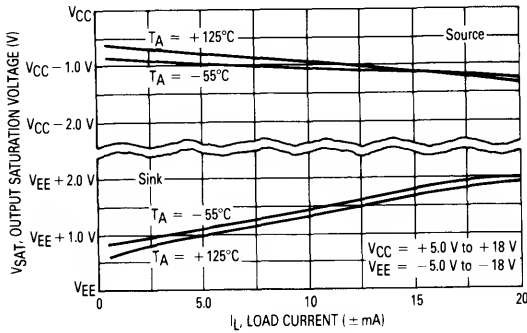


FIGURE 10 — OUTPUT VOLTAGE
versus FREQUENCY

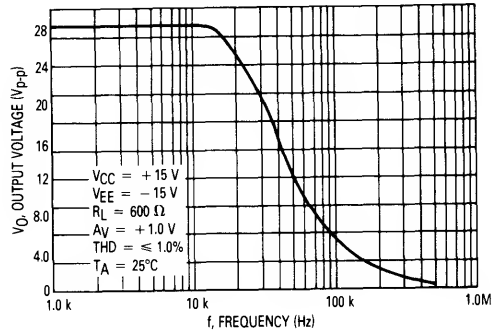


FIGURE 11 — COMMON MODE REJECTION
versus FREQUENCY OVER TEMPERATURE

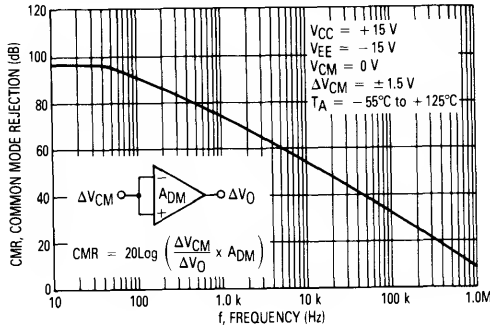


FIGURE 12 — POWER SUPPLY REJECTION
versus FREQUENCY OVER TEMPERATURE

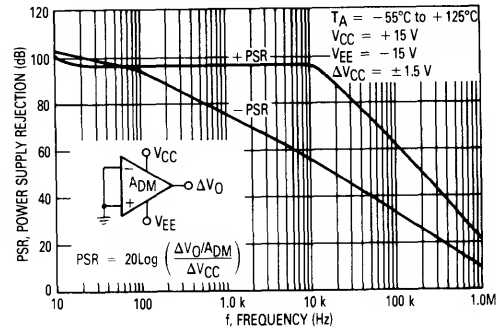


FIGURE 13 — OUTPUT SHORT CIRCUIT CURRENT
versus OUTPUT VOLTAGE

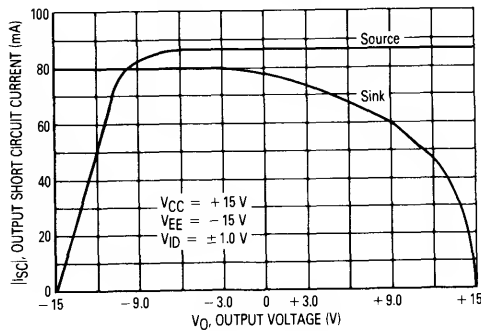


FIGURE 14 — OUTPUT SHORT CIRCUIT CURRENT
versus TEMPERATURE

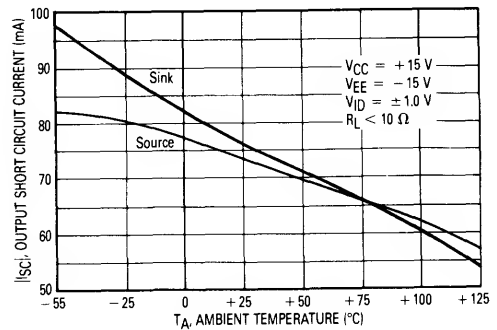


FIGURE 15 — SUPPLY CURRENT versus SUPPLY VOLTAGE WITH NO LOAD

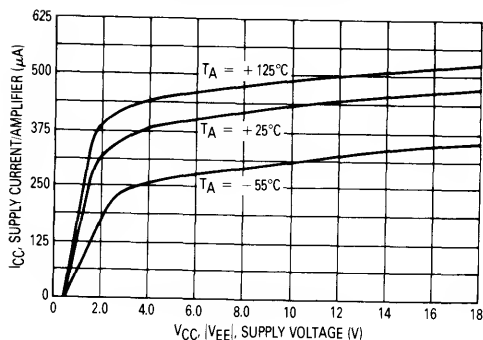


FIGURE 16 — NORMALIZED SLEW RATE versus TEMPERATURE

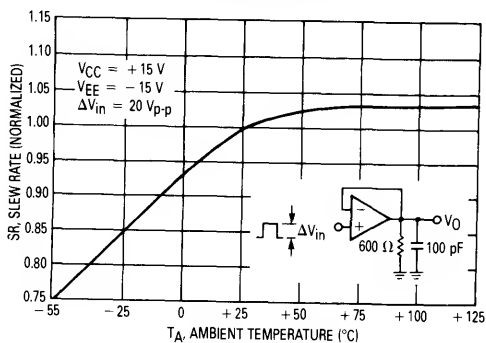


FIGURE 17 — GAIN BANDWIDTH PRODUCT versus TEMPERATURE

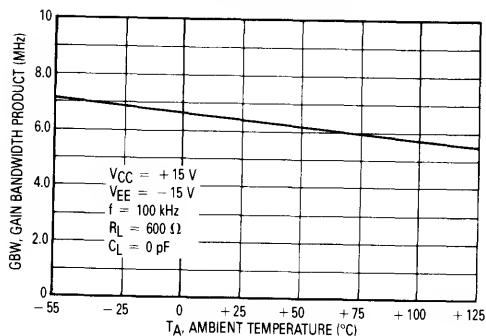


FIGURE 18 — VOLTAGE GAIN AND PHASE versus FREQUENCY

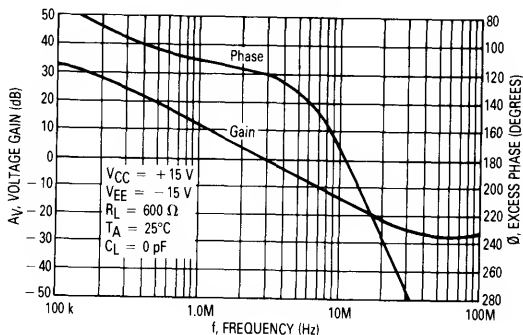


FIGURE 19 — VOLTAGE GAIN AND PHASE versus FREQUENCY

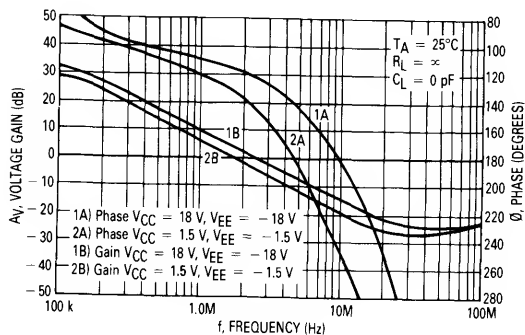


FIGURE 20 — OPEN LOOP GAIN MARGIN versus TEMPERATURE

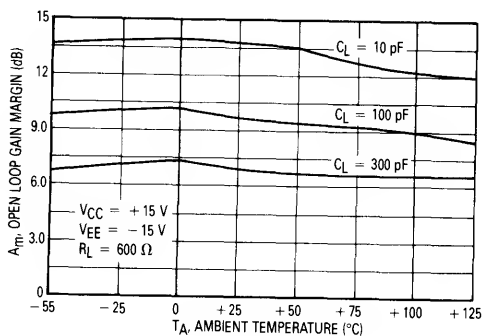


FIGURE 21 — PHASE MARGIN
versus TEMPERATURE

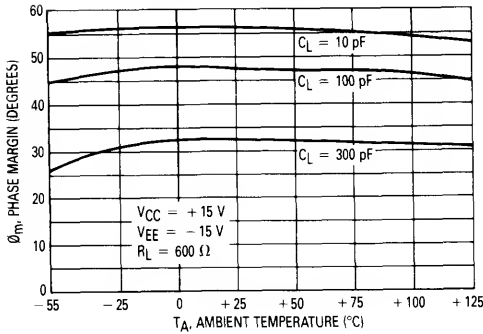


FIGURE 22 — PHASE MARGIN AND GAIN MARGIN
versus DIFFERENTIAL SOURCE RESISTANCE

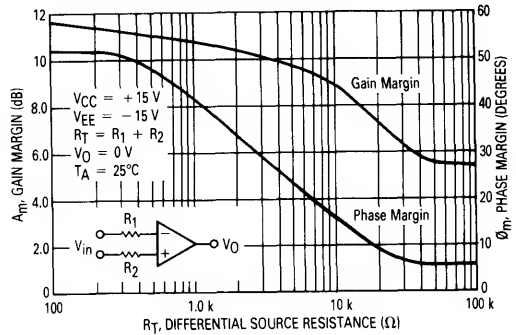


FIGURE 23 — OPEN LOOP GAIN MARGIN AND PHASE
MARGIN versus OUTPUT LOAD CAPACITANCE

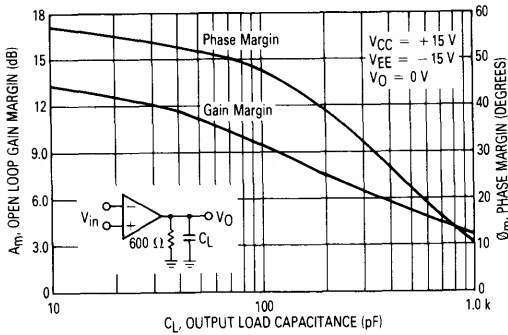


FIGURE 24 — CHANNEL SEPARATION
versus FREQUENCY

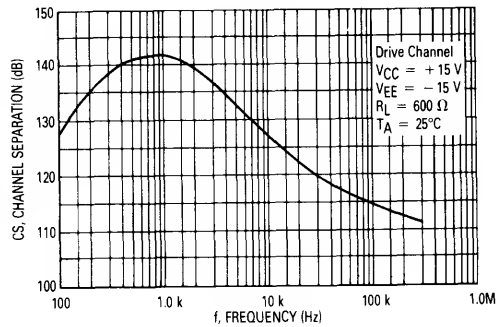


FIGURE 25 — TOTAL HARMONIC DISTORTION
versus FREQUENCY

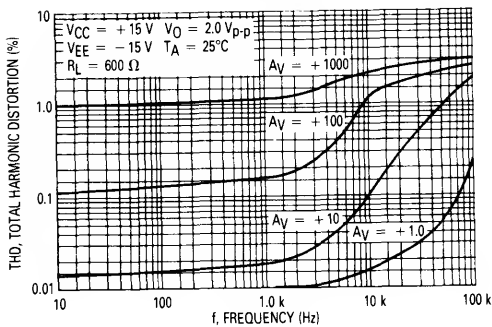
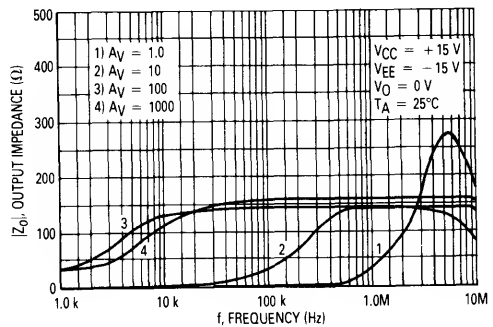
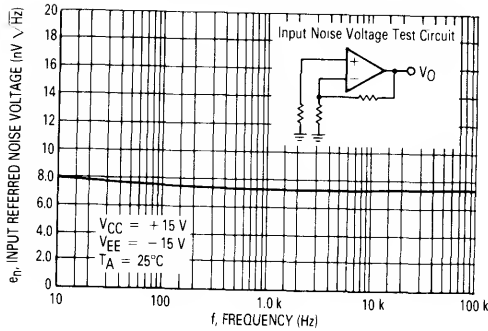


FIGURE 26 — OUTPUT IMPEDANCE
versus FREQUENCY

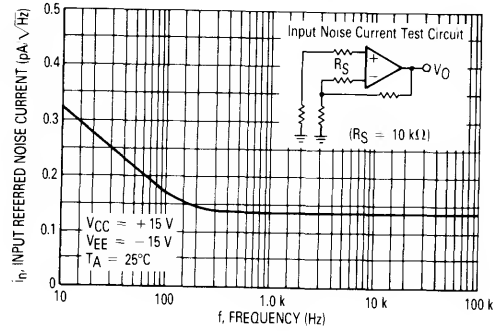


MC33178, MC33179

**FIGURE 27 — INPUT REFERRED NOISE VOLTAGE
versus FREQUENCY**



**FIGURE 28 — INPUT REFERRED NOISE CURRENT
versus FREQUENCY**



**FIGURE 29 — PERCENT OVERSHOOT versus
LOAD CAPACITANCE**

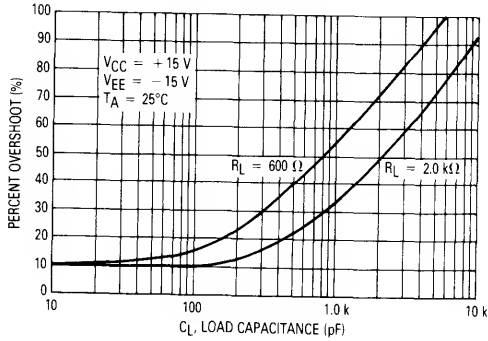


FIGURE 30 — NONINVERTING AMPLIFIER SLEW RATE

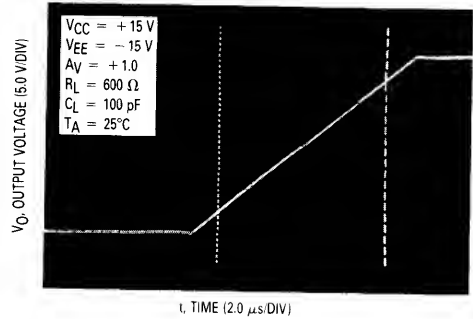


FIGURE 31 — SMALL SIGNAL TRANSIENT RESPONSE

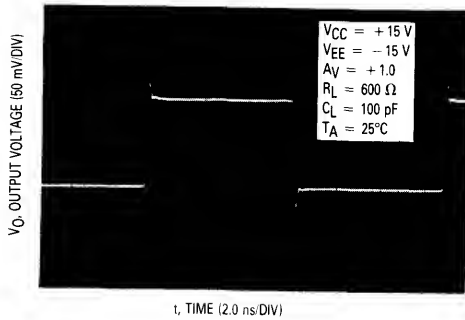


FIGURE 32 — LARGE SIGNAL TRANSIENT RESPONSE

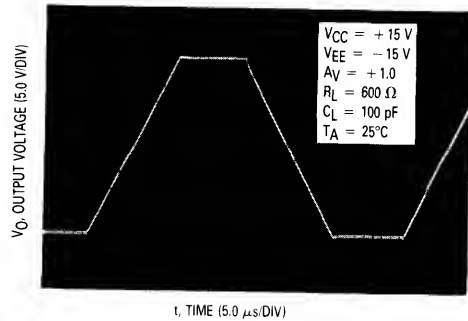
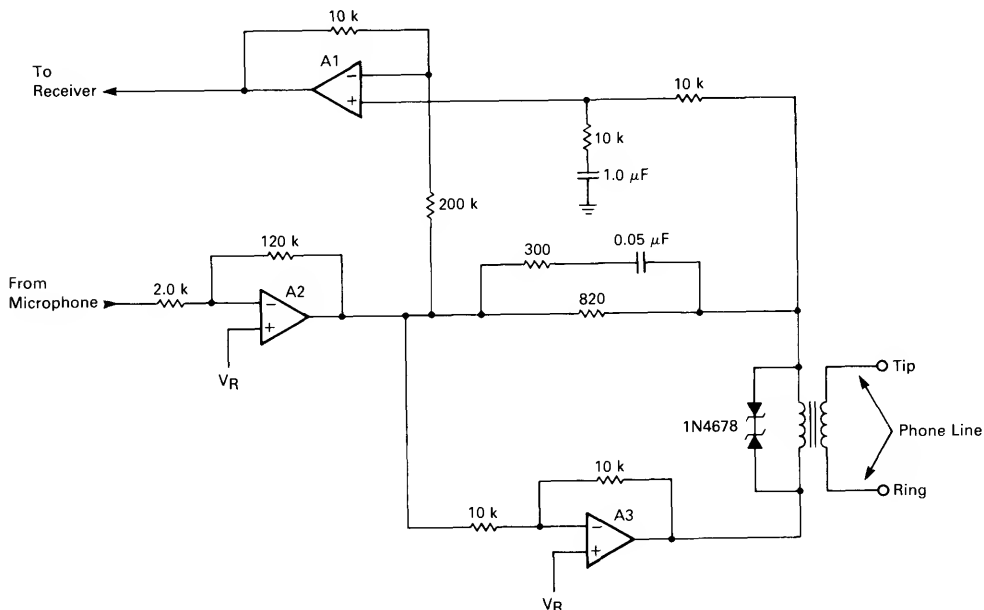


FIGURE 33 — TELEPHONE LINE
INTERFACE CIRCUIT

APPLICATION INFORMATION

This unique device uses a boosted output stage to combine a high output current with a drain current lower than similar bipolar input op amps. Its 60° phase margin and 15 dB gain margin ensure stability with up to 1000 pF of load capacitance (see Figure 23). The ability to drive a minimum 600 Ω load makes it particularly suitable for telecom applications. Note that in the sample circuit in Figure 33 both A2 and A3 are driving equivalent loads of approximately 600 Ω .

The low input offset voltage and moderately high slew rate and gain bandwidth product make it attractive for a variety of other applications. For example, although it is not single supply (the common mode input range does not include ground), it is specified at +5.0 V with a typical common mode rejection of 110 dB. This makes it an excellent choice for use with digital circuits. The high common mode rejection, which is stable over temperature, coupled with a low noise figure and low distortion is an ideal op amp for audio circuits.

The output stage of the op amp is current limited and therefore has a certain amount of protection in the event of a short circuit. However, because of its high current output, it is especially important not to allow the device to exceed the maximum junction temperature, particularly with the MC33179 (quad op amp). Shorting more

than one amplifier could easily exceed the junction temperature to the extent of causing permanent damage.

STABILITY

As usual with most high frequency amplifiers, proper lead dress, component placement, and PC board layout should be exercised for optimum frequency performance. For example, long unshielded input or output leads may result in unwanted input/output coupling. In order to preserve the relatively low input capacitance associated with these amplifiers, resistors connected to the inputs should be immediately adjacent to the input pin to minimize additional stray input capacitance. This not only minimizes the input pole frequency for optimum frequency response, but also minimizes extraneous "pick up" at this node. Supplying decoupling with adequate capacitance immediately adjacent to the supply pin is also important, particularly over temperature, since many types of decoupling capacitors exhibit great impedance changes over temperature.

Additional stability problems can be caused by high load capacitances and/or a high source resistance. Simple compensation schemes can be used to alleviate these effects.

If a high source resistance is used ($R1 > 1.0 \text{ k}\Omega$), a compensation capacitor equal to or greater than the input capacitance of the op amp (10 pF) placed across the feedback resistor (see Figure 34) can be used to neutralize that pole and prevent outer loop oscillation. Since the closed loop transient response will be a function of that capacitance it is important to choose the optimum value for that capacitor. This can be determined by the following formula:

$$(1) \quad C_C = (1 + [R1/R2])^2 \cdot C_L (Z_O/R2)$$

where: Z_O is the output impedance of the op amp.

For moderately high capacitive loads ($500 \text{ pF} < C_L < 1500 \text{ pF}$) the addition of a compensation resistor on the order of 20Ω between the output and the feedback loop will help to decrease miller loop oscillation (see Figure 35). For high capacitive loads ($C_L > 1500 \text{ pF}$) a combined compensation scheme should be used (see Figure 36). Both the compensation resistor and the compensation capacitor affect the transient response and can be calculated for optimum performance. The value of C_C can be calculated using formula (1). The formula to calculate R_C is as follows:

$$(2) \quad R_C = Z_O \cdot R1/R2$$

FIGURE 34 — COMPENSATION FOR HIGH SOURCE IMPEDANCE

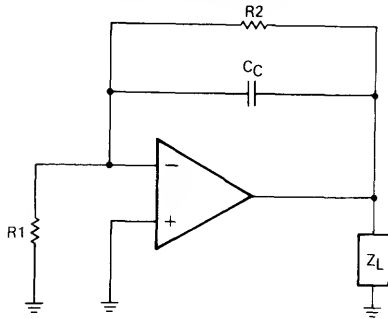


FIGURE 35 — COMPENSATION CIRCUIT FOR MODERATE CAPACITIVE LOADS

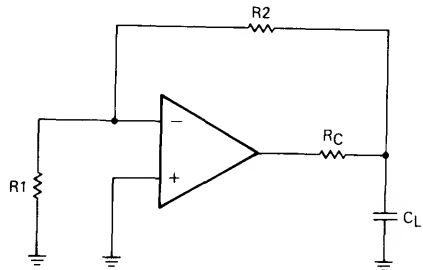
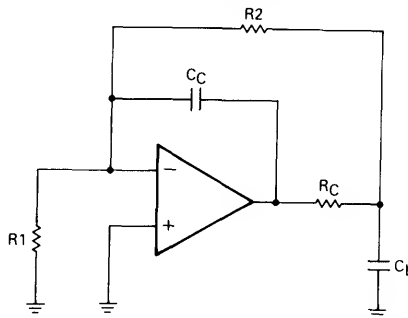


FIGURE 36 — COMPENSATION CIRCUIT FOR HIGH CAPACITIVE LOADS



**SINGLE SUPPLY, HIGH SLEW RATE
 LOW INPUT OFFSET VOLTAGE,
 BIPOLAR OPERATIONAL AMPLIFIERS**

The MC33272/4 series of monolithic operational amplifiers are quality fabricated with innovative Bipolar design concepts. This dual and quad operational amplifier series incorporates Bipolar inputs along with a patented Zip-R-Trim element for input offset voltage reduction. The MC33272/4 series of operational amplifiers exhibits a low input offset voltage and high gain bandwidth product. Dual-doublet frequency compensation is used to increase the slew rate while maintaining low input noise characteristics. Its all NPN output stage exhibits no deadband crossover distortion, large output voltage swing, and an excellent phase and gain margin. It also provides a low open-loop high frequency output impedance with symmetrical source and sink AC frequency performance.

The MC33272/4 series is specified over -40°C to $+85^{\circ}\text{C}$ and is available in the plastic DIP and SOIC surface mount packages (P and D suffixes).

- Input Offset Voltage Trimmed to $100\ \mu\text{V}$ (Typ)
- Low Input Bias Current: $300\ \text{nA}$
- Low Input Offset Current: $3.0\ \text{nA}$
- High Input Resistance: $16\ \text{M}\Omega$
- Low Noise: $18\ \text{nV}/\sqrt{\text{Hz}}$ @ $1.0\ \text{kHz}$
- High Gain Bandwidth Product: $24\ \text{MHz}$ @ $100\ \text{kHz}$
- High Slew Rate: $10\ \text{V}/\mu\text{s}$
- Power Bandwidth: $160\ \text{kHz}$
- Excellent Frequency Stability
- Unity Gain Stable: w/Capacitance Loads to $500\ \text{pF}$
- Large Output Voltage Swing: $+14.1\ \text{V}/-14.6\ \text{V}$
- Low Total Harmonic Distortion: 0.003%
- Power Supply Drain Current: $2.15\ \text{mA}$ per Amplifier
- Single or Split Supply Operation: $+3.0\ \text{V}$ to $+36\ \text{V}$ or $\pm 1.5\ \text{V}$ to $\pm 18\ \text{V}$

ORDERING INFORMATION

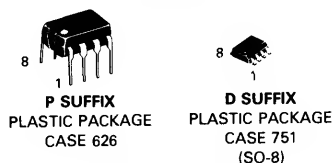
Op Amp Function	Device	Specified Ambient Temperature Range	Package
Dual	MC33272D	-40°C to $+85^{\circ}\text{C}$	SO-8
	MC33272P		Plastic DIP
	MC33274D		SO-14
Quad	MC33274P		Plastic DIP

MC33272
MC33274

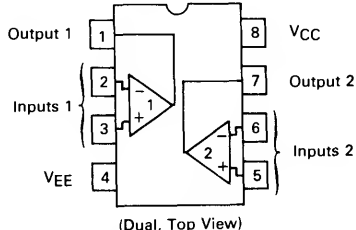
**HIGH PERFORMANCE
 OPERATIONAL
 AMPLIFIERS**

**SILICON MONOLITHIC
 INTEGRATED CIRCUIT**

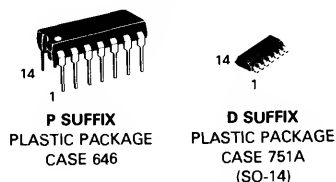
MC33272



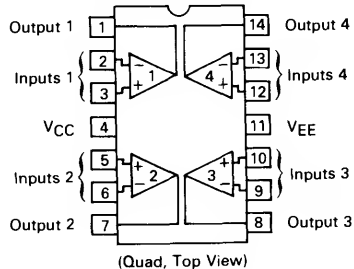
PIN ASSIGNMENTS



MC33274



PIN ASSIGNMENTS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC} to V_{EE}	+36	V
Input Differential Voltage Range	V_{IDR}	(Note 1)	V
Input Voltage Range	V_{IR}	(Note 1)	V
Output Short Circuit Duration (Note 2)	t_S	Indefinite	Seconds
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	-60 to +150	°C
Maximum Power Dissipation	P_D	(Note 2)	mW

NOTES:

1. Either or both input voltages should not exceed V_{CC} or V_{EE} .
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (see Figure 2).

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = +15$ V, $V_{EE} = -15$ V, $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S = 10\ \Omega$, $V_{CM} = 0$ V, $V_O = 0$ V) ($V_{CC} = +15$ V, $V_{EE} = -15$ V) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ ($V_{CC} = 5.0$ V, $V_{EE} = 0$) $T_A = +25^\circ\text{C}$	3	$ V_{IO} $	— — —	0.1 — —	1.0 1.8 2.0	mV
Average Temperature Coefficient of Input Offset Voltage $R_S = 10\ \Omega$, $V_{CM} = 0$ V, $V_O = 0$ V, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	3	$\Delta V_{IO}/\Delta T$	—	2.0	—	$\mu\text{V}/^\circ\text{C}$
Input Bias Current ($V_{CM} = 0$ V, $V_O = 0$ V) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	4, 5	I_{IB}	— —	300 —	650 800	nA
Input Offset Current ($V_{CM} = 0$ V, $V_O = 0$ V; $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		$ I_{IO} $	— —	3.0 —	65 80	nA
Common Mode Input Voltage Range ($\Delta V_{IO} = 5.0$ mV, $V_O = 0$ V) $T_A = +25^\circ\text{C}$	6	V_{ICR}	V_{EE} to $(V_{CC} - 1.8)$			V
Large Signal Voltage Gain ($V_O = 0$ to 10 V, $R_L = 2.0\ \text{k}\Omega$) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	7	A_{VOL}	90 86	100 —	— —	dB
Output Voltage Swing ($V_{ID} = \pm 1.0$ V) ($V_{CC} = +15$ V, $V_{EE} = -15$ V) $R_L = 2.0\ \text{k}\Omega$ $R_L = 2.0\ \text{k}\Omega$ $R_L = 10\ \text{k}\Omega$ $R_L = 10\ \text{k}\Omega$ ($V_{CC} = 5.0$ V, $V_{EE} = 0$ V) $R_L = 2.0\ \text{k}\Omega$ $R_L = 2.0\ \text{k}\Omega$	8, 9, 12 10, 11	V_{O+} V_{O-} V_{O+} V_{O-} V_{OH} V_{OL}	13.4 — 13.4 — — 3.7	13.9 -13.9 14 -14.7 — —	— -13.5 — -14.1 0.2 5.0	V
Common Mode Rejection ($V_{in} = +13.2$ V to -15 V)	13	CMR	90	100	—	dB
Power Supply Rejection $V_{CC}/V_{EE} = +15$ V/-15 V, +5.0 V/-15 V, +15 V/-5.0 V	14, 15	PSR	90	105	—	dB
Output Short Circuit Current ($V_{ID} = 1.0$ V, Output to Ground) Source Sink	16	I_{SC}	+25 -25	+37 -37	— —	mA
Power Supply Current Per Amplifier ($V_O = 0$ V) ($V_{CC} = +15$ V, $V_{EE} = -15$ V) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ ($V_{CC} = 5.0$ V, $V_{EE} = 0$ V) $T_A = +25^\circ\text{C}$	17	I_{CC}	— — —	2.15 — —	2.75 3.0 2.75	mA

MC33272, MC33274

2

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Slew Rate ($V_{in} = -10\text{ V to } +10\text{ V}$, $R_L = 2.0\text{ k}\Omega$, $C_L = 100\text{ pF}$, $A_V = +1.0$)	18, 33	SR	8.0	10	—	$\text{V}/\mu\text{s}$
Gain Bandwidth Product ($f = 100\text{ kHz}$)	19	GBW	17	24	—	MHz
AC Voltage Gain ($R_L = 2.0\text{ k}\Omega$, $V_O = 0\text{ V}$, $f = 20\text{ kHz}$)	20, 21, 22	A_{VO}	—	65	—	dB
Unity Gain Frequency (Open-Loop)		f_U	—	5.5	—	MHz
Gain Margin ($R_L = 2.0\text{ k}\Omega$, $C_L = 0\text{ pF}$)	23, 24, 26	A_m	—	12	—	dB
Phase Margin ($R_L = 2.0\text{ k}\Omega$, $C_L = 0\text{ pF}$)	23, 25, 26	ϕ_m	—	55	—	Deg
Channel Separation ($f = 20\text{ Hz to } 20\text{ kHz}$)	27	CS	—	~120	—	dB
Power Bandwidth ($V_O = 20\text{ V}_{p-p}$, $R_L = 2.0\text{ k}\Omega$, $\text{THD} \leq 1.0\%$)		BWP	—	160	—	kHz
Total Harmonic Distortion ($R_L = 2.0\text{ k}\Omega$, $f = 20\text{ Hz to } 20\text{ kHz}$, $V_O = 3.0\text{ V}_{rms}$, $A_V = +1.0$)	28	THD	—	0.003	—	%
Open-Loop Output Impedance ($V_O = 0\text{ V}$, $f = 6.0\text{ MHz}$)	29	$ Z_O $	—	35	—	Ω
Differential Input Resistance ($V_{CM} = 0\text{ V}$)		R_{IN}	—	16	—	$\text{M}\Omega$
Differential Input Capacitance ($V_{CM} = 0\text{ V}$)		C_{IN}	—	3.0	—	pF
Equivalent Input Noise Voltage ($R_S = 100\text{ }\Omega$, $f = 1.0\text{ kHz}$)	30	e_n	—	18	—	$\text{nV}/\sqrt{\text{Hz}}$
Equivalent Input Noise Current ($f = 1.0\text{ kHz}$)	31	i_n	—	0.5	—	$\text{pA}/\sqrt{\text{Hz}}$

**FIGURE 1 — EQUIVALENT CIRCUIT SCHEMATIC
(EACH AMPLIFIER)**

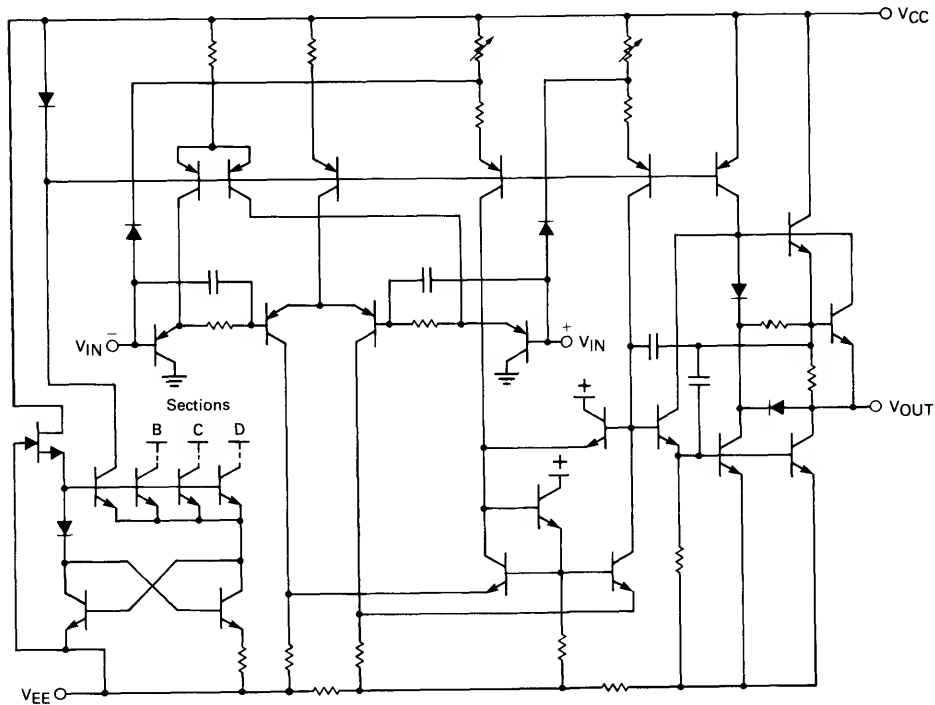


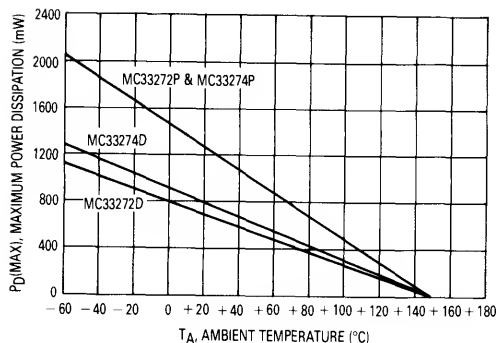
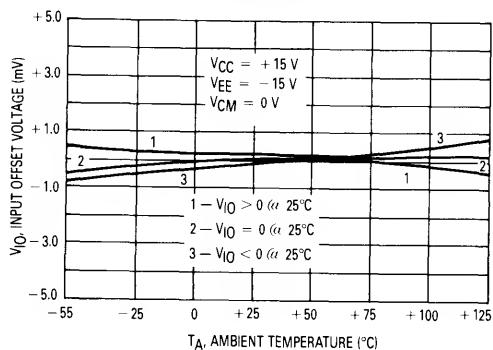
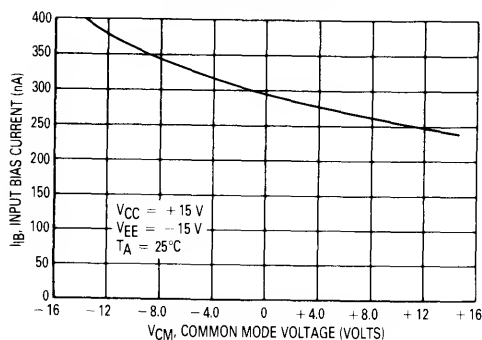
FIGURE 2 — MAXIMUM POWER DISSIPATION
versus TEMPERATUREFIGURE 3 — INPUT OFFSET VOLTAGE versus TEMPERATURE
FOR TYPICAL UNITSFIGURE 4 — INPUT BIAS CURRENT versus
COMMON MODE VOLTAGE

FIGURE 5 — INPUT BIAS CURRENT versus TEMPERATURE

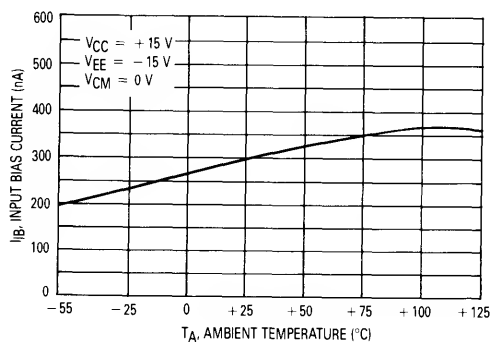
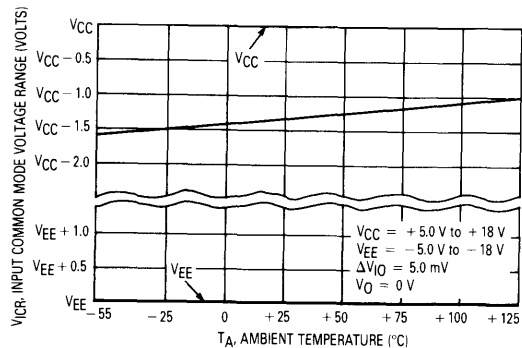
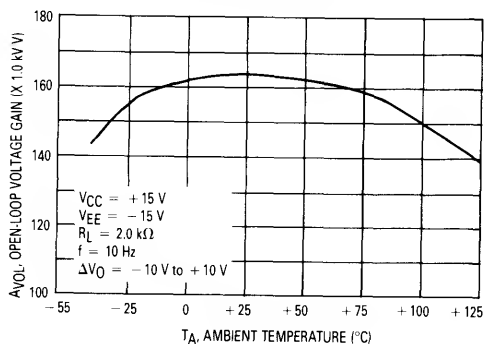
FIGURE 6 — INPUT COMMON MODE VOLTAGE RANGE
versus TEMPERATUREFIGURE 7 — OPEN-LOOP VOLTAGE GAIN
versus TEMPERATURE

FIGURE 8 — SPLIT SUPPLY OUTPUT VOLTAGE SWING
versus SUPPLY VOLTAGE

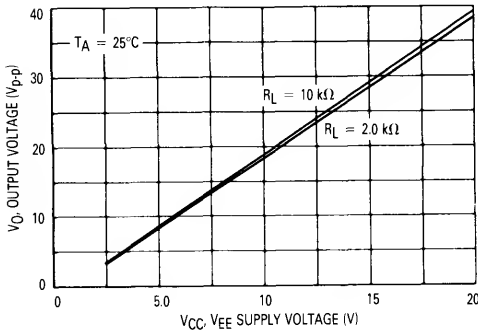


FIGURE 9 — SPLIT SUPPLY OUTPUT SATURATION VOLTAGE
versus LOAD CURRENT

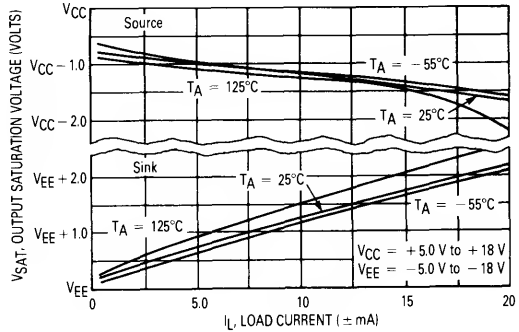


FIGURE 10 — SINGLE SUPPLY OUTPUT SATURATION
VOLTAGE versus LOAD RESISTANCE TO GROUND

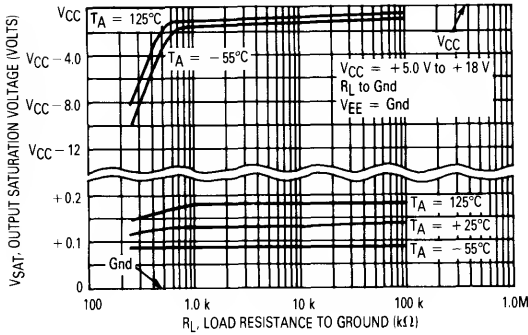


FIGURE 11 — SINGLE SUPPLY OUTPUT SATURATION
VOLTAGE versus LOAD RESISTANCE TO V_CC

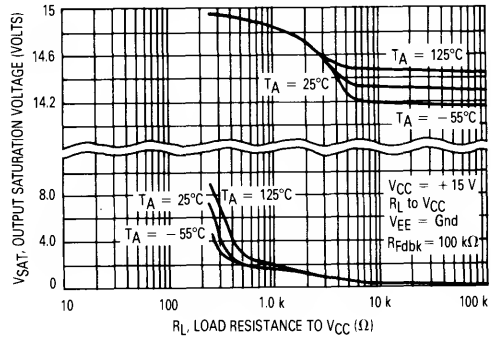


FIGURE 12 — OUTPUT VOLTAGE versus FREQUENCY

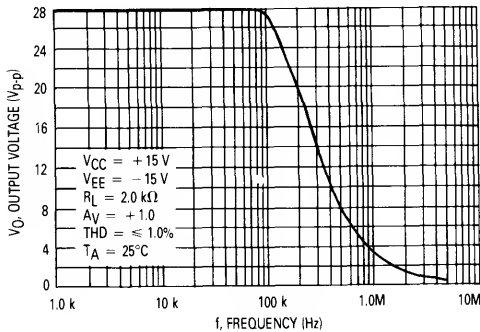


FIGURE 13 — COMMON MODE REJECTION
versus FREQUENCY

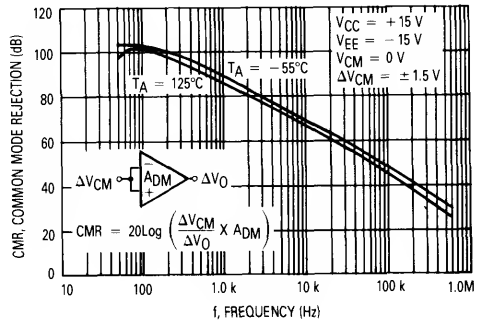


FIGURE 14 — POSITIVE POWER SUPPLY REJECTION
versus FREQUENCY

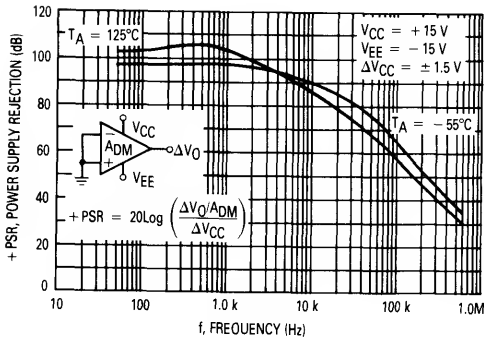


FIGURE 15 — NEGATIVE POWER SUPPLY REJECTION
versus FREQUENCY

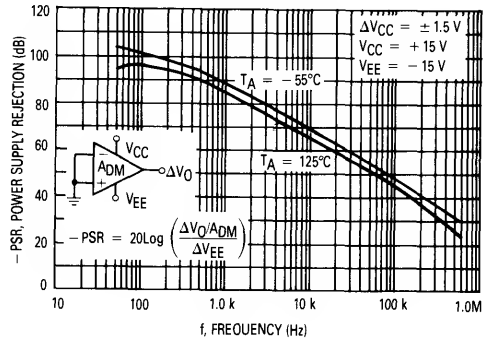


FIGURE 16 — OUTPUT SHORT CIRCUIT CURRENT
versus TEMPERATURE

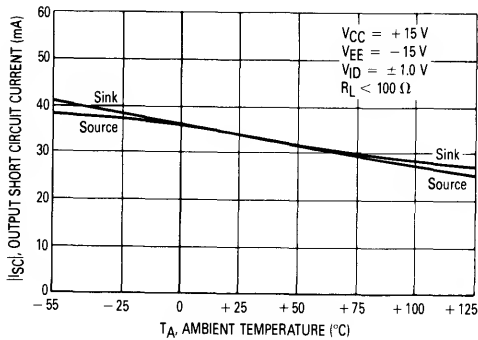


FIGURE 17 — SUPPLY CURRENT versus SUPPLY VOLTAGE

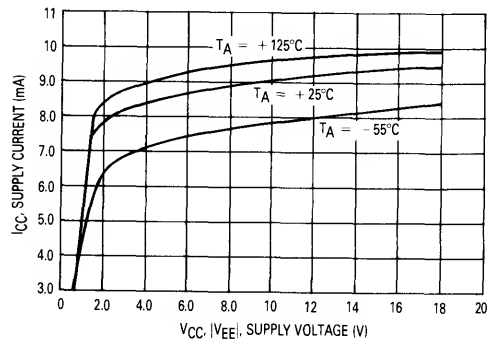


FIGURE 18 — NORMALIZED SLEW RATE
versus TEMPERATURE

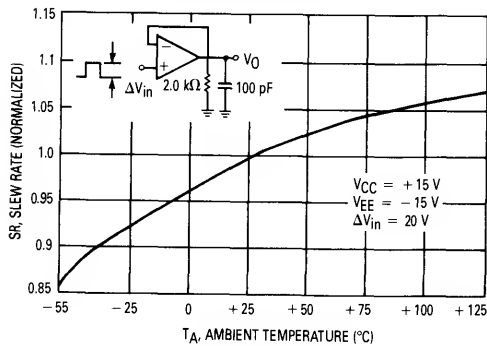
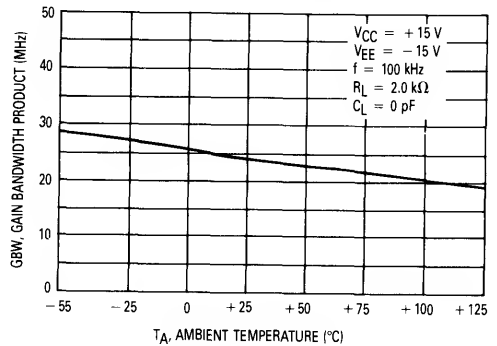


FIGURE 19 — GAIN BANDWIDTH PRODUCT
versus TEMPERATURE



MC33272, MC33274

FIGURE 20 — VOLTAGE GAIN & PHASE versus FREQUENCY

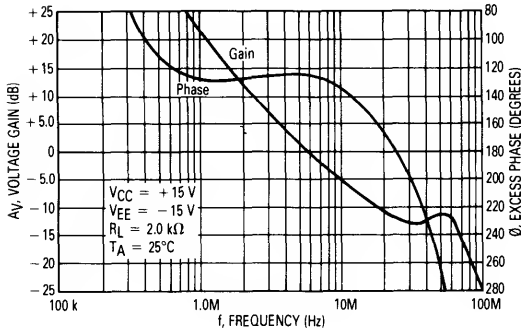


FIGURE 21 — GAIN AND PHASE versus FREQUENCY

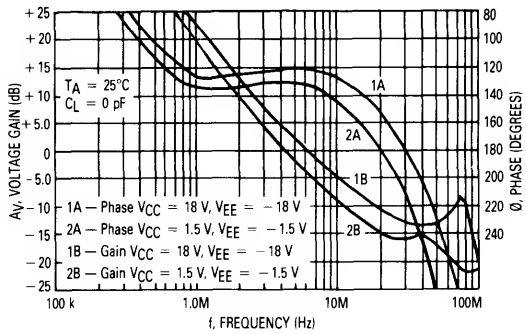


FIGURE 22 — OPEN-LOOP VOLTAGE GAIN & PHASE versus FREQUENCY

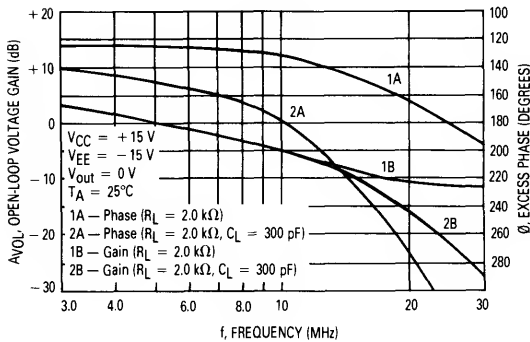


FIGURE 23 — OPEN-LOOP GAIN MARGIN AND PHASE MARGIN versus OUTPUT LOAD CAPACITANCE

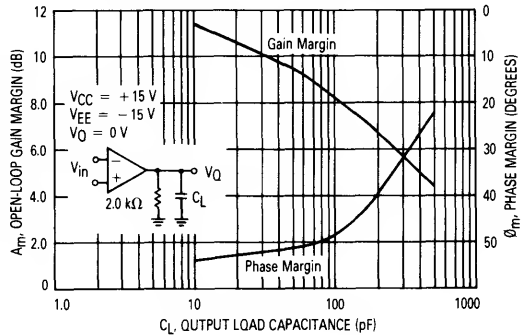


FIGURE 24 — OPEN-LOOP GAIN MARGIN versus TEMPERATURE

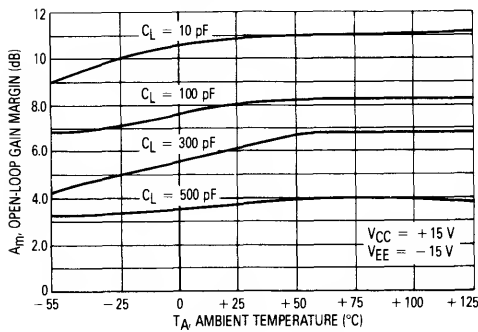


FIGURE 25 — PHASE MARGIN versus TEMPERATURE

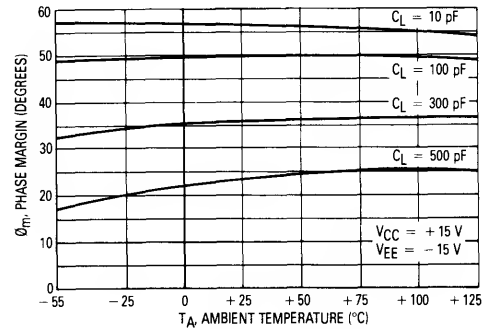


FIGURE 26 — PHASE MARGIN AND GAIN MARGIN versus DIFFERENTIAL SOURCE RESISTANCE

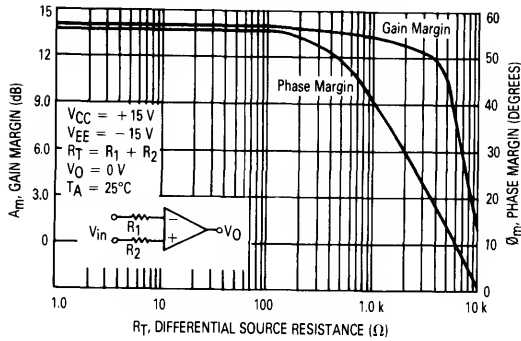


FIGURE 27 — CHANNEL SEPARATION versus FREQUENCY

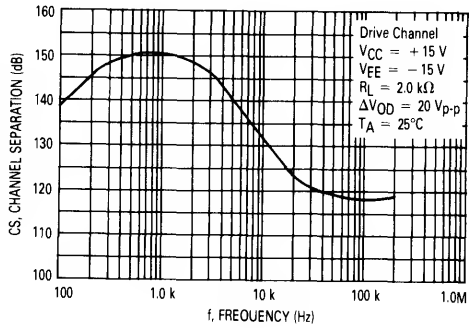


FIGURE 28 — TOTAL HARMONIC DISTORTION versus FREQUENCY

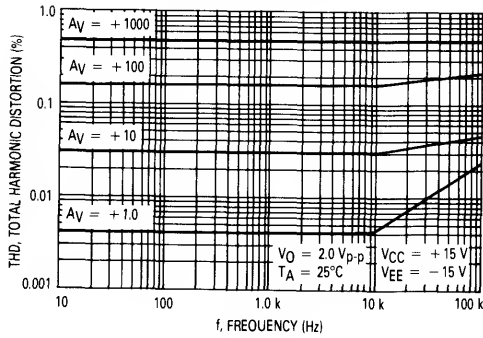


FIGURE 29 — OUTPUT IMPEDANCE versus FREQUENCY

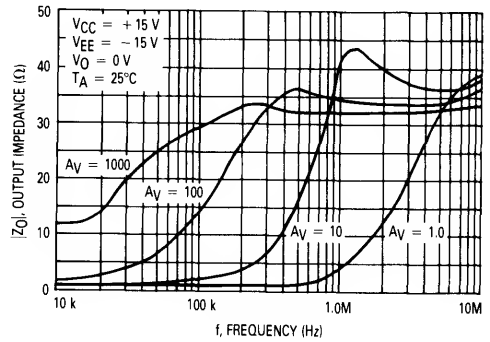


FIGURE 30 — INPUT REFERRED NOISE VOLTAGE versus FREQUENCY

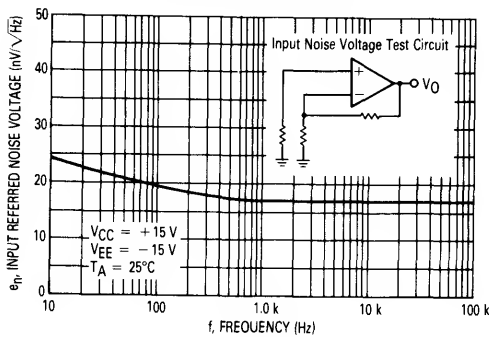


FIGURE 31 — INPUT REFERRED NOISE CURRENT versus FREQUENCY

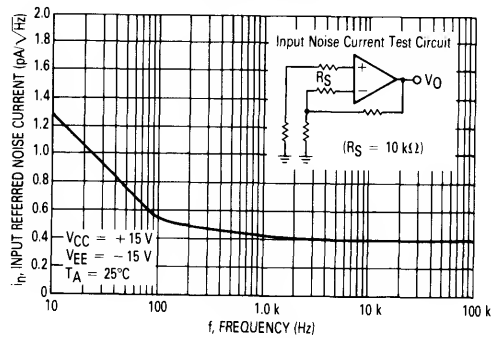


FIGURE 32 — PERCENT OVERSHOOT versus LOAD CAPACITANCE

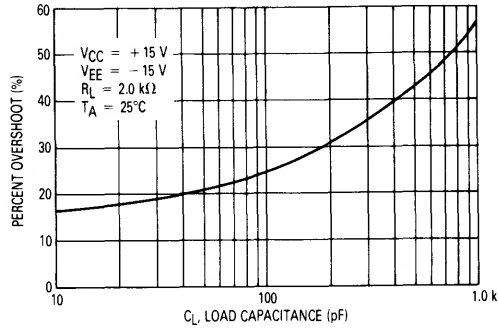


FIGURE 33 — NONINVERTING AMPLIFIER SLEW RATE FOR THE MC33274

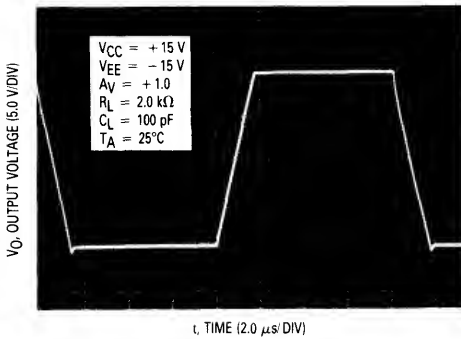


FIGURE 34 — NONINVERTING AMPLIFIER OVERSHOOT FOR THE MC33274

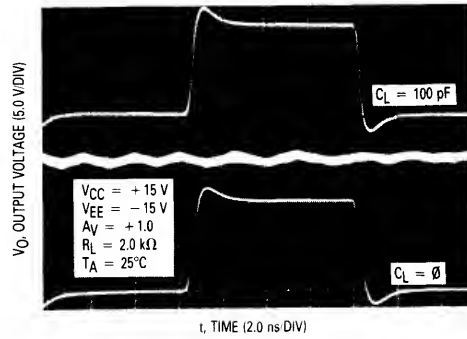


FIGURE 35 — SMALL SIGNAL TRANSIENT RESPONSE FOR MC33274

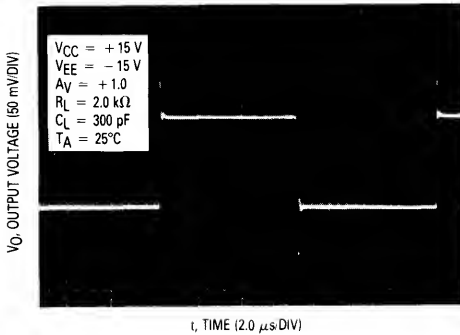
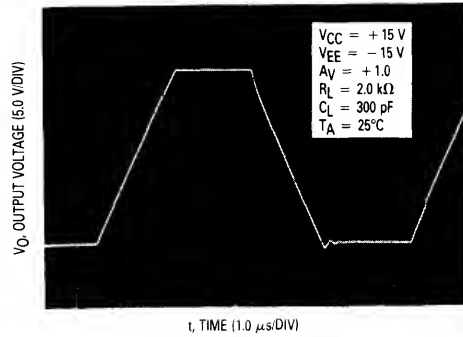


FIGURE 36 — LARGE SIGNAL TRANSIENT RESPONSE FOR MC33274



Product Preview

LOW INPUT OFFSET, HIGH SLEW RATE, WIDE BANDWIDTH, JFET INPUT OPERATIONAL AMPLIFIERS

The MC33282,4 series of monolithic operational amplifiers are quality fabricated with innovative Bipolar and JFET design concepts. This dual and quad operational amplifier series incorporates JFET inputs along with a patented Zip-R-Trim element for input offset voltage reduction. The MC33282,4 series of operational amplifiers exhibits low input offset voltage, low input bias current, high gain bandwidth and high slew rate. Dual-doublet frequency compensation is incorporated to produce high quality phase/gain performance. In addition, the MC33282,4 series exhibits moderately low input noise characteristics for JFET input amplifiers. It's all NPN output stage exhibits no deadband cross-over distortion, large output voltage swing, excellent phase and gain margin, low open-loop high frequency output impedance with symmetrical source and sink AC frequency performance.

The MC33282,4 series is specified over -40°C to $+85^{\circ}\text{C}$ and is available in the plastic DIP and SOIC surface mount packages (P and D suffixes).

- Low Input Offset Voltage: 200 μV
- Low Input Bias Current: 30 pA
- Low Input Offset Current: 6.0 pA
- High Input Resistance: $10^{12} \Omega$
- Low Noise: 18 nV/ $\sqrt{\text{Hz}}$ @ 1.0 kHz
- High Gain Bandwidth Product: 30 MHz @ 100 kHz
- High Slew Rate: 15 V/ μs
- Power Bandwidth: 175 kHz
- Excellent Frequency Stability
- Unity Gain Stable: w/Capacitance Loads to 300 pF
- Large Output Voltage Swing: $+14.1 \text{ V} - 14.6 \text{ V}$
- Low Total Harmonic Distortion: 0.003%
- Power Supply Drain Current: 2.15 mA per Amplifier
- Dual Supply Operation: $\pm 2.5 \text{ V}$ to $\pm 18 \text{ V}$ (Max)

ORDERING INFORMATION

Op Amp Function	Device	Specified Ambient Temperature Range	Package
Dual	MC33282D	-40°C to $+85^{\circ}\text{C}$	SO-8
	MC33282P		Plastic DIP
Quad	MC33284D		SO-14
	MC33284P		Plastic DIP

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MC33282 MC33284

JFET OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUIT

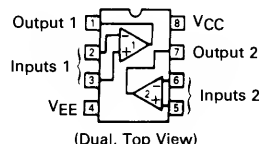
MC33282



P SUFFIX
PLASTIC PACKAGE
CASE 626



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SOP-8)



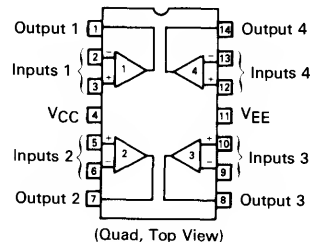
MC33284



P SUFFIX
PLASTIC PACKAGE
CASE 646



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)



MC33282, MC33284

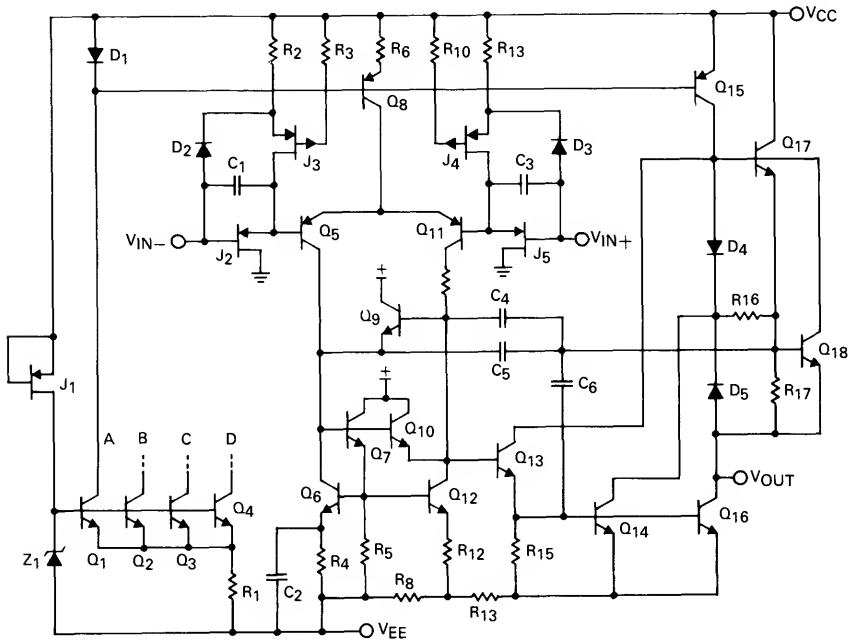
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+36	V
Input Differential Voltage Range	V_{IDR}	(Note 1)	V
Input Voltage Range	V_{IR}	(Note 1)	V
Output Short Circuit Duration (Note 2)	t_S	Indefinite	Seconds
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	-60 to +150	°C
Maximum Power Dissipation	P_D	(Note 2)	mW

NOTES:

1. Either or both input voltages should not exceed V_{CC} or V_{EE} .
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded.
3. V_{CC} and V_{EE} power supply rejection measured separately using 10 V power supply delta.

FIGURE 1 — EQUIVALENT CIRCUIT SCHEMATIC (EACH AMPLIFIER)



MC33282, MC33284

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S = 10\ \Omega$, $V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	$ V_{IO} $	—	0.2	2.0	mV
Average Temperature Coefficient of Input Offset Voltage $R_S = 10\ \Omega$, $V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$, $T_A = T_{low}$ to T_{high}	$\Delta V_{IO}/\Delta T$	—	5.0	—	$\mu\text{V}/^\circ\text{C}$
Input Bias Current ($V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	I_{IB}	-200 -2.0	30 —	200 2.0	pA nA
Input Offset Current ($V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	$ I_{IO} $	-100 -1.0	6.0 —	100 1.0	pA nA
Common Mode Input Voltage Range ($\Delta V_{IO} = 5.0\text{ mV}$, $V_O = 0\text{ V}$)	V_{ICR}	-11 —	-12 +14	— +11	V
Large Signal Voltage Gain ($V_O = \pm 10\text{ V}$, $R_L = 2.0\text{ k}\Omega$) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	A_{VOL}	50 25	200 —	— —	V/mV
Output Voltage Swing ($V_{ID} = \pm 1.0\text{ V}$) $R_L = 2.0\text{ k}\Omega$ $R_L = 2.0\text{ k}\Omega$ $R_L = 10\text{ k}\Omega$ $R_L = 10\text{ k}\Omega$	V_{O+} V_{O-} V_{O+} V_{O-}	13.2 — 13.7 —	13.7 -13.9 14.1 -14.6	— -13.2 — -14.3	V
Common Mode Rejection ($V_{in} = \pm 11\text{ V}$)	CMR	70	95	—	dB
Power Supply Rejection (Note 3) $V_{CC}/V_{EE} = +15\text{ V}/-15\text{ V}$ to $+5.0\text{ V}/-5.0\text{ V}$	PSR	75	105	—	dB
Output Short Circuit Current ($V_{ID} = 1.0\text{ V}$, Output to Ground) Source Sink	I_{SC}	15 —	21 -27	— -15	mA
Power Supply Current ($V_O = 0\text{ V}$, Per Amplifier) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	I_D	— —	2.15 —	2.75 3.0	mA

NOTE:

3. V_{CC} and V_{EE} power supply rejection measured separately using 10 V power supply delta.

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Slew Rate ($V_{in} = -10\text{ V}$ to $+10\text{ V}$, $R_L = 2.0\text{ k}\Omega$, $C_L = 100\text{ pF}$, $A_V = +1.0$)	SR	8.0	15	—	V/ μs
Gain Bandwidth Product ($f = 100\text{ kHz}$)	GBW	20	30	—	MHz
AC Voltage Gain ($R_L = 2.0\text{ k}\Omega$, $V_O = 0\text{ V}$, $f = 20\text{ kHz}$)	A_{VO}	—	1750	—	V/V
Unity Gain Frequency (Open-Loop)	f_U	—	5.5	—	MHz
Gain Margin ($R_L = 2.0\text{ k}\Omega$, $C_L = 0\text{ pF}$)	A_m	—	8.0	—	dB
Phase Margin ($R_L = 2.0\text{ k}\Omega$, $C_L = 0\text{ pF}$)	ϕ_m	—	50	—	Deg
Channel Separation ($f = 20\text{ Hz}$ to 20 kHz)	CS	—	-120	—	dB
Power Bandwidth ($V_O = 27\text{ V}_{p-p}$, $R_L = 2.0\text{ k}\Omega$, THD $\leq 1.0\%$)	BW _p	—	175	—	kHz
Total Harmonic Distortion ($R_L = 2.0\text{ k}\Omega$, $f = 20\text{ Hz}$ to 20 kHz , $V_O = 3.0\text{ V}_{rms}$, $A_V = +1.0$)	THD	—	0.003	—	%
Open-Loop Output Impedance ($V_O = 0\text{ V}$, $f = 9.0\text{ MHz}$)	$ Z_O $	—	37	—	Ω
Differential Input Resistance ($V_{CM} = 0\text{ V}$)	R_{IN}	—	10^{12}	—	k Ω
Differential Input Capacitance ($V_{CM} = 0\text{ V}$)	C_{IN}	—	5.0	—	pF
Equivalent Input Noise Voltage ($R_S = 100\ \Omega$, $f = 1.0\text{ kHz}$)	e_n	—	18	—	nV/ $\sqrt{\text{Hz}}$
Equivalent Input Noise Current ($f = 1.0\text{ kHz}$)	i_n	—	0.01	—	pA/ $\sqrt{\text{Hz}}$

JFET INPUT OPERATIONAL AMPLIFIERS

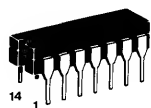
These low cost JFET Input operational amplifiers combine two state-of-the-art linear technologies on a single monolithic integrated circuit. Each internally compensated operational amplifier has well matched high voltage JFET input devices for low input offset voltage. The BIFET technology provides wide bandwidths and fast slew rates with low input bias currents, input offset currents, and supply currents.

The Motorola BIFET family offers single, dual and quad operational amplifiers which are pin-compatible with the industry standard MC1741, MC1458, and the MC3403/LM324 bipolar devices. The MC35001/35002/35004 series are specified over the military operating temperature range of -55°C to $+125^{\circ}\text{C}$ and the MC34001/34002/34004 series are specified from 0°C to $+70^{\circ}\text{C}$.

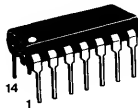
- Input Offset Voltage Options of 5.0 and 10 mV Maximum
- Low Input Bias Current — 40 pA
- Low Input Offset Current — 10 pA
- Wide Gain Bandwidth — 4.0 MHz
- High Slew Rate — 13 V/ μs
- Low Supply Current — 1.4 mA per Amplifier
- High Input Impedance — $10^{12} \Omega$
- High Common-Mode and Supply Voltage Rejection Ratios — 100 dB
- Industry Standard Pinouts

ORDERING INFORMATION

Op Amp Function	Device	Temperature Range	Package
Single	MC34001BD, D	0 to $+70^{\circ}\text{C}$	SO-8
	MC34001BG, G		Metal Can
	MC34001BP, P		Plastic DIP
	MC34001BU, U	-55 to $+125^{\circ}\text{C}$	Ceramic DIP
	MC35001BG, G		Metal Can
	MC35001BU, U		Ceramic DIP
Dual	MC34002BD, D	0 to $+70^{\circ}\text{C}$	SO-8
	MC34002BG, G		Metal Can
	MC34002BP, P		Plastic DIP
	MC34002BU, U	-55 to $+125^{\circ}\text{C}$	Ceramic DIP
	MC35002BG, G		Metal Can
	MC35002BU, U		Ceramic DIP
Quad	MC34004BL, L	0 to $+70^{\circ}\text{C}$	Ceramic DIP
	MC34004BP, P	-55 to $+125^{\circ}\text{C}$	Plastic DIP
	MC35004BL, L		Ceramic DIP



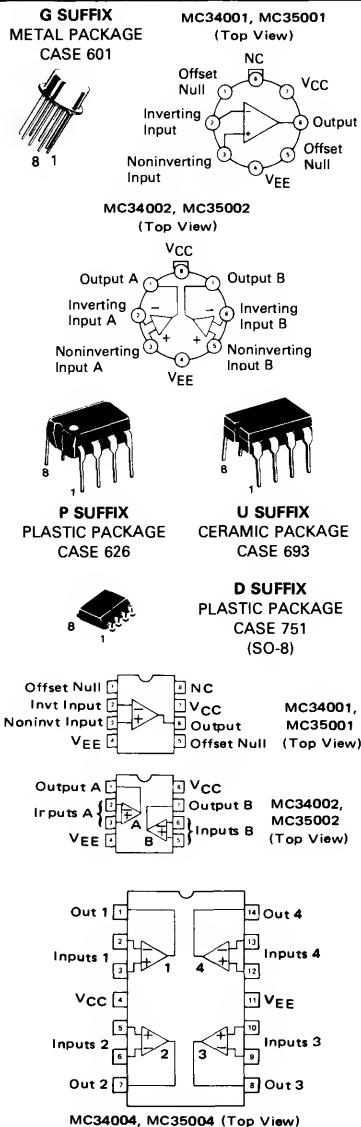
L SUFFIX
 CERAMIC PACKAGE
 CASE 632



P SUFFIX
 PLASTIC PACKAGE
 CASE 646

MC34001, MC35001 MC34002, MC35002 MC34004, MC35004

JFET INPUT OPERATIONAL AMPLIFIERS SILICON MONOLITHIC INTEGRATED CIRCUITS



MC34001, MC35001, MC34002, MC35002, MC34004, MC35004

MAXIMUM RATINGS

Rating	Symbol	MC35001 MC35002 MC35004	MC34001 MC34002 MC34004	Unit
Supply Voltage	V _{CC} V _{EE}	+22 -22	+18 -18	V
Differential Input Voltage (Note 1)	V _{ID}	±40	±30	V
Input Voltage Range	V _{IDR}	±20	±16	V
Output Short-Circuit Duration	t _S	Continuous		
Operating Ambient Temperature Range	T _A	-55 to +125	0 to +70	°C
Operating Junction Temperature Metal and Ceramic Packages Plastic Packages	T _J	150 —	150 150	°C
Storage Temperature Range Metal and Ceramic Packages Plastic Packages	T _{stg}	-65 to +150 —	-65 to +150 -55 to +125	°C

NOTE:

(1) Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = -15 V, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	MC35001/35002/35004			MC34001/34002/34004			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (R _S ≤ 10 k) MC3500XB, MC3400XB MC3500X, MC3400X	V _{IO}	— —	3.0 5.0	5.0 10	— —	3.0 5.0	5.0 10	mV
Average Temperature Coefficient of Input Offset Voltage R _S ≤ 10 k, T _A = T _{low} to T _{high} (Note 2)	ΔV _{IO} /ΔT	—	10	—	—	10	—	μV/°C
Input Offset Current (V _{CM} = 0) (Note 3) MC3500XB, MC3400XB MC3500X, MC3400X	I _{IO}	— —	10 25	50 100	— —	25 25	100 100	pA
Input Bias Current (V _{CM} = 0) (Note 3) MC3500XB, MC3400XB MC3500X, MC3400X	I _{IB}	— —	40 50	100 200	— —	50 50	200 200	pA
Input Resistance	r _i	—	10 ¹²	—	—	10 ¹²	—	Ω
Common Mode Input Voltage Range	V _{ICR}	±11 —	+15 -12	—	±11 —	+15 -12	—	V
Large Signal Voltage Gain (V _O = ±10 V, R _L = 2.0 k) MC3500XB, MC3400XB MC3500X, MC3400X	A _{VOL}	50 25	150 100	— —	50 25	150 100	— —	V/mV
Output Voltage Swing (R _L ≥ 10 k) (R _L ≥ 2.0 k)	V _O	±12 ±10	±14 ±13	— —	±12 ±10	±14 ±13	— —	V
Common Mode Rejection Ratio (R _S ≤ 10 k) MC3500XB, MC3400XB MC3500X, MC3400X	CMRR	80 —	100 —	— —	80 70	100 100	— —	dB
Supply Voltage Rejection Ratio (R _S ≤ 10 k) (Note 4) MC3500XB, MC3400XB MC3500X, MC3400X	PSRR	80 70	100 100	— —	80 70	100 100	— —	dB
Supply Current (Each Amplifier) MC3500XB, MC3400XB MC3500X, MC3400X	I _D	— —	1.4 1.4	2.5 2.7	— —	1.4 1.4	2.5 2.7	mA
Slew Rate (A _v = 1.0)	SR	—	13	—	—	13	—	V/μs
Gain-Bandwidth Product	GBW	—	4.0	—	—	4.0	—	MHz
Equivalent Input Noise Voltage (R _S = 100 Ω, f = 1000 Hz)	e _n	—	25	—	—	25	—	nV/√Hz
Equivalent Input Noise Current (f = 1000 Hz)	i _n	—	0.01	—	—	0.01	—	pA/√Hz

MC34001, MC35001, MC34002, MC35002, MC34004, MC35004

ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = T_{low}$ to T_{high} [Note 2]).

Characteristic	Symbol	MC35001/35002/35004			MC34001/34002/34004			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10\text{ k}$) MC3500XB, MC3400XB C3500X, MC3400X	V_{IO}	— —	— —	7.0 14	— —	— —	7.0 13	mV
Input Offset Current ($V_{CM} = 0$) (Note 3) MC3500XB, MC3400XB MC3500X, MC3400X	I_{IO}	— —	— —	40 40	— —	— —	4.0 4.0	nA
Input Bias Current ($V_{CM} = 0$) (Note 3) MC3500XB, MC3400XB MC3500X, MC3400X	I_{IB}	— —	— —	50 50	— —	— —	8.0 8.0	nA
Common Mode Input Voltage Range	V_{ICR}	± 11	—	—	± 11	—	—	V
Large Signal ($V_O = \pm 10\text{ V}$, $R_L = 2.0\text{ k}$) MC3500XB, MC3400XB MC3500X, MC3400X	$AVOL$	25 15	— —	— —	25 15	— —	— —	V/mV
Output Voltage Swing ($R_L \geq 10\text{ k}$) ($R_L \geq 2.0\text{ k}$)	V_O	± 12 ± 10	— —	— —	± 12 ± 10	— —	— —	V
Common Mode Rejection Ratio ($R_S \leq 10\text{ k}$) MC3500XB, MC3400XB MC3500X, MC3400X	CMRR	80 70	— —	— —	80 70	— —	— —	dB
Supply Voltage Rejection Ratio ($R_S \leq 10\text{ k}$) (Note 4) MC3500XB, MC3400XB MC3500X, MC3400X	PSRR	80 70	— —	— —	80 70	— —	— —	dB
Supply Current (Each Amplifier) MC3500XB, MC3400XB MC3500X, MC3400X	I_D	— —	— —	2.8 3.0	— —	— —	2.8 3.0	mA

NOTES:

(2) $T_{low} = -55^\circ\text{C}$ for MC35001/35001B
MC35002/35002B
MC35004/35004B
= 0°C for MC34001/34001B
MC34002/34002B
MC34004/34004B
 $T_{high} = +125^\circ\text{C}$ for MC35001/35001B
MC35002/35002B
MC35004/35004B
= $+70^\circ\text{C}$ for MC34001/34001B
MC34002/34002B
MC34004/34004B

(3) The input bias currents approximately double for every 10°C rise in junction temperature, T_J . Due to limited test time, the input bias currents are correlated to junction temperature. Use of a heatsink is recommended if input bias current is to be kept to a minimum.
(4) Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

2

TYPICAL PERFORMANCE CHARACTERISTICS

2

FIGURE 1 — INPUT BIAS CURRENT
versus TEMPERATURE

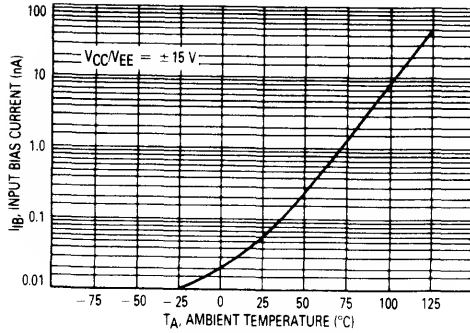


FIGURE 2 — OUTPUT VOLTAGE SWING
versus FREQUENCY

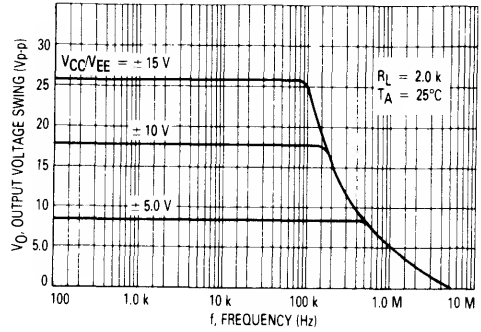


FIGURE 3 — OUTPUT VOLTAGE SWING
versus LOAD RESISTANCE

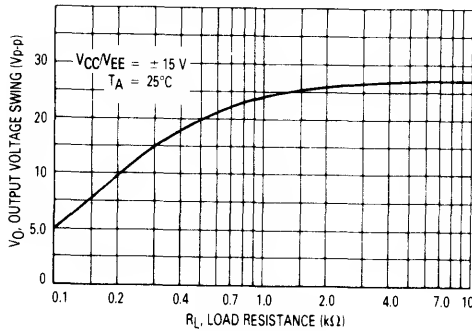


FIGURE 4 — OUTPUT VOLTAGE SWING
versus SUPPLY VOLTAGE

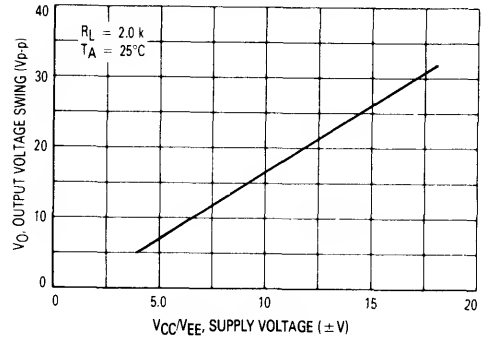


FIGURE 5 — OUTPUT VOLTAGE SWING
versus TEMPERATURE

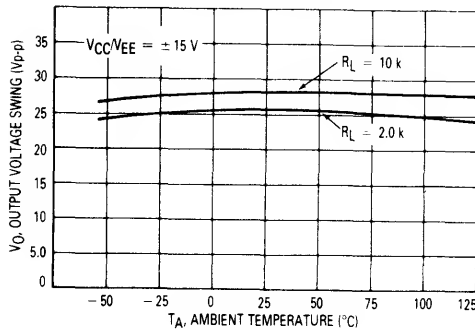


FIGURE 6 — SUPPLY CURRENT PER AMPLIFIER
versus TEMPERATURE

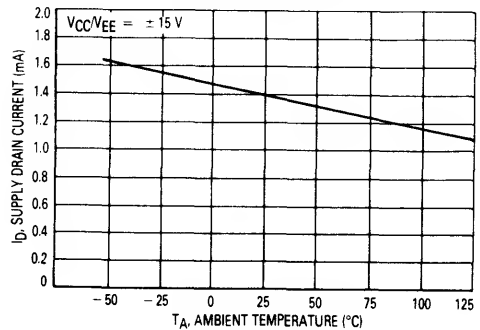


FIGURE 7 — LARGE-SIGNAL VOLTAGE GAIN AND PHASE SHIFT versus FREQUENCY

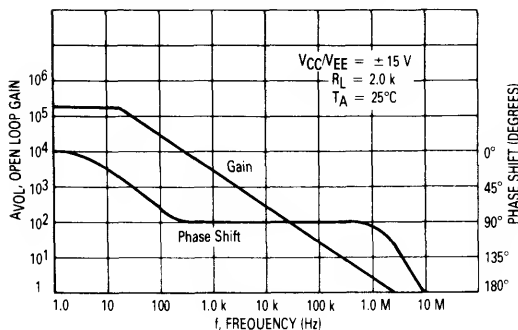


FIGURE 8 — LARGE-SIGNAL VOLTAGE GAIN versus TEMPERATURE

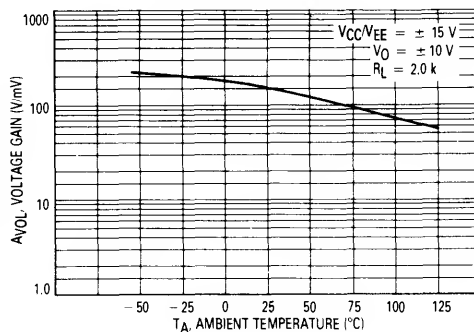


FIGURE 9 — NORMALIZED SLEW RATE versus TEMPERATURE

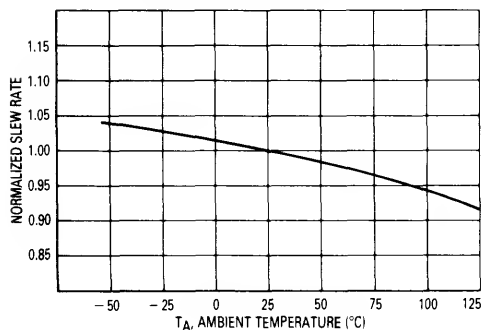


FIGURE 10 — EQUIVALENT INPUT NOISE VOLTAGE versus FREQUENCY

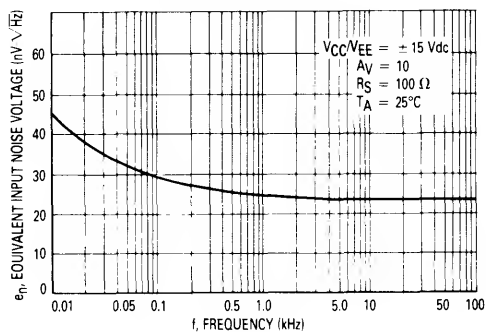
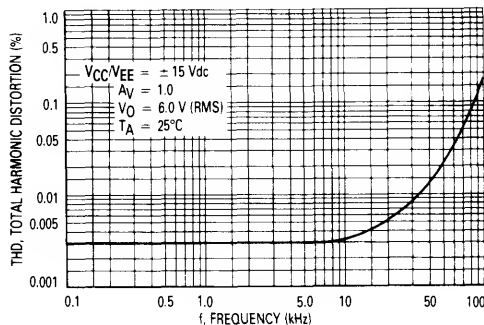
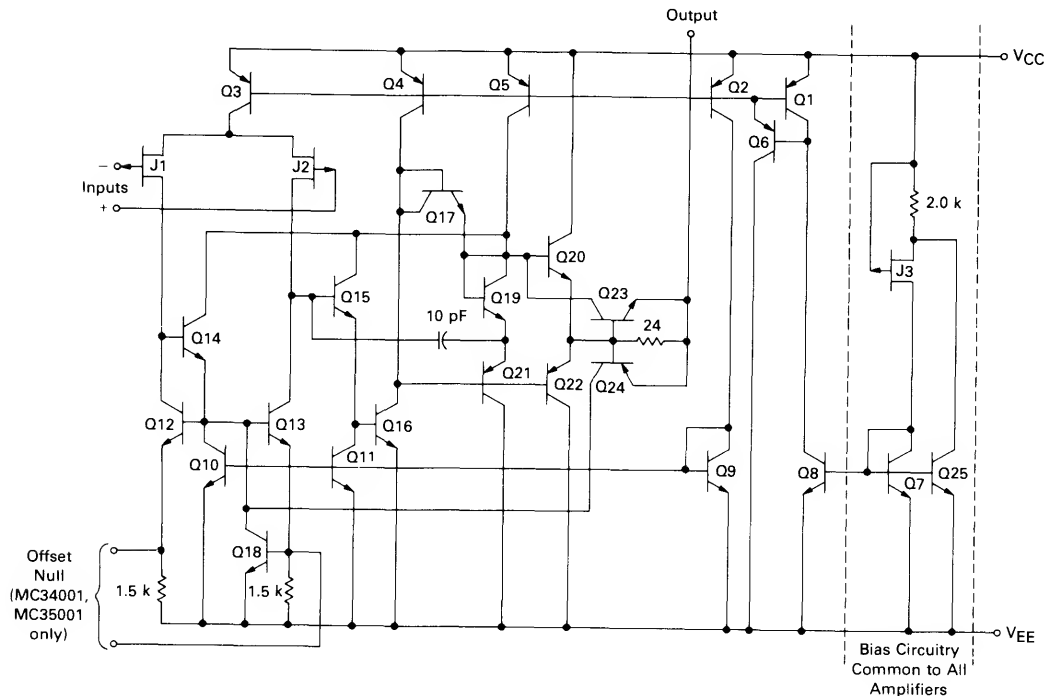


FIGURE 11 — TOTAL HARMONIC DISTORTION versus FREQUENCY

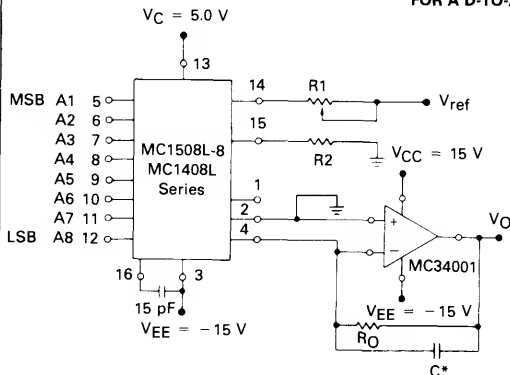


REPRESENTATIVE CIRCUIT SCHEMATIC
(Each Amplifier)



TYPICAL APPLICATIONS

FIGURE 12 — OUTPUT CURRENT TO VOLTAGE TRANSFORMATION
FOR A D-TO-A CONVERTER



Settling time to within 1/2 LSB (± 19.5 mV) is approximately 4.0 μ s from the time all bits are switched.

*The value of C may be selected to minimize overshoot and ringing (C \approx 68 pF).

Theoretical V_O

$$V_O = \frac{V_{ref}}{R_1 (R_O)} \left[\frac{A_1}{2} + \frac{A_2}{4} + \frac{A_3}{8} + \frac{A_4}{16} + \frac{A_5}{32} + \frac{A_6}{64} + \frac{A_7}{128} + \frac{A_8}{256} \right]$$

Adjust V_{ref} , R1 or R_O so that V_O with all digital inputs at high level is equal to 9.961 volts.

$$\begin{aligned} V_{ref} &= 2.0 \text{ Vdc} \\ R_1 &= R_2 \approx 1.0 \text{ k}\Omega \\ R_O &= 5.0 \text{ k}\Omega \end{aligned}$$

$$\begin{aligned} V_O &= \frac{2 \text{ V}}{1 \text{ k}} (5 \text{ k}) \left[\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256} \right] \\ &\approx 10 \text{ V} \left[\frac{255}{256} \right] = 9.961 \text{ V} \end{aligned}$$

FIGURE 13 — POSITIVE PEAK DETECTOR

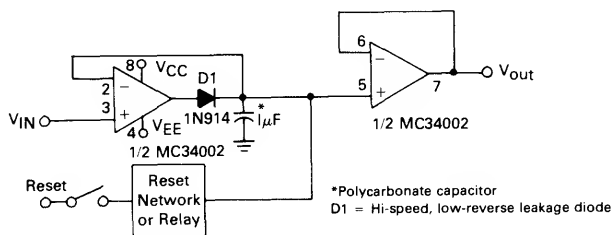
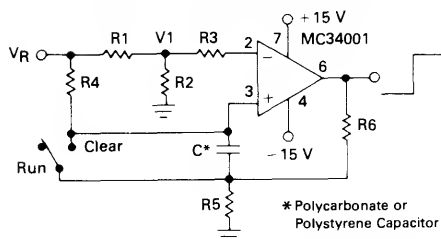


FIGURE 14 — LONG INTERVAL RC TIMER

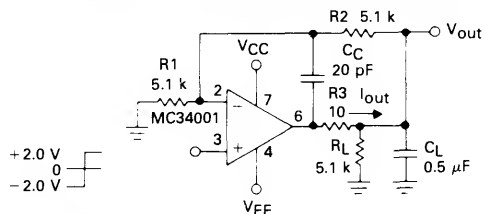


Time (t) = $R_4 C(n (V_R/V_R - V_i))$, $R_3 = R_4$, $R_5 = 0.1 R_6$
If $R_1 = R_2$: $t = 0.693 R_4 C$

Design Example: 100 Second Timer

$V_R = 10 \text{ V}$ $C = 1.0 \mu\text{F}$ $R_3 = R_4 = 144 \text{ M}$
 $R_6 = 20 \text{ k}$ $R_5 = 2.0 \text{ k}$ $R_1 = R_2 = 1.0 \text{ k}$

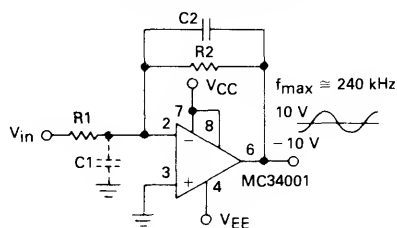
FIGURE 15 — ISOLATING LARGE CAPACITIVE LOADS



- Overshoot < 10%
- $t_s = 10 \mu\text{s}$
- When driving large C_L , the V_{out} slew rate is determined by C_L and $I_{out(max)}$:

$$\frac{\Delta V_{out}}{\Delta t} = \frac{I_{out}}{C_L} = \frac{0.02}{0.5} \text{ V}/\mu\text{s} = 0.04 \text{ V}/\mu\text{s} \text{ (with } C_L \text{ shown)}$$

FIGURE 16 — WIDE BW, LOW NOISE, LOW DRIFT AMPLIFIER



- Power BW: $f_{max} = \frac{S_r}{2\pi V_P} \approx 240 \text{ kHz}$
- Parasitic input capacitance ($C_1 \approx 3 \text{ pF}$ plus any additional layout capacitance) interacts with feedback elements and creates undesirable high-frequency pole. To compensate add C_2 such that: $R_2 C_2 \approx R_1 C_1$.

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

2

HIGH SLEW RATE, WIDE BANDWIDTH, SINGLE SUPPLY OPERATIONAL AMPLIFIERS

Quality bipolar fabrication with innovative design concepts are employed for the MC33071/2/4, MC34071/2/4, MC35071/2/4 series of monolithic operational amplifiers. This series of operational amplifiers offer 4.5 MHz of gain bandwidth product, 13 V/ μ s slew rate and fast settling time without the use of JFET device technology. Although this series can be operated from split supplies, it is particularly suited for single supply operation, since the common mode input voltage range includes ground potential (V_{EE}). With a Darlington input stage, this series exhibits high input resistance, low input offset voltage and high gain. The all NPN output stage, characterized by no deadband crossover distortion and large output voltage swing, provides high capacitance drive capability, excellent phase and gain margins, low open-loop high frequency output impedance and symmetrical source/sink ac frequency response.

The MC33071/2/4, MC34071/2/4, MC35071/2/4 series of devices are available in standard or prime performance (A Suffix) grades and are specified over the commercial, industrial/vehicular or military temperature ranges. The complete series of single, dual and quad operational amplifiers are available in the plastic, ceramic DIP and SOIC surface mount packages.

- Wide Bandwidth: 4.5 MHz
- High Slew Rate: 13 V/ μ s
- Fast Settling Time: 1.1 μ s to 0.1%
- Wide Single Supply Operation: 3.0 V to 44 V
- Wide Input Common Mode Voltage Range: Includes Ground (V_{EE})
- Low Input Offset Voltage: 3.0 mV Maximum (A Suffix)
- Large Output Voltage Swing: -14.7 V to +14 V (with ± 15 V Supplies)
- Large Capacitance Drive Capability: 0 to 10,000 pF
- Low Total Harmonic Distortion: 0.02%
- Excellent Phase Margin: 60°
- Excellent Gain Margin: 12 dB
- Output Short Circuit Protection

ORDERING INFORMATION

Op Amp Function	Device	Temperature Range	Package
Single	MC34071P, AP MC34071D, AD MC34071U, AU	0°C to +70°C	Plastic DIP SO-8 Ceramic DIP
	MC33071P, AP MC33071D, AD MC33071U, AU	-40°C to +85°C	Plastic DIP SO-8 Ceramic DIP
	MC35071U, AU	-55°C to +125°C	Ceramic DIP
Dual	MC34072P, AP MC34072D, AD MC34072U, AU	0°C to +70°C	Plastic DIP SO-8 Ceramic DIP
	MC33072P, AP MC33072D, AD MC33072U, AU	-40°C to +85°C	Plastic DIP SO-8 Ceramic DIP
	MC35072U, AU	-55°C to +125°C	Ceramic DIP
Quad	MC34074P, AP MC34074D, AD MC34074L, AL	0°C to +70°C	Plastic DIP SO-14 Ceramic DIP
	MC33074P, AP MC33074D, AD MC33074L, AL	-40°C to +85°C	Plastic DIP SO-14 Ceramic DIP
	MC35074L, AL	-55°C to +125°C	Ceramic DIP


MC34071,2,4 MC35071,2,4 MC33071,2,4

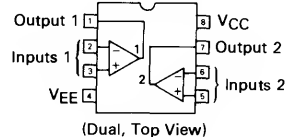
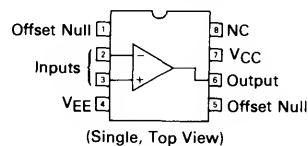
HIGH PERFORMANCE SINGLE SUPPLY OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC
INTEGRATED CIRCUIT


P SUFFIX
PLASTIC PACKAGE
CASE 626



U SUFFIX
CERAMIC PACKAGE
CASE 693

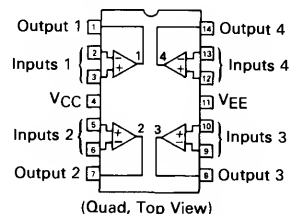

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)




P SUFFIX
PLASTIC PACKAGE
CASE 646


L SUFFIX
CERAMIC PACKAGE
CASE 632


D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)



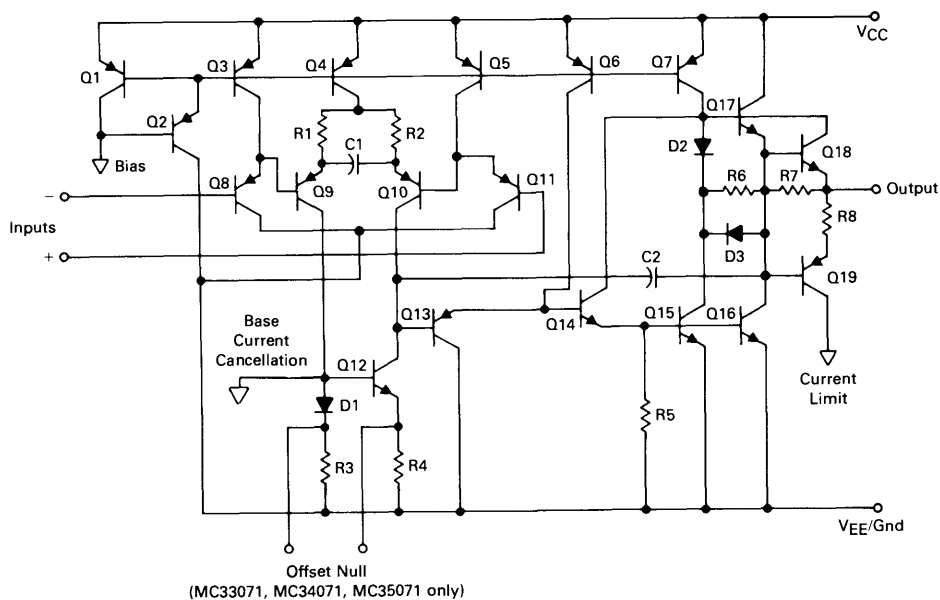
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (from V_{EE} to V_{CC})	V_S	+44	Volts
Input Differential Voltage Range	V_{IDR}	Note 1	Volts
Input Voltage Range	V_{IR}	Note 1	Volts
Output Short-Circuit Duration (Note 2)	t_S	Indefinite	Seconds
Operating Junction Temperature	T_J		$^{\circ}\text{C}$
Ceramic Package		+160	
Plastic Package		+150	
Storage Temperature Range	T_{stg}		$^{\circ}\text{C}$
Ceramic Package		-65 to +160	
Plastic Package		-60 to +150	

NOTES:

1. Either or both input voltages should not exceed the magnitude of V_{CC} or V_{EE} .
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (see Figure 1).

EQUIVALENT CIRCUIT SCHEMATIC (EACH AMPLIFIER)



DC ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $R_L =$ connected to ground unless otherwise noted.
See [Note 3] for $T_A = T_{\text{low}}$ to T_{high})

Characteristic	Symbol	A Suffix			Non-Suffix			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S = 100\ \Omega$, $V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$) $V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{ V}$, $V_{EE} = 0\text{ V}$, $T_A = +25^\circ\text{C}$ $V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = T_{\text{low}}$ to T_{high}	V_{IO}	—	0.5	3.0	—	1.0	5.0	mV
		—	0.5	3.0	—	1.5	5.0	
		—	—	5.0	—	—	7.0	
Average Temperature Coefficient of Input Offset Voltage $R_S = 10\ \Omega$, $V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$, $T_A = T_{\text{low}}$ to T_{high}	$\Delta V_{IO}/\Delta T$	—	10	—	—	10	—	$\mu\text{V}/^\circ\text{C}$
Input Bias Current ($V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$) $T_A = +25^\circ\text{C}$ $T_A = T_{\text{low}}$ to T_{high}	I_{IB}	—	100	500	—	100	500	nA
		—	—	700	—	—	700	
Input Offset Current ($V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$) $T_A = +25^\circ\text{C}$ $T_A = T_{\text{low}}$ to T_{high}	I_{IO}	—	6.0	50	—	6.0	75	nA
		—	—	300	—	—	300	
Input Common Mode Voltage Range $T_A = +25^\circ\text{C}$ $T_A = T_{\text{low}}$ to T_{high}	V_{ICR}	V_{EE} to $(V_{CC} - 1.8)$ V_{EE} to $(V_{CC} - 2.2)$			V_{EE} to $(V_{CC} - 1.8)$ V_{EE} to $(V_{CC} - 2.2)$			V
Large Signal Voltage Gain ($V_O = \pm 10\text{ V}$, $R_L = 2.0\text{ k}\Omega$) $T_A = +25^\circ\text{C}$ $T_A = T_{\text{low}}$ to T_{high}	A_{VOL}	50	100	—	25	100	—	V/mV
		25	—	—	20	—	—	
Output Voltage Swing ($V_{ID} = \pm 1.0\text{ V}$) $V_{CC} = +5.0\text{ V}$, $V_{EE} = 0\text{ V}$, $R_L = 2.0\text{ k}\Omega$, $T_A = +25^\circ\text{C}$ $V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $R_L = 10\text{ k}\Omega$, $T_A = +25^\circ\text{C}$ $V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $R_L = 2.0\text{ k}\Omega$, $T_A = T_{\text{low}}$ to T_{high}	V_{OH}	3.7	4.0	—	3.7	4.0	—	V
		13.6	14	—	13.6	14	—	
		13.4	—	—	13.4	—	—	
$V_{CC} = +5.0\text{ V}$, $V_{EE} = 0\text{ V}$, $R_L = 2.0\text{ k}\Omega$, $T_A = +25^\circ\text{C}$ $V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $R_L = 10\text{ k}\Omega$, $T_A = +25^\circ\text{C}$ $V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $R_L = 2.0\text{ k}\Omega$, $T_A = T_{\text{low}}$ to T_{high}	V_{OL}	—	0.1	0.3	—	0.1	0.3	V
		—	-14.7	-14.3	—	-14.7	-14.3	
		—	—	-13.5	—	—	-13.5	
Output Short-Circuit Current ($V_{ID} = 1.0\text{ V}$, $V_O = 0\text{ V}$, $T_A = 25^\circ\text{C}$) Source Sink	I_{SC}	10	30	—	10	30	—	mA
		20	30	—	20	30	—	
Common Mode Rejection $R_S = 100\text{ k}\Omega$, $V_{CM} = V_{ICR}$, $T_A = 25^\circ\text{C}$	CMR	80	97	—	70	97	—	dB
Power Supply Rejection ($R_S = 100\ \Omega$) $V_{CC}/V_{EE} = +16.5\text{ V}/-16.5\text{ V}$ to $+13.5\text{ V}/-13.5\text{ V}$, $T_A = 25^\circ\text{C}$	PSR	80	97	—	70	97	—	dB
Power Supply Current (Per Amplifier, No Load) $V_{CC} = +5.0\text{ V}$, $V_{EE} = 0\text{ V}$, $V_O = +2.5\text{ V}$, $T_A = +25^\circ\text{C}$ $V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $V_O = 0\text{ V}$, $T_A = +25^\circ\text{C}$ $V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $V_O = 0\text{ V}$, $T_A = T_{\text{low}}$ to T_{high}	I_D	—	1.6	2.0	—	1.6	2.0	mA
		—	1.9	2.5	—	1.9	2.5	
		—	—	2.8	—	—	2.8	

NOTES: (continued)

3. $T_{\text{low}} = -55^\circ\text{C}$ for MC35071,2,4/A
 $= -40^\circ\text{C}$ for MC33071,2,4/A
 $= 0^\circ\text{C}$ for MC34071,2,4/A

$T_{\text{high}} = +125^\circ\text{C}$ for MC35071,2,4/A
 $= +85^\circ\text{C}$ for MC33071,2,4/A
 $= +70^\circ\text{C}$ for MC34071,2,4/A

MC34071, 34072, 34074/MC35071, 35072, 35074/MC33071, 33072, 33074

2

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $R_L =$ connected to ground, $T_A = +25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	A Suffix			Non-Suffix			Unit
		Min	Typ	Max	Min	Typ	Max	
Slew Rate ($V_{in} = -10\text{ V to }+10\text{ V}$, $R_L = 2.0\text{ k}\Omega$, $C_L = 500\text{ pF}$) $A_V = +1.0$ $A_V = -1.0$	SR	8.0 —	10 13	— —	8.0 —	10 13	— —	$\text{V}/\mu\text{s}$
Settling Time (10 V Step, $A_V = -1.0$) To 0.1% (+ 1/2 LSB of 9-Bits) To 0.01% (+ 1/2 LSB of 12-Bits)	t_s	— —	1.1 2.2	— —	— —	1.1 2.2	— —	μs
Gain Bandwidth Product ($f = 100\text{ kHz}$)	GBW	3.5	4.5	—	3.5	4.5	—	MHz
Power Bandwidth $A_V = +1.0$, $R_L = 2.0\text{ k}\Omega$, $V_O = 20\text{ V}_{p-p}$, THD = 5.0%	BW	—	200	—	—	200	—	kHz
Phase Margin $R_L = 2.0\text{ k}\Omega$ $R_L = 2.0\text{ k}\Omega$, $C_L = 300\text{ pF}$	ϕ_m	— —	60 40	— —	— —	60 40	— —	Deg
Gain Margin $R_L = 2.0\text{ k}\Omega$ $R_L = 2.0\text{ k}\Omega$, $C_L = 300\text{ pF}$	A_m	— —	12 4.0	— —	— —	12 4.0	— —	dB
Equivalent Input Noise Voltage $R_S = 100\text{ }\Omega$, $f = 1.0\text{ kHz}$	e_n	—	32	—	—	32	—	$\text{pA}/\sqrt{\text{Hz}}$
Equivalent Input Noise Current $f = 1.0\text{ kHz}$	i_n	—	0.22	—	—	0.22	—	$\text{pA}/\sqrt{\text{Hz}}$
Differential Input Resistance $V_{CM} = 0\text{ V}$	R_{IN}	—	150	—	—	150	—	$\text{M}\Omega$
Differential Input Capacitance $V_{CM} = 0\text{ V}$	C_{IN}	—	2.5	—	—	2.5	—	pF
Total Harmonic Distortion $A_V = +10$, $R_L = 2.0\text{ k}\Omega$, $2.0\text{ V}_{p-p} \leq V_O \leq 20\text{ V}_{p-p}$, $f = 10\text{ kHz}$	THD	—	0.02	—	—	0.02	—	%
Channel Separation ($f = 10\text{ kHz}$)	—	—	120	—	—	120	—	dB
Open-Loop Output Impedance ($f = 1.0\text{ MHz}$)	$ Z_O $	—	30	—	—	30	—	Ω

FIGURE 1 — POWER SUPPLY CONFIGURATIONS

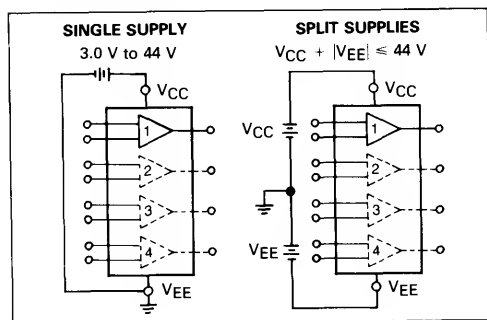
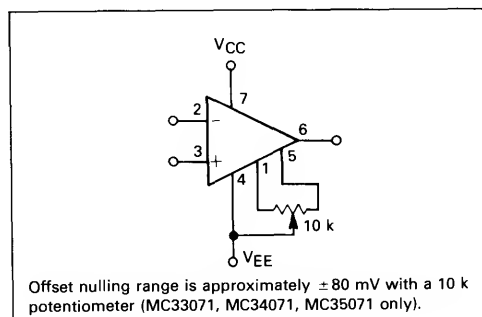


FIGURE 2 — OFFSET NULL CIRCUIT



TYPICAL PERFORMANCE CURVES

FIGURE 3 — MAXIMUM POWER DISSIPATION versus TEMPERATURE FOR PACKAGE TYPES

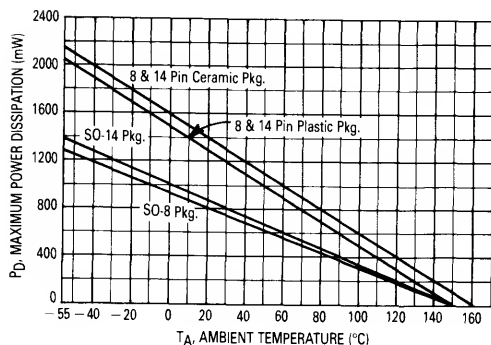


FIGURE 4 — INPUT OFFSET VOLTAGE versus TEMPERATURE FOR REPRESENTATIVE UNITS

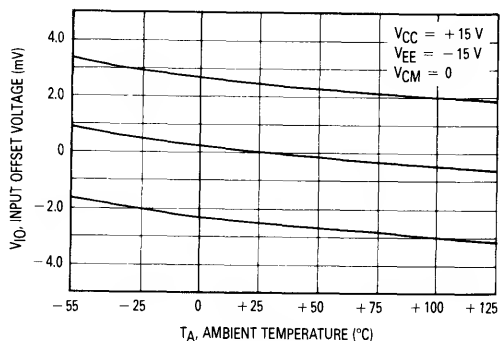


FIGURE 5 — INPUT COMMON MODE VOLTAGE RANGE versus TEMPERATURE

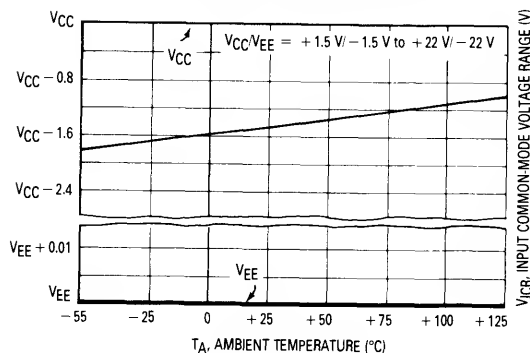


FIGURE 6 — NORMALIZED INPUT BIAS CURRENT versus TEMPERATURE

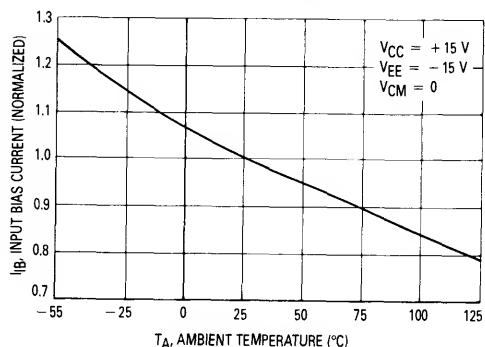


FIGURE 7 — NORMALIZED INPUT BIAS CURRENT versus INPUT COMMON MODE VOLTAGE

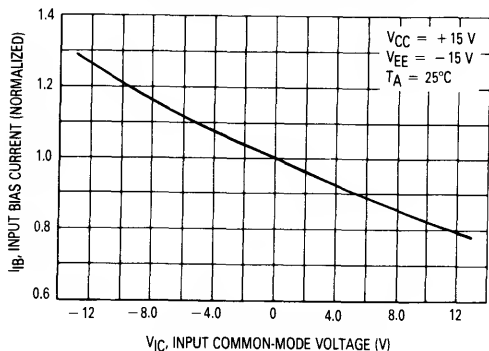


FIGURE 8 — SPLIT SUPPLY OUTPUT VOLTAGE SWING versus SUPPLY VOLTAGE

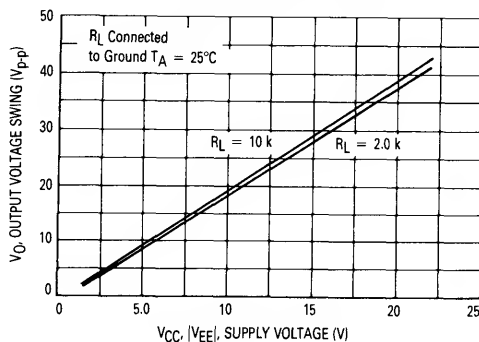


FIGURE 9 — SPLIT SUPPLY OUTPUT SATURATION
versus LOAD CURRENT

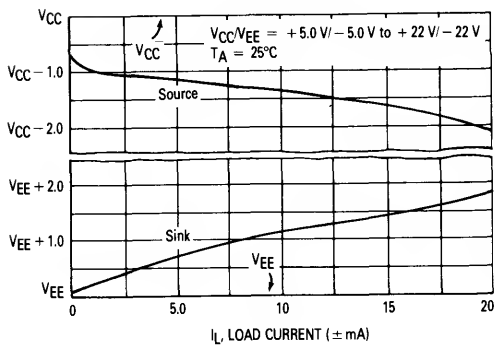


FIGURE 10 — SINGLE SUPPLY OUTPUT SATURATION
versus LOAD RESISTANCE TO GROUND

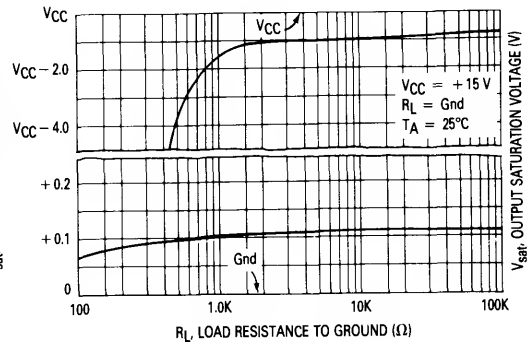


FIGURE 11 — SINGLE SUPPLY OUTPUT SATURATION
versus LOAD RESISTANCE TO V_{CC}

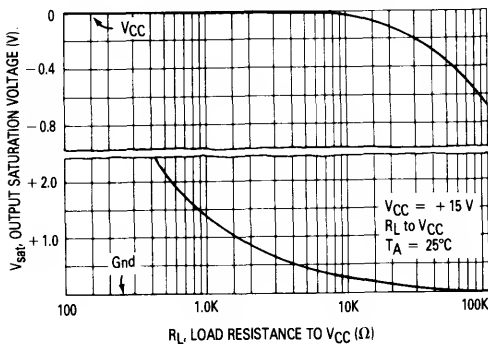


FIGURE 12 — OUTPUT SHORT CIRCUIT CURRENT
versus TEMPERATURE

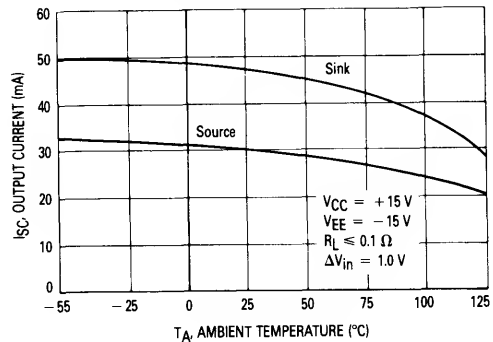


FIGURE 13 — OUTPUT IMPEDANCE versus FREQUENCY

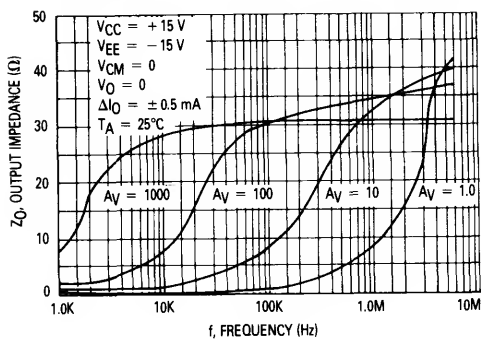


FIGURE 14 — OUTPUT VOLTAGE SWING versus FREQUENCY

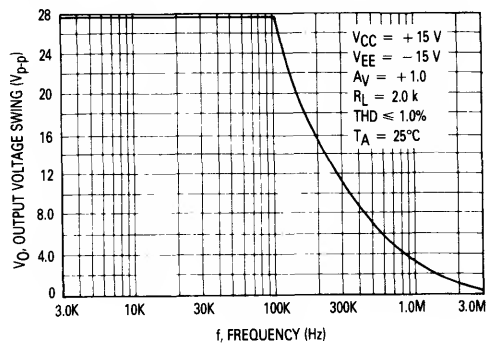


FIGURE 15 — OUTPUT DISTORTION versus FREQUENCY

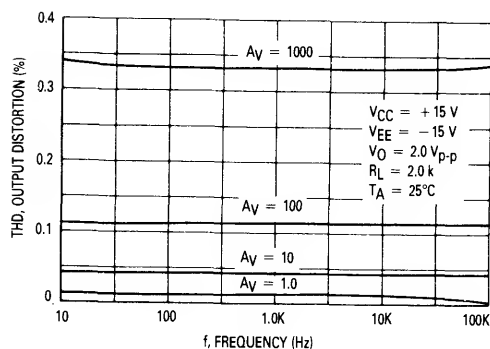


FIGURE 16 — OUTPUT DISTORTION versus OUTPUT VOLTAGE SWING

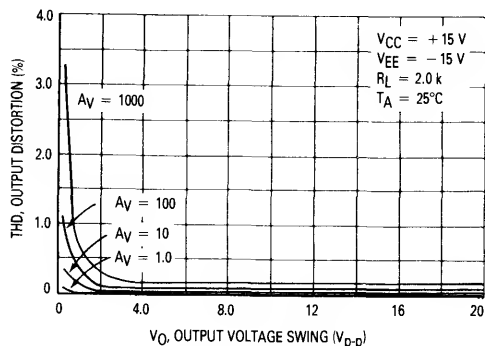


FIGURE 17 — OPEN-LOOP VOLTAGE GAIN versus TEMPERATURE

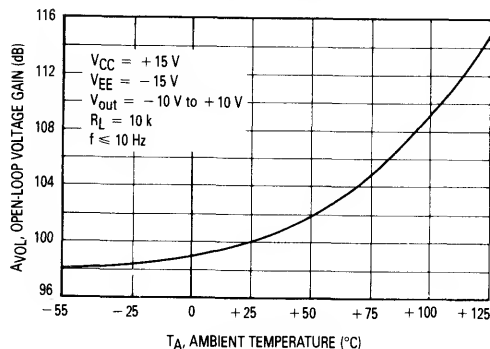


FIGURE 18 — OPEN-LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY

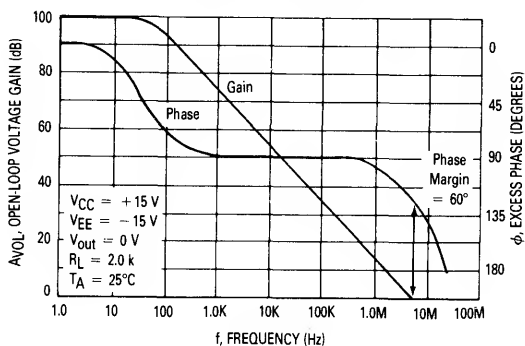


FIGURE 19 — OPEN-LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY

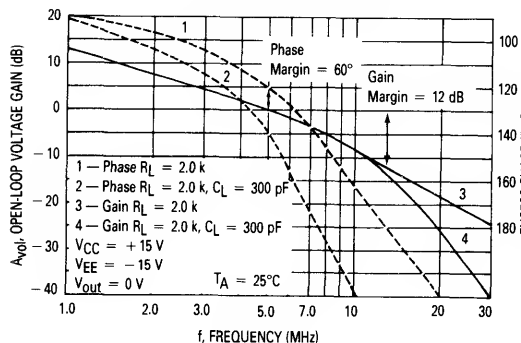


FIGURE 20 — NORMALIZED GAIN BANDWIDTH PRODUCT versus TEMPERATURE

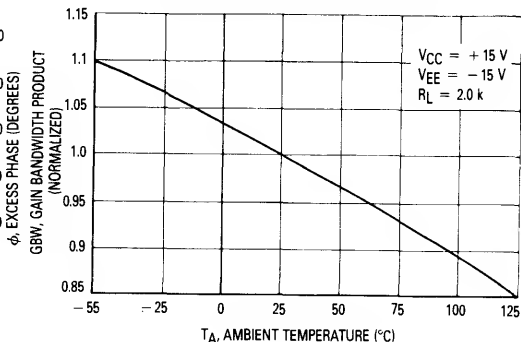


FIGURE 21 — PERCENT OVERSHOOT versus LOAD CAPACITANCE

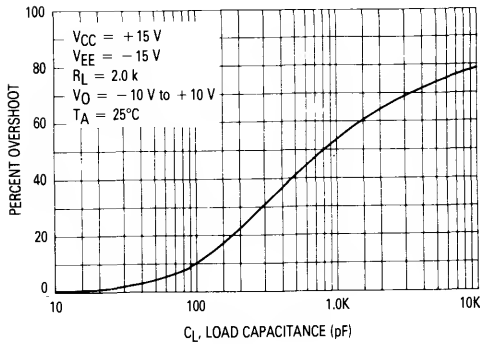


FIGURE 22 — PHASE MARGIN versus LOAD CAPACITANCE

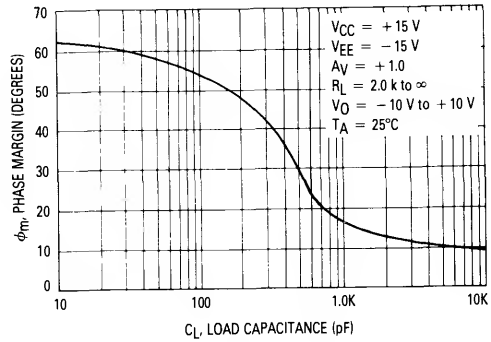


FIGURE 23 — GAIN MARGIN versus LOAD CAPACITANCE

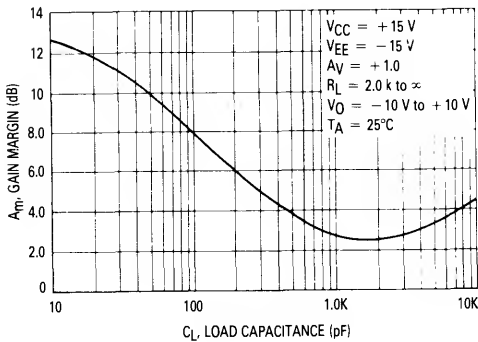


FIGURE 24 — PHASE MARGIN versus TEMPERATURE

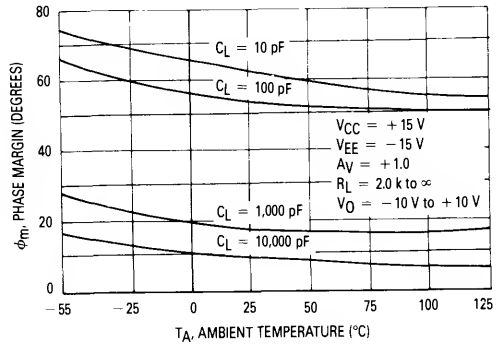


FIGURE 25 — GAIN MARGIN versus TEMPERATURE

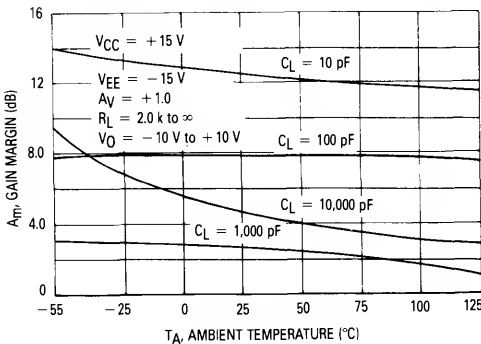
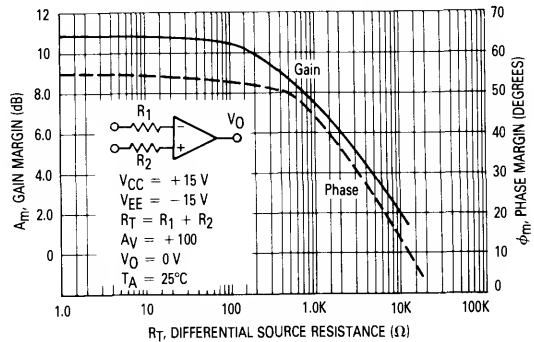


FIGURE 26 — PHASE MARGIN AND GAIN MARGIN versus DIFFERENTIAL SOURCE RESISTANCE



2

FIGURE 27 — NORMALIZED SLEW RATE
versus TEMPERATURE

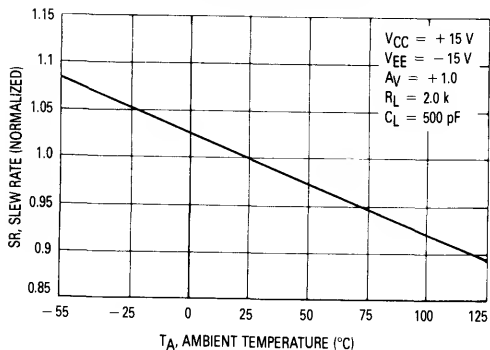


FIGURE 28 — OUTPUT SETTLING TIME

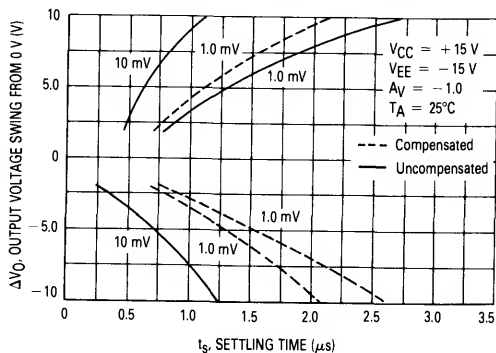


FIGURE 29 — SMALL SIGNAL TRANSIENT RESPONSE

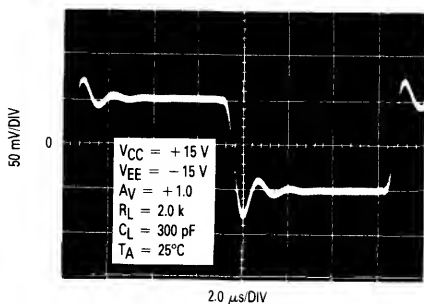


FIGURE 30 — LARGE SIGNAL TRANSIENT RESPONSE

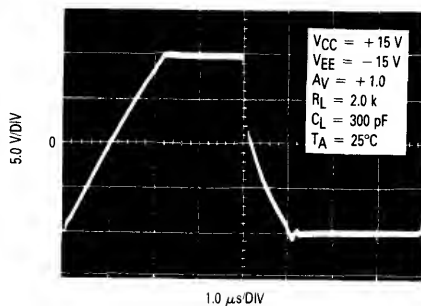


FIGURE 31 — COMMON MODE REJECTION
versus FREQUENCY

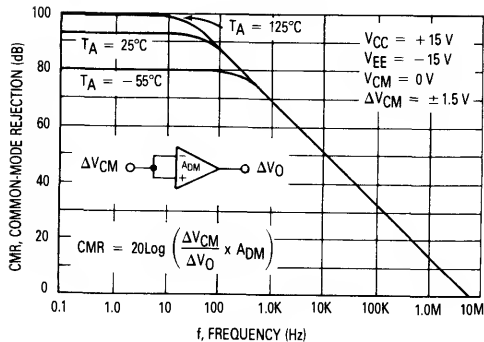


FIGURE 32 — POWER SUPPLY REJECTION
versus FREQUENCY

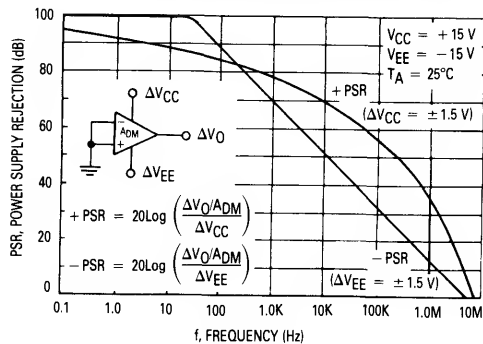


FIGURE 33 — SUPPLY CURRENT versus SUPPLY VOLTAGE

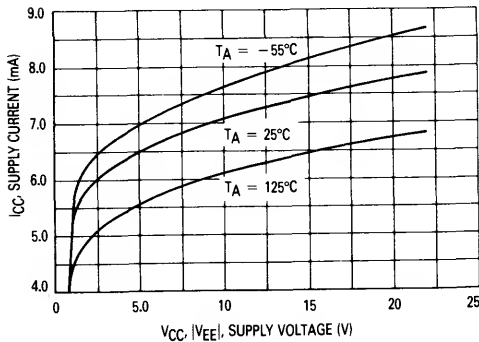


FIGURE 35 — CHANNEL SEPARATION versus FREQUENCY

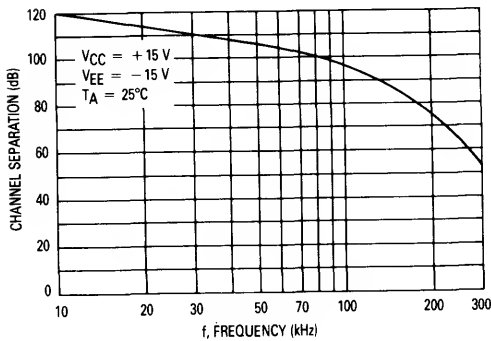


FIGURE 34 — POWER SUPPLY REJECTION versus TEMPERATURE

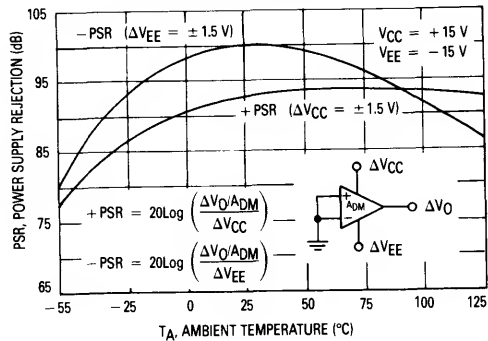
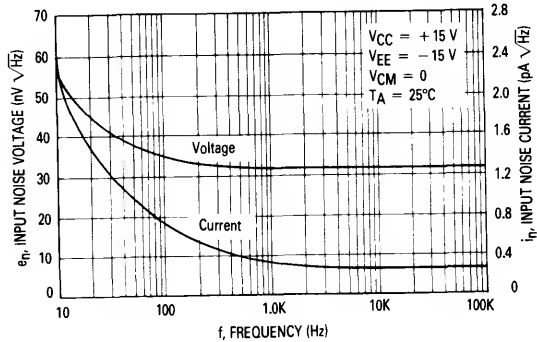


FIGURE 36 — INPUT NOISE versus FREQUENCY



APPLICATIONS INFORMATION

CIRCUIT DESCRIPTION/PERFORMANCE FEATURES OF THE MC34071 SERIES

Although the bandwidth, slew rate, and settling time of the MC34071 amplifier series are similar to op amp products utilizing JFET input devices, these amplifiers offer other additional distinct advantages as a result of the PNP transistor differential input stage and an all NPN transistor output stage.

Since the input common mode voltage range of this input stage includes the V_{EE} potential, single supply operation is feasible to as low as 3.0 volts with the common mode input voltage at ground potential.

The input stage also allows differential input voltages up to ± 44 volts, provided the maximum input voltage range is not exceeded. Specifically, the input voltages must range between V_{EE} and V_{CC} supply voltages as

shown by the maximum rating table. In practice, although not recommended, the input voltages can exceed the V_{CC} voltage by approximately 3.0 volts and decrease below the V_{EE} voltage by 0.3 volts without causing product damage, although output phase reversal may occur. It is also possible to source up to approximately 5.0 mA of current from V_{EE} through either input's clamping diode without damage or latching, although phase reversal may again occur.

If one or both inputs exceed the upper common mode voltage limit the amplifier output is readily predictable and may be in a low or high state depending on the existing input bias conditions.

Since the input capacitance associated with the small geometry input device is substantially lower (2.5 pF) than the typical JFET input gate capacitance (5.0 pF), better frequency response for a given input source resistance can be achieved using the MC34071 series of amplifiers. This performance feature becomes evident, for example, in fast settling D-to-A current to voltage conversion applications where the feedback resistance can form an input pole with the input capacitance of the op amp. This input pole creates a 2nd order system with the single pole op amp and is therefore detrimental to its settling time. In this context, lower input capacitance is desirable especially for higher values of feedback resistances (lower current DAC's). This input pole can be compensated for by creating a feedback zero with a capacitance across the feedback resistance, if necessary, to reduce overshoot. For 2.0 k Ω of feedback resistance, the MC34071 series can settle to within 1/2 LSB of 8 bits in 1.0 μ s, and within 1/2 LSB of 12 bits in 2.2 μ s for a 10 volt step. In a inverting unity gain fast settling configuration, the symmetrical slew rate is ± 13 volts/ μ s. In the classic noninverting unity gain configuration the output positive slew rate is +10 volts/ μ s, and the corresponding negative slew rate will exceed the positive slew rate as a function of the fall time of the input waveform.

Since the bipolar input device matching characteristics are superior to that of JFETs, a low untrimmed maximum offset voltage of 3.0 mV prime and 5.0 mV downgrade can be economically offered with high frequency performance characteristics. This combination is ideal for low cost precision, high speed quad op amp applications.

The all NPN output stage, shown in its basic form on the equivalent circuit schematic, offers unique advantages over the more conventional NPN/PNP transistor Class AB output stage. A 10 k Ω load resistance can swing within 1.0 volt of the positive rail (V_{CC}), and within 0.3 volts of the negative rail (V_{EE}), providing a 28.7 V_{p-p} swing from ± 15 volt supplies. This large output swing becomes most noticeable at lower supply voltages.

The positive swing is limited by the saturation voltage of the current source transistor Q7, and V_{BE} of the NPN pull up transistor Q17, and the voltage drop associated with the short circuit resistance, R_7 . The negative swing is limited by the saturation voltage of the pull-down transistor Q16, the voltage drop $I_L R_6$, and the voltage drop associated with resistance R_7 , where I_L is the sink load current. For small valued sink currents, the above voltage drops are negligible, allowing the negative swing voltage to approach within millivolts of V_{EE} . For large valued sink currents (> 5.0 mA), diode D3 clamps the voltage across R_6 , thus limiting the negative swing to the saturation voltage of Q16, plus the forward diode drop of D3 ($\approx V_{EE} + 1.0$ V). Thus for a given supply voltage, unprecedented peak-to-peak output voltage swing is possible as indicated by the output swing specifications.

If the load resistance is referenced to V_{CC} instead of ground for single supply applications, the maximum possible output swing can be achieved for a given sup-

ply voltage. For light load currents, the load resistance will pull the output to V_{CC} during the positive swing and the output will pull the load resistance near ground during the negative swing. The load resistance value should be much less than that of the feedback resistance to maximize pull up capability.

Because the PNP output emitter-follower transistor has been eliminated, the MC34071 series offers a 20 mA minimum current sink capability, typically to an output voltage of ($V_{EE} + 1.8$ V). In single supply applications the output can directly source or sink base current from a common emitter NPN transistor for fast high current switching applications.

In addition, the all NPN transistor output stage is inherently fast, contributing to the bipolar amplifier's high gain bandwidth product and fast settling capability. The associated high frequency low output impedance (30 Ω typ @ 1.0 MHz) allows capacitive drive capability from 0 to 10,000 pF without oscillation in the unity closed loop gain configuration. The 60° phase margin and 12 dB gain margin as well as the general gain and phase characteristics are virtually independent of the source/sink output swing conditions. This allows easier system phase compensation, since output swing will not be a phase consideration. The high frequency characteristics of the MC34071 series also allow excellent high frequency active filter capability, especially for low voltage single supply applications.

Although the single supply specification is defined at 5.0 volts, these amplifiers are functional to 3.0 volts @ 25°C although slight changes in parametrics such as bandwidth, slew rate, and dc gain may occur.

If power to this integrated circuit is applied in reverse polarity or if the IC is installed backwards in a socket, large unlimited current surges will occur through the device that may result in device destruction.

Special static precautions are not necessary for these bipolar amplifiers since there are no MOS transistors on the die.

As usual with most high frequency amplifiers, proper lead dress, component placement, and PC board layout should be exercised for optimum frequency performance. For example, long unshielded input or output leads may result in unwanted input-output coupling. In order to preserve the relatively low input capacitance associated with these amplifiers, resistors connected to the inputs should be immediately adjacent to the input pin to minimize additional stray input capacitance. This not only minimizes the input pole for optimum frequency response, but also minimizes extraneous "pick up" at this node. Supply decoupling with adequate capacitance immediately adjacent to the supply pin is also important, particularly over temperature, since many types of decoupling capacitors exhibit great impedance changes over temperature.

The output of any one amplifier is current limited and thus protected from a direct short to ground. However, under such conditions, it is important not to allow the device to exceed the maximum junction temperature rating. Typically for ± 15 volt supplies, any one output can be shorted continuously to ground without exceeding the maximum temperature rating.

TYPICAL SINGLE SUPPLY APPLICATIONS $V_{CC} = 5.0$ VOLTS

FIGURE 37 — AC COUPLED NONINVERTING AMPLIFIER

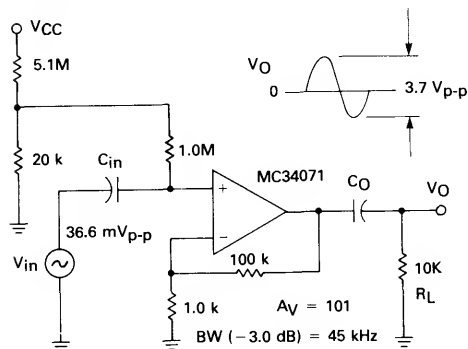


FIGURE 38 — AC COUPLED INVERTING AMPLIFIER

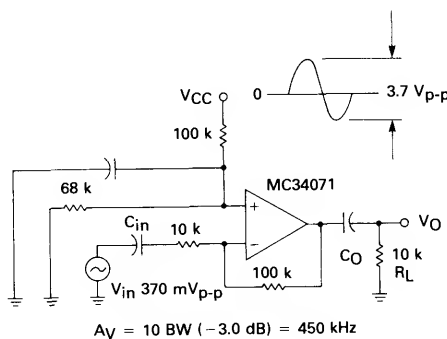


FIGURE 39 — DC COUPLED INVERTING AMPLIFIER
MAXIMUM OUTPUT SWING

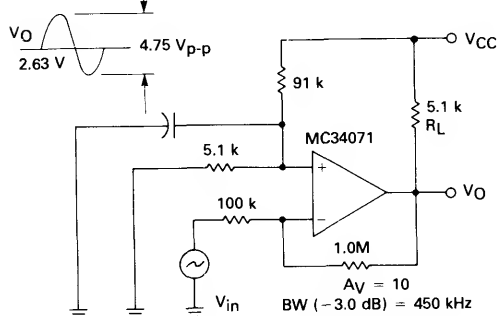


FIGURE 40 — UNITY GAIN BUFFER TTL DRIVER

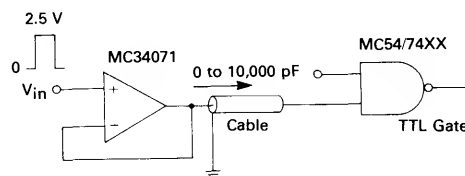


FIGURE 41 — ACTIVE HIGH-Q NOTCH FILTER

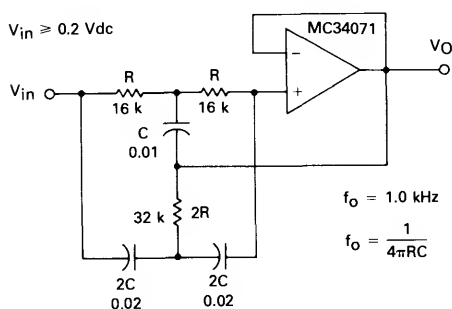
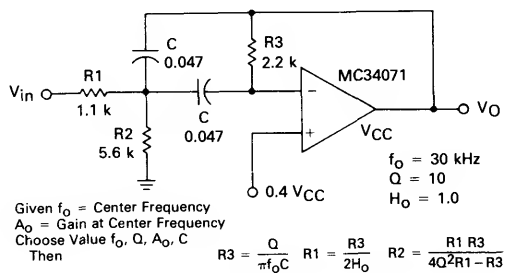


FIGURE 42 — ACTIVE BANDPASS FILTER



For less than 10% error from operational amplifier

$$\frac{Q_0 f_0}{GBW} < 0.1$$

Where f_0 and GBW are expressed in Hz.
 $GBW = 4.5$ MHz Typ.

FIGURE 43 — LOW VOLTAGE FAST D/A CONVERTER

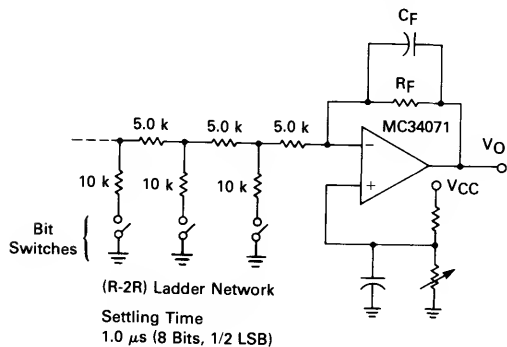


FIGURE 44 — HIGH SPEED LOW VOLTAGE COMPARATOR

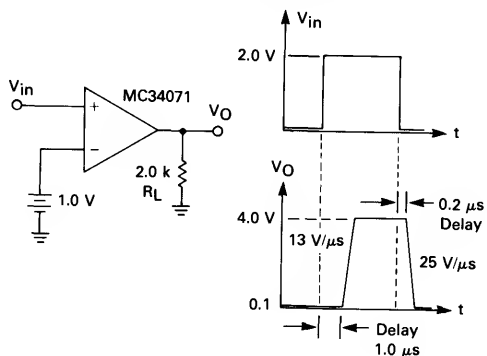


FIGURE 45 — LED DRIVER

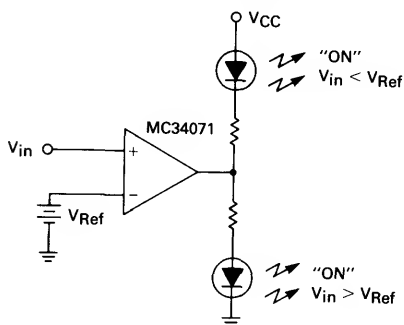


FIGURE 46 — TRANSISTOR DRIVER

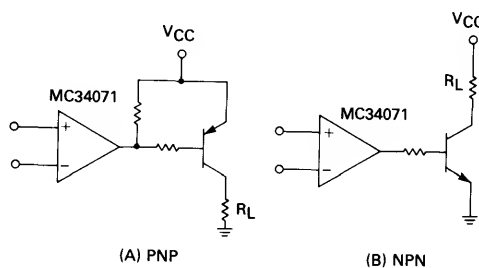


FIGURE 47 — AC/DC GROUND CURRENT MONITOR

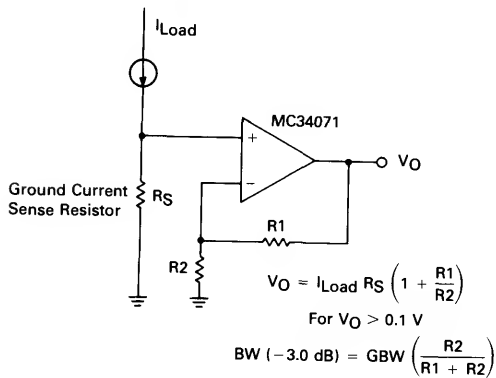


FIGURE 48 — PHOTOVOLTAIC CELL AMPLIFIER

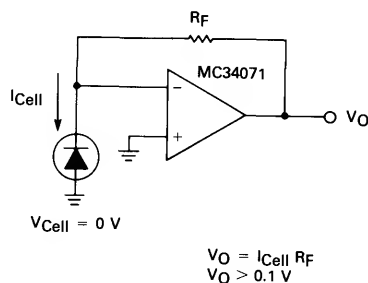


FIGURE 49 — LOW INPUT VOLTAGE COMPARATOR WITH HYSTERESIS

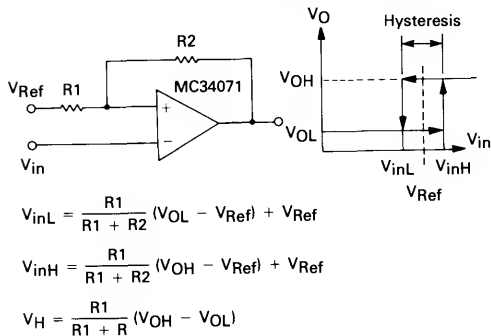


FIGURE 50 — HIGH COMPLIANCE VOLTAGE TO SINK CURRENT CONVERTER

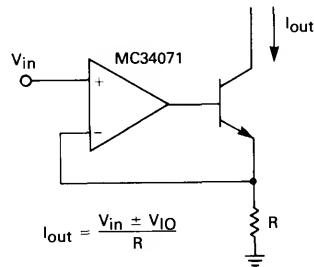


FIGURE 51 — HIGH INPUT IMPEDANCE DIFFERENTIAL AMPLIFIER

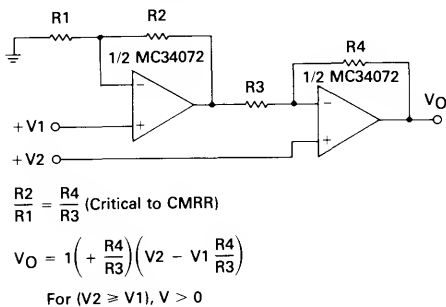


FIGURE 52 — BRIDGE CURRENT AMPLIFIER

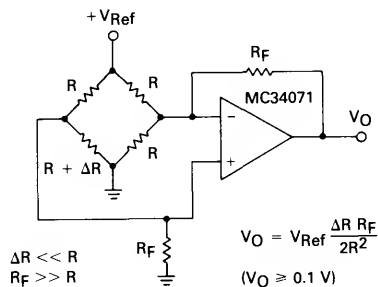


FIGURE 53 — LOW VOLTAGE PEAK DETECTOR

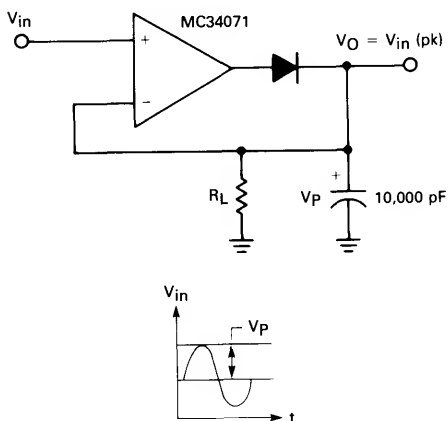
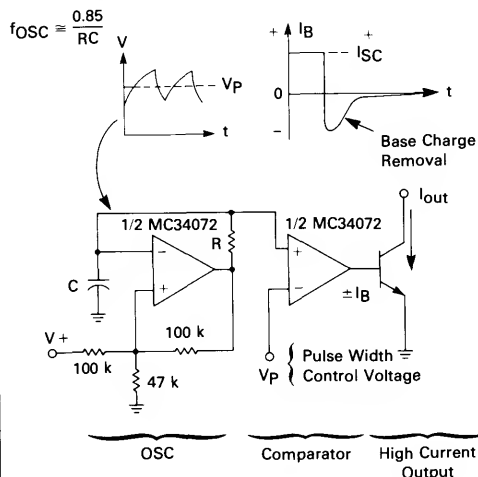


FIGURE 54 — HIGH FREQUENCY PULSE WIDTH MODULATION



GENERAL ADDITIONAL APPLICATIONS INFORMATION $V_S = \pm 15$ VOLTS

FIGURE 55 — SECOND ORDER LOW-PASS ACTIVE FILTER

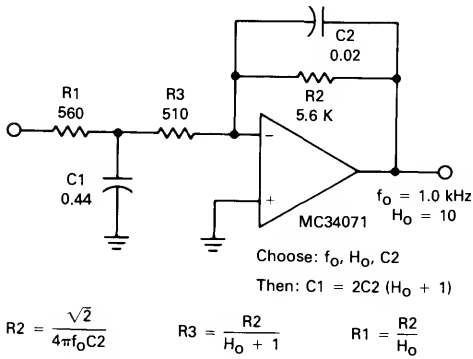


FIGURE 56 — SECOND ORDER HIGH-PASS ACTIVE FILTER

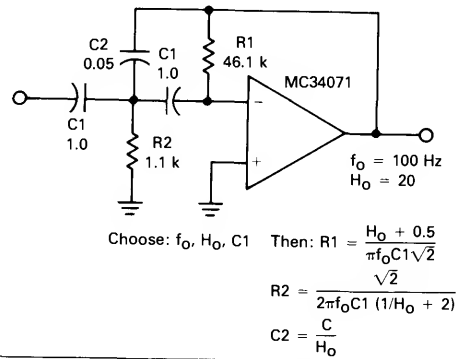


FIGURE 57 — FAST SETTLING INVERTER

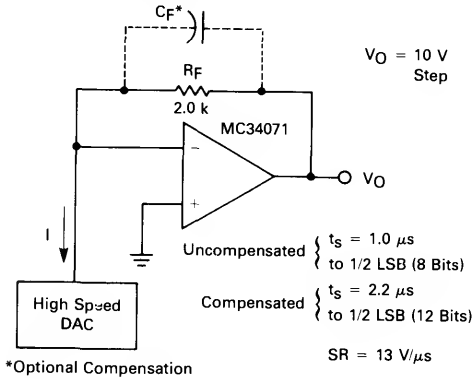


FIGURE 58 — BASIC INVERTING AMPLIFIER

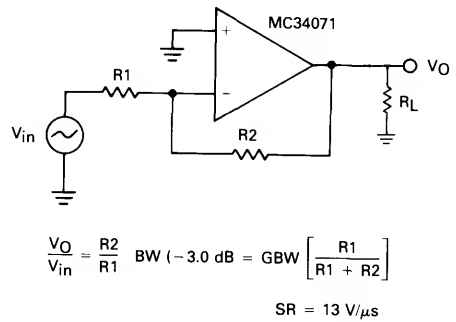


FIGURE 59 — BASIC NON INVERTING AMPLIFIER

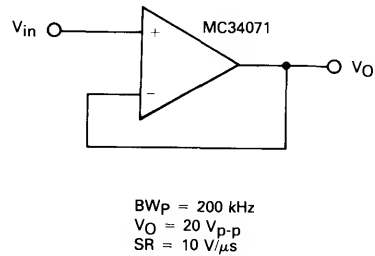
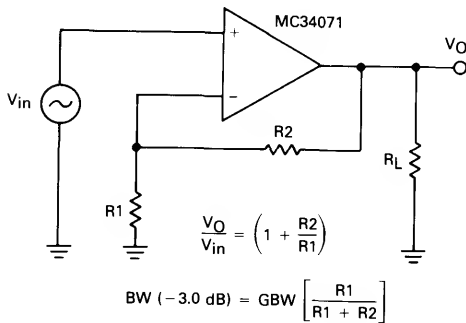


FIGURE 61 — HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER

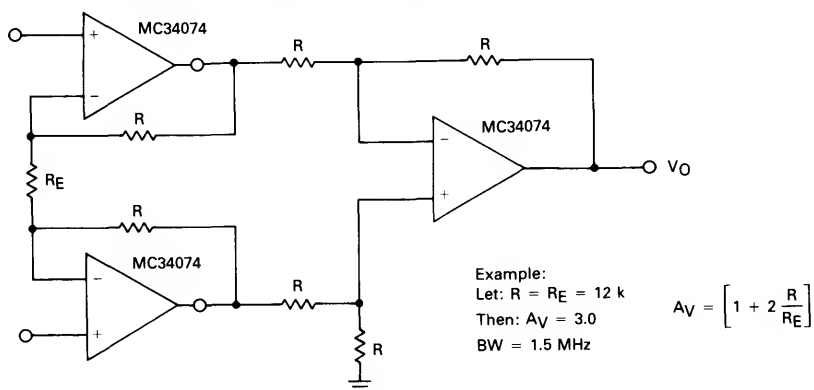
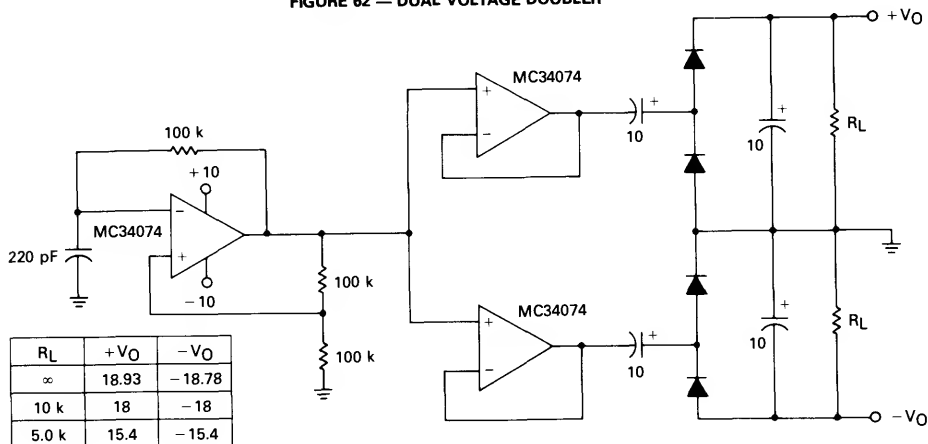


FIGURE 62 — DUAL VOLTAGE DOUBLER



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

HIGH SLEW RATE, WIDE BANDWIDTH, JFET INPUT OPERATIONAL AMPLIFIERS

These devices are a new generation of high speed JFET input monolithic operational amplifiers. Innovative design concepts along with JFET technology provide wide gain bandwidth product and high slew rate. Well matched JFET input devices and advanced trim techniques ensure low input offset errors and bias currents. The all NPN output stage features large output voltage swing, no deadband crossover distortion, high capacitive drive capability, excellent phase and gain margins, low open-loop output impedance, and symmetrical source/sink ac frequency response.

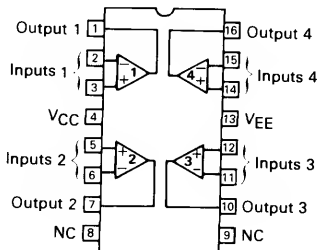
This series of devices are available in standard or prime performance (A suffix) grades, fully compensated or decompensated ($A_{VCL} \geq 2$) and are specified over commercial or Military temperature ranges. They are pin compatible with existing Industry standard operational amplifiers, and allow the designer to easily upgrade the performance of existing designs.

- Wide Gain Bandwidth: 8.0 MHz for Fully Compensated Devices
16 MHz for Decompensated Devices
- High Slew Rate: 25 V/ μ s for Fully Compensated Devices
50 V/ μ s for Decompensated Devices
- High Input Impedance: $10^{12} \Omega$
- Input Offset Voltage: 0.5 mV Maximum (Single Amplifier)
- Large Output Voltage Swing: -14.7 V to $+14$ V for
 $V_{CC}/V_{EE} = \pm 15$ V
- Low Open-Loop Output Impedance: 30Ω @ 1.0 MHz
- Low THD Distortion: 0.01%
- Excellent Phase/Gain Margins: 55°/7.6 dB for Fully Compensated Devices

ORDERING INFORMATION

Op Amp Function	Fully Compensated	$A_{VCL} \geq 2$ Decompensated	Temperature Range	Package
Single	MC35081U,AU	MC35080U,AU	-55 to $+125^\circ\text{C}$	Ceramic DIP
	MC34081D,AD MC34081P,AP	MC34080D,AD MC34080P,AP		SO-8 Plastic DIP
Dual	MC34082P,AP	MC34083P,AP	0 to $+70^\circ\text{C}$	Plastic DIP
Quad	MC35084L,AL	MC35085L,AL	-55 to $+125^\circ\text{C}$	Ceramic DIP
	MC34084DW,ADW MC34084P,AP	MC34085DW,ADW MC34085P,AP		SO-16L Plastic DIP


DW SUFFIX
PLASTIC PACKAGE
CASE 751G
(SO-16L)



MC34080/MC35080 thru MC34085/MC35085

HIGH PERFORMANCE JFET INPUT OPERATIONAL AMPLIFIERS



P SUFFIX
PLASTIC PACKAGE
CASE 626

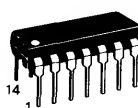
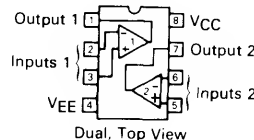
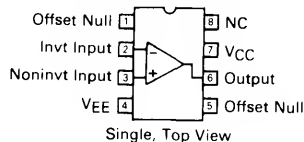


U SUFFIX
CERAMIC PACKAGE
CASE 693

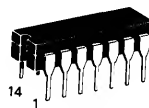
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)



PIN ASSIGNMENTS

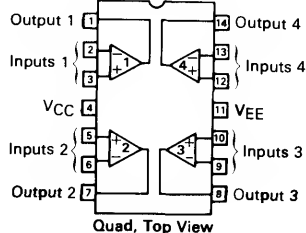


P SUFFIX
PLASTIC PACKAGE
CASE 646



L SUFFIX
CERAMIC PACKAGE
CASE 632

PIN ASSIGNMENTS



2

Rating	Symbol	Value	Unit
Supply Voltage (from V_{CC} to V_{EE})	V_S	+ 44	V
Input Differential Voltage Range	V_{IDR}	(Note 1)	V
Input Voltage Range	V_{IR}	(Note 1)	V
Output Short-Circuit Duration (Note 2)	t_S	Indefinite	Seconds
Operating Ambient Temperature Range MC35XXX MC34XXX	T_A	- 55 to + 125 0 to + 70	°C
Operating Junction Temperature Ceramic Package Plastic Package	T_J	+ 165 + 125	°C
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}	- 65 to + 165 - 55 to + 125	°C

2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded.

MOTOROLA LINEAR/INTERFACE DEVICES

MC34080, MC35080 Series

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = T_{\text{low}}$ to T_{high} [Note 3], unless otherwise noted)

Characteristic	Symbol	A Suffix			Non-Suffix			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 4) Single $T_A = +25^\circ\text{C}$ $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ (MC34080, MC34081) $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ (MC35080, MC35081) Dual $T_A = +25^\circ\text{C}$ $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ (MC34082, MC34083) $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ (MC35082, MC35083) Quad $T_A = +25^\circ\text{C}$ $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ (MC34084, MC34085) $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ (MC35084, MC35085)	V_{IO}	—	0.3	0.5	—	0.5	1.0	mV
		—	—	2.5	—	—	3.0	
		—	—	3.5	—	—	4.0	
		—	0.6	1.0	—	1.0	3.0	
		—	—	3.0	—	—	5.0	
		—	—	4.0	—	—	6.0	
		—	3.0	6.0	—	6.0	12	
		—	—	8.0	—	—	14	
		—	—	9.0	—	—	15	
Average Temperature Coefficient of Offset Voltage	$\Delta V_{IO}/\Delta T$	—	10	—	—	10	—	$\mu\text{V}/^\circ\text{C}$
Input Bias Current ($V_{CM} = 0$ Note 5) $T_A = +25^\circ\text{C}$ $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$	I_{IB}	—	0.06	0.2	—	0.06	0.2	nA
		—	—	4.0	—	—	4.0	
		—	—	50	—	—	50	
Input Offset Current ($V_{CM} = 0$ Note 5) $T_A = +25^\circ\text{C}$ $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$	I_{IO}	—	0.02	0.1	—	0.02	0.1	nA
		—	—	2.0	—	—	2.0	
		—	—	25	—	—	25	
Large Signal Voltage Gain ($V_O = \pm 10\text{ V}$, $R_L = 2.0\text{ k}$) $T_A = +25^\circ\text{C}$ $T_A = T_{\text{low}}$ to T_{high}	A_{VOL}	50 25	80 —	— —	25 15	80 —	— —	V/mV
Output Voltage Swing $R_L = 2.0\text{ k}$, $T_A = +25^\circ\text{C}$ $R_L = 10\text{ k}$, $T_A = +25^\circ\text{C}$ $R_L = 10\text{ k}$, $T_A = T_{\text{low}}$ to T_{high}	V_{OH}	13.2 13.4 13.4	13.7 13.9 —	— — —	13.2 13.4 13.4	13.7 13.9 —	— — —	V
	V_{OL}	— — —	-14.1 -14.7 -14.0	-13.5 -14.1 —	— -14.7 —	-14.1 -14.7 —	-13.5 -14.1 -14.0	
Output Short-Circuit Current ($T_A = +25^\circ\text{C}$) Input Overdrive = 1.0 V, Output to Ground Source Sink	I_{SC}	20 20	31 28	— —	20 20	31 28	— —	mA
Input Common Mode Voltage Range $T_A = +25^\circ\text{C}$	V_{ICR}	$(V_{EE} + 4.0)$ to $(V_{CC} - 2.0)$			$(V_{EE} + 4.0)$ to $(V_{CC} - 2.0)$			V
Common Mode Rejection Ratio ($R_S \leq 10\text{ k}$, $T_A = +25^\circ\text{C}$)	CMRR	75	90	—	70	90	—	dB
Power Supply Rejection Ratio ($R_S = 100\ \Omega$, $T_A = 25^\circ\text{C}$)	PSRR	75	86	—	70	86	—	dB
Power Supply Current Single $T_A = +25^\circ\text{C}$ $T_A = T_{\text{low}}$ to T_{high} Dual $T_A = +25^\circ\text{C}$ $T_A = T_{\text{low}}$ to T_{high} Quad $T_A = +25^\circ\text{C}$ $T_A = T_{\text{low}}$ to T_{high}	I_D	— — — — —	2.5 — 4.9 — 9.7	3.4 4.2 6.0 7.5 11	— — — — —	2.5 — 4.9 — 9.7	3.4 4.2 6.0 7.5 11	mA
		—	—	13	—	—	13	

NOTES: (CONTINUED)

3. $T_{\text{low}} = -55^\circ\text{C}$ for MC35080,A $T_{\text{low}} = 0^\circ\text{C}$ for MC34080,A $T_{\text{high}} = +125^\circ\text{C}$ for MC35080,A $T_{\text{high}} = +70^\circ\text{C}$ for MC34080,A
- | | | | |
|-----------|-----------|-----------|-----------|
| MC35081,A | MC34081,A | MC35081,A | MC34081,A |
| MC35082,A | MC34082,A | MC35082,A | MC34082,A |
| MC35083,A | MC34083,A | MC35083,A | MC34083,A |
| MC35084,A | MC34084,A | MC35084,A | MC34084,A |
| MC35085,A | MC34085,A | MC35085,A | MC34085,A |

4. See application information for typical changes in input offset voltage due to solderability and temperature cycling.
5. Limits at $T_A = +25^\circ\text{C}$ are guaranteed by high temperature (T_{high}) testing.

MC34080, MC35080 Series

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = +25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	A Suffix			Non-Suffix			Unit
		Min	Typ	Max	Min	Typ	Max	
Slew Rate ($V_{in} = -10\text{ V to } +10\text{ V}$, $R_L = 2.0\text{ k}$, $C_L = 100\text{ pF}$) Compensated $A_V = +1.0$ $A_V = -1.0$ Decompensated $A_V = +2.0$ $A_V = -1.0$	SR	20	25	—	20	25	—	V/ μs
Settling Time (10 V Step, $A_V = -1.0$) To 0.10% ($\pm 1/2$ LSB of 9-Bits) To 0.01% ($\pm 1/2$ LSB of 12-Bits)	t_s	—	0.72	—	—	0.72	—	μs
Gain Bandwidth Product ($f = 200\text{ kHz}$) Compensated Decompensated	GBW	6.0	8.0	—	6.0	8.0	—	MHz
Power Bandwidth ($R_L = 2.0\text{ k}$, $V_O = 20\text{ V}_{p-p}$, THD = 5.0%) Compensated $A_V = +1.0$ Decompensated $A_V = -1.0$	BWp	—	400	—	—	400	—	kHz
Phase Margin (Compensated) $R_L = 2.0\text{ k}$ $R_L = 2.0\text{ k}$, $C_L = 100\text{ pF}$	ϕ_m	—	55	—	—	55	—	Degrees
Gain Margin (Compensated) $R_L = 2.0\text{ k}$ $R_L = 2.0\text{ k}$, $C_L = 100\text{ pF}$	A_m	—	7.6	—	—	7.6	—	dB
Equivalent Input Noise Voltage $R_S = 100\text{ }\Omega$, $f = 1.0\text{ kHz}$	e_n	—	30	—	—	30	—	nV/ $\sqrt{\text{Hz}}$
Equivalent Input Noise Current ($f = 1.0\text{ kHz}$)	i_n	—	0.01	—	—	0.01	—	pA/ $\sqrt{\text{Hz}}$
Input Capacitance	C_i	—	5.0	—	—	5.0	—	pF
Input Resistance	r_i	—	10^{12}	—	—	10^{12}	—	Ω
Total Harmonic Distortion $A_V = +10$, $R_L = 2.0\text{ k}$, $2.0 \leq V_O \leq 20\text{ V}_{p-p}$, $f = 10\text{ kHz}$	THD	—	0.05	—	—	0.05	—	%
Channel Separation ($f = 10\text{ kHz}$)	—	—	120	—	—	120	—	dB
Open-Loop Output Impedance ($f = 1.0\text{ MHz}$)	z_o	—	35	—	—	35	—	Ω

TYPICAL PERFORMANCE CURVES

FIGURE 1 — INPUT COMMON MODE VOLTAGE RANGE
versus TEMPERATURE

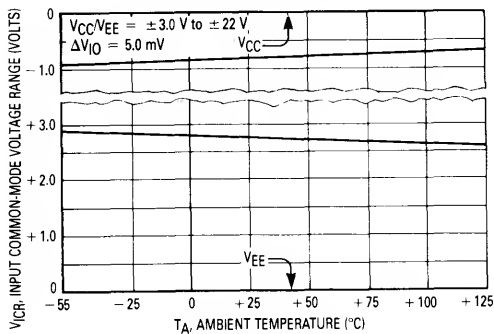


FIGURE 2 — INPUT BIAS CURRENT
versus TEMPERATURE

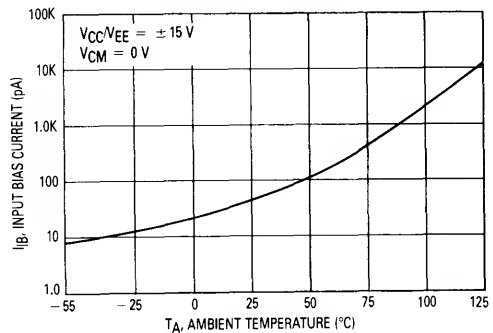


FIGURE 3 — INPUT BIAS CURRENT versus INPUT COMMON-MODE VOLTAGE

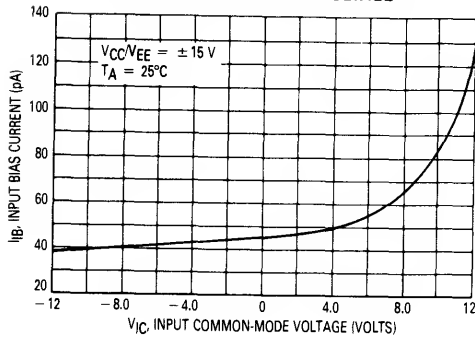


FIGURE 4 — OUTPUT VOLTAGE SWING versus SUPPLY VOLTAGE

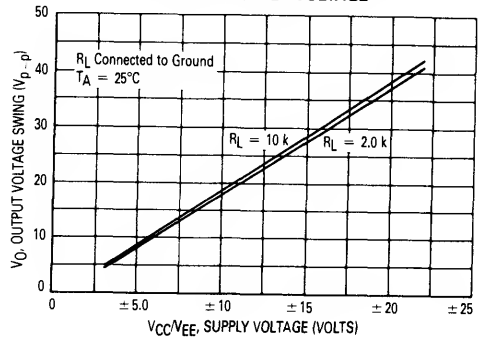


FIGURE 5 — OUTPUT SATURATION versus LOAD CURRENT

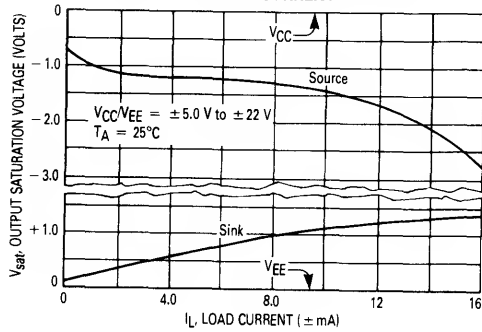


FIGURE 6 — OUTPUT SATURATION versus LOAD RESISTANCE TO GROUND

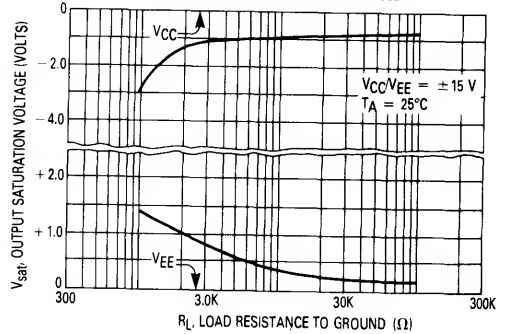


FIGURE 7 — OUTPUT SATURATION versus LOAD RESISTANCE TO V_{CC}

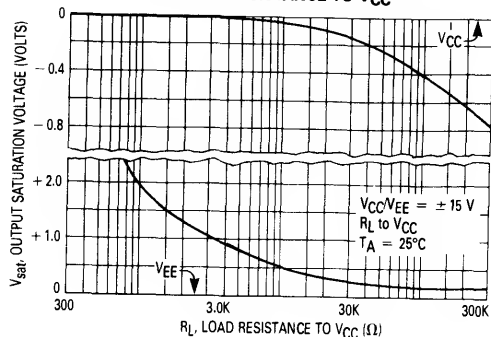


FIGURE 8 — OUTPUT SHORT CIRCUIT CURRENT versus TEMPERATURE

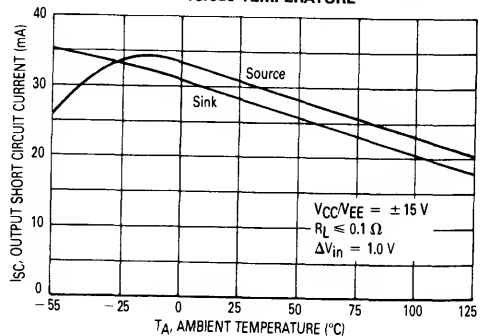


FIGURE 9 — OUTPUT IMPEDANCE versus FREQUENCY

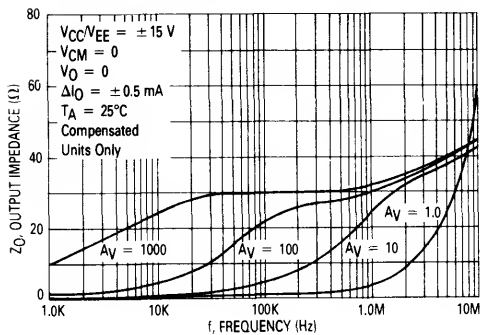


FIGURE 10 — OUTPUT IMPEDANCE versus FREQUENCY

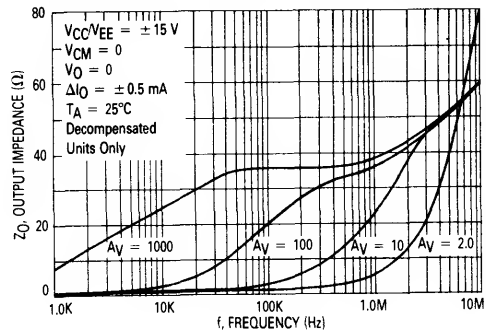


FIGURE 11 — OUTPUT VOLTAGE SWING versus FREQUENCY

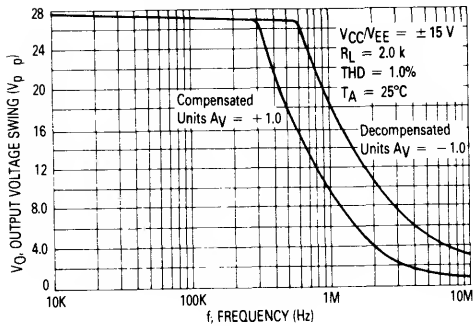


FIGURE 12 — OUTPUT DISTORTION versus FREQUENCY

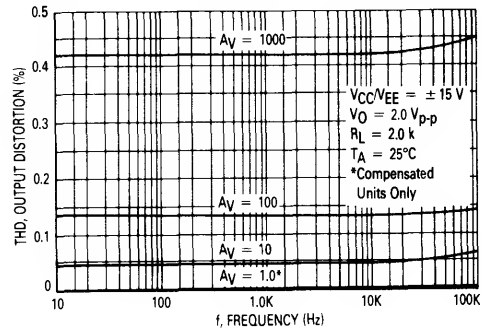


FIGURE 13 — OPEN-LOOP VOLTAGE GAIN versus TEMPERATURE

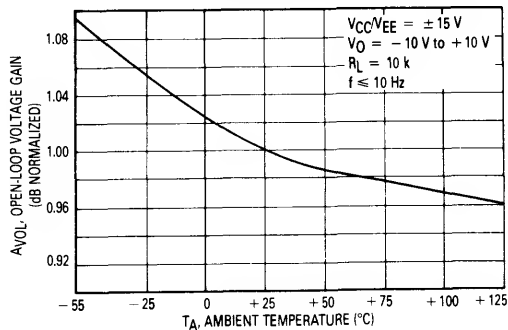


FIGURE 14 — OPEN-LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY

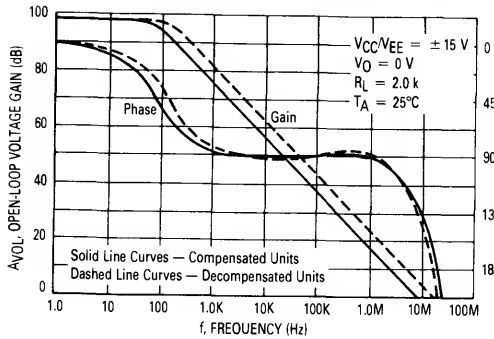


FIGURE 15 — OPEN-LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY

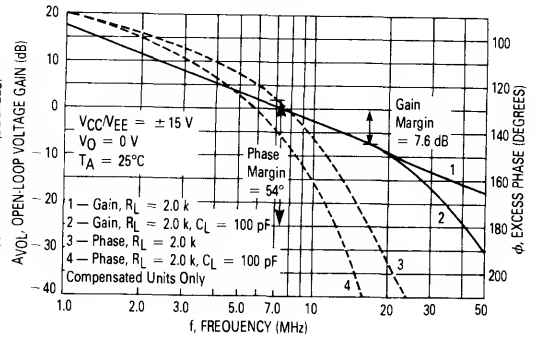


FIGURE 16 — OPEN-LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY

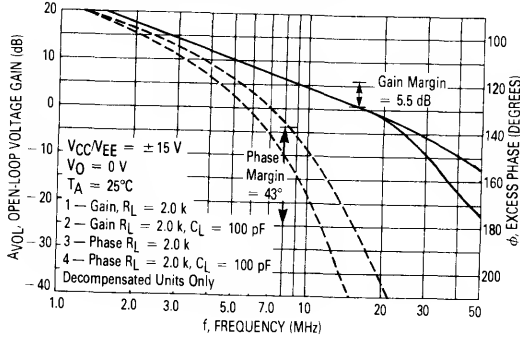


FIGURE 17 — NORMALIZED GAIN BANDWIDTH PRODUCT versus TEMPERATURE

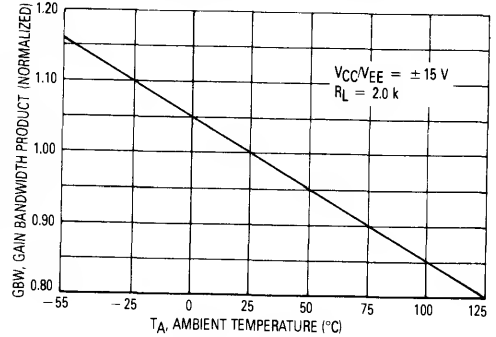


FIGURE 18 — PERCENT OVERSHOOT versus LOAD CAPACITANCE

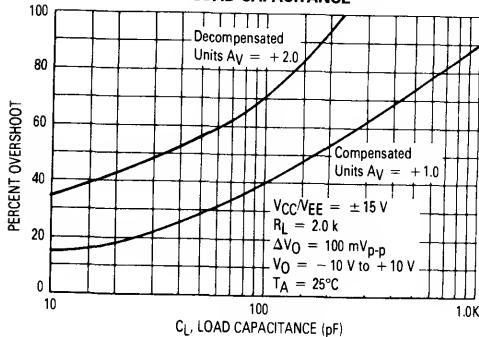


FIGURE 19 — PHASE MARGIN versus LOAD CAPACITANCE

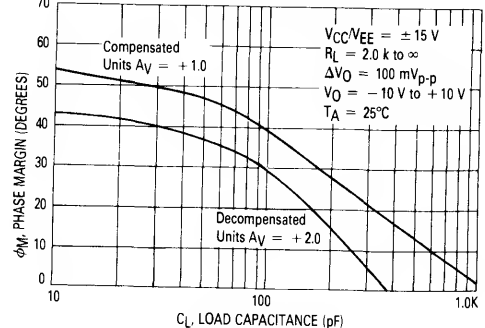


FIGURE 20 — GAIN MARGIN versus LOAD CAPACITANCE

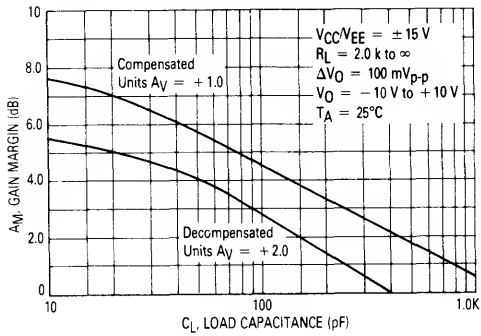


FIGURE 21 — PHASE MARGIN versus TEMPERATURE

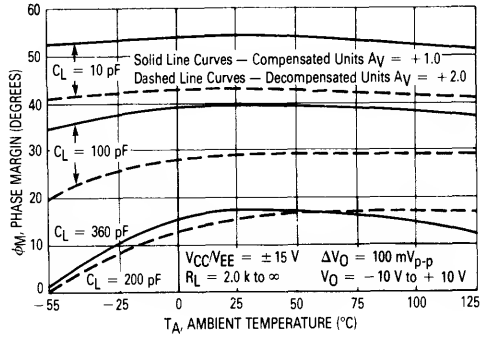


FIGURE 22 — GAIN MARGIN versus TEMPERATURE

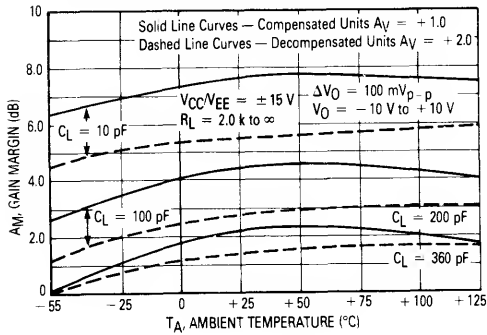
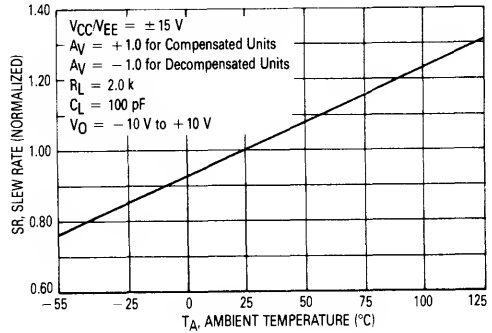


FIGURE 23 — NORMALIZED SLEW RATE versus TEMPERATURE



MC34084 TRANSIENT RESPONSE

$A_V = +1.0$, $R_L = 2.0 \text{ k}$, $V_{CC}/V_{EE} = \pm 15 \text{ V}$, $T_A = 25^\circ\text{C}$

FIGURE 24 — SMALL-SIGNAL

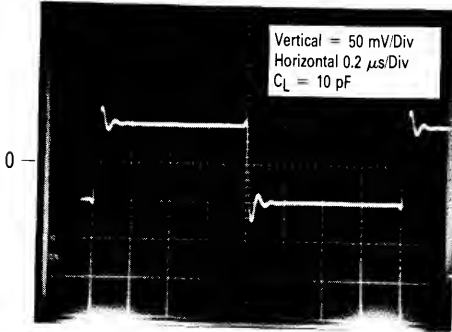
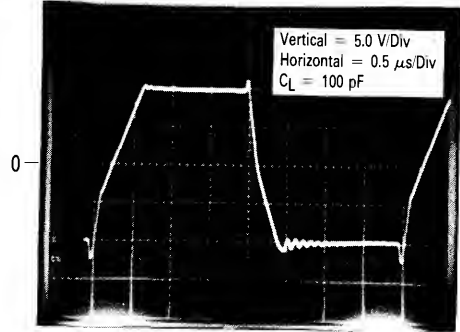


FIGURE 25 — LARGE-SIGNAL



MC34085 TRANSIENT RESPONSE

$A_V = +2.0$, $R_L = 2.0 \text{ k}$, $V_{CC}/V_{EE} = \pm 15 \text{ V}$, $T_A = 25^\circ\text{C}$

FIGURE 26 — SMALL-SIGNAL

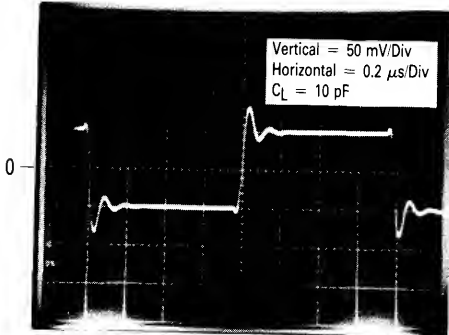


FIGURE 27 — LARGE-SIGNAL

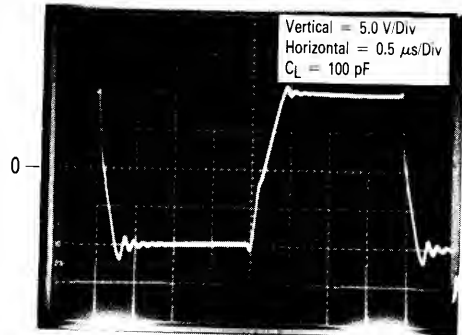


FIGURE 28 — COMMON-MODE REJECTION RATIO
versus FREQUENCY

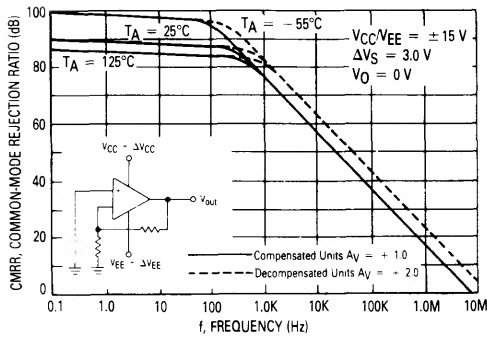


FIGURE 29 — POWER SUPPLY REJECTION RATIO
versus FREQUENCY

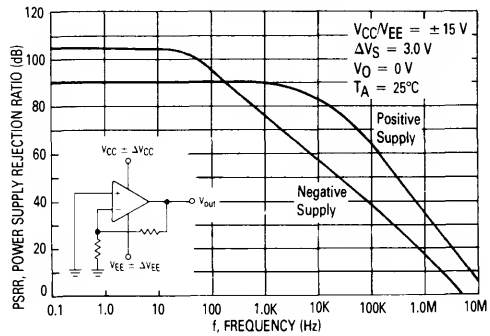


FIGURE 30 — POWER SUPPLY REJECTION RATIO
versus TEMPERATURE

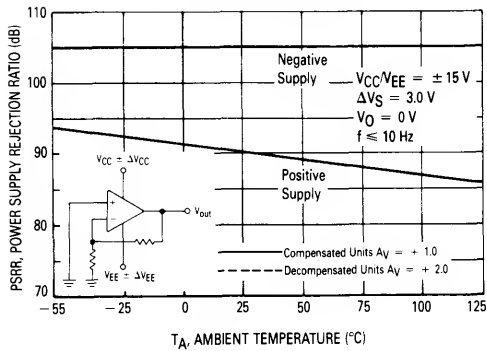


FIGURE 31 — NORMALIZED SUPPLY CURRENT
versus SUPPLY VOLTAGE

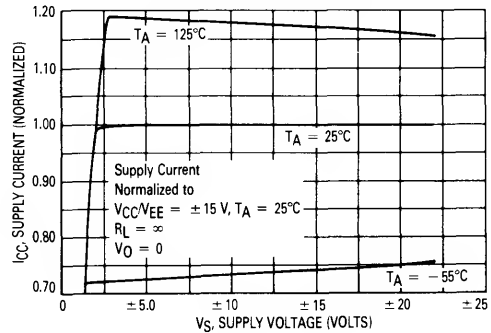


FIGURE 32 — CHANNEL SEPARATION versus FREQUENCY

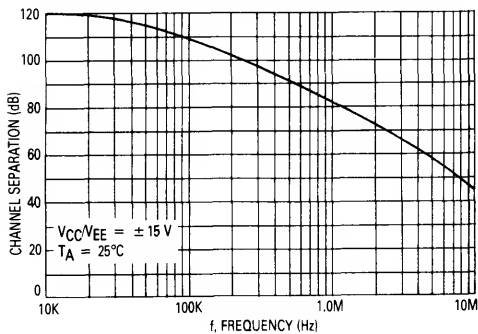
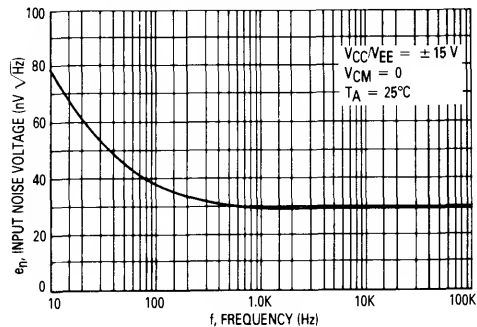


FIGURE 33 — SPECTRAL NOISE DENSITY



APPLICATIONS INFORMATION

The bandwidth and slew rate of the MC34080 series is nearly double that of currently available general purpose JFET op-amps. This improvement in ac performance is due to the P-channel JFET differential input stage driving a compensated miller integration amplifier in conjunction with an all NPN output stage.

The all NPN output stage offers unique advantages over the more conventional NPN/PNP transistor Class AB output stage. With a 10 k load resistance, the op-amp can typically swing within 1.0 V of the positive rail (V_{CC}), and within 0.3 volts of the negative rail (V_{EE}), providing a 28.7 Vp-p swing from ± 15 volt supplies. This large output swing becomes most noticeable at lower supply voltages. If the load resistance is referenced to V_{CC} instead of ground, the maximum possible output swing can be achieved for a given supply voltage. For light load currents, the load resistance will pull the output to V_{CC} during the positive swing and the NPN output transistor will pull the output very near V_{EE} during the negative swing. The load resistance value should be much less than that of the feedback resistance to maximize pull-up capability.

The all NPN transistor output stage is also inherently fast, contributing to the operational amplifier's high gain-bandwidth product and fast settling time. The associated high frequency output impedance is 50 ohms (typical) at 8.0 MHz. This allows driving capacitive loads from 0 to 300 pF without oscillations over the military temperature range, and over the full range of output swing. The 55° phase margin and 7.6 dB gain margin as well as the general gain and phase characteristics are virtually independent of the sink/source output swing conditions. The high frequency characteristics of the MC34080 series is especially useful for active filter applications.

The common mode input range is from 2.0 volts below the positive rail (V_{CC}) to 4.0 volts above the neg-

ative rail (V_{EE}). The amplifier remains active if the inputs are biased at the positive rail. This may be useful for some applications in that single supply operation is possible with a single negative supply. However, a degradation of offset voltage and voltage gain may result.

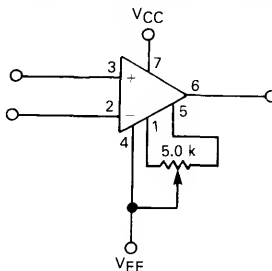
Phase reversal does not occur if either the inverting or noninverting input (or both) exceeds the positive common mode limit. If either input (or both) exceeds the negative common mode limit, the output will be in the high state. The input stage also allows a differential up to ± 44 volts, provided the maximum input voltage range is not exceeded. The supply voltage operating range is from ± 5.0 V to ± 22 V.

For optimum frequency performance and stability careful component placement and printed circuit board layout should be exercised. For example, long unshielded input or output leads may result in unwanted input-output coupling. In order to reduce the input capacitance, resistors connected to the input pins should be physically close to these pins. This not only minimizes the input pole for optimum frequency response, but also minimizes extraneous "pickup" at this node.

Supply decoupling with adequate capacitance close to the supply pin is also important, particularly over temperature, since many types of decoupling capacitors exhibit large impedance changes over temperature.

Primarily due to the JFET inputs of the op amp, the input offset voltage may change due to temperature cycling and board soldering. After 20 temperature cycles (-55°C to 165°C), the typical standard deviation for input offset voltage is 559 μV and 473 μV in the plastic and ceramic packages respectively. With respect to board soldering (260°C , 10 seconds) the typical standard deviation for input offset voltage is 525 μV and 227 μV in the plastic and ceramic package respectively. Socketed plastic or ceramic packaged devices should be used over a minimal temperature range for optimum input offset voltage performance.

FIGURE 34 — OFFSET NULLING CIRCUIT



**LOW POWER, HIGH SLEW RATE, WIDE BANDWIDTH,
JFET INPUT OPERATIONAL AMPLIFIERS**

Quality bipolar fabrication with innovative design concepts are employed for the MC33181/2/4, MC34181/2/4, MC35181/2/4 series of monolithic operational amplifiers. This JFET input series of operational amplifiers operate at 210 μ A per amplifier and offer 4.0 MHz of gain bandwidth product and 10 V/ μ s slew rate. Precision matching and an innovative trim technique of the single and dual versions provide low input offset voltages. With a JFET input stage, this series exhibits high input resistance, low input offset voltage and high gain. The all NPN output stage, characterized by no deadband crossover distortion and large output voltage swing, provides high capacitance drive capability, excellent phase and gain margins, low open-loop high frequency output impedance and symmetrical source/sink ac frequency response.

The MC33181/2/4, MC34181/2/4, MC35181/2/4 series of devices are specified over the commercial, industrial/vehicular or military temperature ranges. The complete series of single, dual and quad operational amplifiers are available in the plastic and ceramic DIP as well as the SOIC surface mount packages.

- Low Supply Current: 210 μ A (Per Amplifier)
- Wide Supply Operating Range: ± 1.5 V to ± 18 V
- Wide Bandwidth: 4.0 MHz
- High Slew Rate: 10 V/ μ s
- Low Input Offset Voltage: 2.0 mV
- Large Output Voltage Swing: -14 V to $+14$ V (with ± 15 V Supplies)
- Large Capacitance Drive Capability: 0 to 500 pF
- Low Total Harmonic Distortion: 0.04%
- Excellent Phase Margin: 67°
- Excellent Gain Margin: 6.7 dB
- Output Short Circuit Protection

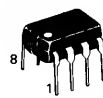
ORDERING INFORMATION

Op Amp Function	Device	Test Temperature Range	Package
Single	MC34181P MC34181D	0 to $+70^\circ\text{C}$	Plastic DIP SO-8
	MC33181P MC33181D	-40 to $+85^\circ\text{C}$	Plastic DIP SO-8
	MC35181U	-55 to $+125^\circ\text{C}$	Ceramic DIP
Dual	MC34182P MC34182D	0 to $+70^\circ\text{C}$	Plastic DIP SO-8
	MC33182P MC33182D	-40 to $+85^\circ\text{C}$	Plastic DIP SO-8
	MC35182U	-55 to $+125^\circ\text{C}$	Ceramic DIP
Quad	MC34184P MC34184D	0 to $+70^\circ\text{C}$	Plastic DIP SO-14
	MC33184P MC33184D	-40 to $+85^\circ\text{C}$	Plastic DIP SO-14
	MC35184L	-55 to $+125^\circ\text{C}$	Ceramic DIP

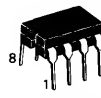
MC34181,2,4
MC35181,2,4
MC33181,2,4

**LOW POWER
JFET INPUT
OPERATIONAL AMPLIFIERS**

**SILICON MONOLITHIC
INTEGRATED CIRCUITS**



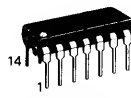
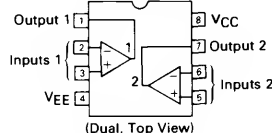
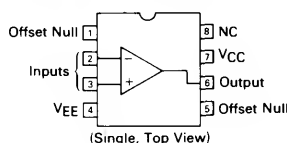
P SUFFIX
PLASTIC PACKAGE
CASE 626



U SUFFIX
CERAMIC PACKAGE
CASE 693



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)



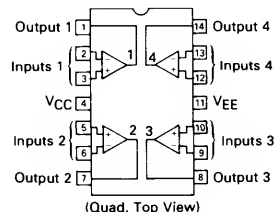
P SUFFIX
PLASTIC PACKAGE
CASE 646



L SUFFIX
CERAMIC PACKAGE
CASE 632



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)



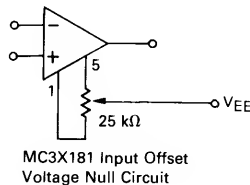
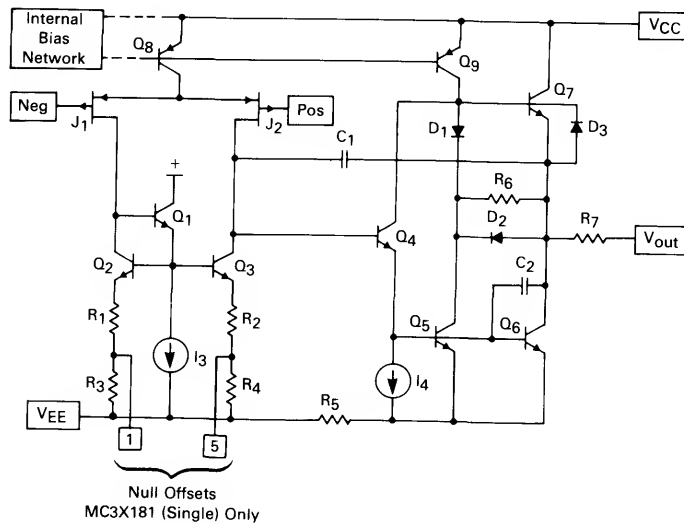
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (from V_{CC} to V_{EE})	V_S	+36	Volts
Input Differential Voltage Range	V_{IDR}	Note 1	Volts
Input Voltage Range	V_{IR}	Note 1	Volts
Output Short-Circuit Duration (Note 2)	t_S	Indefinite	Seconds
Operating Junction Temperature	T_J		$^{\circ}\text{C}$
Ceramic Package		+160	
Plastic Package		+150	
Storage Temperature Range	T_{stg}		$^{\circ}\text{C}$
Ceramic Package		-65 to +160	
Plastic Package		-60 to +150	

NOTES:

1. Either or both input voltages must not exceed the magnitude of V_{CC} or V_{EE} .
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (see Figure 1).

EQUIVALENT CIRCUIT SCHEMATIC (EACH AMPLIFIER)



MC34181,2,4, MC35181,2,4, MC33181,2,4

2

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S = 50\ \Omega$, $V_O = 0\text{ V}$)	V_{IO}				mV
Single					
$T_A = +25^\circ\text{C}$		—	0.5	2.0	
$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ (MC34181)		—	—	3.0	
$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ (MC33181)		—	—	3.5	
$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ (MC35181)		—	—	4.5	
Dual					
$T_A = +25^\circ\text{C}$		—	1.0	3.0	
$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ (MC34182)		—	—	4.0	
$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ (MC33182)		—	—	4.5	
$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ (MC35182)		—	—	5.5	
Quad					
$T_A = +25^\circ\text{C}$		—	4.0	10	
$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ (MC34184)		—	—	11	
$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ (MC33184)		—	—	11.5	
$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ (MC35184)		—	—	12.5	
Average Temperature Coefficient of V_{IO} ($R_S = 50\ \Omega$, $V_O = 0\text{ V}$)	$\Delta V_{IO}/\Delta T$	—	10	—	$\mu\text{V}/^\circ\text{C}$
Input Offset Current ($V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$)	I_{IO}				nA
$T_A = +25^\circ\text{C}$		—	0.001	0.05	
$T_A = 0^\circ\text{C to } +70^\circ\text{C}$		—	—	1.0	
$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		—	—	2.0	
$T_A = -55^\circ\text{C to } +125^\circ\text{C}$		—	—	13	
Input Bias Current ($V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$)	I_{IB}				nA
$T_A = +25^\circ\text{C}$		—	0.003	0.1	
$T_A = 0^\circ\text{C to } +70^\circ\text{C}$		—	—	2.0	
$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		—	—	4.0	
$T_A = -55^\circ\text{C to } +125^\circ\text{C}$		—	—	25	
Input Common Mode Voltage Range	V_{ICR}	($V_{EE} + 4.0\text{ V}$) to ($V_{CC} - 2.0\text{ V}$)			V
Large Signal Voltage Gain ($R_L = 10\text{ k}\Omega$, $V_O = \pm 10\text{ V}$)	A_{VOL}				V/mV
$T_A = +25^\circ\text{C}$		25	60	—	
$T_A = T_{low}\text{ to } T_{high}$		15	—	—	
Output Voltage Swing ($V_{ID} = 1.0\text{ V}$, $R_L = 10\text{ k}\Omega$)	V_{O+} V_{O-}	+13.5 —	+14 -14	— -13.5	V
Common Mode Rejection ($R_S = 50\ \Omega$, $V_{CM} = V_{ICR}$, $V_O = 0\text{ V}$)	CMR	70	86	—	dB
Power Supply Rejection ($R_S = 50\ \Omega$, $V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$)	PSR	70	84	—	dB
Output Short Circuit Current ($V_{ID} = 1.0\text{ V}$, Output to Ground)	I_{SC}				mA
Source		3.0	8.0	—	
Sink		8.0	11	—	
Power Supply Current (No Load, $V_O = 0\text{ V}$)	I_D				μA
Single					
$T_A = +25^\circ\text{C}$		—	210	250	
$T_A = T_{low}\text{ to } T_{high}$		—	—	250	
Dual					
$T_A = +25^\circ\text{C}$		—	420	500	
$T_A = T_{low}\text{ to } T_{high}$		—	—	500	
Quad					
$T_A = +25^\circ\text{C}$		—	840	1000	
$T_A = T_{low}\text{ to } T_{high}$		—	—	1000	

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = +25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Slew Rate ($V_{in} = -10\text{ V to } +10\text{ V}$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$) $A_V = +1.0$ $A_V = -1.0$	SR	7.0 —	10 10	— —	$\text{V}/\mu\text{s}$
Settling Time ($A_V = -1.0$, $R_L = 10\text{ k}\Omega$, $V_O = 0\text{ V to } +10\text{ V Step}$) To Within 0.10% To Within 0.01%	t_s	— —	1.1 1.5	— —	μs
Gain Bandwidth Product ($f = 100\text{ kHz}$)	GBW	3.0	4.0	—	MHz
Power Bandwidth ($A_V = +1.0$, $R_L = 10\text{ k}\Omega$, $V_O = 20\text{ V}_{p-p}$, THD = 5%)	BW_p	—	200	—	kHz
Phase Margin ($-10\text{ V} < V_O < +10\text{ V}$) $R_L = 10\text{ k}\Omega$ $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$	ϕ_m	— —	67 34	— —	Degrees
Gain Margin ($-10\text{ V} < V_O < +10\text{ V}$) $R_L = 10\text{ k}\Omega$ $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$	A_m	— —	6.7 3.4	— —	dB
Equivalent Input Noise Voltage $R_S = 100\text{ }\Omega$, $f = 1.0\text{ kHz}$	e_n	—	38	—	$\text{nV}/\sqrt{\text{Hz}}$
Equivalent Input Noise Current $f = 1.0\text{ kHz}$	i_n	—	0.01	—	$\text{pA}/\sqrt{\text{Hz}}$
Differential Input Capacitance	C_i	—	3.0	—	pF
Differential Input Resistance	R_i	—	10^{12}	—	Ω
Total Harmonic Distortion $A_V = 10$, $R_L = 10\text{ k}\Omega$, $2\text{ V}_{p-p} < V_O < 20\text{ V}_{p-p}$, $f = 10\text{ kHz}$	THD	—	0.04	—	%
Channel Separation ($R_L = 10\text{ k}\Omega$, $-10\text{ V} < V_O < +10\text{ V}$, $0\text{ Hz} < f < 10\text{ kHz}$)	—	—	120	—	dB
Open-Loop Output Impedance ($f = 1.0\text{ MHz}$)	$ Z_O $	—	200	—	Ω

FIGURE 1 — MAXIMUM POWER DISSIPATION versus TEMPERATURE FOR PACKAGE VARIATIONS

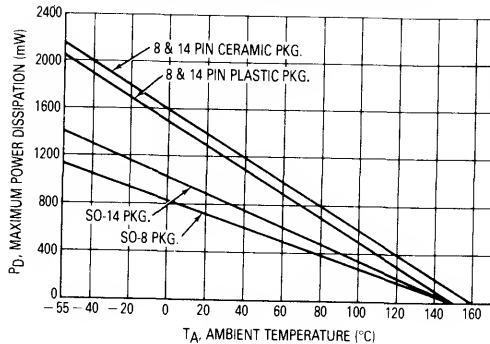


FIGURE 2 — INPUT COMMON-MODE VOLTAGE RANGE versus TEMPERATURE

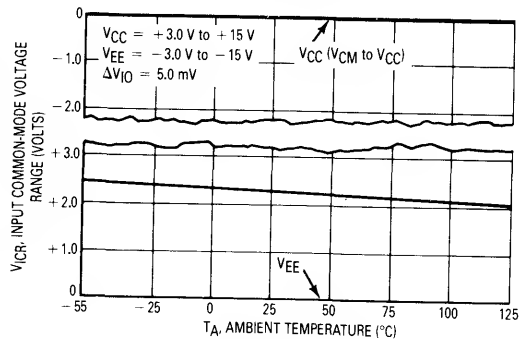


FIGURE 3 — INPUT BIAS CURRENT
versus TEMPERATURE

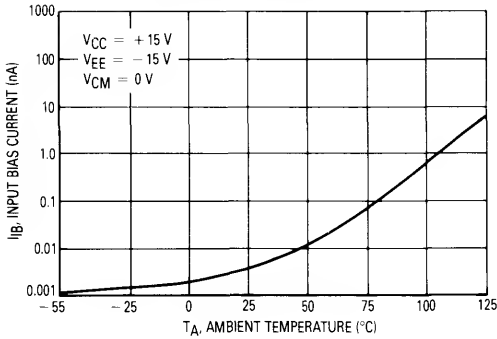


FIGURE 4 — INPUT BIAS CURRENT versus INPUT
COMMON-MODE VOLTAGE

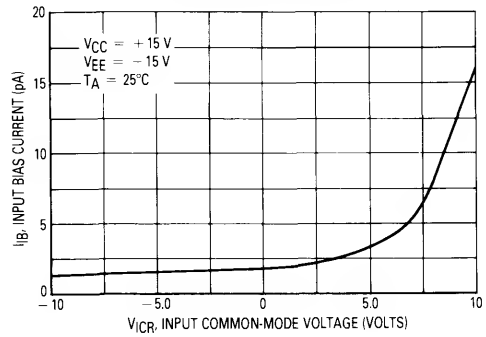


FIGURE 5 — OUTPUT VOLTAGE SWING
versus SUPPLY VOLTAGE

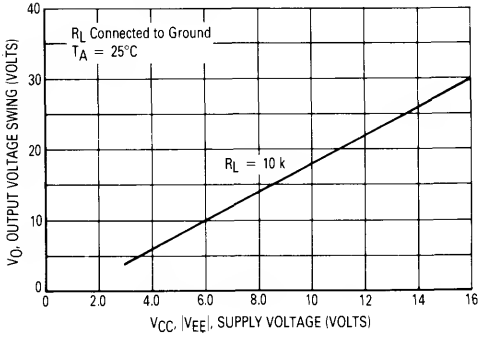


FIGURE 6 — OUTPUT SATURATION VOLTAGE versus
LOAD CURRENT

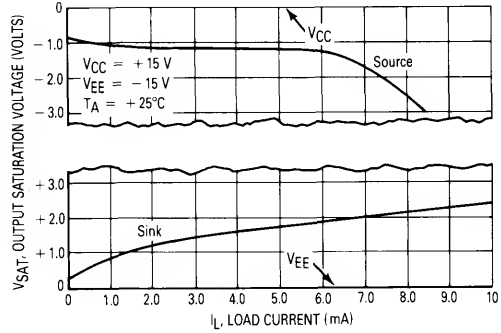


FIGURE 7 — OUTPUT SATURATION VOLTAGE versus
LOAD RESISTANCE TO GROUND

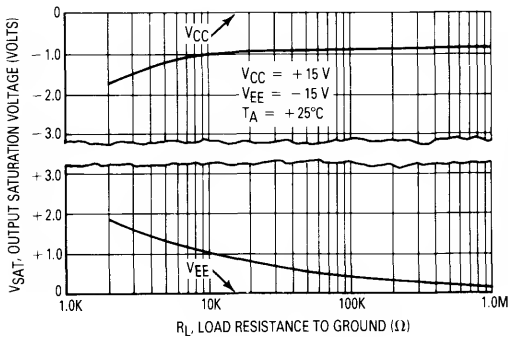


FIGURE 8 — OUTPUT SATURATION VOLTAGE versus
LOAD RESISTANCE TO V_{CC}

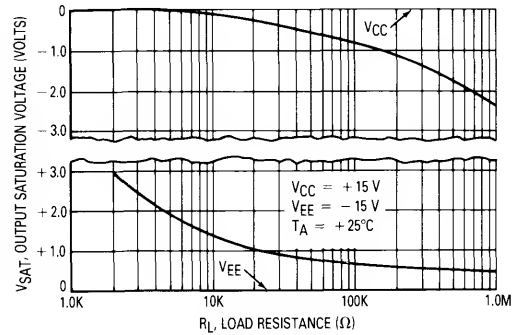


FIGURE 9 — OUTPUT SHORT CIRCUIT CURRENT
versus TEMPERATURE

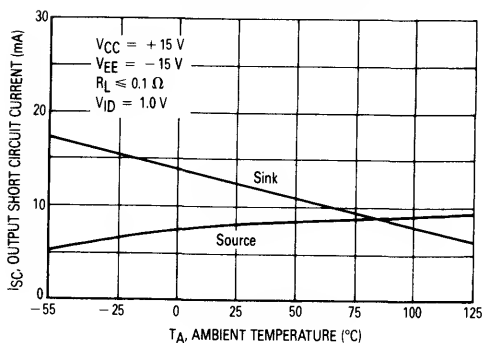


FIGURE 10 — OUTPUT IMPEDANCE versus FREQUENCY

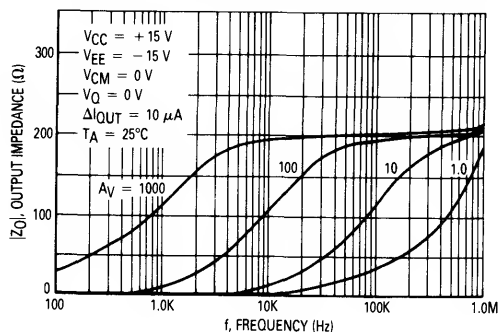


FIGURE 11 — OUTPUT VOLTAGE SWING
versus FREQUENCY

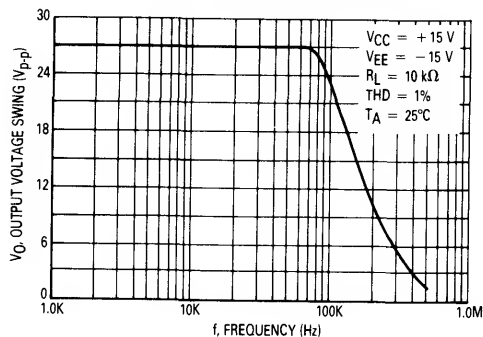


FIGURE 12 — OUTPUT DISTORTION versus FREQUENCY

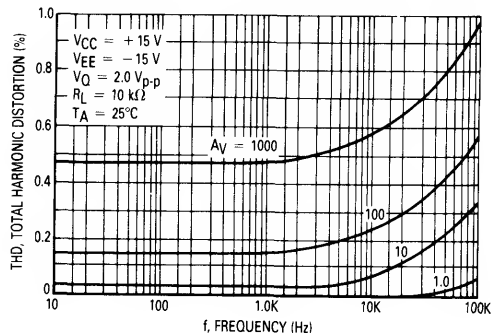


FIGURE 13 — OPEN-LOOP VOLTAGE GAIN
versus TEMPERATURE

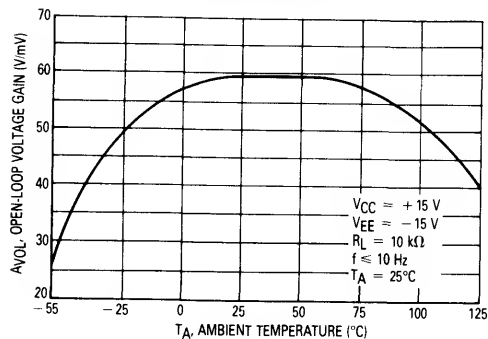


FIGURE 14 — OPEN-LOOP VOLTAGE GAIN AND PHASE
versus FREQUENCY

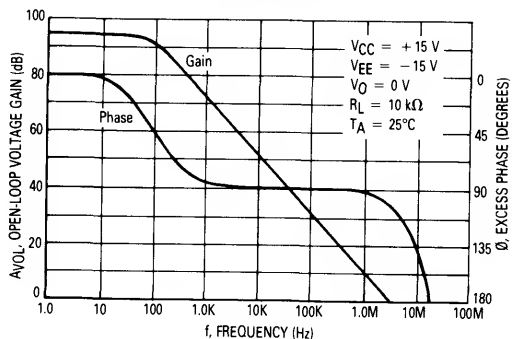


FIGURE 15 — NORMALIZED GAIN BANDWIDTH PRODUCT
versus TEMPERATURE

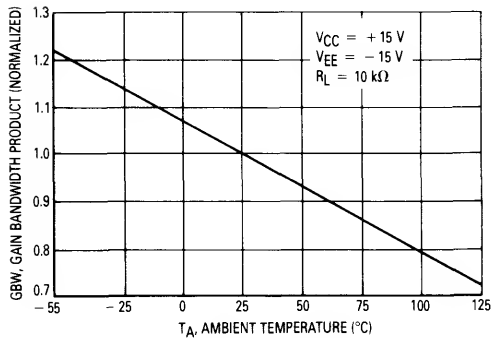


FIGURE 16 — OUTPUT VOLTAGE OVERSHOOT versus
LOAD CAPACITANCE

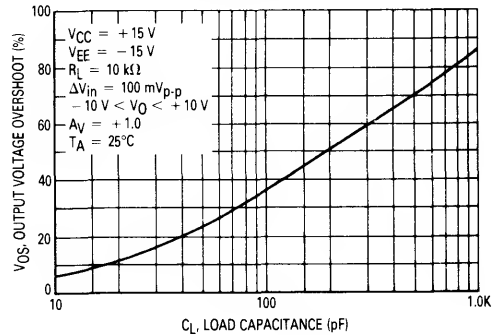


FIGURE 17 — PHASE MARGIN versus LOAD CAPACITANCE

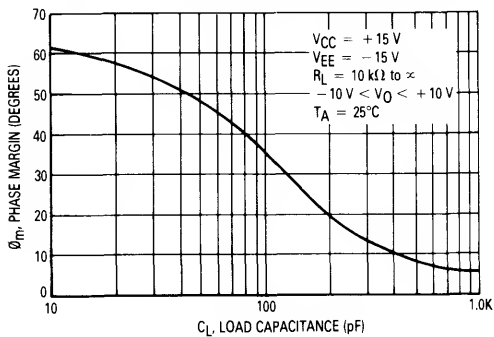


FIGURE 18 — GAIN MARGIN versus LOAD CAPACITANCE

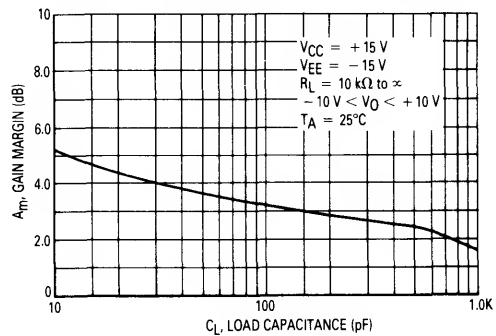


FIGURE 19 — PHASE MARGIN versus TEMPERATURE

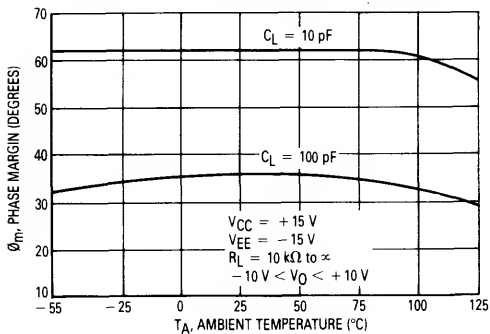


FIGURE 20 — GAIN MARGIN versus TEMPERATURE

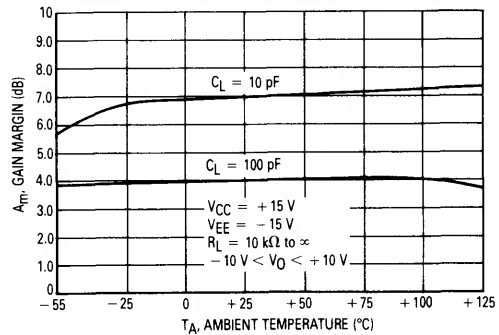


FIGURE 21 — NORMALIZED SLEW RATE
versus TEMPERATURE

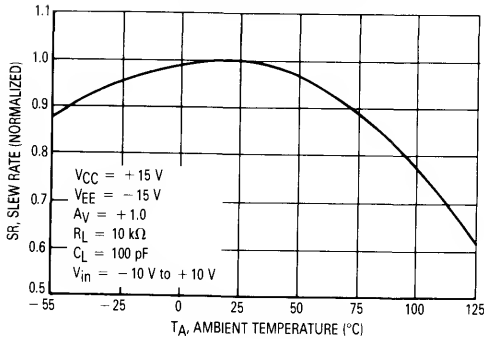


FIGURE 22 — COMMON MODE REJECTION versus
FREQUENCY

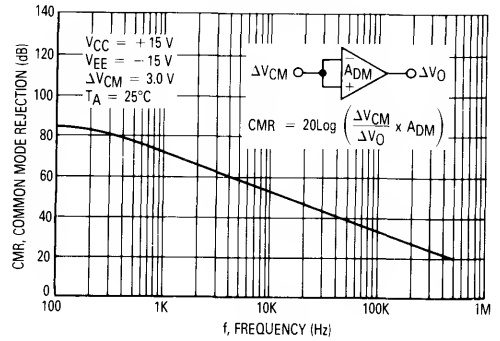


FIGURE 23 — INPUT NOISE VOLTAGE versus FREQUENCY

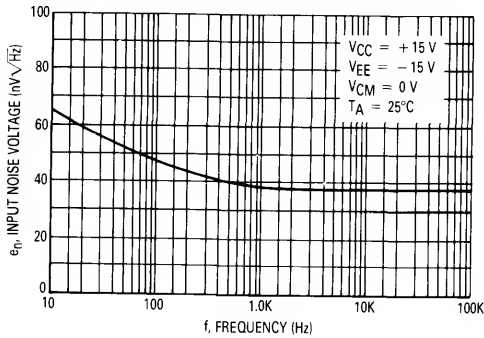


FIGURE 24 — POWER SUPPLY REJECTION
versus TEMPERATURE

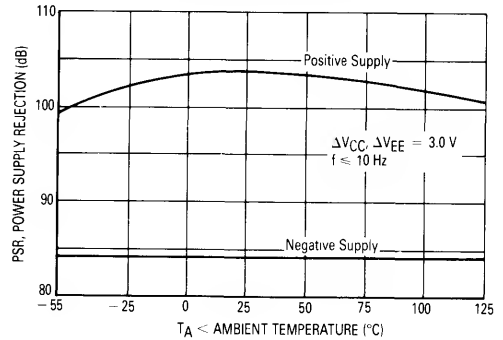


FIGURE 25 — POWER SUPPLY REJECTION
versus FREQUENCY

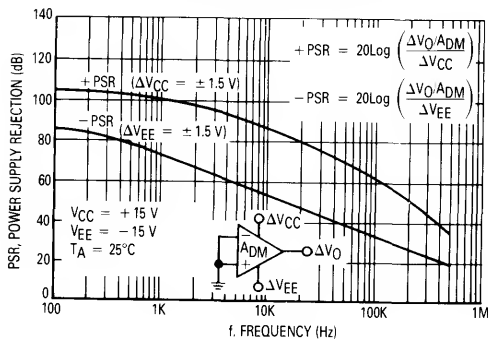
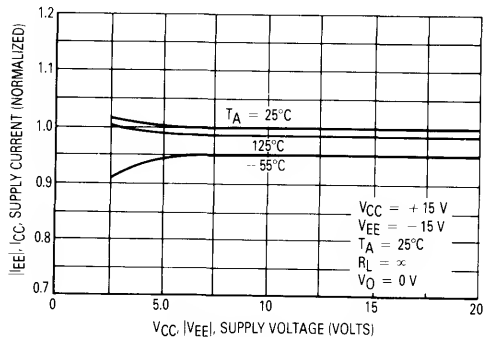


FIGURE 26 — NORMALIZED SUPPLY CURRENT
versus SUPPLY VOLTAGE



MC34181,2,4, MC35181,2,4, MC33181,2,4

FIGURE 27 — CHANNEL SEPARATION versus FREQUENCY

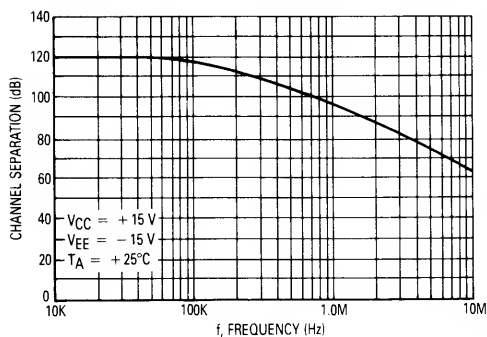


FIGURE 28 — TRANSIENT RESPONSE

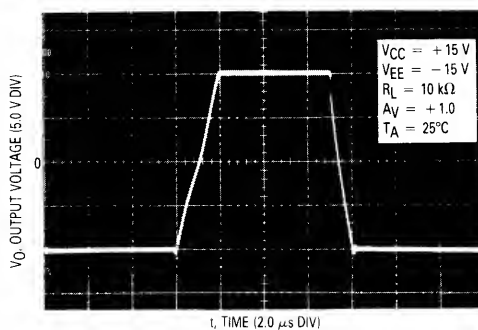
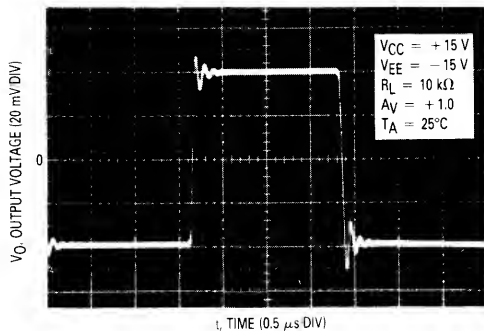


FIGURE 29 — SMALL SIGNAL TRANSIENT RESPONSE



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

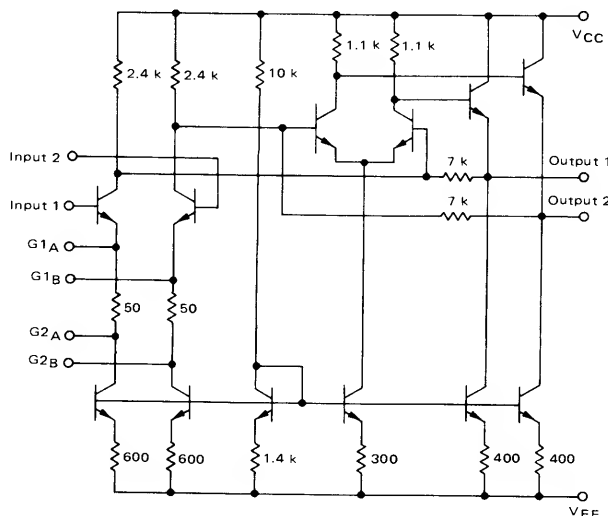
2

DIFFERENTIAL TWO STAGE VIDEO AMPLIFIER

The SE/NE592 is a monolithic, two stage, differential output, wideband video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high pass, low pass, or band pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display and video recorder systems. The 592 is a pin-for-pin replacement for the MC1733.

- 90 MHz Bandwidth
- Adjustable Gains From 0 to 400
- Adjustable Pass Band
- No Frequency Compensation Required

CIRCUIT SCHEMATIC



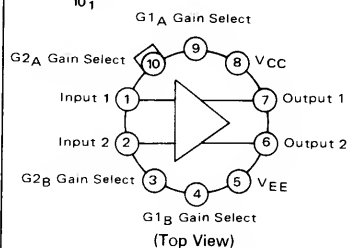
**NE592
SE592**

VIDEO AMPLIFIER

SILICON MONOLITHIC
INTEGRATED CIRCUIT

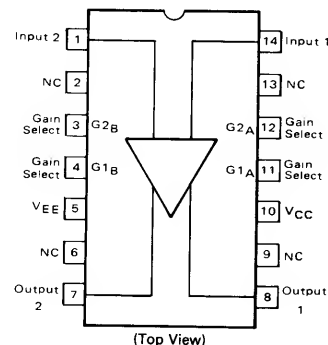


**H SUFFIX
METAL PACKAGE
CASE 603**



**D SUFFIX
PLASTIC PACKAGE
CSE 751A
(SO-14)**

PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
NE592D	0 to 70°C	SO-14
NE592N		Plastic DIP
NE592H	-55 to +125°C	Metal Can
SE592H		Metal Can

NE592, SE592

2

MAXIMUM RATINGS ($T_A = +25^{\circ}\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+8.0 -8.0	Volts
Differential Input Voltages	V_{ID}	± 5.0	Volts
Common-Mode Input Voltage	V_{IC}	± 6.0	Volts
Output Current	I_O	10	mA
Operating Ambient Temperature Range SE592 NE592	T_A	-55 to +125 0 to +70	$^{\circ}\text{C}$
Operating Junction Temperature Range Metal and Ceramic Packages Plastic Package	T_J	175 150	$^{\circ}\text{C}$
Storage Temperature Range Metal and Ceramic Packages Plastic Package	T_{stg}	-65 to +150 -55 to +125	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS $T_A = 25^{\circ}\text{C}$ unless otherwise noted. ($V_{CC} = +6.0\text{ V}$, $V_{EE} = -6.0\text{ V}$, $V_{CM} = 0$)

Characteristic	Symbol	SE592			NE592			Units
		Min	Typ	Max	Min	Typ	Max	
Differential Voltage Gain — Figure 3 ($R_L = 2\text{ k}\Omega$, $e_{out} = 3\text{ Vp-p}$) (Gain 1, Note 1) (Gain 2, Note 2)	A_{vd}	300 90	400 100	500 110	250 80	400 100	600 120	V/V
Bandwidth — Figure 3 (Gain 1, Note 1) (Gain 1, Note 2)	BW	— —	40 90	— —	— —	40 90	— —	MHz
Rise Time — Figure 3 (Gain 1, $e_{out} = 1\text{ Vp-p}$, Note 1) (Gain 2, $e_{out} = 1\text{ Vp-p}$, Note 2)	t_{TLH} t_{THL}	— —	10.5 4.5	— 10	— —	10.5 4.5	— 12	ns
Propagation Delay — Figure 3 (Gain 1, $e_{out} = 1\text{ Vp-p}$, Note 1) (Gain 2, $e_{out} = 1\text{ Vp-p}$, Note 2)	t_{PLH} t_{PHL}	— —	7.5 6.0	— 10	— —	7.5 6.0	— 10	ns
Input Resistance (Gain 1, Note 1) (Gain 2, Note 2)	R_{in}	— 20	4.0 30	— —	— 10	4.0 30	— —	k Ω
Input Capacitance (Gain 2, Note 2)	C_{in}	—	2.0	—	—	2.0	—	pF
Input Offset Current (Gain 3, Note 3) — Fig. 2	I_{IO}	—	0.4	3.0	—	0.4	5.0	μA
Input Bias Current (Gain 3, Note 3) — Fig. 2	I_{IB}	—	9.0	20	—	9.0	30	μA
Input Noise Voltage (Gain 1 and Gain 2) (BW = 1 kHz to 10 MHz) — Figure 1	V_n	—	12	—	—	12	—	$\mu\text{V(rms)}$
Input Voltage Range (Gain 2, Note 2) — Fig. 3	V_{in}	± 1.0	—	—	± 1.0	—	—	V
Common-Mode Rejection Ratio — Figure 3 (Gain 2, $V_{CM} = \pm 1\text{ V}$, $f \leq 100\text{ kHz}$) (Gain 2, $V_{CM} = \pm 1\text{ V}$, $f = 5\text{ MHz}$)	CMRR	60 —	86 60	— —	60 —	86 60	— —	dB
Supply Voltage Rejection Ratio — Figure 2 (Gain 2, $\Delta V_S = \pm 0.5\text{ V}$)	PSRR	50	70	—	50	70	—	dB
Output Offset Voltage — Figure 2 (Gain 3, $R_L = \infty$, Note 3)	V_{OO}	—	0.35	0.75	—	0.35	0.75	V
Output Common-Mode Voltage — Figure 2 ($R_L = \infty$, Gain 3, Note 3)	V_{CMO}	2.4	2.9	3.4	2.4	2.9	3.4	V
Output Voltage Swing — Figure 3 ($R_L = 2\text{ k}\Omega$, Gain 2, Note 2)	V_O	3.0	4.0	—	3.0	4.0	—	Vp-p
Output Resistance	r_o	—	20	—	—	20	—	Ω
Power Supply Current — Figure 2 ($R_L = \infty$, Gain 2, Note 2)	I_D	—	18	24	—	18	24	mA

Note 1. Gain select pins $G1_A$ and $G1_B$ connected together.

Note 2. Gain select pins $G2_A$ and $G2_B$ connected together.

Note 3. All gain select pins open.

NE592, SE592

ELECTRICAL CHARACTERISTICS $T_A = T_{\text{High}}$ to T_{Low} unless otherwise noted.* ($V_{CC} = +6.0 \text{ Vdc}$, $V_{EE} = -6.0 \text{ Vdc}$, $V_{CM} = 0$)

Characteristic	Symbol	SE592			NE592			Units
		Min	Typ	Max	Min	Typ	Max	
Differential Voltage Gain — Figure 3 ($R_L = 2 \text{ k}\Omega$, $e_{\text{out}} = 3 \text{ Vp-p}$) (Gain 1, Note 1) (Gain 2, Note 2)	A_{vd}	200 80	— —	600 120	250 80	— —	600 120	V/V
Input Resistance (Gain 2)	R_{in}	8.0	—	—	8.0	—	—	$\text{k}\Omega$
Input Offset Current (Gain 3) — Figure 2	I_{IO}	—	—	5.0	—	—	6.0	μA
Input Bias Current (Gain 3) — Figure 2	I_{IB}	—	—	40	—	—	40	μA
Input Voltage Range (Gain 2) — Figure 3	V_{in}	± 1.0	—	—	± 1.0	—	—	V
Common-Mode Rejection Ratio — Figure 3 (Gain 2, $V_{CM} = \pm 1 \text{ V}$, $f \leq 100 \text{ kHz}$)	CMRR	50	—	—	50	—	—	dB
Supply Voltage Rejection Ratio — Figure 2 (Gain 2, $\Delta V_S = \pm 0.5 \text{ V}$)	PSRR	50	—	—	50	—	—	dB
Output Offset Voltage (Gain 3) — Figure 2	V_{OO}	—	—	1.2	—	—	1.5	V
Output Voltage Swing (Gain 2) — Figure 3	V_O	2.5	—	—	2.5	—	—	Vp-p
Power Supply Current (Gain 2) — Figure 2	I_D	—	—	27	—	—	27	mA

* $T_{\text{Low}} = 0^\circ\text{C}$ for NE592, -55°C for SE592

$T_{\text{High}} = +70^\circ\text{C}$ for NE592, $+125^\circ\text{C}$ for SE592

GENERAL TEST CIRCUITS

FIGURE 1

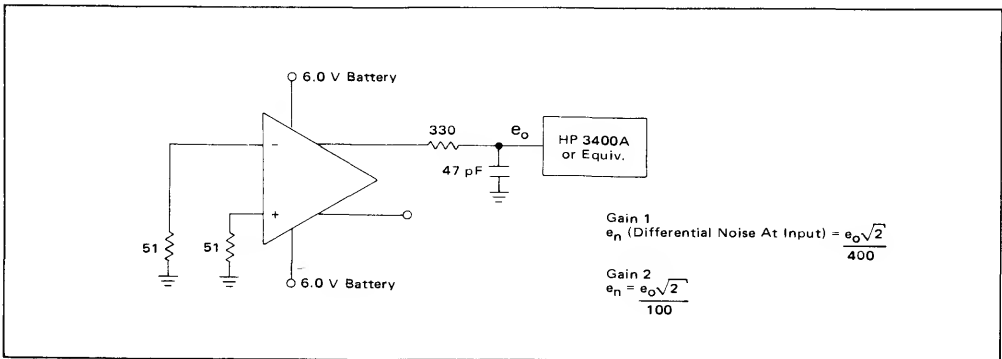


FIGURE 2

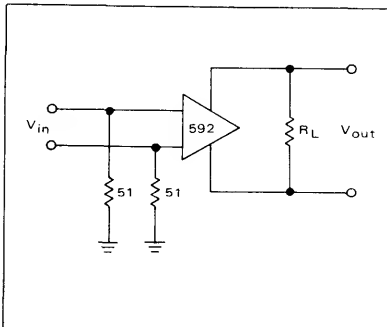


FIGURE 3

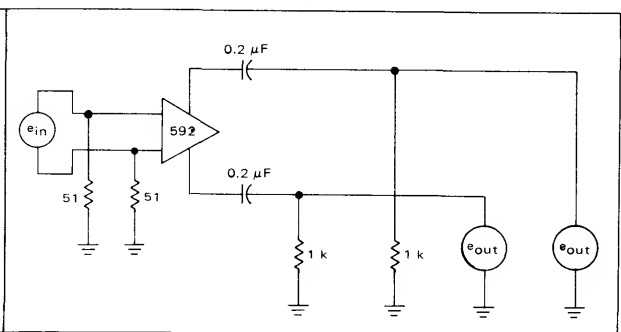


FIGURE 4 – GAIN 1 versus FREQUENCY

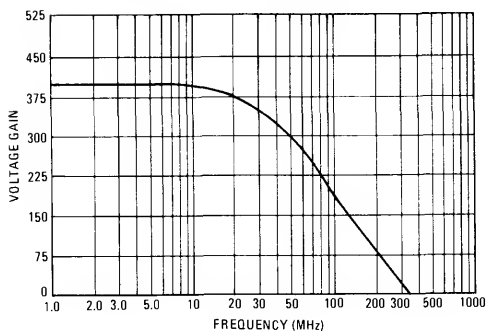


FIGURE 5 – GAIN 2 versus FREQUENCY

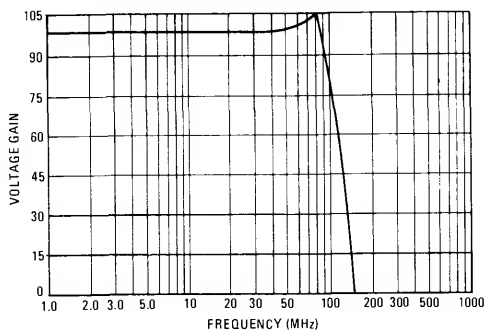


FIGURE 6 – OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY

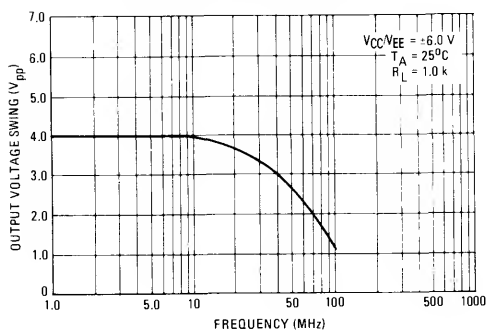


FIGURE 7 – OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

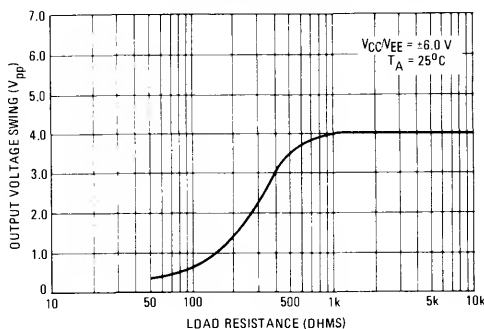
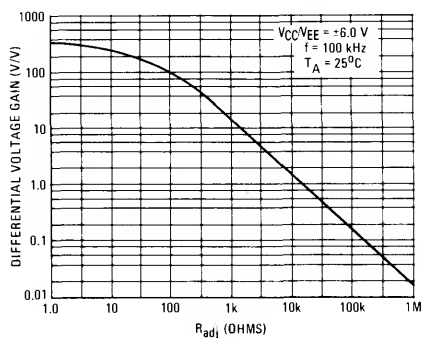
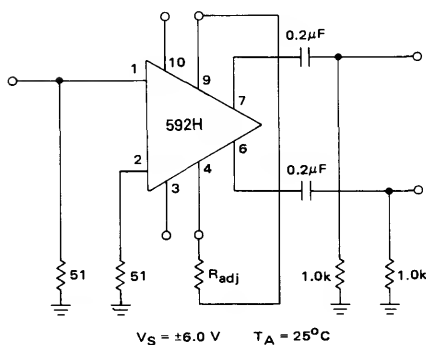


FIGURE 8 – VOLTAGE GAIN AS A FUNCTION OF R_{adj} RESISTANCE



NE592, SE592

FIGURE 9 — DISK/TAPE PHASE MODULATED
READBACK SYSTEMS

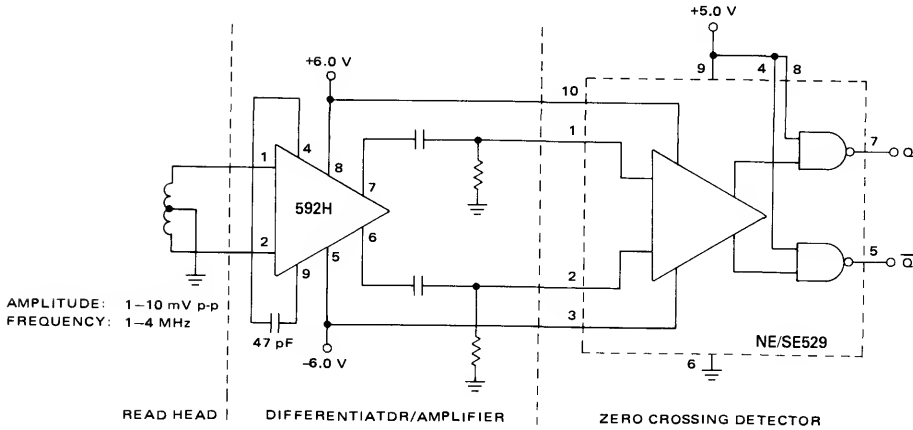


FIGURE 10 — DIFFERENTIATION WITH HIGH COMMON
MODE NOISE REJECTION

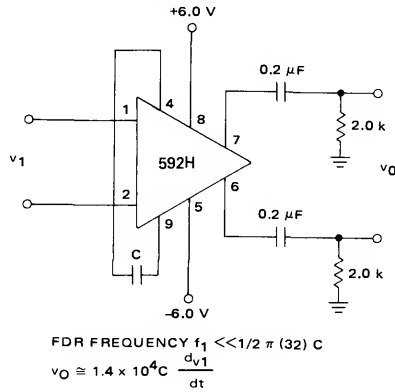
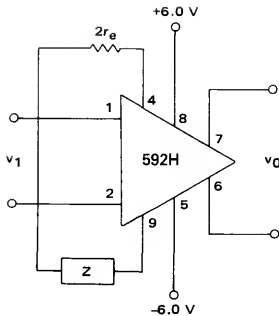


FIGURE 11 — FILTER NETWORKS



BASIC CONFIGURATION		
Z NETWORK	FILTER TYPE	$v_O(s)$ TRANSFER $v_1(s)$ FUNCTION
	Low Pass	$\frac{1.4 \times 10^4}{L} \left[\frac{1}{s + R/L} \right]$
	High Pass	$\frac{1.4 \times 10^4}{R} \left[\frac{s}{s + 1/RC} \right]$
	Band Pass	$\frac{1.4 \times 10^4}{L} \left[\frac{s}{s^2 + R/L s + 1/LC} \right]$
	Band Reject	$\frac{1.4 \times 10^4}{R} \left[\frac{s^2 + 1/LC}{s^2 + 1/LC + s/RC} \right]$

NOTE:
In the networks above, the R value used is assumed to include $2r_e$, or approximately 30 Ohms.

OP-27

2

ULTRA-LOW NOISE PRECISION, HIGH SPEED OPERATIONAL AMPLIFIER

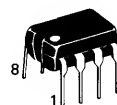
The OP-27 series of monolithic operational amplifiers combine low-noise, precision dc performance and high bandwidth in one device. Advanced Bipolar processing and innovative design techniques are used to produce this low noise precision operational amplifier. This device is trimmed for extremely low initial input offset voltage by utilizing a highly stable and reliable zener zap technique during factory testing which yields guaranteed V_{IO} limits as tight as 25 μ V. A unique input bias current cancellation scheme maintains low I_{IB} and I_{IO} to typically ± 20 nA and 15 nA respectively over the full military temperature range. Other sources of input errors are reduced in excess of -120 dB due to extremely high common mode and power supply rejection ratios. The OP-27 has a gain bandwidth product of 8.0 MHz and slew rate of 2.8 V/ μ s.

The precision, low noise and high speed characteristics of this device makes it ideal for amplifying transducer signals, RIAA phono, NAB tape head and microphone preamplifiers, wide band instrumentation amplifiers and high speed signal conditioning for data acquisition systems.

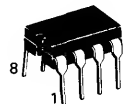
- Extremely Low-Noise — 3.0 nV/ $\sqrt{\text{Hz}}$ at 1.0 kHz
 80 nVp-p, 0.1 Hz to 10 Hz
- Low Initial Input Offset Voltage — 10 μ V
- Ultra Stable Input Offset Voltage — 0.2 μ V/mo.
- High Gain Bandwidth Product and High Slew Rate — 8.0 MHz,
 2.8 V/ μ s
- High Open-Loop Gain — 1.8 Million
- High Common-Mode Rejection — 126 dB

ULTRA-LOW NOISE PRECISION, HIGH SPEED OPERATIONAL AMPLIFIER

**SILICON MONOLITHIC
 INTEGRATED CIRCUIT**



P SUFFIX
 PLASTIC PACKAGE
 CASE 626

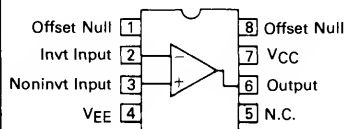


Z SUFFIX
 CERAMIC PACKAGE
 CASE 693

ORDERING INFORMATION

Slew Rate	Device		Temperature Range	Package
	$V_{IO} \leq 60 \mu\text{V}$	$V_{IO} \leq 100 \mu\text{V}$		
$\geq 1.7 \text{ V}/\mu\text{s}$	OP-27BZ	OP-27CZ	-55 to +125°C	Ceramic DIP
	OP-27FZ	OP-27GZ	-25 to +85°C	Ceramic DIP
	OP-27FP	OP-27GP	0 to +70°C	Plastic DIP

PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC} V_{EE}	+22 -22	V
Input Voltage Range (Note 1)	V_{IDR}	± 22	V
Differential Input Voltage (Note 2)	V_{ID}	± 0.7	V
Differential Input Current (Note 2)	I_{ID}	± 25	mA
Output Short-Circuit Duration	t_s	Indefinite	
Power Dissipation and Thermal Characteristics Plastic Package (P Suffix) $T_A = +36^\circ\text{C}$	P_D	500	mW
Derate above $T_A = +75^\circ\text{C}$	$1/R_{\theta JA}$	6.7	mW/ $^\circ\text{C}$
Ceramic Package (Z Suffix) $T_A = +75^\circ\text{C}$	P_D	500	mW
Derate above $T_A = +80^\circ\text{C}$	$1/R_{\theta JA}$	7.1	mW/ $^\circ\text{C}$
Operating Ambient Temperature A, B and C Grades	T_A	-55 to +125	$^\circ\text{C}$
F and G Grades (Ceramic Package)		-25 to +85	
FP and GP Grades (Plastic Package)		0 to +70	
Junction Temperature	T_J	+150	$^\circ\text{C}$
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}	-65 to +150 -65 to +125	$^\circ\text{C}$

NOTES:

- For supply voltages less than ± 22 V, the absolute maximum input voltage range is equal to the supply voltage.
- The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ± 0.7 V, the input current must be limited to 25 mA.

ELECTRICAL CHARACTERISTICS ($V_{CC} = +15$ V, $V_{EE} = -15$ V, $T_A = +25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	OP-27B/F/FP			OP-27C/G/GP			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	—	20	60	—	30	100	μV
Long Term Input Offset Voltage Stability (Note 3)	V_{IO}/t	—	0.3	1.5	—	0.4	2.0	$\mu\text{V}/\text{mo}$
Input Offset Current	I_{IO}	—	9.0	50	—	12	75	nA
Input Bias Current	I_{IB}	—	± 12	± 55	—	± 15	± 80	nA
Input Noise Voltage 0.1 to 10 Hz (Note 4)	e_{np-p}	—	0.08	0.18	—	0.09	0.25	μV_{p-p}
Input Noise Voltage Density (Note 4)	e_n	—	—	—	—	—	—	$\text{nV}/\sqrt{\text{Hz}}$
$f_o = 10$ Hz		—	3.5	5.5	—	3.8	8.0	
$f_o = 30$ Hz		—	3.1	4.5	—	3.3	5.6	
$f_o = 1000$ Hz	—	—	3.0	3.8	—	3.2	4.5	—
Input Noise Current Density (Note 4)	i_n	—	—	—	—	—	—	$\text{pA}/\sqrt{\text{Hz}}$
$f_o = 10$ Hz		—	1.7	4.0	—	1.7	—	
$f_o = 30$ Hz		—	1.0	2.3	—	1.0	—	
$f_o = 1000$ Hz	—	—	0.4	0.6	—	0.4	0.6	—
Input Resistance — Differential Mode	r_i	1.2	5.0	—	0.8	4.0	—	M Ω
Input Resistance — Common Mode	R_{incm}	—	2.5	—	—	2.0	—	G Ω
Input Voltage Range	V_{IR}	± 11	± 12.3	—	± 11	± 12.3	—	V

(continued)

ELECTRICAL CHARACTERISTICS (continued) ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = +25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	OP-27B/F/FP			OP-27C/G/GP			Unit
		Min	Typ	Max	Min	Typ	Max	
Common Mode Rejection Ratio $V_{CM} = \pm 11\text{ V}$	CMRR	106	123	—	100	120	—	dB
Power Supply Rejection Ratio $V_{CC}/V_{EE} = \pm 4.0\text{ V to } \pm 18\text{ V}$	PSRR	100	120	—	94	114	—	dB
Large-Signal Voltage Gain $R_L \geq 2.0\text{ k}\Omega$, $V_O = \pm 10\text{ V}$ $R_L \geq 1.0\text{ k}\Omega$, $V_O = \pm 10\text{ V}$ $R_L = 600\text{ }\Omega$, $V_O = \pm 1.0\text{ V}$, $V_{CC}/V_{EE} = \pm 4.0\text{ V to } \pm 18\text{ V}$	A_{VOL}	1000 800 —	1800 1500 700	— — —	700 — —	1500 1500 500	— — —	V/mV
Output Voltage Swing $R_L \geq 2.0\text{ k}\Omega$ $R_L = 600\text{ }\Omega$	V_O	± 12 ± 10	± 13.8 ± 11.5	— —	± 11.5 ± 10	± 13.5 ± 11.5	— —	V
Slew Rate, $R_L \geq 2.0\text{ k}\Omega$	SR	1.7	2.8	—	1.7	2.8	—	V/ μs
Gain Bandwidth Product	GBW	5.0	8.0	—	5.0	8.0	—	MHz
Open Loop Output Resistance $V_O = 0$, $I_O = 0$	r_o	—	70	—	—	70	—	Ω
Power Dissipation $V_O = 0$, No Load	P_D	—	90	140	—	100	170	mW
Offset Adjustment Range $R_p = 10\text{ k}\Omega$		—	± 4.0	—	—	± 4.0	—	mV

NOTES (continued):

- Long term input offset voltage stability for the OP-27 series, refers to the average trend line of V_{IO} versus time over extended periods after the first 30 days of operation. Excluding the first hour of operation, changes in V_{IO} during the first 30 days are typically $2.5\text{ }\mu\text{V}$.
- Sample tested.

ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = T_{low}\text{ to } T_{high}$ [Note 5])

Characteristic	Symbol	OP-27B			OP-27C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	—	50	200	—	70	300	μV
Average Input Offset Drift (Note 6)	TCV_{IO}	—	0.3	1.3	—	0.4	1.8	$\mu\text{V}/^\circ\text{C}$
Input Offset Current	I_{IO}	—	22	85	—	30	135	nA
Input Bias Current	I_{IB}	—	± 28	± 95	—	± 35	± 150	nA
Input Voltage Range	V_{IR}	± 10.3	± 11.5	—	± 10.2	± 11.5	—	V
Common Mode Rejection Ratio $V_{CM} = \pm 10\text{ V}$	CMRR	100	119	—	94	116	—	dB
Power Supply Rejection Ratio $V_{CC}/V_{EE} = \pm 4.5\text{ V to } \pm 18\text{ V}$	PSRR	94	114	—	86	108	—	dB
Large-Signal Voltage Gain $R_L \geq 2\text{ k}\Omega$, $V_O = \pm 10\text{ V}$	A_{VOL}	500	1000	—	300	800	—	V/mV
Output Voltage Swing $R_L \geq 2\text{ k}\Omega$	V_O	± 11	± 13.2	—	± 10.5	± 13	—	V

NOTES (continued):

- $T_{low} = -55^\circ\text{C}$ for OP-27B
 $\quad\quad\quad$ OP-27C
 $\quad\quad\quad = -25^\circ\text{C}$ for OP-27F
 $\quad\quad\quad$ OP-27G
 $\quad\quad\quad = 0^\circ\text{C}$ for OP-27FP
 $\quad\quad\quad$ OP-27GP
- $T_{high} = +125^\circ\text{C}$ for OP-27B
 $\quad\quad\quad$ OP-27C
 $\quad\quad\quad = +85^\circ\text{C}$ for OP-27F
 $\quad\quad\quad$ OP-27G
 $\quad\quad\quad = +70^\circ\text{C}$ for OP-27FP
 $\quad\quad\quad$ OP-27GP
- TCV_{IO} performance is within specifications unnullled or when nullled with a potentiometer $R_p = 8.0\text{ k}\Omega$ to $20\text{ k}\Omega$.

ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = T_{\text{low}}$ to T_{high} [Note 5])

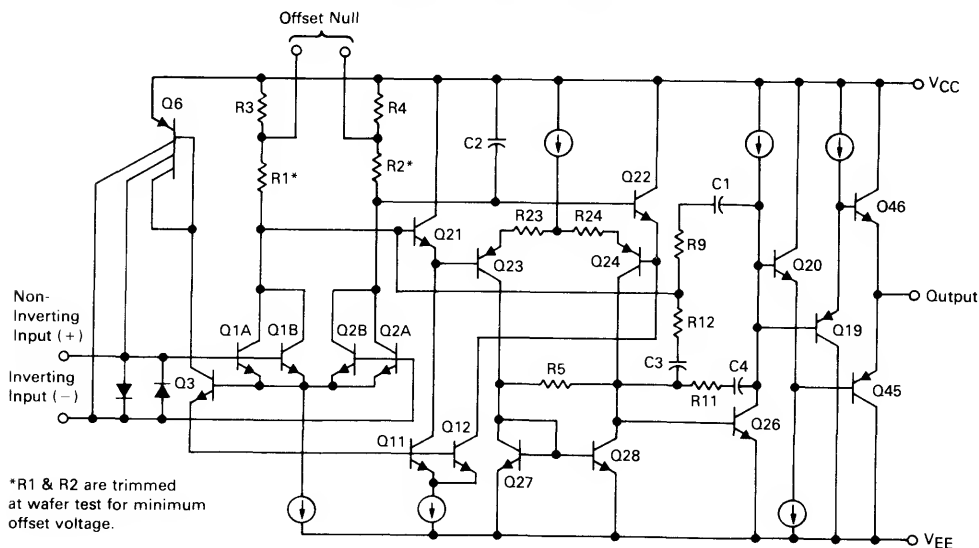
Characteristic	Symbol	OP-27F/FP			OP-27G/GP			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	—	40	140	—	55	220	μV
Average Input Offset Drift (Note 6)	TCV_{IO}	—	0.3	1.3	—	0.4	1.8	$\mu\text{V}/^\circ\text{C}$
Input Offset Current	I_{IQ}	—	14	85	—	20	135	nA
Input Bias Current	I_{IB}	—	± 18	± 95	—	± 25	± 150	nA
Input Voltage Range	V_{IR}	± 10.5	± 11.8	—	± 10.5	± 11.8	—	V
Common Mode Rejection Ratio $V_{CM} = \pm 10\text{ V}$	CMRR	102	121	—	96	118	—	dB
Power Supply Rejection Ratio $V_{CC}/V_{EE} = \pm 4.5\text{ V}$ to $\pm 18\text{ V}$	PSRR	96	114	—	90	114	—	dB
Large-Signal Voltage Gain $R_L \geq 2.0\text{ k}\Omega$, $V_O = \pm 10\text{ V}$	A_{VOL}	700	1300	—	450	1000	—	V/mV
Output Voltage Swing $R_L \geq 2.0\text{ k}\Omega$	V_O	± 11.4	± 13.5	—	± 11	± 13.3	—	V

NOTES (continued):

5. $T_{\text{low}} = -55^\circ\text{C}$ for OP-27B
 OP-27C
 $= -25^\circ\text{C}$ for OP-27F
 OP-27G
 $= 0^\circ\text{C}$ for OP-27FP
 OP-27GP

- $T_{\text{high}} = +125^\circ\text{C}$ for OP-27B
 OP-27C
 $= +85^\circ\text{C}$ for OP-27F
 OP-27G
 $= +70^\circ\text{C}$ for OP-27FP
 OP-27GP

6. TCV_{IO} performance is within specifications unnullled or when nullled with a potentiometer $R_p = 8.0\text{ k}\Omega$ to $20\text{ k}\Omega$.

ABBREVIATED CIRCUIT SCHEMATIC

TYPICAL CHARACTERISTICS

FIGURE 1 — VOLTAGE NOISE TESTER GAIN
versus FREQUENCY

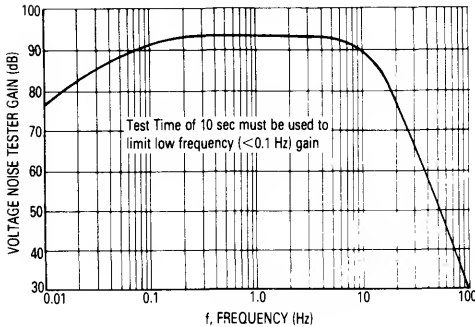
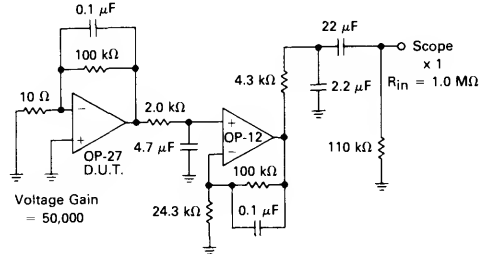


FIGURE 2 — VOLTAGE NOISE TEST CIRCUIT
(0.1 Hz TO 10 Hz)



Note: All capacitor values are for nonpolarized capacitors only.

FIGURE 3 — VOLTAGE NOISE versus FREQUENCY

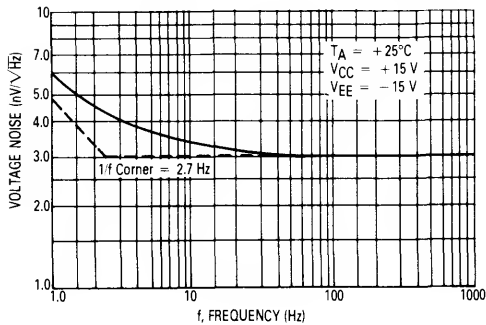


FIGURE 4 — INPUT WIDEBAND VOLTAGE NOISE versus
BANDWIDTH (0.1 Hz TO FREQUENCY INDICATED)

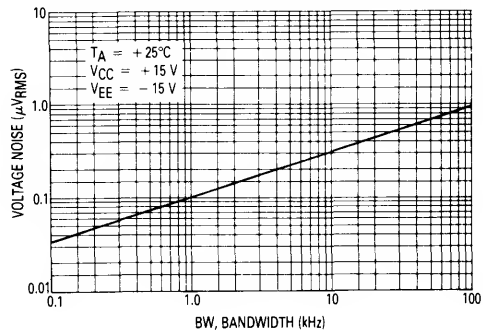


FIGURE 5 — TOTAL NOISE versus SOURCE RESISTANCE

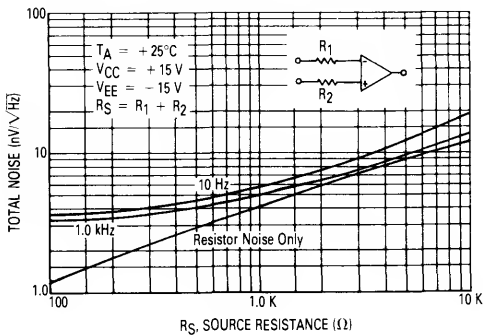


FIGURE 6 — VOLTAGE NOISE versus TEMPERATURE

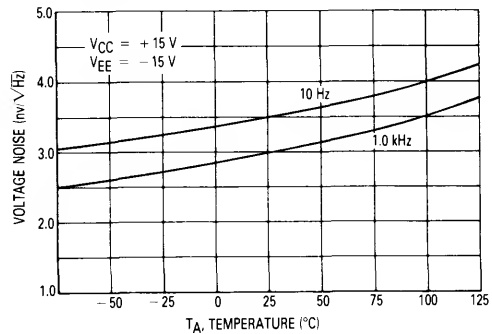


FIGURE 7 — VOLTAGE NOISE versus SUPPLY VOLTAGE

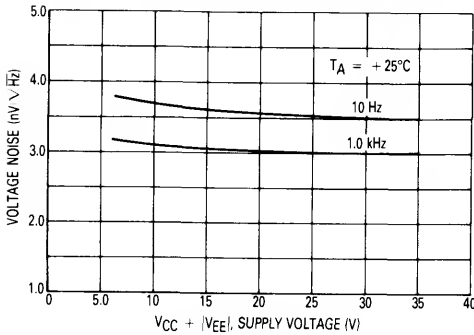


FIGURE 8 — CURRENT NOISE versus FREQUENCY

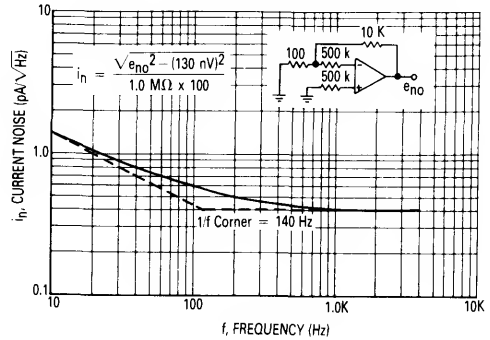


FIGURE 9 — SUPPLY CURRENT versus SUPPLY VOLTAGE

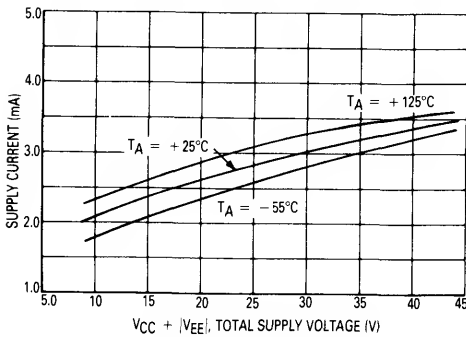


FIGURE 10 — INPUT BIAS CURRENT versus TEMPERATURE

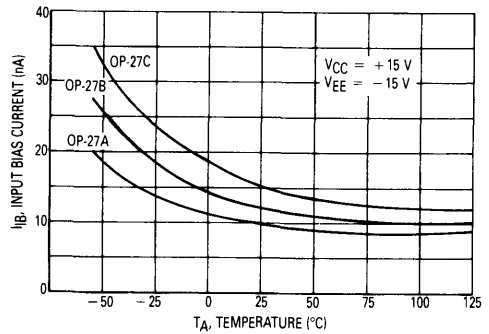


FIGURE 11 — INPUT OFFSET CURRENT versus TEMPERATURE

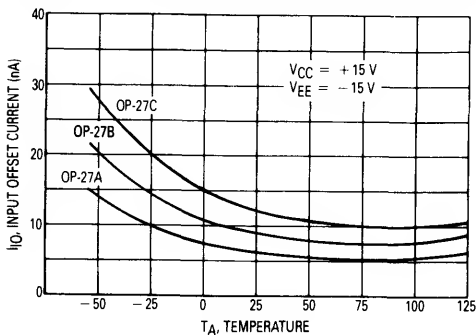


FIGURE 12 — COMMON MODE INPUT RANGE versus SUPPLY VOLTAGE

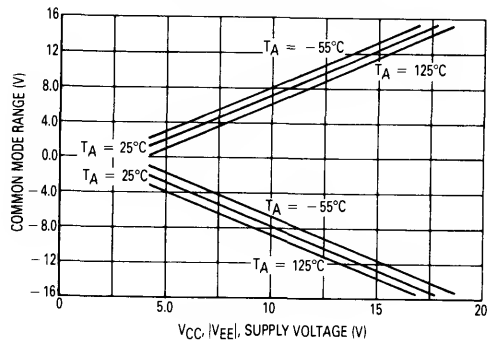


FIGURE 13 — OPEN LOOP VOLTAGE GAIN
versus SUPPLY VOLTAGE

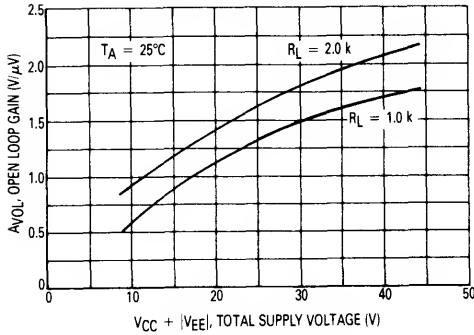


FIGURE 14 — OPEN LOOP VOLTAGE GAIN
versus LOAD RESISTANCE

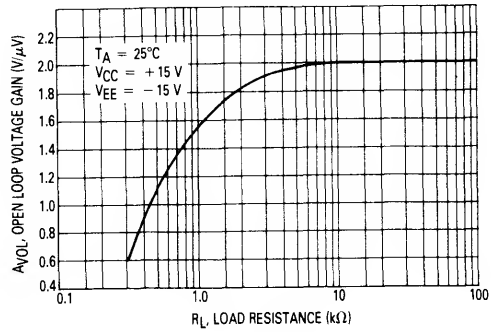


FIGURE 15 — MAXIMUM OUTPUT SWING
versus RESISTIVE LOAD

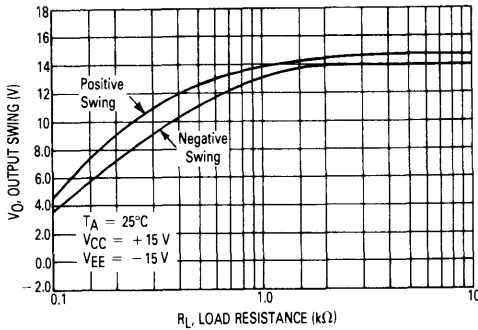


FIGURE 16 — POWER SUPPLY REJECTION RATIO
versus FREQUENCY

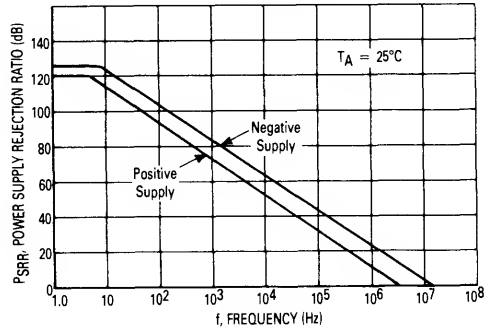


FIGURE 17 — COMMON MODE REJECTION RATIO
versus FREQUENCY

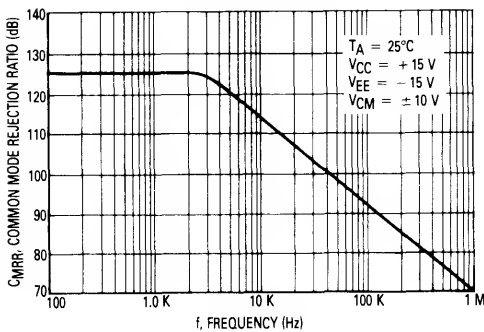


FIGURE 18 — OPEN LOOP GAIN versus FREQUENCY

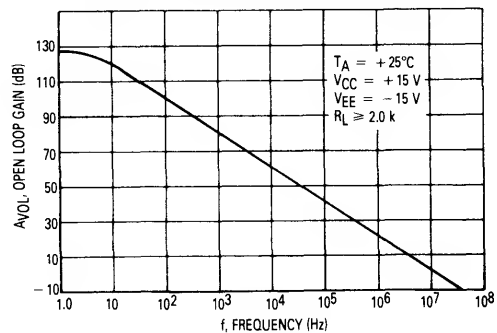


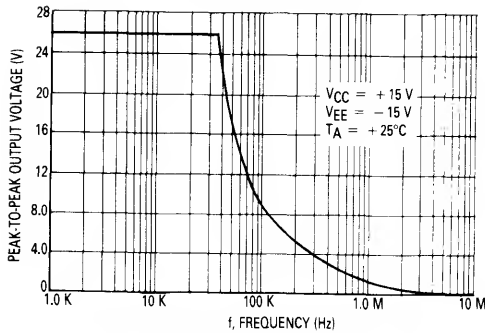
FIGURE 19 — MAXIMUM UNDISTORTED OUTPUT
versus FREQUENCY

FIGURE 20 — SMALL-SIGNAL TRANSIENT RESPONSE

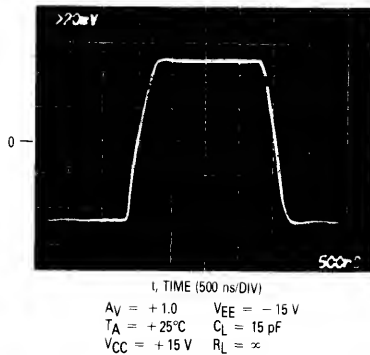
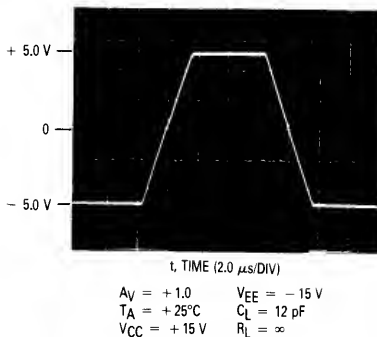


FIGURE 21 — LARGE-SIGNAL TRANSIENT RESPONSE



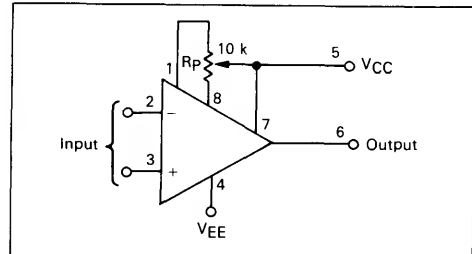
APPLICATIONS INFORMATION

The designer is cautioned that stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can prevent realization of the drift performance indicated. Best operation will be obtained when both input contacts are maintained at the same temperature, preferably close to the temperature of the device's package.

OFFSET VOLTAGE ADJUSTMENT

The input offset voltage and drift over temperature are permanently trimmed at wafer testing. However, if further adjustment of V_{IO} is required, nulling with a 10 k Ω potentiometer as shown in Figure 22 will not degrade TCV_{IO} . Other potentiometer values from 1.0 k Ω to 1.0 M Ω can be used with a slight degradation (0.1 to 0.2 $\mu V/^{\circ}C$) of TCV_{IO} . Trimming to a value other than zero creates a drift of ($V_{IO}/300$) $\mu V/^{\circ}C$, e.g. if V_{IO} is adjusted to 100 μV , the change in TCV_{IO} will be 0.33 $\mu V/^{\circ}C$. The offset voltage adjustment range with a 10 k Ω potentiometer is ± 4.0 mV. If a smaller adjustment range is required, the sensitivity and/or resolution of the nulling can be increased by using a smaller pot in conjunction with fixed resistors.

FIGURE 22 — OFFSET NULLING CIRCUIT



NOISE MEASUREMENTS

The extremely low noise of these devices can make accurate measurement a difficult task. In order to realize the 80 nV peak-to-peak noise specification of the op amp in the 0.1 Hz to 10 Hz frequency range, the following guidelines must be observed:

- (1) The device has to be warmed up for at least five minutes. As the op amp warms up, its offset voltage changes typically 4.0 μV due to its chip temperature increasing 14 to 20 $^{\circ}C$ from the moment the power supplies are turned on. In the 10 sec measurement interval these temperature-induced effects can easily exceed tens of nanovolts.
- (2) For similar reasons, the device has to be well shielded from air currents to eliminate the possibility of thermoelectric effects in excess of several nanovolts.

- (3) Sudden motion in the vicinity of the device can also "feed-through" to increase the observed noise.
- (4) The test time to measure 0.1 Hz to 10 Hz noise should not exceed 10 sec. As shown in the noise tester frequency response curve (Figure 1) the 0.1 Hz corner is defined by only one zero. The test time of 10 sec acts as an additional zero to eliminate noise contributions from the frequency band below 0.1 Hz.

A noise-voltage density test is recommended when measuring noise on a large number of units. A 10 Hz noise-voltage density measurement will correlate well with a 0.1 Hz-to-10 Hz peak-to-peak noise reading since both results are determined by the white noise and the location of the $1/f$ corner frequency.

UNITY GAIN BUFFER APPLICATIONS

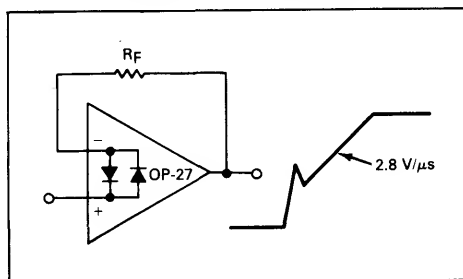
When $R_F \leq 100 \Omega$ and the input is driven with a fast, large signal pulse ($> 1.0 \text{ V}$), the output waveform will look as shown in Figure 23.

During the initial fast input step, the input protection diodes effectively short the output to the input and current limit only by the output short circuit protection of

the op amp and the source resistance of the generator. With $R_F \geq 500 \Omega$, the output is capable of handling the current requirements ($I_L \leq 20 \text{ mA}$ at 10 V) and the amplifier stays in its active mode and a smooth transition will occur.

As with all operational amplifiers when $R_F > 2.0 \text{ k}\Omega$, a pole will be created with R_F and the amplifier's input capacitance (8.0 pF), creating additional phase shift and reducing the phase margin. A small capacitor (20 to 50 pF) in parallel with R_F will eliminate this problem.

FIGURE 23 — PULSED OPERATION

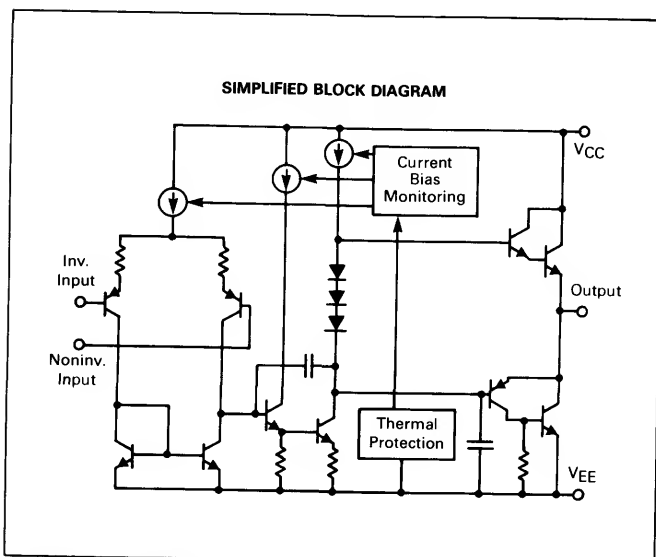


Advance Information

DUAL POWER OPERATIONAL AMPLIFIER

The TCA0372 is a monolithic circuit intended for use as a power operational amplifier in a wide range of applications, including servo amplifiers and power supplies. No deadband crossover distortion provides better performance for driving coils.

- Output Current to 1.0 A
- Slew Rate of $1.3 \text{ V}/\mu\text{s}$
- Wide Bandwidth of 1.1 MHz
- Internal Thermal Shutdown
- Single or Split Supply Operation
- Excellent Gain and Phase Margins
- Common Mode Input Includes Ground
- Zero Deadband Crossover Distortion

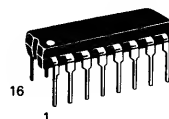


This document contains information on a new product. Specifications and information herein are subject to change without notice.

TCA0372

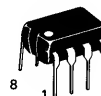
DUAL POWER OPERATIONAL AMPLIFIER

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**

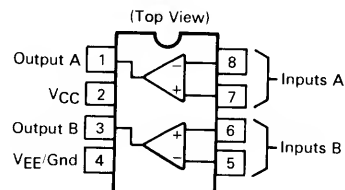
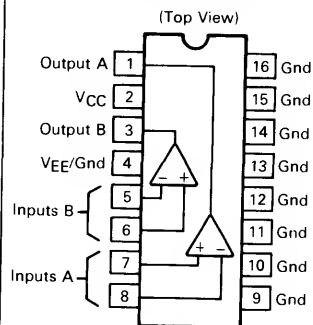


DP1 SUFFIX
PLASTIC PACKAGE
CASE 626

DP2 SUFFIX
PLASTIC PACKAGE
CASE 648



PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Junction Temperature Range	Package
TCA0372DP1	$T_J = -40^\circ\text{C to } +125^\circ\text{C}$	Plastic DIP
TCA0372DP2		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (from V_{CC} to V_{EE})	V_S	40	Volts
Input Differential Voltage Range	V_{IDR}	(Note 1)	Volts
Input Voltage Range	V_{IR}	(Note 1)	Volts
Operating Junction Temperature (Note 2)	T_J	+125	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C
DC Output Current	I_O	1.0	A
Peak Output Current (Nonrepetitive)	I_{max}	1.5	A

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, R_L connected to ground $T_J = T_{low}$ to T_{high} (Note 3) unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($V_{CM} = 0$) $V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_J = +25^\circ\text{C}$ $V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_J = T_{low}$ to T_{high}	V_{IO}	— —	3.0 —	15 20	mV
Average Temperature Coefficient of Offset Voltage	$\Delta V_{IO}/\Delta T$	—	20	—	$\mu\text{V}/^\circ\text{C}$
Input Bias Current ($V_{CM} = 0$)	I_{IB}	—	100	500	nA
Input Offset Current ($V_{CM} = 0$)	I_{IO}	—	10	50	nA
Large Signal Voltage Gain $V_O = \pm 10\text{ V}$, $R_L = 2.0\text{ k}$	A_{VOL}	30	100	—	V/mV
Output Voltage Swing ($I_L = 100\text{ mA}$) $V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_J = +25^\circ\text{C}$ $V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_J = T_{low}$ to T_{high}	V_{OH} V_{OL}	14 13.9	14.2 —	— —	V
$V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_J = +25^\circ\text{C}$ $V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_J = T_{low}$ to T_{high}	V_{OH} V_{OL}	— —	-14.2 —	-14 -13.9	V
Output Voltage Swing ($I_L = 1.0\text{ A}$) $V_{CC} = +24\text{ V}$, $V_{EE} = 0\text{ V}$, $T_J = +25^\circ\text{C}$ $V_{CC} = +24\text{ V}$, $V_{EE} = 0\text{ V}$, $T_J = T_{low}$ to T_{high}	V_{OH} V_{OL}	22.5 22.5	22.7 —	— —	V
$V_{CC} = +24\text{ V}$, $V_{EE} = 0\text{ V}$, $T_J = +25^\circ\text{C}$ $V_{CC} = +24\text{ V}$, $V_{EE} = 0\text{ V}$, $T_J = T_{low}$ to T_{high}	V_{OH} V_{OL}	— —	1.3 —	1.5 1.5	V
Input Common Mode Voltage Range $T_J = +25^\circ\text{C}$ $T_J = T_{low}$ to T_{high}	V_{ICR}	V_{EE} to $(V_{CC} - 1.0)$ V_{EE} to $(V_{CC} - 1.3)$			V
Common Mode Rejection Ratio ($R_S = 10\text{ k}$)	CMRR	70	90	—	dB
Power Supply Rejection Ratio ($R_S = 100\text{ }\Omega$)	PSRR	70	90	—	dB
Power Supply Current $V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_J = +25^\circ\text{C}$ $V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_J = T_{low}$ to T_{high}	I_D	— —	7.0 —	10 14	mA

NOTES:

1. Either or both input voltages must not exceed the magnitude of V_{CC} or V_{EE} .
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded.
3. $T_{low} = -40^\circ\text{C}$ $T_{high} = +125^\circ\text{C}$

TCA0372

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, R_L connected to ground, $T_J = +25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Slew Rate ($V_{in} = -10\text{ V}$ to $+10\text{ V}$, $R_L = 2.0\text{ k}$, $C_L = 100\text{ pF}$) $A_V = -1.0$, $T_J = T_{low}$ to T_{high}	SR	1.0	1.4	—	$\text{V}/\mu\text{s}$
Gain Bandwidth Product ($f = 100\text{ kHz}$, $C_L = 100\text{ pF}$, $R_L = 2.0\text{ k}$) $T_J = 25^\circ\text{C}$ $T_J = T_{low}$ to T_{high}	GBW	0.9 0.7	1.1 —	— —	MHz
Phase Margin $T_J = T_{low}$ to T_{high} $R_L = 2.0\text{ k}$, $C_L = 100\text{ pF}$	ϕ_m	—	80	—	Degrees
Gain Margin $R_L = 2.0\text{ k}$, $C_L = 100\text{ pF}$	A_m	—	15	—	dB
Equivalent Input Noise Voltage $R_S = 100\text{ Ohms}$, $f = 1.0\text{ kHz}$ to 100 kHz	e_n	—	22	—	$\text{nV}/\sqrt{\text{Hz}}$
Total Harmonic Distortion $A_V = -1.0$, $R_L = 50\text{ Ohms}$, $V_O = 0.5\text{ VRMS}$, $f = 1.0\text{ kHz}$	THD	—	0.02	—	%

NOTE: In case V_{EE} is disconnected before V_{CC} , a diode between V_{EE} and GROUND is recommended to avoid damaging device.

FIGURE 1 — BIDIRECTIONAL DC MOTOR CONTROL WITH MICROPROCESSOR-COMPATIBLE INPUTS

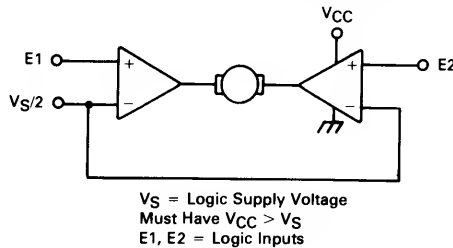
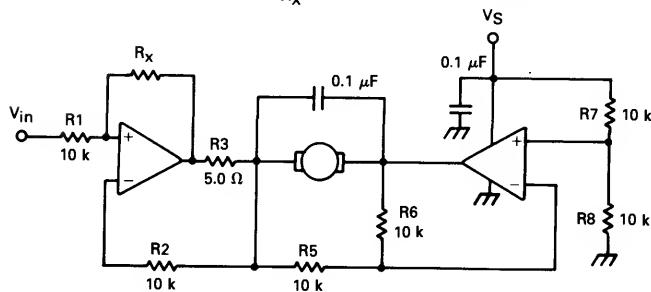


FIGURE 2 — BIDIRECTIONAL SPEED CONTROL OF DC MOTORS

For circuit stability ensure that $R_X > \frac{2R_3 \cdot R_1}{R_M}$ where $R_M = \text{internal resistance of motor}$. The voltage available at the terminals of the motor is:

$$V_M = 2 \left(V_1 - \frac{V_S}{2} \right) + |R_O| \cdot I_M$$

where $|R_O| = \frac{2R_3 \cdot R_1}{R_X}$ and I_M is the motor current.



THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(TA)} = \frac{T_{J(max)} - T_A}{R_{\theta JA}(\text{TYP})}$$

Where: $P_{D(TA)} = \text{Power dissipation allowable at a given operating ambient temperature.}$

This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(max)}$ = Maximum operating junction temperature as listed in the maximum ratings section.

T_A = Maximum desired operating ambient temperature.

$R_{\theta JA}(\text{typ})$ = Typical thermal resistance junction to ambient.

**LOW POWER JFET INPUT
 OPERATIONAL AMPLIFIER**

These JFET input operational amplifiers are designed for low power applications. They feature high input impedance, low input bias current and low input offset current. Advanced design techniques allow for higher slew rates, gain bandwidth products and output swing. The TL061 device provides for the external null adjustment of input offset voltage.

These devices are specified over the commercial, vehicular and military temperature ranges. The commercial and vehicular devices are available in Plastic dual in-line and SOIC packages. The military devices are available in Ceramic dual in-line packages.

- Low Supply Current — 200 μ A/Amplifier
- Low Input Bias Current — 5.0 pA
- High Gain Bandwidth — 2.0 MHz
- High Slew Rate — 6.0 V/ μ s
- High Input Impedance — $10^{12} \Omega$
- Large Output Voltage Swing — ± 14 V
- Output Short Circuit Protection

ORDERING INFORMATION

Op Amp Function	Device	Tested Temperature Range	Package
Single	TL061CD, ACD	0 to +70°C	SO-8 Plastic DIP
	TL061CP, ACP		
	TL061VD	-40 to +85°C	SO-8 Plastic DIP
	TL061VP		
	TL061MJG	-55 to +125°C	Ceramic DIP
Dual	TL062CD, ACD	0 to +70°C	SO-8 Plastic DIP
	TL062CP, ACP		
	TL062VD	-40 to +85°C	SO-8 Plastic DIP
	TL062VP		
	TL062MJG	-55 to +125°C	Ceramic DIP
Quad	TL064CD, ACD	0 to +70°C	SO-14 Plastic DIP
	TL064CN, ACN		
	TL064VD	-40 to +85°C	SO-14 Plastic DIP
	TL064VN		
	TL064MJ	-55 to +125°C	Ceramic DIP

**TL061
 TL062
 TL064**

**LOW POWER
 JFET INPUT
 OPERATIONAL AMPLIFIERS**

**SILICON MONOLITHIC
 INTEGRATED CIRCUITS**



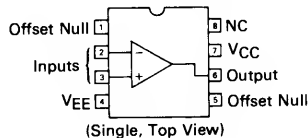
P SUFFIX
 PLASTIC PACKAGE
 CASE 626



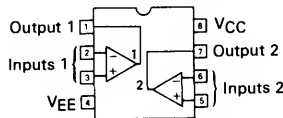
JG SUFFIX
 CERAMIC PACKAGE
 CASE 693



D SUFFIX
 PLASTIC PACKAGE
 CASE 751
 (SO-8)



(Single, Top View)



(Dual, Top View)



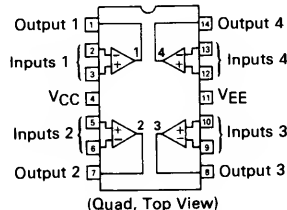
N SUFFIX
 PLASTIC PACKAGE
 CASE 646



J SUFFIX
 CERAMIC PACKAGE
 CASE 632



D SUFFIX
 PLASTIC PACKAGE
 CASE 751A
 (SO-14)



(Quad, Top View)

TL061, TL062, TL064

2

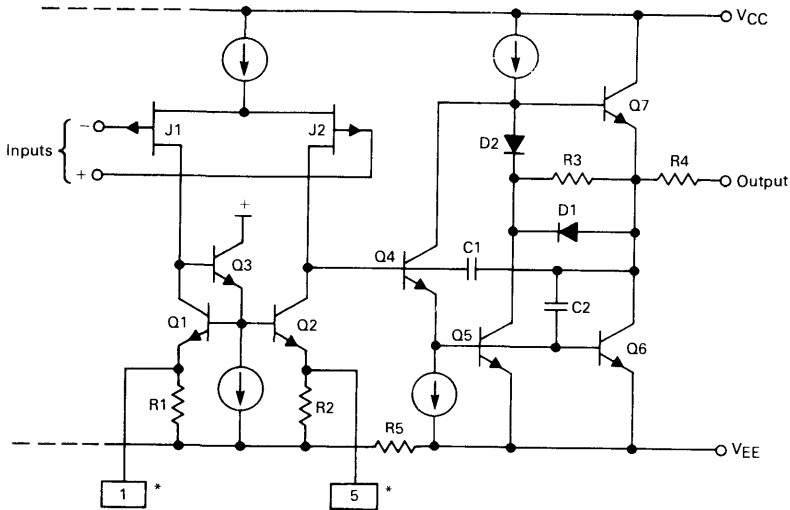
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (from V_{CC} to V_{EE})	V_S	+ 36	V
Input Differential Voltage Range (Note 1)	V_{IDR}	± 30	V
Input Voltage Range (Notes 1 and 2)	V_{IR}	± 15	V
Output Short-Circuit Duration (Note 3)	t_S	Indefinite	Seconds
Operating Junction Temperature (Note 3)	T_J		$^{\circ}\text{C}$
Ceramic Package		+ 160	
Plastic Package		+ 150	
Storage Temperature Range	T_{stg}		$^{\circ}\text{C}$
Ceramic Package		- 65 to + 160	
Plastic Package		- 60 to + 150	

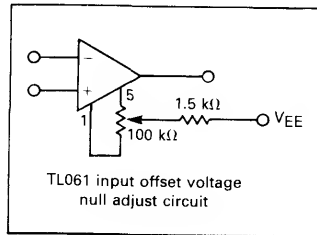
NOTES:

1. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
2. The magnitude of the input voltage must never exceed the magnitude of the supply or 15 volts, whichever is less.
3. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded. (See Figure 1.)

EQUIVALENT CIRCUIT SCHEMATIC (EACH AMPLIFIER)



*Null adjustment pins for TL061 only.



TL061, TL062, TL064

2

ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, unless otherwise noted)

Characteristic	Symbol	TL061AC TL062AC TL064AC			TL061C TL062C TL064C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S = 50\ \Omega$, $V_O = 0\text{ V}$) $T_A = 25^\circ\text{C}$ $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$	V_{IO}	— —	3.0 —	6.0 7.5	— —	3.0 —	15 20	mV
Average Temperature Coefficient for Offset Voltage ($R_S = 50\ \Omega$, $V_O = 0\text{ V}$)	$\Delta V_{IO}/\Delta T$	—	10	—	—	10	—	$\mu\text{V}/^\circ\text{C}$
Input Offset Current ($V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$) $T_A = 25^\circ\text{C}$ $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$	I_{IO}	— —	0.5 —	100 2.0	— —	0.5 —	200 2.0	pA nA
Input Bias Current ($V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$) $T_A = 25^\circ\text{C}$ $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$	I_{IB}	— —	3.0 —	200 7.0	— —	3.0 —	200 10	pA nA
Input Common Mode Voltage Range $T_A = 25^\circ\text{C}$	V_{ICR}	— -11.5	+14.5 -12	+11.5 —	— -11	+14.5 -12	+11 —	V
Large Signal Voltage Gain ($R_L = 10\text{ k}\Omega$, $V_O = \pm 10\text{ V}$) $T_A = 25^\circ\text{C}$ $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$	A_{VOL}	4.0 4.0	58 —	— —	3.0 3.0	58 —	— —	V/mV
Output Voltage Swing ($R_L = 10\text{ k}\Omega$, $V_{ID} = 1.0\text{ V}$) $T_A = 25^\circ\text{C}$ $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$	V_{O+} V_{O-} V_{O+} V_{O-}	+10 — +10 —	+14 -14 — —	— -10 — -10	+10 — +10 —	+14 -14 — —	— -10 — -10	V
Common Mode Rejection ($R_S = 50\ \Omega$, $V_{CM} = V_{ICR}\text{ min}$, $V_O = 0\text{ V}$, $T_A = 25^\circ\text{C}$)	CMR	80	84	—	70	84	—	dB
Power Supply Rejection ($R_S = 50\ \Omega$, $V_{CM} = 0\text{ V}$, $V_O = 0$, $T_A = 25^\circ\text{C}$)	PSR	80	86	—	70	86	—	dB
Power Supply Current (each amplifier) (No Load, $V_O = 0\text{ V}$, $T_A = 25^\circ\text{C}$)	I_D	—	200	250	—	200	250	μA
Total Power Dissipation (each amplifier) (No Load, $V_O = 0\text{ V}$, $T_A = 25^\circ\text{C}$)	P_D	—	6.0	7.5	—	6.0	7.5	mW

TL061, TL062, TL064

2

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = T_{\text{low}}$ to T_{high} (Note 4), unless otherwise noted)

Characteristic	Symbol	TL061M,V TL062M,V			TL064M,V			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S = 50\ \Omega$, $V_O = 0\text{ V}$) $T_A = 25^\circ\text{C}$ $T_A = T_{\text{low}}$ to T_{high}	V_{IO}	—	3.0	6.0 9.0	—	3.0	9.0 15	mV
Average Temperature Coefficient of Offset Voltage ($R_S = 50\ \Omega$, $V_O = 0\text{ V}$)	$\Delta V_{IO}/\Delta T$	—	10	—	—	10	—	$\mu\text{V}/^\circ\text{C}$
Input Offset Current ($V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$) $T_A = 25^\circ\text{C}$ $T_A = T_{\text{low}}$ to T_{high}	I_{IO}	—	5.0	100 20	—	5.0	100 20	pA nA
Input Bias Current ($V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$) $T_A = 25^\circ\text{C}$ $T_A = T_{\text{low}}$ to T_{high}	I_{IB}	—	30	200 50	—	30	200 50	pA nA
Input Common Mode Voltage Range ($T_A = 25^\circ\text{C}$)	V_{ICR}	— -11.5	+14.5 -12	+11.5 —	— -11.5	+14.5 -12	+11.5 —	V
Large Signal Voltage Gain ($R_L = 10\text{ k}\Omega$, $V_O = \pm 10\text{ V}$) $T_A = 25^\circ\text{C}$ $T_A = T_{\text{low}}$ to T_{high}	A_{VOL}	4.0 4.0	58 —	— —	4.0 4.0	58 —	— —	V mV
Output Voltage Swing ($R_L = 10\text{ k}\Omega$, $V_{ID} = 1.0\text{ V}$) $T_A = 25^\circ\text{C}$ $T_A = T_{\text{low}}$ to T_{high}	V_{O+} V_{O-} V_{O+} V_{O-}	+10 — +10 —	+14 -14 — —	— -10 — -10	+10 — +10 —	+14 -14 — —	— -10 — -10	V
Common Mode Rejection ($R_S = 50\ \Omega$, $V_{CM} = V_{ICR\text{ min}}$, $V_O = 0\text{ V}$, $T_A = 25^\circ\text{C}$)	CMR	80	84	—	80	84	—	dB
Power Supply Rejection ($R_S = 50\ \Omega$, $V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$, $T_A = 25^\circ\text{C}$)	PSR	80	86	—	80	86	—	dB
Power Supply Current (each Amplifier) (No Load, $V_O = 0\text{ V}$, $T_A = 25^\circ\text{C}$)	I_D	—	200	250	—	200	250	μA
Total Power Dissipation (each Amplifier) (No Load, $V_O = 0\text{ V}$, $T_A = 25^\circ\text{C}$)	P_D	—	6.0	7.5	—	6.0	7.5	mW

Note 4. TL06XM $T_{\text{low}} = -55^\circ\text{C}$ $T_{\text{high}} = +125^\circ\text{C}$
 TL06XV $T_{\text{low}} = -40^\circ\text{C}$ $T_{\text{high}} = +85^\circ\text{C}$

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = +25^\circ\text{C}$, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Slew Rate ($V_{in} = -10\text{ V}$ to $+10\text{ V}$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, $A_V = +1.0$)	SR	2.0	6.0	—	$\text{V}/\mu\text{s}$
Rise Time ($V_{in} = 20\text{ mV}$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, $A_V = +1.0$)	t_r	—	0.1	—	μs
Overshoot ($V_{in} = 20\text{ mV}$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, $A_V = +1.0$)	OS	—	10	—	%
Settling Time ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $A_V = -1.0$, $R_L = 10\text{ k}\Omega$, $V_O = 0\text{ V}$ to $+10\text{ V}$ step)	t_s	—	1.6 2.2	—	μs
Gain Bandwidth Product ($f = 200\text{ kHz}$)	GBW	—	2.0	—	MHz
Equivalent Input Noise ($R_S = 100\ \Omega$, $f = 1.0\text{ kHz}$)	e_n	—	47	—	$\text{nV}/\sqrt{\text{Hz}}$
Input Resistance	R_i	—	10^{12}	—	Ω
Channel Separation ($f = 10\text{ kHz}$)	CS	—	120	—	dB

TL061, TL062, TL064

TYPICAL PERFORMANCE CURVES

FIGURE 1 — MAXIMUM POWER DISSIPATION versus TEMPERATURE FOR PACKAGE VARIATIONS

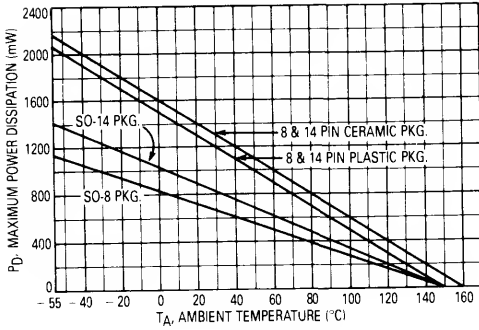


FIGURE 2 — OUTPUT VOLTAGE SWING versus SUPPLY VOLTAGE

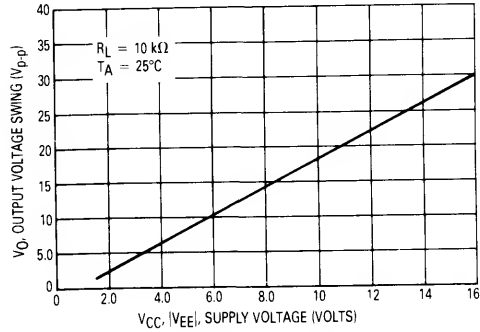


FIGURE 3 — OUTPUT VOLTAGE SWING versus TEMPERATURE

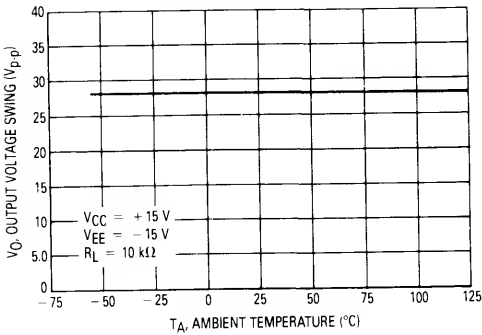


FIGURE 4 — OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

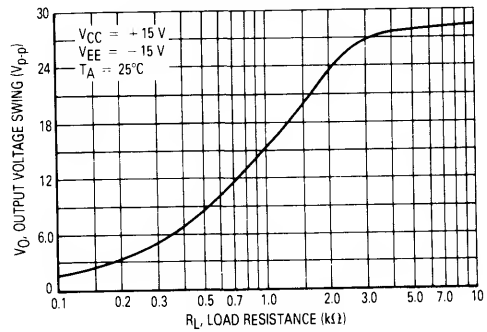


FIGURE 5 — OUTPUT VOLTAGE SWING versus FREQUENCY

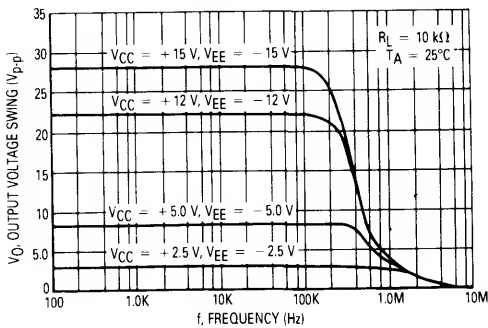


FIGURE 6 — LARGE SIGNAL VOLTAGE GAIN versus TEMPERATURE

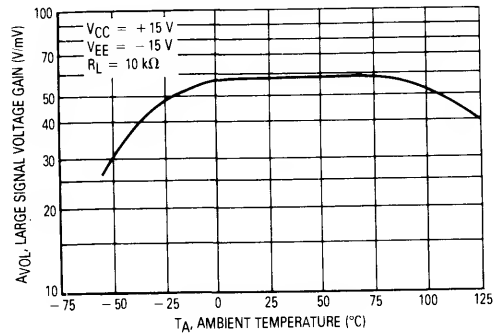


FIGURE 7 — OPEN-LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY

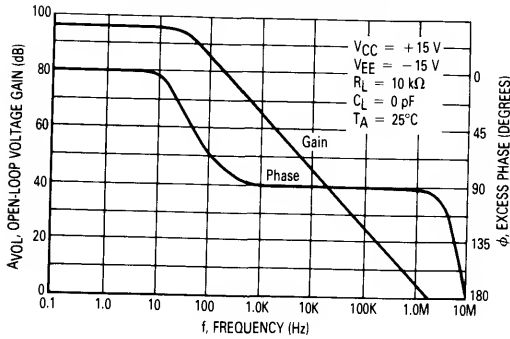


FIGURE 8 — SUPPLY CURRENT PER AMPLIFIER versus SUPPLY VOLTAGE

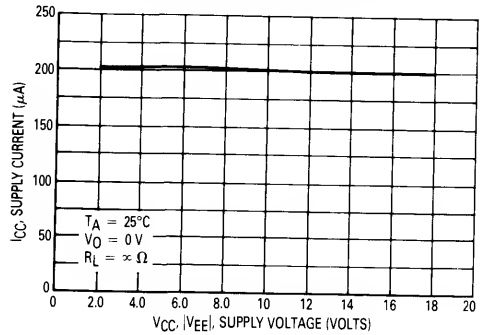


FIGURE 9 — SUPPLY CURRENT PER AMPLIFIER versus TEMPERATURE

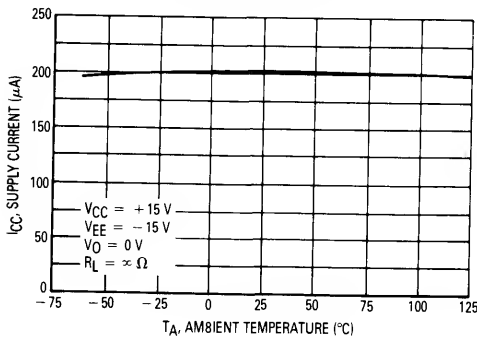


FIGURE 10 — TOTAL POWER DISSIPATION versus TEMPERATURE

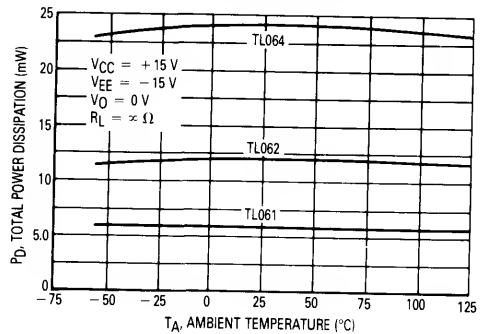


FIGURE 11 — COMMON-MODE REJECTION versus TEMPERATURE

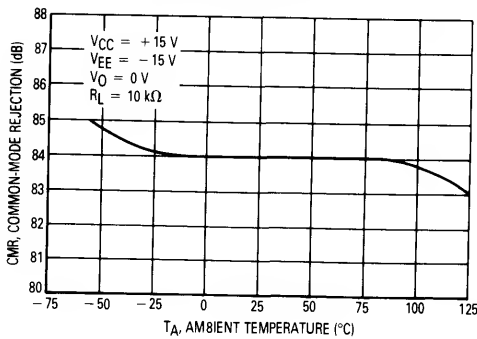


FIGURE 12 — COMMON-MODE REJECTION versus FREQUENCY

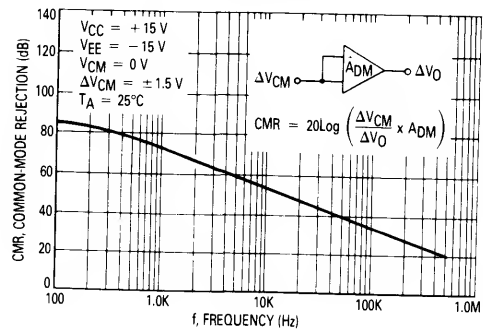


FIGURE 13 — POWER SUPPLY REJECTION
versus FREQUENCY

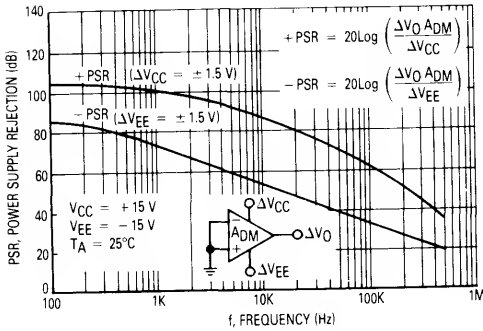


FIGURE 14 — NORMALIZED GAIN BANDWIDTH
PRODUCT AND SLEW RATE AND PHASE MARGIN versus TEMPERATURE

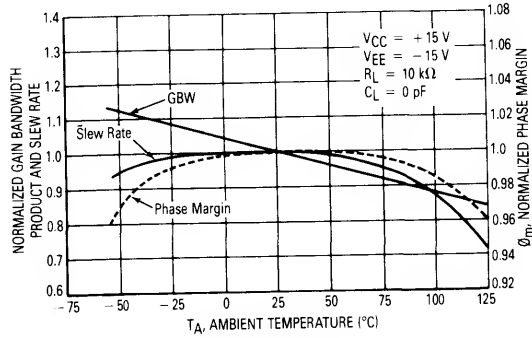


FIGURE 15 — INPUT BIAS CURRENT
versus TEMPERATURE

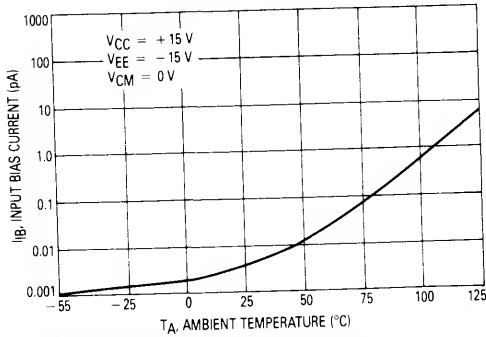


FIGURE 16 — INPUT NOISE VOLTAGE versus FREQUENCY

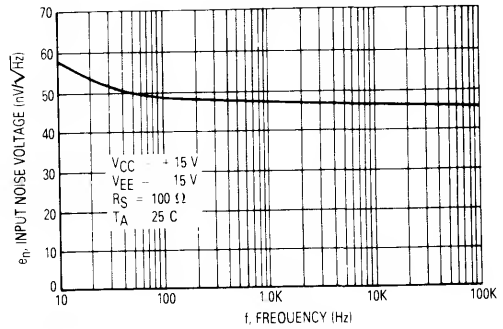


FIGURE 17 — SMALL SIGNAL RESPONSE

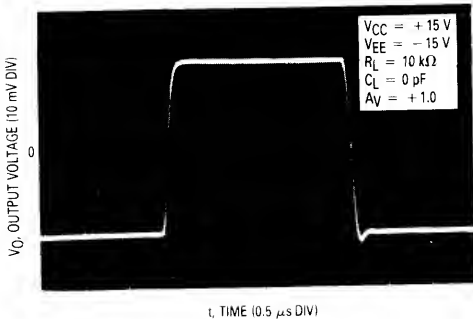


FIGURE 18 — LARGE SIGNAL RESPONSE

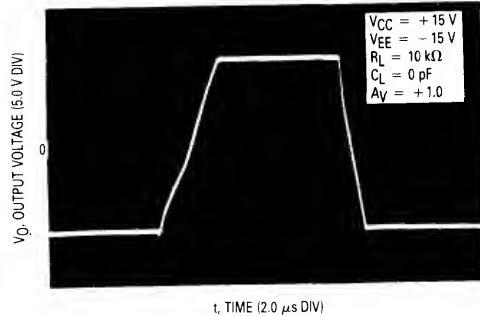


FIGURE 19 — AC AMPLIFIER

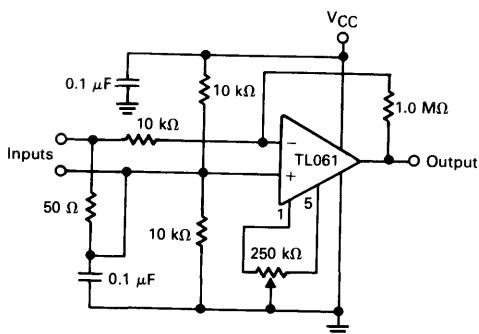


FIGURE 20 — HIGH-Q NOTCH FILTER

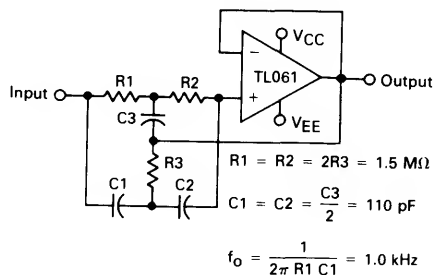


FIGURE 21 — INSTRUMENTATION AMPLIFIER

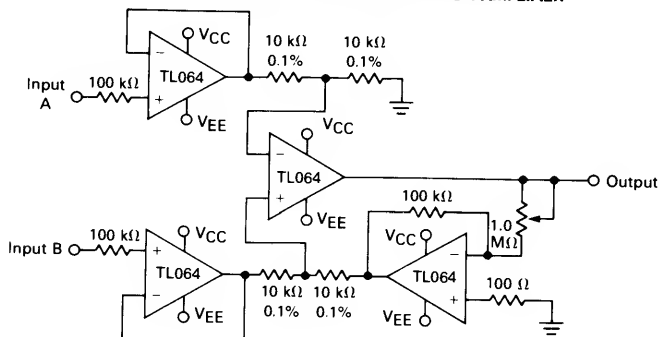


FIGURE 22 — 0.5 Hz SQUARE-WAVE OSCILLATOR

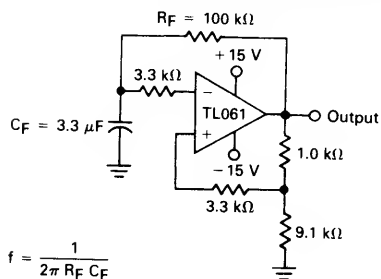
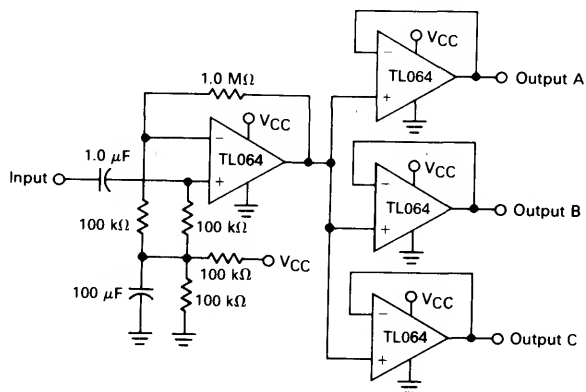


FIGURE 23 — AUDIO DISTRIBUTION AMPLIFIER



TL071
TL072
TL074

LOW NOISE, JFET INPUT
OPERATIONAL AMPLIFIERS
SILICON MONOLITHIC
INTEGRATED CIRCUITS

LOW NOISE, JFET INPUT
OPERATIONAL AMPLIFIERS

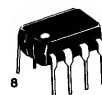
These low noise JFET input operational amplifiers combine two state-of-the-art linear technologies on a single monolithic integrated circuit. Each internally compensated operational amplifier has well matched high voltage JFET input devices for low input offset voltage. The BIFET technology provides wide bandwidths and fast slew rates with low input bias currents, input offset currents, and supply currents. Moreover, the devices exhibit low noise and low harmonic distortion making them ideal for use in high fidelity audio amplifier applications.

These devices are available in single, dual and quad operational amplifiers which are pin-compatible with the industry standard MC1741, MC1458, and the MC3403/LM324 bipolar products.

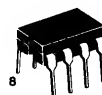
- Low Input Noise Voltage — $18 \text{ nV}/\sqrt{\text{Hz}}$ Typ
- Low Harmonic Distortion — 0.01% Typ
- Low Input Bias and Offset Currents
- High Input Impedance — $10^{12} \Omega$ Typ
- High Slew Rate — $13 \text{ V}/\mu\text{s}$ Typ
- Wide Gain Bandwidth — 4.0 MHz Typ
- Low Supply Current — 1.4 mA per Amp

ORDERING INFORMATION

Op Amp Function	Device	Temperature Range	Package
Single	TL071ACD, CD	0 to +70°C	SO-8
	TL071ACJG, CJG		Ceramic DIP
	TL071ACP, CP		Plastic DIP
Dual	TL072ACD, CD	0 to +70°C	SO-8
	TL072ACJG, CJG		Ceramic DIP
	TL072ACP, CP		Plastic DIP
Quad	TL074ACJ, CJ	0 to +70°C	Ceramic DIP
	TL074ACN, CN		Plastic DIP



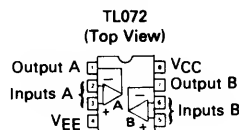
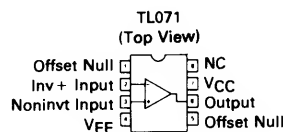
P SUFFIX
 PLASTIC PACKAGE
 CASE 626



JG SUFFIX
 CERAMIC PACKAGE
 CASE 693



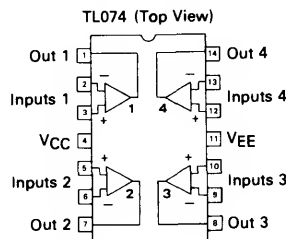
D SUFFIX
 PLASTIC PACKAGE
 CASE 751
 (SO-8)



N SUFFIX
 PLASTIC PACKAGE
 CASE 646
 (TL074 Only)



J SUFFIX
 CERAMIC PACKAGE
 CASE 632
 (TL074 Only)



TL071, TL072, TL074

MAXIMUM RATINGS

Rating	Symbol	TL07_C TL07_AC	Unit
Supply Voltage	V _{CC} V _{EE}	+18 -18	V
Differential Input Voltage	V _{ID}	±30	V
Input Voltage Range (Note 1)	V _{IDR}	±15	V
Output Short-Circuit Duration (Note 2)	t _S	Continuous	
Power Dissipation			
Plastic Package (N, P)	P _D	680	mW
Derate above T _A = +47°C	1/θ _{JA}	10	mW/°C
Ceramic Package (J, JG)	P _D	680	mW
Derate above T _A = +82°C	1/θ _{JA}	10	mW/°C
Operating Ambient Temperature Range	T _A	0 to +70	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

- NOTES:** 1. The magnitude of the input voltage must not exceed the magnitude of the supply voltage or 15 volts, whichever is less.
2. The output may be shorted to ground or either supply. Temperature and/or supply voltages must be limited to ensure that power dissipation ratings are not exceeded.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = -15 V, T_A = +25°C unless otherwise noted)

Characteristic	Symbol	TL07_C TL07_AC			Unit
		Min	Typ	Max	
Input Offset Voltage (R _S ≤ 10 k, V _{CM} = 0) TL071, TL072 TL074 TL07_A	V _{IO}	— — —	3.0 3.0 3.0	10 10 6.0	mV
Average Temperature Coefficient of Input Offset Voltage R _S = 50 Ω, T _A = T _{low} to T _{high} (Note 3)	ΔV _{IO} /ΔT	—	10	—	μV/°C
Input Offset Current (V _{CM} = 0) (Note 4) TL07_— TL07_A	I _{IO}	— —	5.0 5.0	50 50	pA
Input Bias Current (V _{CM} = 0) (Note 4) TL07_— TL07_A	I _{IB}	— —	30 30	200 200	pA
Input Resistance	r _i	—	10 ¹²	—	Ω
Common Mode Input Voltage Range TL07_— TL07_A	V _{ICR}	±10 ±11	+15, -12 +15, -12	— —	V
Large-Signal Voltage Gain (V _O = ±10 V, R _L ≥ 2.0 k) TL07_— TL07_A	A _{VOL}	25 50	150 150	— —	V/mV
Output Voltage Swing (Peak-to-Peak) (R _L = 10 k)	V _O	24	28	—	V
Common Mode Rejection Ratio (R _S ≤ 10 k) TL07_— TL07_A	CMRR	70 80	100 100	— —	dB
Supply Voltage Rejection Ratio (R _S ≤ 10 k) TL07_— TL07_A	PSRR	70 80	100 100	— —	dB
Supply Current (Each Amplifier)	I _D	—	1.4	2.5	mA
Unity Gain Bandwidth	BW	—	4.0	—	MHz
Slew Rate (See Figure 1) V _{in} = 10 V, R _L = 2.0 k, C _L = 100 pF	SR	—	13	—	V/μs

TL071, TL072, TL074

2

ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = +25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	TL07_C TL07_AC			Unit
		Min	Typ	Max	
Rise Time (See Figure 1)	t_r	—	0.1	—	μs
Overshoot Factor $V_{in} = 20\text{ mV}$, $R_L = 2.0\text{ k}$, $C_L = 100\text{ pF}$	—	—	10	—	%
Equivalent Input Noise Voltage $R_S = 100\ \Omega$, $f = 1000\text{ Hz}$	e_n	—	18	—	$\text{nV}/\sqrt{\text{Hz}}$
Equivalent Input Noise Current $R_S = 100\ \Omega$, $f = 1000\text{ Hz}$	i_n	—	0.01	—	$\text{pA}/\sqrt{\text{Hz}}$
Total Harmonic Distortion $V_O (\text{RMS}) = 10\text{ V}$, $R_S \leq 1.0\text{ k}$ $R_L \geq 2.0\text{ k}$, $f = 1000\text{ Hz}$	THD	—	0.01	—	%
Channel Separation $A_V = 100$	—	—	120	—	dB

ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = T_{\text{high}}$ to T_{low} (Note 3))

Characteristic	Symbol	TL07_C TL07_AC			Unit
		Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10\text{ k}$, $V_{CM} = 0$) TL071, TL072 TL074 TL07_A	V_{IO}	— — —	— — —	13 13 7.5	mV
Input Offset Current ($V_{CM} = 0$) (Note 4) TL07_— TL07_A	I_{IO}	— —	— —	2.0 2.0	nA
Input Bias Current ($V_{CM} = 0$) (Note 4) TL07_— TL07_A	I_{IB}	— —	— —	7.0 7.0	nA
Large-Signal Voltage Gain ($V_O = \pm 10\text{ V}$, $R_L \geq 2.0\text{ k}$) TL07_— TL07_A	A_{VOL}	15 25	— —	— —	V/mV
Output Voltage Swing (Peak-to-Peak) ($R_L \geq 10\text{ k}$) ($R_L \geq 2.0\text{ k}$)	V_O	24 20	— —	— —	V

NOTES (continued):

3. $T_{\text{low}} = 0^\circ\text{C}$ for TL071C, TL071AC
TL072C, TL072AC
TL074C, TL074AC

$T_{\text{high}} = +70^\circ\text{C}$ for TL071C, TL071AC
TL072C, TL072AC
TL074C, TL074AC

4. Input Bias currents of JFET input op amps approximately double for every 10°C rise in Junction Temperature as shown in Figure 3. To maintain Junction Temperature as close to Ambient Temperature as possible, pulse techniques must be used during testing.

TEST CIRCUITS

FIGURE 1 — UNITY GAIN VOLTAGE FOLLOWER

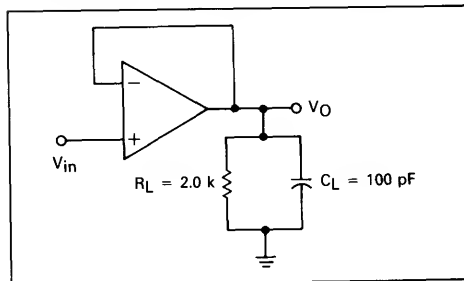


FIGURE 2 — INVERTING GAIN OF 10 AMPLIFIER

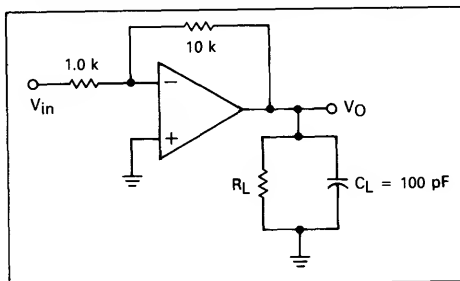


FIGURE 3 — INPUT BIAS CURRENT
versus TEMPERATURE

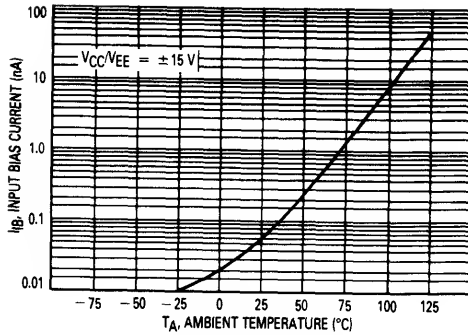


FIGURE 4 — OUTPUT VOLTAGE SWING
versus FREQUENCY

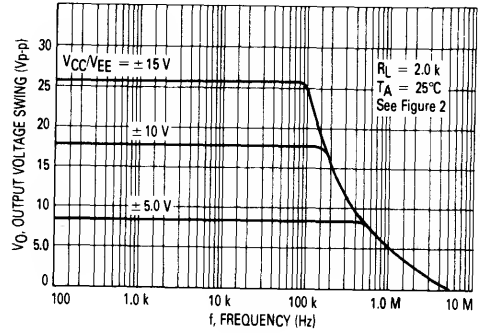


FIGURE 5 — OUTPUT VOLTAGE SWING
versus LOAD RESISTANCE

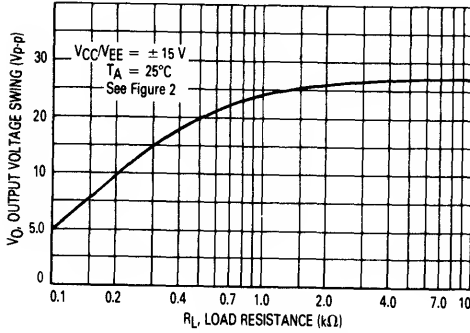


FIGURE 6 — OUTPUT VOLTAGE SWING
versus SUPPLY VOLTAGE

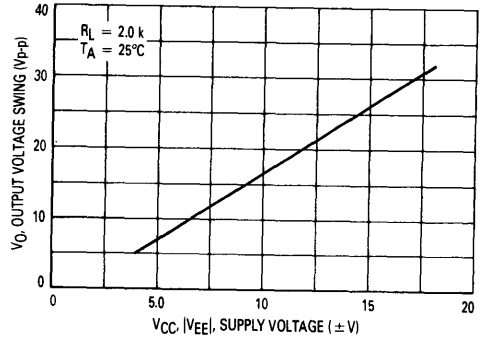


FIGURE 7 — OUTPUT VOLTAGE SWING
versus TEMPERATURE

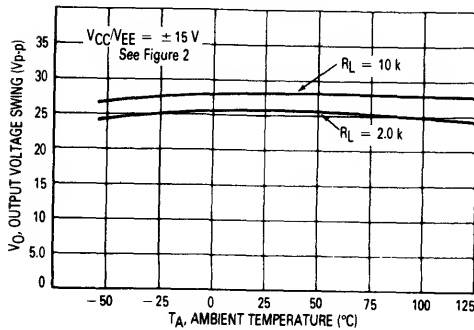


FIGURE 8 — SUPPLY CURRENT PER AMPLIFIER
versus TEMPERATURE

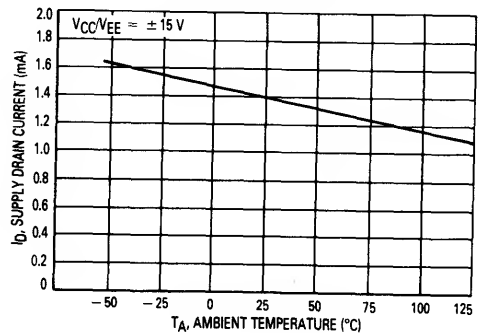


FIGURE 9 — LARGE-SIGNAL VOLTAGE GAIN AND PHASE SHIFT versus FREQUENCY

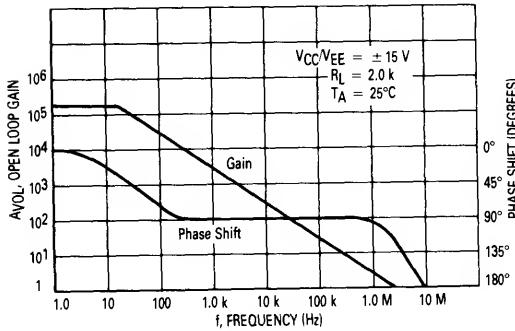


FIGURE 10 — LARGE-SIGNAL VOLTAGE GAIN versus TEMPERATURE

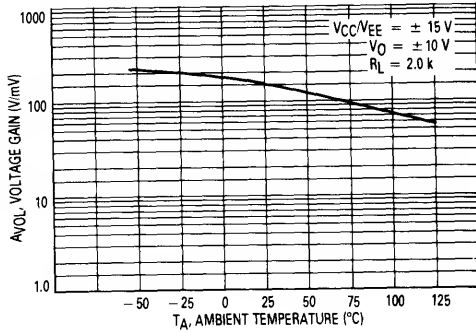


FIGURE 11 — NORMALIZED SLEW RATE versus TEMPERATURE

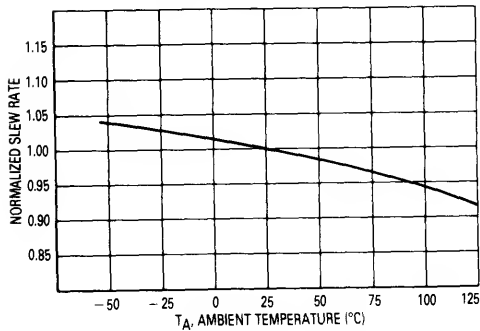


FIGURE 12 — EQUIVALENT INPUT NOISE VOLTAGE versus FREQUENCY

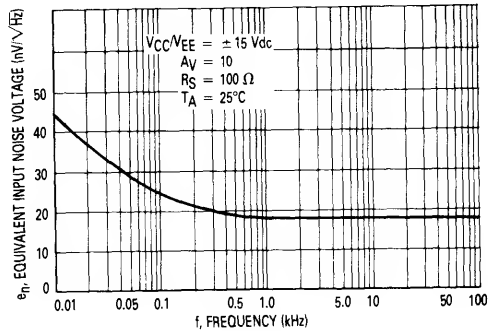
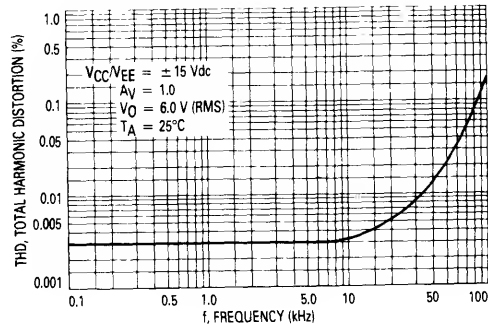


FIGURE 13 — TOTAL HARMONIC DISTORTION versus FREQUENCY



REPRESENTATIVE CIRCUIT SCHEMATIC
(Each Amplifier)

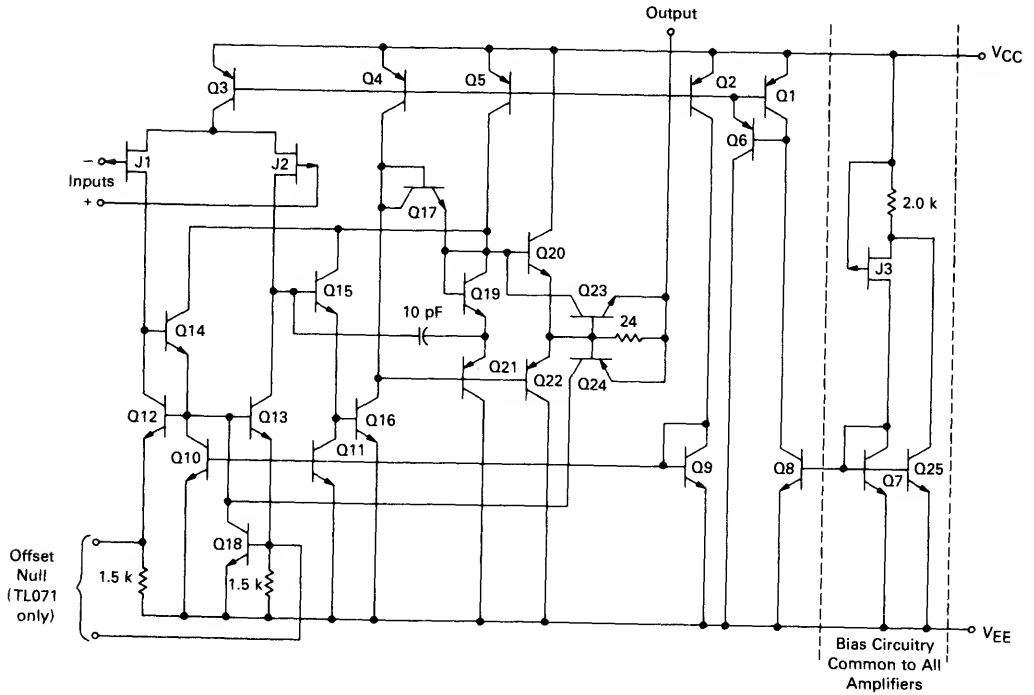


FIGURE 14 — AUDIO TONE CONTROL AMPLIFIER

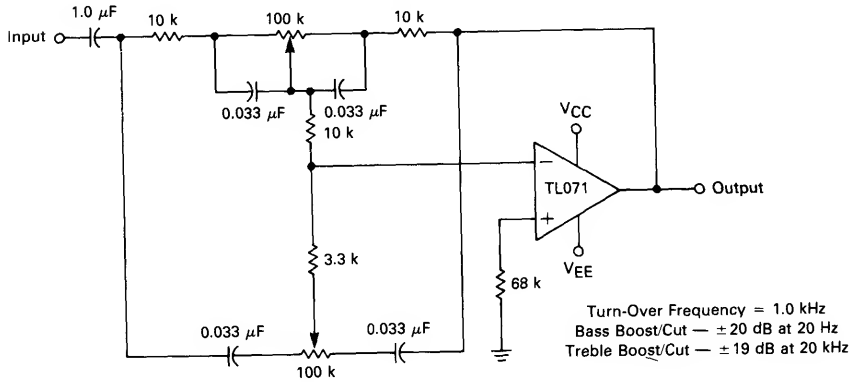
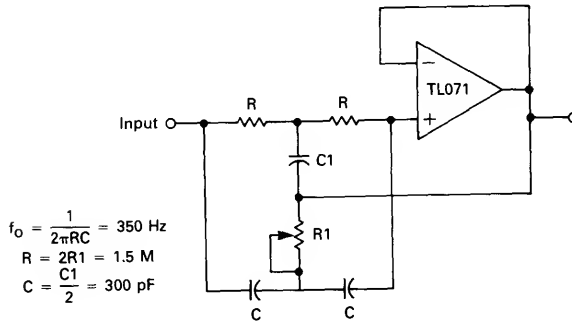


FIGURE 15 — HIGH Q NOTCH FILTER



JFET INPUT OPERATIONAL AMPLIFIERS

These low-cost JFET input operational amplifiers combine two state-of-the-art linear technologies on a single monolithic integrated circuit. Each internally compensated operational amplifier has well matched high voltage JFET input devices for low input offset voltage. The BIFET technology provides wide bandwidths and fast slew rates with low input bias currents, input offset currents, and supply currents.

These devices are available in single, dual and quad operational amplifiers which are pin-compatible with the industry standard MC1741, MC1458, and the MC3403/LM324 bipolar products. Devices with an "M" suffix are specified over the military operating temperature range of -55°C to $+125^{\circ}\text{C}$ and those with a "C" suffix are specified from 0°C to $+70^{\circ}\text{C}$.

- Input Offset Voltage Options of 6.0, and 15 mV Max
- Low Input Bias Current — 30 pA
- Low Input Offset Current — 5.0 pA
- Wide Gain Bandwidth — 4.0 MHz
- High Slew Rate — 13 V/ μs
- Low Supply Current — 1.4 mA per Amplifier
- High Input Impedance — $10^{12} \Omega$
- Industry Standard Pinouts

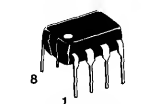
ORDERING INFORMATION

Op Amp Function	Device	Temperature Range	Package
Single	TL081ACD, CD	0 to $+70^{\circ}\text{C}$	SO-8
	TL081ACJG, CJG		Ceramic DIP
	TL081ACP, CP	-55 to $+125^{\circ}\text{C}$	Plastic DIP
	TL081MJG		Ceramic DIP
Dual	TL082ACD, CD	0 to $+70^{\circ}\text{C}$	SO-8
	TL082ACJG, CJG		Ceramic DIP
	TL082ACP, CP	-55 to $+125^{\circ}\text{C}$	Plastic DIP
	TL082MJG		Ceramic DIP
Quad	TL084ACJ, CJ	0 to $+70^{\circ}\text{C}$	Ceramic DIP
	TL084ACN, CN		Plastic DIP
	TL084MJ	-55 to $+125^{\circ}\text{C}$	Ceramic DIP

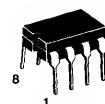
TL081 TL082 TL084

JFET INPUT OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUITS



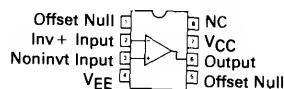
P SUFFIX
PLASTIC PACKAGE
CASE 626



JG SUFFIX
CERAMIC PACKAGE
CASE 693



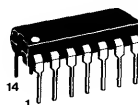
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)



TL081
(Top View)



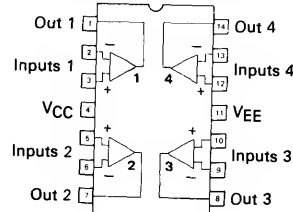
TL082
(Top View)



N SUFFIX
PLASTIC PACKAGE
CASE 646
(TL084 Only)



J SUFFIX
CERAMIC PACKAGE
CASE 632
(TL084 Only)



TL084 (Top View)

TL081, TL082, TL084

2

MAXIMUM RATINGS

Rating	Symbol	TL08_M	TL08_C TL08_AC	Unit
Supply Voltage	V _{CC} V _{EE}	+18 -18	+18 -18	V
Differential Input Voltage	V _{ID}	±30	±30	V
Input Voltage Range (Note 1)	V _{IDR}	±15	±15	V
Output Short-Circuit Duration (Note 2)	t _S	Continuous		
Power Dissipation	P _D	—	680	mW
Plastic Package (N, P) Derate above T _A = +47°C	1/θ _{JA}	—	10	mW/°C
Ceramic Package (J, JG) Derate above T _A = +82°C	1/θ _{JA}	680 10	680 10	mW mW/°C
Operating Ambient Temperature Range	T _A	-55 to +125	0 to +70	°C
Storage Temperature Range	T _{stg}	-65 to +150	-65 to +150	°C

NOTES: 1. The magnitude of the input voltage must not exceed the magnitude of the supply voltage or 15 volts, whichever is less.
2. The output may be shorted to ground or either supply. Temperature and/or supply voltages must be limited to ensure that power dissipation ratings are not exceeded.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = -15 V, T_A = +25°C unless otherwise noted)

Characteristic	Symbol	TL08_M			TL08_C TL08_AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (R _S ≤ 10 k, V _{CM} = 0) TL081, TL082 TL084 TL08_A	V _{IO}	— — —	3.0 3.0 —	6.0 9.0 —	— — —	5.0 5.0 3.0	15 15 6.0	mV
Average Temperature Coefficient of Input Offset Voltage R _S = 50 Ω, T _A = T _{low} to T _{high} (Note 3)	ΔV _{IO} /ΔT	—	10	—	—	10	—	μV/°C
Input Offset Current (V _{CM} = 0) (Note 4) TL08_ TL08_A	I _{IO}	— —	5.0 —	100 —	— —	5.0 5.0	200 100	pA
Input Bias Current (V _{CM} = 0) (Note 4) TL08_ TL08_A	I _{IB}	— —	30 —	200 —	— —	30 30	400 200	pA
Input Resistance	r _i	—	10 ¹²	—	—	10 ¹²	—	Ω
Common Mode Input Voltage Range TL08_ TL08_A	V _{ICR}	±11 —	+15, -12 —	— —	±10 ±11	+15, -12 +15, -12	— —	V
Large-Signal Voltage Gain (V _O = ±10 V, R _L ≥ 2.0 k) TL08_ TL08_A	A _{VOL}	25 —	150 —	— —	25 50	150 150	— —	V/mV
Output Voltage Swing (Peak-to-Peak) (R _L = 10 k)	V _O	24	28	—	24	28	—	V
Common Mode Rejection Ratio (R _S ≤ 10 k) TL08_ TL08_A	CMRR	80 —	100 —	— —	70 80	100 100	— —	dB
Supply Voltage Rejection Ratio (R _S ≤ 10 k) TL08_ TL08_A	PSRR	80 —	100 —	— —	70 80	100 100	— —	dB
Supply Current (Each Amplifier)	I _D	—	1.4	2.8	—	1.4	2.8	mA
Unity Gain Bandwidth	BW	—	4.0	—	—	4.0	—	MHz

TL081, TL082, TL084

ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = +25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	TL08_M			TL08_C TL08_AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Slew Rate (See Figure 1) $V_{in} = 10\text{ V}$, $R_L = 2.0\text{ k}$, $C_L = 100\text{ pF}$	SR	8.0	13	—	—	13	—	$\text{V}/\mu\text{s}$
Rise Time (See Figure 1)	t_r	—	0.1	—	—	0.1	—	μs
Overshoot Factor $V_{in} = 20\text{ mV}$, $R_L = 2.0\text{ k}$, $C_L = 100\text{ pF}$	—	—	10	—	—	10	—	%
Equivalent Input Noise Voltage $R_S = 100\ \Omega$, $f = 1000\text{ Hz}$	e_n	—	25	—	—	25	—	$\text{nV}/\sqrt{\text{Hz}}$
Channel Separation $A_V = 100$	—	—	120	—	—	120	—	dB

ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = T_{low}$ to T_{high} [Note 3])

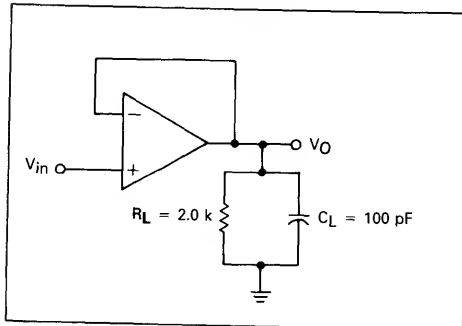
Characteristic	Symbol	TL08_M			TL08_C TL08_AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10\text{ k}$, $V_{CM} = 0$) TL081, TL082 TL084 TL08_A	V_{IO}	— — —	— — —	9.0 15 —	— — —	— — —	20 20 7.5	mV
Input Offset Current ($V_{CM} = 0$) (Note 4) TL08_— TL08_A	I_{IO}	— —	— —	20 —	— —	— —	5.0 3.0	nA
Input Bias Current ($V_{CM} = 0$) (Note 4) TL08_— TL08_A	I_{IB}	— —	— —	50 —	— —	— —	10 7.0	nA
Large-Signal Voltage Gain ($V_O = \pm 10\text{ V}$, $R_L \geq 2.0\text{ k}$) TL08_— TL08_A	A_{VOL}	15 —	— —	— —	15 25	— —	— —	V/mV
Output Voltage Swing (Peak-to-Peak) ($R_L \geq 10\text{ k}$) ($R_L \geq 2.0\text{ k}$)	V_O	24 20	— —	— —	24 20	— —	— —	V

NOTES (continued):

3. $T_{low} = -55^\circ\text{C}$ for TL081M, TL082M, TL084M $T_{high} = +125^\circ\text{C}$ for TL081M, TL082M, TL084M
 $= 0^\circ\text{C}$ for TL081C, TL081AC
 $= +70^\circ\text{C}$ for TL081C, TL081AC
TL082C, TL082AC
TL084C, TL084AC

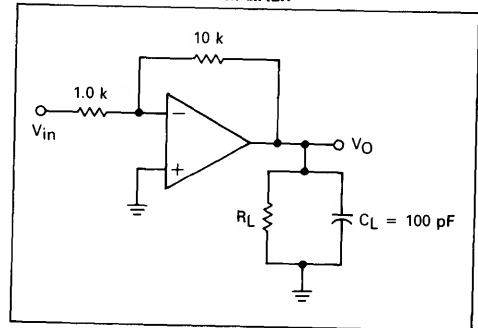
4. Input Bias currents of JFET input op amps approximately double for every 10°C rise in Junction Temperature as shown in Figure 3. To maintain Junction Temperature as close to ambient temperatures as possible, pulse techniques must be used during test.

FIGURE 1 — UNITY GAIN VOLTAGE FOLLOWER

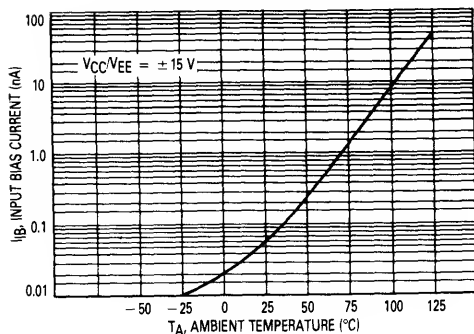


TEST CIRCUITS

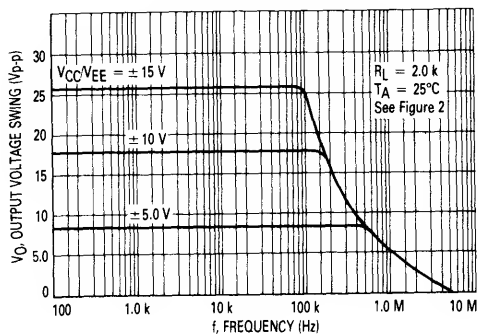
FIGURE 2 — INVERTING GAIN OF 10 AMPLIFIER



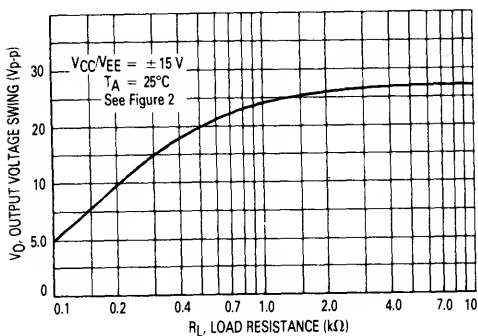
**FIGURE 3 — INPUT BIAS CURRENT
versus TEMPERATURE**



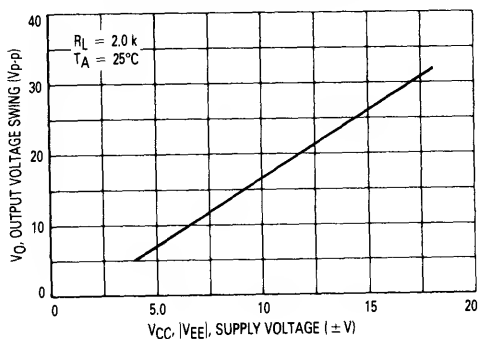
**FIGURE 4 — OUTPUT VOLTAGE SWING
versus FREQUENCY**



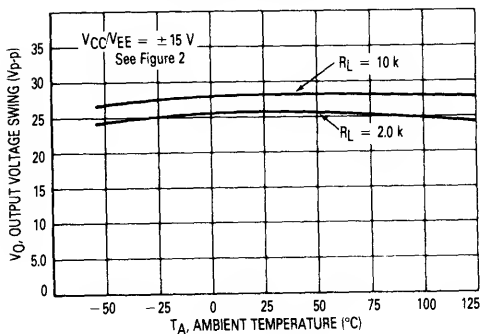
**FIGURE 5 — OUTPUT VOLTAGE SWING
versus LOAD RESISTANCE**



**FIGURE 6 — OUTPUT VOLTAGE SWING
versus SUPPLY VOLTAGE**



**FIGURE 7 — OUTPUT VOLTAGE SWING
versus TEMPERATURE**



**FIGURE 8 — SUPPLY CURRENT PER AMPLIFIER
versus TEMPERATURE**

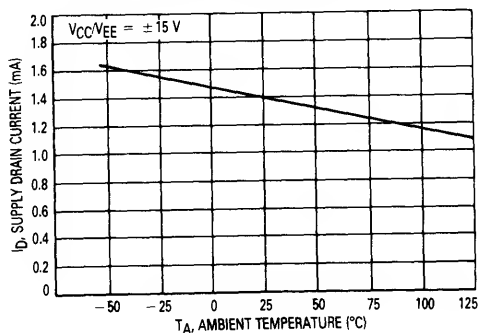


FIGURE 9 — LARGE-SIGNAL VOLTAGE GAIN AND PHASE SHIFT versus FREQUENCY

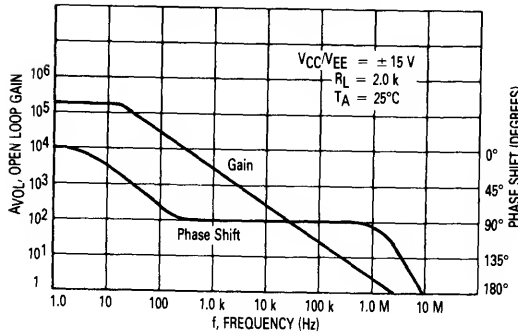


FIGURE 10 — LARGE-SIGNAL VOLTAGE GAIN versus TEMPERATURE

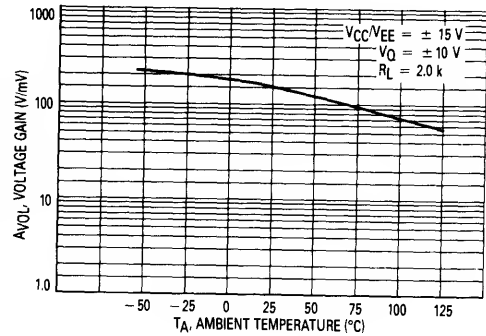


FIGURE 11 — NORMALIZED SLEW RATE versus TEMPERATURE

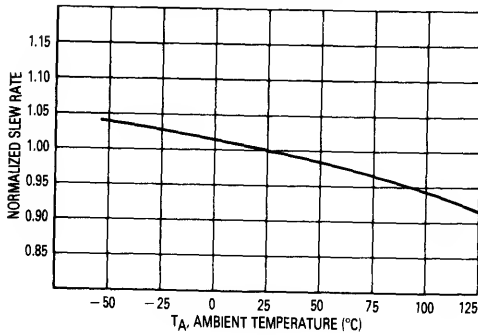


FIGURE 12 — EQUIVALENT INPUT NOISE VOLTAGE versus FREQUENCY

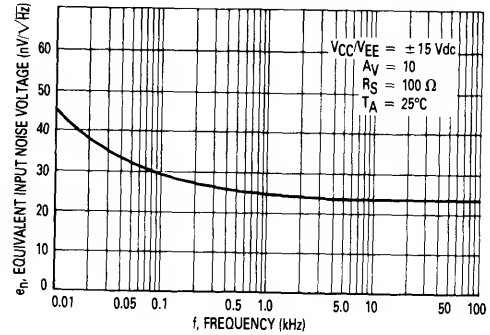
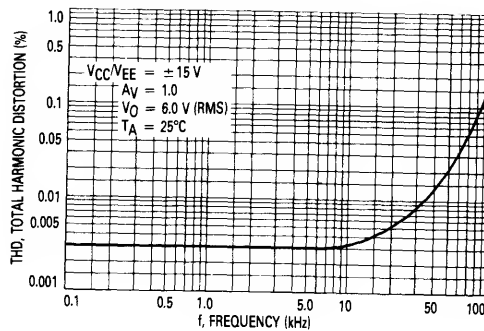
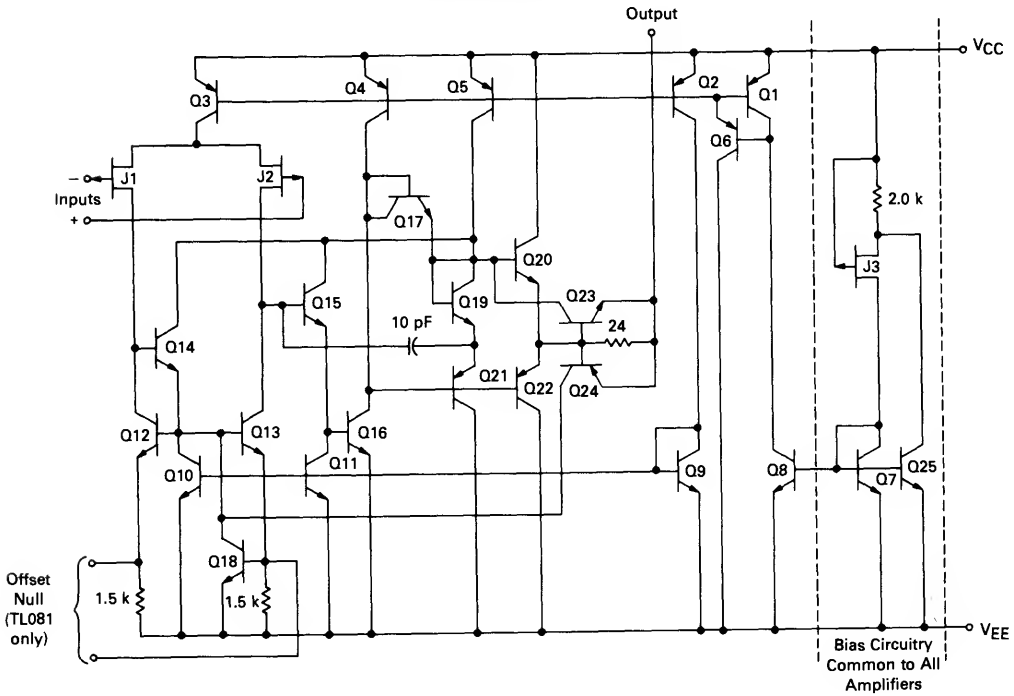


FIGURE 13 — TOTAL HARMONIC DISTORTION versus FREQUENCY



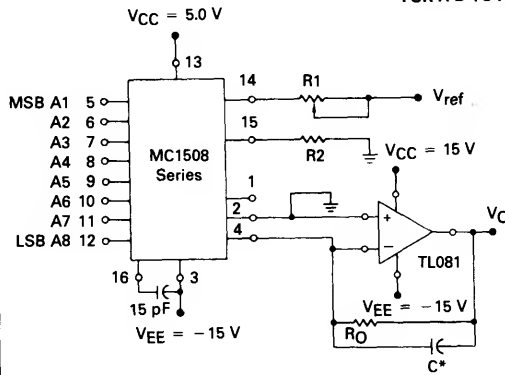
TL081, TL082, TL084

REPRESENTATIVE CIRCUIT SCHEMATIC (Each Amplifier)



TYPICAL APPLICATIONS

FIGURE 14 — OUTPUT CURRENT TO VOLTAGE TRANSFORMATION
FOR A D-TO-A CONVERTER



Settling time to within $\frac{1}{2}$ LSB (± 19.5 mV) is approximately $4.0 \mu\text{s}$ from the time all bits are switched.

*The value of C may be selected to minimize overshoot and ringing ($C \approx 68$ pF).

Theoretical V_0

$$V_0 = \frac{V_{\text{ref}}}{R_1} (R_0) \left[\frac{A_1}{2} + \frac{A_2}{4} + \frac{A_3}{8} + \frac{A_4}{16} + \frac{A_5}{32} + \frac{A_6}{64} + \frac{A_7}{128} + \frac{A_8}{256} \right]$$

Adjust V_{ref} , R_1 or R_0 so that V_0 with all digital inputs at high level is equal to 9.961 volts.

$$\begin{aligned} V_{\text{ref}} &= 2.0 \text{ Vdc} \\ R_1 &= R_2 \approx 1.0 \text{ k}\Omega \\ R_0 &= 5.0 \text{ k}\Omega \end{aligned}$$

$$\begin{aligned} V_0 &= \frac{2.0 \text{ V}}{1.0 \text{ k}} (5.0 \text{ k}) \left[\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256} \right] \\ &= 10 \text{ V} \left[\frac{255}{256} \right] = 9.961 \text{ V} \end{aligned}$$

FIGURE 15 — POSITIVE PEAK DETECTOR

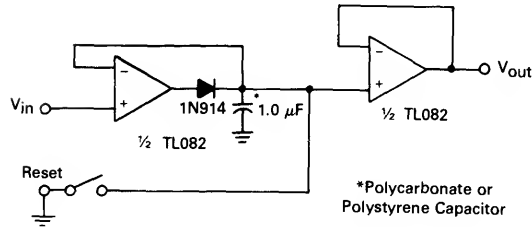
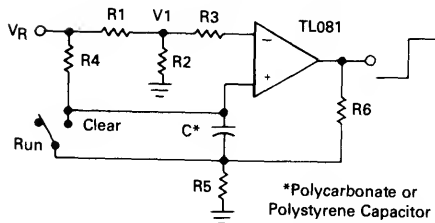
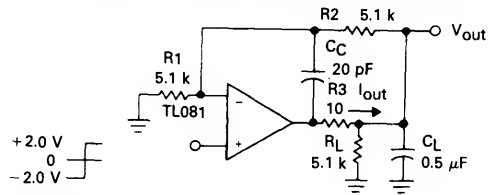


FIGURE 16 — LONG INTERVAL RC TIMER



Time (t) = $R_4 C \ln(V_R/V_R - V_1)$, $R_3 = R_4$, $R_5 = 0.1 R_6$
 If $R_1 = R_2$: $t = 0.693 R_4 C$
 Design Example: 100 Second Timer
 $V_R = 10 \text{ V}$ $C = 1.0 \mu\text{F}$ $R_3 = R_4 = 144 \text{ M}$
 $R_6 = 20 \text{ k}$ $R_5 = 2.0 \text{ k}$ $R_1 = R_2 = 1.0 \text{ k}$

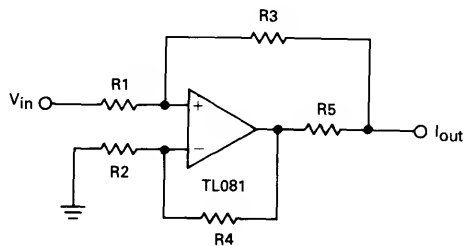
FIGURE 17 — ISOLATING LARGE CAPACITIVE LOADS



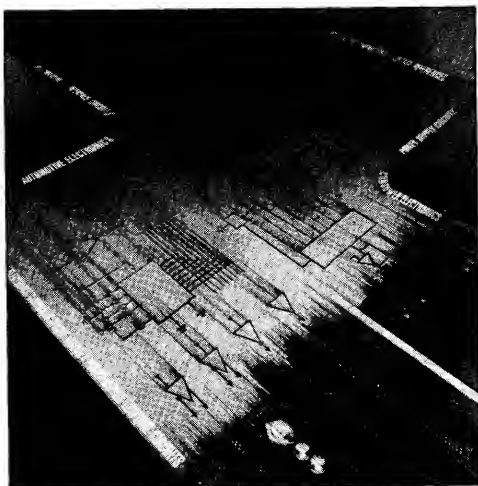
- Overshoot < 10%
- $t_s = 10 \mu\text{s}$
- When driving large C_L , the V_{out} slew rate is determined by C_L and $I_{out(max)}$:

$$\frac{\Delta V_{out}}{\Delta t} = \frac{I_{out}}{C_L} \approx \frac{0.02}{0.5} \text{ V}/\mu\text{s} = 0.04 \text{ V}/\mu\text{s} \text{ (with } C_L \text{ shown)}$$

FIGURE 18 — VOLTAGE CONTROLLED CURRENT SOURCE



If R_1 through $R_4 \gg R_5$ then $I_{out} = \frac{V_{in}}{R_5}$



In Brief . . .

In most electronic systems some form of voltage regulation is required. Yesterday the task of voltage regulator design was tediously accomplished with discrete devices, and the results were quite often complex and costly. Today with bipolar monolithic regulators, this task has been reduced considerably. The designer now has a wide choice of fixed, low V_{diff} , adjustable, and tracking series-type regulators.

These devices incorporate many built-in protection features making them virtually immune to the catastrophic failures encountered in older discrete designs.

The Switching Power Supply continues to increase in popularity and is one of the fastest growing markets in the world of power conversion. They offer the designer several important advantages over that of linear series-pass regulators. These advantages include significant advancements in the areas of size and weight reduction, efficiency, and the ability to perform voltage step-up and voltage-inverting. Motorola offers an ever increasing diverse portfolio of full featured switching regulator control circuits which meet the needs of today's modern compact electronic equipment.

Power Supply Circuits

Selector Guide

Linear Voltage Regulators	3-2
Switching Regulators	3-7
Special Switching Regulator	
Controllers	3-9
Power Supervisory	3-10

Alphanumeric Listing	3-13
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Related Application Notes	3-15
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Data Sheets	3-16
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Power Supply Circuits

Linear Voltage Regulators

Fixed Output

These low cost monolithic circuits provide positive and/or negative regulation at currents from 100 mA to 3.0 A. They are ideal for on-card regulation employing current limiting and thermal shutdown. Low V_{diff} devices are offered for battery powered systems.

Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

Fixed-Voltage, 3-Terminal Regulators for Positive or Negative Polarity Power Supplies

Regulator Voltage, Power, Supplies										
V _{out} Volts	Tol.† Volts	I _O mA Max	Device Positive Output	Device Negative Output	V _{in} Min/Max	Regline mV	Regload mV	ΔV _O /ΔT mV/°C Typ	Package Suffix	
5.0	± 0.5	100	LM2931-5.0	—	5.6/40	30	50	1.0	Z, T	
	± 0.25		MC78L05C	MC79L05C	6.7/30	200	60		P, G	
			LM2931A-5.0	—	5.6/40	30	50		Z, T	
			MC78L05AC	MC79L05AC	6.7/30	150	60		P, G	
		500	MC78M05C	MC79M05C	7.0/35	100	100			G, T
	± 0.5	750,10	LM2935	—	5.6/26	30	50			T/314D
	± 0.4	1500	LM109	—	7.0/35	100	100	1.1	K, H	
			LM209	—		50		1.0		
	± 0.25		LM309	—						
	± 0.35		MC7805*	—	8.0/35			0.6	K	
	± 0.25		MC7805B#	—		100		1.0	T	
			MC7805C	MC7905C	7.0/35				K, T	
	± 0.2		MC7805A*	—	7.5/35	10	50	0.6	K	
			MC7805AC	MC7905AC			100		K, T	
	± 0.25		LM140-5*	—	7.0/35	50	50		K	
	± 0.2		LM140A-5*	—		10	25			
	± 0.25		LM340-5	—		50	50		K, T	
	± 0.2		LM340A-5	—		10	25			
	± 0.1		TL780-05C	—				0.06	KC	
	± 0.25	3000	MC78T05C	—	7.3/35	25	30	0.1	K, T	
	± 0.2		MC78T05AC	—		10	25			

#T_J = -40° to +125°C

†Output Voltage Tolerance for Worst Case

*T_J = -55° to +150°C

(continued)

Fixed Output Voltage Regulators (continued)

V _{out} Volts	Tol.† Volts	I _o mA Max	Device Positive Output	Device Negative Output	V _{in} Min/Max	Regline mV	Regload mV	ΔV _o /ΔT mV/°C Typ	Package Suffix		
5.0	±0.4	3000	LM123*	—	7.5/20	25	100	0.1	K		
	LM223		—	T							
	±0.25		LM323	—		15	50		K		
	±0.2		LM123A	—					T		
			LM223A	—							
			LM323A	—							
5.2	±0.26	1500	—	MC7905.2C	7.2/35	105	105	1.0	T		
6.0	±0.3	500	MC78M06C	—	8.0/35	100	120	0.7	K		
	±0.35	1500	MC7806*	—	9.0/35	60	100		T		
	±0.3		MC7806B#	—		120	120		K, T		
			MC7806C	MC7906C	8.0/35		11		100	T	
	±0.24		MC7806AC	—	8.6/35	K					
	±0.3		LM140-6*	—	8.0/35	60				60	K, T
			LM340-6	—							
8.0	±0.8	100	MC78L08C	—	9.7/30	200	80	—	P, G		
			MC78L08AC	—		175					
	±0.4	500	MC78M08C	—	10/35	100	160		G, T		
			1500	MC7808*	—	11.5/35	80		100	K	
		MC7808B#		—	160		160		T		
		MC7808C		MC7908C		10.5/35	K, T				
		±0.3		MC7808AC	—	10.6/35	13		100	T	
	±0.4	1500	LM140-8*	—	10.5/35	80	80		K		
			LM340-8	—					K, T		
			MC78T08C	—					10.4/35	35	30
	9.0	±0.39	1500	MC7809C	—	11.5/35	50		50	1.0	T
	12	±1.2	100	MC78L12C	MC79L12C	13.7/35	250		100	—	P, G
MC78L12AC				MC79L12AC							
±0.6		500	MC78M12C	MC79M12C	14/35	100	240	1.0	G, T		
			1500	MC7812*	—	15.5/35	120	120	1.5		K
MC7812B#		—		240	240		T				
MC7812C		MC7912C			14.5/35	18	50	K, T			
MC7812A*		—		14.8/35	100			K			
MC7812AC		—						T			
±0.5		LM140-12*		—	14.5/35	120	120	1.5	K		
±0.6		LM140A-12*	—	18					32		K, T
		LM340-12	—								
±0.5		LM340A-12	—	18		32	0.15	KC			
±0.24		TL780-12C	—						5.0		
±0.6		3000	MC78T12C	—		14.5/35	45	30	0.24		K, T
			MC78T12AC	—	18		25				

#T_J = -40° to +125°C

†Output Voltage Tolerance for Worst Case

*T_J = -55° to +150°C

(continued)

Fixed Output Voltage Regulators (continued)

V _{out} Volts	Tol.† Volts	I _O mA Max	Device Positive Output	Device Negative Output	V _{in} Min/Max	Regline mV	Regload mV	ΔV _O /ΔT mV/°C Typ	Package Suffix		
15	± 1.5	100	MC78L15C	MC79L15C	16.7/35	300	150	—	P, G		
	± 0.75	500	MC78L15AC	MC79L15A	17/35	100	300	1.0	G, T		
			MC78M15C	MC79M15C		150	150		K		
			MC7815*	—		300	300		T		
			MC7815B#	—			K, T				
	± 0.6	3000	MC7815C	MC7915C	17.5/35	22	50	0.18	K		
			MC7815A*	—	17.9/35		100		K, T		
			MC7815AC	—	17.5/35	150	150		K		
			LM140-15*	—		22	35		K, T		
	LM340-15		—	150		150					
	LM340A-15		—	22		35					
	± 0.75		TL780-15C	—	15	60	0.3		KC		
	± 0.6		MC78T15C	—	55	30			K, T		
	± 0.3		MC78T15AC	—	22	25					
	18		± 1.8	100	MC78L18C	MC79L18C	19.7/35		325	170	—
± 0.9			MC78L18AC		MC79L18AC						
± 0.7			500	MC78M18C	—	20/35	100		360	1.0	G, T
		1500	MC7818*	—	22/35	180	180	2.3	K		
			MC7818B#	—		360	360		T		
			MC7818C	MC7918C	21/35	31	100		K, T		
MC7818AC			—	180		180	T				
± 0.9		LM340-18	—								
20	± 1.0	500	MC78M20C	—	22/40	10	400	1.1	G, T		
24	± 2.4	100	MC78L24C	MC79L24C	25.7/40	350	200	—	P		
	± 1.2		MC78L24AC	MC79L24AC		300					
	± 1.0	500	MC78M24C	—	26/40	100	480	1.2	G, T		
		1500	MC7824*	—	28/40	240	240	3.0	K		
			MC7824B#	—		480	480		T		
			MC7824C	MC7924C	27/40	36	100		K, T		
	MC7824AC		—	27.3/40	240				240	T	
	± 1.2	LM340-24	—								

#T_J = -40° to +125°C

†Output Voltage Tolerance for Worst Case

*T_J = -55° to +150°C

Adjustable Output Voltage Regulators

Motorola offers a broad line of adjustable output voltage regulators with a variety of output current capabilities. Adjustable voltage regulators provide users the capability of stocking a single integrated circuit provid-

ing a wide range of output voltages for industrial and communications applications. The three-terminal devices require only two external resistors to set the output voltage.

Adjustable Positive Output Regulators

I _O mA Max	Device	Suffix	V _{out} Volts		V _{in} Volts		V _{in} — V _{out} Differ- ential Volts Min	P _D Watts Max		Regulation % V _{out} @ T _A = 25°C Max		T _C V _{out} Typ %/°C	T _J = °C Max	Package		
			Min	Max	Min	Max		T _A = 25°C	T _C = 25°C	Line	Load					
100	LM317L	H,Z	1.2	37	5.0	40	3.0	Internally Limited		0.04	0.5	0.006	125	29,79		
	LM217L#									0.02	0.3	0.004	150			
	LM117L*											0.003				
	LM2931C	T	3.0	24	3.16		0.6	0.15	1.0	—	125	314D				
150	MC1723	CP	2.0	37	9.5	40	3.0	1.25	—	0.1	0.3	0.003	150	646		
		CG						1.0	2.1			0.003		603C		
		G						1.5	—			0.002				
		CL										0.003	175	632		
		L										0.002				
500	LM317M	T	1.2	37	5.0	40	3.0	Internally Limited		0.04	0.5	0.0056	125	221A		
1500	LM317	T	1.2	37	5.0	40	3.0	Internally Limited		0.04	0.5	0.006	125	221A		
	LM317	H, K								0.02	0.3	0.004	150	79, 1		
	LM217#															
	LM117*															
3000	LM350	T	1.2	33	5.0	36	3.0	Internally Limited		0.03	0.5	0.008	125	221A		
	LM350	K								0.01	0.3	0.0057	150	1		
	LM250#															
	LM150*											0.0051				

Adjustable Negative Output Regulators

I _O mA Max	Device	Suffix	V _{out} Volts		V _{in} Volts		V _{in} — V _{out} Differ- ential Volts Min	P _D Watts Max		Regulation % V _{out} @ T _A = 25°C Max		T _C V _{out} Typ %°C	T _J = °C Max	Package
			Min	Max	Min	Max		T _A = 25°C	T _C = 25°C	Line	Load			
500	LM337M	T	− 1.2	− 37	5.0	40	3.0	Internally Limited		0.04	1.0	0.0048	125	221A
1500	LM337	T	− 1.2	− 37	5.0	40	3.0	Internally Limited		0.04	1.0	0.0048	125	221A 79, 1
	LM337									0.02	0.5	0.0034	150	
	LM237 #													
	LM137*											0.0031		

#T_J = -25° to +150°C *T_J = -55° to +150°C

Floating Voltage and Current Regulator

Designed for laboratory type power supplies. Voltage is limited only by the breakdown voltage of associated, external, series-pass transistors.

V _{out} Volts		I _O mA Max	Device	Suffix	V _{aux} Volts		P _D Watts Max	$\Delta V_{ref}/V_{ref}$ %		$\Delta I_L/L$ % Max	TC V _{out} %/°C Typ	Package
Min	Max				Min	Max		Line	Load			
0	*	*	MC1466	L	21	30	0.75	0.015	0.015	0.2	0.01	632

*Dependent on characteristics of external series-pass elements.

Dual ± 15 V Tracking Regulators

Internally, the device is set for ± 15 V, but an external adjustment can change both outputs simultaneously, from 8.0 V to 20 V.

V _{out} Volts		I _O mA Max	V _{in} Volts		Device	Suffix	P _D Watts Max	Regline mV	Regload mV	TC %/°C (T _{low} to T _{high}) Typ	T _A °C	Package
Min	Max		Min	Max								
14.5	15.5	± 100	-17	30	MC1468	G	0.8	10	10	3.0	0 to +75	603C
						L	1.0					632
					MC1568	G	0.8				-55 to +125	603C
						L	1.0					632

Microprocessor Voltage Regulator/Supervisory Circuit

A 5.0 V fixed output with many monitoring functions required in microprocessor-based systems.

V _{out} , V _{ref} Volts		I _{SINK} mA Max	V _{in} Volts		Regline mV Max	Regload mV Max	Device	Suffix	T _A °C	Package
Min	Max		Min	Max						
4.75	5.25	100	7.0	40	40	50	MC34160	P	0 to +70	648C
2.47	2.73	2.0	5.0		20	30	MC33160		-40 to +85	

Switching Regulator Control Circuits

These devices contain the primary building blocks which are required to implement a variety of switching power supplies. The product offerings fall into three major categories consisting of single-ended and double-ended controllers, plus single-ended ICs with on-chip power switch transistors. These circuits operate in voltage, current or resonant modes

and are designed to drive many of the standard switching topologies. The single-ended configurations include buck, boost, flyback and forward converters. The double-ended devices control push-pull, half bridge and full bridge configurations.

Single-Ended Controllers

These single-ended voltage and current mode controllers are designed for use in buck, boost, flyback, and forward converters. They are cost effective in applications that range from 0.1 to 200 watts power output.

I _O mA Max	Minimum Operating Voltage Range Volts	Operating Mode	Reference Volts	Maximum Useful Oscillator Freq. (kHz)	Device	Suffix	T _A °C	Package
250	7.0 to 40	Voltage	5.0 ± 5.0%	200	MC34060	P	0 to +70	646
			L		632			
			MC35060		L	−55 to +125		
500			MC34060A		D		751A	
					P	646		
			MC33060A		D	751A		
		P	646					
	MC35060A	L	−55 to +125	632				
1000	4.2 to 12	Current	1.25 ± 2.0%	300	MC34129	D	0 to +70	751A
						P		646
			MC33129	D	−40 to +85	751A		
			P	646				
	11.5 to 30		5.0 ± 2.0%	500	UC3842A	D	0 to +70	751A
						N		626
	11 to 30		5.0 ± 1.0%		UC2842A	D	−25 to +85	751A
						J		693
					N	626		
	8.2 to 30		5.0 ± 2.0%		UC3843A	D	0 to +70	751A
						N		626
			5.0 ± 1.0%		UC2843A	D	−25 to +85	751A
					J	693		
					N	626		
	11.5 to 30		5.0 ± 2.0%		UC3844	D	0 to +70	751A
						N		626
	11 to 30		5.0 ± 1.0%		UC2844	D	−25 to +85	751A
						J		693
					N	626		
	8.2 to 30		5.0 ± 2.0%		UC3845	D	0 to +70	751A
						N		626
5.0 ± 1.0%		UC2845	D	−25 to +85	751A			
			J		693			
		N	626					

Single-Ended Controllers With On-Chip Power Switch

These monolithic power switching regulators contain all the active functions required to implement standard DC-to-DC converter configurations with a minimum number of external components.

I _O mA Max	Minimum Operating Voltage Range Volts	Operating Mode	Reference Volts	Maximum Useful Oscillator Freq. (kHz)	Device	Suffix	T _A °C	Package
1500	2.5 to 40	Voltage	1.25 ± 5.2%#	100	μA78S40	PC	0 to +70	648
						DC		620
						PV	-40 to +85	648
						DM		620

#Tolerance applies over the specified operating temperature range.

(continued)

SINGLE-ENDED CONTROLLERS WITH ON-CHIP POWER SWITCH (continued)

I_O mA Max	Minimum Operating Voltage Range Volts	Operating Mode	Reference Volts	Maximum Useful Oscillator Freq. (kHz)	Device	Suffix	T_A °C	Package
1500	2.5 to 40	Voltage	$1.25 \pm 5.6\% \#$	100	MC34063	P1	0 to +70	626
						U		693
					MC33063	P1	-40 to +85	626
						U		693
			MC35063		U	~55 to +125		
			$1.25 \pm 2.0\%$		MC34063A	D	0 to +70	751
						P1		626
					MC33063A	D	-40 to +85	751
						P1		626
			3400				$1.25 \pm 2.0\%$ and $5.05 \pm 3.0\%$	
MC34163	P	0 to +70		648C				
MC33163		-40 to +85						
3500†	6.8 to 40		$5.05 \pm 2.0\%$	72 Internally Fixed	MC34166	T	0 to +70	314D
					MC33166		-40 to +85	

Double-Ended Controllers

These double-ended voltage and resonant mode controllers are designed for use in push-pull, half-bridge, and full-bridge converters. They are cost effective in applications that range from 100 to 2000 watts power output.

I_O mA Max	Minimum Operating Voltage Range Volts	Operating Mode	Reference Volts	Maximum Useful Oscillator Freq. (kHz)	Device	Suffix	T_A °C	Package			
500	7.0 to 40	Voltage	$5.0 \pm 5.0\% \#$	200	TL494	CN	0 to +70	648			
						CJ		620			
						IN	-25 to +85	648			
						IJ		620			
						MJ	-55 to +125				
± 500	8.0 to 40		$5.0 \pm 1.5\%$	300	TL594	CN	0 to +70	648			
						IN	-25 to +85				
			$5.1 \pm 2.0\%$	400	SG3525A	N	0 to +70	648			
						J		620			
			$5.1 \pm 1.0\%$		SG2525A	N	-25 to +85	648			
						J		620			
			$5.1 \pm 2.0\%$		SG1525A	J	-55 to +125				
						SG3527A		N	0 to +70	648	
			$5.1 \pm 1.0\%$		SG2527A	N	-25 to +85	648			
						J		620			
			± 200							J	-55 to +125
$5.0 \pm 2.0\%$					SG3526	N	0 to +125*	707			
						J		726			
$5.0 \pm 1.0\%$					SG2526	N	-25 to +150*	707			
						J		726			
$5.1 \pm 2.0\%$					SG1526	J	-55 to +150*				
						N		648			
± 1500	9.6 to 20				Resonant	$5.1 \pm 2.0\%$	1000	MC34066	DW	0 to +70	751G
									P		648
			MC33066					DW	-40 to +85	751G	
		P		648							

#Tolerance applies over the specified operating temperature range.

*Junction Temperature Range.

†Guaranteed minimum, typically 4300 mA.

Special Switching Regulator Controllers

Dual Channel Current Mode Controllers

These high performance dual channel controllers are optimized for off-line AC-to-DC power supplies and DC-to-DC converters in the flyback topology. Applications include desktop computers, peripherals, televisions, games, and various consumer appliances.

I_O mA Max	Minimum Operating Voltage Range Volts	Operating Mode	Reference Volts	Maximum Useful Oscillator Freq. (kHz)	Device	Suffix	T_A °C	Package
± 1000	11 to 15.5	Current	$5.0 \pm 2.0\%$	500	MC34065	DW	0 to +70	751G
						P		648
					MC33065	DW	-40 to +85	751G
						P		648

Universal Microprocessor Power Supply Controller

A versatile power supply control circuit for microprocessor-based systems which is mainly intended for automotive applications and battery powered instruments. The device provides a power-on Reset delay and a Watchdog feature for orderly microprocessor operation.

Regulated Outputs	Output Current mA	Device	VCC Volts		T_A °C	Reference Volts	Key Supervisory Features	Package
			Min	Max				
E ² PROM Programmable Output: 24 Volts (Write Mode) 5.0 Volts (Read Mode)	150 peak	TCA5600, TCF5600	6.0	35	-40 to +75	$2.5 \pm 3.2\%$	MPU Reset and Watchdog Circuit	707
Fixed Linear Output: 5.0 Volts								

Control IC for Line-Isolated Free Running Flyback Converter

Regulates and monitors the switching transistor in power supplies based on the free oscillating flyback converter principle. Provides excellent Switchmode performance in Hi-Fi equipment, active loudspeakers, as well as applications in TV receivers and video recorders.

I_O mA Max	Minimum Operating Voltage Range Volts	Operating Mode	Reference Volts	Maximum Useful Oscillator Freq. (kHz)	Device	Suffix	T_A °C	Package
± 1500	12.3 to 20	Voltage	$4.2 \pm 5.0\%$	100	TDA4601	—	-15 to +85	762

Power Supervisory Circuits

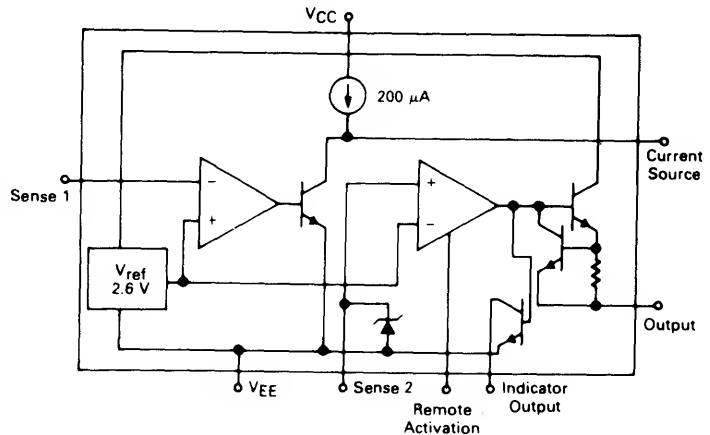
A variety of Power Supervisory Circuits are offered. Overvoltage sensing circuits which drive "crowbar" SCR's are provided in several configurations from a low cost three-terminal version to 8-pin devices which provide pin-programmable trip-voltages or additional features such as an indicator output drive and remote activation capability. An over-under-voltage protection circuit is also offered.

Overvoltage "Crowbar" Sensing Circuit

MC3523U — $T_A = -55^\circ$ to $+125^\circ\text{C}$, Case 693

MC3423P1, U — $T_A = 0^\circ$ to $+70^\circ\text{C}$, Case 626, 693

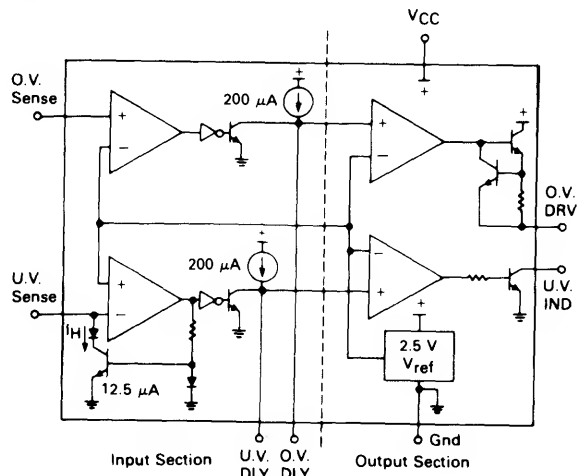
This device can protect sensitive circuitry from power supply transients or regulator failure when used with an external "Crowbar" SCR. The device senses voltage and compares it to an internal 2.6 V reference. Over-voltage trip is adjustable by means of an external resistive voltage divider. A minimum duration before trip is programmable with an external capacitor. Other features include a 300 mA high current output for driving the gate of a "Crowbar" SCR, an open-collector indicator output and remote activation capability.



Over/Undervoltage Protection Circuit

MC3425P1 — $T_A = 0^\circ$ to $+70^\circ\text{C}$, Case 626

The MC3425 is a power supply supervisory circuit containing all the necessary functions required to monitor over and undervoltage fault conditions. This device features dedicated over and undervoltage sensing channels with independently programmable time delays. The overvoltage channel has a high current Drive Output for use in conjunction with an external SCR "Crowbar" for shutdown. The undervoltage channel input comparator has hysteresis which is externally programmable, and an open-collector output for fault indication.



Undervoltage Sensing Circuit

MC34064P-5, D-5 — $T_A = 0^\circ$ to $+70^\circ\text{C}$, Case 29, 751

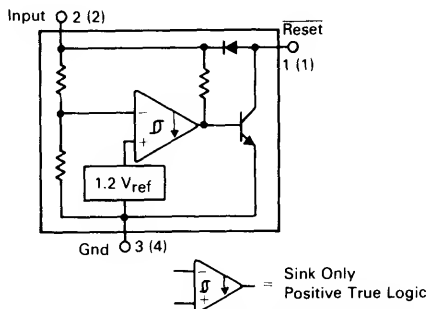
MC33064P-5, D-5 — $T_A = -40^\circ$ to $+85^\circ\text{C}$, Case 29, 751

MC34164P-5, D-5 — $T_A = 0^\circ$ to $+70^\circ\text{C}$, Case 29, 751

MC33164P-5, D-5 — $T_A = -40^\circ$ to $+85^\circ\text{C}$, Case 29, 751

The MC34064/MC34164 is a family of undervoltage sensing circuits specifically designed for use as reset controllers in microprocessor-based systems. They offer the designer an economical solution for low voltage detection with a single external resistor. Both parts feature a trimmed bandgap reference, and a comparator with precise thresholds and built-in hysteresis to prevent erratic reset operation. The MC34064 has a threshold voltage of 4.6 V, while the MC34164 threshold is at 4.3 V, and features a larger hysteresis window. The open collector reset outputs are capable of sinking in excess of 10 mA (MC34064) and 7.0 mA (MC34164). Operation is guaranteed down to 1.0 volt input with low standby current. The MC34164 is specifically designed for battery powered applications where low bias current (one-tenth of the MC34064's) is an important characteristic.

Applications include direct monitoring of the 5.0 volt MPU/logic power supply used in appliance, automotive, consumer, and industrial equipment.



Pin numbers adjacent to terminals are for the 3 pin TO-92 package. Pin numbers in parenthesis are for the D suffix SO-8 package.

Microprocessor Voltage Regulator and Supervisory Circuit

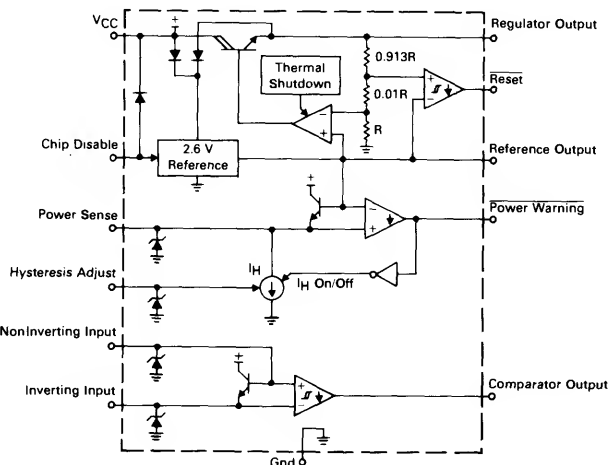
MC34160P — $T_A = 0^\circ$ to $+70^\circ\text{C}$, Case 648C

MC33160P — $T_A = -40^\circ$ to $+85^\circ\text{C}$, Case 648C

The MC34160 Series is a voltage regulator and supervisory circuit containing many of the necessary monitoring functions required in microprocessor based systems. It is specifically designed for appliance and industrial applications offering the designer a cost effective solution with minimal external components. These integrated circuits feature a 5.0 V, 100 mA regulator with short circuit current limiting, pinned out 2.6 V bandgap reference, low voltage reset comparator, power warning comparator with programmable hysteresis, and an uncommitted comparator ideally suited for microprocessor line synchronization.

Additional features include a chip disable input for low standby current, and internal thermal shutdown for over temperature protection.

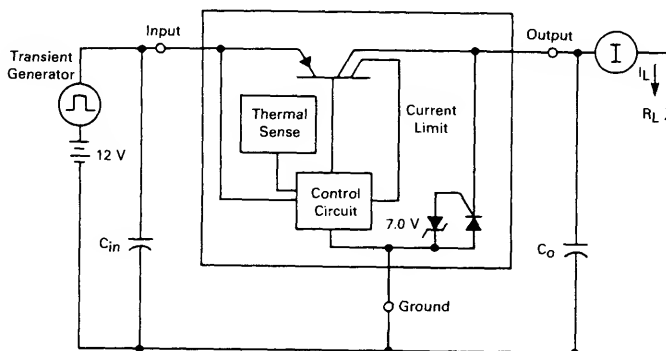
These devices are contained in a 16 pin dual-in-line heat tab plastic package for improved thermal conduction.



Series Switch Transient Protection Circuit

MC3397T — $T_J = -40^\circ$ to $+125^\circ\text{C}$, Case 221A

This device acts as a saturated series pass element with a very low voltage drop for load currents in excess of 750 mA. In the event of an over voltage condition (≥ 17.5 V typically) or high voltage transient of either positive or negative polarity, the MC3397T instantaneously switches to an open circuit (OFF) state, interrupting power to the load and protecting the load during this potentially destructive condition. The device will immediately recover to an ON state when supply voltages fall within the normal operating range.



POWER SUPPLY CIRCUITS

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UC3844	High Performance Current Mode Controller	3-377
UC3845	High Performance Current Mode Controller	3-377
μA78S40	Universal Switching Regulator Subsystem	3-390

Special Switching Regulator Controllers

Device	Function	Page
MC33065	High Performance Dual Channel Current Mode Controller	3-232
MC34065	High Performance Dual Channel Current Mode Controller	3-232
TCA5600	Universal Microprocessor Power Supply Controller	3-319
TCF5600	Universal Microprocessor Power Supply Controller	3-319
TDA4601	Flyback Converter Regulator Control Circuit	3-330

Power Drivers

Device	Function	Page
MC33151	High Speed Dual MOSFET Driver	3-266
MC33152	High Speed Dual MOSFET Driver	3-274
MC33153	High Speed Dual MOSFET Driver	3-274
MC34151	High Speed Dual MOSFET Driver	3-266
MC34152	High Speed Dual MOSFET Driver	3-274
MC34153	High Speed Dual MOSFET Driver	3-274

Power Supervisory

Device	Function	Page
MC3397T	Transient Suppressor	See Chapter 10
MC3423	Overvoltage Sensing Circuit	3-121
MC3425	Power Supply Supervisory/Over-Under-Voltage Protection Circuit	3-127
MC3523	Overvoltage Sensing Circuit	3-121
MC33064	Pin-Programmable Overvoltage Sensing Circuit	3-227
MC33160	Microprocessor Voltage Regulator and Supervisory Circuit	3-279
MC33164	Micropower Undervoltage Sensing Circuit	3-297
MC34064	Pin-Programmable Overvoltage Sensing Circuit	3-227
MC34160	Microprocessor Voltage Regulator and Supervisory Circuit	3-279
MC34164	Micropower Undervoltage Sensing Circuit	3-297

RELATED APPLICATION NOTES

Application Note	Title	Related Device
AN703	Designing Digitally-Controlled Power Supplies	MC1466, MC1723
AN719	A New Approach To Switching Regulators	General
AN1040	Mounting Techniques for Power Semiconductors	LM317, LM337, MC7800, MC78M00, MC7900, MC79M00
AN920R2	Theory and Applications of the MC34063 and μ A78S40 Switching Regulator Control Circuits	MC34063, μ A78S40
AN976	A New High Performance Current-Mode Controller Teams Up with Current Sensing Power MOSFETs	MC34129
AN983	A Simplified Power Supply Design Using the TL494 Control Circuit	TL494
ANE002	130 W Ringing Choke Power Supply Using TDA4601	TDA4601,B
ANE424	50 W Current Mode Controlled Offline Switchmode Power Supply	UC3842A, UC2842A UC3843A, UC2843A
HB206 Rev 3	Linear Switchmode Regulator Handbook	Various

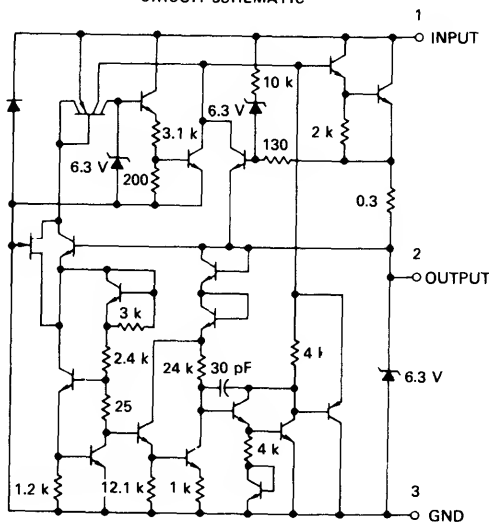
**POSITIVE THREE-TERMINAL
FIXED VOLTAGE REGULATORS**

A versatile positive fixed +5.0-volt regulator designed for easy application as an on-card, local voltage regulator for digital logic systems. Current limiting and thermal shutdown are provided to make the units extremely rugged.

In most applications only one external component, a capacitor, is required in conjunction with the LM109 Series devices. Even this component may be omitted if the power-supply filter is not located an appreciable distance from the regulator.

- High Maximum Output Current — Over 1.0 Ampere in K Suffix Package — Over 200 mA in H Suffix Package
- Minimum External Components Required
- Internal Short-Circuit Protection
- Internal Thermal Overload Protection
- Excellent Line and Load Transient Rejection
- Designed for Use with Popular MDTL and MTTL Logic

CIRCUIT SCHEMATIC

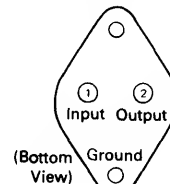


LM109
LM209
LM309

**POSITIVE
VOLTAGE REGULATORS**



**K SUFFIX
METAL PACKAGE
CASE 1**



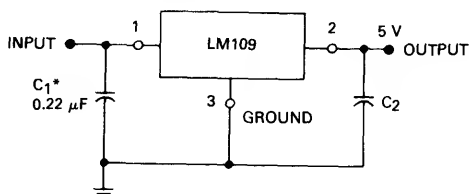
**H SUFFIX
METAL PACKAGE
CASE 79**

CASE IS GROUND

ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
LM109H	$T_J = -55^{\circ}\text{C to } +150^{\circ}\text{C}$	Metal Can
LM109K	$T_J = -55^{\circ}\text{C to } +150^{\circ}\text{C}$	Metal Power
LM209H	$T_J = -25^{\circ}\text{C to } +150^{\circ}\text{C}$	Metal Can
LM209K	$T_J = -25^{\circ}\text{C to } +150^{\circ}\text{C}$	Metal Power
LM309H	$T_J = 0^{\circ}\text{C to } +125^{\circ}\text{C}$	Metal Can
LM309K	$T_J = 0^{\circ}\text{C to } +125^{\circ}\text{C}$	Metal Power

**TYPICAL APPLICATION
FIXED 5.0 V REGULATOR**



* Required if regulator is located an appreciable distance from power supply filter. Although no output capacitor is needed for stability, it does improve transient response.

LM109, LM209, LM309

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	V_{in}	35	Vdc
Power Dissipation	P_D	Internally Limited	
Junction Temperature Range	T_J	-55 to +150 -25 to +150 0 to +150	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Lead Temperature (soldering, $t = 60$ s)	T_S	300	°C

3

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	LM109/LM209 ¹			LM309 ²			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	4.7	5.05	5.3	4.8	5.05	5.2	Vdc
Input Regulation ($T_J = +25^\circ\text{C}$) $7.0 \leq V_{in} \leq 25$ V	Reg _{line}	—	4.0	50	—	4.0	50	mV
Load Regulation ($T_J = +25^\circ\text{C}$) Case 1-03 $5.0 \text{ mA} \leq I_O \leq 1.5$ A Case 79-03 $5.0 \text{ mA} \leq I_O \leq 0.5$ A	Reg _{load}	—	50 20	100 50	—	50 20	100 50	mV
Output Voltage Range $7.0 \text{ V} \leq V_{in} \leq 25$ V $5.0 \text{ mA} \leq I_O \leq I_{max}$, $P \leq P_{max}$	V_O	4.6	—	5.4	4.75	—	5.25	Vdc
Quiescent Current ($7.0 \text{ V} \leq V_{in} \leq 25$ V) Quiescent Current Change ($7.0 \text{ V} \leq V_{in} \leq 25$ V) $5.0 \text{ mA} \leq I_O \leq I_{max}$	I_B ΔI_B	— —	5.2 —	10 0.5	— —	5.2 —	10 0.5	mAdc 0.8
Output Noise Voltage ($T_A = +25^\circ\text{C}$) $10 \text{ Hz} \leq f \leq 100 \text{ kHz}$	V_N	—	40	—	—	40	—	μV
Long Term Stability	S	—	—	10	—	—	20	mV
Thermal Resistance, Junction to Case ³ Case 1-03 Case 79-03	θ_{JC}	— —	3.0 15	— —	— —	3.0 15	— —	°C/W

NOTES:

- Unless otherwise specified, these specifications apply for $-55^\circ\text{C} \leq T_J \leq +150^\circ\text{C}$ ($-25^\circ\text{C} \leq T_J \leq +150^\circ\text{C}$ for the LM209). For Case 79-03 $V_{in} = 10$ V, $I_O = 0.1$ A, $I_{max} = 0.2$ A and $P_{max} = 2.0$ W. For Case 1-03 $V_{in} = 10$ V, $I_O = 0.5$ A, $I_{max} = 1.0$ A and $P_{max} = 20$ W.
- Unless otherwise specified, these specifications apply for $0^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$, $V_{in} = 10$ V. For Case 79-03 $I_O = 0.1$ A, $I_{max} = 0.2$ A and $P_{max} = 2.0$ W. For Case 1-03 $I_O = 0.5$ A, $I_{max} = 1.0$ A and $P_{max} = 20$ W.
- Without a heat sink, the thermal resistance of the Case 79-03 package is about 150°C/W , while that of the Case 1-03 package is approximately 35°C/W . With a heat sink, the effective thermal resistance can only approach the values specified, depending on the efficiency of the heat sink.

TYPICAL CHARACTERISTICS

($V_{in} = 10$ V, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 1 — MAXIMUM AVERAGE POWER DISSIPATION
(LM109K, LM209K)

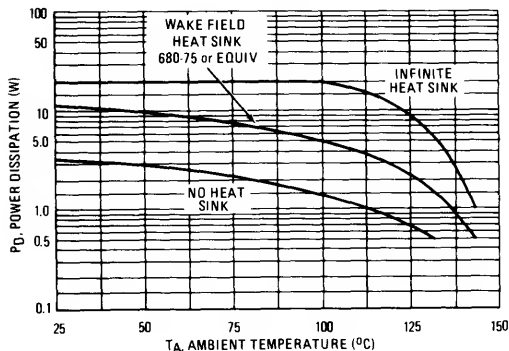
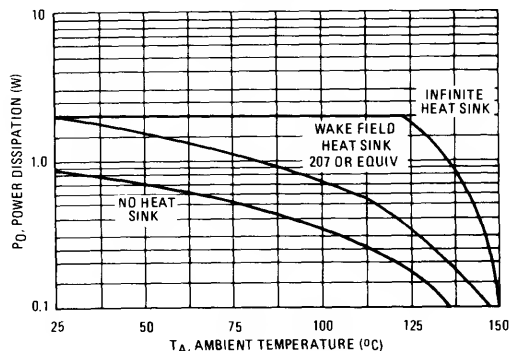


FIGURE 2 — MAXIMUM AVERAGE POWER DISSIPATION
(LM109H, LM209H)



LM109, LM209, LM309

TYPICAL CHARACTERISTICS (continued)

($V_{in} = 10\text{ V}$, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 3 – MAXIMUM AVERAGE POWER DISSIPATION (LM309K)

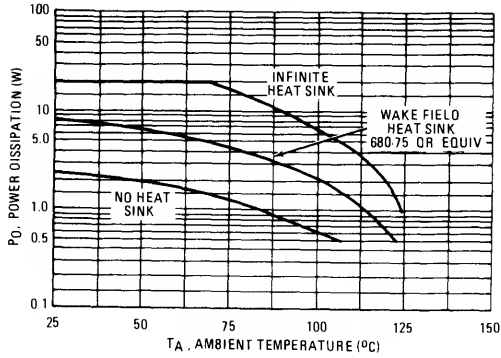


FIGURE 4 – MAXIMUM AVERAGE POWER DISSIPATION (LM309H)

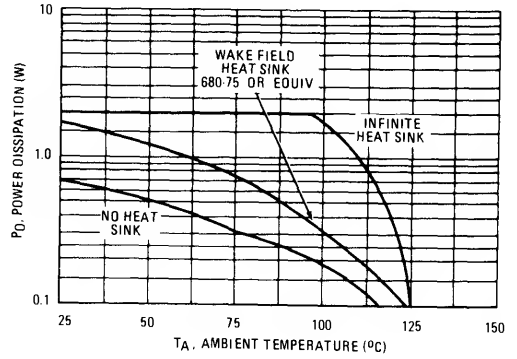


FIGURE 5 – OUTPUT IMPEDANCE versus FREQUENCY

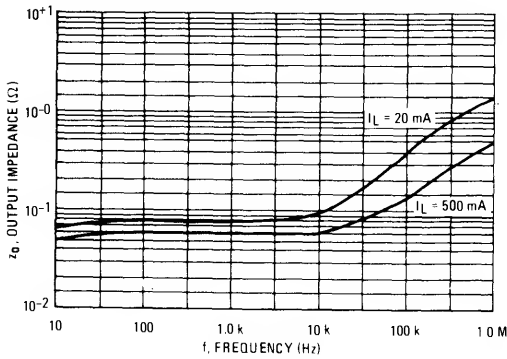


FIGURE 6 – PEAK OUTPUT CURRENT (K PACKAGE)

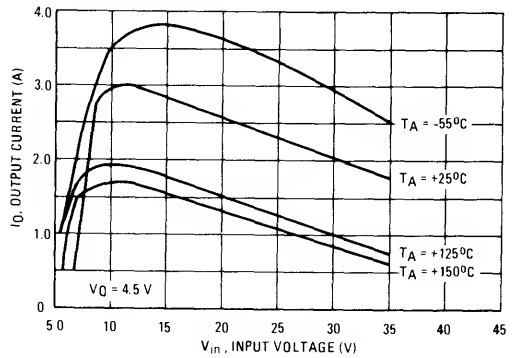


FIGURE 7 – PEAK OUTPUT CURRENT (H PACKAGE)

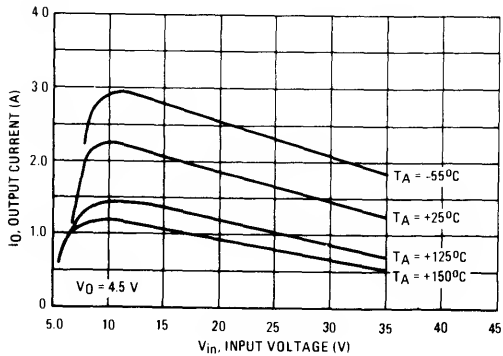
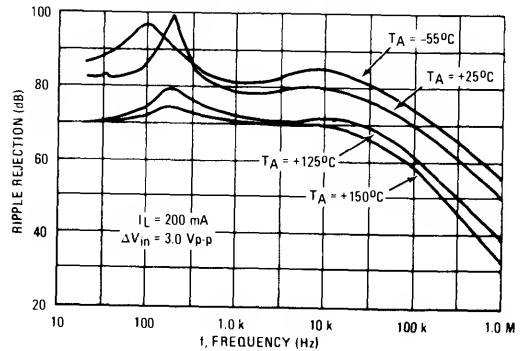


FIGURE 8 – RIPPLE REJECTION



LM109, LM209, LM309

TYPICAL CHARACTERISTICS (continued)

FIGURE 9 – DROPOUT VOLTAGE

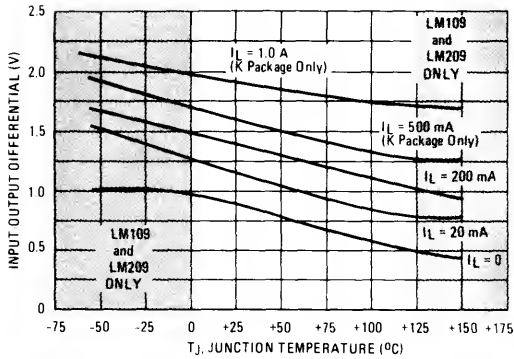


FIGURE 10 – DROPOUT CHARACTERISTIC (K PACKAGE)

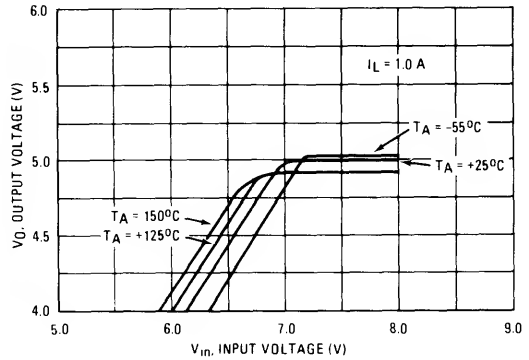


FIGURE 11 – OUTPUT VOLTAGE

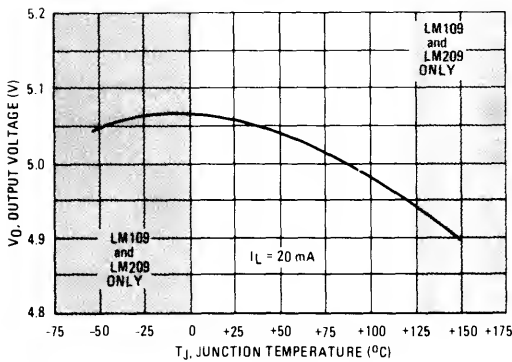


FIGURE 12 – OUTPUT NOISE VOLTAGE

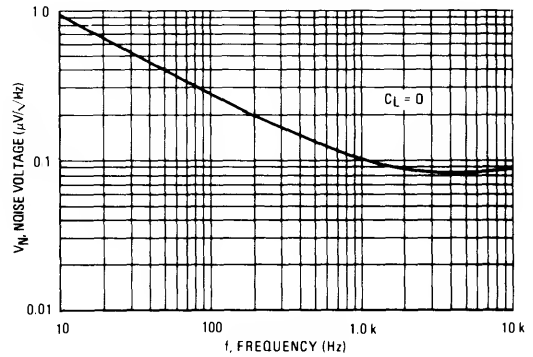


FIGURE 13 – QUIESCENT CURRENT

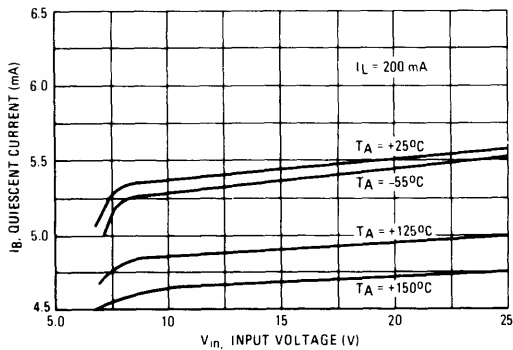
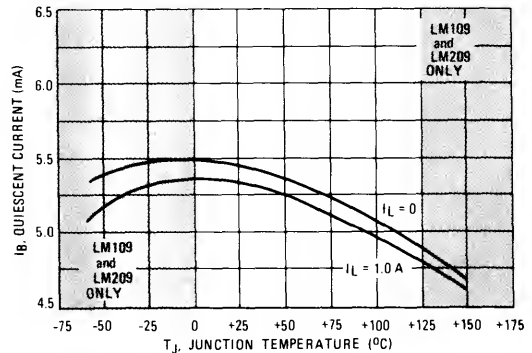


FIGURE 14 – QUIESCENT CURRENT



LM109, LM209, LM309

TYPICAL APPLICATIONS

FIGURE 15 – ADJUSTABLE OUTPUT REGULATOR

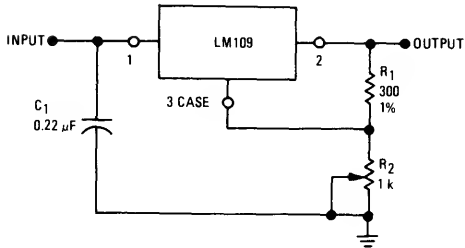


FIGURE 16 – CURRENT REGULATOR

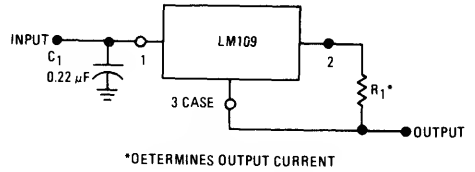


FIGURE 17 – 5.0-VOLT, 3.0-AMPERE REGULATOR
(with plastic boost transistor)

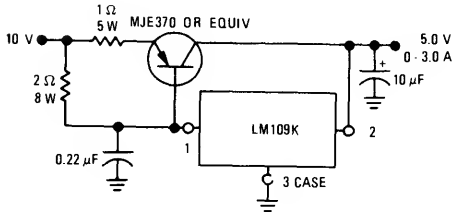


FIGURE 18 – 5.0 VOLT, 4.0-AMPERE TRANSISTOR
(with plastic Darlington boost transistor)

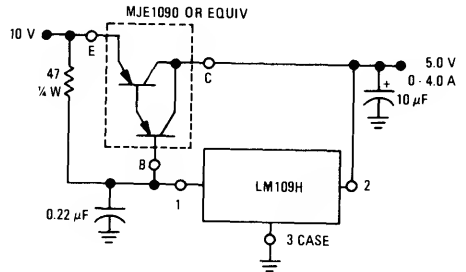


FIGURE 19 – 5.0-VOLT, 10-AMPERE REGULATOR

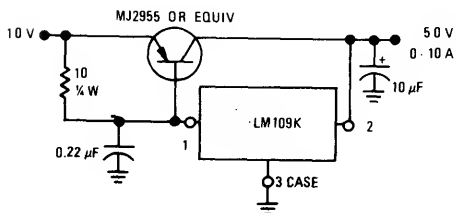
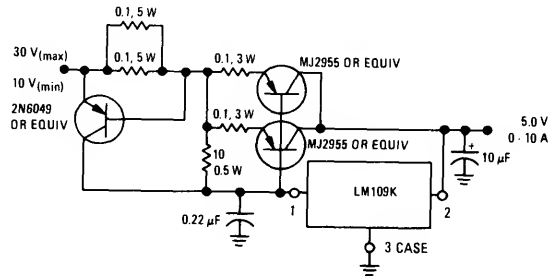


FIGURE 20 – 5.0-VOLT, 10-AMPERE REGULATOR
(with Short-Circuit Current Limiting for
Safe-Area Protection of pass transistors)



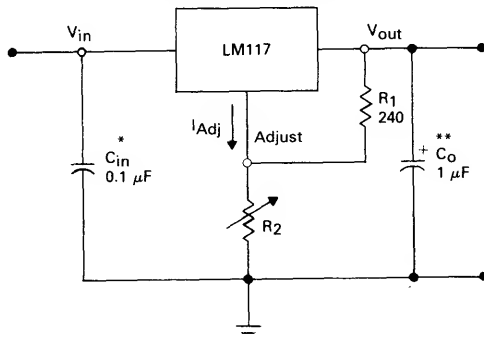
**THREE-TERMINAL ADJUSTABLE
OUTPUT POSITIVE VOLTAGE REGULATORS**

The LM117/217/317 are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 1.5 A over an output voltage range of 1.2 V to 37 V. These voltage regulators are exceptionally easy to use and require only two external resistors to set the output voltage. Further, they employ internal current limiting, thermal shutdown and safe area compensation, making them essentially blow-out proof.

The LM117 series serve a wide variety of applications including local, on card regulation. This device can also be used to make a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM117 series can be used as a precision current regulator.

- Output Current in Excess of 1.5 Ampere in K and T Suffix Packages
- Output Current in Excess of 0.5 Ampere in H Suffix Package
- Output Adjustable between 1.2 V and 37 V
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting Constant with Temperature
- Output Transistor Safe-Area Compensation
- Floating Operation for High Voltage Applications
- Standard 3-lead Transistor Packages
- Eliminates Stocking Many Fixed Voltages

STANDARD APPLICATION



* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_o is not needed for stability, however it does improve transient response.

$$V_{out} = 1.25 V \left(1 + \frac{R_2}{R_1} \right) + I_{Adj} R_2$$

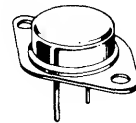
Since I_{Adj} is controlled to less than 100 μA , the error associated with this term is negligible in most applications.

LM117
LM217
LM317

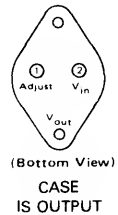
**THREE-TERMINAL
ADJUSTABLE POSITIVE
VOLTAGE REGULATORS**

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**

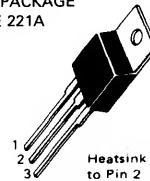
K SUFFIX
METAL PACKAGE
CASE 1



Pins 1 and 2 electrically isolated from case.
Case is third electrical connection.



T SUFFIX
PLASTIC PACKAGE
CASE 221A

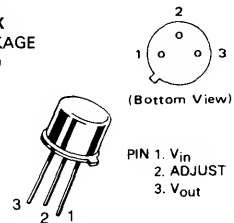


PIN 1. ADJUST
2. V_{out}
3. V_{in}

Heatsink surface connected to Pin 2

H SUFFIX
METAL PACKAGE
CASE 79

CASE IS OUTPUT



ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
LM117H LM117K	$T_J = -55^\circ C$ to $+150^\circ C$	Metal Can Metal Power
LM217H LM217K	$T_J = -25^\circ C$ to $+150^\circ C$	Metal Can Metal Power
LM317H LM317K LM317T	$T_J = 0^\circ C$ to $+125^\circ C$	Metal Can Metal Power Plastic Power
LM317BT#	$T_J = -40^\circ C$ to $+125^\circ C$	Plastic Power

#Automotive temperature range selections are available with special test conditions and additional tests.
Contact your local Motorola sales office for information.

LM117, LM217, LM317

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input-Output Voltage Differential	$V_I - V_O$	40	Vdc
Power Dissipation	P_D	Internally Limited	
Operating Junction Temperature Range LM117 LM217 LM317	T_J	-55 to +150 -25 to +150 0 to +150	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS ($V_I - V_O = 5.0$ V; $I_O = 0.5$ A for K and T packages; $I_O = 0.1$ A for H package; $T_J = T_{low}$ to T_{high} [see Note 1]; I_{max} and P_{max} per Note 2; unless otherwise specified.)

Characteristic	Figure	Symbol	LM117/217			LM317			Unit
			Min	Typ	Max	Min	Typ	Max	
Line Regulation (Note 3) $T_A = 25^\circ\text{C}$, $3.0 \text{ V} \leq V_I - V_O \leq 40 \text{ V}$	1	Regline	—	0.01	0.02	—	0.01	0.04	%/V
Load Regulation (Note 3) $T_A = 25^\circ\text{C}$, $10 \text{ mA} \leq I_O \leq I_{max}$ $V_O \leq 5.0 \text{ V}$ $V_O \geq 5.0 \text{ V}$	2	Regload	— —	5.0 0.1	15 0.3	— —	5.0 0.1	25 0.5	mV %/V _O
Thermal Regulation ($T_A = +25^\circ\text{C}$) 20 ms Pulse	—	—	—	0.02	0.07	—	0.03	0.07	%/W
Adjustment Pin Current	3	I_{Adj}	—	50	100	—	50	100	μA
Adjustment Pin Current Change $2.5 \text{ V} \leq V_I - V_O \leq 40 \text{ V}$ $10 \text{ mA} \leq I_L \leq I_{max}$, $P_D \leq P_{max}$	1,2	ΔI_{Adj}	—	0.2	5.0	—	0.2	5.0	μA
Reference Voltage (Note 4) $3.0 \text{ V} \leq V_I - V_O \leq 40 \text{ V}$ $10 \text{ mA} \leq I_O \leq I_{max}$, $P_D \leq P_{max}$	3	V_{ref}	1.2	1.25	1.3	1.2	1.25	1.3	V
Line Regulation (Note 3) $3.0 \text{ V} \leq V_I - V_O \leq 40 \text{ V}$	1	Regline	—	0.02	0.05	—	0.02	0.07	%/V
Load Regulation (Note 3) $10 \text{ mA} \leq I_O \leq I_{max}$ $V_O \leq 5.0 \text{ V}$ $V_O \geq 5.0 \text{ V}$	2	Regload	— —	20 0.3	50 1.0	— —	20 0.3	70 1.5	mV %/V _O
Temperature Stability ($T_{low} \leq T_J \leq T_{high}$)	3	T_S	—	0.7	—	—	0.7	—	%/V _O
Minimum Load Current to Maintain Regulation ($V_I - V_O = 40 \text{ V}$)	3	I_{Lmin}	—	3.5	5.0	—	3.5	10	mA
Maximum Output Current $V_I - V_O \leq 15 \text{ V}$, $P_D \leq P_{max}$ K and T Packages H Package $V_I - V_O = 40 \text{ V}$, $P_D \leq P_{max}$, $T_A = 25^\circ\text{C}$ K and T Packages H Package	3	I_{max}	1.5 0.5 0.25 —	2.2 0.8 0.4 0.07	— — — —	1.5 0.5 0.15 —	2.2 0.8 0.4 0.07	— — — —	A
RMS Noise, % of V_O $T_A = 25^\circ\text{C}$, $10 \text{ Hz} \leq f \leq 10 \text{ kHz}$	—	N	—	0.003	—	—	0.003	—	%/V _O
Ripple Rejection, $V_O = 10 \text{ V}$, $f = 120 \text{ Hz}$ (Note 5) Without C_{Adj} $C_{Adj} = 10 \mu\text{F}$	4	RR	— 66	65 80	— —	— 66	65 80	— —	dB
Long-Term Stability, $T_J = T_{high}$ (Note 6) $T_A = 25^\circ\text{C}$ for Endpoint Measurements	3	S	—	0.3	1.0	—	0.3	1.0	%/1.0 k Hrs.
Thermal Resistance Junction to Case H Package K Package T Package	—	$R_{\theta JC}$	— — —	12 2.3 —	15 3.0 —	— — —	12 2.3 5.0	15 3.0 —	°C/W

NOTES: (1) $T_{low} = -55^\circ\text{C}$ for LM117 $T_{high} = +150^\circ\text{C}$ for LM117
 $= -25^\circ\text{C}$ for LM217 $= +150^\circ\text{C}$ for LM217
 $= 0^\circ\text{C}$ for LM317 $= +125^\circ\text{C}$ for LM317

(2) $I_{max} = 1.5$ A for K and T Packages
 $= 0.5$ A for H Package

$P_{max} = 20$ W for K Package

$= 20$ W for T Package

$= 2.0$ W for H Package

(3) Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must

be taken into account separately. Pulse testing with low duty cycle is used.

(4) Selected devices with tightened tolerance reference voltage available.

(5) C_{Adj} , when used, is connected between the adjustment pin and ground.

(6) Since Long-Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

LM117, LM217, LM317

FIGURE 2 – LOAD REGULATION AND ΔI_{Adj} /LOAD TEST CIRCUIT

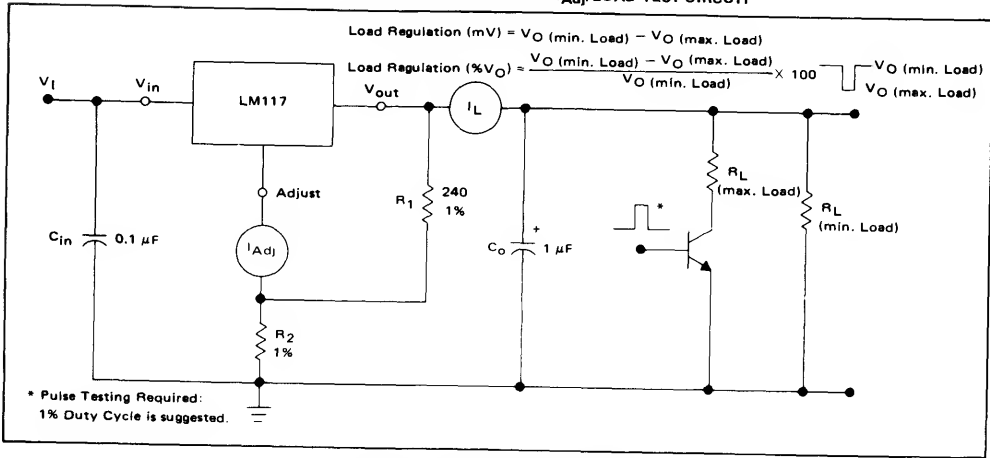


FIGURE 3 – STANDARD TEST CIRCUIT

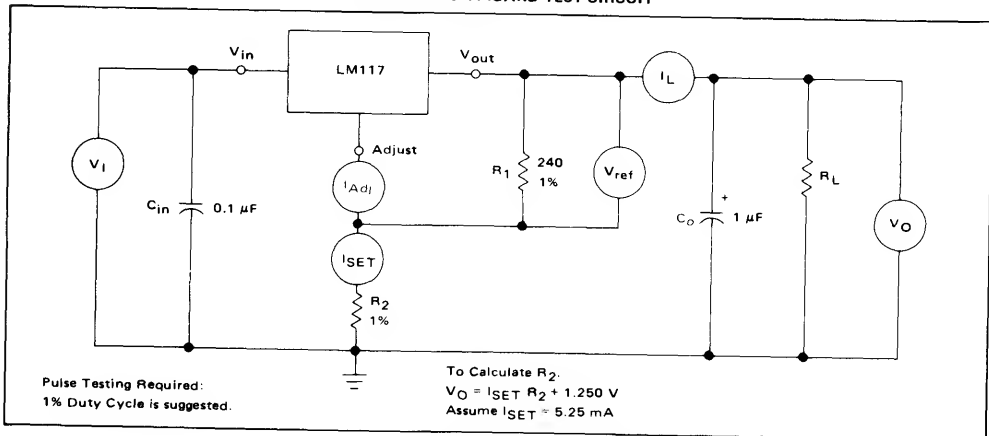
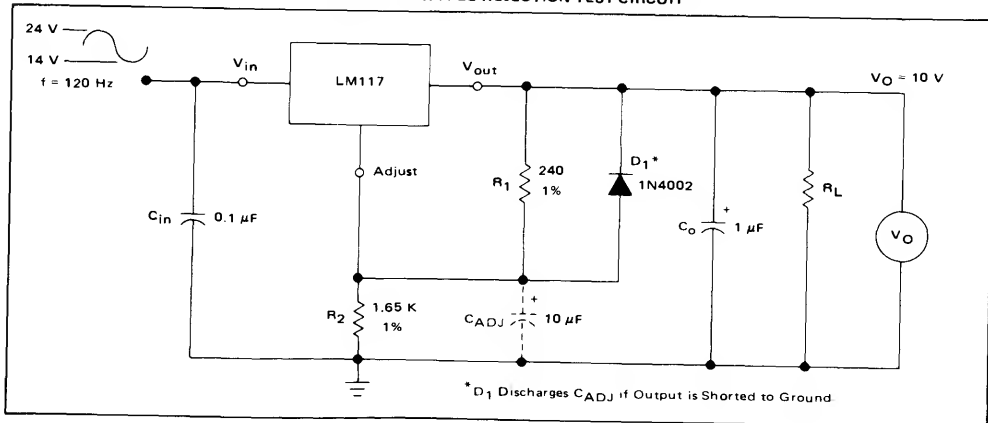


FIGURE 4 – RIPPLE REJECTION TEST CIRCUIT



LM117, LM217, LM317

FIGURE 5 – LOAD REGULATION

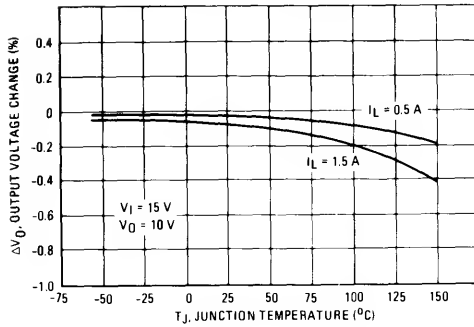


FIGURE 6 – CURRENT LIMIT

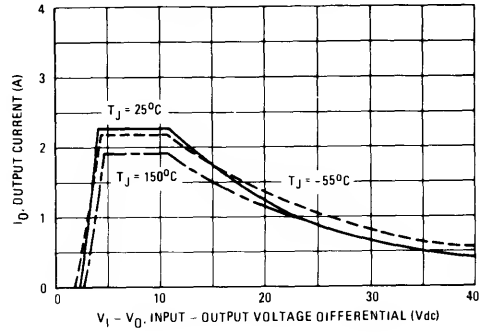


FIGURE 7 – ADJUSTMENT PIN CURRENT

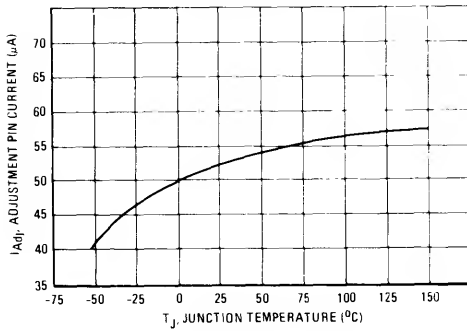


FIGURE 8 – DROPOUT VOLTAGE

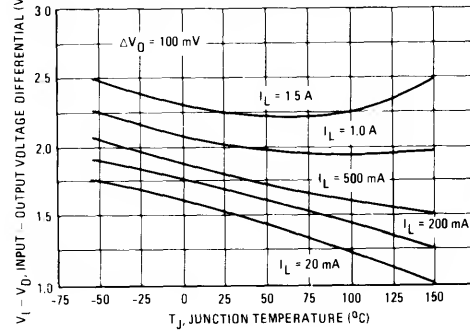


FIGURE 9 – TEMPERATURE STABILITY

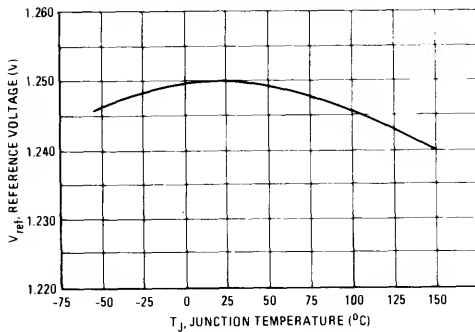


FIGURE 10 – MINIMUM OPERATING CURRENT

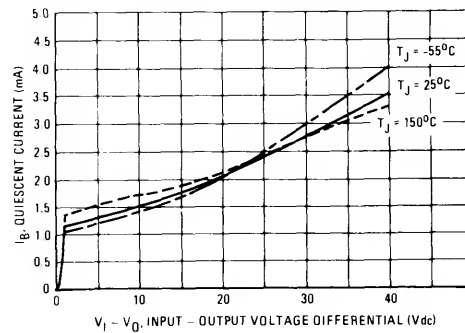


FIGURE 11 — RIPPLE REJECTION versus OUTPUT VOLTAGE

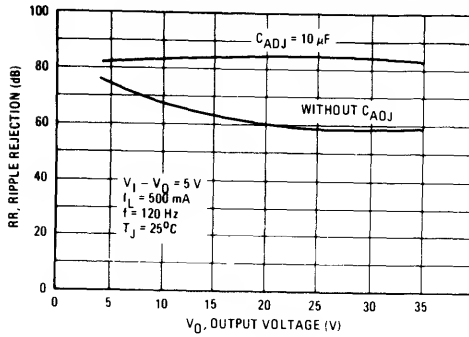


FIGURE 12 — RIPPLE REJECTION versus OUTPUT CURRENT

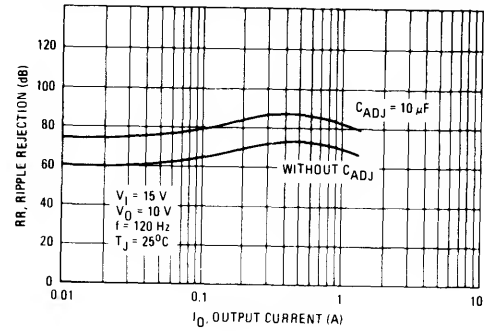


FIGURE 13 — RIPPLE REJECTION versus FREQUENCY

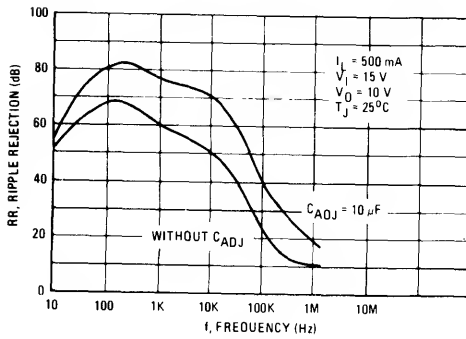


FIGURE 14 — OUTPUT IMPEDANCE

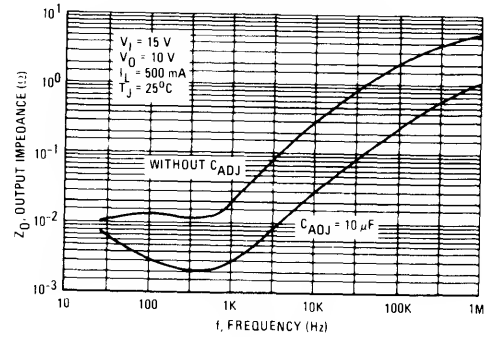


FIGURE 15 — LINE TRANSIENT RESPONSE

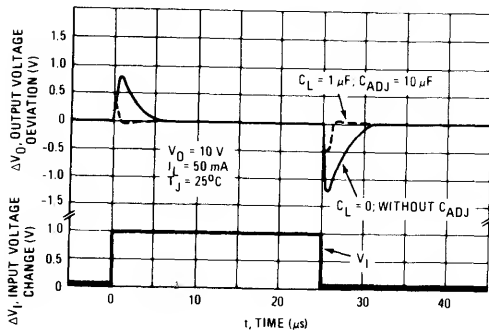
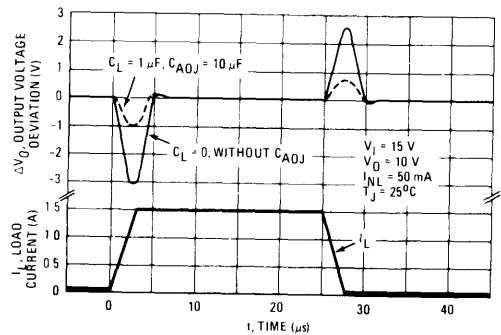


FIGURE 16 — LOAD TRANSIENT RESPONSE



APPLICATIONS INFORMATION

BASIC CIRCUIT OPERATION

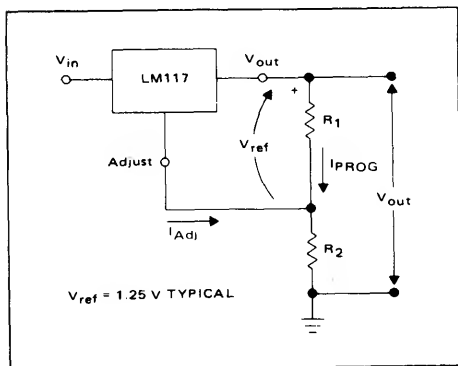
The LM117 is a 3-terminal floating regulator. In operation, the LM117 develops and maintains a nominal 1.25 volt reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by R_1 (see Figure 17), and this constant current flows through R_2 to ground. The regulated output voltage is given by:

$$V_{out} = V_{ref} \left(1 + \frac{R_2}{R_1}\right) + I_{Adj} R_2$$

Since the current from the adjustment terminal (I_{Adj}) represents an error term in the equation, the LM117 was designed to control I_{Adj} to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM117 is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

FIGURE 17 – BASIC CIRCUIT CONFIGURATION



LOAD REGULATION

The LM117 is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R_1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R_2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

EXTERNAL CAPACITORS

A 0.1 μF disc or 1 μF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{ADJ}) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15dB at 120 Hz in a 10 volt application.

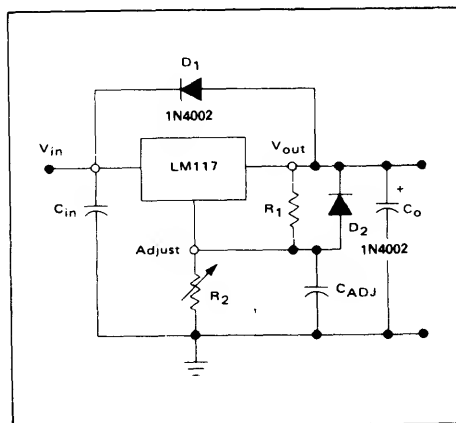
Although the LM117 is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance (C_o) in the form of a 1 μF tantalum or 25 μF aluminum electrolytic capacitor on the output swamps this effect and insures stability.

PROTECTION DIODES

When external capacitors are used with any I.C. regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 18 shows the LM117 with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values ($C_o > 25 \mu F$, $C_{ADJ} > 10 \mu F$). Diode D_1 prevents C_o from discharging thru the I.C. during an input short circuit. Diode D_2 protects against capacitor C_{ADJ} discharging through the I.C. during an output short circuit. The combination of diodes D_1 and D_2 prevents C_{ADJ} from discharging through the I.C. during an input short circuit.

FIGURE 18 – VOLTAGE REGULATOR WITH PROTECTION DIODES



LM117, LM217, LM317

FIGURE 19 — "LABORATORY" POWER SUPPLY WITH ADJUSTABLE CURRENT LIMIT AND OUTPUT VOLTAGE

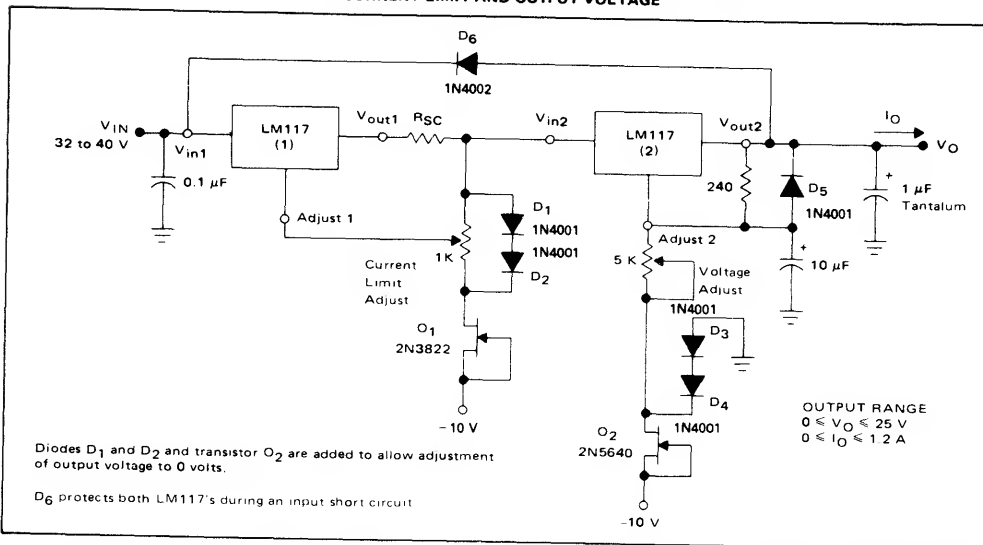


FIGURE 20 — ADJUSTABLE CURRENT LIMITER

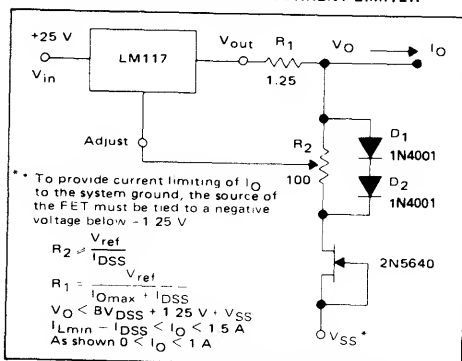


FIGURE 21 — 5 V ELECTRONIC SHUT DOWN REGULATOR

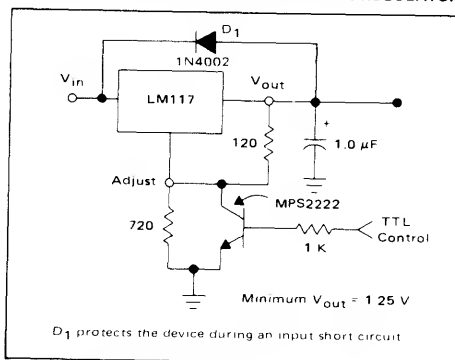


FIGURE 22 — SLOW TURN-ON REGULATOR

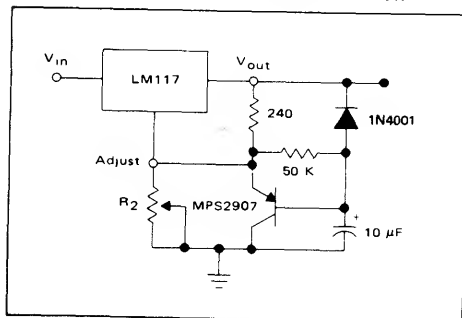
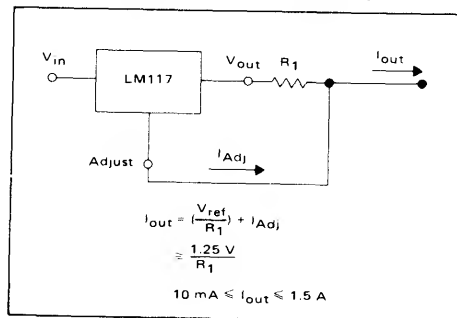


FIGURE 23 — CURRENT REGULATOR



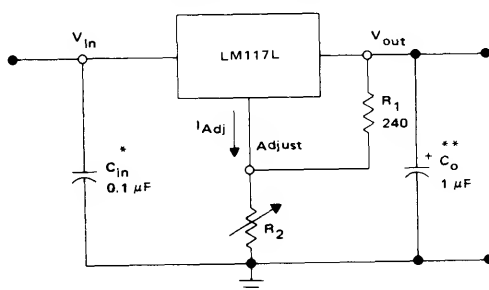
**THREE-TERMINAL ADJUSTABLE
OUTPUT POSITIVE VOLTAGE REGULATORS**

The LM117L/217L/317L are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 100 mA over an output voltage range of 1.2 V to 37 V. These voltage regulators are exceptionally easy to use and require only two external resistors to set the output voltage. Further, they employ internal current limiting, thermal shutdown and safe area compensation, making them essentially blow-out proof.

The LM117L series serves a wide variety of applications including local, on card regulation. This device can also be used to make a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM117L series can be used as a precision current regulator.

- Output Current in Excess of 100 mA
- Output Adjustable Between 1.2 V and 37 V
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Floating Operation for High Voltage Applications
- Standard 3-Lead Transistor Packages
- Eliminates Stocking Many Fixed Voltages

STANDARD APPLICATION



* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_o is not needed for stability, however it does improve transient response.

$$V_{out} = 1.25 V \left(1 + \frac{R_2}{R_1} \right) + I_{Adj} R_2$$

Since I_{Adj} is controlled to less than 100 μA , the error associated with this term is negligible in most applications

#Automotive temperature range selections are available with special test conditions and additional tests. Contact your local Motorola sales office for information.

LM117L
LM217L
LM317L

**LOW-CURRENT
THREE-TERMINAL
ADJUSTABLE POSITIVE
VOLTAGE REGULATORS**

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**

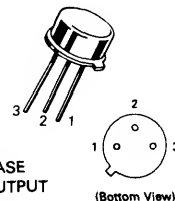
Z SUFFIX
PLASTIC PACKAGE
CASE 29

PIN 1. ADJUST
2. V_{OUT}
3. V_{IN}



H SUFFIX
METAL PACKAGE
CASE 79

PIN 1. V_{IN}
2. ADJUST
3. V_{OUT}



CASE
IS OUTPUT

(Bottom View)

D SUFFIX
PLASTIC PACKAGE
CASE 751
SOP-8*



PIN 1. V_{IN}
2. V_{OUT}
3. V_{OUT}
4. ADJUST
5. N.C.
6. V_{OUT}
7. V_{OUT}
8. N.C.

SOP-8 is an internally modified SO-8 Package. Pins 2, 3, 6 and 7 are electrically common to the die attach flag. This internal lead frame modification decreases package thermal resistance and increases power dissipation capability when appropriately mounted on a printed circuit board. SOP-8 conforms to all external dimensions of the standard SO-8 Package.

ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
LM117LH	$T_J = -55^{\circ}C$ to $+150^{\circ}C$	Metal Can
LM217LH	$T_J = -25^{\circ}C$ to $+150^{\circ}C$	Metal Can
LM317LD		SOP-8
LM317LH	$T_J = 0^{\circ}C$ to $+125^{\circ}C$	Metal Can
LM317LZ		Plastic
LM317LBZ#	$T_J = -40^{\circ}C$ to $+125^{\circ}C$	Plastic

LM117L, LM217L, LM317L

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input-Output Voltage Differential	$V_I - V_O$	40	Vdc
Power Dissipation	P_D	Internally Limited	
Operating Junction Temperature Range	T_J	-55 to +150 -25 to +150 0 to +150	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

($V_I - V_O = 5.0$ V; $I_O = 40$ mA; $T_J = T_{low}$ to T_{high} [see Note 1]; I_{max} and P_{max} per Note 2; unless otherwise specified.)

Characteristic	Figure	Symbol	LM117L/217L			LM317L			Unit
			Min	Typ	Max	Min	Typ	Max	
Line Regulation (Note 3) $T_A = 25^\circ\text{C}$, $3.0\text{ V} \leq V_I - V_O \leq 40\text{ V}$	1	Regline	—	0.01	0.02	—	0.01	0.04	%/V
Load Regulation (Note 3), $T_A = 25^\circ\text{C}$ $5.0\text{ mA} \leq I_O \leq I_{max}$ — LM117L/217L $10\text{ mA} \leq I_O \leq I_{max}$ — LM317L $V_O \leq 5.0\text{ V}$ $V_O \geq 5.0\text{ V}$	2	Regload	— —	5.0 0.1	15 0.3	— —	5.0 0.1	25 0.5	mV % V_O
Adjustment Pin Current	3	I_{Adj}	—	50	100	—	50	100	μA
Adjustment Pin Current Change $2.5\text{ V} \leq V_I - V_O \leq 40\text{ V}$, $P_D \leq P_{max}$ $5.0\text{ mA} \leq I_O \leq I_{max}$ — LM117L/217L $10\text{ mA} \leq I_O \leq I_{max}$ — LM317L	1,2	ΔI_{Adj}	—	0.2	5.0	—	0.2	5.0	μA
Reference Voltage (Note 4) $3.0\text{ V} \leq V_I - V_O \leq 40\text{ V}$, $P_D \leq P_{max}$ $5.0\text{ mA} \leq I_O \leq I_{max}$ — LM117L/217L $10\text{ mA} \leq I_O \leq I_{max}$ — LM317L	3	V_{ref}	1.20	1.25	1.30	1.20	1.25	1.30	V
Line Regulation (Note 3) $3.0\text{ V} \leq V_I - V_O \leq 40\text{ V}$	1	Regline	—	0.02	0.05	—	0.02	0.07	%/V
Load Regulation (Note 3) $5.0\text{ mA} \leq I_O \leq I_{max}$ — LM117L/217L $10\text{ mA} \leq I_O \leq I_{max}$ — LM317L $V_O \leq 5.0\text{ V}$ $V_O \geq 5.0\text{ V}$	2	Regload	— —	20 0.3	50 1.0	— —	20 0.3	70 1.5	mV % V_O
Temperature Stability ($T_{low} \leq T_J \leq T_{high}$)	3	T_S	—	0.7	—	—	0.7	—	% V_O
Minimum Load Current to Maintain Regulation ($V_I - V_O = 40\text{ V}$)	3	I_{Lmin}	—	3.5	5.0	—	3.5	10	mA
Maximum Output Current $V_I - V_O \leq 20\text{ V}$, $P_D \leq P_{max}$, H Package $V_I - V_O \leq 6.25\text{ V}$, $P_D \leq P_{max}$, Z Package $V_I - V_O = 40\text{ V}$, $P_D \leq P_{max}$, $T_A = 25^\circ\text{C}$ H Package Z Package	3	I_{max}	100 100 — —	200 200 50 20	— — — —	100 100 — —	200 200 50 20	— — — —	mA
RMS Noise, % of V_O $T_A = 25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 10\text{ kHz}$	—	N	—	0.003	—	—	0.003	—	% V_O
Ripple Rejection (Note 5) $V_O = 1.25\text{ V}$, $f = 120\text{ Hz}$ $C_{ADJ} = 10\text{ }\mu\text{F}$, $V_O = 10.0\text{ V}$	4	RR	66 —	80 80	— —	60 —	80 80	— —	dB
Long Term Stability, $T_J = T_{high}$ (Note 6) $T_A = 25^\circ\text{C}$ for Endpoint Measurements	3	S	—	0.3	1.0	—	0.3	1.0	%/1.0 k Hrs.
Thermal Resistance Junction to Case H Package Z Package	—	$R_{\theta JC}$	— —	40 —	— —	— —	40 83	— —	°C/W
Thermal Resistance Junction to Air H Package Z Package	—	$R_{\theta JA}$	— —	185 —	— —	— —	185 160	— —	°C/W

NOTES

(1) $T_{low} = -55^\circ\text{C}$ for LM117L
-25°C for LM217L
0°C for LM317L

$T_{high} = +150^\circ\text{C}$ for LM117L
+150°C for LM217L
+125°C for LM317L

(2) $I_{max} = 100\text{ mA}$
 $P_{max} = 2\text{ W}$ for H Package
= 625 mW for Z Package

(3) Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

(4) Selected devices with tightened tolerance reference voltage available

(5) C_{ADJ} , when used, is connected between the adjustment pin and ground

(6) Since Long Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot

LM117L, LM217L, LM317L

SCHEMATIC DIAGRAM

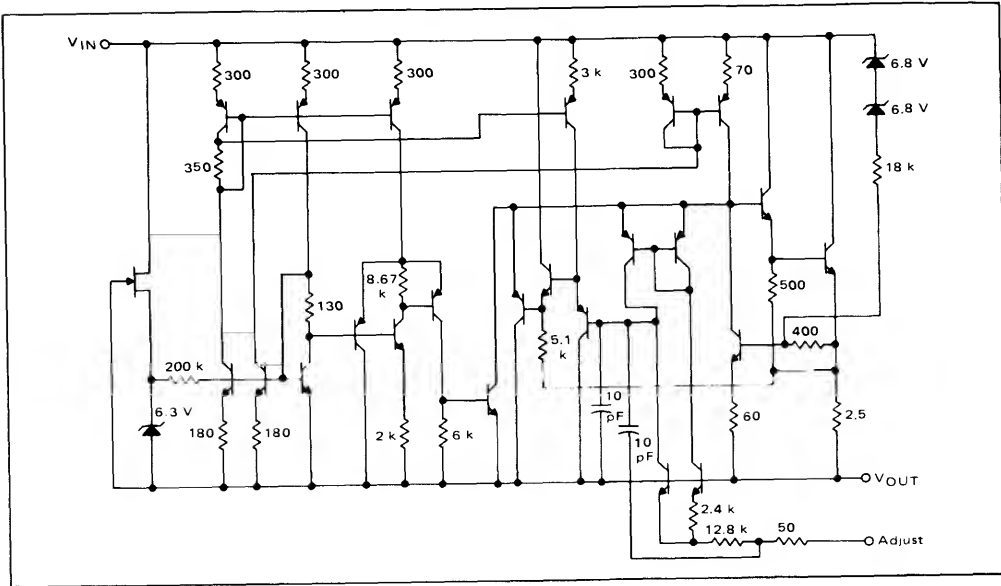
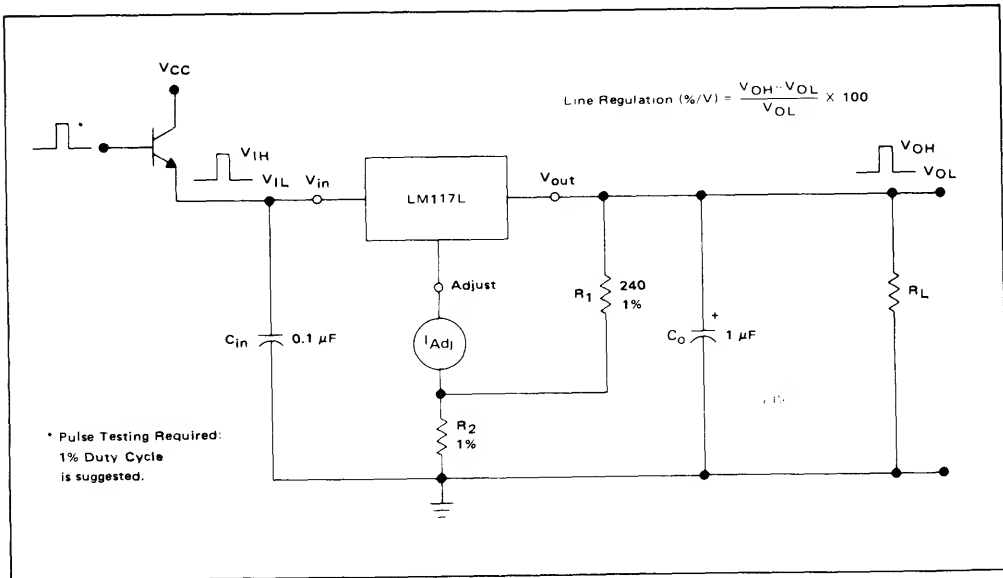


FIGURE 1 – LINE REGULATION AND $\Delta I_{Adj}/LINE$ TEST CIRCUIT



LM117L, LM217L, LM317L

FIGURE 2 – LOAD REGULATION AND ΔI_{Adj} /LOAD TEST CIRCUIT

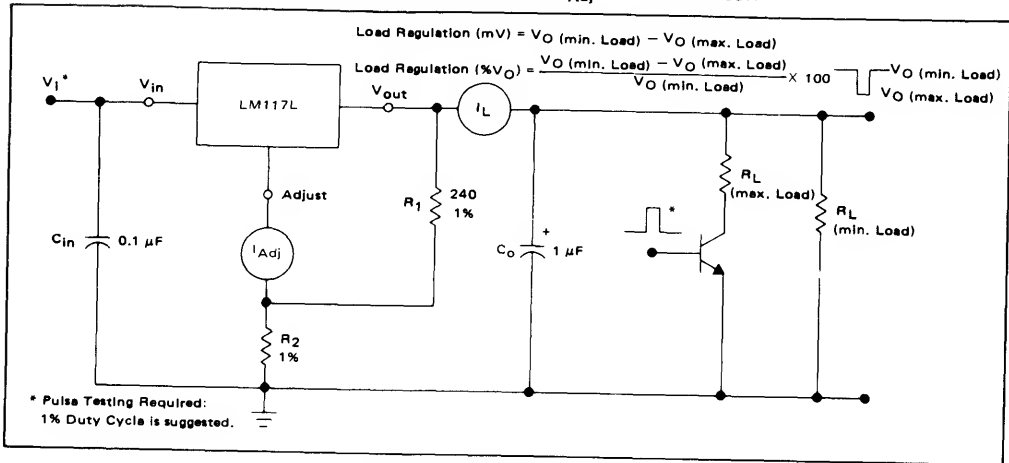


FIGURE 3 – STANDARD TEST CIRCUIT

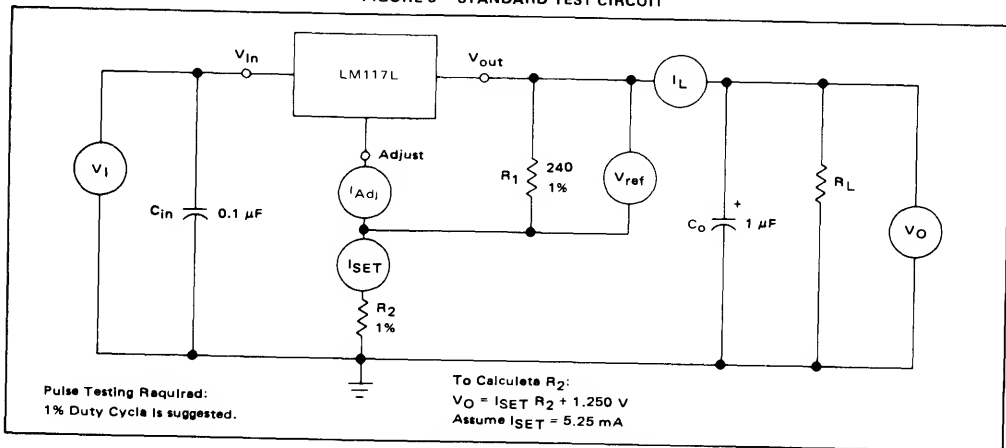
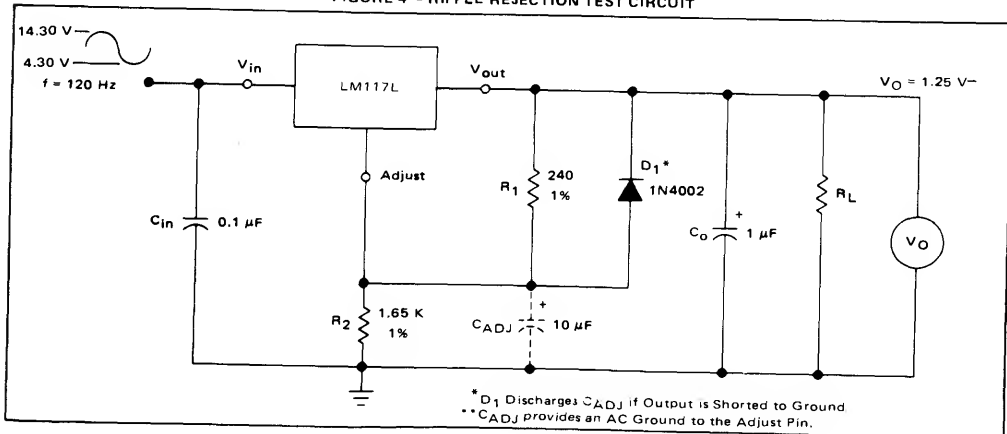


FIGURE 4 – RIPPLE REJECTION TEST CIRCUIT



LM117L, LM217L, LM317L

FIGURE 5 – LOAD REGULATION

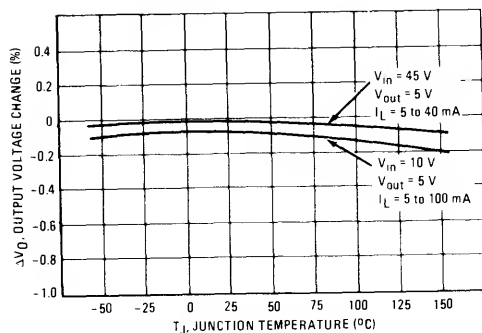


FIGURE 6 – RIPPLE REJECTION

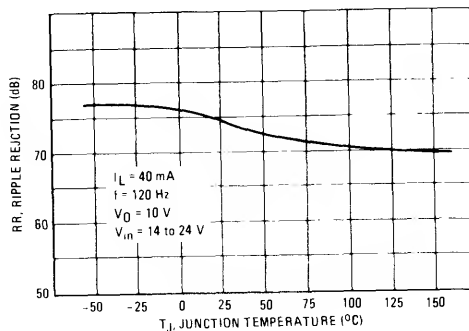


FIGURE 7 – CURRENT LIMIT

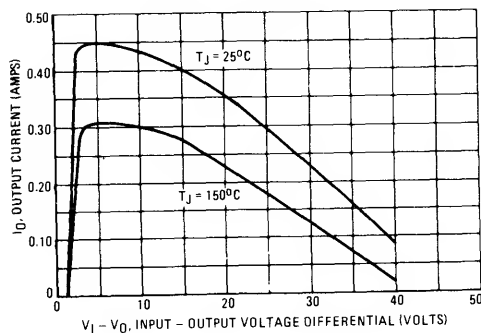


FIGURE 8 – DROPOUT VOLTAGE

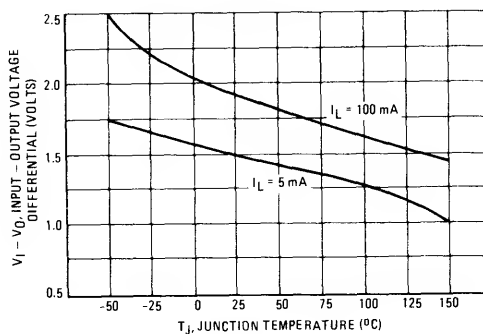


FIGURE 9 – MINIMUM OPERATING CURRENT

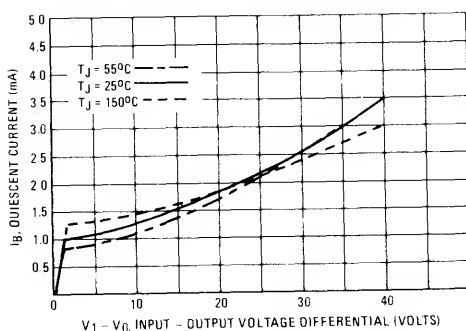
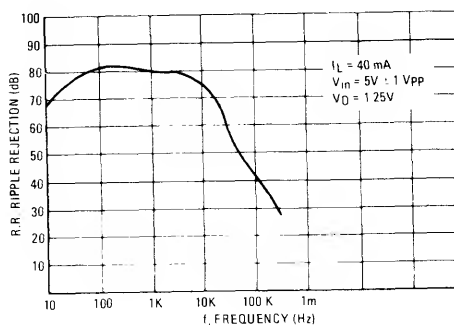


FIGURE 10 – RIPPLE REJECTION versus FREQUENCY



LM117L, LM217L, LM317L

FIGURE 11 – TEMPERATURE STABILITY

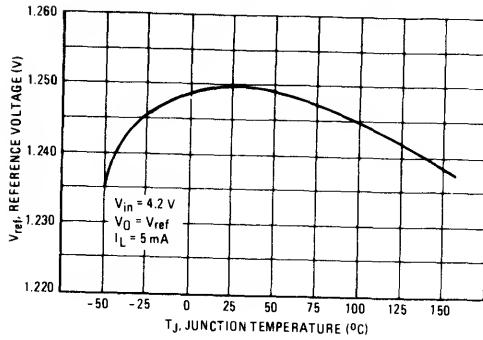


FIGURE 12 – ADJUSTMENT PIN CURRENT

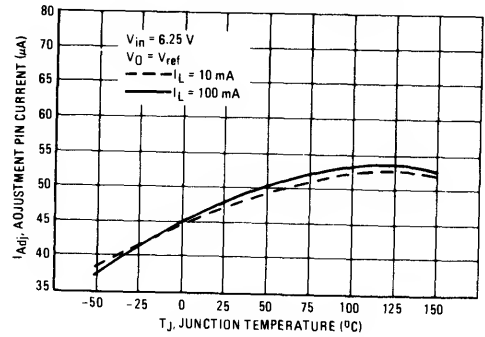


FIGURE 13 – LINE REGULATION

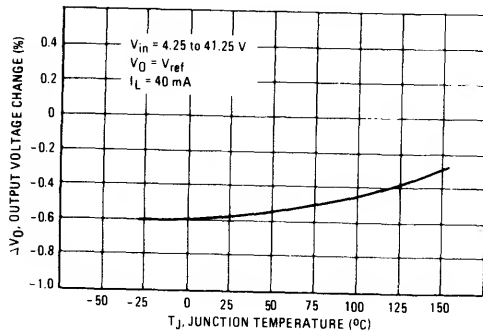


FIGURE 14 – OUTPUT NOISE

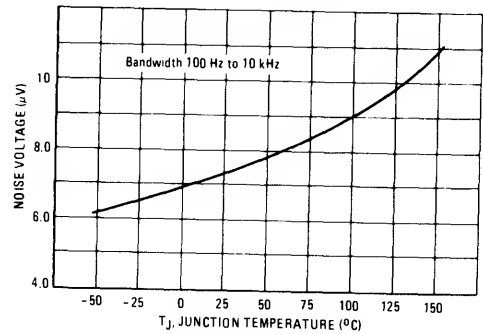


FIGURE 15 – LINE TRANSIENT RESPONSE

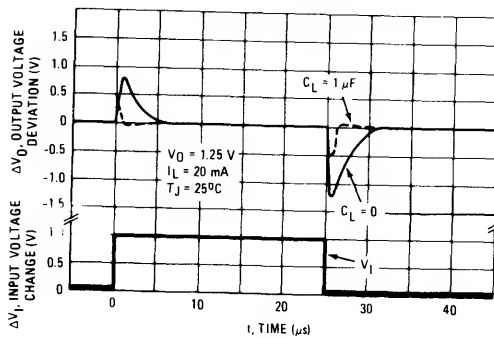
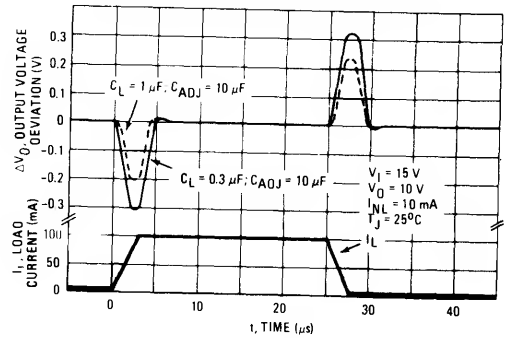


FIGURE 16 – LOAD TRANSIENT RESPONSE



APPLICATIONS INFORMATION

BASIC CIRCUIT OPERATION

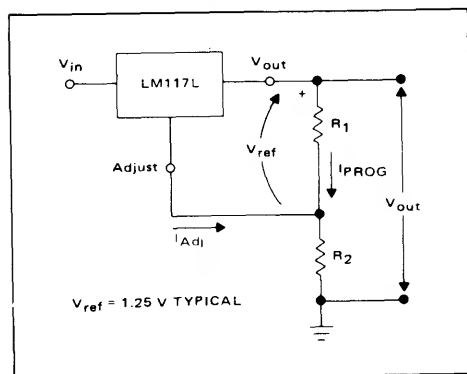
The LM117L is a 3-terminal floating regulator. In operation, the LM117L develops and maintains a nominal 1.25 volt reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by R_1 (see Figure 13), and this constant current flows through R_2 to ground. The regulated output voltage is given by:

$$V_{out} = V_{ref} \left(1 + \frac{R_2}{R_1}\right) + I_{Adj} R_2$$

Since the current from the adjustment terminal (I_{Adj}) represents an error term in the equation, the LM117L was designed to control I_{Adj} to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM117L is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

FIGURE 17 – BASIC CIRCUIT CONFIGURATION



LOAD REGULATION

The LM117L is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R_1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R_2 can be returned near the load point to provide remote ground sensing and improve load regulation.

EXTERNAL CAPACITORS

A 0.1 μF disc or 1 μF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{ADJ}) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15dB at 120 Hz in a 10 volt application.

Although the LM117L is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance (C_o) in the form of a 1 μF tantalum or 25 μF aluminum electrolytic capacitor on the output swamps this effect and insures stability.

PROTECTION DIODES

When external capacitors are used with any I.C. regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 14 shows the LM117L with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values ($C_o > 10 \mu F$, $C_{ADJ} > 5 \mu F$). Diode D_1 prevents C_o from discharging thru the I.C. during an input short circuit. Diode D_2 protects against capacitor C_{ADJ} discharging through the I.C. during an output short circuit. The combination of diodes D_1 and D_2 prevents C_{ADJ} from discharging through the I.C. during an input short circuit.

FIGURE 18 – VOLTAGE REGULATOR WITH PROTECTION DIODES

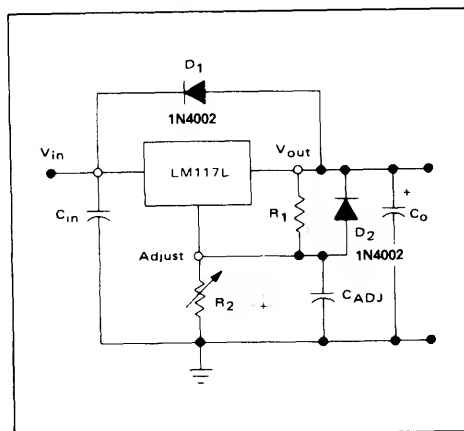


FIGURE 19 — ADJUSTABLE CURRENT LIMITER

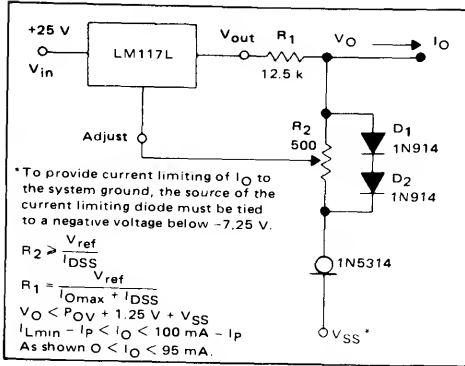


FIGURE 20 — 5 V ELECTRONIC SHUTDOWN REGULATOR

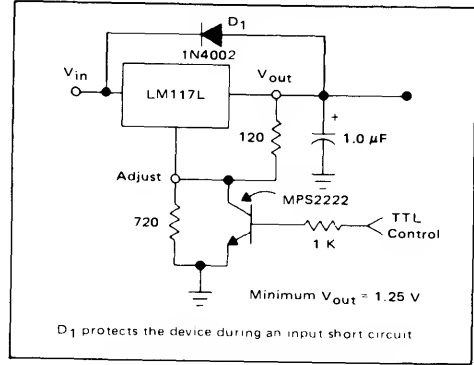


FIGURE 21 — SLOW TURN-ON REGULATOR

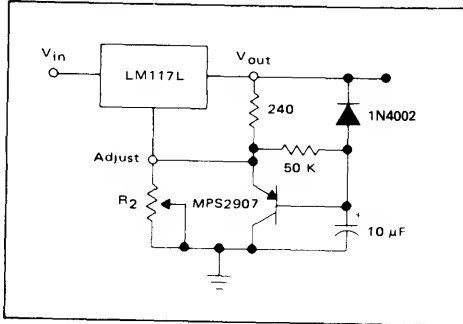
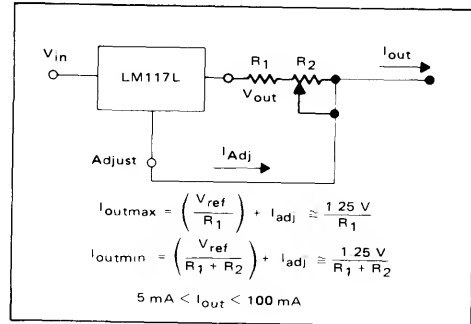


FIGURE 22 — CURRENT REGULATOR



LM123, LM123A
LM223, LM223A
LM323, LM323A

3-AMPERE, 5 VOLT
POSITIVE
VOLTAGE REGULATORS

SILICON MONOLITHIC
INTEGRATED CIRCUIT

POSITIVE VOLTAGE REGULATORS

The LM123, A/LM223, A/LM323, A are a family of monolithic integrated circuits which supply a fixed positive 5.0 volt output with a load driving capability in excess of 3.0 amperes. These three-terminal regulators employ internal current limiting, thermal shut-down, and safe-area compensation. An improved series with superior electrical characteristics and a 2% output voltage tolerance is available as A-suffix (LM123A/LM223A/LM323A) device types.

These regulators are offered in a hermetic metal power package in three operating temperature ranges. A 0°C to +125°C temperature range version is also available in a low cost plastic power package.

Although designed primarily as a fixed voltage regulator, these devices can be used with external components to obtain adjustable voltages and currents. This series of devices can be used with a series pass transistor to supply up to 15 amperes at 5.0 volts.

- Output Current in Excess of 3.0 Amperes
- Available with 2% Output Voltage Tolerance
- No external Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Thermal Regulation and Ripple Rejection Have Specified Limits

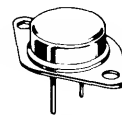
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	V_{in}	20	Vdc
Power Dissipation	P_D	Internally Limited	
Operating Junction Temperature Range	T_J	-55 to +150 -25 to +150 0 to +150	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Lead Temperature (Soldering, 10 s)	T_{solder}	300	°C

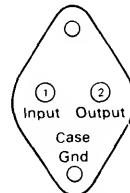
ORDERING INFORMATION

Device	Output Voltage Tolerance	Tested Operating Junction Temp. Range	Package
LM123K	6%	-55 to +150°C	Metal Power
LM123AK	2%		
LM223K	6%	-25 to +150°C	
LM223AK	2%		
LM323K	4%	0 to +125°C	Plastic Power
LM323AK	2%		
LM323T	4%		
LM323AT	2%		

K SUFFIX
METAL PACKAGE
CASE 1

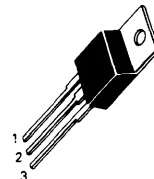


PIN 1. INPUT
2. OUTPUT
CASE GROUND



(Bottom View)

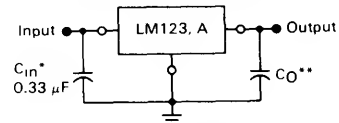
T SUFFIX
PLASTIC PACKAGE
CASE 221A



PIN 1. INPUT
2. GROUND
3. OUTPUT

(Heatsink surface connected to Pin 2)

STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.5 V above the output voltage even during the low point on the input ripple voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter. (See Applications Information for details.)

** = C_O is not needed for stability; however, it does improve transient response.

LM123, LM123A, LM223, LM223A, LM323, LM323A

ELECTRICAL CHARACTERISTICS ($T_J = T_{low}$ to T_{high} [see Note 1] unless otherwise specified.)

Characteristic	Symbol	LM123A/LM223A/LM323A			LM123/LM223			LM323			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage ($V_{in} = 7.5\text{ V}$, $0 \leq I_{out} \leq 3.0\text{ A}$, $T_J = 25^\circ\text{C}$)	V_O	4.9	5.0	5.1	4.7	5.0	5.3	4.8	5.0	5.2	V
Output Voltage ($7.5\text{ V} \leq V_{in} \leq 15\text{ V}$, $0 \leq I_{out} \leq 3.0\text{ A}$, $P \leq P_{max}$ (Note 2))	V_O	4.8	5.0	5.2	4.6	5.0	5.4	4.75	5.0	5.25	V
Line Regulation ($7.5\text{ V} \leq V_{in} \leq 15\text{ V}$, $T_J = 25^\circ\text{C}$) (Note 3)	Reg_{line}	—	1.0	15	—	1.0	25	—	1.0	25	mV
Load Regulation ($V_{in} = 7.5\text{ V}$, $0 \leq I_{out} \leq 3.0\text{ A}$, $T_J = 25^\circ\text{C}$) (Note 3)	Reg_{load}	—	10	50	—	10	100	—	10	100	mV
Thermal Regulation (Pulse = 10 ms, $P = 20\text{ W}$, $T_A = 25^\circ\text{C}$)	Reg_{therm}	—	0.001	0.01	—	0.002	0.03	—	0.002	0.03	% V_O /W
Quiescent Current ($7.5\text{ V} \leq V_{in} \leq 15\text{ V}$, $0 \leq I_{out} \leq 3.0\text{ A}$)	I_Q	—	3.5	10	—	3.5	20	—	3.5	20	mA
Output Noise Voltage (10 Hz $\leq f \leq 100\text{ kHz}$, $T_J = 25^\circ\text{C}$)	V_N	—	40	—	—	40	—	—	40	—	μV_{rms}
Ripple Rejection ($8.0\text{ V} \leq V_{in} \leq 18\text{ V}$, $I_{out} = 2.0\text{ A}$, $f = 120\text{ Hz}$, $T_J = 25^\circ\text{C}$)	RR	66	75	—	62	75	—	62	75	—	dB
Short Circuit Current Limit ($V_{in} = 15\text{ V}$, $T_J = 25^\circ\text{C}$) ($V_{in} = 7.5\text{ V}$, $T_J = 25^\circ\text{C}$)	I_{SC}	—	4.5 5.5	—	—	4.5 5.5	—	—	4.5 5.5	—	A
Long Term Stability	S	—	—	35	—	—	35	—	—	35	mV
Thermal Resistance Junction to Case (Note 4)	$R_{\theta JC}$	—	2.0	—	—	2.0	—	—	2.0	—	$^\circ\text{C/W}$

Note 1. $T_{low} = -55^\circ\text{C}$ for LM123, A
 -25°C for LM223, A
 $= 0^\circ\text{C}$ for LM323, A
 $T_{high} = +150^\circ\text{C}$ for LM123, A
 $= +150^\circ\text{C}$ for LM223, A
 $= +125^\circ\text{C}$ for LM323, A

Note 2. Although power dissipation is internally limited, specifications apply only for $P \leq P_{max}$
 $P_{max} = 30\text{ W}$ for K package
 $P_{max} = 25\text{ W}$ for T package

Note 3. Load and line regulation are specified at constant junction temperature. Pulse testing is required with a pulse width $\leq 1.0\text{ ms}$ and a duty cycle $\leq 5\%$.

Note 4. Without a heat sink, the thermal resistance ($R_{\theta JA}$) is 35°C/W for the K package, and 65°C/W for the T package. With a heat sink, the effective thermal resistance can approach the specified values of 2.0°C/W , depending on the efficiency of the heat sink.

VOLTAGE REGULATOR PERFORMANCE

The performance of a voltage regulator is specified by its immunity to changes in load, input voltage, power dissipation, and temperature. Line and load regulation are tested with a pulse of short duration ($< 100\text{ }\mu\text{s}$) and are strictly a function of electrical gain. However, pulse widths of longer duration ($> 1.0\text{ ms}$) are sufficient to affect temperature gradients across the die. These temperature gradients can cause a change in the output voltage, in addition to changes caused by line and load regulation. Longer pulse widths and thermal gradients make it desirable to specify thermal regulation.

Thermal regulation is defined as the change in output voltage caused by a change in dissipated power for a specified time, and is expressed as a percentage output voltage change per watt. The

change in dissipated power can be caused by a change in either the input voltage or the load current. Thermal regulation is a function of I.C. layout and die attach techniques, and usually occurs within 10 ms of a change in power dissipation. After 10 ms, additional changes in the output voltage are due to the temperature coefficient of the device.

Figure 1 shows the line and thermal regulation response of a typical LM123A to a 20 watt input pulse. The variation of the output voltage due to line regulation is labeled ① and the thermal regulation component is labeled ②. Figure 2 shows the load and thermal regulation response of a typical LM123A to a 20 watt load pulse. The output voltage variation due to load regulation is labeled ① and the thermal regulation component is labeled ②.

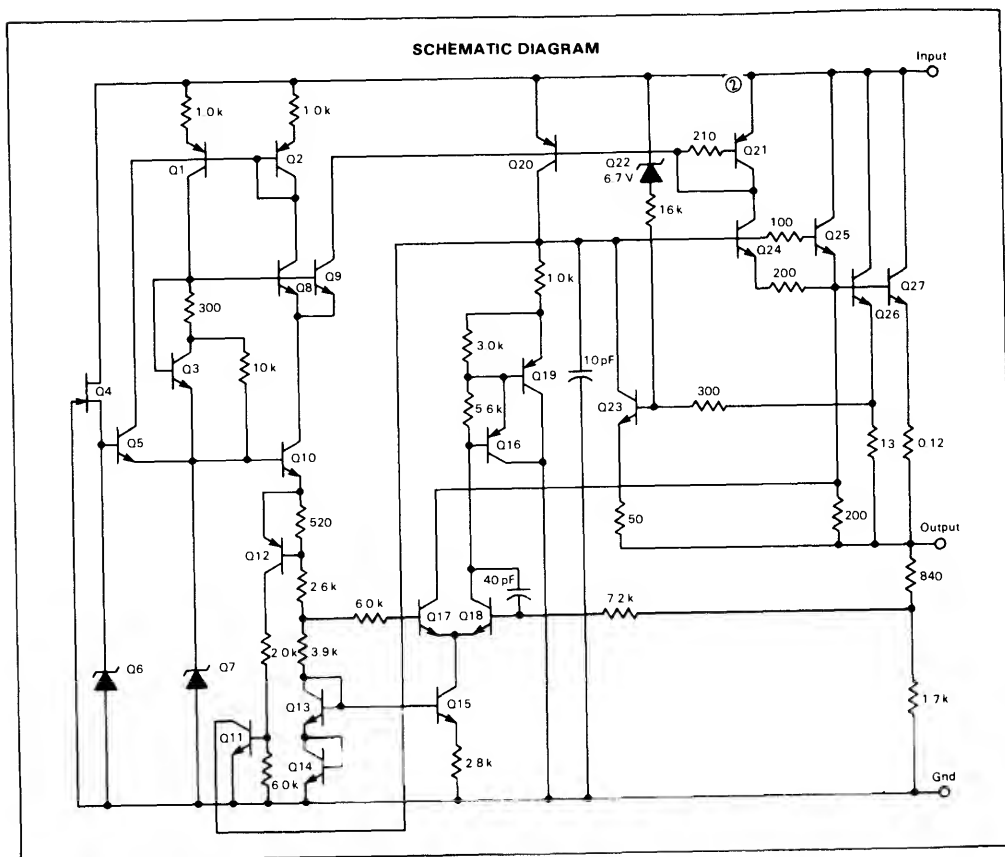
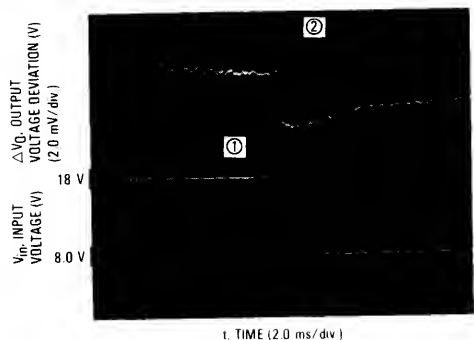


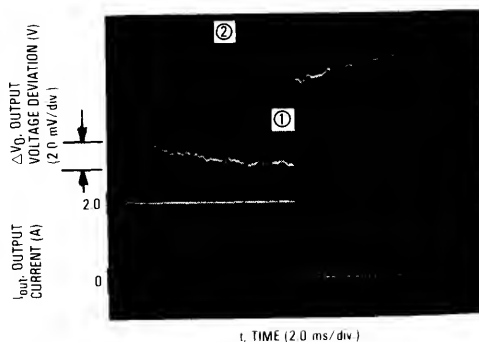
FIGURE 1 — LINE AND THERMAL REGULATION



LM123A
 $V_O = 5.0 \text{ V}$
 $V_{in} = 8.0 \text{ V} \rightarrow 18 \text{ V} \rightarrow 8.0 \text{ V}$
 $I_{out} = 2.0 \text{ A}$

① = $\text{Reg}_{line} = 2.4 \text{ mV}$
 ② = $\text{Reg}_{therm} = 0.0015\% V_O / ^\circ\text{W}$

FIGURE 2 — LOAD AND THERMAL REGULATION



LM123A
 $V_O = 5.0 \text{ V}$
 $V_{in} = 15$
 $I_{out} = 0 \text{ A} \rightarrow 2.0 \text{ A} \rightarrow 0 \text{ A}$

① = $\text{Reg}_{load} = 4.4 \text{ mV}$
 ② = $\text{Reg}_{therm} = 0.0015\% V_O / ^\circ\text{W}$

LM123, LM123A, LM223, LM223A, LM323, LM323A

FIGURE 3 — TEMPERATURE STABILITY

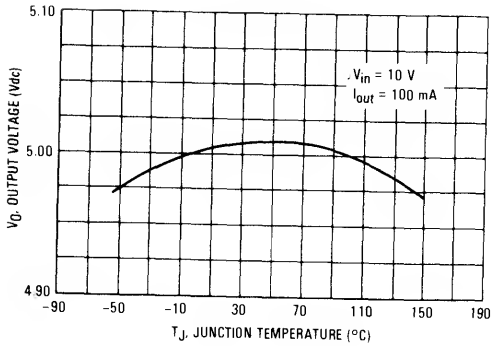


FIGURE 4 — OUTPUT IMPEDANCE

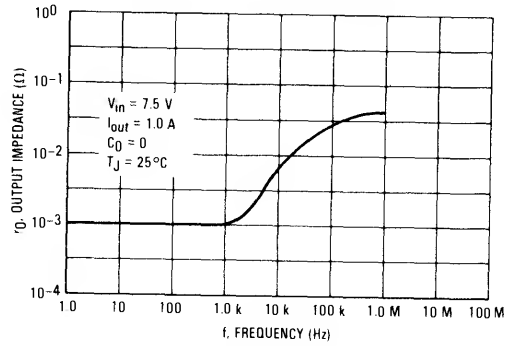


FIGURE 5 — RIPPLE REJECTION versus FREQUENCY

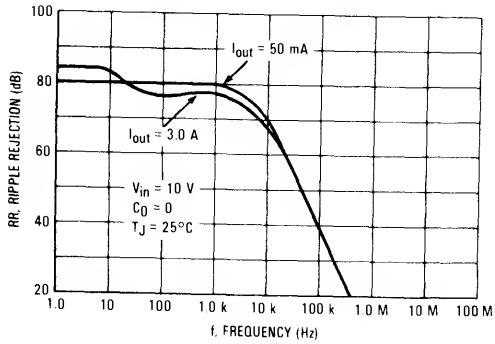


FIGURE 6 — RIPPLE REJECTION versus OUTPUT CURRENT

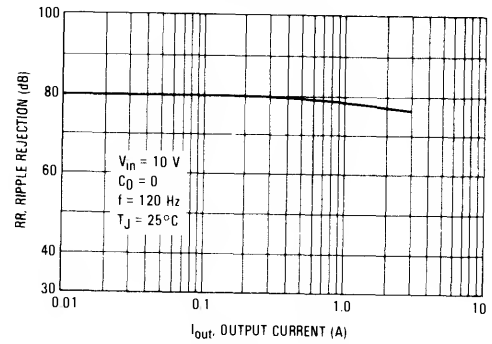


FIGURE 7 — QUIESCENT CURRENT versus INPUT VOLTAGE

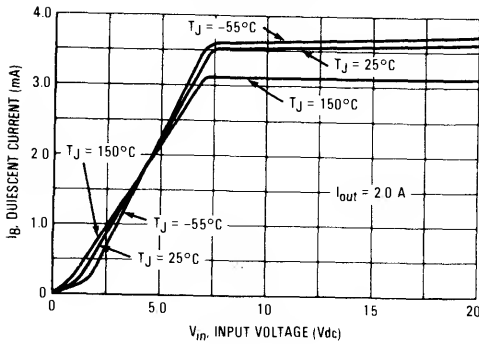
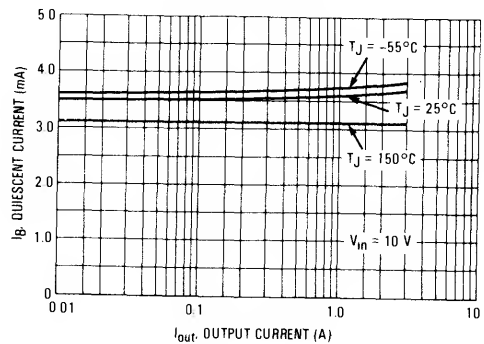


FIGURE 8 — QUIESCENT CURRENT versus OUTPUT CURRENT



LM123, LM123A, LM223, LM223A, LM323, LM323A

FIGURE 9 — DROPOUT VOLTAGE

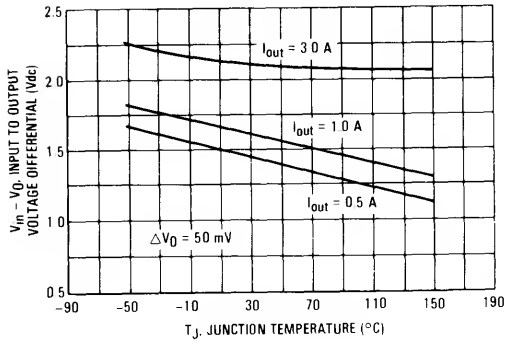


FIGURE 10 — SHORT CIRCUIT CURRENT

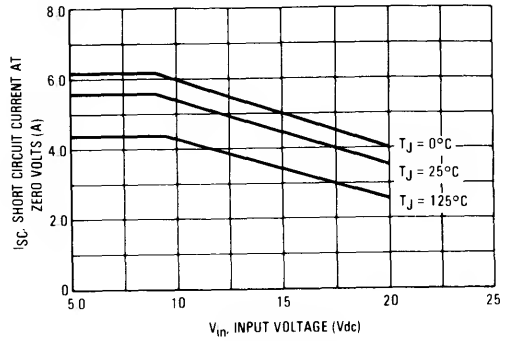


FIGURE 11 — LINE TRANSIENT RESPONSE

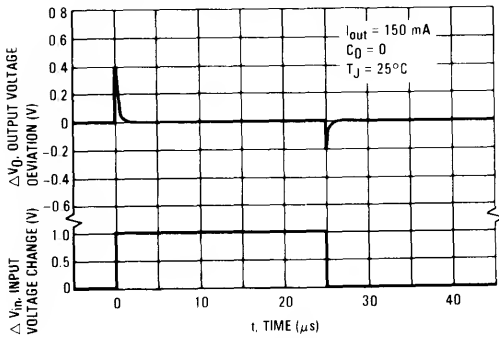


FIGURE 12 — LOAD TRANSIENT RESPONSE

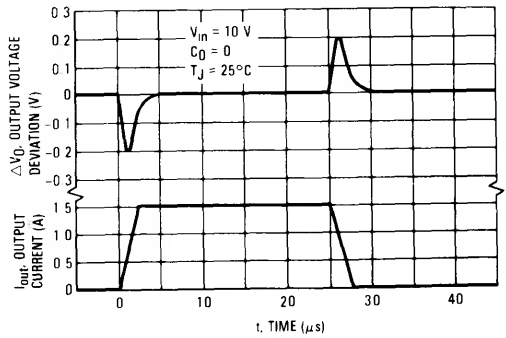


FIGURE 13 — MAXIMUM AVERAGE POWER DISSIPATION FOR LM123K and LM223K

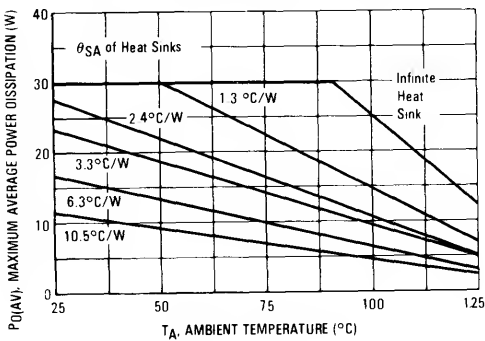
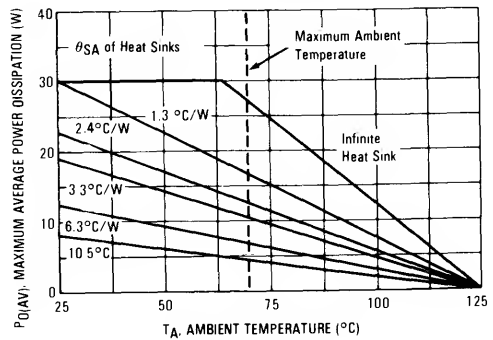


FIGURE 14 — MAXIMUM AVERAGE POWER DISSIPATION FOR LM323K



LM123, LM123A, LM223, LM223A, LM323, LM323A

APPLICATIONS INFORMATION

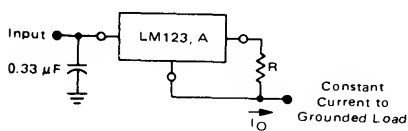
Design Considerations

The LM123A Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with

long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μ F or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulator's input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

FIGURE 15 — CURRENT REGULATOR



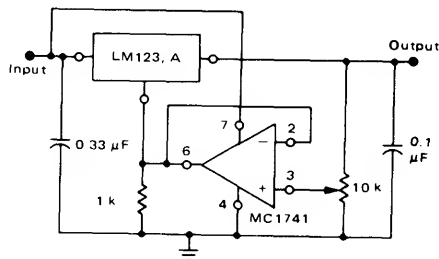
The LM123A regulator can also be used as a current source when connected as above. Resistor R determines the current as follows:

$$I_O = \frac{5.0 \text{ V}}{R} + I_B$$

$\Delta I_B \approx 0.7 \text{ mA}$ over line, load and temperature changes
 $I_B \approx 3.5 \text{ mA}$

For example, a 2-ampere current source would require R to be a 2.5 ohm, 15 W resistor and the output voltage compliance would be the input voltage less 7.5 volts.

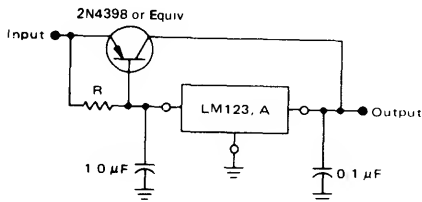
FIGURE 16 — ADJUSTABLE OUTPUT REGULATOR



$V_O: 8.0 \text{ V to } 20 \text{ V}$
 $V_{in} - V_O \geq 2.5 \text{ V}$

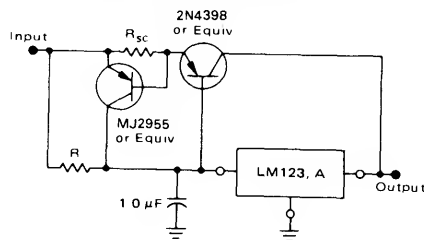
The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 3.0 volts greater than the regulator voltage.

FIGURE 17 — CURRENT BOOST REGULATOR



The LM123A series can be current boosted with a PNP transistor. The 2N4398 provides current to 15 amperes. Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short-circuit proof. Input-output differential voltage minimum is increased by the V_{BE} of the pass transistor.

FIGURE 18 — CURRENT BOOST WITH SHORT-CIRCUIT PROTECTION



The circuit of Figure 17 can be modified to provide supply protection against short circuits by adding a short-circuit sense resistor, R_{SC} , and an additional PNP transistor. The current sensing PNP must be able to handle the short-circuit current of the three-terminal regulator. Therefore, an eight-ampere power transistor is specified.

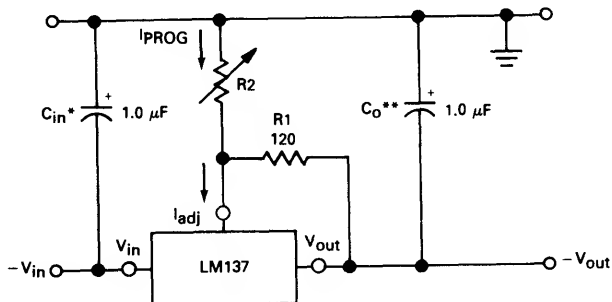
THREE-TERMINAL ADJUSTABLE OUTPUT NEGATIVE VOLTAGE REGULATORS

The LM137/237/337 are adjustable 3-terminal negative voltage regulators capable of supplying in excess of 1.5 A over an output voltage range of -1.2 V to -37 V . These voltage regulators are exceptionally easy to use and require only two external resistors to set the output voltage. Further, they employ internal current limiting, thermal shutdown and safe area compensation, making them essentially blow-out proof.

The LM137 series serve a wide variety of applications including local, on-card regulation. This device can also be used to make a programmable output regulator; or, by connecting a fixed resistor between the adjustment and output, the LM137 series can be used as a precision current regulator.

- Output Current in Excess of 1.5 Ampere in K and T Suffix Packages
- Output Current in Excess of 0.5 Ampere in H Suffix Package
- Output Adjustable Between -1.2 V and -37 V
- Internal Thermal Overload Protection
- Internal Short-Circuit-Current Limiting, Constant with Temperature
- Output Transistor Safe-Area Compensation
- Floating Operation for High Voltage Applications
- Standard 3-Lead Transistor Packages
- Eliminates Stocking Many Fixed Voltages

STANDARD APPLICATION



* C_{in} is required if regulator is located more than 4 inches from power supply filter. A $1\text{ }\mu\text{F}$ solid tantalum or $10\text{ }\mu\text{F}$ aluminum electrolytic is recommended.

** C_o is necessary for stability. A $1\text{ }\mu\text{F}$ solid tantalum or $10\text{ }\mu\text{F}$ aluminum electrolytic is recommended.

$$V_{out} = -1.25\text{ V} \left(1 + \frac{R_2}{R_1}\right)$$

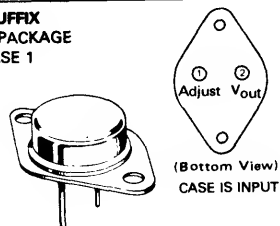
#Automotive temperature range selections are available with special test conditions and additional tests. Contact your local Motorola sales office for information.

LM137
LM237
LM337

THREE-TERMINAL ADJUSTABLE NEGATIVE VOLTAGE REGULATORS

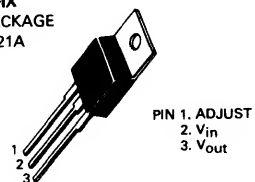
**SILICON MONOLITHIC
INTEGRATED CIRCUIT**

K SUFFIX METAL PACKAGE CASE 1



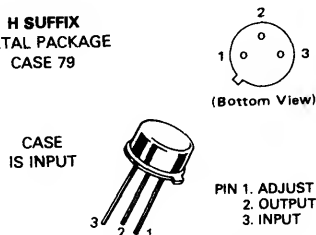
Pins 1 and 2 electrically isolated from case.
Case is third electrical connection.

T SUFFIX PLASTIC PACKAGE CASE 221A



Heatsink surface connected to Pin 2

H SUFFIX METAL PACKAGE CASE 79



ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
LM137H	$T_J = -55^\circ\text{C}$ to $+150^\circ\text{C}$	Metal Can
LM137K		Metal Power
LM237H	$T_J = -25^\circ\text{C}$ to $+150^\circ\text{C}$	Metal Can
LM237K		Metal Power
LM337H	$T_J = 0^\circ\text{C}$ to $+125^\circ\text{C}$	Metal Can
LM337K		Metal Power
LM337T		Plastic Power
LM337BT#	$T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$	Plastic Power

LM137, LM237, LM337

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input-Output Voltage Differential	$V_I - V_O$	40	Vdc
Power Dissipation	P_D	Internally Limited	
Operating Junction Temperature Range	T_J	-55 to +150 -25 to +150 0 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS ($|V_I - V_O| = 5.0$ V, $I_O = 0.5$ A for K and T packages; $I_O = 0.1$ A for H package; $T_J = T_{low}$ to T_{high} [see Note 1], I_{max} and P_{max} per Note 2, unless otherwise specified.)

Characteristic	Figure	Symbol	LM137/237			LM337			Unit
			Min	Typ	Max	Min	Typ	Max	
Line Regulation (Note 3) $T_A = 25^\circ\text{C}$, $3.0\text{ V} \leq V_I - V_O \leq 40\text{ V}$	1	Regline	—	0.01	0.02	—	0.01	0.04	%/V
Load Regulation (Note 3) $T_A = 25^\circ\text{C}$, $10\text{ mA} \leq I_O \leq I_{max}$ $ V_O \leq 5.0\text{ V}$ $ V_O \geq 5.0\text{ V}$	2	Regload	— —	15 0.3	25 0.5	— —	15 0.3	50 1.0	mV % V_O
Thermal Regulation 10 ms Pulse, $T_A = 25^\circ\text{C}$	—	Regtherm	—	0.002	0.02	—	0.003	0.04	% V_O /W
Adjustment Pin Current	3	I_{Adj}	—	65	100	—	65	100	μA
Adjustment Pin Current Change $2.5\text{ V} \leq V_I - V_O \leq 40\text{ V}$ $10\text{ mA} \leq I_L \leq I_{max}$ $P_D \leq P_{max}$, $T_A = 25^\circ\text{C}$	1.2	ΔI_{Adj}	—	2.0	5.0	—	2.0	5.0	μA
Reference Voltage (Note 4) $T_A = +25^\circ\text{C}$ $3.0\text{ V} \leq V_I - V_O \leq 40\text{ V}$, $10\text{ mA} \leq I_O \leq I_{max}$, $P_D \leq P_{max}$, $T_J = T_{low}$ to T_{high}	3	V_{ref}	-1.225 -1.20	-1.250 -1.25	-1.275 -1.30	-1.213 -1.20	-1.250 -1.25	-1.287 -1.30	V
Line Regulation (Note 3) $3.0\text{ V} \leq V_I - V_O \leq 40\text{ V}$	1	Regline	—	0.02	0.05	—	0.02	0.07	%/V
Load Regulation (Note 3) $10\text{ mA} \leq I_O \leq I_{max}$ $ V_O \leq 5.0\text{ V}$ $ V_O \geq 5.0\text{ V}$	2	Regload	— —	20 0.3	50 1.0	— —	20 0.3	70 1.5	mV % V_O
Temperature Stability ($T_{low} \leq T_J \leq T_{high}$)	3	T_S	—	0.6	—	—	0.6	—	% V_O
Minimum Load Current to Maintain Regulation ($ V_I - V_O \leq 10\text{ V}$) ($ V_I - V_O \leq 40\text{ V}$)	3	I_{Lmin}	— —	1.2 2.5	3.0 5.0	— —	1.5 2.5	6.0 10	mA
Maximum Output Current $ V_I - V_O \leq 15\text{ V}$, $P_D \leq P_{max}$ K and T Packages H Package $ V_I - V_O = 40\text{ V}$, $P_D \leq P_{max}$, $T_J = 25^\circ\text{C}$ K and T Packages H Package	3	I_{max}	1.5 0.5 0.24 0.15	2.2 0.8 0.4 0.2	— — — —	1.5 0.5 0.15 0.1	2.2 0.8 0.4 0.2	— — — —	A
RMS Noise, % of V_O $T_A = 25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 10\text{ kHz}$	—	N	—	0.003	—	—	0.003	—	% V_O
Ripple Rejection, $V_O = -10\text{ V}$, $f = 120\text{ Hz}$ (Note 5) Without C_{Adj} $C_{Adj} = 10\text{ }\mu\text{F}$	4	RR	— 66	60 77	— —	— 66	60 77	— —	dB
Long-Term Stability, $T_J = T_{high}$ (Note 6) $T_A = 25^\circ\text{C}$ for Endpoint Measurements	3	S	—	0.3	1.0	—	0.3	1.0	%/1.0 k Hrs.
Thermal Resistance Junction to Case H Package K Package T Package	—	$R_{\theta JC}$	— — —	12 2.3 —	15 3.0 —	— — —	12 2.3 4.0	15 3.0 —	°C/W

NOTES:

- (1) $T_{low} = -55^\circ\text{C}$ for LM137
 -25°C for LM237
 0°C for LM337
 $T_{high} = +150^\circ\text{C}$ for LM137
 $+150^\circ\text{C}$ for LM237
 $+125^\circ\text{C}$ for LM337
- (2) $I_{max} = 1.5$ A for K and T Packages
 0.5 A for H Package
 $P_{max} = 20$ W for K and T Packages
 2 W for H Package
- (3) Load and line regulation are specified at a constant junction temperature. Pulse testing with a low duty cycle is used. Change in V_O because of heating effects is covered under the Thermal Regulation specification.
- (4) Selected devices with tightened tolerance reference voltage available.

- (5) C_{Adj} , when used, is connected between the adjustment pin and ground.
- (6) Since Long Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.
- (7) Power dissipation within an I.C. voltage regulator produces a temperature gradient on the die, affecting individual I.C. components on the die. These effects can be minimized by proper integrated circuit design and layout techniques. Thermal Regulation is the effect of these temperature gradients on the output voltage and is expressed in percentage of output change per watt of power change in a specified time.

LM137, LM237, LM337

SCHEMATIC DIAGRAM

3

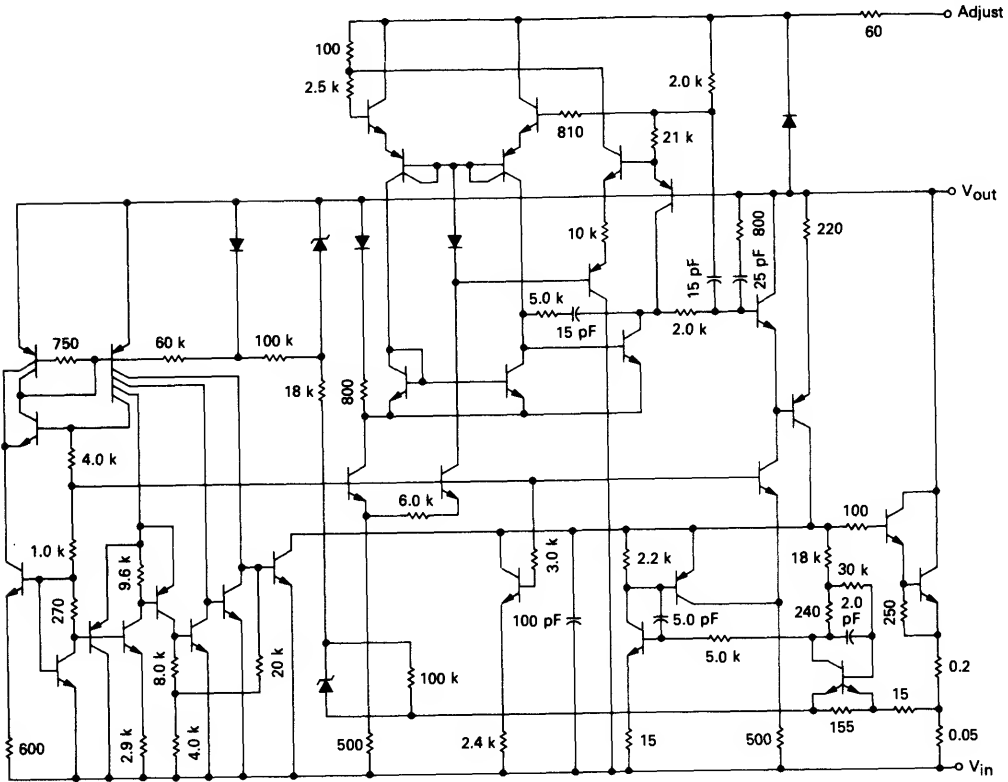
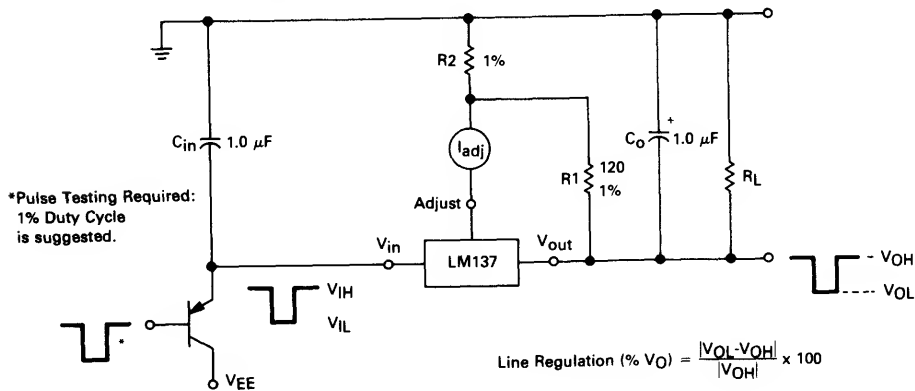


FIGURE 1 — LINE REGULATION AND ΔI_{Adj} /LINE TEST CIRCUIT



LM137, LM237, LM337

FIGURE 2 — LOAD REGULATION AND $\Delta I_{adj}/\text{LOAD}$ TEST CIRCUIT

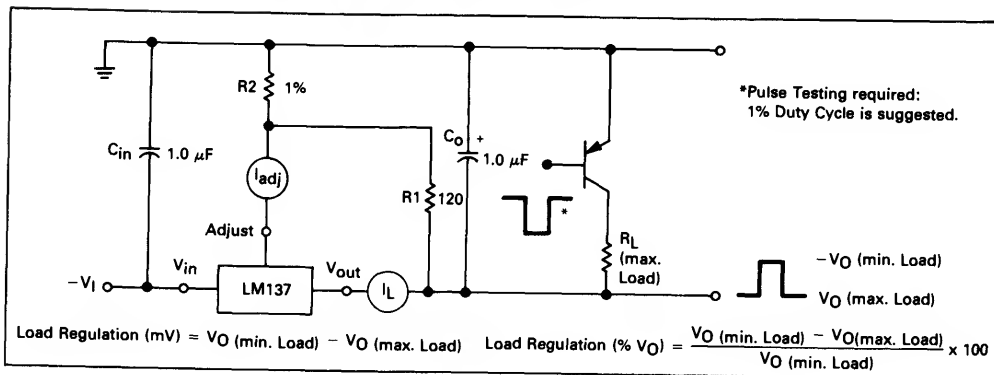


FIGURE 3 — STANDARD TEST CIRCUIT

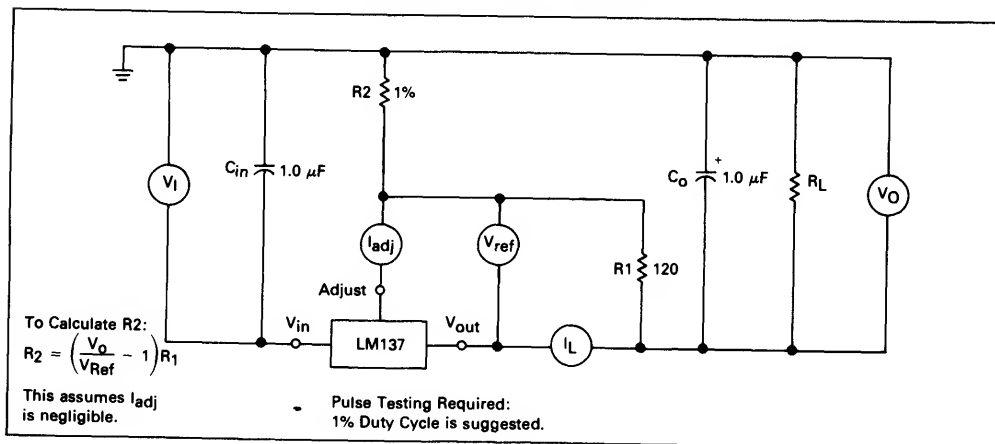


FIGURE 4 — RIPPLE REJECTION TEST CIRCUIT

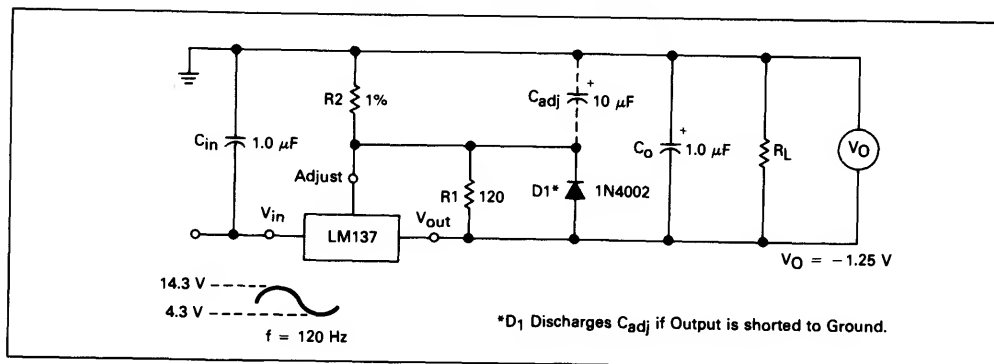


FIGURE 5 – LOAD REGULATION

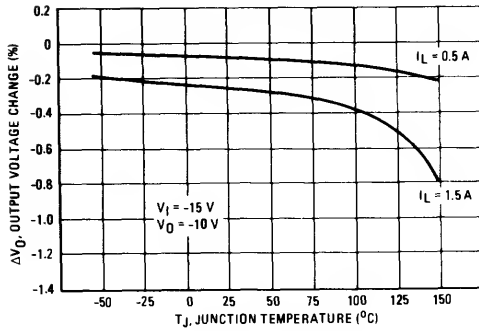


FIGURE 6 – CURRENT LIMIT

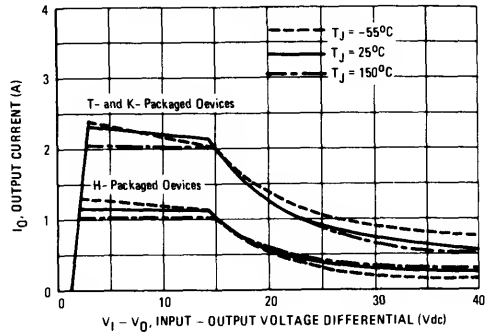


FIGURE 7 – ADJUSTMENT PIN CURRENT

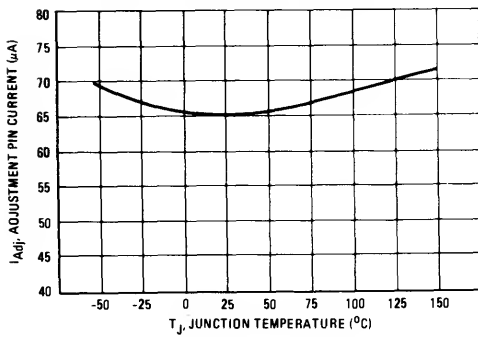


FIGURE 8 – DROPOUT VOLTAGE

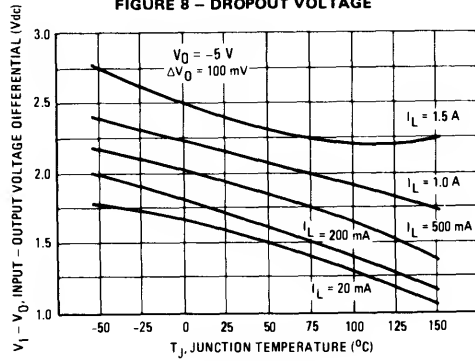


FIGURE 9 – TEMPERATURE STABILITY

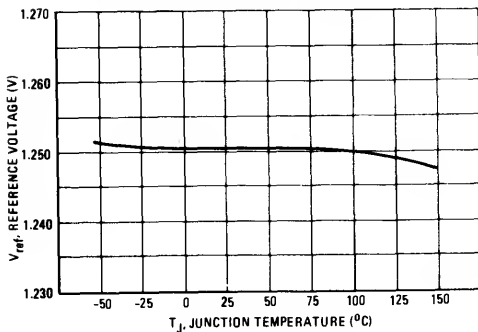


FIGURE 10 – MINIMUM OPERATING CURRENT

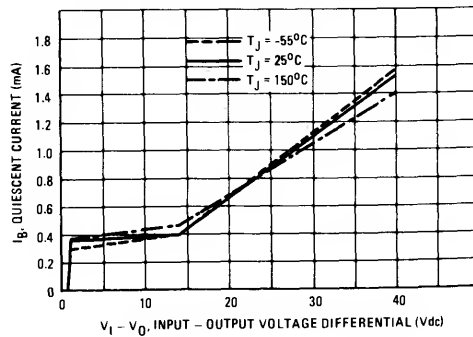


FIGURE 11 — RIPPLE REJECTION versus OUTPUT VOLTAGE

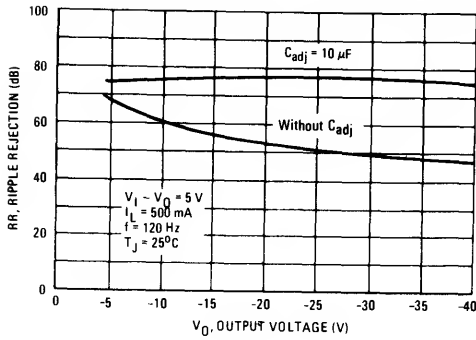


FIGURE 12 — RIPPLE REJECTION versus OUTPUT CURRENT

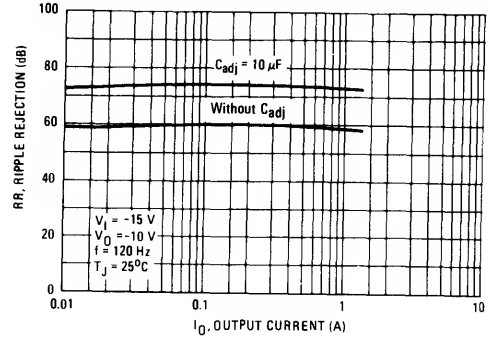


FIGURE 13 — RIPPLE REJECTION versus FREQUENCY

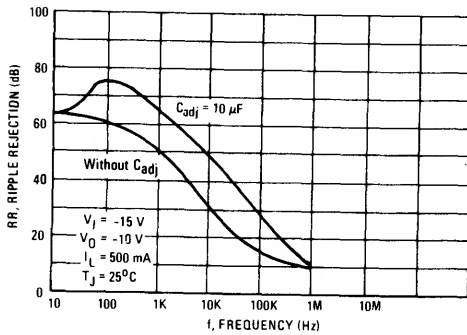


FIGURE 14 — OUTPUT IMPEDANCE

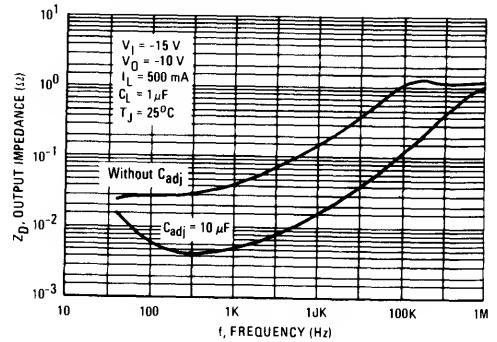


FIGURE 15 — LINE TRANSIENT RESPONSE

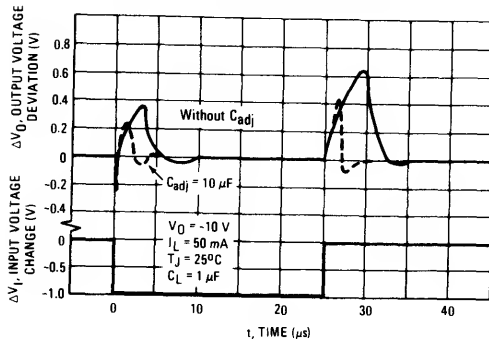
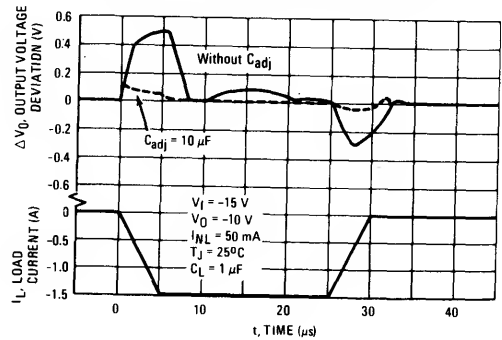


FIGURE 16 — LOAD TRANSIENT RESPONSE



APPLICATIONS INFORMATION

BASIC CIRCUIT OPERATION

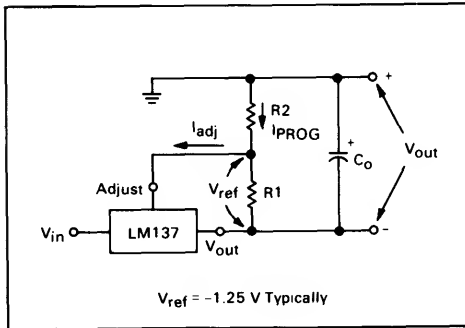
The LM137 is a 3-terminal floating regulator. In operation, the LM137 develops and maintains a nominal -1.25 volt reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by $R1$ (see Figure 17), and this constant current flows through $R2$ from ground. The regulated output voltage is given by:

$$V_{out} = V_{ref} \left(1 + \frac{R2}{R1}\right) + I_{adj} R2$$

Since the current into the adjustment terminal (I_{adj}) represents an error term in the equation, the LM137 was designed to control I_{adj} to less than $100 \mu A$ and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will increase.

Since the LM137 is a floating regulator, it is only the voltage differential across the circuit that is important to performance, and operation at high voltages with respect to ground is possible.

FIGURE 17 – BASIC CIRCUIT CONFIGURATION



LOAD REGULATION

The LM137 is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor ($R1$) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of $R2$ can be

returned near the load ground to provide remote ground sensing and improve load regulation.

EXTERNAL CAPACITORS

A $1 \mu F$ tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{adj}) prevents ripple from being amplified as the output voltage is increased. A $10 \mu F$ capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 volt application.

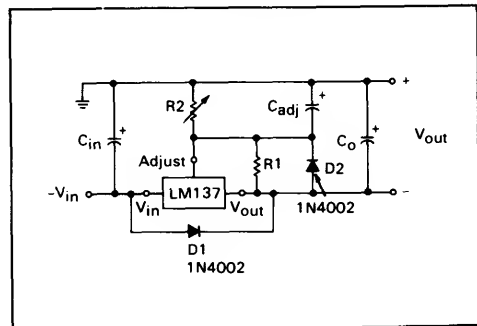
An output capacitor (C_o) in the form of a $1 \mu F$ tantalum or $10 \mu F$ aluminum electrolytic capacitor is required for stability.

PROTECTION DIODES

When external capacitors are used with any I.C. regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 18 shows the LM137 with the recommended protection diodes for output voltages in excess of -25 V or high capacitance values ($C_o > 25 \mu F$, $C_{adj} > 10 \mu F$). Diode $D1$ prevents C_o from discharging thru the I.C. during an input short circuit. Diode $D2$ protects against capacitor C_{adj} discharging through the I.C. during an output short circuit. The combination of diodes $D1$ and $D2$ prevents C_{adj} from discharging through the I.C. during an input short circuit.

FIGURE 18 – VOLTAGE REGULATOR WITH PROTECTION DIODES



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

3

THREE-TERMINAL POSITIVE VOLTAGE REGULATORS

This family of fixed voltage regulators are monolithic integrated circuits capable of driving loads in excess of 1.0 ampere. These three-terminal regulators employ internal current limiting, thermal shutdown, and safe-area compensation. Devices are available with improved specifications, including a 2% output voltage tolerance, on A-suffix 5.0, 12 and 15 volt device types.

Although designed primarily as a fixed voltage regulator, these devices can be used with external components to obtain adjustable voltages and currents. This series of devices can be used with a series-pass transistor to boost output current capability at the nominal output voltage.

- Output Current in Excess of 1.0 Ampere
- No External Components Required
- Output Voltage Offered in 2% and 4% Tolerance*
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation

ORDERING INFORMATION

Device	Output Voltage and Tolerance	Tested Operating Junction Temp. Range	Package
LM140K-5.0	5.0 V \pm 4%	-55°C to +150°C	Metal Power
LM140AK-5.0	5.0 V \pm 2%		
LM140K-8.0	8.0 V \pm 4%		
LM140K-12	12 V \pm 4%		
LM140AK-12	12 V \pm 2%		
LM140K-15	15 V \pm 4%		
LM140AK-15	15 V \pm 2%	0°C to +125°C	Metal Power
LM340K-5.0	5.0 V \pm 4%		Plastic Power
LM340AK-5.0	5.0 V \pm 2%		Plastic Power
LM340T-5.0	5.0 V \pm 4%		Metal Power
LM340AT-5.0	5.0 V \pm 2%		Plastic Power
LM340K-6.0	6.0 V \pm 4%		Metal Power
LM340K-8.0	8.0 V \pm 4%		Plastic Power
LM340T-8.0	8.0 V \pm 4%		Metal Power
LM340K-12	12 V \pm 4%		Plastic Power
LM340AK-12	12 V \pm 2%		Metal Power
LM340T-12	12 V \pm 4%		Plastic Power
LM340AT-12	12 V \pm 2%		Metal Power
LM340K-15	15 V \pm 4%		Plastic Power
LM340AK-15	15 V \pm 2%		Metal Power
LM340T-15	15 V \pm 4%		Plastic Power
LM340AT-15	15 V \pm 2%		Metal Power
LM340T-18	18 V \pm 4%		Plastic Power
LM340T-24	24 V \pm 4%		Plastic Power

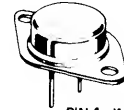
*2% regulators are available in 5, 12 and 15 volt devices

LM140,A Series LM340,A Series

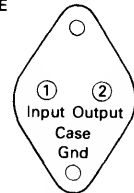
THREE-TERMINAL POSITIVE FIXED VOLTAGE REGULATORS

SILICON MONOLITHIC INTEGRATED CIRCUIT

K SUFFIX METAL PACKAGE CASE 1

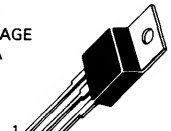


PIN 1. INPUT
2. OUTPUT
CASE GROUND



(Bottom View)

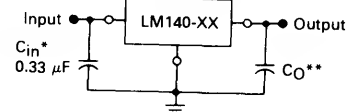
T SUFFIX PLASTIC PACKAGE CASE 221A



PIN 1. INPUT
2. GROUND
3. OUTPUT

(Heatsink surface connected to Pin 2)

STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 1.7 V above the output voltage even during the low point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

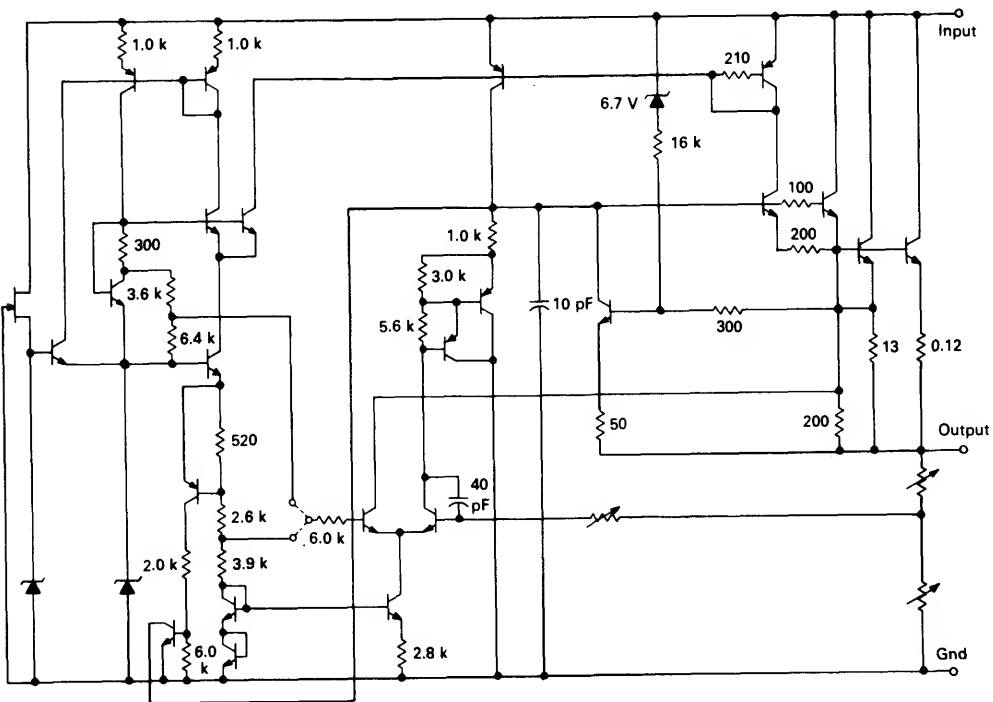
** = C_0 is not needed for stability; however, it does improve transient response. If needed, use a 0.1 μ F ceramic disc.

LM140,A, LM340,A

MAXIMUM RATINGS ($T_A = +25^{\circ}\text{C}$ unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (5.0 V – 18 V) (24 V)	V_{in}	35 40	Vdc
Power Dissipation and Thermal Characteristics			
Plastic Package			
$T_A = +25^{\circ}\text{C}$	P_D	Internally Limited	Watts
Derate above $T_A = +25^{\circ}\text{C}$	$1/\theta_{JA}$	15.4	mW/ $^{\circ}\text{C}$
Thermal Resistance, Junction to Air	θ_{JA}	65	$^{\circ}\text{C/W}$
$T_C = +25^{\circ}\text{C}$	P_D	Internally Limited	Watts
Derate above $T_C = +75^{\circ}\text{C}$ (See Figure 1)	$1/\theta_{JC}$	200	mW/ $^{\circ}\text{C}$
Thermal Resistance, Junction to Case	θ_{JC}	5.0	$^{\circ}\text{C/W}$
Metal Package			
$T_C = +25^{\circ}\text{C}$	P_D	Internally Limited	Watts
Derate above $T_A = +25^{\circ}\text{C}$	$1/\theta_{JA}$	22.5	mW/ $^{\circ}\text{C}$
Thermal Resistance, Junction to Air	θ_{JA}	45	$^{\circ}\text{C/W}$
$T_C = +25^{\circ}\text{C}$	P_D	Internally Limited	Watts
Derate above $T_C = +65^{\circ}\text{C}$ (See Figure 2)	$1/\theta_{JC}$	182	mW/ $^{\circ}\text{C}$
Thermal Resistance, Junction to Case	θ_{JC}	5.5	$^{\circ}\text{C/W}$
Storage Junction Temperature Range	T_{stg}	- 65 to + 150	$^{\circ}\text{C}$
Operating Junction Temperature Range	T_J	- 55 to + 150 0 to + 150	$^{\circ}\text{C}$

EQUIVALENT SCHEMATIC DIAGRAM



LM140,A, LM340,A

DEFINITIONS

Line Regulation — The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation — The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation — The maximum total device

dissipation for which the regulator will operate within specifications.

Quiescent Current — That part of the input current that is not delivered to the load.

Output Noise Voltage — The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

LM140/340 — 5.0

ELECTRICAL CHARACTERISTICS ($V_{in} = 10\text{ V}$, $I_O = 500\text{ mA}$, $T_J = T_{low}$ to T_{high} (Note 1), unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^\circ\text{C}$) $I_O = 5.0\text{ mA to }1.0\text{ A}$	V_O	4.8	5.0	5.2	Vdc
Line Regulation (Note 2) 8.0 to 20 Vdc 7.0 to 25 Vdc ($T_J = +25^\circ\text{C}$) 8.0 to 12 Vdc, $I_O = 1.0\text{ A}$ 7.3 to 20 Vdc, $I_O = 1.0\text{ A}$ ($T_J = +25^\circ\text{C}$)	Regline	—	—	50 50 25 50	mV
Load Regulation (Note 2) 5.0 mA $\leq I_O \leq 1.0\text{ A}$ 5.0 mA $\leq I_O \leq 1.5\text{ A}$ ($T_J = +25^\circ\text{C}$) 250 mA $\leq I_O \leq 750\text{ mA}$ ($T_J = +25^\circ\text{C}$)	Regload	—	—	50 50 25	mV
Output Voltage LM140 8.0 $\leq V_{in} \leq 20\text{ Vdc}$, 5.0 mA $\leq I_O \leq 1.0\text{ A}$, $P_D \leq 15\text{ W}$ LM340 7.0 $\leq V_{in} \leq 20\text{ Vdc}$, 5.0 mA $\leq I_O \leq 1.0\text{ A}$, $P_D \leq 15\text{ W}$	V_O	4.75	—	5.25	Vdc
Quiescent Current $I_O = 1.0\text{ A}$ LM140 LM340 LM140 ($T_J = +25^\circ\text{C}$) LM340 ($T_J = +25^\circ\text{C}$)	I_B	—	—	7.0 8.5 6.0 8.0	mA
Quiescent Current Change 8.0 $\leq V_{in} \leq 25\text{ Vdc}$, $I_O = 500\text{ mA}$ LM140 7.0 $\leq V_{in} \leq 25\text{ Vdc}$, $I_O = 500\text{ mA}$ LM340 5.0 mA $\leq I_O \leq 1.0\text{ A}$, $V_{in} = 10\text{ V}$ LM140, LM340 8.0 $\leq V_{in} \leq 20\text{ Vdc}$, $I_O = 1.0\text{ A}$ LM140 7.5 $\leq V_{in} \leq 20\text{ Vdc}$, $I_O = 1.0\text{ A}$ LM340	ΔI_B	—	—	0.8 1.0 0.5 0.8 1.0	mA
Ripple Rejection LM140 LM340 $I_O = 1.0\text{ A}$ ($T_J = +25^\circ\text{C}$) LM140 LM340	RR	68 62 68 62	— — 80 80	— — — —	dB
Dropout Voltage	$V_{in} - V_O$	—	1.7	—	Vdc
Output Resistance ($f = 1.0\text{ kHz}$)	r_O	—	2.0	—	m Ω
Short-Circuit Current Limit ($T_J = +25^\circ\text{C}$)	I_{sc}	—	2.0	—	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$) 10 Hz $\leq f \leq 100\text{ kHz}$	V_n	—	40	—	μV
Average Temperature Coefficient of Output Voltage $I_O = 5.0\text{ mA}$	TCV_O	—	± 0.6	—	mV/ $^\circ\text{C}$
Peak Output Current ($T_J = +25^\circ\text{C}$)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation ($T_J = +25^\circ\text{C}$) $I_O = 1.0\text{ A}$		7.3	—	—	Vdc

NOTES: 1. $T_{low} = -55^\circ\text{C}$ for LM140 $T_{high} = +150^\circ\text{C}$ for LM140
 $= 0^\circ\text{C}$ for LM340 $= +125^\circ\text{C}$ for LM340

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

LM140,A, LM340,A

3

LM140A/340A — 5.0

ELECTRICAL CHARACTERISTICS ($V_{in} = 10\text{ V}$, $I_O = 1.0\text{ A}$, $T_J = T_{low}$ to T_{high} (Note 1), unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^\circ\text{C}$) $I_O = 5.0\text{ mA}$ to 1.0 A	V_O	4.9	5.0	5.1	Vdc
Line Regulation (Note 2) 7.5 to 20 Vdc, $I_O = 500\text{ mA}$ 7.3 to 20 Vdc ($T_J = +25^\circ\text{C}$) 8.0 to 12 Vdc 8.0 to 12 Vdc ($T_J = +25^\circ\text{C}$)	Regline	— — — —	— 3.0 — —	10 10 12 4.0	mV
Load Regulation (Note 2) 5.0 mA $\leq I_O \leq 1.0\text{ A}$ 5.0 mA $\leq I_O \leq 1.5\text{ A}$ ($T_J = +25^\circ\text{C}$) 250 mA $\leq I_O \leq 750\text{ mA}$ ($T_J = +25^\circ\text{C}$)	Regload	— — — —	— — — —	25 25 15	mV
Output Voltage 7.5 $\leq V_{in} \leq 20\text{ Vdc}$, 5.0 mA $\leq I_O \leq 1.0\text{ A}$, $P_D \leq 15\text{ W}$	V_O	4.8	—	5.2	Vdc
Quiescent Current ($T_J = +25^\circ\text{C}$)	I_B	— —	— 3.5	6.5 6.0	mA
Quiescent Current Change 5.0 mA $\leq I_O \leq 1.0\text{ A}$, $V_{in} = 10\text{ V}$ 8.0 $\leq V_{in} \leq 25\text{ Vdc}$, $I_O = 500\text{ mA}$ 7.5 $\leq V_{in} \leq 20\text{ Vdc}$, $I_O = 1.0\text{ A}$ ($T_J = +25^\circ\text{C}$)	ΔI_B	— — —	— — —	0.5 0.8 0.8	mA
Ripple Rejection 8.0 $\leq V_{in} \leq 18\text{ Vdc}$, $f = 120\text{ Hz}$ $I_O = 500\text{ mA}$ $I_O = 1.0\text{ A}$ ($T_J = +25^\circ\text{C}$)	RR	68 68	— 80	— —	dB
Dropout Voltage	$V_{in} - V_O$	—	1.7	—	Vdc
Output Resistance ($f = 1.0\text{ kHz}$)	r_O	—	2.0	—	m Ω
Short-Circuit Current Limit ($T_J = +25^\circ\text{C}$)	I_{sc}	—	2.0	—	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$) 10 Hz $\leq f \leq 100\text{ kHz}$	V_n	—	40	—	μV
Average Temperature Coefficient of Output Voltage $I_O = 5.0\text{ mA}$	TCVO	—	± 0.6	—	mV/ $^\circ\text{C}$
Peak Output Current ($T_J = +25^\circ\text{C}$)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation ($T_J = +25^\circ\text{C}$)		7.3	—	—	Vdc

NOTES:

- $T_{low} = -55^\circ\text{C}$ for LM140A $T_{high} = +150^\circ\text{C}$ for LM140A
= 0°C for LM340A = $+125^\circ\text{C}$ for LM340A
- Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used

LM140,A, LM340,A

LM140/340 — 6.0

ELECTRICAL CHARACTERISTICS ($V_{in} = 11\text{ V}$, $I_O = 500\text{ mA}$, $T_J = T_{low}$ to T_{high} (Note 1), unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^\circ\text{C}$) $I_O = 5.0\text{ mA to } 1.0\text{ A}$	V_O	5.75	6.0	6.25	Vdc
Line Regulation (Note 2) 9.0 to 21 Vdc 8.0 to 25 Vdc ($T_J = +25^\circ\text{C}$) 9.0 to 13 Vdc, $I_O = 1.0\text{ A}$ 8.3 to 21 Vdc, $I_O = 1.0\text{ A}$ ($T_J = +25^\circ\text{C}$)	Reg _{line}	— — — —	— — — —	60 60 30 60	mV
Load Regulation (Note 2) 5.0 mA $\leq I_O \leq 1.0\text{ A}$ 5.0 mA $\leq I_O \leq 1.5\text{ A}$ ($T_J = +25^\circ\text{C}$) 250 mA $\leq I_O \leq 750\text{ mA}$ ($T_J = +25^\circ\text{C}$)	Reg _{load}	— — —	— — —	60 60 30	mV
Output Voltage LM140 9.0 $\leq V_{in} \leq 21\text{ Vdc}$, 5.0 mA $\leq I_O \leq 1.0\text{ A}$, $P_D \leq 15\text{ W}$ LM340 8.0 $\leq V_{in} \leq 21\text{ Vdc}$, 6.0 mA $\leq I_O \leq 1.0\text{ A}$, $P_D \leq 15\text{ W}$	V_O	5.7 5.7	— —	6.3 6.3	Vdc
Quiescent Current $I_O = 1.0\text{ A}$ LM140 LM340 LM140 ($T_J = +25^\circ\text{C}$) LM340 ($T_J = +25^\circ\text{C}$)	I_B	— — — —	— — 4.0 4.0	7.0 8.5 6.0 8.0	mA
Quiescent Current Change 9.0 $\leq V_{in} \leq 25\text{ Vdc}$, $I_O = 500\text{ mA}$ LM140 8.0 $\leq V_{in} \leq 25\text{ Vdc}$, $I_O = 500\text{ mA}$ LM340 5.0 mA $\leq I_O \leq 1.0\text{ A}$, $V_{in} = 11\text{ V}$ LM140, LM340 9.0 $\leq V_{in} \leq 21\text{ Vdc}$, $I_O = 1.0\text{ A}$ LM140 8.6 $\leq V_{in} \leq 21\text{ Vdc}$, $I_O = 1.0\text{ A}$ LM340	ΔI_B	— — — — —	— — — — —	0.8 1.0 0.5 0.8 1.0	mA
Ripple Rejection LM140 LM340 $I_O = 1.0\text{ A}$ ($T_J = +25^\circ\text{C}$) LM140 LM340	RR	65 59 65 59	— — 78 78	— — — —	dB
Dropout Voltage	$V_{in} - V_O$	—	1.7	—	Vdc
Output Resistance ($f = 1.0\text{ kHz}$)	r_O	—	2.0	—	m Ω
Short-Circuit Current Limit ($T_J = +25^\circ\text{C}$)	I_{sc}	—	1.9	—	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$) 10 Hz $\leq f \leq 100\text{ kHz}$	V_n	—	45	—	μV
Average Temperature Coefficient of Output Voltage $I_O = 5.0\text{ mA}$	TCV_O	—	± 0.7	—	mV/ $^\circ\text{C}$
Peak Output Current ($T_J = +25^\circ\text{C}$)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation ($T_J = +25^\circ\text{C}$) $I_O = 1.0\text{ A}$		8.3	—	—	Vdc

NOTES:

- $T_{low} = -55^\circ\text{C}$ for LM140 $T_{high} = +150^\circ\text{C}$ for LM140
 $= 0^\circ\text{C}$ for LM340 $= +125^\circ\text{C}$ for LM340

- Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

LM140,A, LM340,A

3

LM140/340 — 8.0

ELECTRICAL CHARACTERISTICS ($V_{in} = 14\text{ V}$, $I_O = 500\text{ mA}$, $T_J = T_{low}$ to T_{high} (Note 1), unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^\circ\text{C}$) $I_O = 5.0\text{ mA}$ to 1.0 A	V_O	7.7	8.0	8.3	Vdc
Line Regulation (Note 2) 11 to 23 Vdc 10.5 to 25 Vdc ($T_J = +25^\circ\text{C}$) 11 to 17 Vdc, $I_O = 1.0\text{ A}$ 10.5 to 23 Vdc, $I_O = 1.0\text{ A}$ ($T_J = +25^\circ\text{C}$)	Reg _{line}	— — — —	— — — —	80 80 40 80	mV
Load Regulation (Note 2) 5.0 mA $\leq I_O \leq 1.0\text{ A}$ 5.0 mA $\leq I_O \leq 1.5\text{ A}$ ($T_J = +25^\circ\text{C}$) 250 mA $\leq I_O \leq 750\text{ mA}$ ($T_J = +25^\circ\text{C}$)	Reg _{load}	— — —	— — —	80 80 40	mV
Output Voltage LM140 11.5 $\leq V_{in} \leq 23\text{ Vdc}$, 5.0 mA $\leq I_O \leq 1.0\text{ A}$, $P_D \leq 15\text{ W}$ LM340 10.5 $\leq V_{in} \leq 23\text{ Vdc}$, 5.0 mA $\leq I_O \leq 1.0\text{ A}$, $P_D \leq 15\text{ W}$	V_O	7.6 7.6	— —	8.4 8.4	Vdc
Quiescent Current $I_O = 1.0\text{ A}$ LM140 LM340 LM140 ($T_J = +25^\circ\text{C}$) LM340 ($T_J = +25^\circ\text{C}$)	I_B	— — — —	— — 4.0 4.0	7.0 8.5 6.0 8.0	mA
Quiescent Current Change 11.5 $\leq V_{in} \leq 25\text{ Vdc}$, $I_O = 500\text{ mA}$ LM140 10.5 $\leq V_{in} \leq 25\text{ Vdc}$, $I_O = 500\text{ mA}$ LM340 5.0 mA $\leq I_O \leq 1.0\text{ A}$, $V_{in} = 14\text{ V}$ LM140, LM340 11.5 $\leq V_{in} \leq 23\text{ Vdc}$, $I_O = 1.0\text{ A}$ LM140 10.6 $\leq V_{in} \leq 23\text{ Vdc}$, $I_O = 1.0\text{ A}$ LM340	ΔI_B	— — — — —	— — — — —	0.8 1.0 0.5 0.8 1.0	mA
Ripple Rejection LM140 LM340 $I_O = 1.0\text{ A}$ ($T_J = +25^\circ\text{C}$) LM140 LM340	RR	62 56 62 56	— — 76 76	— — — —	dB
Dropout Voltage	$V_{in} - V_O$	—	1.7	—	Vdc
Output Resistance ($f = 1.0\text{ kHz}$)	r_O	—	2.0	—	m Ω
Short-Circuit Current Limit ($T_J = +25^\circ\text{C}$)	I_{sc}	—	1.5	—	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$) 10 Hz $\leq f \leq 100\text{ kHz}$	V_n	—	52	—	μV
Average Temperature Coefficient of Output Voltage $I_O = 5.0\text{ mA}$	TCV_O	—	± 1.0	—	mV/ $^\circ\text{C}$
Peak Output Current ($T_J = +25^\circ\text{C}$)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation ($T_J = +25^\circ\text{C}$) $I_O = 1.0\text{ A}$		10.5	—	—	Vdc

NOTES:

- $T_{low} = -55^\circ\text{C}$ for LM140 $T_{high} = +150^\circ\text{C}$ for LM140
= 0°C for LM340 = $+125^\circ\text{C}$ for LM340
- Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

LM140,A, LM340,A

LM140/340 — 12

ELECTRICAL CHARACTERISTICS ($V_{in} = 19\text{ V}$, $I_O = 500\text{ mA}$, $T_J = T_{low}$ to T_{high} (Note 1), unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^\circ\text{C}$) $I_O = 5.0\text{ mA to }1.0\text{ A}$	V_O	11.5	12	12.5	Vdc
Line Regulation (Note 2) 15 to 27 Vdc 14.6 to 30 Vdc ($T_J = +25^\circ\text{C}$) 16 to 22 Vdc, $I_O = 1.0\text{ A}$ 14.6 to 27 Vdc, $I_O = 1.0\text{ A}$ ($T_J = +25^\circ\text{C}$)	Reg _{line}	—	—	120 120 60 120	mV
Load Regulation (Note 2) 5.0 mA $\leq I_O \leq 1.0\text{ A}$ 5.0 mA $\leq I_O \leq 1.5\text{ A}$ ($T_J = +25^\circ\text{C}$) 250 mA $\leq I_O \leq 750\text{ mA}$ ($T_J = +25^\circ\text{C}$)	Reg _{load}	—	—	120 120 60	mV
Output Voltage LM140 15.5 $\leq V_{in} \leq 27\text{ Vdc}$, 5.0 mA $\leq I_O \leq 1.0\text{ A}$, $P_D \leq 15\text{ W}$ LM340 14.5 $\leq V_{in} \leq 27\text{ Vdc}$, 5.0 mA $\leq I_O \leq 1.0\text{ A}$, $P_D \leq 15\text{ W}$	V_O	11.4 11.4	—	12.6 12.6	Vdc
Quiescent Current $I_O = 1.0\text{ A}$ LM140 LM340 LM140 ($T_J = +25^\circ\text{C}$) LM340 ($T_J = +25^\circ\text{C}$)	I_B	— — — —	— — 4.0 4.0	7.0 8.5 6.0 8.0	mA
Quiescent Current Change 15 $\leq V_{in} \leq 30\text{ Vdc}$, $I_O = 500\text{ mA}$ LM140 14.5 $\leq V_{in} \leq 30\text{ Vdc}$, $I_O = 500\text{ mA}$ LM340 5.0 mA $\leq I_O \leq 1.0\text{ A}$, $V_{in} = 19\text{ V}$ LM140, LM340 15 $\leq V_{in} \leq 27\text{ Vdc}$, $I_O = 1.0\text{ A}$ LM140 14.8 $\leq V_{in} \leq 27\text{ Vdc}$, $I_O = 1.0\text{ A}$ LM340	ΔI_B	— — — — —	— — — — —	0.8 1.0 0.5 0.8 1.0	mA
Ripple Rejection LM140 LM340 $I_O = 1.0\text{ A}$ ($T_J = +25^\circ\text{C}$) LM140 LM340	RR	61 55 61 55	— — 72 72	— — — —	dB
Dropout Voltage	$V_{in} - V_O$	—	1.7	—	Vdc
Output Resistance ($f = 1.0\text{ kHz}$)	r_O	—	2.0	—	m Ω
Short-Circuit Current Limit ($T_J = +25^\circ\text{C}$)	I_{sc}	—	1.1	—	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$) 10 Hz $\leq f \leq 100\text{ kHz}$	V_n	—	75	—	μV
Average Temperature Coefficient of Output Voltage $I_O = 5.0\text{ mA}$	TCV_O	—	± 1.5	—	mV/ $^\circ\text{C}$
Peak Output Current ($T_J = +25^\circ\text{C}$)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation ($T_J = +25^\circ\text{C}$) $I_O = 1.0\text{ A}$		14.6	—	—	Vdc

NOTES:

- $T_{low} = -55^\circ\text{C}$ for LM140 $T_{high} = +150^\circ\text{C}$ for LM140
= $+125^\circ\text{C}$ for LM340
- Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

LM140,A, LM340,A

LM140A/340A — 12

ELECTRICAL CHARACTERISTICS ($V_{in} = 19\text{ V}$, $I_O = 1.0\text{ A}$, $T_J = T_{low}$ to T_{high} (Note 1), unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^\circ\text{C}$) $I_O = 5.0\text{ mA}$ to 1.0 A	V_O	11.75	12	12.25	Vdc
Line Regulation (Note 2) 14.8 to 27 Vdc, $I_O = 500\text{ mA}$ 14.5 to 27 Vdc ($T_J = +25^\circ\text{C}$) 16 to 22 Vdc 16 to 22 Vdc ($T_J = +25^\circ\text{C}$)	Reg _{line}	—	— 4.0	18 18 30 9.0	mV
Load Regulation (Note 2) 5.0 mA $\leq I_O \leq 1.0\text{ A}$ 5.0 mA $\leq I_O \leq 1.5\text{ A}$ ($T_J = +25^\circ\text{C}$) 250 mA $\leq I_O \leq 750\text{ mA}$ ($T_J = +25^\circ\text{C}$)	Reg _{load}	—	—	60 32 19	mV
Output Voltage 14.8 $\leq V_{in} \leq 27\text{ Vdc}$, 5.0 mA $\leq I_O \leq 1.0\text{ A}$, $P_D \leq 15\text{ W}$	V_O	11.5	—	12.5	Vdc
Quiescent Current ($T_J = +25^\circ\text{C}$)	I_B	—	— 3.5	6.5 6.0	mA
Quiescent Current Change 5.0 mA $\leq I_O \leq 1.0\text{ A}$, $V_{in} = 19\text{ V}$ 15 $\leq V_{in} \leq 30\text{ Vdc}$, $I_O = 500\text{ mA}$ 14.8 $\leq V_{in} \leq 27\text{ Vdc}$, $I_O = 1.0\text{ A}$ ($T_J = +25^\circ\text{C}$)	ΔI_B	—	—	0.5 0.8 0.8	mA
Ripple Rejection 15 $\leq V_{in} \leq 25\text{ Vdc}$, $f = 120\text{ Hz}$ $I_O = 500\text{ mA}$ $I_O = 1.0\text{ A}$, ($T_J = +25^\circ\text{C}$)	RR	61 61	— 72	— —	dB
Dropout Voltage	$V_{in} - V_O$	—	1.7	—	Vdc
Output Resistance ($f = 1.0\text{ kHz}$)	r_O	—	2.0	—	m Ω
Short-Circuit Current Limit ($T_J = +25^\circ\text{C}$)	I_{sc}	—	1.1	—	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$) 10 Hz $\leq f \leq 100\text{ kHz}$	V_n	—	75	—	μV
Average Temperature Coefficient of Output Voltage $I_O = 5.0\text{ mA}$	TCV_O	—	± 1.5	—	mV/ $^\circ\text{C}$
Peak Output Current ($T_J = +25^\circ\text{C}$)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation ($T_J = +25^\circ\text{C}$)		14.5	—	—	Vdc

NOTES:

- $T_{low} = -55^\circ\text{C}$ for LM140A $T_{high} = +150^\circ\text{C}$ for LM140A
 $= 0^\circ\text{C}$ for LM340A $= +125^\circ\text{C}$ for LM340A
- Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

LM140,A, LM340,A

LM140A/340 — 15

ELECTRICAL CHARACTERISTICS ($V_{in} = 23\text{ V}$, $I_O = 500\text{ mA}$, $T_J = T_{low}$ to T_{high} (Note 1), unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^\circ\text{C}$) $I_O = 5.0\text{ mA}$ to 1.0 A	V_O	14.4	15	15.6	Vdc
Line Regulation (Note 2) 18.5 to 30 Vdc 17.5 to 30 Vdc ($T_J = +25^\circ\text{C}$) 20 to 26 Vdc, $I_O = 1.0\text{ A}$ 17.7 to 30 Vdc, $I_O = 1.0\text{ A}$ ($T_J = +25^\circ\text{C}$)	Reg _{line}	—	—	150 150 75 150	mV
Load Regulation (Note 2) 5.0 mA $\leq I_O \leq 1.0\text{ A}$ 5.0 mA $\leq I_O \leq 1.5\text{ A}$ ($T_J = +25^\circ\text{C}$) 250 mA $\leq I_O \leq 750\text{ mA}$ ($T_J = +25^\circ\text{C}$)	Reg _{load}	—	—	150 150 75	mV
Output Voltage LM140 18.5 $\leq V_{in} \leq 30\text{ Vdc}$, 5.0 mA $\leq I_O \leq 1.0\text{ A}$, $P_D \leq 15\text{ W}$ LM340 17.5 $\leq V_{in} \leq 30\text{ Vdc}$, 5.0 mA $\leq I_O \leq 1.0\text{ A}$, $P_D \leq 15\text{ W}$	V_O	14.25 14.25	— —	15.75 15.75	Vdc
Quiescent Current $I_O = 1.0\text{ A}$ LM140 LM340 LM140 ($T_J = +25^\circ\text{C}$) LM340 ($T_J = +25^\circ\text{C}$)	I_B	— — — —	— — 4.0 4.0	7.0 8.5 6.0 8.0	mA
Quiescent Current Change 18.5 $\leq V_{in} \leq 30\text{ Vdc}$, $I_O = 500\text{ mA}$ LM140 17.5 $\leq V_{in} \leq 30\text{ Vdc}$, $I_O = 500\text{ mA}$ LM340 5.0 mA $\leq I_O \leq 1.0\text{ A}$, $V_{in} = 23\text{ V}$ LM140, LM340 18.5 $\leq V_{in} \leq 30\text{ Vdc}$, $I_O = 1.0\text{ A}$ LM140 17.9 $\leq V_{in} \leq 30\text{ Vdc}$, $I_O = 1.0\text{ A}$ LM340	ΔI_B	— — — — —	— — — — —	0.8 1.0 0.5 0.8 1.0	mA
Ripple Rejection LM140 LM340 $I_O = 1.0\text{ A}$ ($T_J = +25^\circ\text{C}$) LM140 LM340	RR	60 54 60 54	— — 70 70	— — — —	dB
Dropout Voltage	$V_{in} - V_O$	—	1.7	—	Vdc
Output Resistance ($f = 1.0\text{ kHz}$)	r_O	—	2.0	—	m Ω
Short-Circuit Current Limit ($T_J = +25^\circ\text{C}$)	I_{sc}	—	800	—	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$) 10 Hz $\leq f \leq 100\text{ kHz}$	V_n	—	90	—	μV
Average Temperature Coefficient of Output Voltage $I_O = 5.0\text{ mA}$	TCV_O	—	± 1.8	—	mV/ $^\circ\text{C}$
Peak Output Current ($T_J = +25^\circ\text{C}$)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation ($T_J = +25^\circ\text{C}$) $I_O = 1.0\text{ A}$		17.7	—	—	Vdc

NOTES:

- $T_{low} = -55^\circ\text{C}$ for LM140 $T_{high} = +150^\circ\text{C}$ for LM140
= $+125^\circ\text{C}$ for LM340
- Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

LM140,A, LM340,A

LM140A/340A — 15

ELECTRICAL CHARACTERISTICS ($V_{in} = 23 \text{ V}$, $I_O = 1.0 \text{ A}$, $T_J = T_{low} \text{ to } T_{high}$ (Note 1), unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^\circ\text{C}$) $I_O = 5.0 \text{ mA to } 1.0 \text{ A}$	V_O	14.7	15	15.3	Vdc
Line Regulation (Note 2) 17.9 to 30 Vdc, $I_O = 500 \text{ mA}$ 17.5 to 30 Vdc ($T_J = +25^\circ\text{C}$) 20 to 26 Vdc, $I_O = 1.0 \text{ A}$ 20 to 26 Vdc, $I_O = 1.0 \text{ A}$ ($T_J = +25^\circ\text{C}$)	Regline	— — — —	— 4.0 — —	22 22 30 10	mV
Load Regulation (Note 2) $5.0 \text{ mA} \leq I_O \leq 1.0 \text{ A}$ $5.0 \text{ mA} \leq I_O \leq 1.5 \text{ A}$ ($T_J = +25^\circ\text{C}$) $250 \text{ mA} \leq I_O \leq 750 \text{ mA}$ ($T_J = +25^\circ\text{C}$)	Regload	— — —	— 12 —	75 35 21	mV
Output Voltage $17.9 \leq V_{in} \leq 30 \text{ Vdc}$, $5.0 \text{ mA} \leq I_O \leq 1.0 \text{ A}$, $P_D \leq 15 \text{ W}$	V_O	14.4	—	15.6	Vdc
Quiescent Current ($T_J = +25^\circ\text{C}$)	I_B	— —	— 3.5	6.5 6.0	mA
Quiescent Current Change $5.0 \text{ mA} \leq I_O \leq 1.0 \text{ A}$, $V_{in} = 23 \text{ V}$ $17.9 \leq V_{in} \leq 30 \text{ Vdc}$, $I_O = 500 \text{ mA}$ $17.9 \leq V_{in} \leq 30 \text{ Vdc}$, $I_O = 1.0 \text{ A}$ ($T_J = +25^\circ\text{C}$)	ΔI_B	— — —	— — —	0.5 0.8 0.8	mA
Ripple Rejection $18.5 \leq V_{in} \leq 28.5 \text{ Vdc}$, $f = 120 \text{ Hz}$ $I_O = 500 \text{ mA}$ $I_O = 1.0 \text{ A}$, ($T_J = +25^\circ\text{C}$)	RR	60 60	— 70	— —	dB
Dropout Voltage	$V_{in} - V_O$	—	1.7	—	Vdc
Output Resistance ($f = 1.0 \text{ kHz}$)	r_O	—	2.0	—	m Ω
Short-Circuit Current Limit ($T_J = +25^\circ\text{C}$)	I_{sc}	—	800	—	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$) $10 \text{ Hz} \leq f \leq 100 \text{ kHz}$	V_n	—	90	—	μV
Average Temperature Coefficient of Output Voltage $I_O = 5.0 \text{ mA}$	TCV_O	—	± 1.8	—	mV/ $^\circ\text{C}$
Peak Output Current ($T_J = +25^\circ\text{C}$)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation ($T_J = +25^\circ\text{C}$)		17.5	—	—	Vdc

NOTES:

1. $T_{low} = -55^\circ\text{C}$ for LM140A $T_{high} = +150^\circ\text{C}$ for LM140A
= 0°C for LM340A = $+125^\circ\text{C}$ for LM340A

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

LM140,A, LM340,A

LM140/340 — 18

ELECTRICAL CHARACTERISTICS ($V_{in} = 27\text{ V}$, $I_O = 500\text{ mA}$, $T_J = T_{low}$ to T_{high} (Note 1), unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^\circ\text{C}$) $I_O = 5.0\text{ mA}$ to 1.0 A	V_O	17.3	18	18.7	Vdc
Line Regulation (Note 2) 21.5 to 33 Vdc 21 to 33 Vdc ($T_J = +25^\circ\text{C}$) 24 to 30 Vdc, $I_O = 1.0\text{ A}$ 21 to 33 Vdc, $I_O = 1.0\text{ A}$ ($T_J = +25^\circ\text{C}$)	Regline	— — — —	— — — —	180 180 90 180	mV
Load Regulation (Note 2) 5.0 mA $\leq I_O \leq 1.0\text{ A}$ 5.0 mA $\leq I_O \leq 1.5\text{ A}$ ($T_J = +25^\circ\text{C}$) 250 mA $\leq I_O \leq 750\text{ mA}$ ($T_J = +25^\circ\text{C}$)	Regload	— — —	— — —	180 180 90	mV
Output Voltage LM140 22 $\leq V_{in} \leq 33\text{ Vdc}$, 5.0 mA $\leq I_O \leq 1.0\text{ A}$, $P_D \leq 15\text{ W}$ LM340 21 $\leq V_{in} \leq 33\text{ Vdc}$, 5.0 mA $\leq I_O \leq 1.0\text{ A}$, $P_D \leq 15\text{ W}$	V_O	17.1 17.1	— —	18.9 18.9	Vdc
Quiescent Current $I_O = 1.0\text{ A}$ LM140 LM340 LM140 ($T_J = +25^\circ\text{C}$) LM340 ($T_J = +25^\circ\text{C}$)	I_B	— — — —	— — 4.0 4.0	7.0 8.5 6.0 8.0	mA
Quiescent Current Change 22 $\leq V_{in} \leq 33\text{ Vdc}$, $I_O = 500\text{ mA}$ LM140 21 $\leq V_{in} \leq 33\text{ Vdc}$, $I_O = 500\text{ mA}$ LM340 5.0 mA $\leq I_O \leq 1.0\text{ A}$, $V_{in} = 27\text{ V}$ LM140, LM340 22 $\leq V_{in} \leq 33\text{ Vdc}$, $I_O = 1.0\text{ A}$ LM140 21 $\leq V_{in} \leq 33\text{ Vdc}$, $I_O = 1.0\text{ A}$ LM340	ΔI_B	— — — — —	— — — — —	0.8 1.0 0.5 0.8 1.0	mA
Ripple Rejection LM140 LM340 $I_O = 1.0\text{ A}$ ($T_J = +25^\circ\text{C}$) LM140 LM340	RR	59 53 59 53	— — 69 69	— — — —	dB
Dropout Voltage	$V_{in} - V_O$	—	1.7	—	Vdc
Output Resistance ($f = 1.0\text{ kHz}$)	r_O	—	2.0	—	m Ω
Short-Circuit Current Limit ($T_J = +25^\circ\text{C}$)	I_{sc}	—	500	—	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$) 10 Hz $\leq f \leq 100\text{ kHz}$	V_n	—	110	—	μV
Average Temperature Coefficient of Output Voltage $I_O = 5.0\text{ mA}$	TCV_O	—	± 2.3	—	mV/ $^\circ\text{C}$
Peak Output Current ($T_J = +25^\circ\text{C}$)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation ($T_J = +25^\circ\text{C}$) $I_O = 1.0\text{ A}$		21	—	—	Vdc

NOTES:

1. $T_{low} = -55^\circ\text{C}$ for LM140 $T_{high} = +150^\circ\text{C}$ for LM140
 $= 0^\circ\text{C}$ for LM340 $= +125^\circ\text{C}$ for LM340

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

LM140,A, LM340,A

3

LM140/340 — 24

ELECTRICAL CHARACTERISTICS ($V_{in} = 33\text{ V}$, $I_O = 500\text{ mA}$, $T_J = T_{low}$ to T_{high} (Note 1), unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^\circ\text{C}$) $I_O = 5.0\text{ mA}$ to 1.0 A	V_O	23	24	25	Vdc
Line Regulation (Note 2) 28 to 38 Vdc 27 to 38 Vdc ($T_J = +25^\circ\text{C}$) 30 to 36 Vdc, $I_O = 1.0\text{ A}$ 27.1 to 38 Vdc, $I_O = 1.0\text{ A}$ ($T_J = +25^\circ\text{C}$)	Reg _{line}	—	—	240 240 120 240	mV
Load Regulation (Note 2) $5.0\text{ mA} \leq I_O \leq 1.0\text{ A}$ $5.0\text{ mA} \leq I_O \leq 1.5\text{ A}$ ($T_J = +25^\circ\text{C}$) $250\text{ mA} \leq I_O \leq 750\text{ mA}$ ($T_J = +25^\circ\text{C}$)	Reg _{load}	—	—	240 240 120	mV
Output Voltage LM140 28 $\leq V_{in} \leq 38\text{ Vdc}$, $5.0\text{ mA} \leq I_O \leq 1.0\text{ A}$, $P_D \leq 15\text{ W}$ LM340 27 $\leq V_{in} \leq 38\text{ Vdc}$, $5.0\text{ mA} \leq I_O \leq 1.0\text{ A}$, $P_D \leq 15\text{ W}$	V_O	22.8 22.8	—	25.2 25.2	Vdc
Quiescent Current $I_O = 1.0\text{ A}$ LM140 LM340 LM140 ($T_J = +25^\circ\text{C}$) LM340 ($T_J = +25^\circ\text{C}$)	I_B	— — — —	— — 4.0 4.0	7.0 8.5 6.0 8.0	mA
Quiescent Current Change 28 $\leq V_{in} \leq 38\text{ Vdc}$, $I_O = 500\text{ mA}$ LM140 27 $\leq V_{in} \leq 38\text{ Vdc}$, $I_O = 500\text{ mA}$ LM340 5.0 $\text{mA} \leq I_O \leq 1.0\text{ A}$, $V_{in} = 33\text{ V}$ LM140, LM340 28 $\leq V_{in} \leq 38\text{ Vdc}$, $I_O = 1.0\text{ A}$ LM140 27.3 $\leq V_{in} \leq 38\text{ Vdc}$, $I_O = 1.0\text{ A}$ LM340	ΔI_B	— — — — —	— — — — —	0.8 1.0 0.5 0.8 1.0	mA
Ripple Rejection LM140 LM340 $I_O = 1.0\text{ A}$ ($T_J = +25^\circ\text{C}$) LM140 LM340	RR	56 50 56 50	— — 66 66	— — — —	dB
Dropout Voltage	$V_{in} - V_O$	—	1.7	—	Vdc
Output Resistance ($f = 1.0\text{ kHz}$)	r_O	—	2.0	—	m Ω
Short-Circuit Current Limit ($T_J = +25^\circ\text{C}$)	I_{sc}	—	200	—	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$) 10 $\text{Hz} \leq f \leq 100\text{ kHz}$	V_n	—	170	—	μV
Average Temperature Coefficient of Output Voltage $I_O = 5.0\text{ mA}$	TCV_O	—	± 3.0	—	mV/ $^\circ\text{C}$
Peak Output Current ($T_J = +25^\circ\text{C}$)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation ($T_J = +25^\circ\text{C}$) $I_O = 1.0\text{ A}$		27.1	—	—	Vdc

NOTES:

- $T_{low} = -55^\circ\text{C}$ for LM140 $T_{high} = +150^\circ\text{C}$ for LM140
= 0°C for LM340 = $+125^\circ\text{C}$ for LM340
- Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

VOLTAGE REGULATOR PERFORMANCE

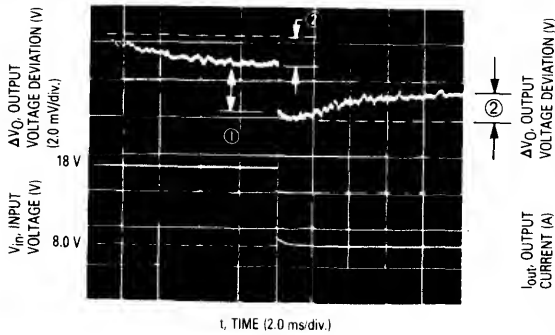
The performance of a voltage regulator is specified by its immunity to changes in load, input voltage, power dissipation, and temperature. Line and load regulation are tested with a pulse of short duration ($< 100 \mu\text{s}$) and are strictly a function of electrical gain. However, pulse widths of longer duration ($> 1.0 \text{ ms}$) are sufficient to affect temperature gradients across the die. These temperature gradients can cause a change in the output voltage, in addition to changes caused by line and load regulation. Longer pulse widths and thermal gradients make it desirable to specify thermal regulation.

Thermal regulation is defined as the change in output voltage caused by a change in dissipated power for a specified time, and is expressed as a percentage output voltage change per watt. The change in dissipated

power can be caused by a change in either the input voltage or the load current. Thermal regulation is a function of IC layout and die attach techniques, and usually occurs within 10 ms of a change in power dissipation. After 10 ms, additional changes in the output voltage are due to the temperature coefficient of the device.

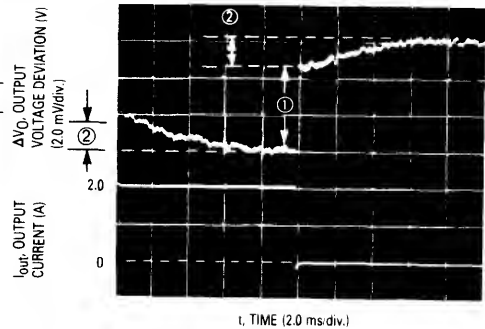
Figure 1 shows the line and thermal regulation response of a typical LM140AK-5.0 to a 10 watt input pulse. The variation of the output voltage due to line regulation is labeled ① and the thermal regulation component is labeled ②. Figure 2 shows the load and thermal regulation response of a typical LM140AK-5.0 to a 15 watt load pulse. The output voltage variation due to load regulation is labeled ① and the thermal regulation component is labeled ②.

FIGURE 1 — LINE AND THERMAL REGULATION



LM140AK-5.0
 $V_O = 5.0 \text{ V}$
 $V_{in} = 8.0 \text{ V} \rightarrow 18 \text{ V} \rightarrow 8.0 \text{ V}$ ① = $\text{Reg}_{line} = 2.4 \text{ mV}$
 $I_{out} = 1.0 \text{ A}$ ② = $\text{Reg}_{therm} = 0.0030\%V_O/\text{W}$

FIGURE 2 — LOAD AND THERMAL REGULATION



LM140AK-5.0
 $V_O = 5.0 \text{ V}$
 $V_{in} = 15$ ① = $\text{Reg}_{load} = 4.4 \text{ mV}$
 $I_{out} = 0 \text{ A} \rightarrow 1.5 \text{ A} \rightarrow 0 \text{ A}$ ② = $\text{Reg}_{therm} = 0.0020\%V_O/\text{W}$

FIGURE 3 — TEMPERATURE STABILITY

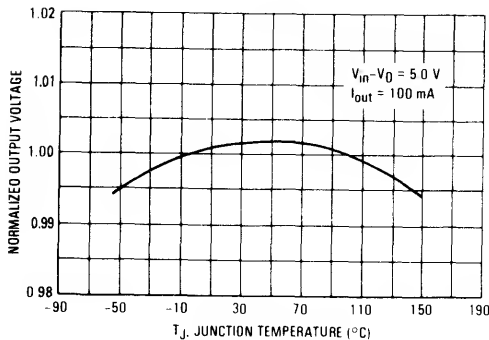
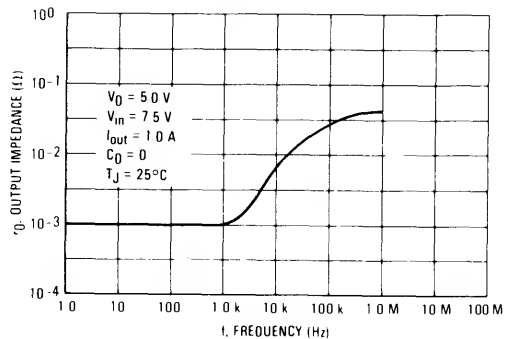


FIGURE 4 — OUTPUT IMPEDANCE



LM140,A, LM340,A

3

FIGURE 5 — RIPPLE REJECTION versus FREQUENCY

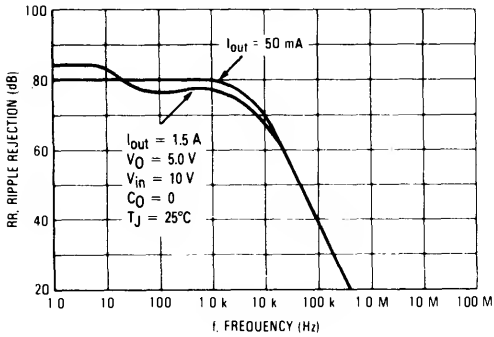


FIGURE 6 — RIPPLE REJECTION versus OUTPUT CURRENT

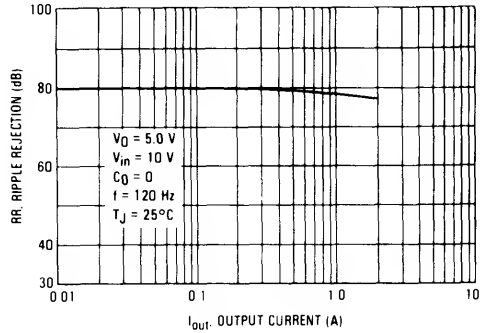


FIGURE 7 — QUIESCENT CURRENT versus INPUT VOLTAGE

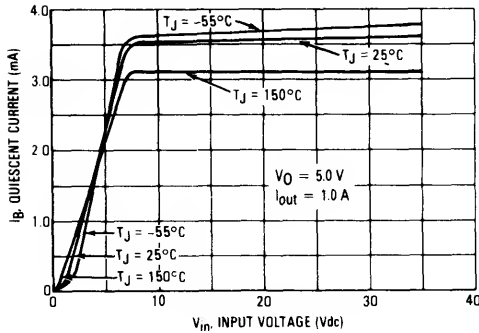


FIGURE 8 — QUIESCENT CURRENT versus OUTPUT CURRENT

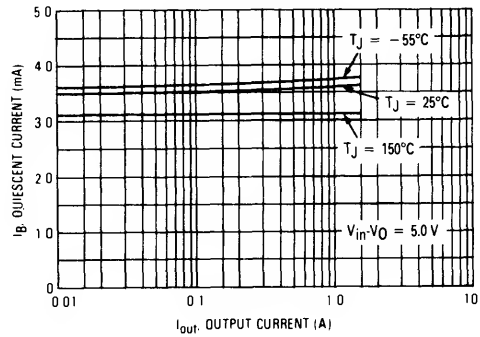


FIGURE 9 — DROPOUT VOLTAGE

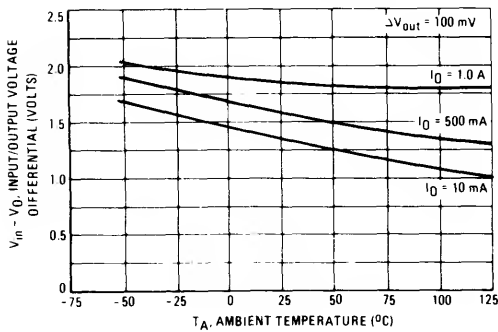


FIGURE 10 — PEAK OUTPUT CURRENT

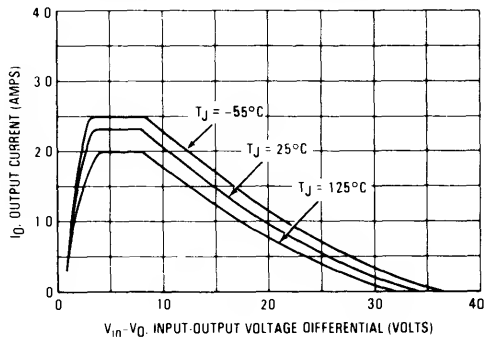


FIGURE 11 — LINE TRANSIENT RESPONSE

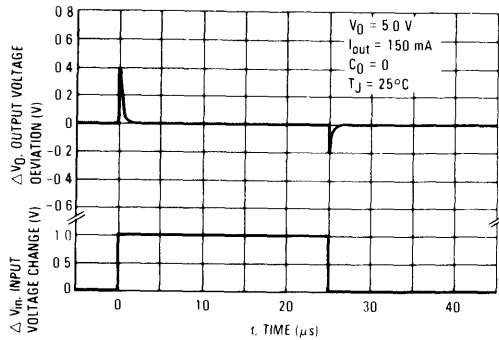


FIGURE 12 — LOAD TRANSIENT RESPONSE

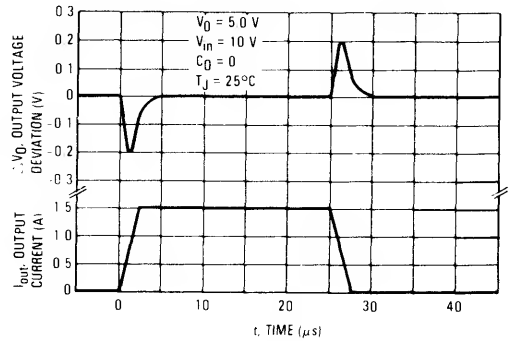


FIGURE 13 — WORST CASE POWER DISSIPATION versus AMBIENT TEMPERATURE (Case 221A)

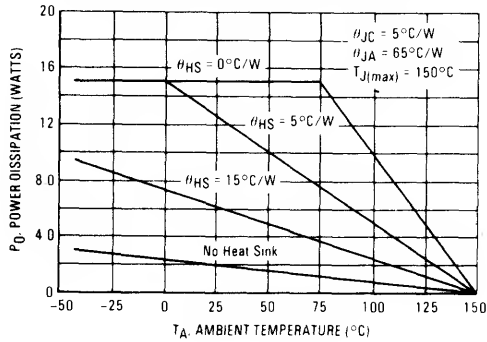
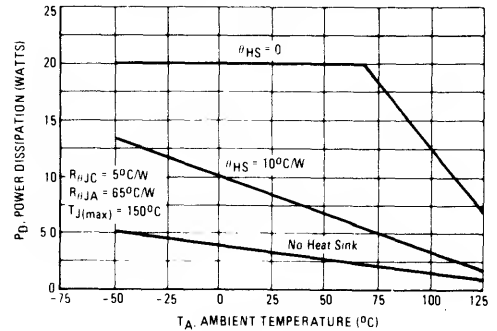


FIGURE 14 — WORST CASE POWER DISSIPATION versus AMBIENT TEMPERATURE (Case 1)



Design Considerations

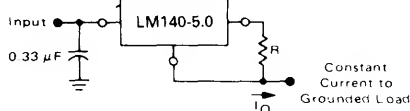
The LM140 Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter

APPLICATIONS INFORMATION

with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

FIGURE 15 — CURRENT REGULATOR



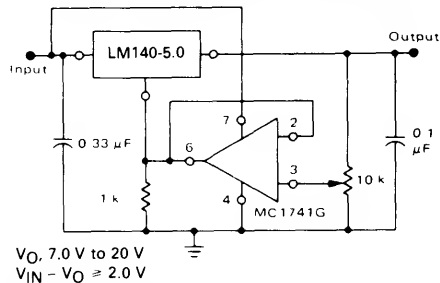
These regulators can also be used as a current source when connected as above. In order to minimize dissipation the LM140-5.0 is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5.0 \text{ V}}{R} + I_Q$$

$I_Q \approx 1.5 \text{ mA}$ over line and load changes

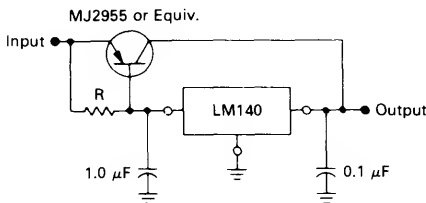
For example, a 1-ampere current source would require R to be a 5-ohm, 10-W resistor and the output voltage compliance would be the input voltage less 7.0 volts.

FIGURE 16 — ADJUSTABLE OUTPUT REGULATOR



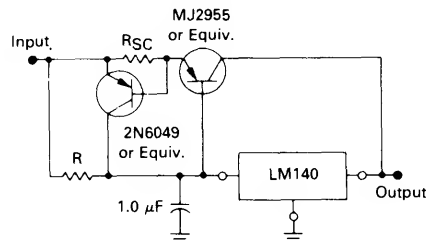
The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 2.0 volts greater than the regulator voltage.

FIGURE 17 — CURRENT BOOST REGULATOR



The LM140 series can be current boosted with a PNP transistor. The MJ2955 provides current to 5.0 amperes. Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short-circuit proof. Input-output differential voltage minimum is increased by V_{BE} of the pass transistor.

FIGURE 18 — SHORT-CIRCUIT PROTECTION



The circuit of Figure 17 can be modified to provide supply protection against short circuits by adding a short-circuit sense resistor, R_{SC} , and an additional PNP transistor. The current sensing PNP must be able to handle the short-circuit current of the three-terminal regulator. Therefore, a four-ampere plastic power transistor is specified.

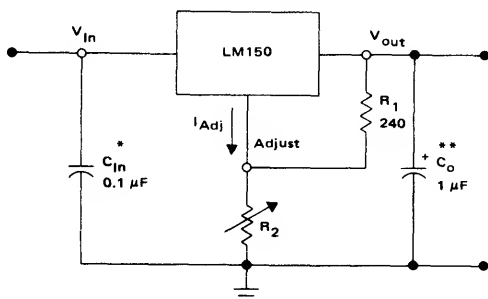
**THREE-TERMINAL ADJUSTABLE
OUTPUT POSITIVE VOLTAGE REGULATORS**

The LM150/250/350 are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 3.0 A over an output voltage range of 1.2 V to 33 V. These voltage regulators are exceptionally easy to use and require only two external resistors to set the output voltage. Further, they employ internal current limiting, thermal shutdown and safe area compensation, making them essentially blow-out proof.

The LM150 series serve a wide variety of applications including local, on card regulation. This device also makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM150 series can be used as a precision current regulator.

- Guaranteed 3.0 Amps Output Current
- Output Adjustable between 1.2 V and 33 V
- Load Regulation Typically 0.1%
- Line Regulation Typically 0.005%/V
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting Constant with Temperature
- Output Transistor Safe-area Compensation
- Floating Operation for High Voltage Applications
- Standard 3-lead Transistor Packages
- Eliminates Stocking Many Fixed Voltages

STANDARD APPLICATION



* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_o is not needed for stability, however it does improve transient response.

$$V_{out} = 1.25 V \left(1 + \frac{R_2}{R_1} \right) + I_{Adj} R_2$$

Since I_{Adj} is controlled to less than 100 μA , the error associated with this term is negligible in most applications

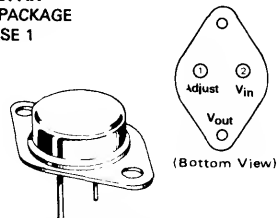
#Automotive temperature range selections are available with special test conditions and additional tests. Contact your local Motorola sales office for information.

LM150
LM250
LM350

**THREE-TERMINAL
ADJUSTABLE POSITIVE
VOLTAGE REGULATORS**

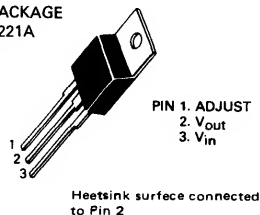
**SILICON MONOLITHIC
INTEGRATED CIRCUIT**

**K SUFFIX
METAL PACKAGE
CASE 1**



Pins 1 and 2 electrically isolated from case.
Case is third electrical connection.

**T SUFFIX
PLASTIC PACKAGE
CASE 221A**



ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
LM150K	$T_J = -55^\circ C$ to $+150^\circ C$	Metal Power
LM250K	$T_J = -25^\circ C$ to $+150^\circ C$	
LM350K	$T_J = 0^\circ C$ to $+125^\circ C$	Plastic Power
LM350T	$T_J = 0^\circ C$ to $+125^\circ C$	
LM350BT#	$T_J = -40^\circ C$ to $+125^\circ C$	

LM150, LM250, LM350

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input-Output Voltage Differential	$V_I - V_O$	35	Vdc
Power Dissipation	P_D	Internally Limited	
Operating Junction Temperature Range	T_J	-55 to +150 -25 to +150 0 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Soldering Lead Temperature (10 seconds)		300	°C

3

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, $V_I - V_O = 5.0$ V; $I_L = 1.5$ A; $T_J = T_{low}$ to T_{high} ; P_{max} [see Note 1].)

Characteristic	Figure	Symbol	LM150/250			LM350			Unit
			Min	Typ	Max	Min	Typ	Max	
Line Regulation (Note 2) $T_A = 25^\circ\text{C}$, $3.0 \text{ V} \leq V_I - V_O \leq 35 \text{ V}$	1	Regline	—	0.005	0.01	—	0.005	0.03	%/V
Load Regulation (Note 2) $T_A = 25^\circ\text{C}$, $10 \text{ mA} \leq I_L \leq 3.0 \text{ A}$ $V_O \leq 5.0 \text{ V}$ $V_O \geq 5.0 \text{ V}$	2	Regload	— —	5.0 0.1	15 0.3	— —	5.0 0.1	25 0.5	mV % V_O
Thermal Regulation, Pulse = 20 ms, $T_A = 25^\circ\text{C}$	—	Regtherm	—	0.002	—	—	0.002	—	% V_O/W
Adjustment Pin Current	3	I_{Adj}	—	50	100	—	50	100	μA
Adjustment Pin Current Change $3.0 \text{ V} \leq V_I - V_O \leq 35 \text{ V}$ $10 \text{ mA} \leq I_L \leq 3.0 \text{ A}$, $P_D \leq P_{max}$	1,2	ΔI_{Adj}	—	0.2	5.0	—	0.2	5.0	μA
Reference Voltage (Note 3) $3.0 \text{ V} \leq V_I - V_O \leq 35 \text{ V}$ $10 \text{ mA} \leq I_L \leq 3.0 \text{ A}$, $P_D \leq P_{max}$	3	V_{ref}	1.20	1.25	1.30	1.20	1.25	1.30	V
Line Regulation (Note 2) $3.0 \text{ V} \leq V_I - V_O \leq 35 \text{ V}$	1	Regline	—	0.02	0.05	—	0.02	0.07	%/V
Load Regulation (Note 2) $10 \text{ mA} \leq I_L \leq 3.0 \text{ A}$ $V_O \leq 5.0 \text{ V}$ $V_O \geq 5.0 \text{ V}$	2	Regload	— —	20 0.3	50 1.0	— —	20 0.3	70 1.5	mV % V_O
Temperature Stability ($T_{low} \leq T_J \leq T_{high}$)	3	T_S	—	1.0	—	—	1.0	—	% V_O
Minimum Load Current to Maintain Regulation ($V_I - V_O = 35 \text{ V}$)	3	I_{Lmin}	—	3.5	5.0	—	3.5	10	mA
Maximum Output Current $V_I - V_O \leq 10 \text{ V}$, $P_D \leq P_{max}$ $V_I - V_O = 30 \text{ V}$, $P_D \leq P_{max}$, $T_A = 25^\circ\text{C}$	3	I_{max}	3.0 0.3	4.5 1.0	— —	3.0 0.25	4.5 1.0	— —	A
RMS Noise, % of V_O $T_A = 25^\circ\text{C}$, $10 \text{ Hz} \leq f \leq 10 \text{ kHz}$	—	N	—	0.003	—	—	0.003	—	% V_O
Ripple Rejection, $V_O = 10 \text{ V}$, $f = 120 \text{ Hz}$ (Note 4) Without C_{Adj} $C_{Adj} = 10 \mu\text{F}$	4	RR	— 66	65 80	— —	— 66	65 80	— —	dB
Long-Term Stability, $T_J = T_{high}$ (Note 5) $T_A = 25^\circ\text{C}$ for Endpoint Measurements	3	S	—	0.3	1.0	—	0.3	1.0	%/1.0 k Hrs.
Thermal Resistance Junction to Case Peak (Note 6) K Package T Package Average (Note 7) K Package T Package	—	$R_{\theta JC}$	— — — —	2.3 — — —	— — 1.5 —	— — — —	2.3 2.3 — —	— — 1.5 1.5	°C/W

NOTES:

- (1) $T_{low} = -55^\circ\text{C}$ for LM150
-25°C for LM250
0°C for LM350
 $P_{max} = 30 \text{ W}$ for K suffix
 $P_{max} = 25 \text{ W}$ for T suffix
- (2) Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.
- (3) Selected devices with tightened tolerance reference voltage available.
- (4) C_{Adj} , when used, is connected between the adjustment pin and ground.

- (5) Since Long-Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.
- (6) Thermal Resistance evaluated measuring the hottest temperature on the die using an infrared scanner. This method of evaluation yields very accurate thermal resistance values which are conservative when compared to other measurement techniques.
- (7) The average die temperature is used to derive the value of thermal resistance junction to case (average).

LM150, LM250, LM350

SCHEMATIC DIAGRAM

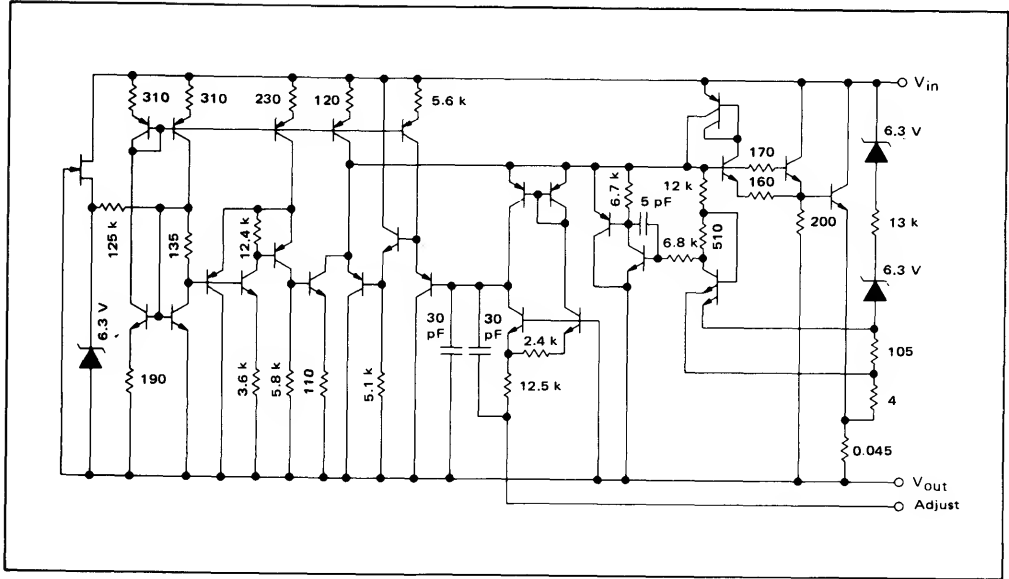
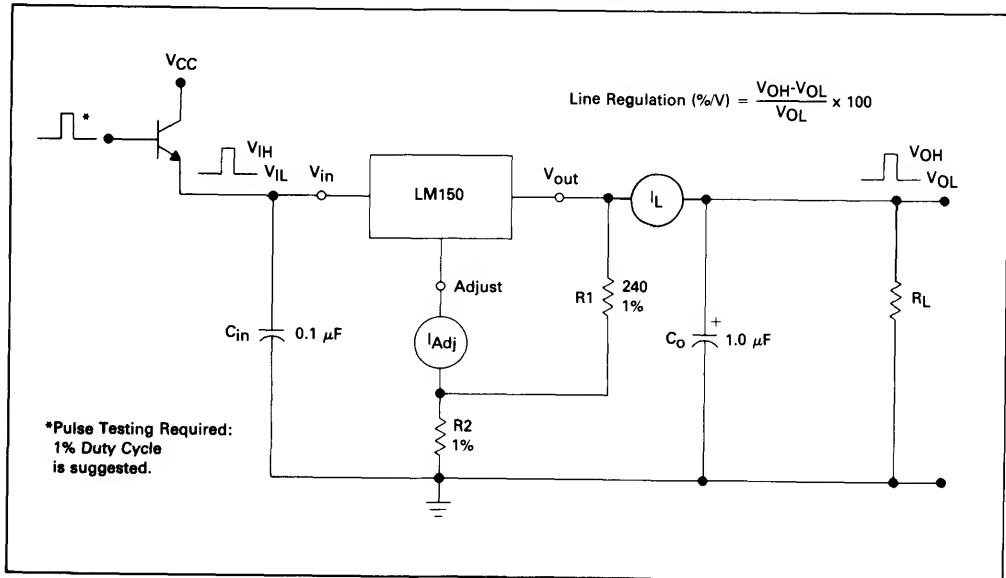


FIGURE 1 — LINE REGULATION AND $\Delta I_{Adj}/LINE$ TEST CIRCUIT



LM150, LM250, LM350

FIGURE 2 — LOAD REGULATION AND ΔI_{Adj} /LOAD TEST CIRCUIT

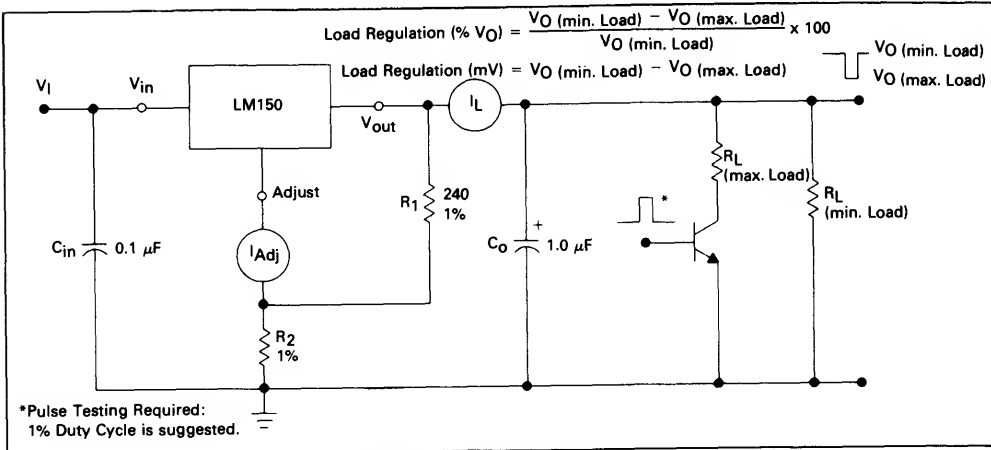


FIGURE 3 — STANDARD TEST CIRCUIT

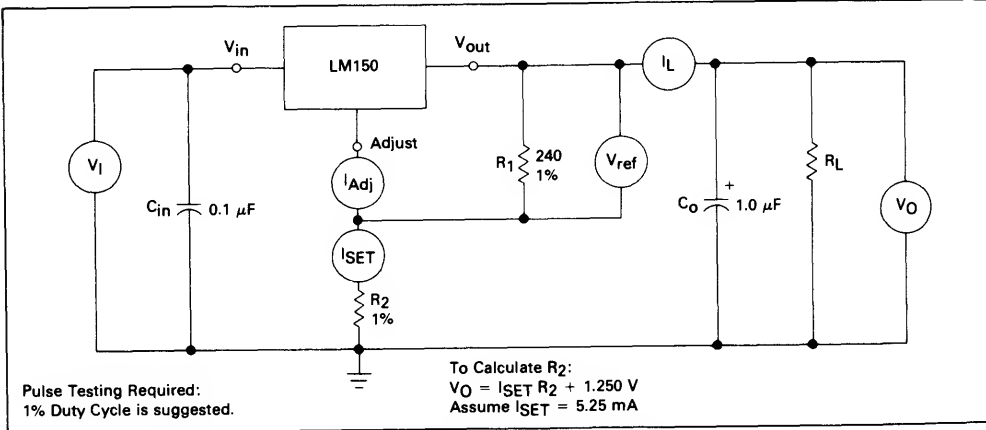
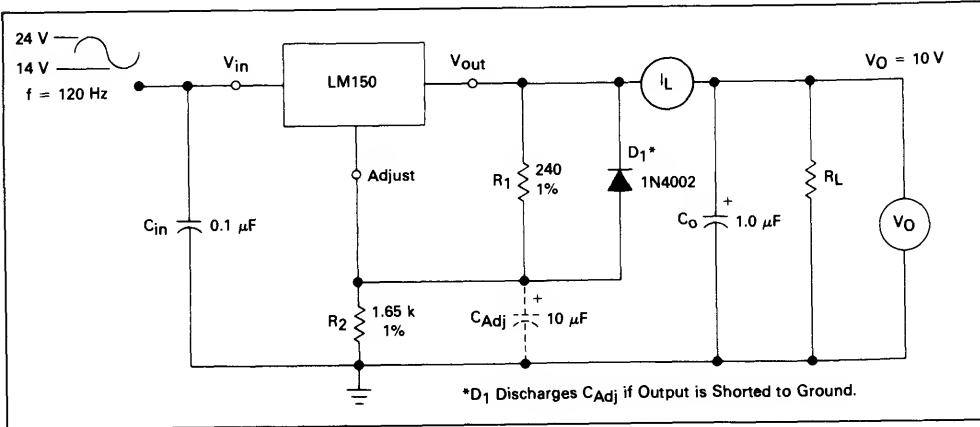


FIGURE 4 — RIPPLE REJECTION TEST CIRCUIT



LM150, LM250, LM350

3

FIGURE 5 – LOAD REGULATION

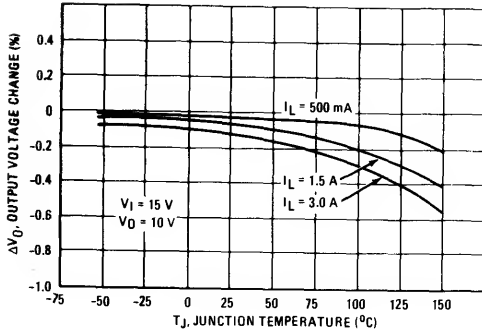


FIGURE 6 – CURRENT LIMIT

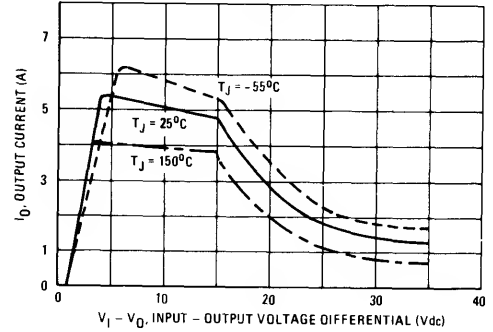


FIGURE 7 – ADJUSTMENT PIN CURRENT

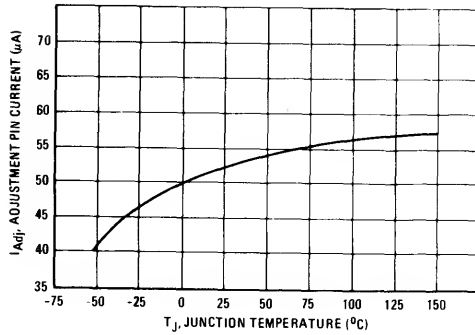


FIGURE 8 – DROPOUT VOLTAGE

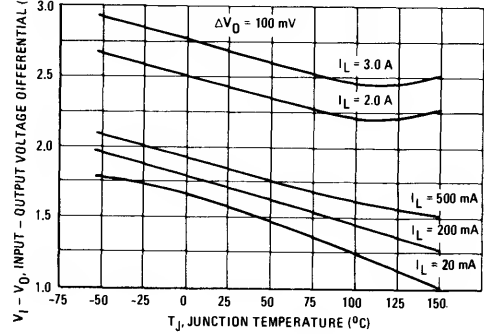


FIGURE 9 – TEMPERATURE STABILITY

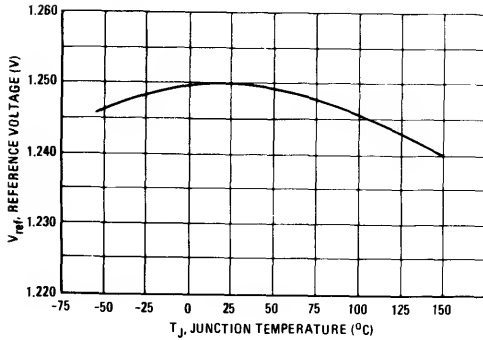
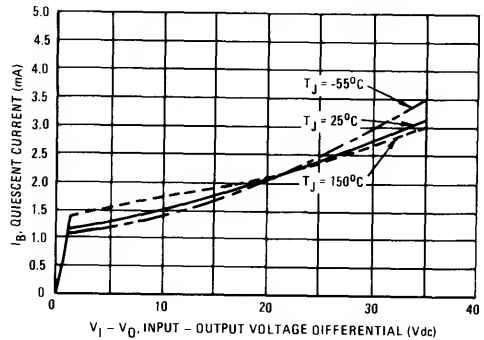


FIGURE 10 – MINIMUM OPERATING CURRENT



LM150, LM250, LM350

FIGURE 11 — RIPPLE REJECTION versus OUTPUT VOLTAGE

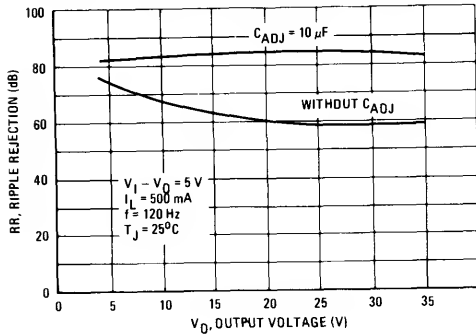


FIGURE 12 — RIPPLE REJECTION versus OUTPUT CURRENT

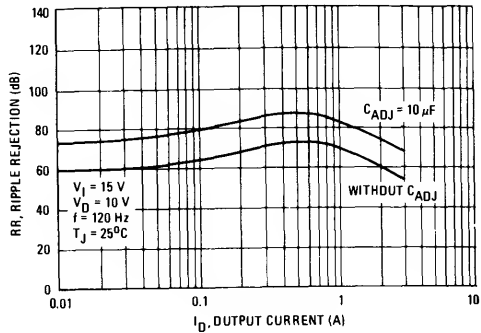


FIGURE 13 — RIPPLE REJECTION versus FREQUENCY

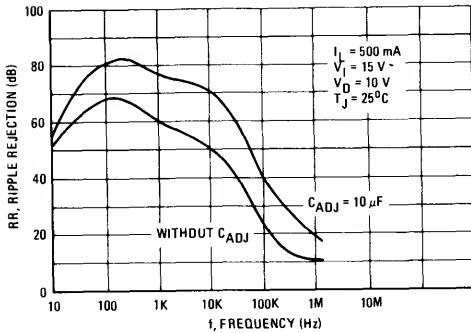


FIGURE 14 — OUTPUT IMPEDANCE

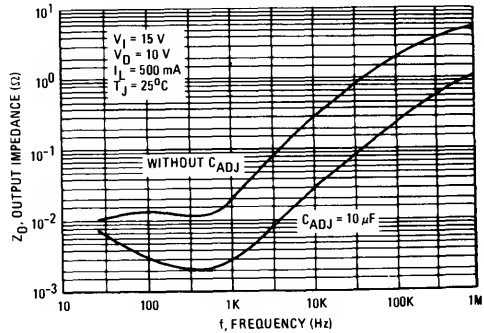


FIGURE 15 — LINE TRANSIENT RESPONSE

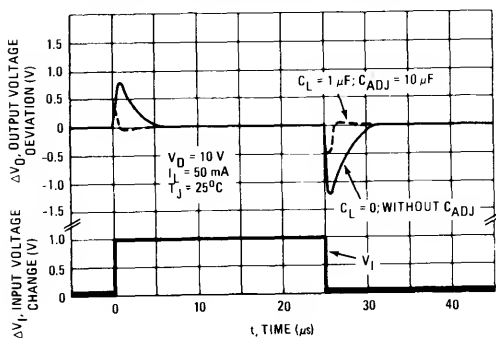
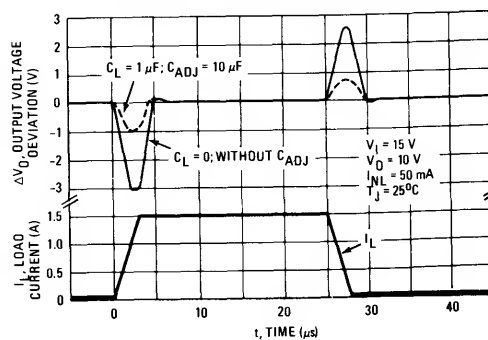


FIGURE 16 — LOAD TRANSIENT RESPONSE



APPLICATIONS INFORMATION

BASIC CIRCUIT OPERATION

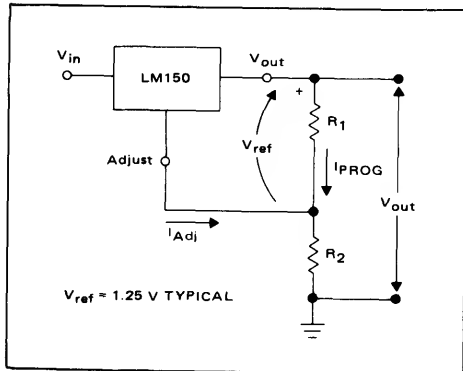
The LM150 is a 3-terminal floating regulator. In operation, the LM150 develops and maintains a nominal 1.25 volt reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by R_1 (see Figure 17), and this constant current flows through R_2 to ground. The regulated output voltage is given by:

$$V_{out} = V_{ref} \left(1 + \frac{R_2}{R_1}\right) + I_{Adj} R_2$$

Since the current from the adjustment terminal (I_{Adj}) represents an error term in the equation, the LM150 was designed to control I_{Adj} to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM150 is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

FIGURE 17 - BASIC CIRCUIT CONFIGURATION



LOAD REGULATION

The LM150 is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R_1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R_2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

EXTERNAL CAPACITORS

A 0.1 μF disc or 1 μF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{ADJ}) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 volt application.

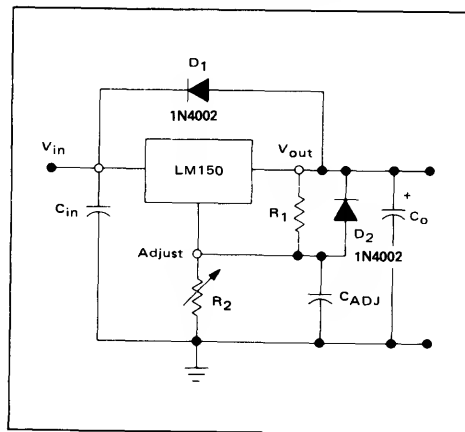
Although the LM150 is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance (C_o) in the form of a 1 μF tantalum or 25 μF aluminum electrolytic capacitor on the output swamps this effect and insures stability.

PROTECTION DIODES

When external capacitors are used with any I.C. regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 18 shows the LM150 with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values ($C_o > 25 \mu F$, $C_{ADJ} > 10 \mu F$). Diode D_1 prevents C_o from discharging thru the I.C. during an input short circuit. Diode D_2 protects against capacitor C_{ADJ} discharging through the I.C. during an output short circuit. The combination of diodes D_1 and D_2 prevents C_{ADJ} from discharging through the I.C. during an input short circuit.

FIGURE 18 - VOLTAGE REGULATOR WITH PROTECTION DIODES



LM150, LM250, LM350

FIGURE 19 – "LABORATORY" POWER SUPPLY WITH ADJUSTABLE CURRENT LIMIT AND OUTPUT VOLTAGE

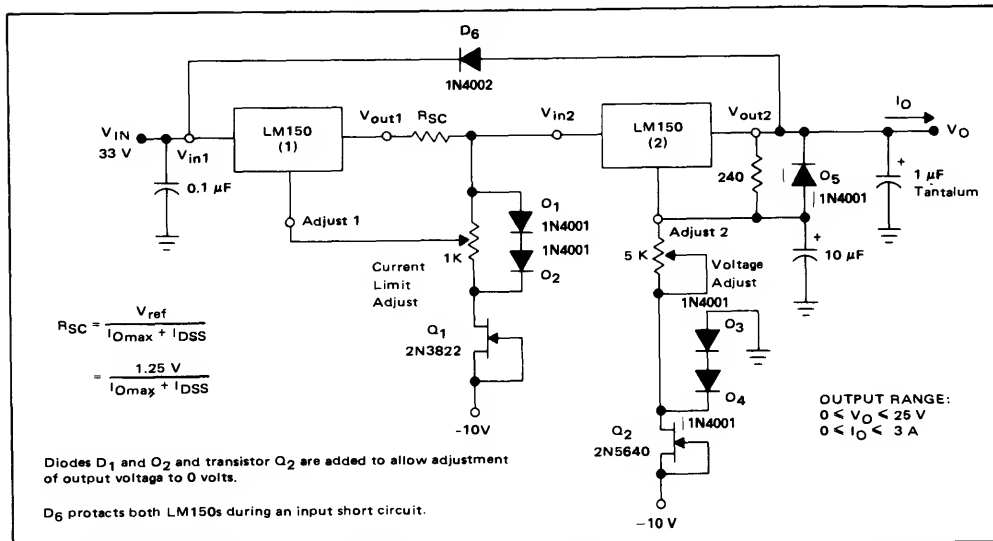


FIGURE 20 – ADJUSTABLE CURRENT LIMITER

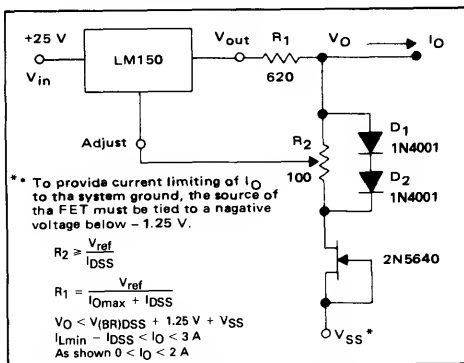


FIGURE 22 – SLOW TURN-ON REGULATOR

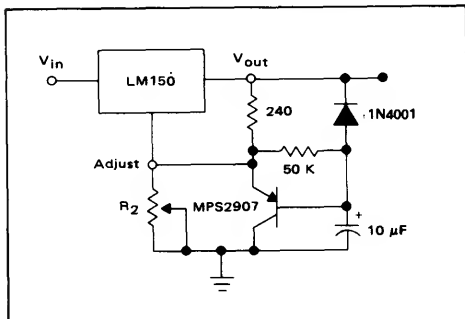


FIGURE 21 – 5 V ELECTRONIC SHUT DOWN REGULATOR

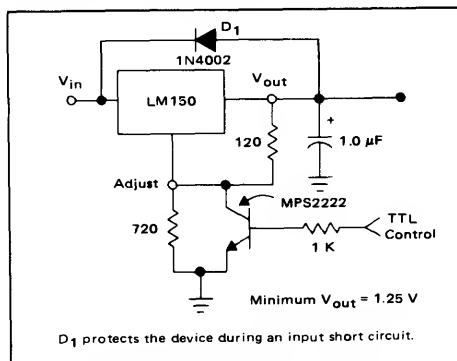
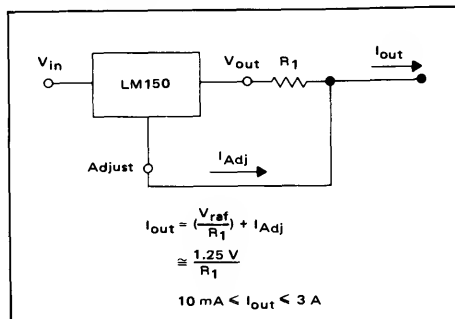


FIGURE 23 – CURRENT REGULATOR



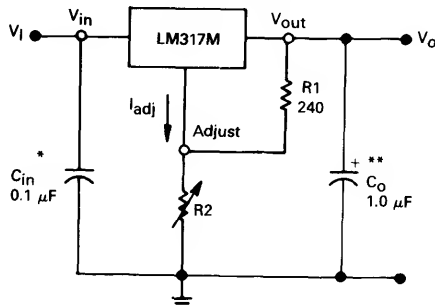
**THREE-TERMINAL ADJUSTABLE
OUTPUT POSITIVE VOLTAGE REGULATOR**

The LM317M is an adjustable 3-terminal positive voltage regulator capable of supplying in excess of 500 mA over an output voltage range of 1.2 V to 37 V. This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, it employs internal current limiting, thermal shutdown and safe area compensation, making it essentially blow-out proof.

The LM317M serves a wide variety of applications including local, on-card regulation. This device also makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjust and output, the LM317M can be used as a precision current regulator.

- Output Current in Excess of 500 mA
- Output Adjustable Between 1.2 V and 37 V
- Internal Thermal Overload Protection
- Internal Short-Circuit-Current Limiting
- Output Transistor Safe-Area Compensation
- Floating Operation for High Voltage Applications
- Standard 3-Lead Transistor Packages
- Eliminates Stocking Many Fixed Voltages

STANDARD APPLICATION



*C_{in} is required if regulator is located in appreciable distance from power supply filter.

**C_O is not needed for stability, however it does improve transient response.

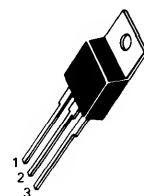
$$V_O = 1.25 \text{ V} \left(1 + \frac{R_2}{R_1} \right) + I_{adj} R_2$$

Since I_{adj} is controlled to less than 100 μA, the error associated with this term is negligible in most applications.

LM317M

**MEDIUM-CURRENT
THREE-TERMINAL
ADJUSTABLE POSITIVE
VOLTAGE REGULATOR**

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**

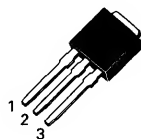


(Heatsink surface
connected to Pin 2)

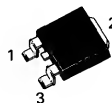
(All 3 Packages)

PIN 1. ADJUST
2. V_{out}
3. V_{in}

**T SUFFIX
PLASTIC PACKAGE
CASE 221A**



**DT-1 SUFFIX
PLASTIC PACKAGE
CASE 369
DPAK**



**DT SUFFIX
PLASTIC PACKAGE
CASE 369A
DPAK**

ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
LM317MT	0°C to +125°C	Plastic Power
LM317MBT#	-40°C to +125°C	Plastic Power
LM317MDT	0 to 125°C	DPAK
LM317MDT-1	0 to 125°C	DPAK

#Automotive temperature range selections are available with special test conditions and additional tests. Contact your local Motorola sales office for information.

LM317M

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input-Output Voltage Differential	$V_I - V_O$	40	Vdc
Power Dissipation	P_D	Internally Limited	
Operating Junction Temperature Range	T_J	0 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

($V_I - V_O = 5.0$ V, $I_O = 0.1$ A, $T_J = T_{low}$ to T_{high} [see Note 1], P_{max} per Note 2, unless otherwise specified.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Line Regulation (Note 3) $T_A = 25^\circ\text{C}$, 3.0 V $\leq V_I - V_O \leq 40$ V	1	Regline	—	0.01	0.04	%/V
Load Regulation (Note 3) $T_A = 25^\circ\text{C}$, 10 mA $\leq I_O \leq 0.5$ A $V_O \leq 5.0$ V $V_O \geq 5.0$ V	2	Regload	— —	5.0 0.1	25 0.5	mV % V_O
Adjustment Pin Current	3	I_{adj}	—	50	100	μA
Adjustment Pin Current Change 2.5 V $\leq V_I - V_O \leq 40$ V, 10 mA $\leq I_L \leq 0.5$ A, $P_D \leq P_{max}$	1,2	ΔI_{adj}	—	0.2	5.0	μA
Reference Voltage (Note 4) 3.0 V $\leq V_I - V_O \leq 40$ V, 10 mA $\leq I_O \leq 0.5$ A, $P_D \leq P_{max}$	3	V_{ref}	1.20	1.25	1.30	V
Line Regulation (Note 3) 3.0 V $\leq V_I - V_O \leq 40$ V	1	Regline	—	0.02	0.07	%/V
Load Regulation (Note 3) 10 mA $\leq I_O \leq 0.5$ A $V_O \leq 5.0$ V $V_O \geq 5.0$ V	2	Regload	— —	20 0.3	70 1.5	mV % V_O
Temperature Stability ($T_{low} \leq T_J \leq T_{high}$)	3	T_S	—	0.7	—	% V_O
Minimum Load Current to Maintain Regulation ($V_I - V_O = 40$ V)	3	I_{Lmin}	—	3.5	10	mA
Maximum Output Current $V_I - V_O \leq 15$ V, $P_D \leq P_{max}$ $V_I - V_O = 40$ V, $P_D \leq P_{max}$, $T_A = 25^\circ\text{C}$	3	I_{max}	0.5 0.15	0.9 0.25	— —	A
RMS Noise, % of V_O $T_A = 25^\circ\text{C}$, 10 Hz $\leq f \leq 10$ kHz	—	N	—	0.003	—	% V_O
Ripple Rejection, $V_O = 10$ V, $f = 120$ Hz (Note 5) Without C_{adj} $C_{adj} = 10$ μF	4	RR	— 66	65 80	— —	dB
Long Term Stability, $T_J = T_{high}$ (Note 6) $T_A = 25^\circ\text{C}$ for Endpoint Measurements	3	S	—	0.3	1.0	%/1.0 k Hrs.
Thermal Resistance Junction to Case, T Suffix Package	—	$R_{\theta JC}$	—	7.0	—	°C/W

NOTES:

(1) T_{low} to $T_{high} = 0^\circ\text{C}$ to $+125^\circ\text{C}$

(2) $P_{max} = 7.5$ W

(3) Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating affects must be taken into account separately. Pulse testing with low duty cycle is used.

(4) Selected devices with tightened tolerance reference voltage available.

(5) C_{adj} , when used, is connected between the adjustment pin and ground.

(6) Since Long Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

LM317M

SCHEMATIC DIAGRAM

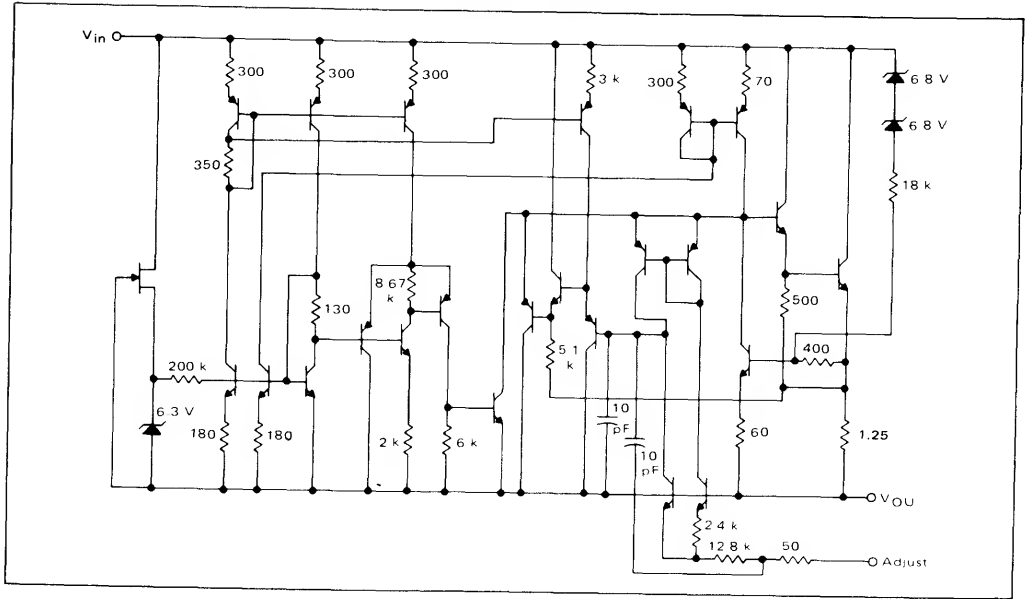
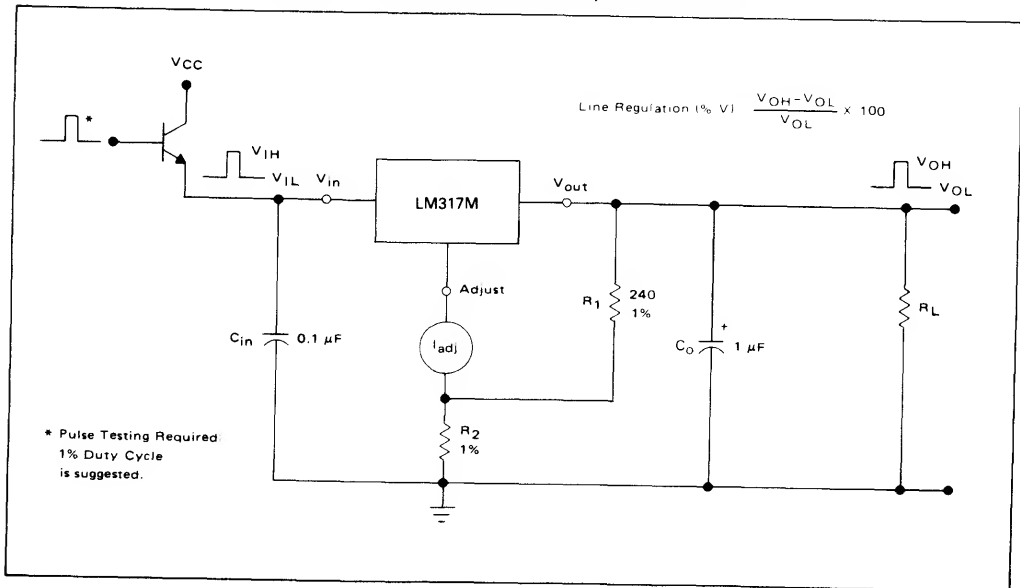


FIGURE 1 – LINE REGULATION AND $\Delta I_{adj}/LINE$ TEST CIRCUIT



LM317M

FIGURE 2 – LOAD REGULATION AND $\Delta I_{Adj}/LOAD$ TEST CIRCUIT

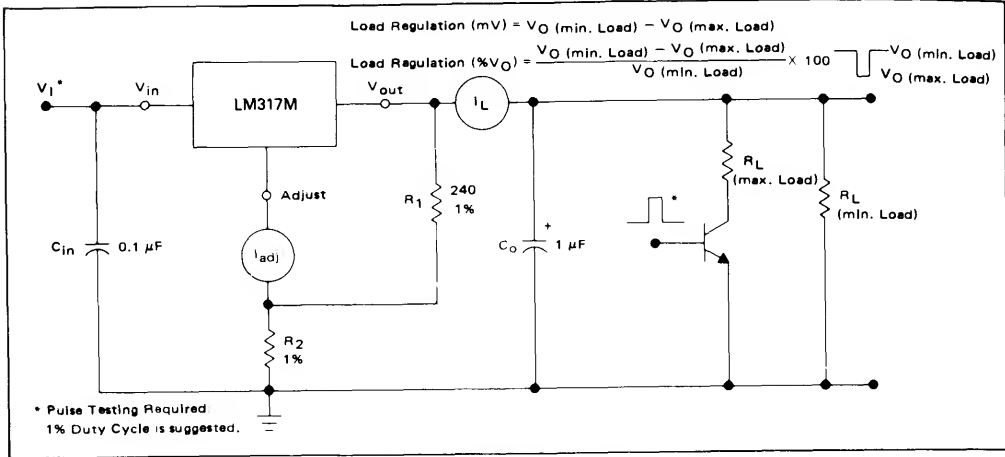


FIGURE 3 – STANDARD TEST CIRCUIT

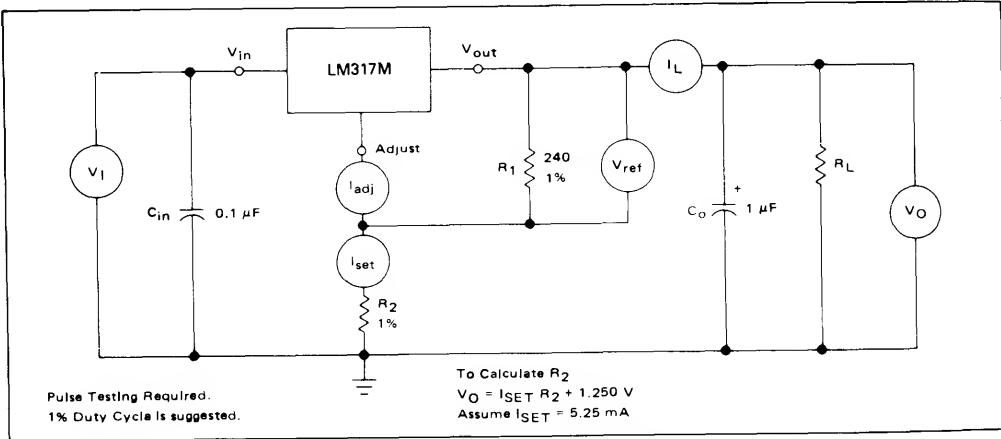


FIGURE 4 – RIPPLE REJECTION TEST CIRCUIT

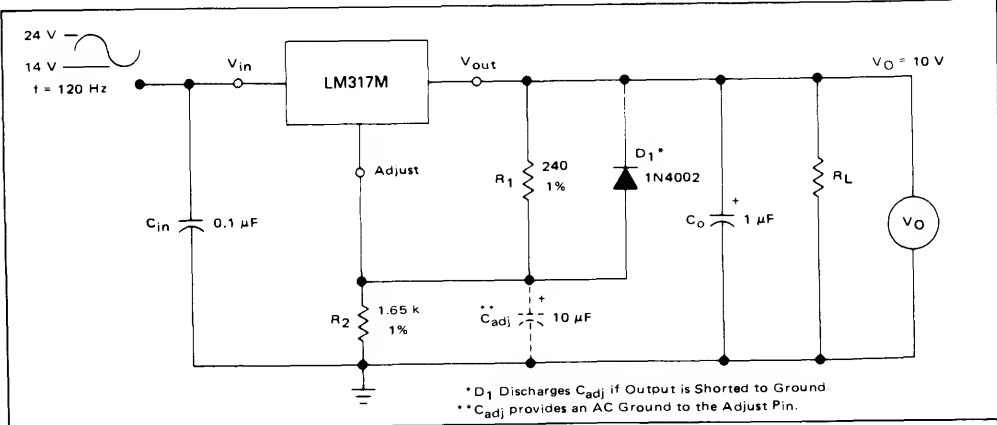


FIGURE 5 – LOAD REGULATION

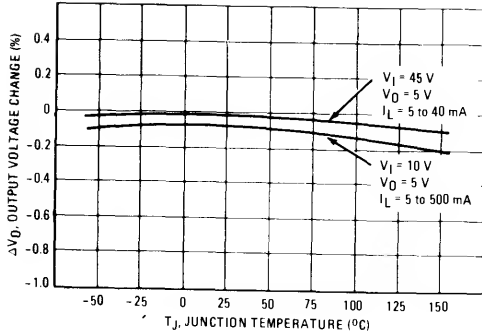


FIGURE 6 – RIPPLE REJECTION

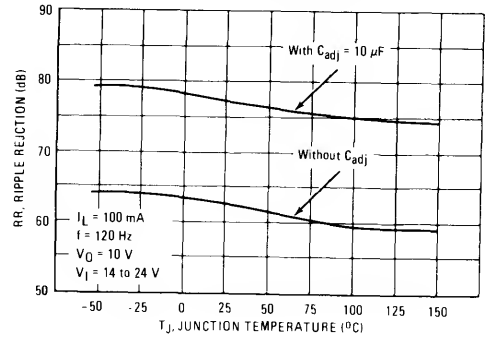


FIGURE 7 – CURRENT LIMIT

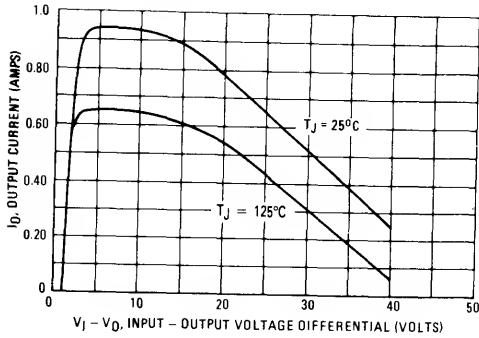


FIGURE 8 – DROPOUT VOLTAGE

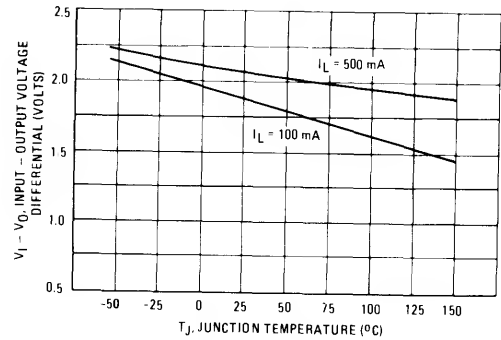


FIGURE 9 – MINIMUM OPERATING CURRENT

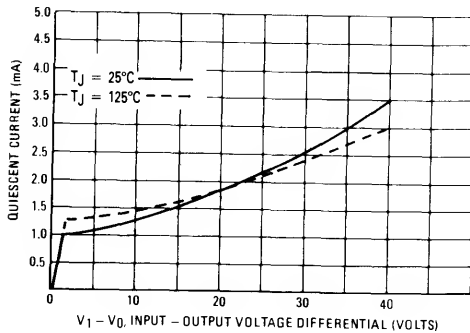


FIGURE 10 – RIPPLE REJECTION versus FREQUENCY

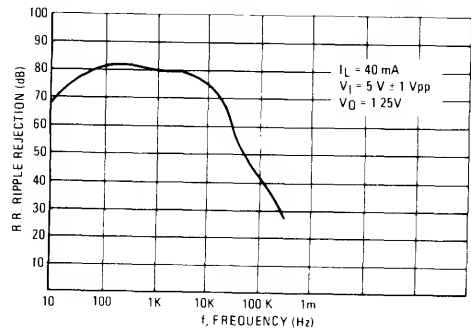


FIGURE 11 – TEMPERATURE STABILITY

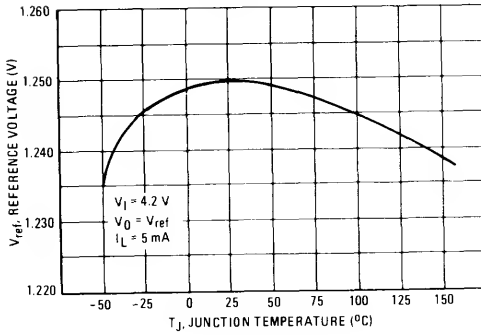


FIGURE 12 – ADJUSTMENT PIN CURRENT

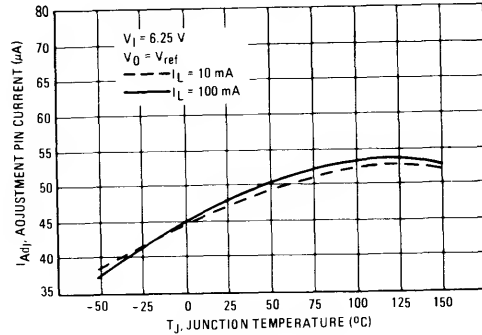


FIGURE 13 – LINE REGULATION

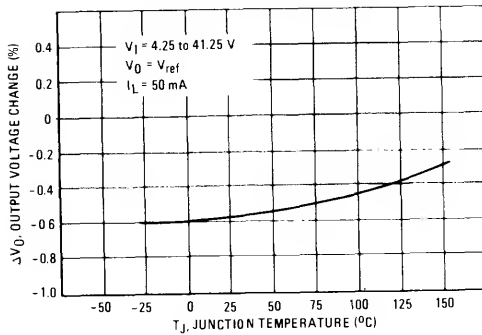


FIGURE 14 – OUTPUT NOISE

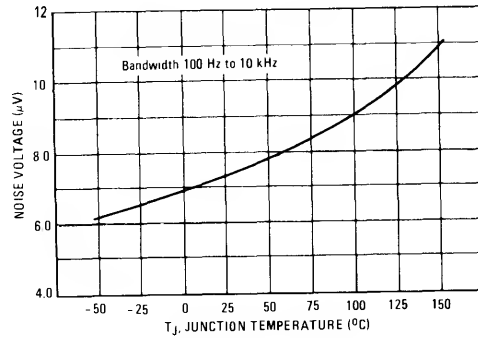


FIGURE 15 – LINE TRANSIENT RESPONSE

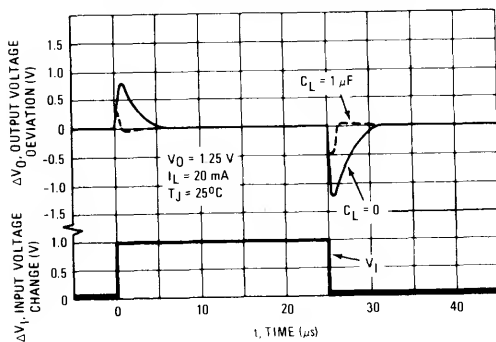
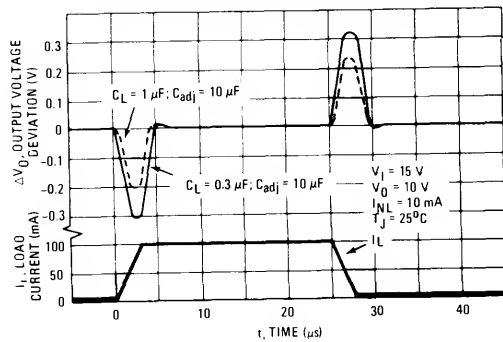


FIGURE 16 – LOAD TRANSIENT RESPONSE



APPLICATIONS INFORMATION

BASIC CIRCUIT OPERATION

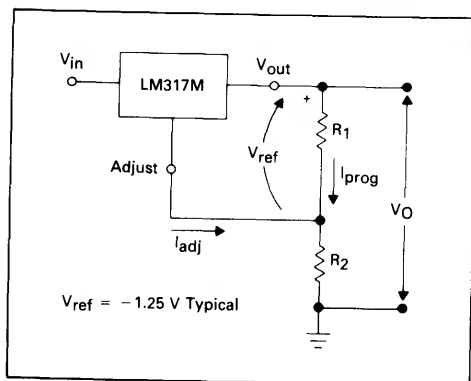
The LM317M is a 3-terminal floating regulator. In operation, the LM317M develops and maintains a nominal 1.25 volt reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{prog}) by R_1 (see Figure 17), and this constant current flows through R_2 to ground. The regulated output voltage is given by:

$$V_O = V_{ref} \left(1 + \frac{R_2}{R_1} \right) + I_{adj} R_2$$

Since the current from the adjustment terminal (I_{adj}) represents an error term in the equation, the LM317M was designed to control I_{adj} to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM317M is a floating regulator, it is only the voltage differential across the circuit that is important to performance, and operation at high voltages with respect to ground is possible.

FIGURE 17 — BASIC CIRCUIT CONFIGURATION



LOAD REGULATION

The LM317M is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R_1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R_2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

EXTERNAL CAPACITORS

A 0.1 μF disc or 1 μF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{adj}) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 volt application.

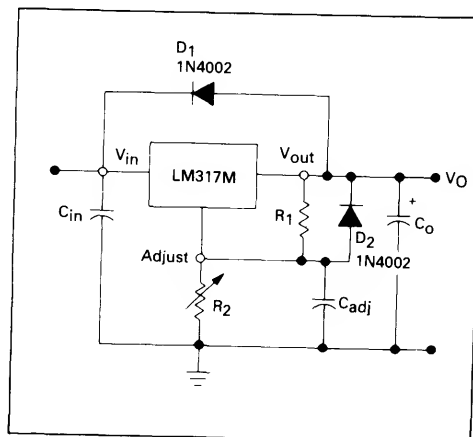
Although the LM317M is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance (C_O) in the form of a 1 μF tantalum or 25 μF aluminum electrolytic capacitor on the output swamps this effect and insures stability.

PROTECTION DIODES

When external capacitors are used with any I.C. regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 18 shows the LM317M with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values ($C_O > 25 \mu F$, $C_{adj} > 5.0 \mu F$). Diode D_1 prevents C_O from discharging thru the I.C. during an input short circuit. Diode D_2 protects against capacitor C_{adj} discharging through the I.C. during an output short circuit. The combination of diodes D_1 and D_2 prevents C_{adj} from discharging through the I.C. during an input short circuit.

FIGURE 18 — VOLTAGE REGULATOR WITH PROTECTION DIODES



LM317M

FIGURE 19 – ADJUSTABLE CURRENT LIMITER

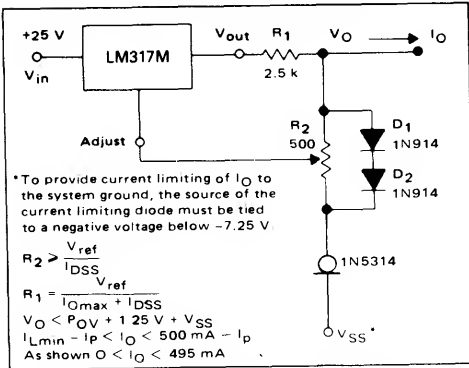


FIGURE 21 – SLOW TURN-ON REGULATOR

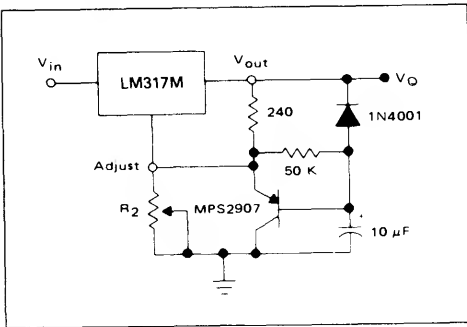


FIGURE 20 – 5 V ELECTRONIC SHUTDOWN REGULATOR

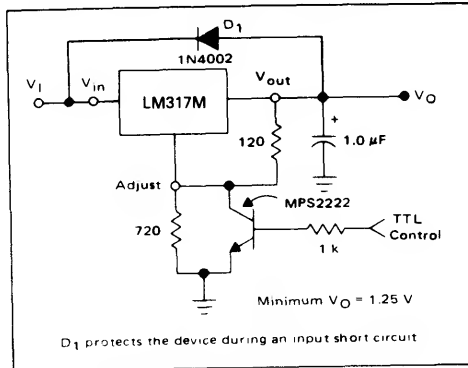
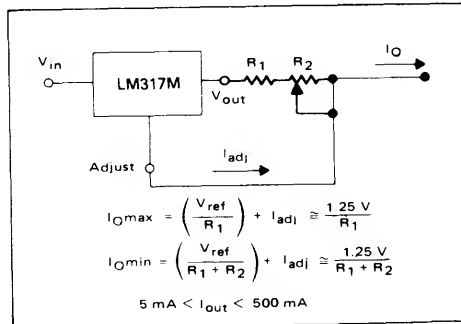


FIGURE 22 – CURRENT REGULATOR



**THREE-TERMINAL ADJUSTABLE
 OUTPUT NEGATIVE VOLTAGE REGULATOR**

The LM337M is an adjustable 3-terminal negative voltage regulator capable of supplying in excess of 500 mA over an output voltage range of -1.2 V to -37 V . This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, it employs internal current limiting, thermal shutdown and safe area compensation, making it essentially blow-out proof.

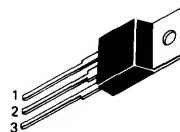
The LM337M serves a wide variety of applications including local, on-card regulation. This device can also be used to make a programmable output regulator; or, by connecting a fixed resistor between the adjustment and output, the LM337M can be used as a precision current regulator.

- Output Current in Excess of 500 mA
- Output Adjustable Between -1.2 V and -37 V
- Internal Thermal Overload Protection
- Internal Short-Circuit-Current Limiting
- Output Transistor Safe-Area Compensation
- Floating Operation for High Voltage Applications
- Standard 3-Lead Transistor Packages
- Eliminates Stocking Many Fixed Voltages

LM337M

**MEDIUM-CURRENT
 THREE-TERMINAL
 ADJUSTABLE NEGATIVE
 VOLTAGE REGULATOR**

**SILICON MONOLITHIC
 INTEGRATED CIRCUIT**



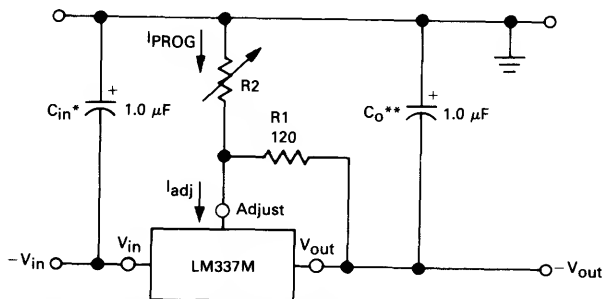
PIN 1. ADJUST
 2. V_{in}
 3. V_{out}

T SUFFIX
PLASTIC PACKAGE
CASE 221A

ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
LM337MT	$T_J = 0^\circ\text{C to } +125^\circ\text{C}$	Plastic Power
LM337MBT	$T_J = -40^\circ\text{C to } +125^\circ\text{C}$	Plastic Power

STANDARD APPLICATION



* C_{in} is required if regulator is located more than 4 inches from power supply filter. A $1.0\text{ }\mu\text{F}$ solid tantalum or $10\text{ }\mu\text{F}$ aluminum electrolytic is recommended.

** C_O is necessary for stability. A $1.0\text{ }\mu\text{F}$ solid tantalum or $10\text{ }\mu\text{F}$ aluminum electrolytic is recommended.

$$V_{out} = -1.25\text{ V} \left(1 + \frac{R_2}{R_1} \right)$$

#Automotive temperature range selections are available with special test conditions and additional tests. Contact your local Motorola sales office for information.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input-Output Voltage Differential	$V_I - V_O$	40	Vdc
Power Dissipation	P_D	Internally Limited	
Operating Junction Temperature Range	T_J	0 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS ($|V_I - V_O| = 5.0$ V, $I_O = 0.1$; $T_J = T_{low}$ to T_{high} [see Note 1], P_{max} per Note 2, unless otherwise specified.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Line Regulation (Note 3) $T_A = 25^\circ\text{C}$, $3.0\text{ V} \leq V_I - V_O \leq 40\text{ V}$	1	Regline	—	0.01	0.04	%/V
Load Regulation (Note 3) $T_A = 25^\circ\text{C}$, $10\text{ mA} \leq I_O \leq 0.5\text{ A}$ $ V_O \leq 5.0\text{ V}$ $ V_O \geq 5.0\text{ V}$	2	Regload	— —	15 0.3	50 1.0	mV % V_O
Thermal Regulation 10 ms Pulse, $T_A = 25^\circ\text{C}$	—	Regtherm	—	0.03	0.04	% V_O /W
Adjustment Pin Current	3	I_{adj}	—	65	100	μA
Adjustment Pin Current Change $2.5\text{ V} \leq V_I - V_O \leq 40\text{ V}$, $10\text{ mA} \leq I_L \leq 0.5\text{ A}$, $P_D \leq P_{max}$, $T_A = 25^\circ\text{C}$	1,2	ΔI_{adj}	—	2.0	5.0	μA
Reference Voltage (Note 4) $3.0\text{ V} \leq V_I - V_O \leq 40\text{ V}$, $10\text{ mA} \leq I_O \leq 0.5\text{ A}$, $P_D \leq P_{max}$, $T_A = 25^\circ\text{C}$ T_{low} to T_{high}	3	V_{ref}	-1.213 -1.20	-1.250 -1.25	-1.287 -1.30	V
Line Regulation (Note 3) $3.0\text{ V} \leq V_I - V_O \leq 40\text{ V}$	1	Regline	—	0.02	0.07	%/V
Load Regulation (Note 3) $10\text{ mA} \leq I_O \leq 0.5\text{ A}$ $ V_O \leq 5.0\text{ V}$ $ V_O \geq 5.0\text{ V}$	2	Regload	— —	20 0.3	70 1.5	mV % V_O
Temperature Stability ($T_{low} \leq T_J \leq T_{high}$)	3	T_S	—	0.6	—	% V_O
Minimum Load Current to Maintain Regulation ($ V_I - V_O \leq 10\text{ V}$) ($ V_I - V_O \leq 40\text{ V}$)	3	I_{Lmin}	— —	1.5 2.5	6.0 10	mA
Maximum Output Current $ V_I - V_O \leq 15\text{ V}$, $P_D \leq P_{max}$ $ V_I - V_O = 40\text{ V}$, $P_D \leq P_{max}$, $T_A = 25^\circ\text{C}$	3	I_{max}	0.5 0.1	0.9 0.25	— —	A
RMS Noise, % of V_O $T_A = 25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 10\text{ kHz}$	—	N	—	0.003	—	% V_O
Ripple Rejection, $V_O = -10\text{ V}$, $f = 120\text{ Hz}$ (Note 5) Without C_{adj} $C_{adj} = 10\text{ }\mu\text{F}$	4	RR	— 66	60 77	— —	dB
Long Term Stability, $T_J = T_{high}$ (Note 6) $T_A = 25^\circ\text{C}$ for Endpoint Measurements	3	S	—	0.3	1.0	%/1.0 k Hrs.
Thermal Resistance Junction to Case	—	$R_{\theta JC}$	—	7.0	—	°C/W

NOTES:

(1) T_{low} to $T_{high} = 0^\circ\text{C}$ to $+125^\circ\text{C}$ (2) $P_{max} = 7.5\text{ W}$ (3) Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

(4) Selected devices with tightened tolerance reference voltage available.

(5) C_{adj} , when used, is connected between the adjustment pin and ground.

(6) Since Long Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

LM337M

3

SCHEMATIC DIAGRAM

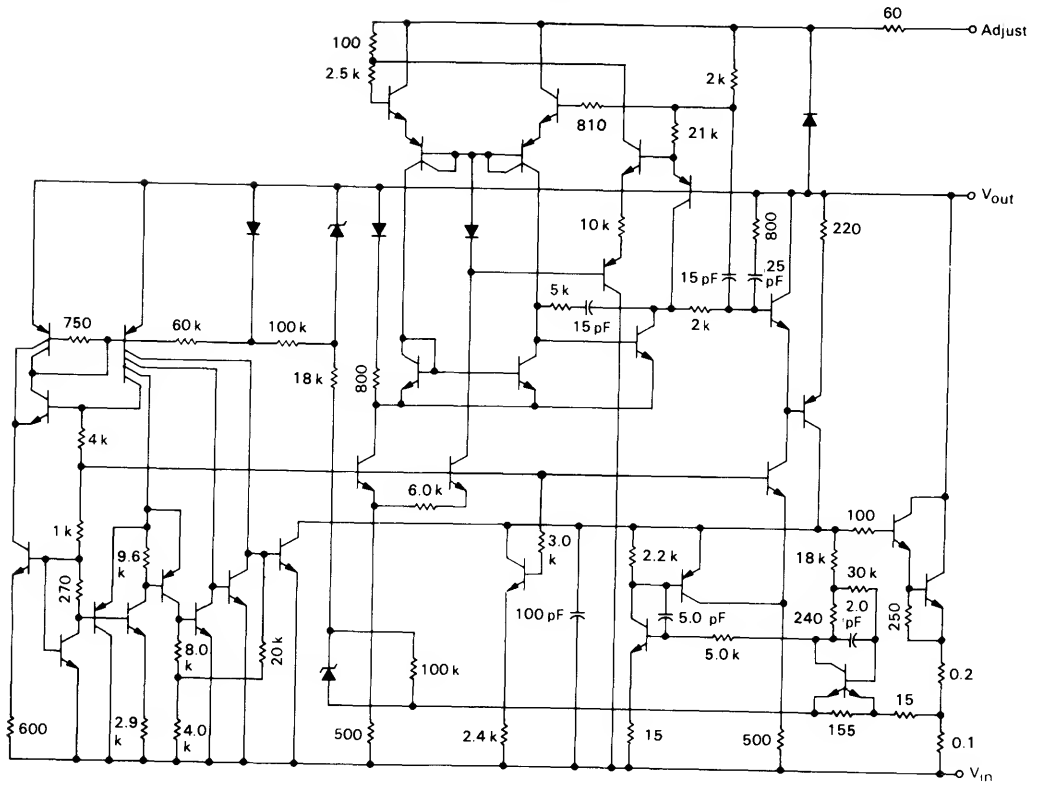


FIGURE 1 - LINE REGULATION AND ΔI_{adj} /LINE TEST CIRCUIT

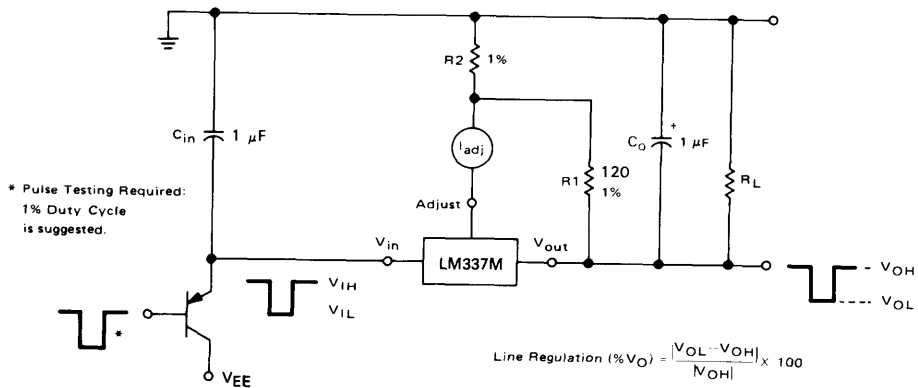


FIGURE 5 – LOAD REGULATION

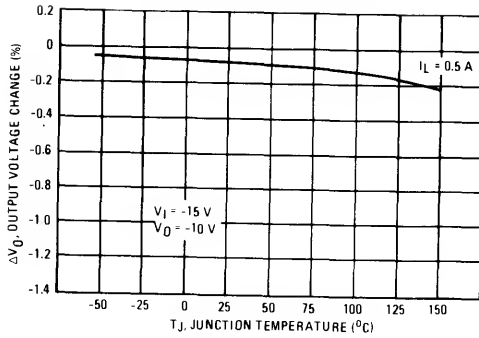


FIGURE 6 – CURRENT LIMIT

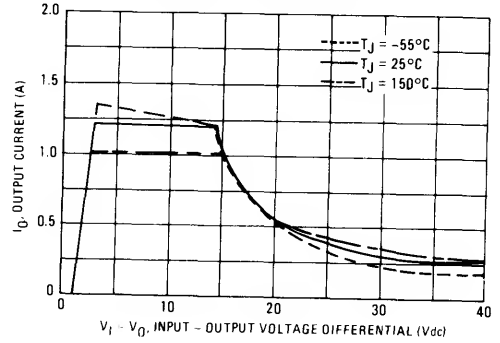


FIGURE 7 – ADJUSTMENT PIN CURRENT

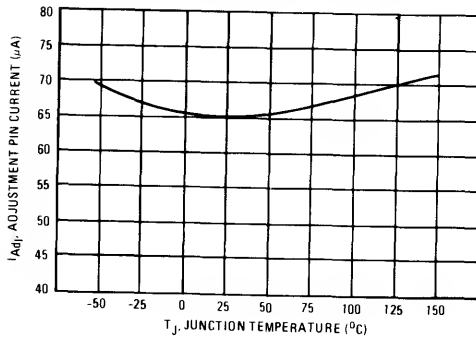


FIGURE 8 – DROPOUT VOLTAGE

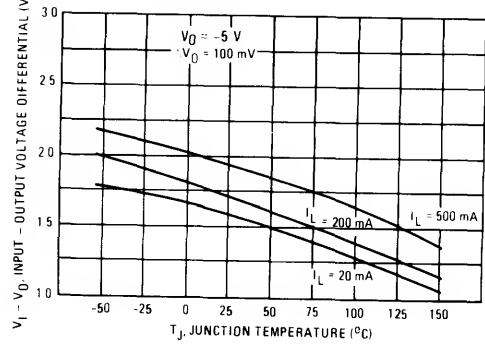


FIGURE 9 – TEMPERATURE STABILITY

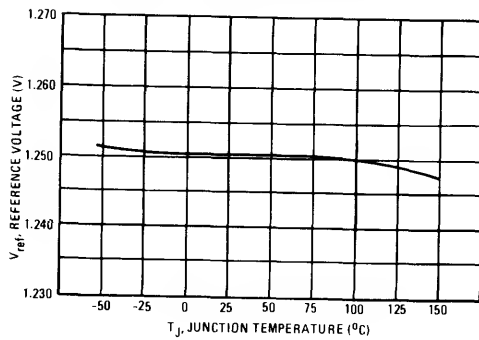


FIGURE 10 – MINIMUM OPERATING CURRENT

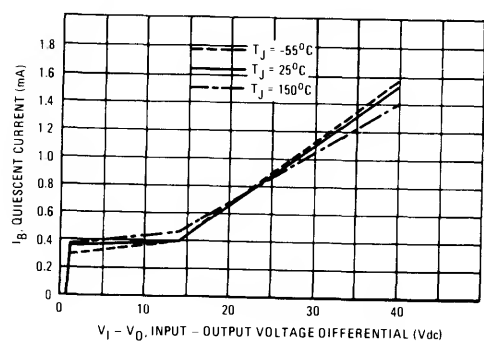


FIGURE 11 — RIPPLE REJECTION versus OUTPUT VOLTAGE

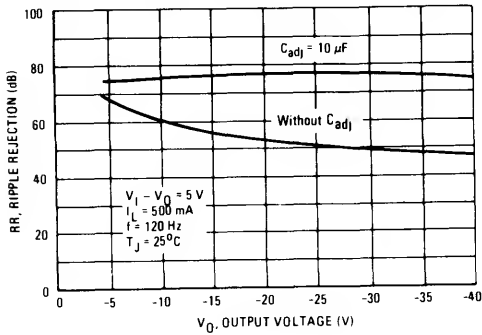


FIGURE 12 — RIPPLE REJECTION versus OUTPUT CURRENT

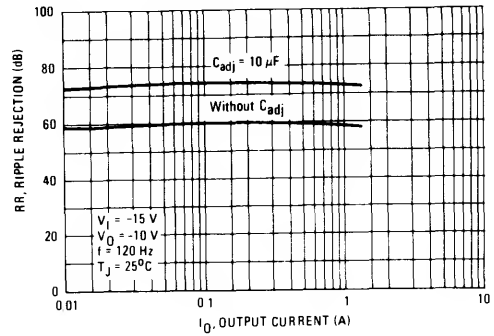


FIGURE 13 — RIPPLE REJECTION versus FREQUENCY

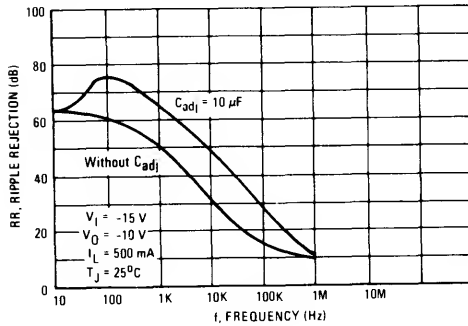


FIGURE 14 — OUTPUT IMPEDANCE

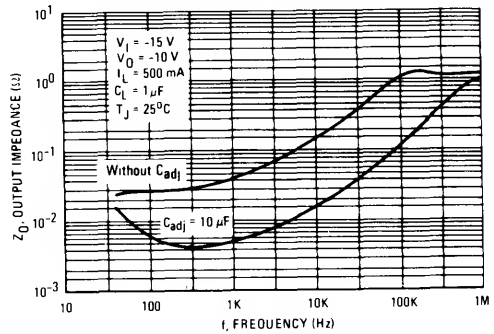


FIGURE 15 — LINE TRANSIENT RESPONSE

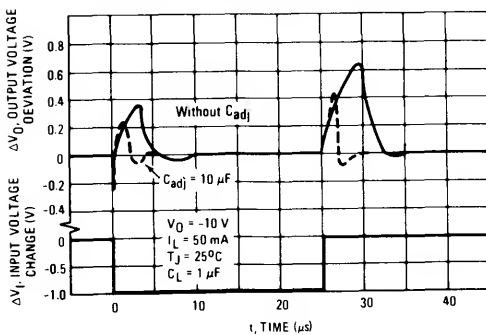
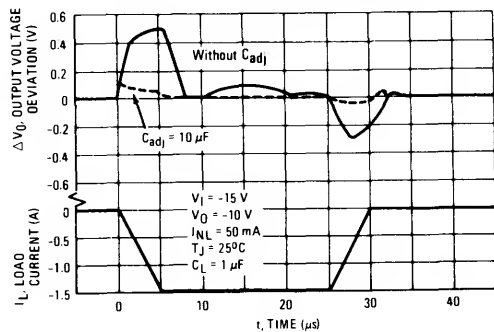


FIGURE 16 — LOAD TRANSIENT RESPONSE



APPLICATIONS INFORMATION

BASIC CIRCUIT OPERATION

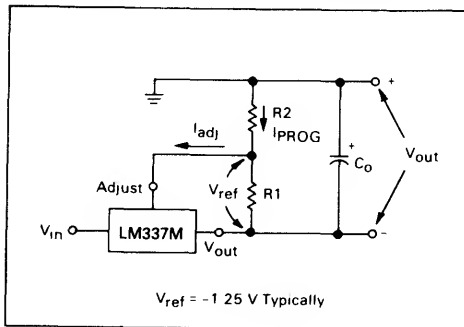
The LM337M is a 3-terminal floating regulator. In operation, the LM337M develops and maintains a nominal -1.25 volt reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by $R1$ (see Figure 17), and this constant current flows through $R2$ from ground. The regulated output voltage is given by:

$$V_{out} = V_{ref} \left(1 + \frac{R2}{R1} \right) + I_{adj} R2$$

Since the current into the adjustment terminal (I_{adj}) represents an error term in the equation, the LM337M was designed to control I_{adj} to less than $100 \mu A$ and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will increase.

Since the LM337M is a floating regulator, it is only the voltage differential across the circuit that is important to performance, and operation at high voltages with respect to ground is possible.

FIGURE 17— BASIC CIRCUIT CONFIGURATION



LOAD REGULATION

The LM337M is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor ($R1$) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of $R2$ can

be returned near the load ground to provide remote ground sensing and improve load regulation.

EXTERNAL CAPACITORS

A $1.0 \mu F$ tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{adj}) prevents ripple from being amplified as the output voltage is increased. A $10 \mu F$ capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 volt application.

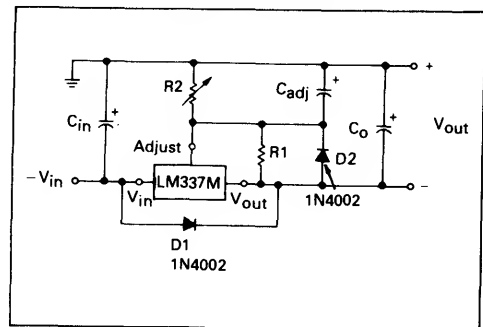
An output capacitor (C_o) in the form of a $1.0 \mu F$ tantalum or $10 \mu F$ aluminum electrolytic capacitor is required for stability.

PROTECTION DIODES

When external capacitors are used with any I.C. regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 18 shows the LM337M with the recommended protection diodes for output voltages in excess of -25 V or high capacitance values ($C_o > 25 \mu F$, $C_{adj} > 10 \mu F$). Diode $D1$ prevents C_o from discharging thru the I.C. during an input short circuit. Diode $D2$ protects against capacitor C_{adj} discharging through the I.C. during an output short circuit. The combination of diodes $D1$ and $D2$ prevents C_{adj} from discharging through the I.C. during an input short circuit.

FIGURE 18— VOLTAGE REGULATOR WITH PROTECTION DIODES



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

LOW DROPOUT VOLTAGE REGULATORS

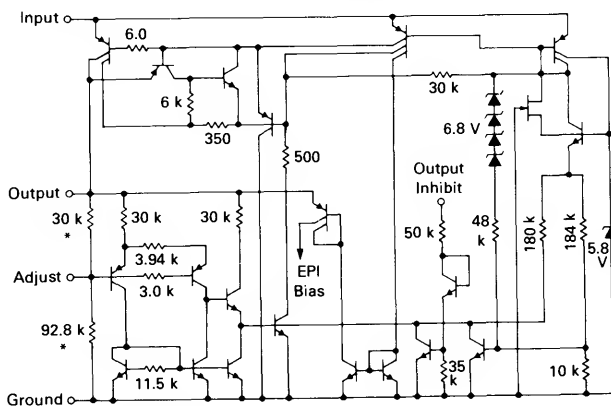
The LM2931 series consists of positive fixed and adjustable output voltage regulators that are specifically designed to maintain proper regulation with an extremely low input-to-output voltage differential. These devices are capable of supplying output currents in excess of 100 mA and feature a low bias current of 0.4 mA at 10 mA output.

Designed primarily to survive in the harsh automotive environment, these devices will protect all external load circuitry from input fault conditions caused by reverse battery connection, two battery jump starts, and excessive line transients during load dump. This series also includes internal current limiting, thermal shutdown, and additionally, is able to withstand temporary power-up with mirror-image insertion.

Due to the low dropout voltage and bias current specifications, the LM2931 series is ideally suited for battery powered industrial and consumer equipment where an extension of useful battery life is desirable. The 'C' suffix adjustable output regulators feature an output inhibit pin which is extremely useful in microprocessor-based systems.

- Input-to-Output Voltage Differential of Less Than 0.6 V at 100 mA
- Output Current in Excess of 100 mA
- Low Bias Current
- 60 V Load Dump Protection
- -50 V Reverse Transient Protection
- Internal Current Limiting with Thermal Shutdown
- Temporary Mirror-Image Protection
- Ideally Suited for Battery Powered Equipment

INTERNAL SCHEMATIC



*Deleted on Adjustable Regulators

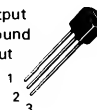
LM2931 Series

LOW DROPOUT VOLTAGE REGULATORS

SILICON MONOLITHIC INTEGRATED CIRCUITS

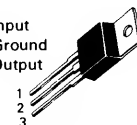
Z SUFFIX
PLASTIC PACKAGE
CASE 29

Pin 1. Output
2. Ground
3. Input

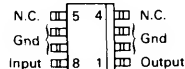


T SUFFIX
PLASTIC PACKAGE
CASE 221A
(Heatsink surface
connected to Pin 2)

Pin 1. Input
2. Ground
3. Output

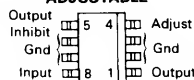


FIXED



(Top View)

ADJUSTABLE



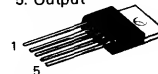
(Top View)

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SOP-8)

ADJUSTABLE

T SUFFIX
PLASTIC PACKAGE
CASE 314D
(Heatsink surface
connected to Pin 3)

Pin 1. Adjust
2. Output Inhibit
3. Ground
4. Input
5. Output



ORDERING INFORMATION

Device	Output		Package Case Number
	Voltage	Tolerance	
LM2931AD-5.0	5.0 V	± 3.8%	751
LM2931AT-5.0	5.0 V	± 3.8%	221A
LM2931AZ-5.0	5.0 V	± 3.8%	29
LM2931D-5.0	5.0 V	± 5.0%	751
LM2931T-5.0	5.0 V	± 5.0%	221A
LM2931Z-5.0	5.0 V	± 5.0%	29
LM2931CD	Adjustable	± 5.0%	751
LM2931CT	Adjustable	± 5.0%	314D

LM2931 Series

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage Continuous	V_{in}	40	V _{dc}
Transient Input Voltage ($\tau \leq 100$ ms)	$V_{in}(\tau)$	60	V _{pk}
Transient Reverse Polarity Input Voltage 1.0% Duty Cycle, $\tau \leq 100$ ms	$-V_{in}(\tau)$	-50	V _{pk}
Power Dissipation Case 29 (TO-92) $T_A = 25^\circ\text{C}$ Thermal Resistance Junction to Ambient Thermal Resistance Junction to Case	P_D θ_{JA} θ_{JC}	Internally Limited 178 83	Watts $^\circ\text{C/W}$ $^\circ\text{C/W}$
Case 751 (SOP-8) $T_A = 25^\circ\text{C}$ Thermal Resistance Junction to Ambient Thermal Resistance Junction to Case	P_D θ_{JA} θ_{JC}	Internally Limited 180 45	Watts $^\circ\text{C/W}$ $^\circ\text{C/W}$
Case 221A and 314D (TO-220 Type) $T_A = 25^\circ\text{C}$ Thermal Resistance Junction to Ambient Thermal Resistance Junction to Case	P_D θ_{JA} θ_{JC}	Internally Limited 65 5.0	Watts $^\circ\text{C/W}$ $^\circ\text{C/W}$
Tested Operating Junction Temperature Range	T_J	-40 to +125	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($V_{in} = 14$ V, $I_O = 10$ mA, $C_O = 100$ μF , $C_O(\text{ESR}) = 0.3$ Ω , $T_J = 25^\circ\text{C}$,
Note 1, unless otherwise noted.)

Characteristic	Symbol	LM2931A-5.0			LM2931-5.0			Unit
		Min	Typ	Max	Min	Typ	Max	
FIXED OUTPUT								
Output Voltage $V_{in} = 14$ V, $I_O = 10$ mA, $T_J = 25^\circ\text{C}$ $V_{in} = 6.0$ V to 26 V, $I_O \leq 100$ mA, $T_J = -40$ to 125°C	V_O	4.81 4.75	5.0 —	5.19 5.25	4.75 4.50	5.0 —	5.25 5.50	V
Line Regulation $V_{in} = 9.0$ V to 16 V $V_{in} = 6.0$ V to 26 V	Reg _{line}	— —	2.0 4.0	10 30	— —	2.0 4.0	10 30	mV
Load Regulation ($I_O = 5.0$ mA to 100 mA)	Reg _{load}	—	14	50	—	14	50	mV
Output Impedance $I_O = 10$ mA, $\Delta I_O = 1.0$ mA, $f = 100$ Hz to 10 kHz	Z_O	—	200	—	—	200	—	m Ω
Bias Current $V_{in} = 14$ V, $I_O = 100$ mA, $T_J = 25^\circ\text{C}$ $V_{in} = 6.0$ V to 26 V, $I_O = 10$ mA, $T_J = -40$ to 125°C	I_B	— —	5.8 0.4	30 1.0	— —	5.8 0.4	30 1.0	mA
Output Noise Voltage ($f = 10$ Hz to 100 kHz)	V_n	—	700	—	—	700	—	μV_{rms}
Long-Term Stability	S	—	20	—	—	20	—	mV/ kHR
Ripple Rejection ($f = 120$ Hz)	RR	60	90	—	60	90	—	dB
Dropout Voltage $I_O = 10$ mA $I_O = 100$ mA	$V_{in}-V_O$	— —	0.015 0.16	0.2 0.6	— —	0.015 0.16	0.2 0.6	V
Over-Voltage Shutdown Threshold	$V_{th}(\text{OV})$	26	29.5	40	26	29.5	40	V
Output Voltage with Reverse Polarity Input ($V_{in} = -15$ V)	$-V_O$	-0.3	0	—	-0.3	0	—	V

NOTES:

- 1) Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
- 2) The reference voltage on the adjustable device is measured from the output to the adjust pin across R_1 .

LM2931 Series

ELECTRICAL CHARACTERISTICS ($V_{in} = 14\text{ V}$, $V_O = 3.0\text{ V}$, $I_O = 10\text{ mA}$, $R_1 = 27\text{ k}$, $C_O = 100\text{ }\mu\text{F}$, $C_O(\text{ESR}) = 0.3\text{ }\Omega$, $T_J = 25^\circ\text{C}$, Note 1, unless otherwise noted.)

T_J = 25°C, Note 1, unless otherwise noted.)

Characteristic	Symbol	LM2931C			Unit
		Min	Typ	Max	
ADJUSTABLE OUTPUT					
Reference Voltage (Note 2, Figure 18) I _O = 10 mA, T _J = 25°C I _O ≤ 100 mA, T _J = -40 to 125°C	V _{ref}	1.14 1.08	1.20 —	1.26 1.32	V
Output Voltage Range	V _{Orange}	3.0	2.7 to 29.5	24	V
Line Regulation (V _{in} = V _O + 0.6 V to 26 V)	Reg _{line}	—	0.2	1.5	mV/V
Load Regulation (I _O = 5.0 mA to 100 mA)	Reg _{load}	—	0.3	1.0	%/V
Output Impedance I _O = 10 mA, ΔI _O = 1.0 mA, f = 10 Hz to 10 kHz	Z _O	—	40	—	mΩ/V
Bias Current I _O = 100 mA I _O = 10 mA Output Inhibited (V _{th(OI)} = 2.5 V)	I _B	— — —	6.0 0.4 0.2	— 1.0 1.0	mA
Adjustment Pin Current	I _{Adj}	—	0.2	—	μA
Output Noise Voltage (f = 10 Hz to 100 kHz)	V _n	—	140	—	μVrms/V
Long-Term Stability	S	—	0.4	—	%/kHR
Ripple Rejection (f = 120 Hz)	RR	0.10	0.003	—	%/V
Dropout Voltage I _O = 10 mA I _O = 100 mA	V _{in-VO}	— —	0.015 0.16	0.2 0.6	V
Over-Voltage Shutdown Threshold	V _{th(OV)}	26	29.5	40	V
Output Voltage with Reverse Polarity Input (V _{in} = -15 V)	-V _O	-0.3	0	—	V
Output Inhibit Threshold Voltages Output "On," T _J = 25°C T _J = -40 to 125°C Output "Off," T _J = 25°C T _J = -40 to 125°C	V _{th(OI)}	— — 2.50 3.25	2.15 — 2.26 —	1.90 1.20 — —	V
Output Inhibit Threshold Current (V _{th(OI)} = 2.5 V)	I _{th(OI)}	—	30	50	μA

NOTES:

- 1) Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
- 2) The reference voltage on the adjustable device is measured from the output to the adjust pin across R_1 .

DEFINITIONS

Dropout Voltage — The input/output voltage differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output decreases 100 mV from nominal value at 14 V input, dropout voltage is affected by junction temperature and load current.

Line Regulation — The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation — The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation — The maximum total device dissipation for which the regulator will operate within specifications.

Bias Current — That part of the input current that is not delivered to the load.

Output Noise Voltage — The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long-Term Stability — Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices electrical characteristics and maximum power dissipation.

FIGURE 1 — DROPOUT VOLTAGE versus OUTPUT CURRENT

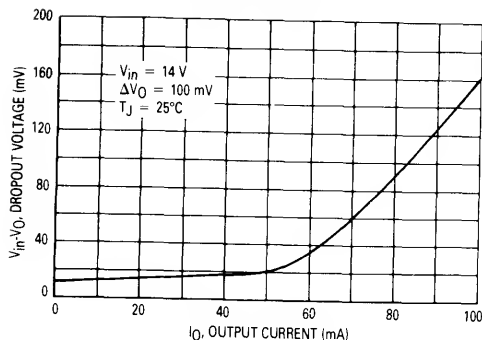


FIGURE 2 — DROPOUT VOLTAGE versus JUNCTION TEMPERATURE

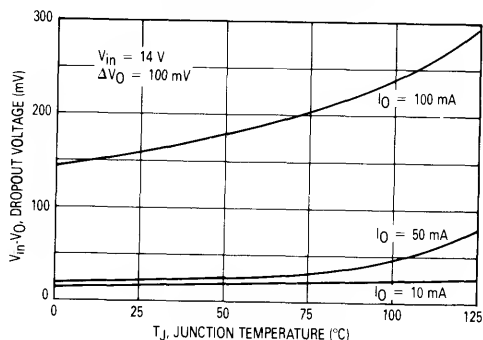


FIGURE 3 — PEAK OUTPUT CURRENT versus INPUT VOLTAGE

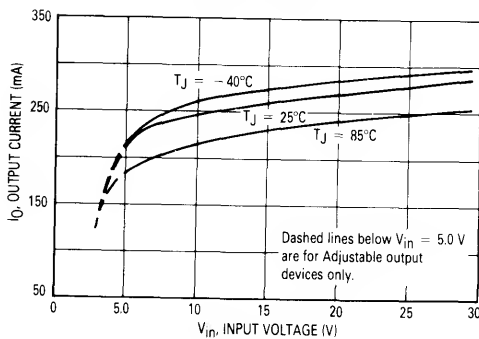


FIGURE 4 — OUTPUT VOLTAGE versus INPUT VOLTAGE

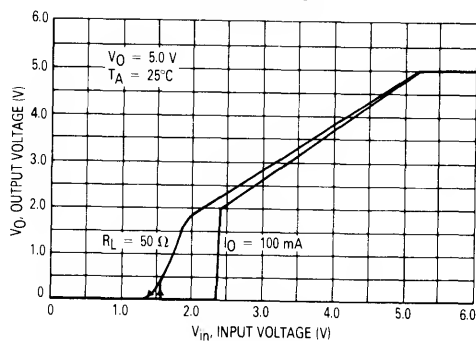


FIGURE 5 — OUTPUT VOLTAGE versus INPUT VOLTAGE

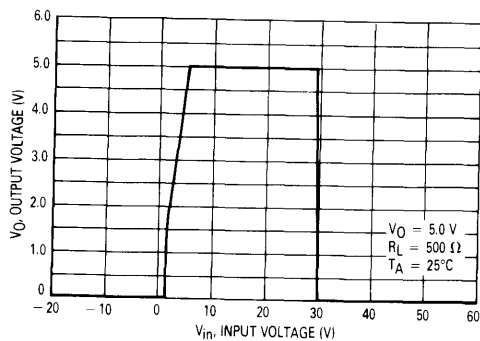
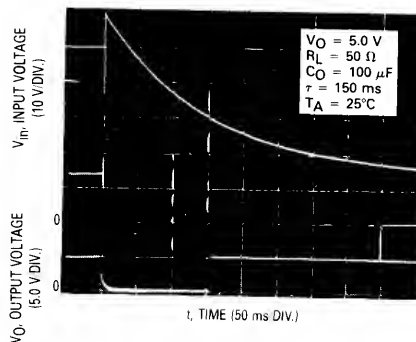


FIGURE 6 — LOAD DUMP CHARACTERISTICS



LM2931 Series

FIGURE 7 — BIAS CURRENT versus INPUT VOLTAGE

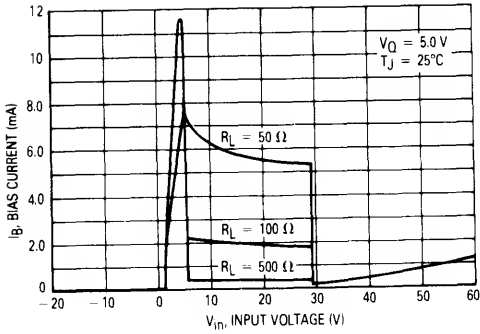
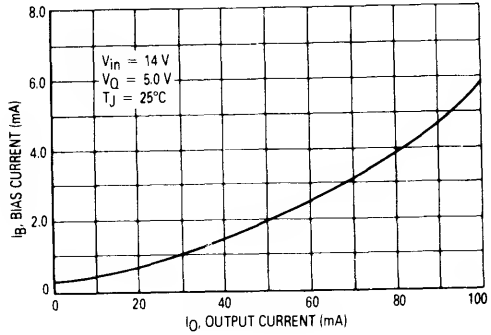


FIGURE 8 — BIAS CURRENT versus OUTPUT CURRENT



3

FIGURE 9 — BIAS CURRENT versus JUNCTION TEMPERATURE

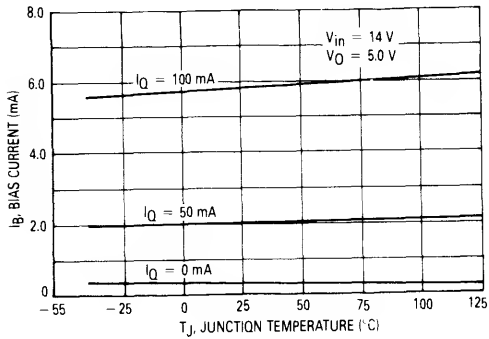


FIGURE 10 — OUTPUT IMPEDANCE versus FREQUENCY

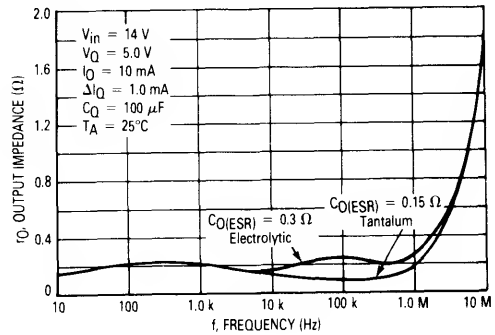


FIGURE 11 — RIPPLE REJECTION versus FREQUENCY

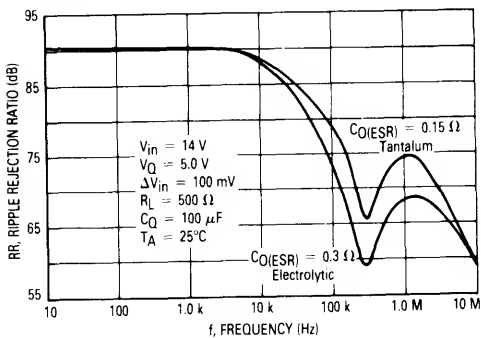
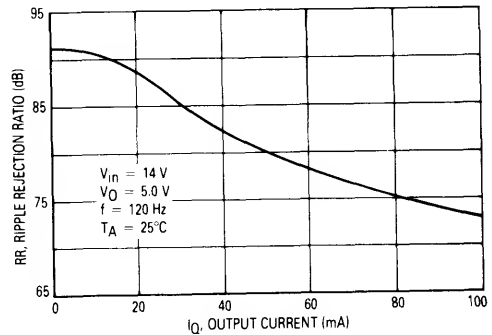


FIGURE 12 — RIPPLE REJECTION versus OUTPUT CURRENT



LM2931 Series

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FIGURE 13 — LINE REGULATION

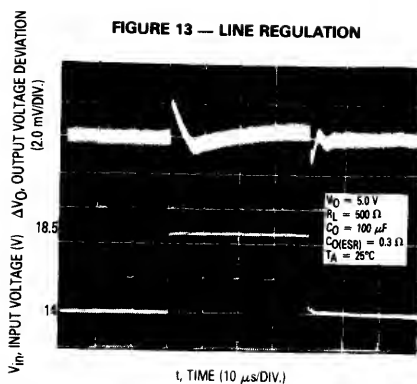


FIGURE 14 — LOAD REGULATION

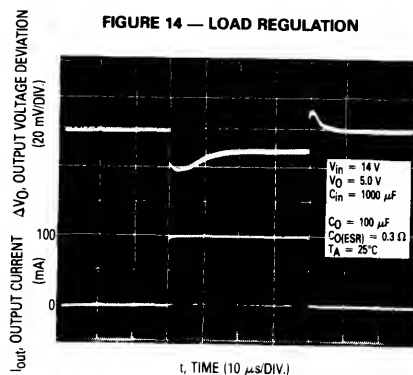


FIGURE 15 — REFERENCE VOLTAGE versus OUTPUT VOLTAGE

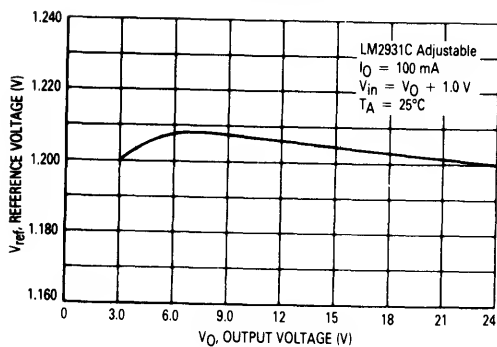
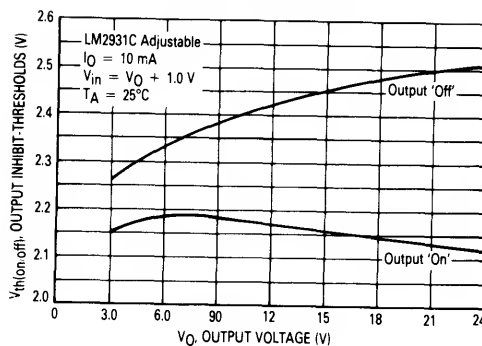


FIGURE 16 — OUTPUT INHIBIT-THRESHOLDS versus OUTPUT VOLTAGE



TYPICAL APPLICATIONS

FIGURE 17 — FIXED OUTPUT REGULATOR

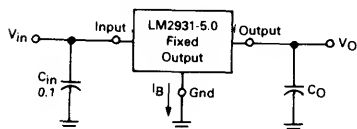
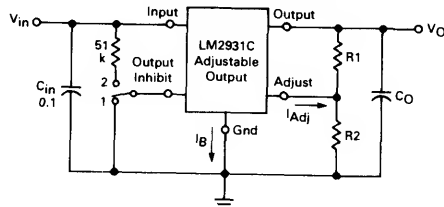


FIGURE 18 — ADJUSTABLE OUTPUT REGULATOR



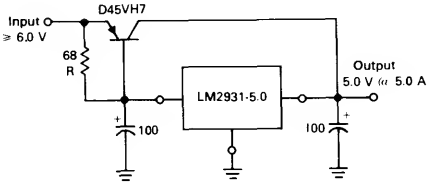
Switch Position 1 = Output 'On,' 2 = Output 'Off'

$$V_O = V_{ref} \left(1 + \frac{R_2}{R_1} \right) + I_{Adj} R_2 \quad 22.5 \text{ k} \geq \frac{R_1 R_2}{R_1 + R_2}$$

LM2931 Series

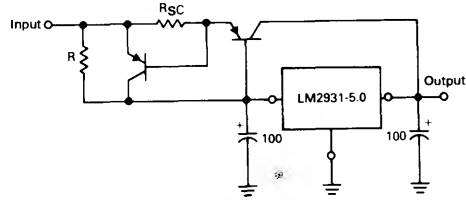
TYPICAL APPLICATIONS (continued)

FIGURE 19 — 5.0 A LOW DIFFERENTIAL VOLTAGE REGULATOR



The LM2931 series can be current boosted with a PNP transistor. The D45VH7, on a heatsink, will provide an output current of 5.0 A with an input to output voltage differential of approximately 1.0 V. Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting. This circuit is not short-circuit proof.

FIGURE 20 — CURRENT BOOST REGULATOR WITH SHORT-CIRCUIT PROJECTION



The circuit of Figure 19 can be modified to provide supply protection against short circuits by adding the current sense resistor R_{SC} and an additional PNP transistor. The current sensing PNP must be capable of handling the short-circuit current of the LM2931. Safe operating area of both transistors must be considered under worst case conditions.

FIGURE 21 — CONSTANT INTENSITY LAMP FLASHER

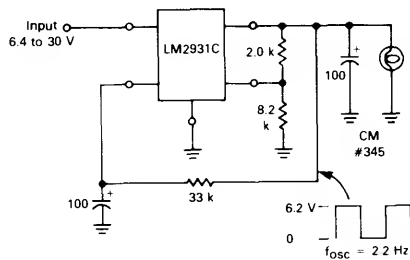
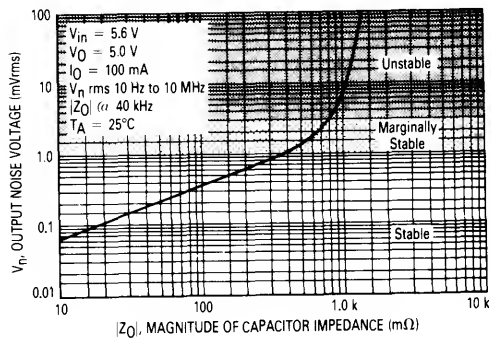


FIGURE 22 — OUTPUT NOISE VOLTAGE versus OUTPUT CAPACITOR IMPEDANCE



APPLICATIONS INFORMATION

The LM2931 series regulators are designed with many protection features making them essentially blow-out proof. These features include internal current limiting, thermal shutdown, overvoltage and reverse polarity input protection, and the capability to withstand temporary power-up with mirror-image insertion. Typical application circuits for the fixed and adjustable output device are shown in Figures 17 and 18.

The input bypass capacitor C_{in} is recommended if the regulator is located an appreciable distance ($\geq 4'$) from the supply input filter. This will reduce the circuit's sensitivity to the input line impedance at high frequencies.

This regulator series is not internally compensated and thus requires an external output capacitor for stability. The capacitance value required is dependent upon the load current, output voltage for the adjustable regulator, and the type of capacitor selected. The least-stable condition is encountered at maximum load current and minimum output voltage. Figure 22 shows that for operation in the "Stable" region, under the conditions specified, the magnitude of the output capacitor impedance $|Z_O|$ must not exceed 0.4 Ω . This limit must

be observed over the entire operating temperature range of the regulator circuit.

With economical electrolytic capacitors, cold temperature operation can pose a serious stability problem. As the electrolyte freezes, around -30°C , the capacitance will decrease and the equivalent series resistance ESR will increase drastically, causing the circuit to oscillate. Quality electrolytic capacitors with extended temperature ranges of -40 to 85°C and -55 to 105°C are readily available. Solid tantalum capacitors may be a better choice if small size is a requirement, however, the maximum $|Z_O|$ limit over temperature must be observed.

Note that in the stable region, the output noise voltage is linearly proportional to $|Z_O|$. In effect, C_O dictates the high frequency roll-off point of the circuit. Operation in the area titled "Marginally Stable" will cause the output of the regulator to exhibit random bursts of oscillation that decay in an under-damped fashion. Continuous oscillation occurs when operating in the area titled "Unstable." It is suggested that oven testing of the entire circuit be performed with maximum load, minimum input voltage, and minimum ambient temperature.

Product Preview

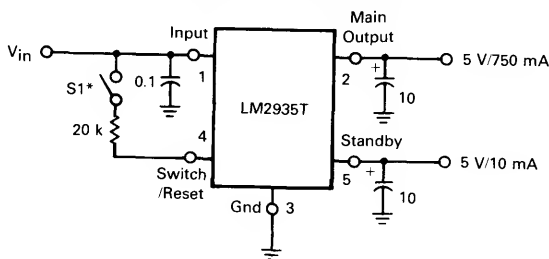
LOW DROPOUT DUAL REGULATOR

The LM2935 is a dual positive 5.0 volt low dropout voltage regulator, designed for standby power systems. The Main Output is capable of supplying 750 mA for microprocessor power, and can be turned on and off by the Switch/Reset input. The other output is dedicated for standby operation of volatile memory, and is capable of supplying up to 10 mA loads. The total device features a low quiescent current of 3.0 mA or less when supplying 10 mA from the Standby Output.

This part was designed for harsh automotive environments and is therefore immune to many input supply voltage problems such as reverse battery (-12 V), double battery ($+24$ V), and load dump transients ($+60$ V).

- Two Regulated 5.0 Volt Outputs
- Main Output Current in Excess of 750 mA
- On/Off Control of Main Output
- Standby Output Current in Excess of 10 mA
- Low Input-Output Differential of Less Than 0.6 V at 500 mA
- Short Circuit Current Limiting
- Internal Thermal Shutdown
- Low Voltage Indicator Output
- Designed for Automotive Environment Including:
 - Reverse Battery Protection
 - Double Battery Protection
 - Load Dump Protection
 - Reverse Transient Protection
- Five Pin TO-220 Package

TYPICAL APPLICATION CIRCUIT



*Note: The Main Output is "Off" with switch S1 open.

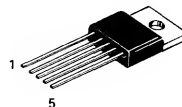
An input bypass capacitor is recommended if the regulator is located more than 4" from the supply input filter. The LM2935 is not internally compensated and thus requires an external output capacitor for stability. A minimum capacitance of 10 μ F is recommended. The actual capacitance value is dependent upon load current, temperature, and the capacitor's equivalent series resistance (ESR). The least stable condition is encountered at maximum load current and minimum ambient temperature.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

LM2935T

LOW DROPOUT DUAL REGULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



T SUFFIX
 PLASTIC PACKAGE
 CASE 314D
 (5 LEAD TO-220 TYPE)

PIN CONNECTIONS



- Pin 1. Input
 2. Main Output
 3. Ground
 4. Switch/Reset
 5. Standby Output

(Heatsink surface connected to Pin 3)

ORDERING INFORMATION

Device	Operating Junction Temperature Range	Package
LM2935T	-40 to $+125^{\circ}\text{C}$	Plastic Power

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage Continuous	V_{in}	60	Vdc
Transient Reverse Polarity Input Voltage 1.0% Duty Cycle, $\tau \leq 100$ ms	$-V_{in}(\tau)$	-50	Vpk
Power Dissipation and Thermal Characteristics Case 3140 (TO-220) T Suffix Maximum Power Dissipation Thermal Resistance Junction to Air Thermal Resistance Junction to Case (Pin 3)	P_D θ_{JA} θ_{JC}	Internally Limited 62.5 1.9	W °C/W °C/W
Operating Junction Temperature Range	T_J	-40 to +150	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS ($V_{in} = 14$ V, $I_O = 500$ mA, $I_{stby} = 0$ mA, $C_O = 10$ μ F, $C_{stby} = 10$ μ F, $T_J = 25^\circ$ C,
Note 1, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
MAIN OUTPUT					
Output Voltage $V_{in} = 6.0$ V to 26 V, $I_O = 5.0$ mA to 500 mA, $T_J = -40^\circ$ C to 125°C	V_O	4.75	5.0	5.25	V
Line Regulation $V_{in} = 9.0$ V to 16 V, $I_O = 5.0$ mA $V_{in} = 6.0$ V to 26 V, $I_O = 5.0$ mA	Regline	—	4.0 10	25 50	mV
Load Regulation ($I_O = 5.0$ mA to 500 mA)	Regload	—	10	50	mV
Output Impedance $I_O = 500$ mAdc and 10 mArms, $f = 100$ Hz to 10 kHz	Z_O	—	200	—	m Ω
Output Noise Voltage ($f = 10$ Hz to 100 kHz)	V_n	—	100	—	μ Vrms
Long Term Stability	S	—	20	—	mV/kHR
Ripple Rejection ($f = 120$ Hz)	RR	—	66	—	dB
Dropout Voltage $I_O = 500$ mA $I_O = 750$ mA	$V_{in}-V_O$	— —	0.45 0.82	0.6 —	V
Short Circuit Current Limit	I_{SC}	0.75	1.2	—	A
Overvoltage Shutdown Threshold	$V_{th(OV)}$	26	31	—	V
Reset Output Voltage Low State, $V_{in} = 4.0$ V, $R_{On/Off} = 20$ k Ω High State, $V_{in} = 14$ V, $R_{On/Off} = 20$ k Ω	V_{OL} V_{OH}	— 4.5	0.9 5.0	1.2 6.0	V
Reset Output Current ($V_{Reset} = 1.2$ V)	I_{Sink}	—	5.0	—	mA
Reset Pull-Up Resistor, On/Off	$R_{On/Off}$	—	20	30	k Ω
Output Voltage with Reverse Polarity Input ($V_{in} = -15$ V, $R_L = 10$ Ω)	$-V_O$	-0.6	0	—	V

NOTE:

1. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

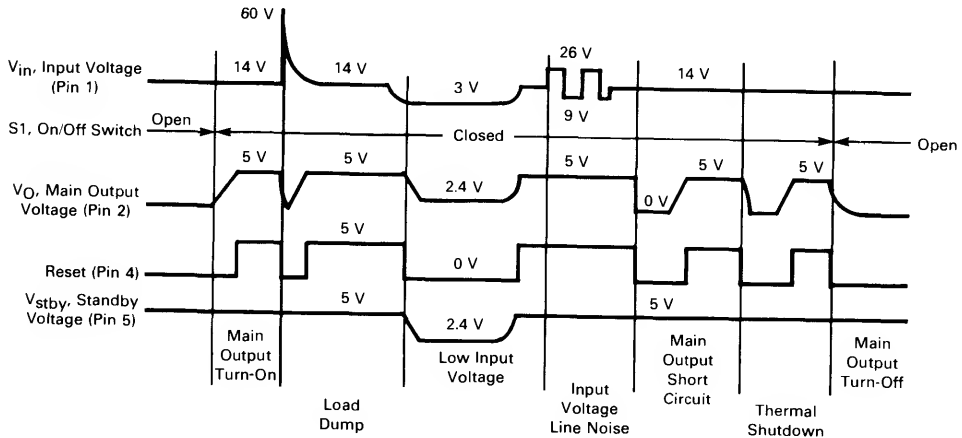
LM2935T

ELECTRICAL CHARACTERISTICS (continued) ($V_{in} = 14\text{ V}$, $I_O = 0\text{ mA}$, $I_{stby} = 10\text{ mA}$, $C_O = 10\text{ }\mu\text{F}$, $C_{stby} = 10\text{ }\mu\text{F}$, $T_J = 25^\circ\text{C}$, Note 1, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
STANDBY OUTPUT					
Output Voltage $V_{in} = 6.0\text{ V to }26\text{ V}$, $I_{stby} = 1.0\text{ mA to }10\text{ mA}$, $T_J = -40^\circ\text{C to }125^\circ\text{C}$	$V_O(stby)$	4.75	5.0	5.25	V
Tracking Voltage	$V_O - V_O(stby)$	-200	0	200	mV
Line Regulation ($V_{in} = 6.0\text{ V to }26\text{ V}$)	Reg _{line}	—	4.0	50	mV
Load Regulation ($I_{stby} = 1.0\text{ mA to }10\text{ mA}$)	Reg _{load}	—	10	50	mV
Output Impedance $I_{stby} = 10\text{ mA}$ dc and 1.0 mA rms, $f = 100\text{ Hz to }10\text{ kHz}$	$Z_O(stby)$	—	1.0	—	Ω
Output Noise Voltage ($f = 10\text{ Hz to }100\text{ kHz}$)	V_n	—	300	—	μVrms
Long Term Stability	S	—	20	—	mV/kHR
Ripple Rejection ($f = 120\text{ Hz}$)	RR	—	66	—	dB
Dropout Voltage ($I_{stby} = 10\text{ mA}$)	$V_{in} - V_O(stby)$	—	0.55	0.7	V
Short Circuit Current Limit	I_{SC}	25	70	—	mA
Output Voltage with Reverse Polarity Input ($V_{in} = -15\text{ V}$, $R_L = 510\text{ }\Omega$)	$-V_O$	-0.3	0	—	V
Output Voltage with Maximum Positive Input $V_{in} = 60\text{ V}$, $R_L = 510\text{ }\Omega$	$V_O(max)$	—	5.0	6.0	V
TOTAL DEVICE					
Bias Current $I_O = 10\text{ mA}$, $I_{stby} = 0\text{ mA}$ $I_O = 500\text{ mA}$, $I_{stby} = 0\text{ mA}$ $I_O = 750\text{ mA}$, $I_{stby} = 0\text{ mA}$ Main Output "Off", $I_{stby} = 10\text{ mA}$	I_B	—	3.0 40 90 2.0	— 100 — 3.0	mA

NOTE 1: Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

TYPICAL CIRCUIT WAVEFORMS



PRECISION WIDE RANGE VOLTAGE and CURRENT REGULATOR

This unique "floating" regulator can deliver hundreds of volts — limited only by the breakdown voltage of the external series pass transistor. Output voltage and output current are adjustable. The MC1466L integrated circuit voltage and current regulator is designed to give "laboratory" power-supply performance.

- Voltage/Current Regulation with Automatic Crossover
- Excellent Line Voltage Regulation, 0.03% + 3.0 mV (Max)
- Excellent Load Voltage Regulation, 0.03% + 3.0 mV (Max)
- Excellent Current Regulation, 0.2% + 1.0 mA
- Short-Circuit Protection
- Output Voltage Adjustable to Zero Volts
- Internal Reference Voltage
- Adjustable Internal Current Source

L SUFFIX
CERAMIC PACKAGE
CASE 632

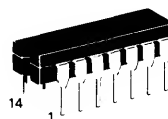


FIGURE 1 — 0-TO-15 Vdc, 10-AMPERES REGULATOR

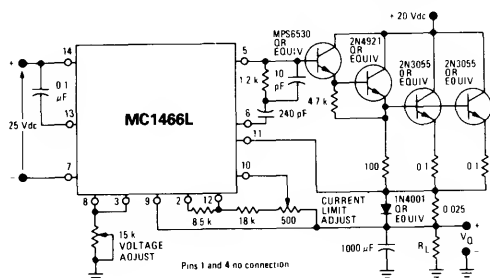


FIGURE 2 — 0-TO-40 Vdc, 0.5-AMPERE REGULATOR

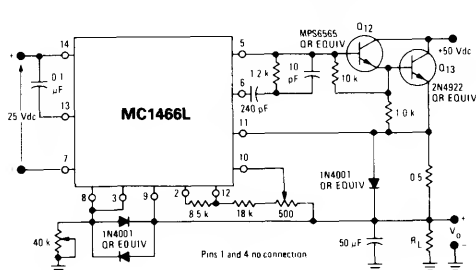


FIGURE 3 — O-TO-25 V_{dc}, 0.1-AMPERE REGULATOR

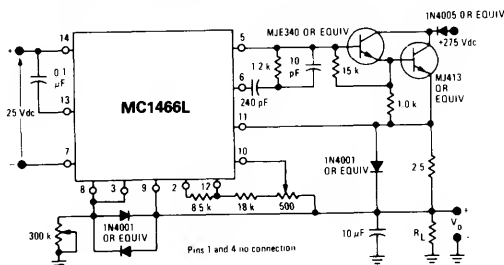
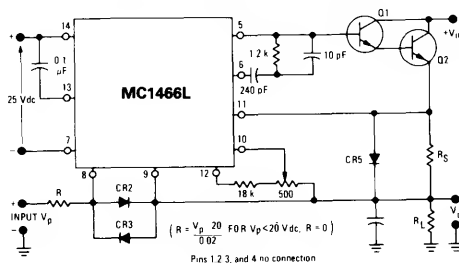


FIGURE 4 — REMOTE PROGRAMMING



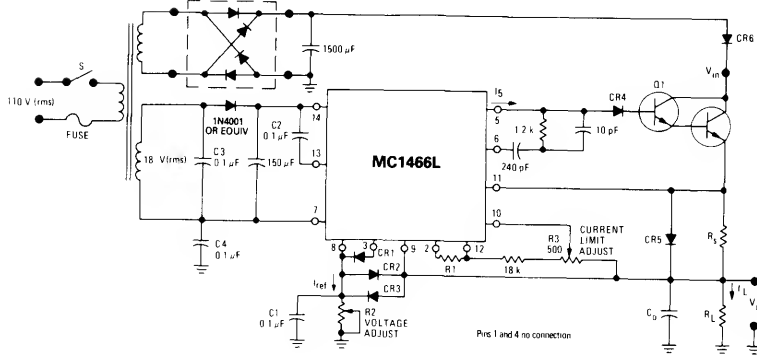
3

Rating	Symbol	Value	Unit
Auxiliary Voltage	V_{aux}	30	Vdc
Power Dissipation (Package Limitation) Derate above $T_A = +50^\circ\text{C}$	P_D $1/\theta_{JA}$	750 6.0	mW mW/°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

Characteristic Definition	Characteristic	Symbol	Min	Typ	Max	Units
<p>Circuit diagram showing the connection for measuring Auxiliary Voltage (V_{aux}). The circuit includes a load resistor R_L connected between pins 14 and 7.</p>	Auxiliary Voltage (See Notes 1 & 2) (Voltage from pin 14 to pin 7)	V_{aux}	21	—	30	Vdc
<p>Circuit diagram showing the connection for measuring Auxiliary Current (I_{aux}). The circuit includes a load resistor R_L connected between pins 14 and 7.</p>	Auxiliary Current	I_{aux}	—	9.0	12	mAdc
<p>Circuit diagram showing the connection for measuring Internal Reference Voltage (V_{IR}). The circuit includes a load resistor R_L connected between pins 12 and 7.</p>	Internal Reference Voltage (Voltage from pin 12 to pin 7)	V_{IR}	17.3	18.2	19.7	Vdc
<p>Circuit diagram showing the connection for measuring Reference Current (I_{ref}). The circuit includes a load resistor R_L connected between pins 14 and 7.</p>	Reference Current (See Note 3)	I_{ref}	0.8	1.0	1.2	mAdc
<p>Circuit diagram showing the connection for measuring Input Current (I_8) at Pin 8. The circuit includes a load resistor R_L connected between pins 8 and 7.</p>	Input Current — Pin 8	I_8	—	6.0	12	μ Adc
<p>Circuit diagram showing the connection for measuring Power Dissipation (P_D). The circuit includes a load resistor R_L connected between pins 14 and 7.</p>	Power Dissipation	P_D	—	—	360	mW
<p>Circuit diagram showing the connection for measuring Input Offset Voltage, Voltage Control Amplifier (V_{ioV}). The circuit includes a load resistor R_L connected between pins 14 and 7.</p>	Input Offset Voltage, Voltage Control Amplifier (See Note 4)	V_{ioV}	0	15	40	mVdc
<p>Circuit diagram showing the connection for measuring Load Voltage Regulation ($\Delta V_{ioV}/\Delta V_{ref}$). The circuit includes a load resistor R_L connected between pins 14 and 7.</p>	Load Voltage Regulation (See Note 5)	$\frac{\Delta V_{ioV}}{\Delta V_{ref}}$	—	1.0 0.015	3.0 0.03	mV %
<p>Circuit diagram showing the connection for measuring Line Voltage Regulation ($\Delta V_{ioV}/\Delta V_{ref}$). The circuit includes a load resistor R_L connected between pins 14 and 7.</p>	Line Voltage Regulation (See Note 6)	$\frac{\Delta V_{ioV}}{\Delta V_{ref}}$	—	1.0 0.015	3.0 0.03	mV %
<p>Circuit diagram showing the connection for measuring Temperature Coefficient of Output Voltage (TCV_o). The circuit includes a load resistor R_L connected between pins 14 and 7.</p>	Temperature Coefficient of Output Voltage ($T_A = 0 \text{ to } +75^\circ\text{C}$)	TCV_o	—	0.01	—	%/ $^\circ\text{C}$
<p>Circuit diagram showing the connection for measuring Input Offset Voltage, Current Control Amplifier (V_{ioI}). The circuit includes a load resistor R_L connected between pins 14 and 7.</p>	Input Offset Voltage, Current Control Amplifier (See Note 4) (Voltage from pin 10 to pin 11)	V_{ioI}	0	15	40	mVdc
<p>Circuit diagram showing the connection for measuring Load Current Regulation ($\Delta I_L/I_L$). The circuit includes a load resistor R_L connected between pins 14 and 7.</p>	Load Current Regulation (See Note 7)	$\frac{\Delta I_L}{I_L}$	—	0.2 —	— 1.0	% mAdc

*Pins 1 and 4 no connection.

FIGURE 6 — TYPICAL CIRCUIT CONNECTION



NORMAL DESIGN PROCEDURE AND DESIGN CONSIDERATIONS

1. Constant Voltage:

For constant voltage operation, output voltage V_O is given by:

$$V_O = (I_{ref}) (R_2)$$

where R_2 is the resistance from pin 8 to ground and I_{ref} is the output current of pin 3.

The recommended value of I_{ref} is 1.0 mAdc. Resistor R_1 sets the value of I_{ref} :

$$I_{ref} = \frac{8.5}{R_1}$$

where R_1 is the resistance between pins 2 and 12.

2. Constant Current:

For constant current operation:

- Select R_S for a 250 mV drop at the maximum desired regulated output current, I_{max} .
 - Adjust potentiometer R_3 to set constant current output at desired value between zero and I_{max} .
3. If V_{in} is greater than 20 Vdc, CR2, CR3, and CR4 are necessary to protect the MC1466 during short circuit or transient conditions.
4. In applications where very low output noise is desired, R_2 may be bypassed with C_1 (0.1 μ F to 2.0 μ F). When R_2 is bypassed, CR1 is necessary for protection during short circuit conditions.
5. CR5 is recommended to protect the MC1466 from simultaneous pass transistor failure and output short circuit.

6. The RC network (10 pF, 240 pF, 1.2 k Ω) is used for compensation. The values shown are valid for all applications. However, the 10 pF capacitor may be omitted if f_r of Q1 and Q2 is greater than 0.5 MHz.

7. For remote sense applications, the positive voltage sense terminal (Pin 9) is connected to the positive load terminal through a separate sense lead; and the negative sense terminal (the ground side of R_2) is connected to the negative load terminal through a separate sense lead.

8. C_O may be selected by using the relationship:

$$C_O = (100 \mu F) I_{L(max)}$$

where $I_{L(max)}$ is the maximum load current in amperes.

9. C_2 is necessary for the internal compensation of the MC1466.

10. For optimum regulation, current out of Pin 5, I_5 should not exceed 0.5 mAdc. Therefore select Q1 and Q2 such that:

$$\frac{I_{max}}{\beta_1 \beta_2} \leq 0.5 \text{ mAdc}$$

where: I_{max} = maximum short-circuit load current (mAdc)

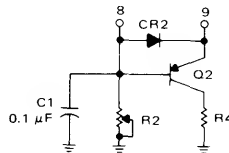
β_1 = minimum beta of Q1

β_2 = minimum beta of Q2

Although Pin 5 will source up to 1.5 mAdc, $I_5 > 0.5$ mAdc will result in a degradation in regulation.

11. CR6 is recommended when $V_O > 150$ Vdc and should be rated such that Peak Inverse Voltage $> V_O$.

12. In applications where R_2 might be rapidly reduced in value, it is recommended that CR3 be replaced by Q2 and R4.



This design consideration prevents R_2 from being destroyed by excessive discharge current from C_O . Components Q2 and R4 should be selected such that:

$$R_4 = \frac{R_2}{10} \text{ and}$$

$$V_{CEO} \text{ of } Q_2 \geq V_O$$

OPERATION AND APPLICATIONS

This section describes the operation and design of the MC1466 voltage and current regulator and also provides information on useful applications.

THEORY OF OPERATION

The schematic of Figure 5 can be simplified by breaking it down into basic functions, beginning with a simplified version of the voltage reference, Figure 7. Zener diodes CR1 and CR5 with their associated forward biased diodes CR2 through CR4 and CR6 through CR8 form the stable reference needed to balance the differential amplifier. At balance ($V_{B1} = V_{B2}$), the output voltage, ($V_{12} - V_7$), is at a value that is twice the drop across either of the two diode strings: $V_{12} - V_7 = 2 (V_{CR1} + V_{CR2} + V_{CR3} + V_{CR4})$. Other voltages, temperature compensated or otherwise, are also derived from these diodes strings for use in other parts of the circuit.

The voltage controlled current source (Figure 8) is a PNP-NPN composite which, due to the high NPN beta,

yields a good working PNP from a lateral device working at a collector current of only a few microamperes. Its base voltage (V_{B2}) is derived from a temperature compensated portion of the diode string and consequently the overall current is dependent on the value of emitter resistor R1. Temperature compensation of the base emitter junction of Q3 is not important because approximately 9 volts exists between V_{B2} and V_{12} , making the ΔV_{BE} 's very small in percentage. Circuit reference voltage is derived from the product of I_R and R_R ; if I_R is set at 1 mA ($R_1 = 8.5 \text{ k}\Omega$), then R_R (in $\text{k}\Omega$) = V_O . Other values of current may be used as long as the following restraints are kept in mind: 1) package dissipation will be increased by about 11 mW/mA and 2) bias current for the voltage control amplifier is $3 \mu\text{A}$, temperature dependent, and is extracted from the reference current. The reference current should

FIGURE 7 — REFERENCE VOLTAGE REGULATOR

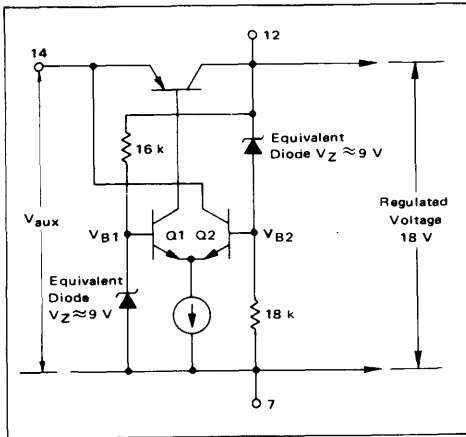
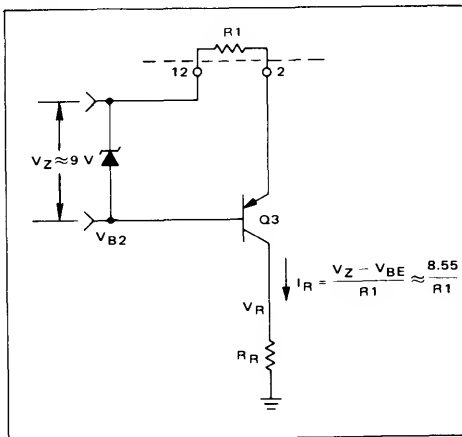


FIGURE 8 — VOLTAGE CONTROLLED CURRENT SOURCE



be at least two orders of magnitude above the largest expected bias current.

Loop amplification in the constant voltage mode is supplied by the voltage controlled amplifier (Figure 9), a standard high gain differential amplifier. The inputs are diode-protected against differential overvoltages and an emitter degenerating resistor, R_{OS} , has been added to one of the transistors. For an emitter current in both Q5 and Q6 of 1/2 milliampere there will exist a preset offset voltage in this differential amplifier of 15 mV to insure that the output voltage will be zero when the reference voltage is zero. Without R_{OS} , the output voltage could be a few millivolts above zero due to the inherent offset. Since the load resistor is so large in this stage compared with the load (Q9) it will be more instructive to look at the gain on a transconductance basis rather than voltage gain. Transconductance of the differential stage is defined for small signals as:

$$g_m = \frac{1}{2r_e + R_E} \quad (1)$$

where

$$r_e \approx \frac{0.026}{I_E} \text{ and}$$

R_E = added emitter degenerating resistance.

For $I_E = 0.5 \text{ mA}$,

$$g_m = \frac{1}{104 + 30} = \frac{1}{134} = 7.5 \text{ mA/volt.} \quad (2)$$

FIGURE 9 - VOLTAGE CONTROL AMPLIFIER

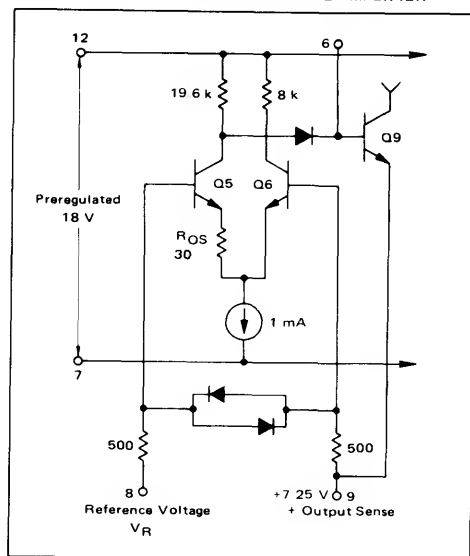
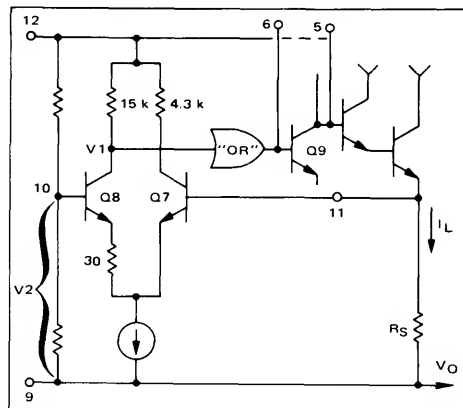


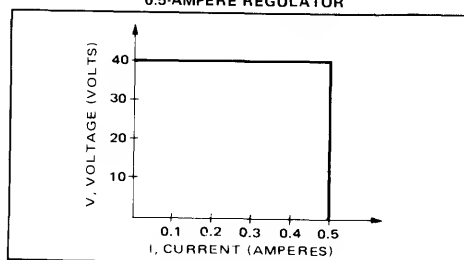
FIGURE 10 - CURRENT CONTROL CIRCUIT



This level is further boosted by the output stage such that in the constant voltage mode overall transconductance is about 300 mA/volt.

A second differential stage nearly identical to the first stage, serves as the current control amplifier (Figure 10). The gain of this stage insures a rapid crossover from the constant voltage to constant current modes and provides a convenient point to control the maximum deliverable load current. In use, a reference voltage derived from the preregulator and a voltage divider is applied to pin 10 while the output current is sampled across R_S by pin 11. When $I_L R_S$ is 15 mV below the reference value, voltage V_1 begins to rapidly rise, eventually gaining complete control of Q9 and limiting output current to a value of V_2/R_S . If V_2 is derived from a variable source, short circuit current may be controlled over the complete output current capability of the regulator. Since the constant-voltage to constant-current change-over requires only a few millivolts the voltage regulation maintains its quality to the current limit and accordingly shows a very sharp "knee" (1% +1 mA, Figure 11). Note that the regulator can switch back into the constant voltage mode if the output voltage reaches a value greater than V_R . Operation through zero milliamperes is guaranteed by the inclusion of another emitter offsetting resistor.

FIGURE 11 - V_1 CURVE FOR 0-TO-40 V, 0.5-AMPERE REGULATOR



Transistor Q9 and five diodes comprise the essential parts of the output stage (Figure 12). The diodes perform an "OR" function which allows only one mode of operation at a time - constant current or constant voltage. However, an additional stage (Q9) must be included to invert the logic and make it compatible with the driving requirements of series pass transistors as well as provide additional gain. A 1.5 mA collector current source sets the maximum deliverable output current and boosts the output impedance to that of the current source.

Note that the negative (substrate) side of the MC1466 is 7.25 volts lower than the output voltage, and the reference regulator guarantees that the positive side is 11 volts above the output. Thus the IC remains at a voltage (relative to ground) solely dependent on the output, "floating" above and below V_O . VCE across Q9 is only two or three V_{BE} 's depending on the number of transistors used in the series pass configuration.

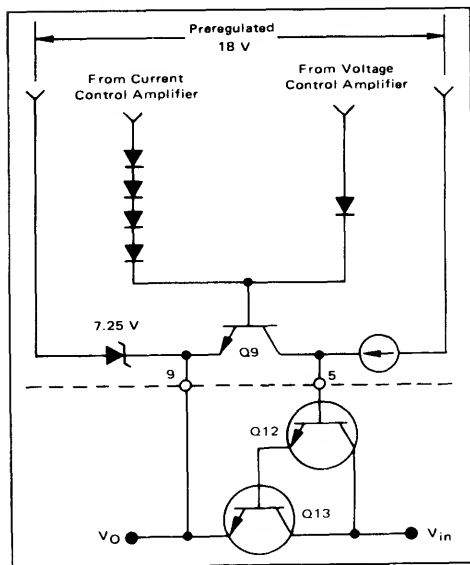
Performance characteristics of the regulator may be approximately calculated for a given circuit (Figure 2). Assuming that the two added transistors (Q12 and Q13) have minimum betas of 20, then the overall regulator transconductance will be:

$$gm_T = (400) 300 \text{ mA/volt} = 120 \text{ A/volt.} \quad (3)$$

For a change in current of 500 mA the output voltage will drop only:

$$\Delta V = \frac{0.5}{120} = 4.2 \text{ mV.} \quad (4)$$

FIGURE 12 — MC1466 OUTPUT STAGE



The analysis thus far does not consider changes in V_R due to output current changes. If I_L increases by 500 mA the collector current of Q9 decreases by 1.25 mA, causing the collector current of Q5 to increase by 30 μ A. Accordingly, I_R will be decreased by $\approx 0.30 \mu$ A which will drop the output by 0.03%. This figure may be improved considerably by either using high beta devices as the pass transistors, or by increasing I_R . Note again, however, that the maximum power rating of the package must be kept in mind. For example if $I_R = 4 \text{ mA}$, power dissipation is

$$P_D = 20 \text{ V} (8 \text{ mA}) + (11 \text{ V} \times 3 \text{ mA}) = 193 \text{ mW.} \quad (5)$$

This indicates that the circuit may be safely operated up to 118°C using 20 volts at the auxiliary supply voltage. If, however, the auxiliary supply voltage is 35 volts,

$$P_D = 35 \text{ V} (8 \text{ mA}) + 26 \text{ V} (3 \text{ mA}) = 358 \text{ mW.} \quad (6)$$

which dictates that the maximum operating temperature must be less than 91°C to keep package dissipation within specified limits.

Line voltage regulation is also a function of the voltage change between pins 8 and 9, and the change of V_{ref} . In this case, however, these voltages change due to changes in the internal regulator's voltages, which in turn are caused by changes in V_{aux} . Note that line voltage regulation is not a function of V_{in} . Note also that the instantaneous value of V_{aux} must always be between 20 and 35 volts.

Figure 6 shows six external diodes (CR1 to CR6) added for protective purposes. CR1 should be used if the output voltage is less than 20 volts and CR2, CR3 are absent. For V_O higher than 20 volts, CR1 should be discarded in favor of CR2 and CR3. Diode CR4 prevents IC failure if the series pass transistors develop collector-base shorts while the main power transistor suffers a simultaneous open emitter. If the possibility of such a transistor failure mode seems remote, CR4 may be deleted. To prevent instantaneous differential and common mode breakdown of the current sense amplifier, CR5 must be placed across the current limit resistor R_S .

Load transients occasionally produce a damaging reversal of current flow from output to input $V_O > 150$ volts (which will destroy the IC). Diode CR6 prevents such reversal and renders the circuit immune from destruction for such conditions, e.g., adding a large output capacitor after the supply is turned "on". Diodes CR1, CR2, CR3, and CR5 may be general purpose silicon units such as 1N4001 or equivalent whereas CR4 and CR6 should have a peak inverse voltage rating equal to V_{in} or greater.

APPLICATIONS

Figure 2 shows a typical 0-to-40 volts, 0.5-ampere regulator with better than 0.01% performance. The RC network between pins 5 and 6 and the capacitor between pins 13 and 14 provide frequency compensation for the MC1466. The external pass transistors are used to boost load current, since the output current of the regulator is less than 2 mA.

Figure 1 is a 0-to-15 volts, 10-ampere regulator with the pass transistor configuration necessary to boost the load current to 10 amperes. Note that C_O has been increased to 1000 μF following the general rule:

$$C_O = 100 \mu\text{F/A } I_L$$

The prime advantage of the MC1466 is its use as a high voltage regulator, as shown in Figure 3. This 0-to-250 volts 0.1-ampere regulator is typical of high voltage applications, limited only by the breakdown and safe areas of the output pass transistors.

The primary limiting factor in high voltage series regulators is the pass transistor. Figure 13 shows a safe area curve for the MJ413. Looking at Figure 3, we see that if the output is shorted, the transistor will have a collector current of 100 mA, with a V_{CE} approximately equal to 260 volts. Thus this point falls on the dc line of the safe area curve, insuring that the transistor will not enter secondary breakdown.

In this respect (Safe Operating Area) the foldback circuit of Figure 14 is superior for handling high voltages and yet is short-circuit protected. This is due to the fact that load current is diminished as output voltage drops (V_{CE} increases as V_O drops) as seen in Figure 15. By careful design the load current at a short, I_{SC} can be made low enough such that the combined V_{CE} (V_{in}) and I_{SC} still falls within the dc safe operating area of the transistor. For the illustrated design (Figure 14), an input voltage of 210 volts is com-

patible with a short circuit current of 100 mA. Yet current foldback allows us to design for a maximum regulated load current of 500 mA, the pertinent design equations are:

$$\text{Let } R_2 \text{ (k}\Omega\text{)} = V_O$$

$$\alpha = \frac{0.25}{V_O} \left[\frac{I_k}{I_{SC}} - 1 \right]$$

$$R_1 \text{ (k}\Omega\text{)} = \frac{\alpha}{1 - \alpha} V_O$$

$$R_{SC} = \frac{0.25}{(1 - \alpha) I_{SC}}$$

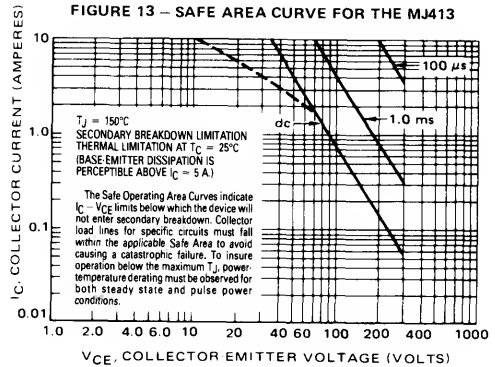
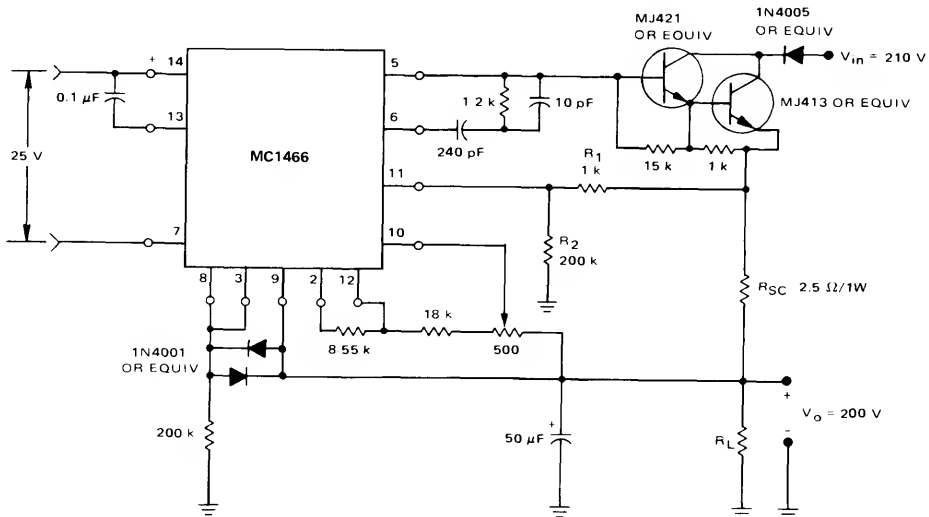


FIGURE 14 — A 200 V, 0.5-AMPERE REGULATOR WITH CURRENT FOLDBACK



The terms I_{SC} and I_k correspond to the short-circuit current and maximum available load current as shown in Figure 15.

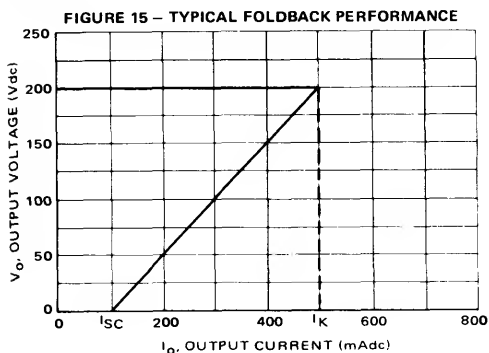


Figure 16 shows a remote sense application which should be used when high current or long wire lengths are used. This type of wiring is recommended for any application where the best possible regulation is desired. Since the sense lines draw only a small current, large voltage drops do not destroy the excellent regulation of the MC1466.

TRANSIENT FAILURES

In industrial areas where electrical machinery is used

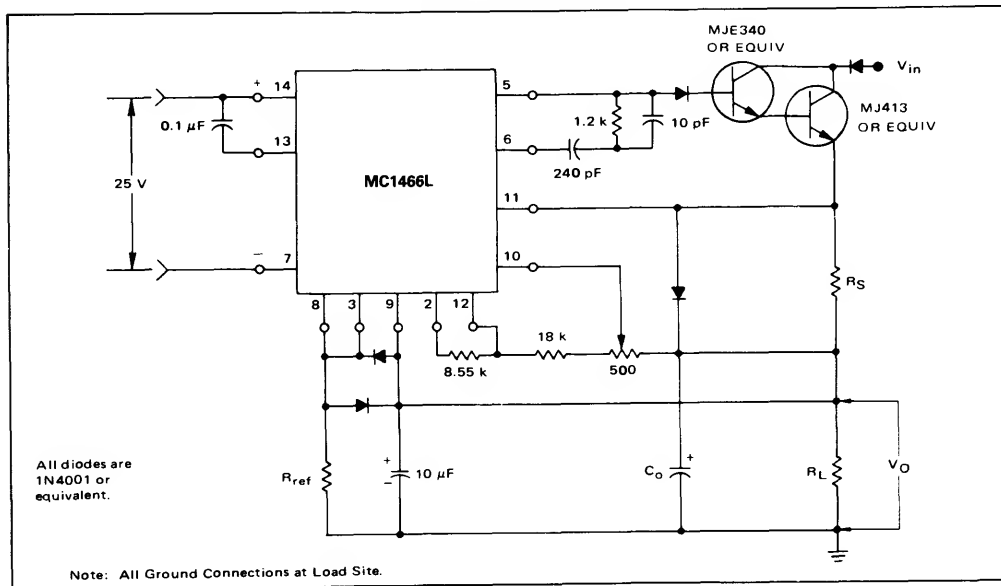
the normal ac line often contains bursts of voltage running from hundreds to thousands of volts in magnitude and only microseconds in duration. Under some conditions this energy is dissipated across the internal zener connected between pins 9 and 7. This transient condition may produce a total failure of the regulator device without any apparent explanation. This type of failure is identified by absence of the 7 volt zener (CR1) between pin 9 and pin 7. To prevent this failure mode the use of a shielded power transformer is recommended, as shown in Figure 6. In addition, it is recommended that C1, C3 and C4 be included to aid in transient repression. These capacitors should have good high frequency characteristics.

If the possibility of transients on the output exists, the addition of a resistor and zener diode between pins 9 and 7 as shown on Figure 17 should be added.

VOLTAGE/CURRENT MODE INDICATOR

There may be times when it is desirable to know when the MC1466 is in the constant current mode or constant voltage mode. A mode indicator signal circuit can be easily added to provide this feature. Figure 18 shows how a PNP transistor has replaced a protection diode between pins 8 and 9 of Figure 2. When the MC1466 goes from constant voltage mode to constant current mode, V_O will drop below V_g and the PNP transistor will turn on. The 1 mA current supplied by pin 8 will now be shunted to base of Q1 thereby providing a mode signal output.

FIGURE 16 – REMOTE SENSE

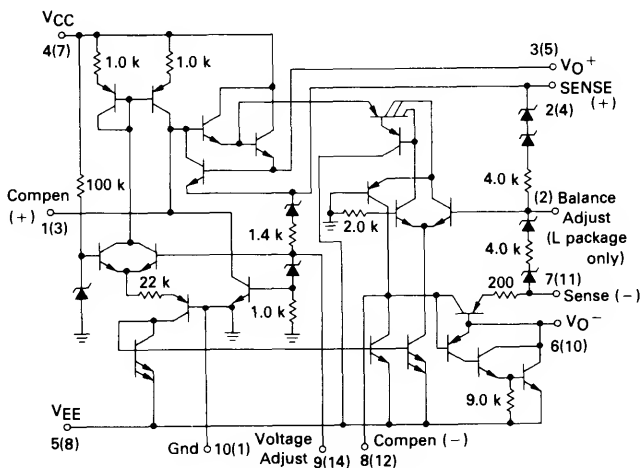


DUAL ± 15 VOLT TRACKING REGULATOR

The MC1468/MC1568 is a dual polarity tracking regulator designed to provide balanced positive and negative output voltages at currents to 100 mA. Internally, the device is set for ± 15 volt outputs but an external adjustment can be used to change both outputs simultaneously from 8.0 to 20 volts. Input voltages up to ± 30 volts can be used and there is provision for adjustable current limiting.

- Internally Set to ± 15 V Tracking Outputs
- Output Currents to 100 mA
- Outputs Balanced to within 1.0% (MC1568)
- Line and Load Regulation of 0.06%
- 1.0% Maximum Output Variation Due to Temperature Changes
- Standby Current Drain of 3.0 mA
- Externally Adjustable Current Limit
- Remote Sensing Provisions

CIRCUIT SCHEMATIC

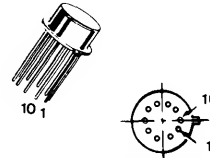


Pin numbers in parentheses are for the L suffix package.

MC1468
MC1568

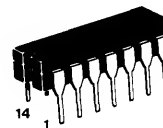
DUAL ± 15 VOLT TRACKING REGULATOR

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**



(Bottom View)

G SUFFIX
METAL PACKAGE
CASE 603C



L SUFFIX
CERAMIC PACKAGE
CASE 632

ORDERING INFORMATION

Device	Temperature Range	Package
MC1468G	0°C to +70°C	Metal Can
MC1468L	0°C to +70°C	Ceramic DIP
MC1568G	-55°C to +125°C	Metal Can
MC1568L	-55°C to +125°C	Ceramic DIP

MC1468, MC1568

MAXIMUM RATINGS (T_C = +25°C unless otherwise noted.)

Rating	Symbol	Value		Unit		
Input Voltage	V _{CC} , V _{EE}	30		Vdc		
Peak Load Current	I _{pk}	100		mA		
Power Dissipation and Thermal Characteristics		G Package	L Package			
		T _A = +25°C	P _D	0.83	1.25	Watts
		Derate above T _A = +25°C	1/θ _{JA}	6.6	10	mW/°C
		Thermal Resistance, Junction to Air	θ _{JA}	150	100	°C/W
		T _C = +25°C	P _D	1.8	2.5	Watts
		Derate above T _C = +25°C	1/θ _{JC}	14.3	20	mW/°C
		Thermal Resistance, Junction to Case	θ _{JC}	70	50	°C/W
		Storage Junction to Temperature Range	T _J , T _{stg}	- 65 to + 150		°C
Minimum Short-Circuit Resistance	R _{SC} (min)	4.0		Ohms		
Ambient Temperature	T _A			°C		
MC1468		0 to +70				
MC1568		- 55 to + 125				

ELECTRICAL CHARACTERISTICS (V_{CC} = +20 V, V_{EE} = -20 V, C₁ = C₂ = 1500 pF, C₃ = C₄ = 1.0 μF, R_{SC+} = R_{SC-} = 4.0 Ω, I_{L+} = I_{L-} = 0, T_C = +25°C unless otherwise noted, see Figure 1.)

Characteristic	Symbol	MC1568			MC1468			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage	V _O	±14.5	±15	±15.5	±14.5	±15	±15.5	Vdc
Input Voltage	V _{in}	—	—	±30	—	—	±30	Vdc
Input-Output Voltage Differential	V _{in} -V _O	2.0	—	—	2.0	—	—	Vdc
Output Voltage Balance (L package only)	V _{Bal}	—	±50	±150	—	±50	±300	mV
Line Regulation Voltage (V _{in} = 18 V to 30 V) T _{low} (Note 1) to T _{high} (Note 2)	Reg _{line}	—	—	10 20	—	—	10 20	mV
Load Regulation Voltage (I _L = 0 to 50 mA, T _J = constant) (T _A = T _{low} to T _{high})	Reg _{load}	—	—	10 30	—	—	10 30	mV
Output Voltage Range L Package (See Figure 4) G Package (See Figures 2 and 13)	V _{OR}	±8.0 ±14.5	—	±20 ±20	±8.0 ±14.5	—	±20 ±20	Vdc
Ripple Rejection (f = 120 Hz)	RR	—	75	—	—	75	—	dB
Output Voltage Temperature Stability (T _{low} to T _{high})	TS _{VO}	—	0.3	1.0	—	0.3	1.0	%
Short-Circuit Current Limit (R _{SC} = 10 ohms)	I _{SC}	—	60	—	—	60	—	mA
Output Noise Voltage (BW = 100 Hz-10 kHz)	V _n	—	100	—	—	100	—	μV(RMS)
Positive Standby Current (V _{in} = +30 V)	I _{B+}	—	2.4	4.0	—	2.4	4.0	mA
Negative Standby Current (V _{in} = -30 V)	I _{B-}	—	1.0	3.0	—	1.0	3.0	mA
Long-Term Stability	ΔV _O /Δt	—	0.2	—	—	0.2	—	%/k Hr

NOTES:

1. T_{low} = 0°C for MC1468
= -55°C for MC1568
2. T_{high} = +70°C for MC1468
= +125°C for MC1568

MC1468, MC1568

TYPICAL APPLICATIONS

FIGURE 1 — BASIC 50-mA REGULATOR

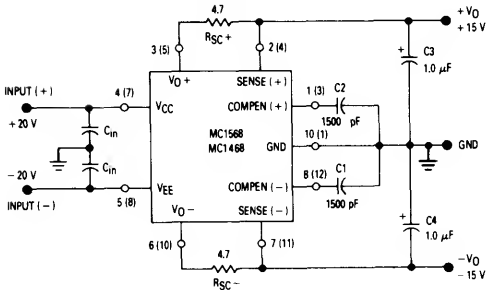
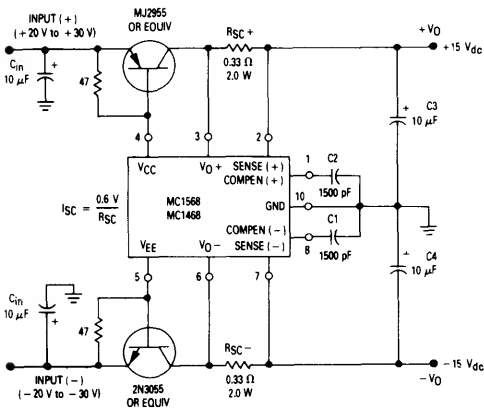


FIGURE 3 — ± 1.5 AMPERE REGULATOR
(Short-Circuit Protected, with Proper Heatsinking)

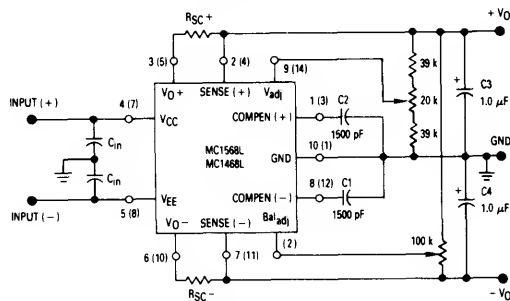


APPLICATIONS INFORMATION

Compensation capacitors C1 and C2 must be located as close to the device as possible to prevent instability due to noise pickup. Input bypass capacitors C_{in} are required if the device is located more than four inches from the power source filter capacitor. Output capacitor C4 is required for stability of the negative regulator. Capacitor C3 is used to improve the positive regulator load transient response. Low impedance quality capacitors are required when operating the MC1568 at its temperature extremes. Extended range ceramic, tantalum, and electrolytic capacitors are readily available from several manufacturers.

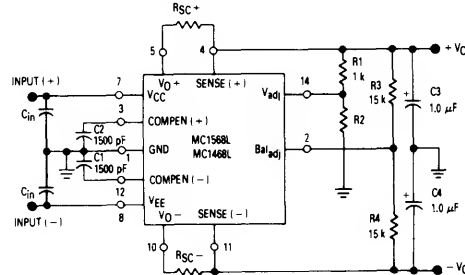
Capacitor values should be determined on a system by system basis. Input lead length, output load, temperature range, and printed circuit board layout are factors that will influence circuit performance. Typical values for capacitors C_{in} , C3, and C4 are 0.1 μ F to 10 μ F while C1 and C2 are 1500 pF.

FIGURE 2 — VOLTAGE ADJUST AND
BALANCE ADJUST CIRCUIT
($14.5 \text{ V} \leq V_{out} \leq 20 \text{ V}$)



Balance adjust available in MC1568L, MC1468L ceramic dual-in-line package only.

FIGURE 4 — OUTPUT VOLTAGE ADJUSTMENT
FOR $8.0 \text{ V} \leq |\pm V_O| \leq 14.5 \text{ V}$
(Ceramic-Packaged Devices Only)



The presence of Baladj, pin 2, on devices housed in the dual in-line package (L suffix) allows the user to adjust the output voltages down to $\pm 8.0 \text{ V}$. The required value of resistor R2 can be calculated from

$$R2 = \frac{R1 R_{int} (\phi + V_z)}{R_{int} (V_O - \phi - V_z) - \phi R1}$$

Where: R_{int} = An Internal Resistor = $R1 = 1.0 \text{ k}\Omega$
 $\phi = 0.68 \text{ V}$
 $V_z = 6.6 \text{ V}$

Some common design values are listed below:

$\pm V_O (\text{V})$	R2	$T_C V_O (\% / ^\circ \text{C})$	$I_g (\text{mA})$
14	1.2 k	0.003	10
12	1.8 k	0.022	7.2
10	3.5 k	0.025	5.0
8.0	∞	0.028	2.6

MC1468, MC1568

TYPICAL CHARACTERISTICS

($V_{CC} = +20\text{ V}$, $V_{EE} = -20\text{ V}$, $V_O = \pm 15\text{ V}$, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 5 — LOAD REGULATION

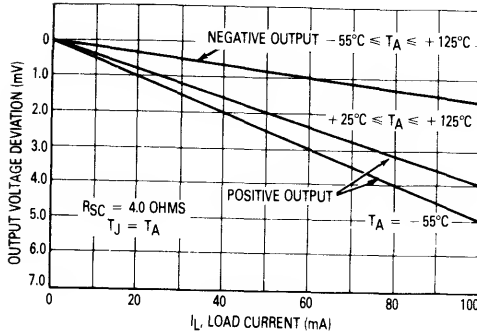


FIGURE 6 — REGULATOR DROPOUT VOLTAGE

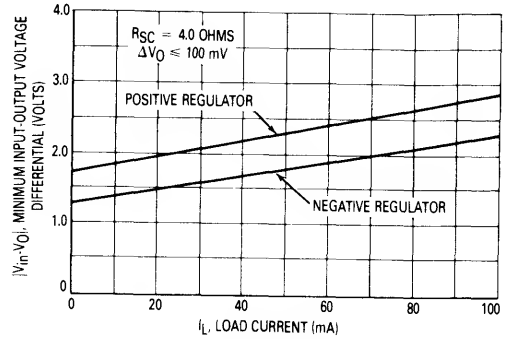


FIGURE 7 — MAXIMUM CURRENT CAPABILITY

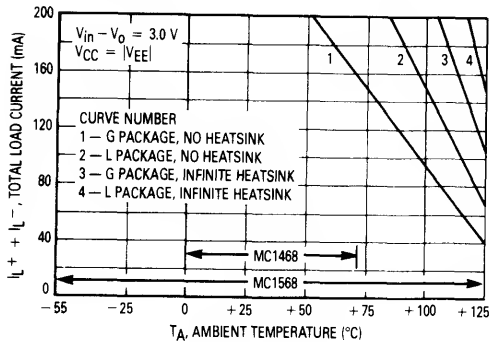


FIGURE 8 — MAXIMUM CURRENT CAPABILITY

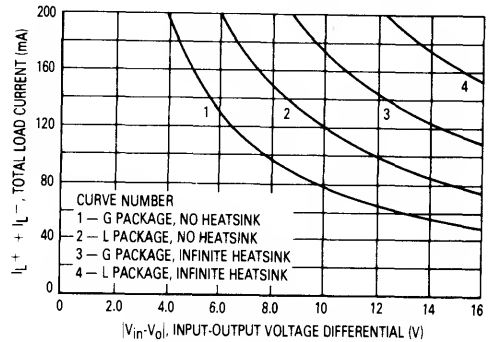


FIGURE 9 — I_{SC} versus R_{SC}

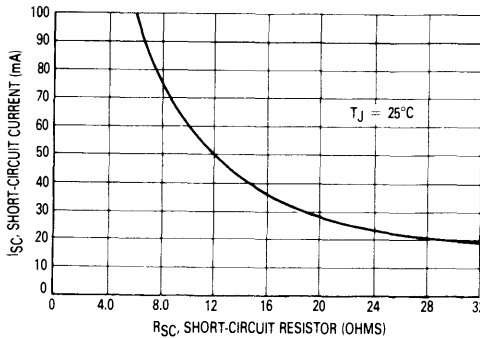
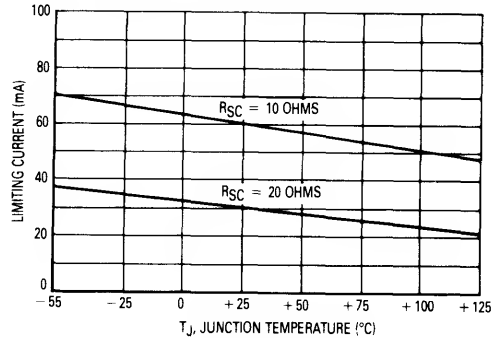


FIGURE 10 — CURRENT-LIMITING CHARACTERISTICS



MC1468, MC1568

TYPICAL CHARACTERISTICS (continued)

($V_{CC} = +20\text{ V}$, $V_{EE} = -20\text{ V}$, $V_O = \pm 15\text{ V}$, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 11 — STANDBY CURRENT DRAIN

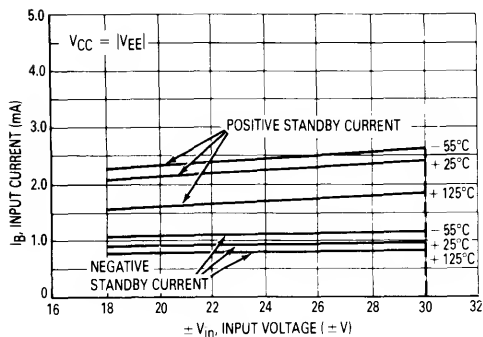


FIGURE 12 — STANDBY CURRENT DRAIN

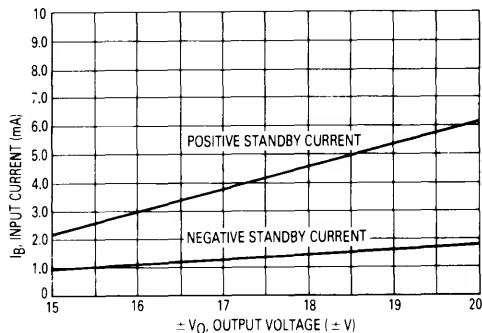


FIGURE 13 — TEMPERATURE COEFFICIENT OF OUTPUT VOLTAGE

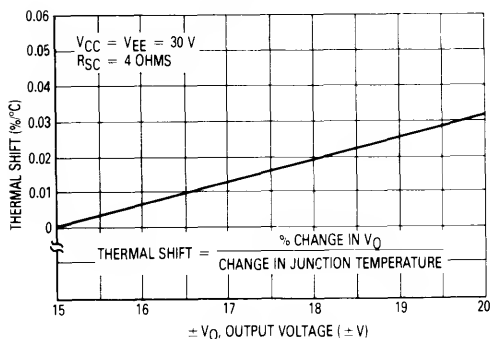


FIGURE 14 — LOAD TRANSIENT RESPONSE

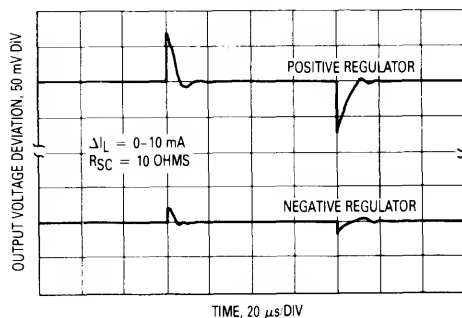


FIGURE 15 — LINE TRANSIENT RESPONSE

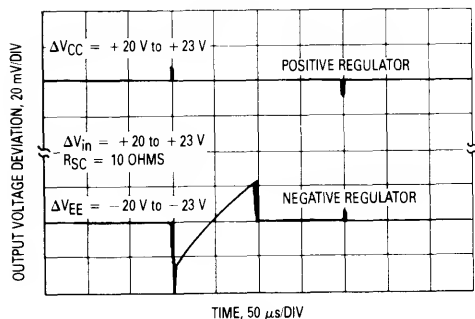
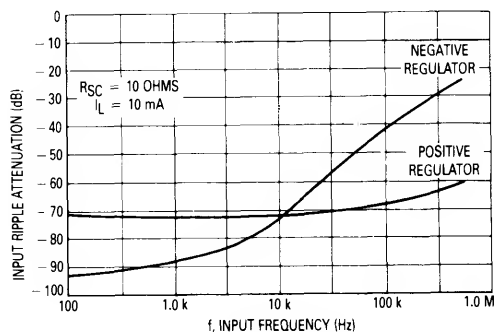


FIGURE 16 — RIPPLE REJECTION

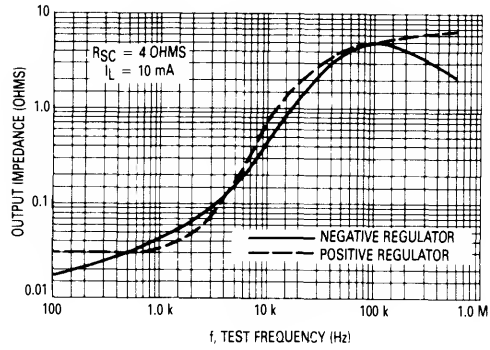


MC1468, MC1568

TYPICAL CHARACTERISTICS (continued)

($V_{CC} = +20\text{ V}$, $V_{EE} = -20\text{ V}$, $V_O = \pm 15\text{ V}$, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 17 — OUTPUT IMPEDANCE



ORDERING INFORMATION

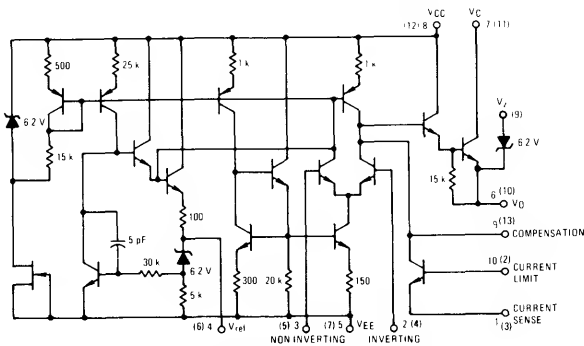
Device	Alternate	Temperature Range	Package
MC1723CD MC1723CG	LM723CH, $\mu A723HC$	0°C to +70°C	SO-14 Metal Can
MC1723CL	LM723CJ, $\mu A723DC$		Ceramic DIP
MC1723CP	LM723CN, $\mu A723PC$		Plastic DIP
MC1723G MC1723L		-55°C to +125°C	Metal Can Ceramic DIP

VOLTAGE REGULATOR

The MC1723 is a positive or negative voltage regulator designed to deliver load current to 150 mAdc. Output current capability can be increased to several amperes through use of one or more external pass transistors. MC1723 is specified for operation over the military temperature range (-55°C to +125°C) and the MC1723C over the commercial temperature range (0 to +70°C)

- Output Voltage Adjustable from 2 Vdc to 37 Vdc
- Output Current to 150 mAdc Without External Pass Transistors
- 0.01% Line and 0.03% Load Regulation
- Adjustable Short-Circuit Protection

FIGURE 1 - CIRCUIT SCHEMATIC



PIN NUMBERS ADJACENT TO TERMINALS ARE FOR THE METAL PACKAGE
PIN NUMBERS IN PARENTHESIS ARE FOR DUAL IN LINE PACKAGES

FIGURE 2 - TYPICAL CIRCUIT CONNECTION

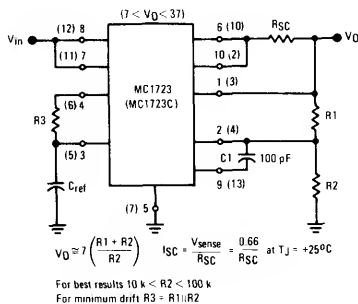
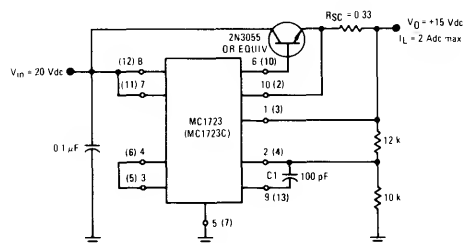


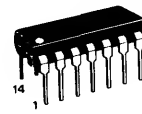
FIGURE 3 - TYPICAL NPN CURRENT BOOST CONNECTION



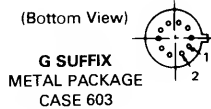
MC1723
MC1723C

VOLTAGE REGULATOR

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**



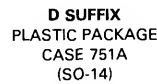
**P SUFFIX
PLASTIC PACKAGE
CASE 646**



**G SUFFIX
METAL PACKAGE
CASE 603**



**L SUFFIX
CERAMIC PACKAGE
CASE 632**



**D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)**

MC1723, MC1723C

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Pulse Voltage from V _{CC} to V _{EE} (50 ms)	V _{in(p)}	50	V _{peak}
Continuous Voltage from V _{CC} to V _{EE}	V _{in}	40	V _{dc}
Input-Output Voltage Differential	V _{in} - V _O	40	V _{dc}
Maximum Output Current	I _L	150	mAdc
Current from V _{ref}	I _{ref}	15	mAdc
Current from V _z	I _z	25	mA
Voltage Between Non-Inverting Input and V _{EE}	V _{ie}	8.0	V _{dc}
Differential Input Voltage	V _{id}	±5.0	V _{dc}
Power Dissipation and Thermal Characteristics			
Plastic Package			
T _A = +25°C	P _D	1.25	W
Derate above T _A = +25°C	1/θ _{JA}	10	mW/°C
Thermal Resistance, Junction to Air	θ _{JA}	100	°C/W
Metal Package			
T _A = +25°C	P _D	1.0	Watt
Derate above T _A = +25°C	1/θ _{JA}	6.6	mW/°C
Thermal Resistance, Junction to Air	θ _{JA}	150	°C/W
T _C = +25°C	P _D	2.1	Watts
Derate above T _A = +25°C	1/θ _{JA}	14	mW/°C
Thermal Resistance, Junction to Case	θ _{JC}	35	°C/W
Dual In-Line Ceramic Package			
Derate above T _A = +25°C	P _D	1.5	Watt
Thermal Resistance, Junction to Air	1/θ _{JA}	10	mW/°C
Thermal Resistance, Junction to Air	θ _{JA}	100	°C/W
Operating and Storage Junction Temperature Range			
Metal Package			
Dual In-Line Ceramic			
Operating Ambient Temperature Range			
MC1723C			
MC1723			
T _J , T _{stg}			
-65 to +150			
-65 to +175			
°C			
T _A			
0 to +70			
-55 to +125			
°C			

ELECTRICAL CHARACTERISTICS (Unless otherwise noted: T_A = +25°C, V_{in} 12 Vdc, V_O = 5.0 Vdc, I_L = 1.0 mAdc, R_{SC} = 0, C₁ = 100 pF, C_{ref} = 0 and divider impedance as seen by the error amplifier ≤ 10 kΩ connected as shown in Figure 2)

Characteristic	Symbol	MC1723			MC1723C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Voltage Range	V _{in}	9.5	—	40	9.5	—	40	V _{dc}
Output Voltage Range	V _O	2.0	—	37	2.0	—	37	V _{dc}
Input-Output Voltage Differential	V _{in} - V _O	3.0	—	38	3.0	—	38	V _{dc}
Reference Voltage	V _{ref}	6.95	7.15	7.35	6.80	7.15	7.50	V _{dc}
Standby Current Drain (I _L = 0, V _{in} = 30 V)	I _{IB}	—	2.3	3.5	—	2.3	4.0	mAdc
Output Noise Voltage (f = 100 Hz to 10 kHz)	V _n	—	—	—	—	—	—	μV(RMS)
C _{ref} = 0		—	20	—	—	20	—	
C _{ref} = 5.0 μF		—	2.5	—	—	2.5	—	
Average Temperature Coefficient of Output Voltage (T _{low} ① < T _A < T _{high} ②)	TCV _O	—	0.002	0.015	—	0.003	0.015	%/°C
Line Regulation	Reg _{line}	—	—	—	—	—	—	%V _O
(T _A = +25°C) { 12 V < V _{in} < 15 V		—	0.01	0.1	—	0.01	0.1	
(T _{low} ① < T _A < T _{high} ②) { 12 V < V _{in} < 40 V		—	0.02	0.2	—	0.1	0.5	
12 V < V _{in} < 15 V		—	—	0.3	—	—	0.3	
Load Regulation (1.0 mA < I _L < 50 mA)	Reg _{load}	—	—	—	—	—	—	%V _O
T _A = +25°C		—	0.03	0.15	—	0.03	0.2	
T _{low} ① < T _A < T _{high} ②		—	—	0.6	—	—	0.6	
Ripple Rejection (f = 50 Hz to 10 kHz)	RR	—	74	—	—	74	—	dB
C _{ref} = 0		—	86	—	—	86	—	
C _{ref} = 5.0 μF		—	—	—	—	—	—	
Short Circuit Current Limit (R _{SC} = 10 Ω, V _O = 0)	I _{sc}	—	65	—	—	65	—	mAdc
Long Term Stability	ΔV _O /Δt	—	0.1	—	—	0.1	—	%/1000 Hr

① T_{low} = 0°C for MC1723C
= -55°C for MC1723

② T_{high} = +70°C for MC1723C
= +125°C for MC1723

MC1723, MC1723C

TYPICAL CHARACTERISTICS

($V_{in} = 12 \text{ Vdc}$, $V_O = 5.0 \text{ Vdc}$, $I_L = 1.0 \text{ mAdc}$, $R_{SC} = 0$, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 4 – MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

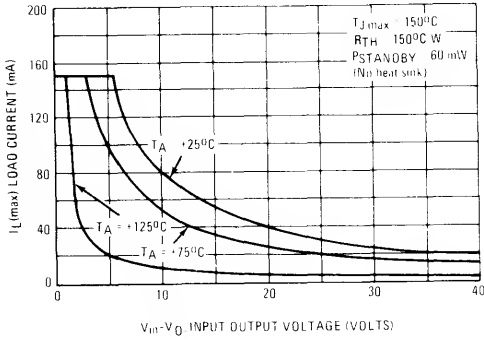


FIGURE 6 – LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING

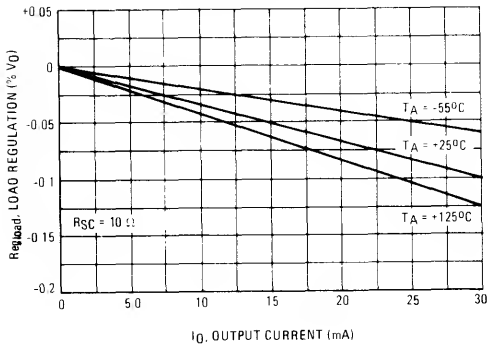


FIGURE 8 – CURRENT LIMITING CHARACTERISTICS

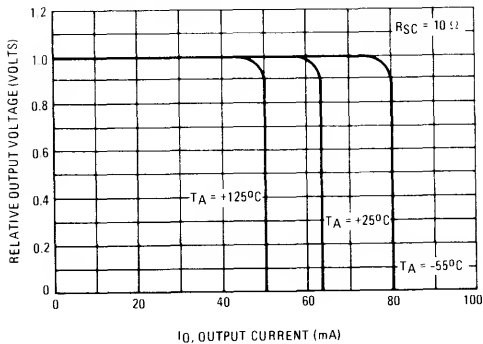


FIGURE 5 – LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING

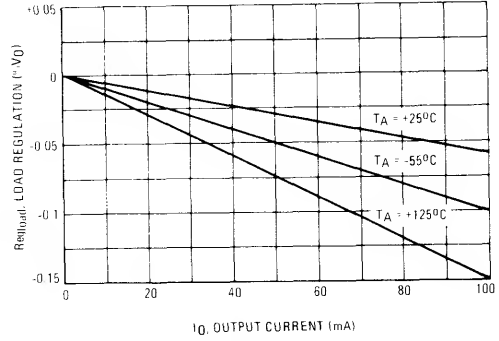


FIGURE 7 – LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING

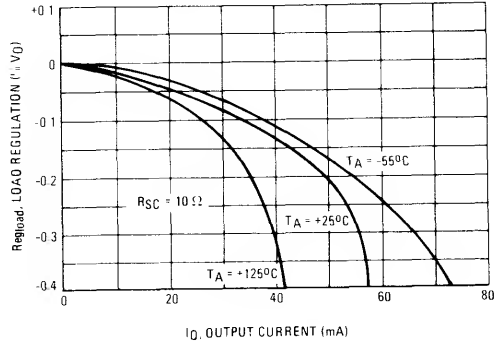
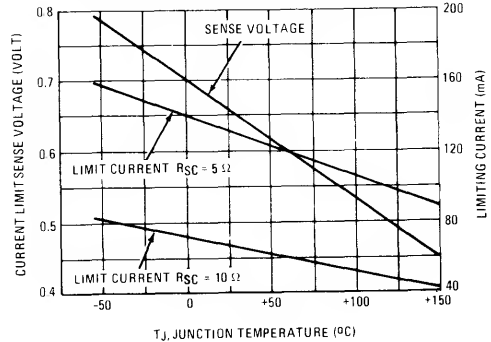


FIGURE 9 – CURRENT LIMITING CHARACTERISTICS AS A FUNCTION OF JUNCTION TEMPERATURE



MC1723, MC1723C

TYPICAL CHARACTERISTICS (continued)

FIGURE 10 – LINE REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

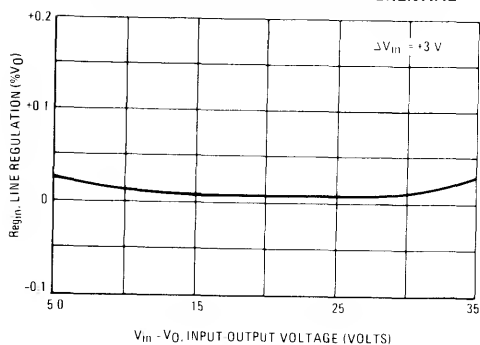


FIGURE 11 – LOAD REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

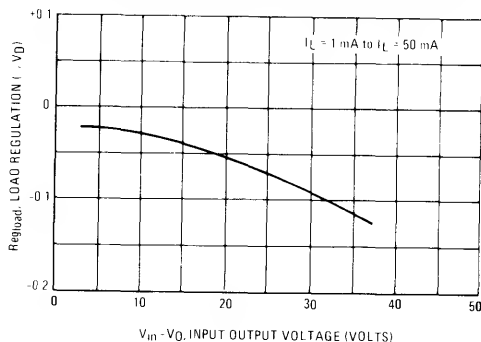


FIGURE 12 – STANDBY CURRENT DRAIN AS A FUNCTION OF INPUT VOLTAGE

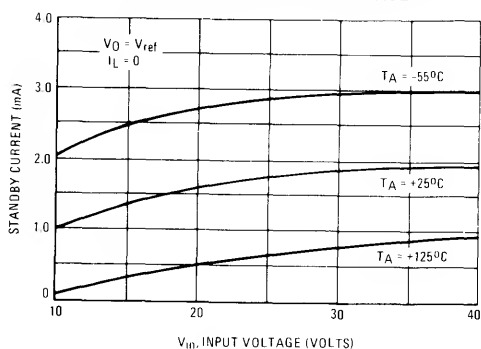


FIGURE 13 – LINE TRANSIENT RESPONSE

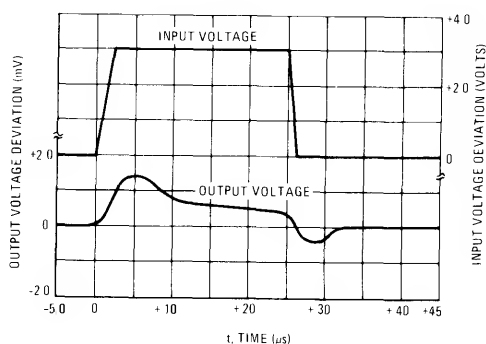


FIGURE 14 – LOAD TRANSIENT RESPONSE

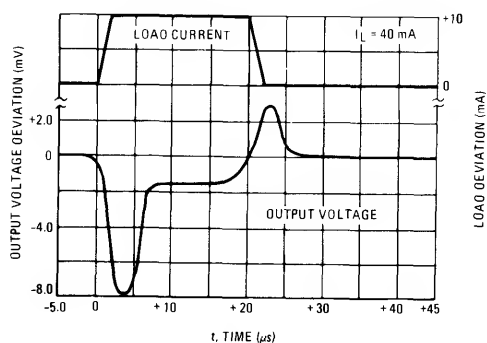
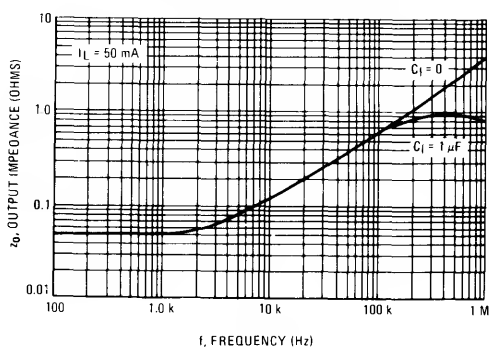


FIGURE 15 – OUTPUT IMPEDANCE AS FUNCTION OF FREQUENCY



MC1723, MC1723C

TYPICAL APPLICATIONS

Pin numbers adjacent to terminals are for the metal package;
pin numbers in parenthesis are for the dual in-line packages.

FIGURE 16 – TYPICAL CONNECTION FOR $2 < V_O < 7$

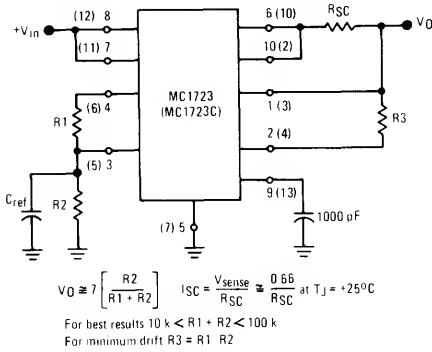


FIGURE 17 – MC1723,C FOLDBACK CONNECTION

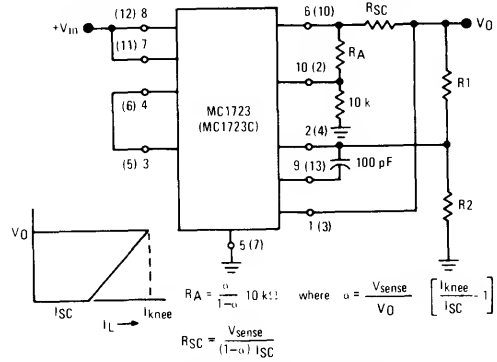


FIGURE 18 – +5 V, 1-AMPERE SWITCHING REGULATOR

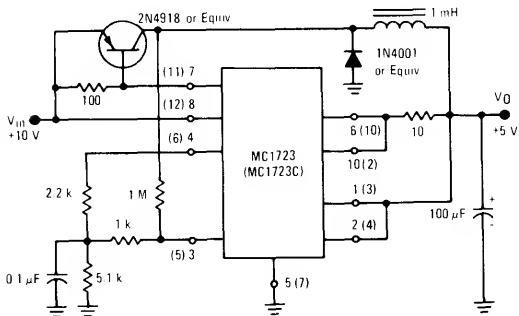


FIGURE 19 – +5 V, 1-AMPERE HIGH EFFICIENCY REGULATOR

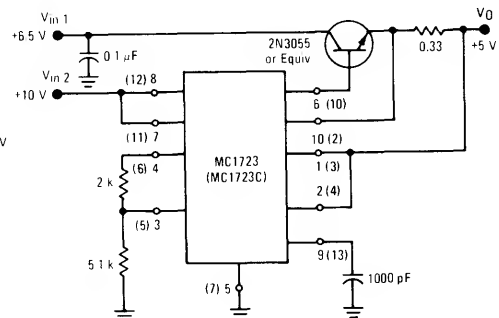


FIGURE 20 – +15 V, 1-AMPERE REGULATOR WITH REMOTE SENSE

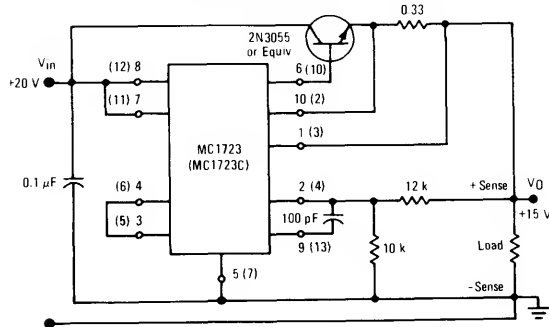
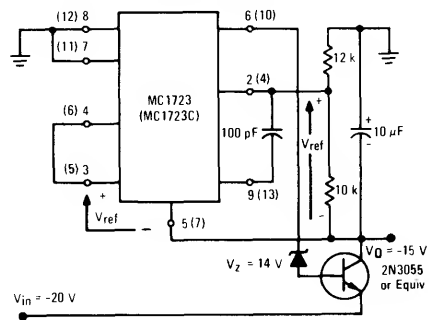


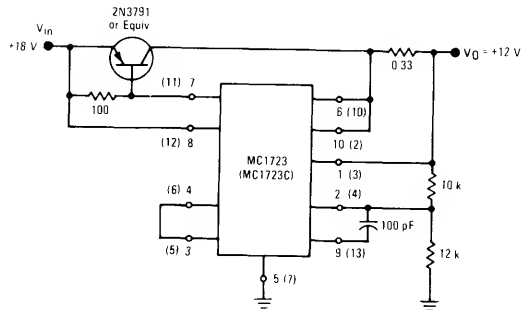
FIGURE 21 – -15 V NEGATIVE REGULATOR



MC1723, MC1723C

TYPICAL APPLICATIONS (continued)

FIGURE 22 — +12 V, 1-AMPERE REGULATOR
USING PNP CURRENT BOOST



MC3423
MC3523

OVERVOLTAGE
SENSING CIRCUIT

SILICON MONOLITHIC
INTEGRATED CIRCUIT

OVERVOLTAGE "CROWBAR" SENSING CIRCUIT

These overvoltage protection circuits (OVP) protect sensitive electronic circuitry from overvoltage transients or regulator failures when used in conjunction with an external "crowbar" SCR. They sense the overvoltage condition and quickly "crowbar" or short circuit the supply, forcing the supply into current limiting or opening the fuse or circuit breaker.

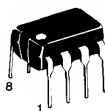
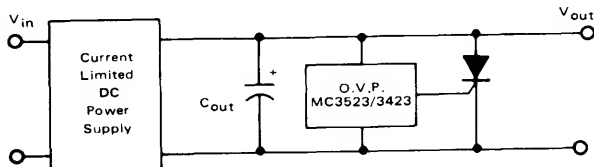
The protection voltage threshold is adjustable and the MC3423/3523 can be programmed for minimum duration of overvoltage condition before tripping, thus supplying noise immunity.

The MC3423/3523 is essentially a "two terminal" system, therefore it can be used with either positive or negative supplies.

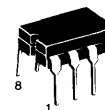
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Differential Power Supply Voltage	$V_{CC-V_{EE}}$	40	Vdc
Sense Voltage (1)	$V_{Sense\ 1}$	6.5	Vdc
Sense Voltage (2)	$V_{Sense\ 2}$	6.5	Vdc
Remote Activation Input Voltage	V_{act}	7.0	Vdc
Output Current	I_O	300	mA
Operating Ambient Temperature Range MC3423 MC3523	T_A	0 to +70 -55 to +125	°C
Operating Junction Temperature Plastic Package Ceramic Package	T_J	125 150	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TYPICAL APPLICATION



P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MC3423 only)

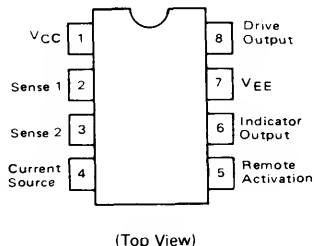


U SUFFIX
CERAMIC PACKAGE
CASE 693



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SOP-8)

PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
MC3423D	0 to +70°C	SO-8
MC3423P1		Plastic DIP
MC3423U		Ceramic DIP
MC3523U	-55 to +125°C	Ceramic DIP

MC3423, MC3523

ELECTRICAL CHARACTERISTICS (5 V ≤ V_{CC} - V_{EE} ≤ 36 V, T_{low} < T_A < T_{high} unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage Range	V _{CC} -V _{EE}	4.5	—	40	V _{dc}
Output Voltage (I _O = 100 mA)	V _O	V _{CC} -2.2	V _{CC} -1.8	—	V _{dc}
Indicator Output Voltage (I _O (Ind) = 1.6 mA)	V _{OL} (Ind)	—	0.1	0.4	V _{dc}
Sense Trip Voltage (T _A = 25°C)	V _{Sense 1} , V _{Sense 2}	2.45	2.6	2.75	V _{dc}
Temperature Coefficient of V _{Sense 1} (Figure 2)	TCV _{S1}	—	0.06	—	%/°C
Remote Activation Input Current (V _{IH} = 2.0 V, V _{CC} -V _{EE} = 5.0 V) (V _{IL} = 0.8 V, V _{CC} -V _{EE} = 5.0 V)	I _{IH} I _{IL}	— —	5.0 -120	40 -180	μA
Source Current	I _{Source}	0.1	0.2	0.3	mA
Output Current Risetime (T _A = 25°C)	t _r	—	400	—	mA/μs
Propagation Delay Time (T _A = 25°C)	t _{pd}	—	0.5	—	μs
Supply Current MC3423 MC3523	I _D	— —	6.0 5.0	10 7.0	mA

T_{low} = -55°C for MC3523
= 0°C for MC3423

T_{high} = +125°C for MC3523
= +70°C for MC3423

FIGURE 1 - BLOCK DIAGRAM

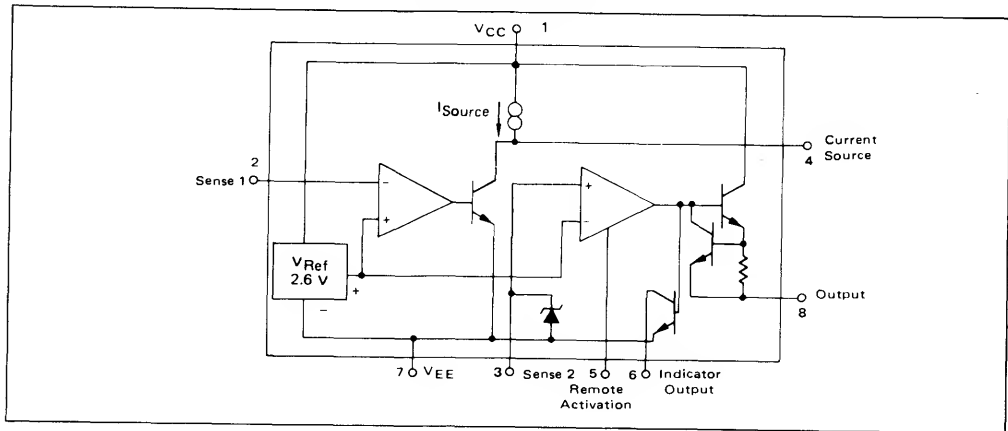
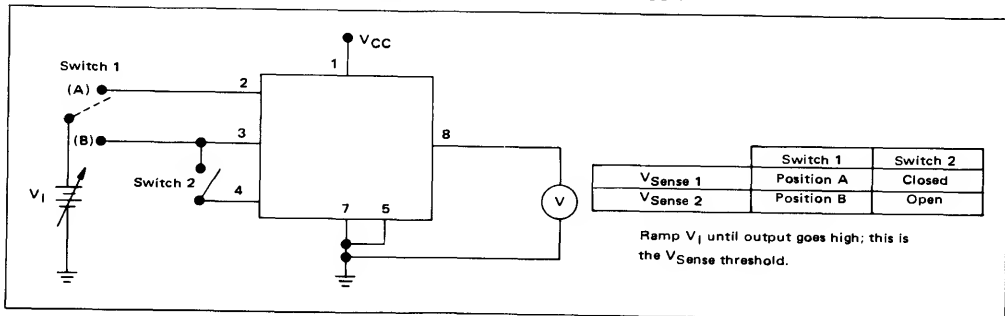


FIGURE 2 - SENSE VOLTAGE TEST CIRCUIT



APPLICATIONS INFORMATION

BASIC CIRCUIT CONFIGURATION

The basic circuit configuration of the MC3423/3523 OVP is shown in Figure 3 for supply voltages from 4.5 V to 36 V, and in Figure 4 for trip voltages above 36 V. The threshold or trip voltage at which the MC3423/3523 will trigger and supply gate drive to the crowbar SCR, Q1, is determined by the selection of R1 and R2. Their values can be determined by the equation given in Figures 3 and 4, or by the graph shown in Figure 8. The minimum value of the gate current limiting resistor, R_G , is given in Figure 9. Using this value of R_G , the SCR, Q1, will receive the greatest gate current possible without damaging the MC3423/3523. If lower output currents are required, R_G can be increased in value. The switch, S1, shown in Figure 3 may be used to reset the SCR crowbar. Otherwise, the power supply, across which the SCR is connected, must be shut down to reset the crowbar. If a non current-limited supply is used, a fuse or circuit breaker, F1, should be used to protect the SCR and/or the load.

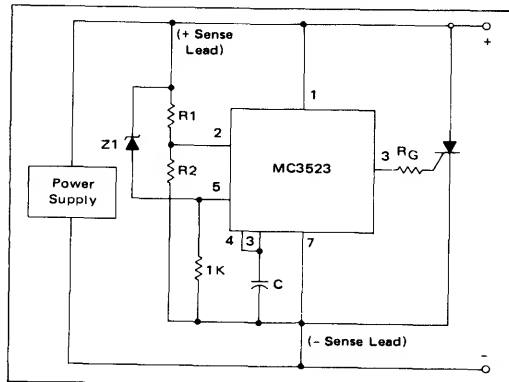
The circuit configurations shown in Figures 3 and 4 will have a typical propagation delay of 1.0 μ s. If faster operation is desired, pin 3 may be connected to pin 2 with pin 4 left floating. This will result in decreasing the propagation delay to approximately 0.5 μ s at the expense of a slightly increased TC for the trip voltage value.

CONFIGURATION FOR PROGRAMMABLE MINIMUM DURATION OF OVERVOLTAGE CONDITION BEFORE TRIPPING

In many instances, the MC3423/3523 OVP will be used in a noise environment. To prevent false tripping of the OVP circuit by noise which would not normally harm the load, MC3423/3523 has a programmable delay feature. To implement this feature, the circuit configuration of Figure 5 is used. In this configuration, a capacitor is connected from pin 3 to V_{EE} . The value of this capacitor determines the minimum duration of the overvoltage condition which is necessary to trip the OVP. The value of C can be found from Figure 10. The circuit operates in the following manner: When V_{CC} rises above the trip point set by R1 and R2, an internal current source (pin 4) begins charging the capacitor, C, connected to pin 3. If the overvoltage condition disappears before this occurs, the capacitor is discharged at a rate ≈ 10 times faster than the charging rate, resetting the timing feature until the next overvoltage condition occurs.

Occasionally, it is desired that immediate crowbarring of the supply occur when a high overvoltage condition occurs, while retaining the false tripping immunity of Figure 5. In this case, the circuit of Figure 6 can be used. The circuit will operate as previously described for small overvoltages, but will immediately trip if the power supply voltage exceeds $V_{Z1} + 1.4$ V.

FIGURE 6 — CONFIGURATION FOR PROGRAMMABLE DURATION OF OVERVOLTAGE CONDITION BEFORE TRIP/WITH IMMEDIATE TRIP AT HIGH OVERVOLTAGES



ADDITIONAL FEATURES

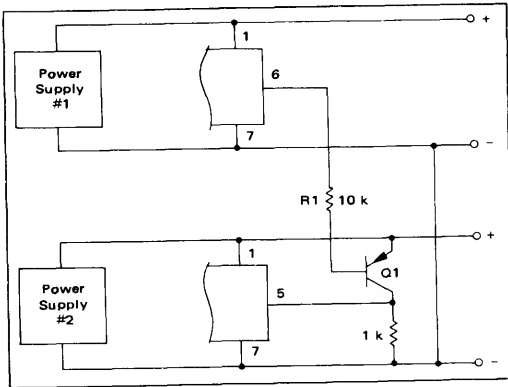
1. Activation Indication Output

An additional output for use as an indicator of OVP activation is provided by the MC3423/3523. This output is an open collector transistor which saturates when the OVP is activated. In addition, it can be used to clock an edge triggered flip-flop whose output inhibits or shuts down the power supply when the OVP trips. This reduces or eliminates the heatsinking requirements for the crowbar SCR.

2. Remote Activation Input

Another feature of the MC3423/3523 is its remote activation input, pin 5. If the voltage on this CMOS/TTL compatible input is held below 0.8 V, the MC3423/3523 operates normally. However, if it is raised to a voltage above 2.0 V, the OVP output is activated independent of whether or not an overvoltage condition is present. It should be noted that pin 5 has an internal pull-up current source. This feature can be used to accomplish an orderly and sequenced shut-down of system power supplies during a system fault condition. In addition, the activation indication output of one MC3423/3523 can be used to activate another MC3423/3523 if a single transistor inverter is used to interface the former's indication output to the latter's remote activation input, as shown in Figure 7. In this circuit, the indication output (pin 6) of the MC3423 on power supply 1 is used to activate the MC3423 associated with power supply 2. Q1 is any small PNP with adequate voltage rating.

FIGURE 7 – CIRCUIT CONFIGURATION FOR
ACTIVATING ONE MC3523 FROM ANOTHER



Note that both supplies have their negative output leads tied together (i.e., both are positive supplies). If their positive leads are common (two negative supplies) the emitter of Q1 would be moved to the positive lead of supply 1 and R1 would therefore have to be resized to deliver the appropriate drive to Q1.

CROWBAR SCR CONSIDERATIONS

Referring to Figure 11, it can be seen that the crowbar SCR, when activated, is subject to a large current surge from the output capacitance, C_{out} . This capacitance consists of the power supply output caps, the load's decoupling caps, and in the case of Figure 11A, the supply's input filter caps. This surge current is illustrated in Figure 12, and can cause SCR failure or degradation by any one of three mechanisms: di/dt , absolute peak surge, or I^2t . The interrelationship of these failure methods and the breadth of the applications make specification of the SCR by the semiconductor manufacturer difficult and expensive. Therefore, the designer must empirically determine the SCR and circuit elements which result in reliable and effective OVP operation. However, an understanding of the factors which influence the SCR's di/dt and surge capabilities simplifies this task.

1. di/dt

As the gate region of the SCR is driven on, its area of conduction takes a finite amount of time to grow, starting as a very small region and gradually spreading. Since the anode current flows through this turned-on gate region, very high current densities can occur in the gate region if high anode currents appear quickly (di/dt). This can result in immediate destruction of the SCR or gradual degradation of its forward blocking voltage capabilities — depending on the severity of the occasion.

FIGURE 8 – R1 versus TRIP VOLTAGE

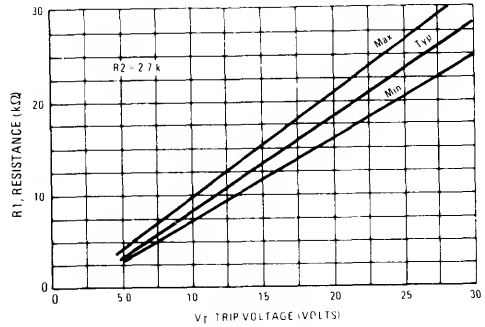


FIGURE 9 – MINIMUM R_G versus SUPPLY VOLTAGE

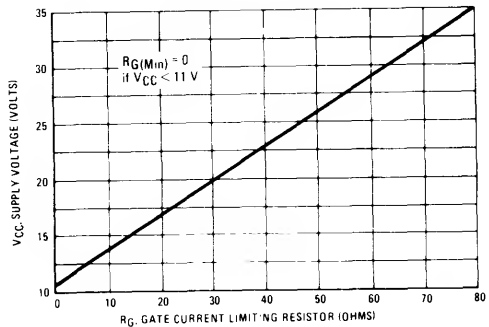


FIGURE 10 – CAPACITANCE versus
MINIMUM OVERVOLTAGE DURATION

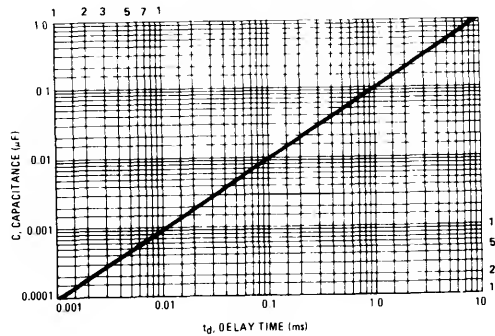


FIGURE 11 – TYPICAL CROWBAR OVP CIRCUIT CONFIGURATIONS

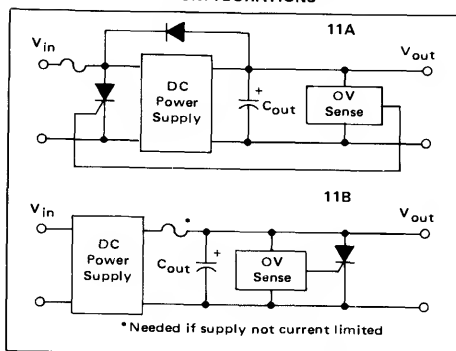


FIGURE 12 – CROWBAR SCR SURGE CURRENT WAVEFORM

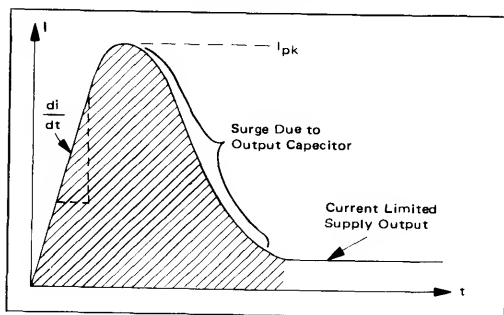
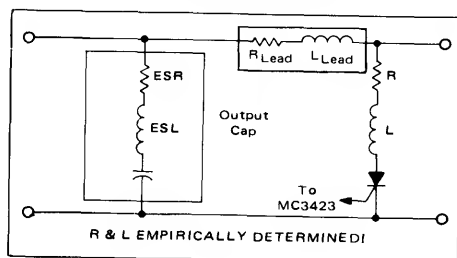


FIGURE 13 – CIRCUIT ELEMENTS AFFECTING SCR SURGE & di/dt



The usual design compromise then is to use a garden variety fuse (3AG or 3AB style) which cannot be relied on to blow before the thyristor does, and trust that if the SCR does fail, it will fail short circuit. In the majority of the designs, this will be the case, though this is difficult to guarantee. Of course, a sufficiently high surge will cause an open. These comments also apply to the fuse in Figure 11B.

For a complete and detailed treatment of SCR and fuse selection, refer to Motorola Application Note AN-789.

The value of di/dt that an SCR can safely handle is influenced by its construction and the characteristics of the gate drive signal. A center-gate-fire SCR has more di/dt capability than a corner-gate-fire type, and heavily overdriving (3 to 5 times I_{GT}) the SCR gate with a fast $< 1.0 \mu s$ rise time signal will maximize its di/dt capability. A typical maximum number in phase control SCRs of less than 50 A(RMS) rating might be 200 A/ μs , assuming a gate current of five times I_{GT} and $< 1.0 \mu s$ rise time. If having done this, a di/dt problem is seen to still exist, the designer can also decrease the di/dt of the current waveform by adding inductance in series with the SCR, as shown in Figure 13. Of course, this reduces the circuit's ability to rapidly reduce the dc bus voltage and a tradeoff must be made between speedy voltage reduction and di/dt .

2. Surge Current

If the peak current and/or the duration of the surge is excessive, immediate destruction due to device overheating will result. The surge capability of the SCR is directly proportional to its die area. If the surge current cannot be reduced (by adding series resistance — see Figure 13) to a safe level which is consistent with the system's requirements for speedy bus voltage reduction, the designer must use a higher current SCR. This may result in the average current capability of the SCR exceeding the steady state current requirements imposed by the dc power supply.

A WORD ABOUT FUSING

Before leaving the subject of the crowbar SCR, a few words about fuse protection are in order. Referring back to Figure 11A, it will be seen that a fuse is necessary if the power supply to be protected is not output current limited. This fuse is not meant to prevent SCR failure but rather to prevent a fire!

In order to protect the SCR, the fuse would have to possess an I^2t rating less than that of the SCR and yet have a high enough continuous current rating to survive normal supply output currents. In addition, it must be capable of successfully clearing the high short circuit currents from the supply. Such a fuse as this is quite expensive, and may not even be available.

CROWBAR SCR SELECTION GUIDE

As an aid in selecting an SCR for crowbar use, the following selection guide is presented.

DEVICE	I_{RMS}	I_{FSM}	PACKAGE
2N6400 Series	16A	160A	TO220 Plastic
2N6504 Series	25A	160A	TO220 Plastic
2N1842 Series	16A	125A	Metal Stud
2N2573 Series	25A	260A	Metal TO-3 Type
2N681 Series	25A	200A	Metal Stud
MCR3935-1 Series	35A	350A	Metal Stud
MCR81-5 Series	80A	1000A	Metal Stud

MC3425

POWER SUPPLY SUPERVISORY/OVER-UNDER-VOLTAGE PROTECTION CIRCUIT

The MC3425 is a power supply supervisory circuit containing all the necessary functions required to monitor over- and under-voltage fault conditions. These integrated circuits contain dedicated over- and under-voltage sensing channels with independently programmable time delays. The over-voltage channel has a high current Drive Output for use in conjunction with an external SCR "Crowbar" for shutdown. The under-voltage channel input comparator has hysteresis which is externally programmable, and an open-collector output for fault indication.

- Dedicated Over- And Under-Voltage Sensing
- Programmable Hysteresis Of Under-Voltage Comparator
- Internal 2.5 V Reference
- 300 mA Over-Voltage Drive Output
- 30 mA Under-Voltage Indicator Output
- Programmable Time Delays
- 4.5 V to 40 V Operation

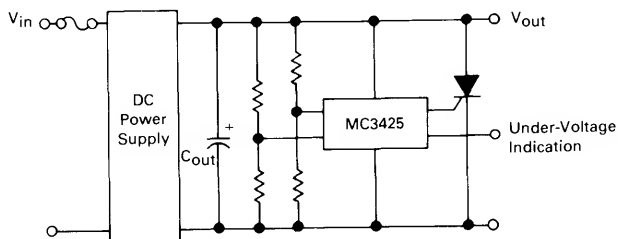
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	Vdc
Comparator Input Voltage Range (Note 1)	V_{IR}	-0.3 to +40	Vdc
Drive Output Short-Circuit Current	$I_{OS(DRV)}$	Internally Limited	mA
Indicator Output Voltage	V_{IND}	0 to 40	Vdc
Indicator Output Sink Current	I_{IND}	30	mA
Power Dissipation and Thermal Characteristics Maximum Power Dissipation ($T_A = 70^\circ\text{C}$) Thermal Resistance Junction to Air	P_D $R_{\theta JA}$	1000 80	mW °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

NOTE: (1) The input signal voltage should not be allowed to go negative by more than 300 mV or positive by more than 40 V, independent of V_{CC} , without device destruction.

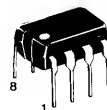
TYPICAL APPLICATION

Over-Voltage Crowbar Protection, Under-Voltage Indication



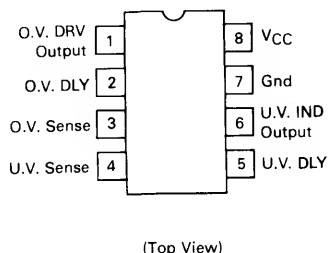
POWER SUPPLY SUPERVISORY/OVER-UNDER-VOLTAGE PROTECTION CIRCUIT

SILICON MONOLITHIC
INTEGRATED CIRCUIT



P1 SUFFIX
PLASTIC PACKAGE
CASE 626

PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
MC3425P1	0 to +70°C	Plastic DIP

ELECTRICAL CHARACTERISTICS (4.5 V ≤ V_{CC} ≤ 40 V; T_A = T_{low} to T_{high} [see Note 2] unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Sense Trip Voltage (Reference Voltage) V _{CC} = 15 V T _A = 25°C T _{low} to T _{high} (Note 2)	V _{Sense}	2.4 2.33	2.5 2.5	2.6 2.63	V _{dc}
Line Regulation of V _{Sense} 4.5 V ≤ V _{CC} ≤ 40 V; T _J = 25°C	Reg _{line}	—	7.0	15	mV
Power Supply Voltage Operating Range	V _{CC}	4.5	—	40	V _{dc}
Power Supply Current V _{CC} = 40 V; T _A = 25°C; No Output Loads O.V. Sense (Pin 3) = 0 V; U.V. Sense (Pin 4) = V _{CC}	I _{CC(off)}	—	8.5	10	mA
O.V. Sense (Pin 3) = V _{CC} ; U.V. Sense (Pin 4) = 0 V	I _{CC(on)}	—	16.5	19	mA
INPUT SECTION					
Input Bias Current, O.V. and U.V. Sense	I _B	—	1.0	2.0	μA
Hysteresis Activation Voltage, U.V. Sense V _{CC} = 15 V; T _A = 25°C; I _H = 10% I _H = 90%	V _{H(act)}	— —	0.6 0.8	— —	V
Hysteresis Current, U.V. Sense V _{CC} = 15 V; T _A = 25°C; U.V. Sense (Pin 4) = 2.5 V	I _H	9.0	12.5	16	μA
Delay Pin Voltage (I _{DLY} = 0 mA) Low State High State	V _{OL(DLY)} V _{OH(DLY)}	— V _{CC} -0.5	0.2 V _{CC} -0.15	0.5 —	V
Delay Pin Source Current V _{CC} = 15 V; V _{DLY} = 0 V	I _{DLY(source)}	140	200	260	μA
Delay Pin Sink Current V _{CC} = 15 V; V _{DLY} = 2.5 V	I _{DLY(sink)}	1.8	3.0	—	mA
OUTPUT SECTION					
Drive Output Peak Current (T _A = 25°C)	I _{DRV(peak)}	200	300	—	mA
Drive Output Voltage I _{DRV} = 100 mA; T _A = 25°C	V _{OH(DRV)}	V _{CC} -2.5	V _{CC} -2.0	—	V
Drive Output Leakage Current V _{DRV} = 0 V	I _{DRV(leak)}	—	15	200	nA
Drive Output Current Slew Rate (T _A = 25°C)	dI/dt	—	2.0	—	A/μs
Drive Output V _{CC} Transient Rejection V _{CC} = 0 V to 15 V at dV/dt = 200 V/μs; O.V. Sense (Pin 3) = 0 V; T _A = 25°C	I _{DRV(trans)}	—	1.0	—	mA (Peak)
Indicator Output Saturation Voltage I _{IND} = 30 mA; T _A = 25°C	V _{IND(sat)}	—	560	800	mV
Indicator Output Leakage Current V _{OH(IND)} = 40 V	I _{IND(leak)}	—	25	200	nA
Output Comparator Threshold Voltage (Note 3)	V _{th(OC)}	2.33	2.5	2.63	V
Propagation Delay Time (V _{CC} = 15 V; T _A = 25°C) Input to Drive Output or Indicator Output 100 mV Overdrive, C _{DLY} = 0 μF	t _{PLH(IN OUT)}	—	1.7	—	μs
Input to Delay 2.5 V Overdrive (0 V to 5.0 V Step)	t _{PLH(IN DLY)}	—	700	—	ns

NOTES:(2) T_{low} = - 0°CT_{high} = + 70°C(3) The V_{th(OC)} limits are approximately the V_{Sense} limits over the applicable temperature range

FIGURE 1 — HYSTERESIS CURRENT versus HYSTERESIS ACTIVATION VOLTAGE

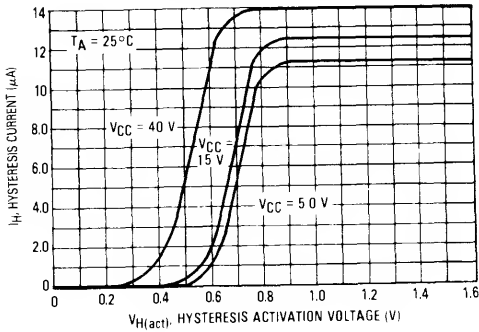


FIGURE 3 — HYSTERESIS CURRENT versus TEMPERATURE

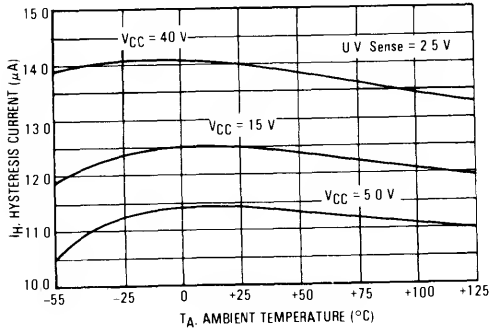


FIGURE 5 — OUTPUT DELAY TIME versus DELAY CAPACITANCE

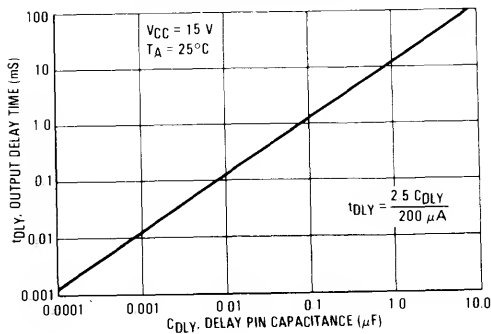


FIGURE 2 — HYSTERESIS ACTIVATION VOLTAGE versus TEMPERATURE

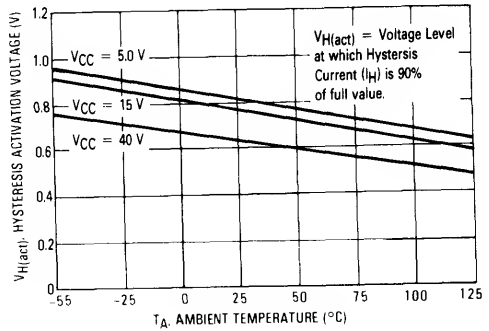


FIGURE 4 — SENSE TRIP VOLTAGE CHANGE versus TEMPERATURE

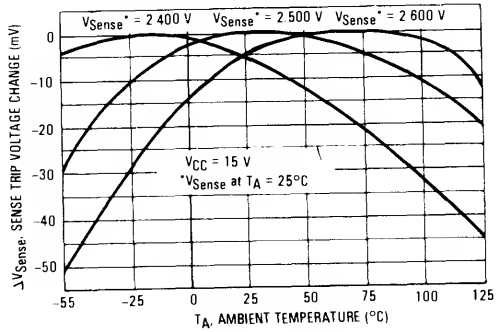
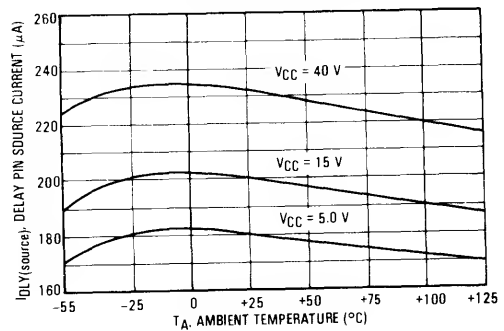
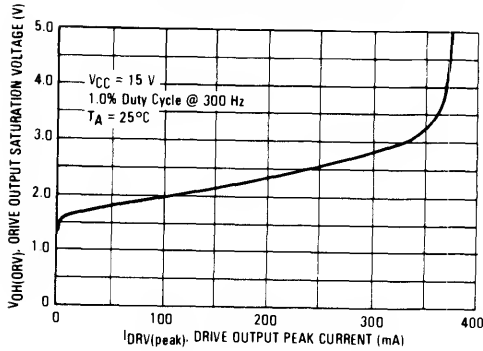


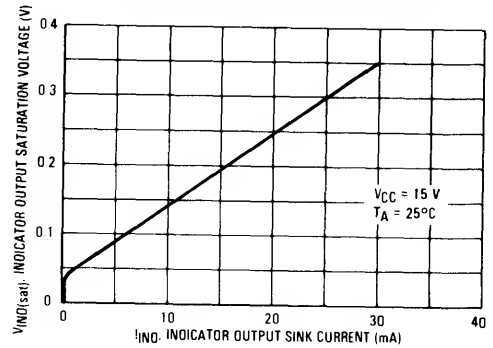
FIGURE 6 — DELAY PIN SOURCE CURRENT versus TEMPERATURE



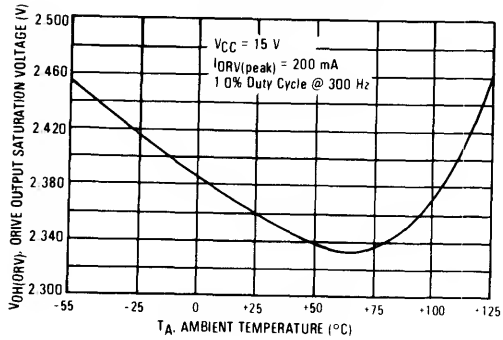
**FIGURE 7 — DRIVE OUTPUT SATURATION VOLTAGE
versus OUTPUT PEAK CURRENT**



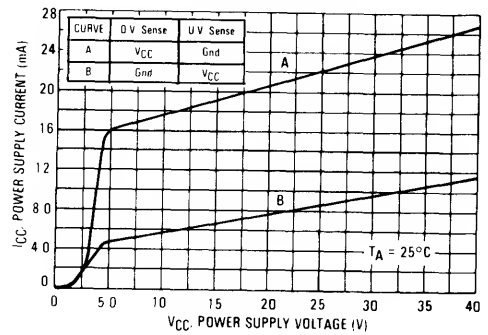
**FIGURE 8 — INDICATOR OUTPUT SATURATION
VOLTAGE versus OUTPUT SINK CURRENT**



**FIGURE 9 — DRIVE OUTPUT SATURATION VOLTAGE
versus TEMPERATURE**



**FIGURE 10 — POWER SUPPLY CURRENT
versus VOLTAGE**



APPLICATIONS INFORMATION

FIGURE 11 — OVERVOLTAGE PROTECTION AND UNDER VOLTAGE FAULT INDICATION WITH PROGRAMMABLE DELAY

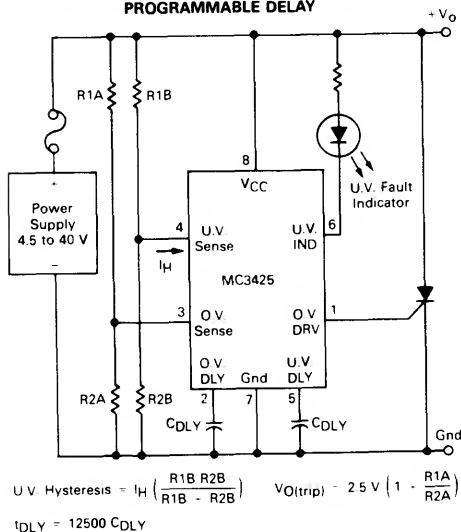


FIGURE 12 — OVERVOLTAGE PROTECTION OF 5.0 V SUPPLY WITH LINE LOSS DETECTOR

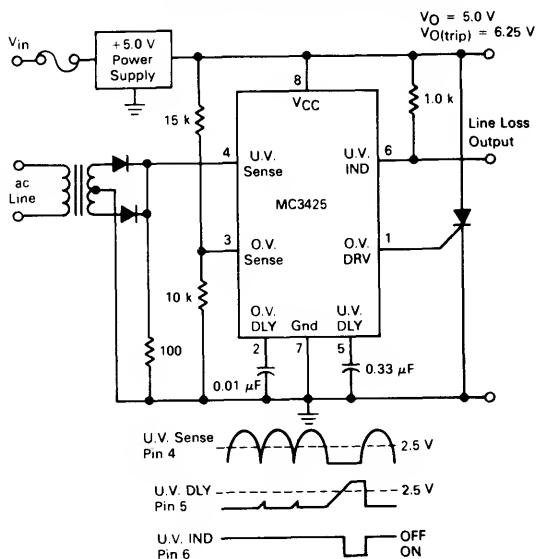


FIGURE 13 — OVERVOLTAGE AUDIO ALARM CIRCUIT

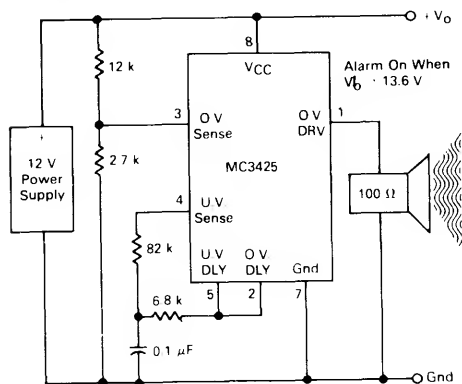
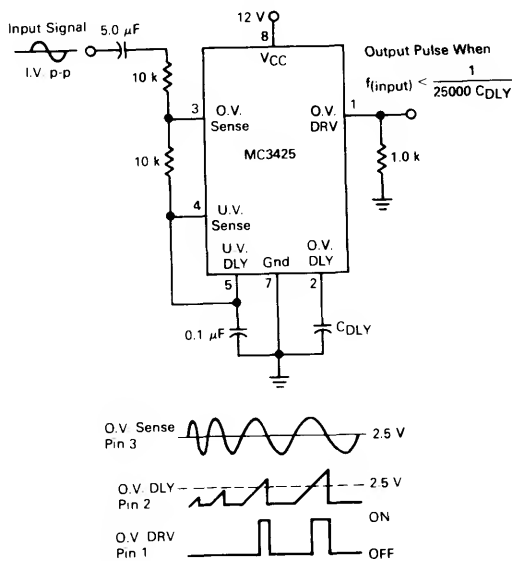


FIGURE 14 — PROGRAMMABLE FREQUENCY SWITCH



CIRCUIT DESCRIPTION

The MC3425 is a power supply supervisory circuit containing all the necessary functions required to monitor over- and under-voltage fault conditions. The block diagram is shown below in Figure 15. The Over-Voltage (O.V.) and Under-Voltage (U.V.) Input Comparators are both referenced to an internal 2.5 V regulator. The U.V. Input Comparator has a feedback activated $12.5 \mu\text{A}$ current sink (I_H) which is used for programming the input hysteresis voltage (V_H). The source resistance feeding this input (R_H) determines the amount of hysteresis voltage by $V_H = I_H R_H = 12.5 \times 10^{-6} R_H$.

Separate Delay pins (O.V. DLY, U.V. DLY) are provided for each channel to independently delay the Drive and Indicator outputs, thus providing greater input noise immunity. The two Delay pins are essentially the outputs of the respective input comparators, and provide a constant current source, $I_{DLY}(\text{source})$, of typically $200 \mu\text{A}$ when the non-inverting input voltage is greater than the inverting input level. A capacitor connected from these Delay pins to ground, will establish a predictable delay time (t_{DLY}) for the Drive and Indicator outputs. The Delay pins are internally connected to the non-inverting inputs of the O.V. and U.V. Output Comparators, which are referenced to the internal 2.5 V regulator. Therefore, delay time (t_{DLY})

is based on the constant current source, $I_{DLY}(\text{source})$, charging the external delay capacitor (C_{DLY}) to 2.5 volts.

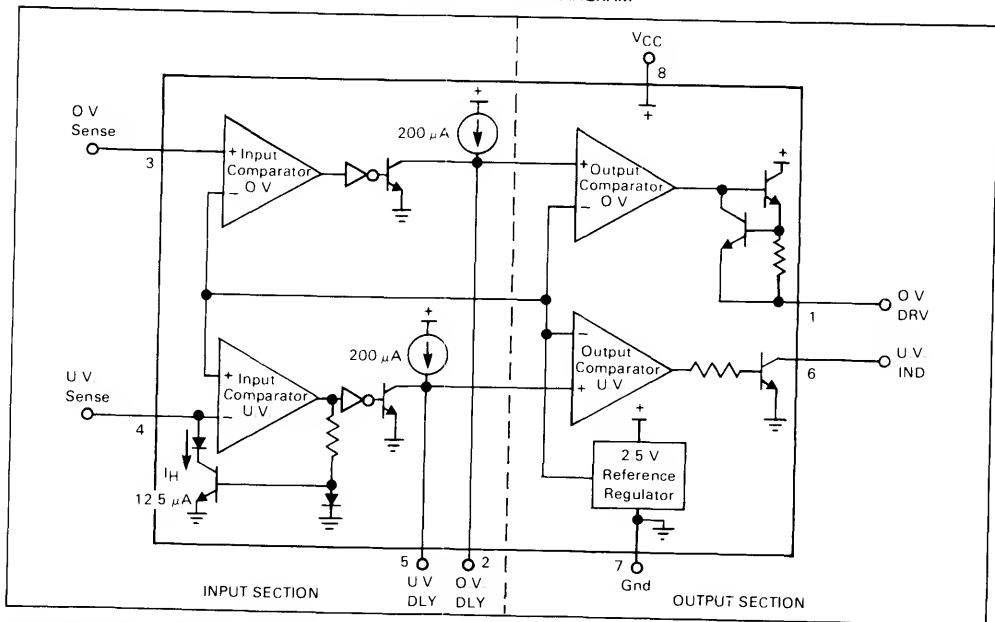
$$t_{DLY} = \frac{V_{ref} C_{DLY}}{I_{DLY}(\text{source})} = \frac{2.5 C_{DLY}}{200 \mu\text{A}} = 12500 C_{DLY}$$

Figure 5 provides C_{DLY} values for a wide range of time delays. The Delay pins are pulled low when the respective input comparator's non-inverting input is less than the inverting input. The sink current, $I_{DLY}(\text{sink})$, capability of the Delay pins is $\geq 1.8 \text{ mA}$ and is much greater than the typical $200 \mu\text{A}$ source current, thus enabling a relatively fast delay capacitor discharge time.

The Over-Voltage Drive Output is a current-limited emitter-follower capable of sourcing 300 mA at a turn-on slew rate of $2.0 \text{ A}/\mu\text{s}$, ideal for driving "Crowbar" SCR's. The Under-Voltage Indicator Output is an open-collector, NPN transistor, capable of sinking 30 mA to provide sufficient drive for LED's, small relays or shut-down circuitry. These current capabilities apply to both channels operating simultaneously, providing device power dissipation limits are not exceeded.

The MC3425 has an internal 2.5 V bandgap reference regulator with an accuracy of $\pm 4.0\%$ for the basic devices and $\pm 1.0\%$ for the A-suffix device types at 25°C . The reference has a typical temperature coefficient of $30 \text{ ppm}/^\circ\text{C}$ for A-suffix devices.

FIGURE 15 — BLOCK DIAGRAM



Note: All voltages and currents are nominal.

CROWBAR SCR CONSIDERATIONS

Referring to Figure 16, it can be seen that the crowbar SCR, when activated, is subject to a large current surge from the output capacitance, C_{out} . This capacitance consists of the power supply output capacitors, the load's decoupling capacitors, and in the case of Figure 16A, the supply's input filter capacitors. This surge current is illustrated in Figure 17, and can cause SCR failure or degradation by any one of three mechanisms: di/dt , absolute peak surge, or I^2t . The interrelationship of these failure methods and the breadth of the applications make specification of the SCR by the semiconductor manufacturer difficult and expensive. Therefore, the designer must empirically determine the SCR and circuit elements which result in reliable and effective OVP operation. However, an understanding of the factors which influence the SCR's di/dt and surge capabilities simplifies this task.

1. di/dt

As the gate region of the SCR is driven on, its area of conduction takes a finite amount of time to grow, starting as a very small region and gradually spreading. Since the anode current flows through this turned-on

gate region, very high current densities can occur in the gate region if high anode currents appear quickly (di/dt). This can result in immediate destruction of the SCR or gradual degradation of its forward blocking voltage capabilities — depending on the severity of the occasion.

The value of di/dt that an SCR can safely handle is influenced by its construction and the characteristics of the gate drive signal. A center-gate-fire SCR has more di/dt capability than a corner-gate-fire type, and heavily overdriving (3 to 5 times I_{GT}) the SCR gate with a fast $<1.0 \mu s$ rise time signal will maximize its di/dt capability. A typical maximum number in phase control SCRs of less than 50 A(RMS) rating might be 200 A/ μs , assuming a gate current of five times I_{GT} and $<1.0 \mu s$ rise time. If having done this, a di/dt problem is seen to still exist, the designer can also decrease the di/dt of the current waveform by adding inductance in series with the SCR, as shown in Figure 18. Of course, this reduces the circuit's ability to rapidly reduce the dc bus voltage and a tradeoff must be made between speedy voltage reduction and di/dt .

FIGURE 16 — TYPICAL CROWBAR CIRCUIT CONFIGURATIONS

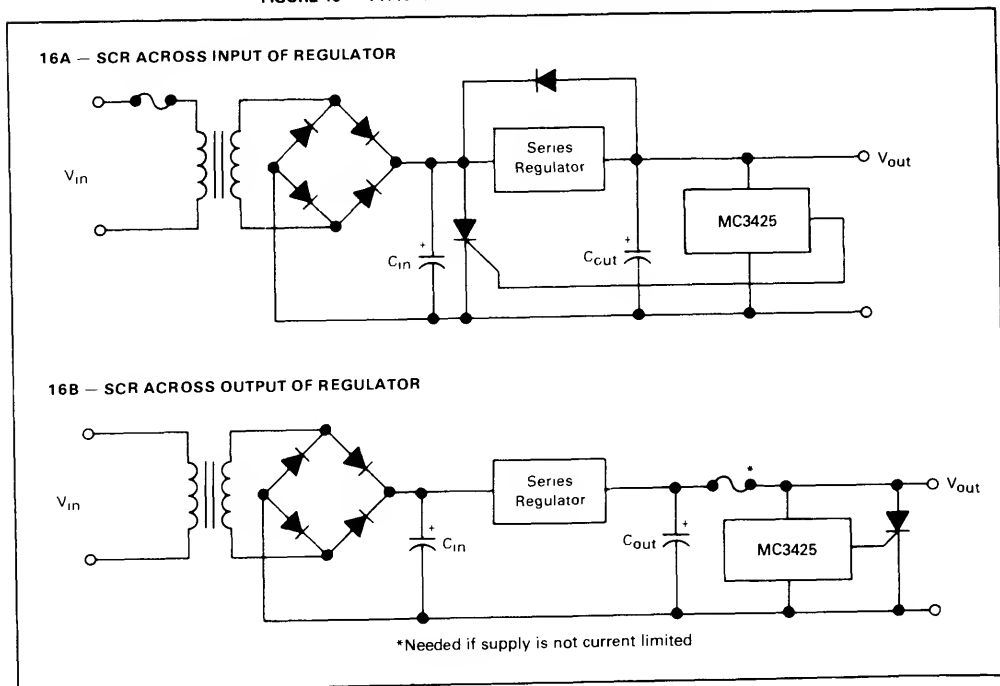
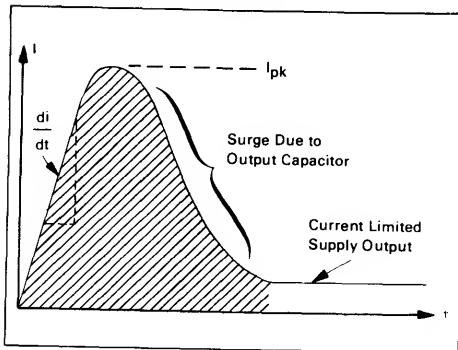
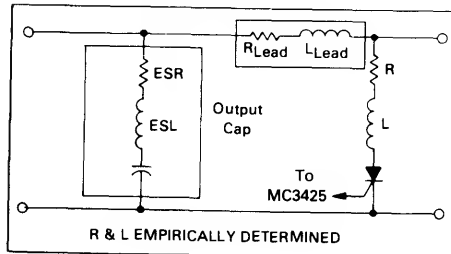


FIGURE 17 — CROWBAR SCR SURGE CURRENT WAVEFORM



2. Surge Current

If the peak current and/or the duration of the surge is excessive, immediate destruction due to device overheating will result. The surge capability of the SCR is directly proportional to its die area. If the surge current cannot be reduced (by adding series resistance — see Figure 18) to a safe level which is consistent with the system's requirements for speedy bus voltage reduction, the designer must use a higher current SCR. This may result in the average current capability of the SCR exceeding the steady state current requirements imposed by the dc power supply.

FIGURE 18 — CIRCUIT ELEMENTS AFFECTING SCR SURGE & di/dt 

A WORD ABOUT FUSING

Before leaving the subject of the crowbar SCR, a few words about fuse protection are in order. Referring back to Figure 16A, it will be seen that a fuse is necessary if the power supply to be protected is not output current limited. This fuse is not meant to prevent SCR failure but rather to prevent a fire!

In order to protect the SCR, the fuse would have to possess an I^2t rating less than that of the SCR and yet have a high enough continuous current rating to survive normal supply output currents. In addition, it must be capable of successfully clearing the high short circuit currents from the supply. Such a fuse as this is quite expensive, and may not even be available.

The usual design compromise then is to use a garden variety fuse (3AG or 3AB style) which cannot be relied on to blow before the thyristor does, and trust that if the SCR does fail, it will fail short circuit. In the majority of the designs, this will be the case, though this is difficult to guarantee. Of course, a sufficiently high surge will cause an open. These comments also apply to the fuse in Figure 16B.

CROWBAR SCR SELECTION GUIDE

As an aid in selecting an SCR for crowbar use, the following selection guide is presented.

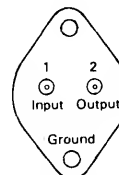
DEVICE	I_{RMS}	I_{FSM}	PACKAGE
MCR67 Series	12 A	100 A	Metal Stud
MCR68 Series	12 A	100 A	TO-220 Plastic
2N1842 Series	16 A	125 A	Metal Stud
2N6400 Series	16 A	160 A	TO-220 Plastic
2N6504 Series	25 A	160 A	TO-220 Plastic
2N681 Series	25 A	200 A	Metal Stud
2N2573 Series	25 A	260 A	TO-3 Metal Can
MCR69 Series	25 A	300 A	TO-220 Plastic
MCR70 Series	35 A	350 A	Metal Stud
MCR71 Series	55 A	550 A	Metal Stud

For a complete and detailed treatment of SCR and fuse selection refer to Motorola Application Note AN789.

THREE-TERMINAL POSITIVE FIXED VOLTAGE REGULATORS

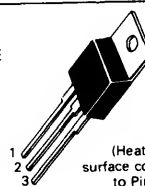
SILICON MONOLITHIC INTEGRATED CIRCUITS

- K SUFFIX**
METAL PACKAGE
CASE 1



Pins 1 and 2 electrically isolated from case. Case is third electrical connection

T SUFFIX
PLASTIC PACKAGE
CASE 221A



PIN 1. INPUT
2. GROUND
3. OUTPUT

(Heatsink
surface connected
to Pin 2.)

A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O is not needed for stability; however, it does improve transient response.

XX indicates nominal voltage

TYPE NO./VOLTAGE

Device	Output Voltage Tolerance	Tested Operating Junction Temp. Range	Package
MC78XXK MC78XXAK*	4% 2%	- 55 to +150°C	Metal Power
MC78XXCK MC78XXACK*	4% 2%	0 to +125°C	Plastic Power
MC78XXCT MC78XXACT	4% 2%	- 40 to +125°C	
MC78XXBT	4%		

MC7805	5.0 Volts	MC7812	12 Volts
MC7806	6.0 Volts	MC7815	15 Volts
MC7808	8.0 Volts	MC7818	18 Volts
MC7809	9.0 Volts	MC7824	24 Volts

MC7800 Series

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (5.0 V — 18 V) (24 V)	V_{in}	35 40	Vdc
Power Dissipation and Thermal Characteristics			
Plastic Package			
$T_A = +25^\circ\text{C}$	P_D	Internally Limited	Watts
Derate above $T_A = +25^\circ\text{C}$	$1/\theta_{JA}$	15.4	mW/ $^\circ\text{C}$
Thermal Resistance, Junction to Air	θ_{JA}	65	$^\circ\text{C/W}$
$T_C = +25^\circ\text{C}$	P_D	Internally Limited	Watts
Derate above $T_C = +75^\circ\text{C}$ (See Figure 1)	$1/\theta_{JC}$	200	mW/ $^\circ\text{C}$
Thermal Resistance, Junction to Case	θ_{JC}	5.0	$^\circ\text{C/W}$
Metal Package			
$T_A = +25^\circ\text{C}$	P_D	Internally Limited	Watts
Derate above $T_A = +25^\circ\text{C}$	$1/\theta_{JA}$	22.5	mW/ $^\circ\text{C}$
Thermal Resistance, Junction to Air	θ_{JA}	45	$^\circ\text{C/W}$
$T_C = +25^\circ\text{C}$	P_D	Internally Limited	Watts
Derate above $T_C = +65^\circ\text{C}$ (See Figure 2)	$1/\theta_{JC}$	182	mW/ $^\circ\text{C}$
Thermal Resistance, Junction to Case	θ_{JC}	5.5	$^\circ\text{C/W}$
Storage Junction Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature Range	T_J		$^\circ\text{C}$
	MC7800A	-55 to +150	
	MC7800C, AC	0 to +150	
	MC7800B	-40 to +150	

DEFINITIONS

Line Regulation — The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation — The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation — The maximum total device dissipation for which the regulator will operate within specifications.

Quiescent Current — That part of the input current that is not delivered to the load.

Output Noise Voltage — The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long Term Stability — Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.

MC7800 Series

MC7805, B, C

ELECTRICAL CHARACTERISTICS ($V_{in} = 10\text{ V}$, $I_O = 500\text{ mA}$, $T_J = T_{low}$ to T_{high} [Note 1] unless otherwise noted)

Characteristic	Symbol	MC7805			MC7805B			MC7805C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	4.8	5.0	5.2	4.8	5.0	5.2	4.8	5.0	5.2	Vdc
Output Voltage ($50\text{ mA} \leq I_O \leq 1.0\text{ A}$, $P_O \leq 15\text{ W}$) $7.0\text{ Vdc} \leq V_{in} \leq 20\text{ Vdc}$ $8.0\text{ Vdc} \leq V_{in} \leq 20\text{ Vdc}$	V_O	—	—	—	—	—	—	4.75	5.0	5.25	Vdc
Line Regulation ($T_J = +25^\circ\text{C}$, Note 2) $7.0\text{ Vdc} \leq V_{in} \leq 25\text{ Vdc}$ $8.0\text{ Vdc} \leq V_{in} \leq 12\text{ Vdc}$	Reg_{line}	—	2.0	50	—	7.0	100	—	7.0	100	mV
Load Regulation ($T_J = +25^\circ\text{C}$, Note 2) $50\text{ mA} \leq I_O \leq 1.5\text{ A}$ $250\text{ mA} \leq I_O \leq 750\text{ mA}$	Reg_{load}	—	25	100	—	40	100	—	40	100	mV
Quiescent Current ($T_J = +25^\circ\text{C}$)	I_B	—	3.2	6.0	—	4.3	8.0	—	4.3	8.0	mA
Quiescent Current Change $7.0\text{ Vdc} \leq V_{in} \leq 25\text{ Vdc}$ $8.0\text{ Vdc} \leq V_{in} \leq 25\text{ Vdc}$ $50\text{ mA} \leq I_O \leq 1.0\text{ A}$	ΔI_B	—	—	—	—	—	—	—	—	1.3	mA
Ripple Rejection $8.0\text{ Vdc} \leq V_{in} \leq 18\text{ Vdc}$, $f = 120\text{ Hz}$	RR	68	75	—	—	68	—	—	68	—	dB
Dropout Voltage ($I_O = 1.0\text{ A}$, $T_J = +25^\circ\text{C}$)	$V_{in} - V_O$	—	2.0	2.5	—	2.0	—	—	2.0	—	Vdc
Output Noise Voltage ($T_A = +25^\circ\text{C}$) $10\text{ Hz} \leq f \leq 100\text{ kHz}$	V_n	—	10	40	—	10	—	—	10	—	$\mu\text{V}/V_O$
Output Resistance ($f = 1.0\text{ kHz}$)	r_O	—	17	—	—	17	—	—	17	—	m Ω
Short Circuit Current Limit ($T_A = +25^\circ\text{C}$) $V_{in} = 35\text{ Vdc}$	I_{sc}	—	0.2	1.2	—	0.2	—	—	0.2	—	A
Peak Output Current ($T_J = +25^\circ\text{C}$)	I_{max}	1.3	2.5	3.3	—	2.2	—	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	± 0.6	—	—	-1.1	—	—	-1.1	—	mV/ $^\circ\text{C}$

MC7805A, AC

ELECTRICAL CHARACTERISTICS ($V_{in} = 10\text{ V}$, $I_O = 1.0\text{ A}$, $T_J = T_{low}$ to T_{high} [Note 1] unless otherwise noted)

Characteristics	Symbol	MC7805A			MC7805AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	4.9	5.0	5.1	4.9	5.0	5.1	Vdc
Output Voltage ($50\text{ mA} \leq I_O \leq 1.0\text{ A}$, $P_O \leq 15\text{ W}$) $7.5\text{ Vdc} \leq V_{in} \leq 20\text{ Vdc}$	V_O	4.8	5.0	5.2	4.8	5.0	5.2	Vdc
Line Regulation (Note 2) $7.5\text{ Vdc} \leq V_{in} \leq 25\text{ Vdc}$, $I_O = 500\text{ mA}$ $8.0\text{ Vdc} \leq V_{in} \leq 12\text{ Vdc}$ $8.0\text{ Vdc} \leq V_{in} \leq 12\text{ Vdc}$, $T_J = +25^\circ\text{C}$ $7.3\text{ Vdc} \leq V_{in} \leq 20\text{ Vdc}$, $T_J = +25^\circ\text{C}$	Reg_{line}	—	2.0	10	—	7.0	50	mV
Load Regulation (Note 2) $50\text{ mA} \leq I_O \leq 1.5\text{ A}$, $T_J = +25^\circ\text{C}$ $50\text{ mA} \leq I_O \leq 1.0\text{ A}$ $250\text{ mA} \leq I_O \leq 750\text{ mA}$, $T_J = +25^\circ\text{C}$ $250\text{ mA} \leq I_O \leq 750\text{ mA}$	Reg_{load}	—	2.0	25	—	25	100	mV
Quiescent Current $T_J = +25^\circ\text{C}$	I_B	—	3.2	5.0	—	4.3	6.0	mA
Quiescent Current Change $8.0\text{ Vdc} \leq V_{in} \leq 25\text{ Vdc}$, $I_O = 500\text{ mA}$ $7.5\text{ Vdc} \leq V_{in} \leq 20\text{ Vdc}$, $T_J = +25^\circ\text{C}$ $50\text{ mA} \leq I_O \leq 1.0\text{ A}$	ΔI_B	—	0.3	0.5	—	—	0.8	mA
Ripple Rejection $8.0\text{ Vdc} \leq V_{in} \leq 18\text{ Vdc}$, $f = 120\text{ Hz}$, $T_J = +25^\circ\text{C}$ $8.0\text{ Vdc} \leq V_{in} \leq 18\text{ Vdc}$, $f = 120\text{ Hz}$, $I_O = 500\text{ mA}$	RR	68	75	—	—	68	—	dB
Dropout Voltage ($I_O = 1.0\text{ A}$, $T_J = +25^\circ\text{C}$)	$V_{in} - V_O$	—	2.0	2.5	—	2.0	—	Vdc
Output Noise Voltage ($T_A = +25^\circ\text{C}$) $10\text{ Hz} \leq f \leq 100\text{ kHz}$	V_n	—	10	40	—	10	—	$\mu\text{V}/V_O$
Output Resistance ($f = 1.0\text{ kHz}$)	r_O	—	2.0	—	—	17	—	m Ω
Short-Circuit Current Limit ($T_A = +25^\circ\text{C}$) $V_{in} = 35\text{ Vdc}$	I_{sc}	—	0.2	1.2	—	0.2	—	A
Peak Output Current ($T_J = +25^\circ\text{C}$)	I_{max}	1.3	2.5	3.3	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	± 0.6	—	—	-1.1	—	mV/ $^\circ\text{C}$

NOTES: 1. $T_{low} = -55^\circ\text{C}$ for MC78XX, A
 $= 0^\circ$ for MC78XXC, AC
 $= -40^\circ\text{C}$ for MC78XXB
 $T_{high} = +150^\circ\text{C}$ for MC78XX, A
 $= +125^\circ\text{C}$ for MC78XXC, AC, B

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7800 Series

MC7806, B, C

ELECTRICAL CHARACTERISTICS ($V_{in} = 11\text{ V}$, $I_O = 500\text{ mA}$, $T_J = T_{low}$ to T_{high} [Note 1] unless otherwise noted).

Characteristic	Symbol	MC7806			MC7806B			MC7806C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	5.75	6.0	6.25	5.75	6.0	6.25	5.75	6.0	6.25	Vdc
Output Voltage ($5.0\text{ mA} \leq I_O \leq 1.0\text{ A}$, $P_O \leq 15\text{ W}$)	V_O	—	—	—	—	—	—	—	—	—	Vdc
8.0 Vdc $\leq V_{in} \leq 21\text{ Vdc}$		—	—	—	—	—	—	—	—	—	
9.0 Vdc $\leq V_{in} \leq 21\text{ Vdc}$		5.65	6.0	6.35	5.7	6.0	6.3	—	6.0	6.3	
Line Regulation ($T_J = +25^\circ\text{C}$, Note 2)	Reg _{line}	—	3.0	60	—	9.0	120	—	9.0	120	mV
8.0 Vdc $\leq V_{in} \leq 25\text{ Vdc}$		—	2.0	30	—	3.0	60	—	3.0	60	
9.0 Vdc $\leq V_{in} \leq 13\text{ Vdc}$		—	—	—	—	—	—	—	—	—	
Load Regulation ($T_J = +25^\circ\text{C}$, Note 2)	Reg _{load}	—	27	100	—	43	120	—	43	120	mV
5.0 mA $\leq I_O \leq 1.5\text{ A}$		—	9.0	30	—	16	60	—	16	60	
250 mA $\leq I_O \leq 750\text{ mA}$		—	—	—	—	—	—	—	—	—	
Quiescent Current ($T_J = +25^\circ\text{C}$)	I_B	—	3.2	6.0	—	4.3	8.0	—	4.3	8.0	mA
Quiescent Current Change	ΔI_B	—	—	—	—	—	—	—	—	—	mA
8.0 Vdc $\leq V_{in} \leq 25\text{ Vdc}$		—	—	—	—	—	—	—	—	—	
9.0 Vdc $\leq V_{in} \leq 25\text{ Vdc}$		—	0.3	0.8	—	—	1.3	—	—	1.3	
5.0 mA $\leq I_O \leq 1.0\text{ A}$		—	0.04	0.5	—	—	0.5	—	—	0.5	
Ripple Rejection	RR	65	73	—	—	65	—	—	65	—	dB
9.0 Vdc $\leq V_{in} \leq 19\text{ Vdc}$, $f = 120\text{ Hz}$		—	—	—	—	—	—	—	—	—	
Dropout Voltage ($I_O = 1.0\text{ A}$, $T_J = +25^\circ\text{C}$)	$V_{in} - V_O$	—	2.0	2.5	—	2.0	—	—	2.0	—	Vdc
Output Noise Voltage ($T_A = +25^\circ\text{C}$)	V_n	—	10	40	—	10	—	—	10	—	$\mu\text{V}/V_O$
10 Hz $\leq f \leq 100\text{ kHz}$		—	—	—	—	—	—	—	—	—	
Output Resistance $f = 1.0\text{ kHz}$	r_O	—	17	—	—	17	—	—	17	—	m Ω
Short-Circuit Current Limit ($T_A = +25^\circ\text{C}$)	I_{sc}	—	0.2	1.2	—	0.2	—	—	0.2	—	A
$V_{in} = 35\text{ Vdc}$		—	—	—	—	—	—	—	—	—	
Peak Output Current ($T_J = +25^\circ\text{C}$)	I_{max}	1.3	2.5	3.3	—	2.2	—	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	± 0.7	—	—	-0.8	—	—	-0.8	—	mV/ $^\circ\text{C}$

MC7806AC

ELECTRICAL CHARACTERISTICS ($V_{in} = 11\text{ V}$, $I_O = 1.0\text{ A}$, $T_J = T_{low}$ to T_{high} [Note 1] unless otherwise noted).

Characteristics	Symbol	MC7806AC			Unit
		Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	5.88	6.0	6.12	Vdc
Output Voltage ($5.0\text{ mA} \leq I_O \leq 1.0\text{ A}$, $P_O \leq 15\text{ W}$)	V_O	5.76	6.0	6.24	Vdc
8.6 Vdc $\leq V_{in} \leq 21\text{ Vdc}$		—	—	—	
Line Regulation (Note 2)	Reg _{line}	—	9.0	60	mV
8.6 Vdc $\leq V_{in} \leq 25\text{ Vdc}$, $I_O = 500\text{ mA}$		—	11	60	
9.0 Vdc $\leq V_{in} \leq 13\text{ Vdc}$		—	3.0	30	
9.0 Vdc $\leq V_{in} \leq 13\text{ Vdc}$, $T_J = +25^\circ\text{C}$		—	9.0	60	
8.3 Vdc $\leq V_{in} \leq 21\text{ Vdc}$, $T_J = +25^\circ\text{C}$		—	—	—	
Load Regulation (Note 2)	Reg _{load}	—	43	100	mV
5.0 mA $\leq I_O \leq 1.5\text{ A}$, $T_J = +25^\circ\text{C}$		—	43	100	
5.0 mA $\leq I_O \leq 1.0\text{ A}$		—	—	—	
250 mA $\leq I_O \leq 750\text{ mA}$, $T_J = +25^\circ\text{C}$		—	16	50	
250 mA $\leq I_O \leq 750\text{ mA}$		—	—	—	
Quiescent Current	I_B	—	—	6.0	mA
$T_J = +25^\circ\text{C}$		—	4.3	6.0	
Quiescent Current Change	ΔI_B	—	—	0.8	mA
9.0 Vdc $\leq V_{in} \leq 25\text{ Vdc}$, $I_O = 500\text{ mA}$		—	—	0.8	
8.6 Vdc $\leq V_{in} \leq 21\text{ Vdc}$, $T_J = +25^\circ\text{C}$		—	—	0.5	
5.0 mA $\leq I_O \leq 1.0\text{ A}$		—	—	—	
Ripple Rejection	RR	—	—	—	dB
9.0 Vdc $\leq V_{in} \leq 19\text{ Vdc}$, $f = 120\text{ Hz}$, $T_J = +25^\circ\text{C}$		—	65	—	
9.0 Vdc $\leq V_{in} \leq 19\text{ Vdc}$, $f = 120\text{ Hz}$, $I_O = 500\text{ mA}$		—	—	—	
Dropout Voltage ($I_O = 1.0\text{ A}$, $T_J = +25^\circ\text{C}$)	$V_{in} - V_O$	—	2.0	—	Vdc
Output Noise Voltage ($T_A = +25^\circ\text{C}$)	V_n	—	10	—	$\mu\text{V}/V_O$
10 Hz $\leq f \leq 100\text{ kHz}$		—	—	—	
Output Resistance ($f = 1.0\text{ kHz}$)	r_O	—	17	—	m Ω
Short-Circuit Current Limit ($T_A = +25^\circ\text{C}$)	I_{sc}	—	0.2	—	A
$V_{in} = 35\text{ Vdc}$		—	—	—	
Peak Output Current ($T_J = +25^\circ\text{C}$)	I_{max}	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	-0.8	—	mV/ $^\circ\text{C}$

NOTES: 1. $T_{low} = -55^\circ\text{C}$ for MC78XX
 $= 0^\circ$ for MC78XXC, AC
 $= -40^\circ\text{C}$ for MC78XXB
 $T_{high} = +150^\circ\text{C}$ for MC78XX
 $= +125^\circ\text{C}$ for MC78XXC, AC, B

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7800 Series

MC7808, B, C

ELECTRICAL CHARACTERISTICS ($V_{in} = 14\text{ V}$, $I_O = 500\text{ mA}$, $T_J = T_{low}$ to T_{high} [Note 1] unless otherwise noted).

Characteristic	Symbol	MC7808			MC7808B			MC7808C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	7.7	8.0	8.3	7.7	8.0	8.3	7.7	8.0	8.3	Vdc
Output Voltage ($5.0\text{ mA} \leq I_O \leq 1.0\text{ A}$, $P_O \leq 15\text{ W}$) $10.5\text{ Vdc} \leq V_{in} \leq 23\text{ Vdc}$ $11.5\text{ Vdc} \leq V_{in} \leq 23\text{ Vdc}$	V_O	—	—	—	—	—	—	7.6	8.0	8.4	Vdc
Line Regulation ($T_J = +25^\circ\text{C}$, Note 2) $10.5\text{ Vdc} \leq V_{in} \leq 25\text{ Vdc}$ $11\text{ Vdc} \leq V_{in} \leq 17\text{ Vdc}$	Regline	—	3.0	80	—	12	160	—	12	160	mV
Load Regulation ($T_J = +25^\circ\text{C}$, Note 2) $5.0\text{ mA} \leq I_O \leq 1.5\text{ A}$ $250\text{ mA} \leq I_O \leq 750\text{ mA}$	Regload	—	28	100	—	45	160	—	45	160	mV
Quiescent Current ($T_J = +25^\circ\text{C}$)	I_B	—	3.2	6.0	—	4.3	8.0	—	4.3	8.0	mA
Quiescent Current Change $10.5\text{ Vdc} \leq V_{in} \leq 25\text{ Vdc}$ $11.5\text{ Vdc} \leq V_{in} \leq 25\text{ Vdc}$ $5.0\text{ mA} \leq I_O \leq 1.0\text{ A}$	ΔI_B	—	—	—	—	—	—	—	—	1.0	mA
Ripple Rejection $11.5\text{ Vdc} \leq V_{in} \leq 21.5\text{ Vdc}$, $f = 120\text{ Hz}$	RR	62	70	—	—	62	—	—	62	—	dB
Dropout Voltage ($I_O = 1.0\text{ A}$, $T_J = +25^\circ\text{C}$)	$V_{in}-V_O$	—	2.0	2.5	—	2.0	—	—	2.0	—	Vdc
Output Noise Voltage ($T_A = +25^\circ\text{C}$) $10\text{ Hz} \leq f \leq 100\text{ kHz}$	V_n	—	10	40	—	10	—	—	10	—	$\mu\text{V}/V_O$
Output Resistance $f = 1.0\text{ kHz}$	r_O	—	18	—	—	18	—	—	18	—	$\text{m}\Omega$
Short-Circuit Current Limit ($T_A = +25^\circ\text{C}$) $V_{in} = 35\text{ Vdc}$	I_{sc}	—	0.2	1.2	—	0.2	—	—	0.2	—	A
Peak Output Current ($T_J = +25^\circ\text{C}$)	I_{max}	1.3	2.5	3.3	—	2.2	—	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	± 1.0	—	—	-0.8	—	—	-0.8	—	$\text{mV}/^\circ\text{C}$

MC7808AC

ELECTRICAL CHARACTERISTICS ($V_{in} = 14\text{ V}$, $I_O = 1.0\text{ A}$, $T_J = T_{low}$ to T_{high} [Note 1] unless otherwise noted).

Characteristics	Symbol	MC7808AC			Unit
		Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	7.84	8.0	8.16	Vdc
Output Voltage ($5.0\text{ mA} \leq I_O \leq 1.0\text{ A}$, $P_O \leq 15\text{ W}$) $10.6\text{ Vdc} \leq V_{in} \leq 23\text{ Vdc}$	V_O	7.7	8.0	8.3	Vdc
Line Regulation (Note 2) $10.6\text{ Vdc} \leq V_{in} \leq 25\text{ Vdc}$, $I_O = 500\text{ mA}$ $11\text{ Vdc} \leq V_{in} \leq 17\text{ Vdc}$ $11\text{ Vdc} \leq V_{in} \leq 17\text{ Vdc}$, $T_J = +25^\circ\text{C}$ $10.4\text{ Vdc} \leq V_{in} \leq 23\text{ Vdc}$, $T_J = +25^\circ\text{C}$	Regline	—	12	80	mV
Load Regulation (Note 2) $5.0\text{ mA} \leq I_O \leq 1.5\text{ A}$, $T_J = +25^\circ\text{C}$ $5.0\text{ mA} \leq I_O \leq 1.0\text{ A}$ $250\text{ mA} \leq I_O \leq 750\text{ mA}$, $T_J = +25^\circ\text{C}$ $250\text{ mA} \leq I_O \leq 750\text{ mA}$	Regload	—	45	100	mV
Quiescent Current $T_J = +25^\circ\text{C}$	I_B	—	—	6.0	mA
Quiescent Current Change $11\text{ Vdc} \leq V_{in} \leq 25\text{ Vdc}$, $I_O = 500\text{ mA}$ $10.6\text{ Vdc} \leq V_{in} \leq 23\text{ Vdc}$, $T_J = +25^\circ\text{C}$ $5.0\text{ mA} \leq I_O \leq 1.0\text{ A}$	ΔI_B	—	—	0.8	mA
Ripple Rejection $11.5\text{ Vdc} \leq V_{in} \leq 21.5\text{ Vdc}$, $f = 120\text{ Hz}$, $T_J = +25^\circ\text{C}$ $11.5\text{ Vdc} \leq V_{in} \leq 21.5\text{ Vdc}$, $f = 120\text{ Hz}$, $I_O = 500\text{ mA}$	RR	—	62	—	dB
Dropout Voltage ($I_O = 1.0\text{ A}$, $T_J = +25^\circ\text{C}$)	$V_{in}-V_O$	—	2.0	—	Vdc
Output Noise Voltage ($T_A = +25^\circ\text{C}$) $10\text{ Hz} \leq f \leq 100\text{ kHz}$	V_n	—	10	—	$\mu\text{V}/V_O$
Output Resistance ($f = 1.0\text{ kHz}$)	r_O	—	18	—	$\text{m}\Omega$
Short-Circuit Current Limit ($T_A = +25^\circ\text{C}$) $V_{in} = 35\text{ Vdc}$	I_{sc}	—	0.2	—	A
Peak Output Current ($T_J = +25^\circ\text{C}$)	I_{max}	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	-0.8	—	$\text{mV}/^\circ\text{C}$

NOTES: 1. $T_{low} = -55^\circ\text{C}$ for MC78XX, $T_{high} = +150^\circ\text{C}$ for MC78XX
 = 0° for MC78XXC, AC
 = -40°C for MC78XXB
 2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used

MC7800 Series

MC7809CT

ELECTRICAL CHARACTERISTICS ($V_{in} = 15\text{ V}$, $I_O = 500\text{ mA}$, $T_J = 0^\circ\text{C}$ to $+125^\circ\text{C}$ unless otherwise noted).

Characteristic	Symbol	MC7809CT			Unit
		Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	8.65	9.0	9.35	Vdc
Output Voltage ($5.0\text{ mA} \leq I_O \leq 1.0\text{ A}$, $P_O \leq 15\text{ W}$) $11.5\text{ Vdc} \leq V_{in} \leq 24\text{ Vdc}$	V_O	8.55	9.0	9.45	Vdc
Line Regulation ($T_J = +25^\circ\text{C}$, Note 1) $11.5\text{ Vdc} \leq V_{in} \leq 26\text{ Vdc}$ $11.5\text{ Vdc} \leq V_{in} \leq 17\text{ Vdc}$	Regline	—	12 5.0	50 25	mV
Load Regulation ($T_J = +25^\circ\text{C}$, Note 1) $5.0\text{ mA} \leq I_O \leq 1.5\text{ A}$ $250\text{ mA} \leq I_O \leq 750\text{ mA}$	Regload	— —	35 12	50 25	mV
Quiescent Current ($T_J = +25^\circ\text{C}$)	I_B	—	4.3	8.0	mA
Quiescent Current Change $11.5\text{ Vdc} \leq V_{in} \leq 26\text{ Vdc}$ $5.0\text{ mA} \leq I_O \leq 1.0\text{ A}$	ΔI_B	— —	— —	1.0 0.5	mA
Ripple Rejection $11.5\text{ Vdc} \leq V_{in} \leq 21.5\text{ Vdc}$, $f = 120\text{ Hz}$	RR	—	61	—	dB
Dropout Voltage ($I_O = 1.0\text{ A}$, $T_J = +25^\circ\text{C}$)	$V_{in} - V_O$	—	2.0	—	Vdc
Output Noise Voltage ($T_A = +25^\circ\text{C}$) $10\text{ Hz} \leq f \leq 100\text{ kHz}$	V_n	—	10	—	$\mu\text{V}/V_O$
Output Resistance $f = 1.0\text{ kHz}$	r_O	—	18	—	$\text{m}\Omega$
Short-Circuit Current Limit ($T_A = +25^\circ\text{C}$) $V_{in} = 35\text{ Vdc}$	I_{sc}	—	0.2	—	A
Peak Output Current ($T_J = +25^\circ\text{C}$)	I_{max}	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	-1.0	—	$\text{mV}/^\circ\text{C}$

NOTE 1: Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7800 Series

MC7812, B, C

ELECTRICAL CHARACTERISTICS ($V_{in} = 19\text{ V}$, $I_O = 500\text{ mA}$, $T_J = T_{low}$ to T_{high} [Note 1] unless otherwise noted)

Characteristic	Symbol	MC7812			MC7812B			MC7812C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	11.5	12	12.5	11.5	12	12.5	11.5	12	12.5	Vdc
Output Voltage ($5.0\text{ mA} \leq I_O \leq 1.0\text{ A}$, $P_O \leq 15\text{ W}$) $14.5\text{ Vdc} \leq V_{in} \leq 27\text{ Vdc}$ $15.5\text{ Vdc} \leq V_{in} \leq 27\text{ Vdc}$	V_O	—	—	—	—	—	—	11.4	12	12.6	Vdc
Line Regulation ($T_J = +25^\circ\text{C}$, Note 2) $14.5\text{ Vdc} \leq V_{in} \leq 30\text{ Vdc}$ $16\text{ Vdc} \leq V_{in} \leq 22\text{ Vdc}$	Reg_{line}	—	5.0	120	—	13	240	—	13	240	mV
Load Regulation ($T_J = +25^\circ\text{C}$, Note 2) $5.0\text{ mA} \leq I_O \leq 1.5\text{ A}$ $250\text{ mA} \leq I_O \leq 750\text{ mA}$	Reg_{load}	—	30	120	—	46	240	—	46	240	mV
Quiescent Current ($T_J = +25^\circ\text{C}$)	I_B	—	3.4	6.0	—	4.4	8.0	—	4.4	8.0	mA
Quiescent Current Change $14.5\text{ Vdc} \leq V_{in} \leq 30\text{ Vdc}$ $15\text{ Vdc} \leq V_{in} \leq 30\text{ Vdc}$ $5.0\text{ mA} \leq I_O \leq 1.0\text{ A}$	ΔI_B	—	—	—	—	—	—	—	—	1.0	mA
Ripple Rejection $15\text{ Vdc} \leq V_{in} \leq 25\text{ Vdc}$, $f = 120\text{ Hz}$	RR	61	68	—	—	60	—	—	60	—	dB
Dropout Voltage ($I_O = 1.0\text{ A}$, $T_J = +25^\circ\text{C}$)	$V_{in} - V_O$	—	2.0	2.5	—	2.0	—	—	2.0	—	Vdc
Output Noise Voltage ($T_A = +25^\circ\text{C}$) $10\text{ Hz} \leq f \leq 100\text{ kHz}$	V_n	—	10	40	—	10	—	—	10	—	$\mu\text{V}/V_O$
Output Resistance ($f = 1.0\text{ kHz}$)	r_O	—	18	—	—	18	—	—	18	—	m Ω
Short-Circuit Current Limit ($T_A = +25^\circ\text{C}$) $V_{in} = 35\text{ Vdc}$	I_{sc}	—	0.2	1.2	—	0.2	—	—	0.2	—	A
Peak Output Current ($T_J = +25^\circ\text{C}$)	I_{max}	1.3	2.5	3.3	—	2.2	—	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	± 1.5	—	—	-1.0	—	—	-1.0	—	mV/ $^\circ\text{C}$

MC7812A, AC

ELECTRICAL CHARACTERISTICS ($V_{in} = 19\text{ V}$, $I_O = 1.0\text{ A}$, $T_J = T_{low}$ to T_{high} [Note 1] unless otherwise noted)

Characteristics	Symbol	MC7812A			MC7812AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	11.75	12	12.25	11.75	12	12.25	Vdc
Output Voltage ($5.0\text{ mA} \leq I_O \leq 1.0\text{ A}$, $P_O \leq 15\text{ W}$) $14.8\text{ Vdc} \leq V_{in} \leq 27\text{ Vdc}$	V_O	11.5	12	12.5	11.5	12	12.5	Vdc
Line Regulation (Note 2) $14.8\text{ Vdc} \leq V_{in} \leq 30\text{ Vdc}$, $I_O = 500\text{ mA}$ $16\text{ Vdc} \leq V_{in} \leq 22\text{ Vdc}$ $16\text{ Vdc} \leq V_{in} \leq 22\text{ Vdc}$, $T_J = +25^\circ\text{C}$ $14.5\text{ Vdc} \leq V_{in} \leq 27\text{ Vdc}$, $T_J = +25^\circ\text{C}$	Reg_{line}	—	5.0	18	—	13	120	mV
Load Regulation (Note 2) $5.0\text{ mA} \leq I_O \leq 1.5\text{ A}$, $T_J = +25^\circ\text{C}$ $5.0\text{ mA} \leq I_O \leq 1.0\text{ A}$ $250\text{ mA} \leq I_O \leq 750\text{ mA}$, $T_J = +25^\circ\text{C}$ $250\text{ mA} \leq I_O \leq 750\text{ mA}$	Reg_{load}	—	2.0	25	—	46	100	mV
Quiescent Current $T_J = +25^\circ\text{C}$	I_B	—	—	5.0	—	—	6.0	mA
Quiescent Current Change $15\text{ Vdc} \leq V_{in} \leq 30\text{ Vdc}$, $I_O = 500\text{ mA}$ $14.8\text{ Vdc} \leq V_{in} \leq 27\text{ Vdc}$, $T_J = +25^\circ\text{C}$ $5.0\text{ mA} \leq I_O \leq 1.0\text{ A}$	ΔI_B	—	0.3	0.5	—	—	0.8	mA
Ripple Rejection $15\text{ Vdc} \leq V_{in} \leq 25\text{ Vdc}$, $f = 120\text{ Hz}$, $T_J = +25^\circ\text{C}$ $15\text{ Vdc} \leq V_{in} \leq 25\text{ Vdc}$, $f = 120\text{ Hz}$, $I_O = 500\text{ mA}$	RR	61	68	—	—	60	—	dB
Dropout Voltage ($I_O = 1.0\text{ A}$, $T_J = +25^\circ\text{C}$)	$V_{in} - V_O$	—	2.0	2.5	—	2.0	—	Vdc
Output Noise Voltage ($T_A = +25^\circ\text{C}$) $10\text{ Hz} \leq f \leq 100\text{ kHz}$	V_n	—	10	40	—	10	—	$\mu\text{V}/V_O$
Output Resistance ($f = 1.0\text{ kHz}$)	r_O	—	2.0	—	—	18	—	m Ω
Short-Circuit Current Limit ($T_A = +25^\circ\text{C}$) $V_{in} = 35\text{ Vdc}$	I_{sc}	—	0.2	1.2	—	0.2	—	A
Peak Output Current ($T_J = +25^\circ\text{C}$)	I_{max}	1.3	2.5	3.3	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	± 1.5	—	—	-1.0	—	mV/ $^\circ\text{C}$

NOTES 1. $T_{low} = -55^\circ\text{C}$ for MC78XX, A
 $= 0^\circ$ for MC78XXC, AC
 $= -40^\circ\text{C}$ for MC78XXB
 $T_{high} = +150^\circ\text{C}$ for MC78XX, A
 $= +125^\circ\text{C}$ for MC78XXC, AC, B

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7800 Series

MC7815, 8, C

ELECTRICAL CHARACTERISTICS ($V_{in} = 23 \text{ V}$, $I_O = 500 \text{ mA}$, $T_J = T_{low}$ to T_{high} [Note 1] unless otherwise noted).

Characteristic	Symbol	MC7815			MC7815B			MC7815C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	14.4	15	15.6	14.4	15	15.6	14.4	15	15.6	Vdc
Output Voltage ($5.0 \text{ mA} \leq I_O \leq 1.0 \text{ A}$, $P_O \leq 15 \text{ W}$) $17.5 \text{ Vdc} \leq V_{in} \leq 30 \text{ Vdc}$ $18.5 \text{ Vdc} \leq V_{in} \leq 30 \text{ Vdc}$	V_O	—	—	—	—	—	—	14.25	15	15.75	Vdc
Line Regulation ($T_J = +25^\circ\text{C}$, Note 2) $17.5 \text{ Vdc} \leq V_{in} \leq 30 \text{ Vdc}$ $20 \text{ Vdc} \leq V_{in} \leq 26 \text{ Vdc}$	Reg_{line}	—	6.0	150	—	13	300	—	13	300	mV
Load Regulation ($T_J = +25^\circ\text{C}$, Note 2) $5.0 \text{ mA} \leq I_O \leq 1.5 \text{ A}$ $250 \text{ mA} \leq I_O \leq 750 \text{ mA}$	Reg_{load}	—	32	150	—	52	300	—	52	300	mV
Quiescent Current ($T_J = +25^\circ\text{C}$)	I_B	—	3.4	6.0	—	4.4	8.0	—	4.4	8.0	mA
Quiescent Current Change $17.5 \text{ Vdc} \leq V_{in} \leq 30 \text{ Vdc}$ $18.5 \text{ Vdc} \leq V_{in} \leq 30 \text{ Vdc}$ $5.0 \text{ mA} \leq I_O \leq 1.0 \text{ A}$	ΔI_B	—	0.3	0.8	—	1.0	—	—	1.0	—	mA
Ripple Rejection $18.5 \text{ Vdc} \leq V_{in} \leq 28.5 \text{ Vdc}$, $f = 120 \text{ Hz}$	RR	60	66	—	—	58	—	—	58	—	dB
Dropout Voltage ($I_O = 1.0 \text{ A}$, $T_J = +25^\circ\text{C}$)	$V_{in} - V_O$	—	2.0	2.5	—	2.0	—	—	2.0	—	Vdc
Output Noise Voltage ($T_A = +25^\circ\text{C}$) $10 \text{ Hz} \leq f \leq 100 \text{ kHz}$	V_n	—	10	40	—	10	—	—	10	—	$\mu\text{V}/V_O$
Output Resistance ($f = 1.0 \text{ kHz}$)	r_O	—	19	—	—	19	—	—	19	—	m Ω
Short-Circuit Current Limit ($T_A = +25^\circ\text{C}$) $V_{in} = 35 \text{ Vdc}$	I_{sc}	—	0.2	1.2	—	0.2	—	—	0.2	—	A
Peak Output Current ($T_J = +25^\circ\text{C}$)	I_{max}	1.3	2.5	3.3	—	2.2	—	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	± 1.8	—	—	-1.0	—	—	-1.0	—	mV/ $^\circ\text{C}$

MC7815A, AC

ELECTRICAL CHARACTERISTICS ($V_{in} = 23 \text{ V}$, $I_O = 1.0 \text{ A}$, $T_J = T_{low}$ to T_{high} [Note 1] unless otherwise noted)

Characteristics	Symbol	MC7815A			MC7815AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	14.7	15	15.3	14.7	15	15.3	Vdc
Output Voltage ($5.0 \text{ mA} \leq I_O \leq 1.0 \text{ A}$, $P_O \leq 15 \text{ W}$) $17.9 \text{ Vdc} \leq V_{in} \leq 30 \text{ Vdc}$	V_O	14.4	15	15.6	14.4	15	15.6	Vdc
Line Regulation (Note 2) $17.9 \text{ Vdc} \leq V_{in} \leq 30 \text{ Vdc}$, $I_O = 500 \text{ mA}$ $20 \text{ Vdc} \leq V_{in} \leq 26 \text{ Vdc}$ $20 \text{ Vdc} \leq V_{in} \leq 26 \text{ Vdc}$, $T_J = +25^\circ\text{C}$ $17.5 \text{ Vdc} \leq V_{in} \leq 30 \text{ Vdc}$, $T_J = +25^\circ\text{C}$	Reg_{line}	—	6.0	22	—	13	150	mV
Load Regulation (Note 2) $5.0 \text{ mA} \leq I_O \leq 1.5 \text{ A}$, $T_J = +25^\circ\text{C}$ $5.0 \text{ mA} \leq I_O \leq 1.0 \text{ A}$ $250 \text{ mA} \leq I_O \leq 750 \text{ mA}$, $T_J = +25^\circ\text{C}$ $250 \text{ mA} \leq I_O \leq 750 \text{ mA}$	Reg_{load}	—	2.0	25	—	52	100	mV
Quiescent Current $T_J = +25^\circ\text{C}$	I_B	—	3.4	4.5	—	4.4	6.0	mA
Quiescent Current Change $17.5 \text{ Vdc} \leq V_{in} \leq 30 \text{ Vdc}$, $I_O = 500 \text{ mA}$ $17.5 \text{ Vdc} \leq V_{in} \leq 30 \text{ Vdc}$, $T_J = +25^\circ\text{C}$ $5.0 \text{ mA} \leq I_O \leq 1.0 \text{ A}$	ΔI_B	—	0.3	0.5	—	—	0.8	mA
Ripple Rejection $18.5 \text{ Vdc} \leq V_{in} \leq 28.5 \text{ Vdc}$, $f = 120 \text{ Hz}$, $T_J = +25^\circ\text{C}$ $18.5 \text{ Vdc} \leq V_{in} \leq 28.5 \text{ Vdc}$, $f = 120 \text{ Hz}$, $I_O = 500 \text{ mA}$	RR	60	66	—	—	—	—	dB
Dropout Voltage ($I_O = 1.0 \text{ A}$, $T_J = +25^\circ\text{C}$)	$V_{in} - V_O$	—	2.0	2.5	—	2.0	—	Vdc
Output Noise Voltage ($T_A = +25^\circ\text{C}$) $10 \text{ Hz} \leq f \leq 100 \text{ kHz}$	V_n	—	10	40	—	10	—	$\mu\text{V}/V_O$
Output Resistance ($f = 1.0 \text{ kHz}$)	r_O	—	2.0	—	—	19	—	m Ω
Short-Circuit Current Limit ($T_A = +25^\circ\text{C}$) $V_{in} = 35 \text{ Vdc}$	I_{sc}	—	0.2	1.2	—	0.2	—	A
Peak Output Current ($T_J = +25^\circ\text{C}$)	I_{max}	1.3	2.5	3.3	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	± 1.8	—	—	-1.0	—	mV/ $^\circ\text{C}$

NOTES 1 $T_{low} = -55^\circ\text{C}$ for MC78XX, A
 $= 0^\circ\text{C}$ for MC78XXC, AC
 $= -40^\circ\text{C}$ for MC78XXB
 $T_{high} = +150^\circ\text{C}$ for MC78XX, A
 $= +125^\circ\text{C}$ for MC78XXC, AC, B

2 Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7800 Series

MC7818, B, C

ELECTRICAL CHARACTERISTICS ($V_{in} = 27\text{ V}$, $I_O = 500\text{ mA}$, $T_J = T_{low}$ to T_{high} [Note 1] unless otherwise noted).

Characteristic	Symbol	MC7818			MC7818B			MC7818C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	17.3	18	18.7	17.3	18	18.7	17.3	18	18.7	Vdc
Output Voltage ($5.0\text{ mA} \leq I_O \leq 1.0\text{ A}$, $P_O \leq 15\text{ W}$) $21\text{ Vdc} \leq V_{in} \leq 33\text{ Vdc}$ $22\text{ Vdc} \leq V_{in} \leq 33\text{ Vdc}$	V_O	— 17.1	— 18	— 18.9	— 17.1	— 18	— 18.9	17.1 —	18 —	18.9 —	Vdc
Line Regulation ($T_J = +25^\circ\text{C}$, Note 2) $21\text{ Vdc} \leq V_{in} \leq 33\text{ Vdc}$ $24\text{ Vdc} \leq V_{in} \leq 30\text{ Vdc}$	Regline	— —	7.0 4.0	180 90	— —	25 10	360 180	— —	25 10	360 180	mV
Load Regulation ($T_J = +25^\circ\text{C}$, Note 2) $5.0\text{ mA} \leq I_O \leq 1.5\text{ A}$ $250\text{ mA} \leq I_O \leq 750\text{ mA}$	Regload	— —	35 12	180 90	— —	55 22	360 180	— —	55 22	360 180	mV
Quiescent Current ($T_J = +25^\circ\text{C}$)	I_B	—	3.5	6.0	—	4.5	8.0	—	4.5	8.0	mA
Quiescent Current Change $21\text{ Vdc} \leq V_{in} \leq 33\text{ Vdc}$ $22\text{ Vdc} \leq V_{in} \leq 33\text{ Vdc}$ $5.0\text{ mA} \leq I_O \leq 1.0\text{ A}$	ΔI_B	— — —	— 0.3 0.04	— 0.8 0.5	— — —	— — —	— 1.0 0.5	— — —	— — —	1.0 — 0.5	mA
Ripple Rejection $22\text{ Vdc} \leq V_{in} \leq 33\text{ Vdc}$, $f = 120\text{ Hz}$	RR	59	65	—	—	57	—	—	57	—	dB
Dropout Voltage ($I_O = 1.0\text{ A}$, $T_J = +25^\circ\text{C}$)	$V_{in}-V_O$	—	2.0	2.5	—	2.0	—	—	2.0	—	Vdc
Output Noise Voltage ($T_A = +25^\circ\text{C}$) $10\text{ Hz} \leq f \leq 100\text{ kHz}$	V_n	—	10	40	—	10	—	—	10	—	$\mu\text{V}/V_O$
Output Resistance $f = 1.0\text{ kHz}$	r_O	—	19	—	—	19	—	—	19	—	m Ω
Short-Circuit Current Limit ($T_A = +25^\circ\text{C}$) $V_{in} = 35\text{ Vdc}$	I_{sc}	—	0.2	1.2	—	0.2	—	—	0.2	—	A
Peak Output Current ($T_J = +25^\circ\text{C}$)	I_{max}	1.3	2.5	3.3	—	2.2	—	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCVO	—	± 2.3	—	—	-1.0	—	—	-1.0	—	mV/ $^\circ\text{C}$

MC7818AC

ELECTRICAL CHARACTERISTICS ($V_{in} = 27\text{ V}$, $I_O = 1.0\text{ A}$, $T_J = T_{low}$ to T_{high} [Note 1] unless otherwise noted).

Characteristics	Symbol	MC7818AC			Unit
		Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	17.64	18	18.36	Vdc
Output Voltage ($5.0\text{ mA} \leq I_O \leq 1.0\text{ A}$, $P_O \leq 15\text{ W}$) $21\text{ Vdc} \leq V_{in} \leq 33\text{ Vdc}$	V_O	17.3	18	18.7	Vdc
Line Regulation (Note 2) $21\text{ Vdc} \leq V_{in} \leq 33\text{ Vdc}$, $I_O = 500\text{ mA}$ $24\text{ Vdc} \leq V_{in} \leq 30\text{ Vdc}$ $24\text{ Vdc} \leq V_{in} \leq 30\text{ Vdc}$, $T_J = +25^\circ\text{C}$ $20.6\text{ Vdc} \leq V_{in} \leq 33\text{ Vdc}$, $T_J = +25^\circ\text{C}$	Regline	— — — —	25 28 10 25	180 180 90 180	mV
Load Regulation (Note 2) $5.0\text{ mA} \leq I_O \leq 1.5\text{ A}$, $T_J = +25^\circ\text{C}$ $5.0\text{ mA} \leq I_O \leq 1.0\text{ A}$ $250\text{ mA} \leq I_O \leq 750\text{ mA}$, $T_J = +25^\circ\text{C}$ $250\text{ mA} \leq I_O \leq 750\text{ mA}$	Regload	— — — —	55 55 — 22	100 100 — 50	mV
Quiescent Current $T_J = +25^\circ\text{C}$	I_B	— —	— 4.5	6.0 6.0	mA
Quiescent Current Change $21\text{ Vdc} \leq V_{in} \leq 33\text{ Vdc}$, $I_O = 500\text{ mA}$ $21\text{ Vdc} \leq V_{in} \leq 33\text{ Vdc}$, $T_J = +25^\circ\text{C}$ $5.0\text{ mA} \leq I_O \leq 1.0\text{ A}$	ΔI_B	— — —	— — —	0.8 0.8 0.5	mA
Ripple Rejection $22\text{ Vdc} \leq V_{in} \leq 32\text{ Vdc}$, $f = 120\text{ Hz}$, $T_J = +25^\circ\text{C}$ $22\text{ Vdc} \leq V_{in} \leq 32\text{ Vdc}$, $f = 120\text{ Hz}$, $I_O = 500\text{ mA}$	RR	— —	— 57	— —	dB
Dropout Voltage ($I_O = 1.0\text{ A}$, $T_J = +25^\circ\text{C}$)	$V_{in}-V_O$	—	2.0	—	Vdc
Output Noise Voltage ($T_A = +25^\circ\text{C}$) $10\text{ Hz} \leq f \leq 100\text{ kHz}$	V_n	—	10	—	$\mu\text{V}/V_O$
Output Resistance ($f = 1.0\text{ kHz}$)	r_O	—	19	—	m Ω
Short-Circuit Current Limit ($T_A = +25^\circ\text{C}$) $V_{in} = 35\text{ Vdc}$	I_{sc}	—	0.2	—	A
Peak Output Current ($T_J = +25^\circ\text{C}$)	I_{max}	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCVO	—	-1.0	—	mV/ $^\circ\text{C}$

NOTES: 1. $T_{low} = -55^\circ\text{C}$ for MC78XX, $T_{high} = +150^\circ\text{C}$ for MC78XX
 $= 0^\circ\text{C}$ for MC78XXC, AC
 $= -40^\circ\text{C}$ for MC78XXB

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7800 Series

MC7824, B, C

ELECTRICAL CHARACTERISTICS ($V_{in} = 33 \text{ V}$, $I_O = 500 \text{ mA}$, $T_J = T_{low} \text{ to } T_{high}$ [Note 1] unless otherwise noted).

Characteristic	Symbol	MC7824			MC7824B			MC7824C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	23	24	25	23	24	25	23	24	25	Vdc
Output Voltage ($5.0 \text{ mA} \leq I_O \leq 1.0 \text{ A}$, $P_O \leq 15 \text{ W}$) $27 \text{ Vdc} \leq V_{in} \leq 38 \text{ Vdc}$ $28 \text{ Vdc} \leq V_{in} \leq 38 \text{ Vdc}$	V_O	—	—	—	—	—	—	—	—	—	Vdc
Line Regulation ($T_J = +25^\circ\text{C}$, Note 2) $27 \text{ Vdc} \leq V_{in} \leq 38 \text{ Vdc}$ $30 \text{ Vdc} \leq V_{in} \leq 36 \text{ Vdc}$	Regline	—	10	240	—	31	480	—	31	480	mV
Load Regulation ($T_J = +25^\circ\text{C}$, Note 2) $5.0 \text{ mA} \leq I_O \leq 1.5 \text{ A}$ $250 \text{ mA} \leq I_O \leq 750 \text{ mA}$	Regload	—	40	240	—	60	480	—	60	480	mV
Quiescent Current ($T_J = +25^\circ\text{C}$)	I_B	—	3.6	6.0	—	4.6	8.0	—	4.6	8.0	mA
Quiescent Current Change $27 \text{ Vdc} \leq V_{in} \leq 38 \text{ Vdc}$ $28 \text{ Vdc} \leq V_{in} \leq 38 \text{ Vdc}$ $5.0 \text{ mA} \leq I_O \leq 1.0 \text{ A}$	ΔI_B	—	—	—	—	—	—	—	—	—	mA
Ripple Rejection $28 \text{ Vdc} \leq V_{in} \leq 38 \text{ Vdc}$, $f = 120 \text{ Hz}$	RR	56	62	—	54	—	—	54	—	—	dB
Dropout Voltage ($I_O = 1.0 \text{ A}$, $T_J = +25^\circ\text{C}$)	$V_{in} - V_O$	—	2.0	2.5	—	2.0	—	—	2.0	—	Vdc
Output Noise Voltage ($T_A = +25^\circ\text{C}$) $10 \text{ Hz} \leq f \leq 100 \text{ kHz}$	V_n	—	10	40	—	10	—	—	10	—	$\mu\text{V}/V_O$
Output Resistance $f = 1.0 \text{ kHz}$	r_O	—	20	—	—	20	—	—	20	—	m Ω
Short-Circuit Current Limit ($T_A = +25^\circ\text{C}$) $V_{in} = 35 \text{ Vdc}$	I_{sc}	—	0.2	1.2	—	0.2	—	—	0.2	—	A
Peak Output Current ($T_J = +25^\circ\text{C}$)	I_{max}	1.3	2.5	3.3	—	2.2	—	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	± 3.0	—	—	-1.5	—	—	-1.5	—	$\text{mV}/^\circ\text{C}$

MC7824AC

ELECTRICAL CHARACTERISTICS ($V_{in} = 33 \text{ V}$, $I_O = 1.0 \text{ A}$, $T_J = T_{low} \text{ to } T_{high}$ [Note 1] unless otherwise noted).

Characteristics	Symbol	MC7824AC			Unit
		Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	23.5	24	24.5	Vdc
Output Voltage ($5.0 \text{ mA} \leq I_O \leq 1.0 \text{ A}$, $P_O \leq 15 \text{ W}$) $27.3 \text{ Vdc} \leq V_{in} \leq 38 \text{ Vdc}$	V_O	23	24	25	Vdc
Line Regulation (Note 2) $27 \text{ Vdc} \leq V_{in} \leq 38 \text{ Vdc}$, $I_O = 500 \text{ mA}$ $30 \text{ Vdc} \leq V_{in} \leq 36 \text{ Vdc}$ $30 \text{ Vdc} \leq V_{in} \leq 36 \text{ Vdc}$, $T_J = +25^\circ\text{C}$ $26.7 \text{ Vdc} \leq V_{in} \leq 38 \text{ Vdc}$, $T_J = +25^\circ\text{C}$	Regline	—	31	240	mV
Load Regulation (Note 2) $5.0 \text{ mA} \leq I_O \leq 1.5 \text{ A}$, $T_J = +25^\circ\text{C}$ $5.0 \text{ mA} \leq I_O \leq 1.0 \text{ A}$ $250 \text{ mA} \leq I_O \leq 750 \text{ mA}$, $T_J = +25^\circ\text{C}$ $250 \text{ mA} \leq I_O \leq 750 \text{ mA}$	Regload	—	60	100	mV
Quiescent Current $T_J = +25^\circ\text{C}$	I_B	—	—	6.0	mA
Quiescent Current Change $27.3 \text{ Vdc} \leq V_{in} \leq 38 \text{ Vdc}$, $I_O = 500 \text{ mA}$ $27.3 \text{ Vdc} \leq V_{in} \leq 38 \text{ Vdc}$, $T_J = +25^\circ\text{C}$ $5.0 \text{ mA} \leq I_O \leq 1.0 \text{ A}$	ΔI_B	—	—	0.8	mA
Ripple Rejection $28 \text{ Vdc} \leq V_{in} \leq 38 \text{ Vdc}$, $f = 120 \text{ Hz}$, $T_J = +25^\circ\text{C}$ $28 \text{ Vdc} \leq V_{in} \leq 38 \text{ Vdc}$, $f = 120 \text{ Hz}$, $I_O = 500 \text{ mA}$	RR	—	54	—	dB
Dropout Voltage ($I_O = 1.0 \text{ A}$, $T_J = +25^\circ\text{C}$)	$V_{in} - V_O$	—	2.0	—	Vdc
Output Noise Voltage ($T_A = +25^\circ\text{C}$) $10 \text{ Hz} \leq f \leq 100 \text{ kHz}$	V_n	—	10	—	$\mu\text{V}/V_O$
Output Resistance ($f = 1.0 \text{ kHz}$)	r_O	—	20	—	m Ω
Short-Circuit Current Limit ($T_A = +25^\circ\text{C}$) $V_{in} = 35 \text{ Vdc}$	I_{sc}	—	0.2	—	A
Peak Output Current ($T_J = +25^\circ\text{C}$)	I_{max}	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	-1.5	—	$\text{mV}/^\circ\text{C}$

NOTES: 1. $T_{low} = -55^\circ\text{C}$ for MC78XX
 $= 0^\circ$ for MC78XXC, AC
 $= -40^\circ\text{C}$ for MC78XXB
 $T_{high} = +150^\circ\text{C}$ for MC78XX
 $= +125^\circ\text{C}$ for MC78XXC, AC, B

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7800 Series

TYPICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 1 — WORST CASE POWER DISSIPATION
versus AMBIENT TEMPERATURE (Case 221A)

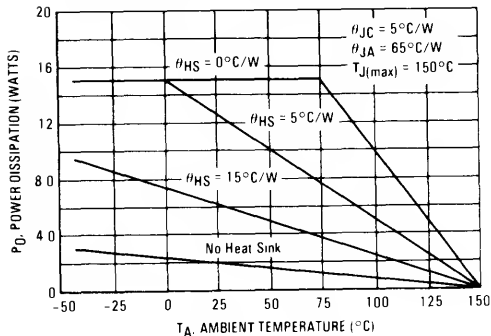


FIGURE 2 — WORST CASE POWER DISSIPATION
versus AMBIENT TEMPERATURE (Case 1)

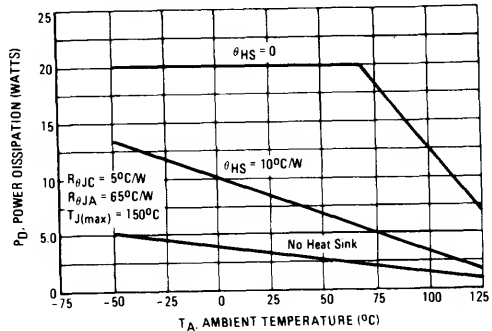


FIGURE 3 — INPUT OUTPUT DIFFERENTIAL AS A
FUNCTION OF JUNCTION TEMPERATURE
(MC78XXC, AC, B)

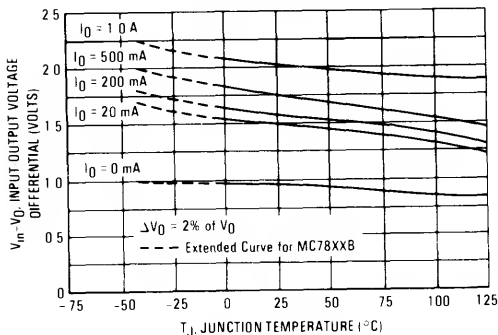


FIGURE 4 — INPUT OUTPUT DIFFERENTIAL AS A
FUNCTION OF JUNCTION TEMPERATURE
(MC78XX, A)

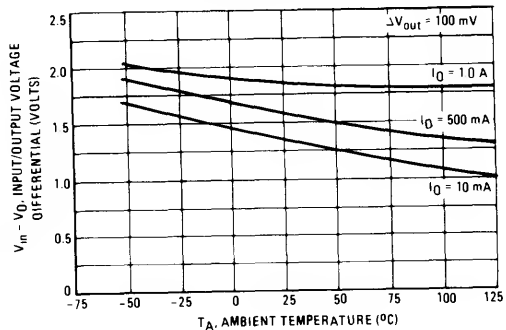


FIGURE 5 — PEAK OUTPUT CURRENT AS A FUNCTION
OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE
(MC78XXC, AC, B)

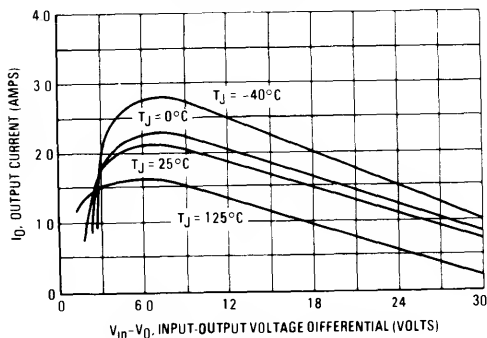
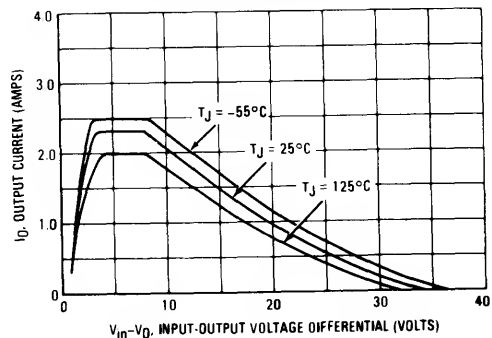


FIGURE 6 — PEAK OUTPUT CURRENT AS A
FUNCTION OF INPUT-OUTPUT DIFFERENTIAL
VOLTAGE (MC78XX, A)



MC7800 Series

TYPICAL CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise noted.)

FIGURE 7 — RIPPLE REJECTION AS A FUNCTION OF OUTPUT VOLTAGES (MC78XXC, AC)

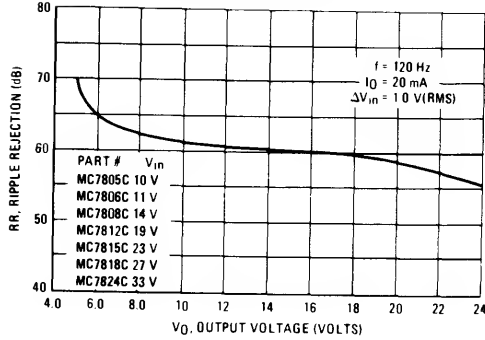


FIGURE 8 — RIPPLE REJECTION AS A FUNCTION OF FREQUENCY (MC78XXC, AC, A)

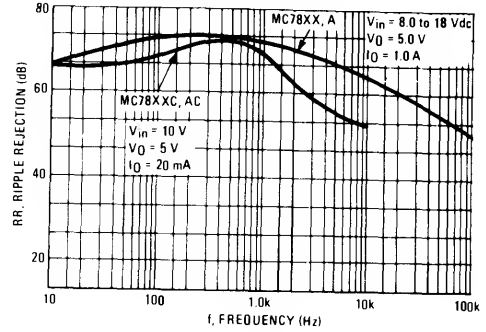


FIGURE 9 — OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE (MC78XXC, AC, B)

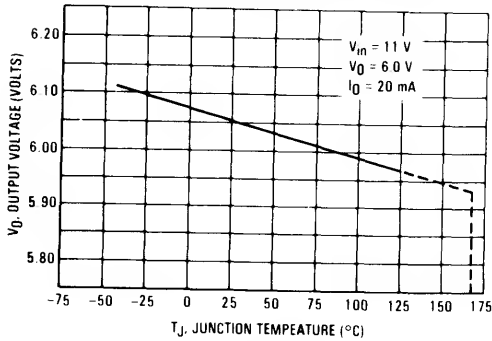


FIGURE 10 — OUTPUT IMPEDANCE AS A FUNCTION OF OUTPUT VOLTAGE (MC78XXC, AC)

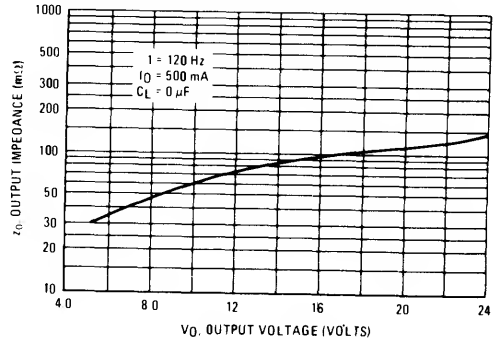


FIGURE 11 — QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE (MC78XXC, AC, B)

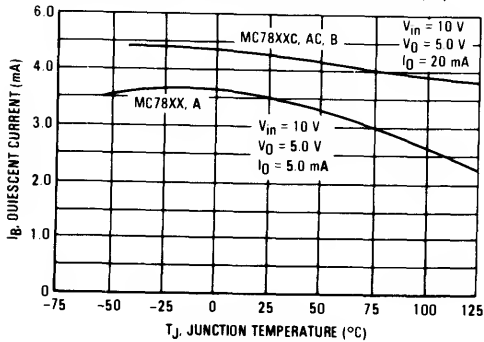
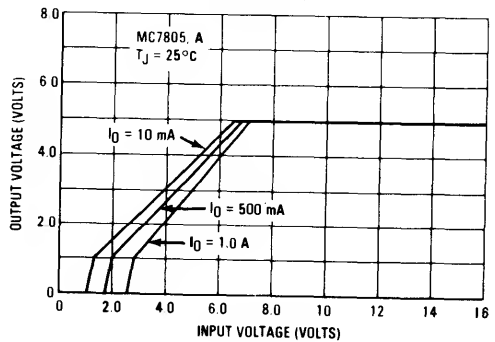


FIGURE 12 — DROPOUT CHARACTERISTICS (MC78XX, A)



MC7800 Series

APPLICATIONS INFORMATION

Design Considerations

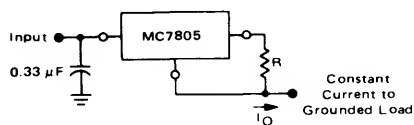
The MC7800 Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected

to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

3

FIGURE 13 – CURRENT REGULATOR



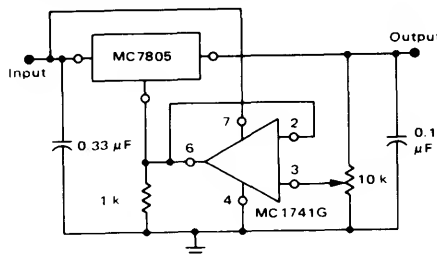
The MC7800 regulators can also be used as a current source when connected as above. In order to minimize dissipation the MC7805C is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5V}{R} + I_Q$$

$$I_Q \approx 1.5 \text{ mA over line and load changes}$$

For example, a 1-ampere current source would require R to be a 5-ohm, 10-W resistor and the output voltage compliance would be the input voltage less 7 volts

FIGURE 14 – ADJUSTABLE OUTPUT REGULATOR

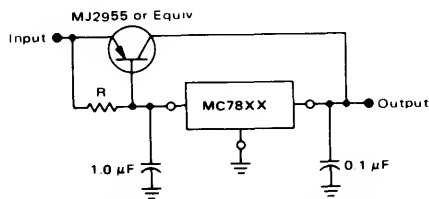


$$V_O, 7.0 \text{ V to } 20 \text{ V}$$

$$V_{IN} V_O \geq 2.0 \text{ V}$$

The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 2.0 volts greater than the regulator voltage.

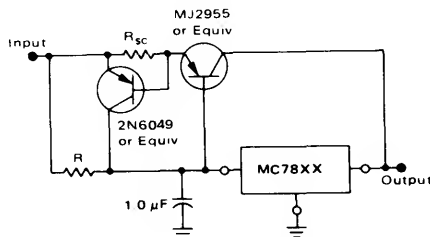
FIGURE 15 – CURRENT BOOST REGULATOR



XX = 2 digits of type number indicating voltage.

The MC7800 series can be current boosted with a PNP transistor. The MJ2955 provides current to 5.0 amperes. Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short-circuit proof. Input-output differential voltage minimum is increased by V_{BE} of the pass transistor.

FIGURE 16 – SHORT-CIRCUIT PROTECTION



XX = 2 digits of type number indicating voltage.

The circuit of Figure 15 can be modified to provide supply protection against short circuits by adding a short-circuit sense resistor, R_{SC} , and an additional PNP transistor. The current sensing PNP must be able to handle the short-circuit current of the three-terminal regulator. Therefore, a four-ampere plastic power transistor is specified.

3

The MC78L00 Series of positive voltage regulators are inexpensive, easy-to-use devices suitable for a multitude of applications that require a regulated supply of up to 100 mA. Like their higher powered MC7800 and MC78M00 Series cousins, these regulators feature internal current limiting and thermal shutdown making them remarkably rugged. No external components are required with the MC78L00 devices in many applications.

- Wide Range of Available, Fixed Output Voltages
- Low Cost
- Internal Short Circuit Current Limiting
- Internal Thermal Overload Protection
- No External Components Required
- Complementary Negative Regulators Offered (MC79L00 Series)
- Available in Either $\pm 5\%$ (AC) or $\pm 10\%$ (C) Selections



*Available in 5, 8, 12 and 15 volt devices.

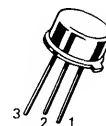
MC78L00,A Series

THREE-TERMINAL LOW CURRENT POSITIVE FIXED VOLTAGE REGULATORS

PIN 1. OUTPUT
2. GROUND
3. INPUT



PIN 1. INPUT
2. OUTPUT



(Bottom View)
(Case Connected To Pin 3)

PIN 1. VOUT	5 NC
2. GND	6 GND
3. GND	7. GND
4 NC	8. VIN

SOP-8 is an internally modified SO-8 Package. Pins 2, 3, 6 and 7 are electrically common to the die attach flag. This internal lead frame modification decreases package thermal resistance and increases power dissipation capability when appropriately mounted on a printed circuit board. SOP-8 conforms to all external dimensions of the standard SO-8 Package.

Device No. 10%	Device No. 5%	Nominal Voltage
MC78L05C	MC78L05AC	5.0
MC78L08C	MC78L08AC	8.0
MC78L12C	MC78L12AC	12
MC78L15C	MC78L15AC	15
MC78L18C	MC78L18AC	18
MC78L24C	MC78L24AC	24

MC78L00,A Series

MAXIMUM RATINGS ($T_A = +125^\circ\text{C}$ unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (2.6 V–8.0 V) (12 V–18 V) (24 V)	V_I	30 35 40	Vdc
Storage Junction Temperature Range	T_{stg}	–65 to +150	$^\circ\text{C}$
Operating Junction Temperature Range	T_J	0 to +150	$^\circ\text{C}$

MC78L05C, MC78L05AC ELECTRICAL CHARACTERISTICS ($V_I = 10\text{ V}$, $I_O = 40\text{ mA}$, $C_I = 0.33\text{ }\mu\text{F}$, $C_O = 0.1\text{ }\mu\text{F}$,
 $0^\circ\text{C} < T_J < +125^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	MC78L05AC			MC78L05C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	4.8	5.0	5.2	4.6	5.0	5.4	Vdc
Line Regulation ($T_J = +25^\circ\text{C}$, $I_O = 40\text{ mA}$) $7.0\text{ Vdc} \leq V_I \leq 20\text{ Vdc}$ $8.0\text{ Vdc} \leq V_I \leq 20\text{ Vdc}$	Regline	— —	55 45	150 100	— —	55 45	200 150	mV
Load Regulation ($T_J = +25^\circ\text{C}$, $1.0\text{ mA} \leq I_O \leq 100\text{ mA}$) ($T_J = +25^\circ\text{C}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$)	Regload	— —	11 5.0	60 30	— —	11 5.0	60 30	mV
Output Voltage ($7.0\text{ Vdc} \leq V_I \leq 20\text{ Vdc}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$) ($V_I = 10\text{ V}$, $1.0\text{ mA} \leq I_O \leq 70\text{ mA}$)	V_O	4.75 4.75	— —	5.25 5.25	4.5 4.5	— —	5.5 5.5	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$) ($T_J = +125^\circ\text{C}$)	I_{IB}	— —	3.8 —	6.0 5.5	— —	3.8 —	6.0 5.5	mA
Input Bias Current Change ($8.0\text{ Vdc} \leq V_I \leq 20\text{ Vdc}$) ($1.0\text{ mA} \leq I_O \leq 40\text{ mA}$)	ΔI_{IB}	— —	— —	1.5 0.1	— —	— —	1.5 0.2	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$)	V_n	—	40	—	—	40	—	μV
Ripple Rejection ($I_O = 40\text{ mA}$, $f = 120\text{ Hz}$, $8.0\text{ V} \leq V_I \leq 18\text{ V}$, $T_J = +25^\circ\text{C}$)	RR	41	49	—	40	49	—	dB
Dropout Voltage ($T_J = +25^\circ\text{C}$)	$V_I - V_O$	—	1.7	—	—	1.7	—	Vdc

MC78L08C, MC78L08AC ELECTRICAL CHARACTERISTICS ($V_I = 14\text{ V}$, $I_O = 40\text{ mA}$, $C_I = 0.33\text{ }\mu\text{F}$, $C_O = 0.1\text{ }\mu\text{F}$,
 $0^\circ\text{C} < T_J < +125^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	MC78L08AC			MC78L08C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	7.7	8.0	8.3	7.36	8.0	8.64	Vdc
Line Regulation ($T_J = +25^\circ\text{C}$, $I_O = 40\text{ mA}$) $10.5\text{ Vdc} \leq V_I \leq 23\text{ Vdc}$ $11\text{ Vdc} \leq V_I \leq 23\text{ Vdc}$	Regline	— —	20 12	175 125	— —	20 12	200 150	mV
Load Regulation ($T_J = +25^\circ\text{C}$, $1.0\text{ mA} \leq I_O \leq 100\text{ mA}$) ($T_J = +25^\circ\text{C}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$)	Regload	— —	15 8.0	80 40	— —	15 6.0	80 40	mV
Output Voltage ($10.5\text{ Vdc} \leq V_I \leq 23\text{ Vdc}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$) ($V_I = 14\text{ V}$, $1.0\text{ mA} \leq I_O \leq 70\text{ mA}$)	V_O	7.6 7.6	— —	8.4 8.4	7.2 7.2	— —	8.8 8.8	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$) ($T_J = +125^\circ\text{C}$)	I_{IB}	— —	3.0 —	6.0 5.5	— —	3.0 —	6.0 5.5	mA
Input Bias Current Change ($11\text{ Vdc} \leq V_I \leq 23\text{ Vdc}$) ($1.0\text{ mA} \leq I_O \leq 40\text{ mA}$)	ΔI_{IB}	— —	— —	1.5 0.1	— —	— —	1.5 0.2	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$)	V_n	—	60	—	—	52	—	μV
Ripple Rejection ($I_O = 40\text{ mA}$, $f = 120\text{ Hz}$, $12\text{ V} \leq V_I \leq 23\text{ V}$, $T_J = +25^\circ\text{C}$)	RR	37	57	—	36	55	—	dB
Dropout Voltage ($T_J = +25^\circ\text{C}$)	$V_I - V_O$	—	1.7	—	—	1.7	—	Vdc

MC78L00,A Series

MC78L12C, MC78L12AC ELECTRICAL CHARACTERISTICS ($V_I = 19\text{ V}$, $I_O = 40\text{ mA}$, $C_I = 0.33\text{ }\mu\text{F}$, $C_O = 0.1\text{ }\mu\text{F}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	MC78L12AC			MC78L12C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	11.5	12	12.5	11.1	12	12.9	Vdc
Line Regulation ($T_J = +25^\circ\text{C}$, $I_O = 40\text{ mA}$) $14.5\text{ Vdc} \leq V_I \leq 27\text{ Vdc}$ $16\text{ Vdc} \leq V_I \leq 27\text{ Vdc}$	Regline	—	120 100	250 200	—	120 100	250 200	mV
Load Regulation ($T_J = +25^\circ\text{C}$, $1.0\text{ mA} \leq I_O \leq 100\text{ mA}$) ($T_J = +25^\circ\text{C}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$)	Regload	—	20 10	100 50	—	20 10	100 50	mV
Output Voltage ($14.5\text{ Vdc} \leq V_I \leq 27\text{ Vdc}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$) ($V_I = 19\text{ V}$, $1.0\text{ mA} \leq I_O \leq 70\text{ mA}$)	V_O	11.4 11.4	—	12.6 12.6	10.8 10.8	—	13.2 13.2	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$) ($T_J = +125^\circ\text{C}$)	I_{IB}	—	4.2 —	6.5 6.0	—	4.2 —	6.5 6.0	mA
Input Bias Current Change ($16\text{ Vdc} \leq V_I \leq 27\text{ Vdc}$) ($1.0\text{ mA} \leq I_O \leq 40\text{ mA}$)	ΔI_{IB}	—	—	1.5 0.1	—	—	1.5 0.2	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$)	V_n	—	80	—	—	80	—	μV
Ripple Rejection ($I_O = 40\text{ mA}$, $f = 120\text{ Hz}$, $15\text{ V} \leq V_I \leq 25\text{ V}$, $T_J = +25^\circ\text{C}$)	RR	37	42	—	36	42	—	dB
Dropout Voltage ($T_J = +25^\circ\text{C}$)	$V_I - V_O$	—	1.7	—	—	1.7	—	Vdc

MC78L15C, MC78L15AC ELECTRICAL CHARACTERISTICS ($V_I = 23\text{ V}$, $I_O = 40\text{ mA}$, $C_I = 0.33\text{ }\mu\text{F}$, $C_O = 0.1\text{ }\mu\text{F}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	MC78L15AC			MC78L15C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	14.4	15	15.6	13.8	15	16.2	Vdc
Line Regulation ($T_J = +25^\circ\text{C}$, $I_O = 40\text{ mA}$) $17.5\text{ Vdc} \leq V_I \leq 30\text{ Vdc}$ $20\text{ Vdc} \leq V_I \leq 30\text{ Vdc}$	Regline	—	130 110	300 250	—	130 110	300 250	mV
Load Regulation ($T_J = +25^\circ\text{C}$, $1.0\text{ mA} \leq I_O \leq 100\text{ mA}$) ($T_J = +25^\circ\text{C}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$)	Regload	—	25 12	150 75	—	25 12	150 75	mV
Output Voltage ($17.5\text{ Vdc} \leq V_I \leq 30\text{ Vdc}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$) ($V_I = 23\text{ V}$, $1.0\text{ mA} \leq I_O \leq 70\text{ mA}$)	V_O	14.25 14.25	—	15.75 15.75	13.5 13.5	—	16.5 16.5	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$) ($T_J = +125^\circ\text{C}$)	I_{IB}	—	4.4 —	6.5 6.0	—	4.4 —	6.5 6.0	mA
Input Bias Current Change ($20\text{ Vdc} \leq V_I \leq 30\text{ Vdc}$) ($1.0\text{ mA} \leq I_O \leq 40\text{ mA}$)	ΔI_{IB}	—	—	1.5 0.1	—	—	1.5 0.2	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$)	V_n	—	90	—	—	90	—	μV
Ripple Rejection ($I_O = 40\text{ mA}$, $f = 120\text{ Hz}$, $18.5\text{ V} \leq V_I \leq 28.5\text{ V}$, $T_J = +25^\circ\text{C}$)	RR	34	39	—	33	39	—	dB
Dropout Voltage ($T_J = +25^\circ\text{C}$)	$V_I - V_O$	—	1.7	—	—	1.7	—	Vdc

MC78L00,A Series

MC78L18C, MC78L18AC ELECTRICAL CHARACTERISTICS ($V_I = 27\text{ V}$, $I_O = 40\text{ mA}$, $C_I = 0.33\text{ }\mu\text{F}$, $C_O = 0.1\text{ }\mu\text{F}$,
 $0^\circ\text{C} < T_J < +125^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	MC78L18AC			MC78L18C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	17.3	18	18.7	16.6	18	19.4	Vdc
Line Regulation ($T_J = +25^\circ\text{C}$, $I_O = 40\text{ mA}$) 21.4 Vdc $\leq V_I \leq 33\text{ Vdc}$ 20.7 Vdc $\leq V_I \leq 33\text{ Vdc}$ 22 Vdc $\leq V_I \leq 33\text{ Vdc}$ 21 Vdc $\leq V_I \leq 33\text{ Vdc}$	Regline	—	45	325	—	32	325	mV
Load Regulation ($T_J = +25^\circ\text{C}$, $1.0\text{ mA} \leq I_O \leq 100\text{ mA}$) ($T_J = +25^\circ\text{C}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$)	Regload	—	30	170	—	30	170	mV
Output Voltage (21.4 Vdc $\leq V_I \leq 33\text{ Vdc}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$) (20.7 Vdc $\leq V_I \leq 33\text{ Vdc}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$) ($V_I = 27\text{ V}$, $1.0\text{ mA} \leq I_O \leq 70\text{ mA}$) ($V_I = 27\text{ V}$, $1.0\text{ mA} \leq I_O \leq 70\text{ mA}$)	V_O	17.1	—	18.9	16.2	—	19.8	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$) ($T_J = +125^\circ\text{C}$)	I_{IB}	—	3.1	6.5	—	3.1	6.5	mA
Input Bias Current Change (22 Vdc $\leq V_I \leq 33\text{ Vdc}$) (21 Vdc $\leq V_I \leq 33\text{ Vdc}$) (1.0 mA $\leq I_O \leq 40\text{ mA}$)	ΔI_{IB}	—	—	1.5	—	—	1.5	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$)	V_n	—	150	—	—	150	—	μV
Ripple Rejection ($I_O = 40\text{ mA}$, $f = 120\text{ Hz}$, 23 V $\leq V_I \leq 33\text{ V}$, $T_J = +25^\circ\text{C}$)	RR	33	48	—	32	46	—	dB
Dropout Voltage ($T_J = +25^\circ\text{C}$)	$V_I - V_O$	—	1.7	—	—	1.7	—	Vdc

MC78L24C, MC78L24AC ELECTRICAL CHARACTERISTICS ($V_I = 33\text{ V}$, $I_O = 40\text{ mA}$, $C_I = 0.33\text{ }\mu\text{F}$, $C_O = 0.1\text{ }\mu\text{F}$,
 $0^\circ\text{C} < T_J < +125^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	MC78L24AC			MC78L24C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	23	24	25	22.1	24	25.9	Vdc
Line Regulation ($T_J = +25^\circ\text{C}$, $I_O = 40\text{ mA}$) 27.5 Vdc $\leq V_I \leq 38\text{ Vdc}$ 28 Vdc $\leq V_I \leq 80\text{ Vdc}$ 27 Vdc $\leq V_I \leq 38\text{ Vdc}$	Regline	—	—	—	—	35	350	mV
Load Regulation ($T_J = +25^\circ\text{C}$, $1.0\text{ mA} \leq I_O \leq 100\text{ mA}$) ($T_J = +25^\circ\text{C}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$)	Regload	—	40	200	—	40	200	mV
Output Voltage (28 Vdc $\leq V_I \leq 38\text{ Vdc}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$) (27 Vdc $\leq V_I \leq 38\text{ Vdc}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$) (28 Vdc $\leq V_I \leq 33\text{ V}$, $1.0\text{ mA} \leq I_O \leq 70\text{ mA}$) (27 Vdc $\leq V_I \leq 33\text{ V}$, $1.0\text{ mA} \leq I_O \leq 70\text{ mA}$)	V_O	22.8	—	25.2	21.6	—	26.4	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$) ($T_J = +125^\circ\text{C}$)	I_{IB}	—	3.1	6.5	—	3.1	6.5	mA
Input Bias Current Change (28 Vdc $\leq V_I \leq 38\text{ Vdc}$) (1.0 mA $\leq I_O \leq 40\text{ mA}$)	ΔI_{IB}	—	—	1.5	—	—	1.5	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$)	V_n	—	200	—	—	200	—	μV
Ripple Rejection ($I_O = 40\text{ mA}$, $f = 120\text{ Hz}$, $29\text{ V} \leq V_I \leq 35\text{ V}$, $T_J = +25^\circ\text{C}$)	RR	31	45	—	30	43	—	dB
Dropout Voltage ($T_J = +25^\circ\text{C}$)	$V_I - V_O$	—	1.7	—	—	1.7	—	Vdc

MC78L00,A Series

TYPICAL CHARACTERISTICS

($T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 1 – DROPOUT CHARACTERISTICS

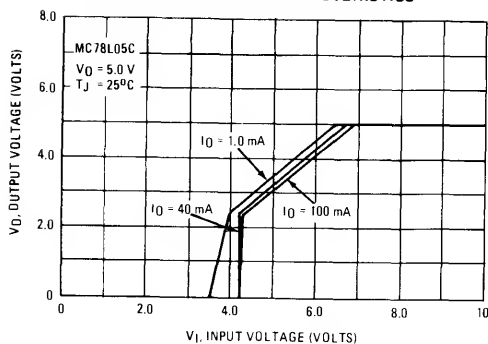


FIGURE 2 – DROPOUT VOLTAGE versus JUNCTION TEMPERATURE

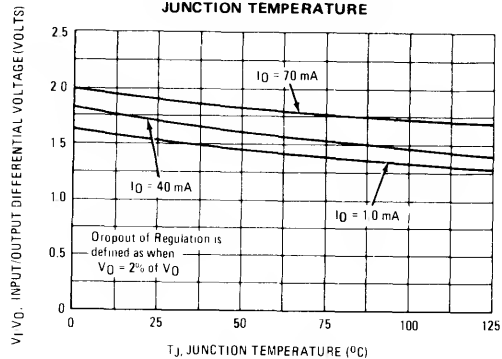


FIGURE 3 – INPUT BIAS CURRENT versus AMBIENT TEMPERATURE

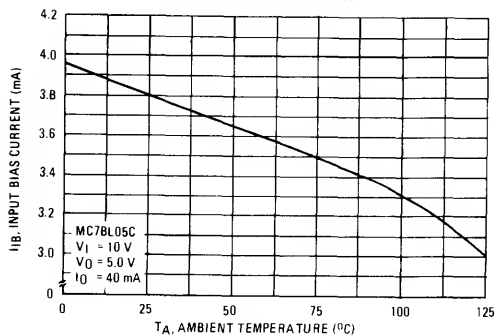


FIGURE 4 – INPUT BIAS CURRENT versus INPUT VOLTAGE

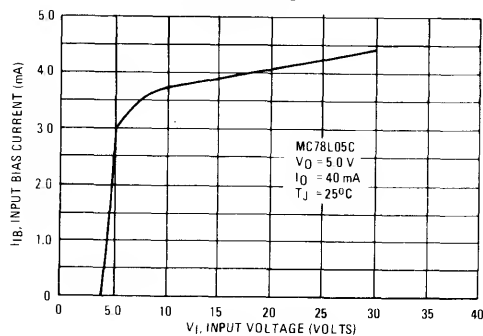


FIGURE 5 – MAXIMUM AVERAGE POWER DISSIPATION versus AMBIENT TEMPERATURE – TO-92 Type Package

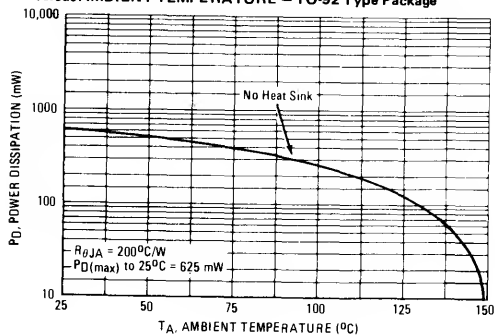
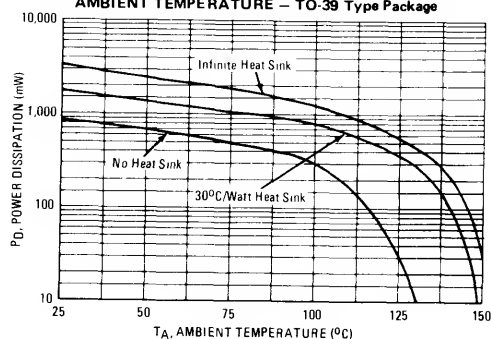


FIGURE 6 – MAXIMUM AVERAGE POWER DISSIPATION versus AMBIENT TEMPERATURE – TO-39 Type Package



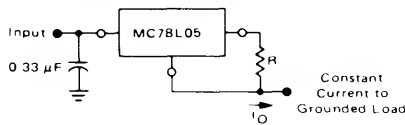
APPLICATIONS INFORMATION

Design Considerations

The MC78L00 Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition. Internal Short-Circuit Protection limits the maximum current the circuit will pass.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. The input bypass capacitor should be selected

FIGURE 7 — CURRENT REGULATOR



The MC78L00 regulators can also be used as a current source when connected as above, in order to minimize dissipation the MC78L05C is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5 \text{ V}}{R} + I_{IB}$$

$I_{IB} = 3.8 \text{ mA}$ over line and load changes

For example, a 100 mA current source would require R to be a 50-ohm, 1/2-W resistor and the output voltage compliance would be the input voltage less 7 volts.

to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.

FIGURE 8 — ±15 V TRACKING VOLTAGE REGULATOR

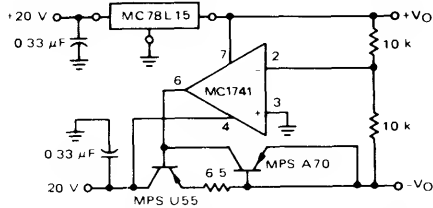


FIGURE 9 — POSITIVE AND NEGATIVE REGULATOR

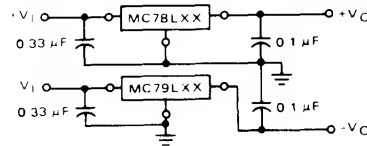
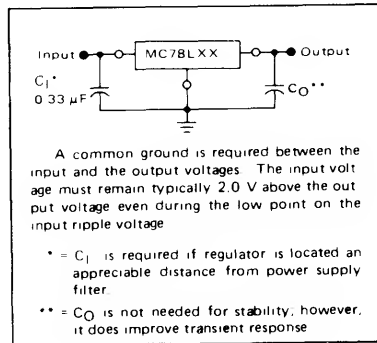


FIGURE 10 — STANDARD APPLICATION



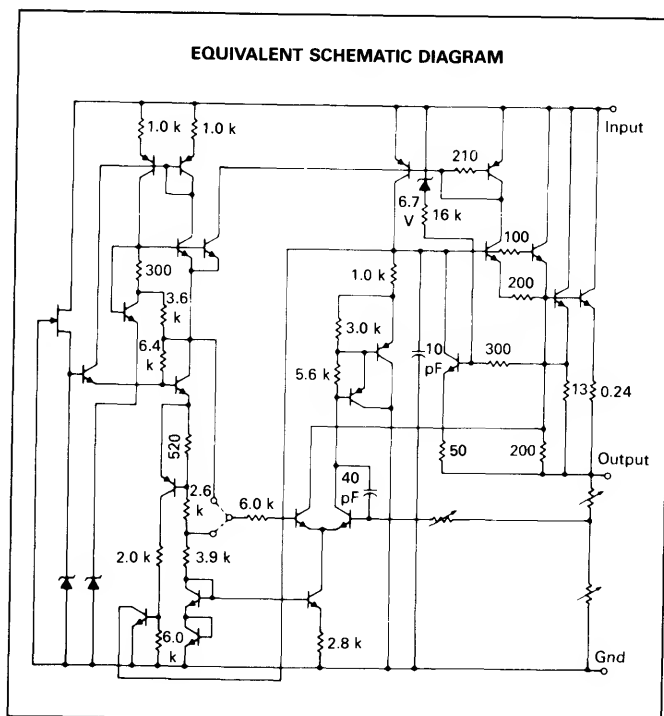
**THREE-TERMINAL MEDIUM CURRENT
 POSITIVE VOLTAGE REGULATORS**

The MC78M00 Series positive voltage regulators are identical to the popular MC7800 Series devices, except that they are specified for only half the output current. Like the MC7800 devices, the MC78M00 three-terminal regulators are intended for local, on-card voltage regulation.

Internal current limiting, thermal shutdown circuitry and safe-area compensation for the internal pass transistor combine to make these devices remarkably rugged under most operating conditions. Maximum output current, with adequate heatsinking is 500 mA.

- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation

EQUIVALENT SCHEMATIC DIAGRAM



TYPE NO./VOLTAGE

MC78M05B,C 5.0 Volts	MC78M12B,C 12 Volts	MC78M20B,C 20 Volts
MC78M06B,C 6.0 Volts	MC78M15B,C 15 Volts	MC78M24B,C 24 Volts
MC78M08B,C 8.0 Volts	MC78M18B,C 18 Volts	

**MC78M00
 Series**

**THREE-TERMINAL MEDIUM
 CURRENT POSITIVE FIXED
 VOLTAGE REGULATORS**

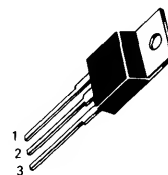
- PIN 1. INPUT
 2. OUTPUT
 3. GROUND



(Bottom View)

G SUFFIX
 METAL PACKAGE
 CASE 79
 (Case connected to Pin 3)

T SUFFIX
 PLASTIC PACKAGE
 CASE 221A



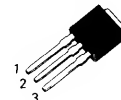
(All 3 Plastic Types)

- PIN 1. INPUT
 2. GROUND
 3. OUTPUT

(Heatsink surface connected to Pin 2)



DT SUFFIX
 PLASTIC PACKAGE
 CASE 369A
 (DPAK)



DT-1 SUFFIX
 PLASTIC PACKAGE
 CASE 369
 (DPAK)

ORDERING INFORMATION

Device	Tested Operating Junction Temp. Range	Package
MC78MXXCG*	$T_J = 0^\circ\text{C to } +125^\circ\text{C}$	Metal Can
MC78MXXCDT* MC78MXXCDT-1*		DPAK
MC78MXXCT		Plastic Power
MC78MXXBT#	$T_J = -40^\circ\text{C to } +125^\circ\text{C}$	Plastic Power

XX Indicates nominal voltage.

* Available in 5, 8, 12 and 15 volt devices.

Automotive temperature range selections are available with special test conditions and additional tests in 5, 8, 12 and 15 volt devices. Contact your local Motorola sales office for information.

MC78M00 Series

3

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (5.0 V–18 V) (20 V–24 V)	V _I	35 40	Vdc
Power Dissipation (Package Limitation) Plastic Package, T Suffix T _A = 25°C Derate above T _A = 25°C T _C = 25°C Derate above T _C = 110°C Metal Package T _A = 25°C Derate above T _A = 25°C T _C = 25°C Derate above T _C = 85°C	P _D θ _{JA} P _D θ _{JC} P _D θ _{JA} P _D θ _{JC}	Internally Limited 70 Internally Limited 5.0 Internally Limited 185 Internally Limited 25	°C/W °C/W °C/W °C/W
Operating Junction Temperature Range MC78MXXC MC78MXXB	T _J	0 to +150 –40 to +150	°C
Storage Temperature Range	T _{stg}	–65 to +150	°C

MC78M05B,C ELECTRICAL CHARACTERISTICS (V_I = 10 V, I_O = 350 mA, 0°C < T_J < +125°C, P_D ≤ 5.0 W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T _J = +25°C)	V _O	4.8	5.0	5.2	Vdc
Line Regulation (T _J = +25°C, 7.0 Vdc ≤ V _I ≤ 25 Vdc, I _O = 200 mA)	Reg _{line}	—	3.0	50	mV
Load Regulation (T _J = +25°C, 5.0 mA ≤ I _O ≤ 500 mA) (T _J = +25°C, 5.0 mA ≤ I _O ≤ 200 mA)	Reg _{load}	— —	20 10	100 50	mV
Output Voltage (7.0 Vdc ≤ V _I ≤ 25 Vdc, 5.0 mA ≤ I _O ≤ 200 mA) (7.0 Vdc ≤ V _I ≤ 20 Vdc, 5.0 mA ≤ I _O ≤ 350 mA)	V _O	4.75	—	5.25	Vdc
Input Bias Current (T _J = +25°C)	I _B	—	3.2	6.0	mA
Quiescent Current Change (8.0 Vdc ≤ V _I ≤ 25 Vdc, I _O = 200 mA) (5.0 mA ≤ I _O ≤ 350 mA)	ΔI _B	— —	— —	0.8 0.5	mA
Output Noise Voltage (T _A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V _n	—	40	—	μV
Ripple Rejection (T, DT and DT-1 suffixes only) (I _O = 100 mA, f = 120 Hz, 8.0 V ≤ V _I ≤ 18 V) (I _O = 300 mA, f = 120 Hz, 8.0 V ≤ V _I ≤ 18 V, T _J = 25°C)	RR	62 62	— 80	— —	dB
Dropout Voltage (T _J = +25°C)	V _I –V _O	—	2.0	—	Vdc
Short Circuit Current Limit (T _J = +25°C, V _I = 35 V)	I _{OS}	—	50	—	mA
Average Temperature Coefficient of Output Voltage (I _O = 5.0 mA)	ΔV _O /ΔT	—	±0.2	—	mV/°C
Peak Output Current (T _J = 25°C)	I _O	—	700	—	mA

MC78M00 Series

MC78M06C ELECTRICAL CHARACTERISTICS ($V_I = 11\text{ V}$, $I_O = 350\text{ mA}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$, $P_D \leq 5.0\text{ W}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	5.75	6.0	6.25	Vdc
Line Regulation ($T_J = +25^\circ\text{C}$, $8.0\text{ Vdc} \leq V_I \leq 25\text{ Vdc}$, $I_O = 200\text{ mA}$)	Regline	—	5.0	50	mV
Load Regulation ($T_J = +25^\circ\text{C}$, $5.0\text{ mA} \leq I_O \leq 500\text{ mA}$) ($T_J = +25^\circ\text{C}$, $5.0\text{ mA} \leq I_O \leq 200\text{ mA}$)	Regload	— —	20 10	120 60	mV
Output Voltage ($8.0\text{ Vdc} \leq V_I \leq 25\text{ Vdc}$, $5.0\text{ mA} \leq I_O \leq 200\text{ mA}$) ($8.0\text{ Vdc} \leq V_I \leq 21\text{ Vdc}$, $5.0\text{ mA} \leq I_O \leq 350\text{ mA}$)	V_O	5.7	—	6.3	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$)	I_{IB}	—	3.2	6.0	mA
Quiescent Current Change ($9.0\text{ Vdc} \leq V_I \leq 25\text{ Vdc}$, $I_O = 200\text{ mA}$) ($5.0\text{ mA} \leq I_O \leq 350\text{ mA}$)	ΔI_{IB}	— —	— —	0.8 0.5	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$)	V_n	—	45	—	μV
Ripple Rejection (T suffix only) ($I_O = 100\text{ mA}$, $f = 120\text{ Hz}$, $9.0\text{ V} \leq V_I \leq 19\text{ V}$) ($I_O = 300\text{ mA}$, $f = 120\text{ Hz}$, $9.0\text{ V} \leq V_I \leq 19\text{ V}$, $T_J = 25^\circ\text{C}$)	RR	59 59	— 80	— —	dB
Dropout Voltage ($T_J = +25^\circ\text{C}$)	$V_I - V_O$	—	2.0	—	Vdc
Short Circuit Current Limit ($T_J = +25^\circ\text{C}$, $V_I = 35\text{ V}$)	I_{OS}	—	50	—	mA
Average Temperature Coefficient of Output Voltage ($I_O = 5.0\text{ mA}$)	$\Delta V_O / \Delta T$	—	± 0.2	—	$\text{mV}/^\circ\text{C}$
Peak Output Current ($T_J = 25^\circ\text{C}$)	I_O	—	700	—	mA

MC78M08B,C ELECTRICAL CHARACTERISTICS ($V_I = 14\text{ V}$, $I_O = 350\text{ mA}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$, $P_D \leq 5.0\text{ W}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	7.7	8.0	8.3	Vdc
Line Regulation ($T_J = +25^\circ\text{C}$, $10.5\text{ Vdc} \leq V_I \leq 25\text{ Vdc}$, $I_O = 200\text{ mA}$)	Regline	—	6.0	50	mV
Load Regulation ($T_J = +25^\circ\text{C}$, $5.0\text{ mA} \leq I_O \leq 500\text{ mA}$) ($T_J = +25^\circ\text{C}$, $5.0\text{ mA} \leq I_O \leq 200\text{ mA}$)	Regload	— —	25 10	160 80	mV
Output Voltage ($10.5\text{ Vdc} \leq V_I \leq 25\text{ Vdc}$, $5.0\text{ mA} \leq I_O \leq 200\text{ mA}$) ($10.5\text{ Vdc} \leq V_I \leq 23\text{ Vdc}$, $5.0\text{ mA} \leq I_O \leq 350\text{ mA}$)	V_O	7.6	—	8.4	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$)	I_{IB}	—	3.2	6.0	mA
Quiescent Current Change ($10.5\text{ Vdc} \leq V_I \leq 25\text{ Vdc}$, $I_O = 200\text{ mA}$) ($5.0\text{ mA} \leq I_O \leq 350\text{ mA}$)	ΔI_{IB}	— —	— —	0.8 0.5	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$)	V_n	—	52	—	μV
Ripple Rejection (T suffix only) ($I_O = 100\text{ mA}$, $f = 120\text{ Hz}$, $11.5\text{ V} \leq V_I \leq 21.5\text{ V}$) ($I_O = 300\text{ mA}$, $f = 120\text{ Hz}$, $11.5\text{ V} \leq V_I \leq 21.5\text{ V}$, $T_J = 25^\circ\text{C}$)	RR	56 56	— 80	— —	dB
Dropout Voltage ($T_J = +25^\circ\text{C}$)	$V_I - V_O$	—	2.0	—	Vdc
Short Circuit Current Limit ($T_J = +25^\circ\text{C}$, $V_I = 35\text{ V}$)	I_{OS}	—	50	—	mA
Average Temperature Coefficient of Output Voltage ($I_O = 5.0\text{ mA}$)	$\Delta V_O / \Delta T$	—	± 0.2	—	$\text{mV}/^\circ\text{C}$
Peak Output Current ($T_J = 25^\circ\text{C}$)	I_O	—	700	—	mA

MC78M00 Series

MC78M12B,C ELECTRICAL CHARACTERISTICS ($V_I = 19\text{ V}$, $I_O = 350\text{ mA}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$, $P_D \leq 5.0\text{ W}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	11.5	12	12.5	Vdc
Line Regulation ($T_J = +25^\circ\text{C}$, $14.5\text{ Vdc} \leq V_I \leq 30\text{ Vdc}$, $I_O = 200\text{ mA}$)	Regline	—	8.0	50	mV
Load Regulation ($T_J = +25^\circ\text{C}$, $5.0\text{ mA} \leq I_O \leq 500\text{ mA}$) ($T_J = +25^\circ\text{C}$, $5.0\text{ mA} \leq I_O \leq 200\text{ mA}$)	Regload	— —	25 10	240 120	mV
Output Voltage ($14.5\text{ Vdc} \leq V_I \leq 27\text{ Vdc}$, $5.0\text{ mA} \leq I_O \leq 350\text{ mA}$)	V_O	11.4	—	12.6	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$)	I_{IB}	—	3.2	6.0	mA
Quiescent Current Change ($14.5\text{ Vdc} \leq V_I \leq 30\text{ Vdc}$, $I_O = 200\text{ mA}$) ($5.0\text{ mA} \leq I_O \leq 350\text{ mA}$)	ΔI_{IB}	— —	— —	0.8 0.5	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$)	V_n	—	75	—	μV
Ripple Rejection (T, DT and DT-1 suffixes only) ($I_O = 100\text{ mA}$, $f = 120\text{ Hz}$, $15\text{ V} \leq V_I \leq 25\text{ V}$) ($I_O = 300\text{ mA}$, $f = 120\text{ Hz}$, $15\text{ V} \leq V_I \leq 25\text{ V}$, $T_J = 25^\circ\text{C}$)	RR	55 55	— 80	— —	dB
Dropout Voltage ($T_J = +25^\circ\text{C}$)	$V_I - V_O$	—	2.0	—	Vdc
Short Circuit Current Limit ($T_J = +25^\circ\text{C}$, $V_I = 35\text{ V}$)	I_{OS}	—	50	—	mA
Average Temperature Coefficient of Output Voltage ($I_O = 5.0\text{ mA}$)	$\Delta V_O / \Delta T$	—	± 0.3	—	$\text{mV}/^\circ\text{C}$
Peak Output Current ($T_J = 25^\circ\text{C}$)	I_O	—	700	—	mA

MC78M15B,C ELECTRICAL CHARACTERISTICS ($V_I = 23\text{ V}$, $I_O = 350\text{ mA}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$, $P_D \leq 5.0\text{ W}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	14.4	15	15.6	Vdc
Input Regulation ($T_J = +25^\circ\text{C}$, $17.5\text{ Vdc} \leq V_I \leq 30\text{ Vdc}$, $I_O = 200\text{ mA}$)	Regline	—	10	50	mV
Load Regulation ($T_J = +25^\circ\text{C}$, $5.0\text{ mA} \leq I_O \leq 500\text{ mA}$) ($T_J = +25^\circ\text{C}$, $5.0\text{ mA} \leq I_O \leq 200\text{ mA}$)	Regload	— —	25 10	300 150	mV
Output Voltage ($17.5\text{ Vdc} \leq V_I \leq 30\text{ Vdc}$, $5.0\text{ mA} \leq I_O \leq 350\text{ mA}$)	V_O	14.25	—	15.75	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$)	I_{IB}	—	3.2	6.0	mA
Quiescent Current Change ($17.5\text{ Vdc} \leq V_I \leq 30\text{ Vdc}$, $I_O = 200\text{ mA}$) ($5.0\text{ mA} \leq I_O \leq 350\text{ mA}$)	ΔI_{IB}	— —	— —	0.8 0.5	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$)	V_n	—	90	—	μV
Ripple Rejection (T, DT and DT-1 suffixes only) ($I_O = 100\text{ mA}$, $f = 120\text{ Hz}$, $18.5\text{ V} \leq V_I \leq 28.5\text{ V}$) ($I_O = 300\text{ mA}$, $f = 120\text{ Hz}$, $18.5\text{ V} \leq V_I \leq 28.5\text{ V}$, $T_J = 25^\circ\text{C}$)	RR	54 54	— 70	— —	dB
Dropout Voltage ($T_J = +25^\circ\text{C}$)	$V_I - V_O$	—	2.0	—	Vdc
Short Circuit Current Limit ($T_J = +25^\circ\text{C}$, $V_I = 35\text{ V}$)	I_{OS}	—	50	—	mA
Average Temperature Coefficient of Output Voltage ($I_O = 5.0\text{ mA}$)	$\Delta V_O / \Delta T$	—	± 0.3	—	$\text{mV}/^\circ\text{C}$
Peak Output Current ($T_J = 25^\circ\text{C}$)	I_O	—	700	—	mA

MC78M00 Series

MC78M18C ELECTRICAL CHARACTERISTICS ($V_I = 27\text{ V}$, $I_O = 350\text{ mA}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$, $P_D \leq 5.0\text{ W}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	17.3	18	18.7	Vdc
Line Regulation ($T_J = +25^\circ\text{C}$, $21\text{ Vdc} \leq V_I \leq 33\text{ Vdc}$, $I_O = 200\text{ mA}$)	Reg_{line}	—	10	50	mV
Load Regulation ($T_J = +25^\circ\text{C}$, $5.0\text{ mA} \leq I_O \leq 500\text{ mA}$) ($T_J = +25^\circ\text{C}$, $5.0\text{ mA} \leq I_O \leq 200\text{ mA}$)	Reg_{load}	— —	30 10	360 180	mV
Output Voltage ($21\text{ Vdc} \leq V_I \leq 33\text{ Vdc}$, $5.0\text{ mA} \leq I_O \leq 350\text{ mA}$)	V_O	17.1	—	18.9	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$)	I_{IB}	—	3.2	6.5	mA
Quiescent Current Change ($21\text{ Vdc} \leq V_I \leq 33\text{ Vdc}$, $I_O = 200\text{ mA}$) ($5.0\text{ mA} \leq I_O \leq 350\text{ mA}$)	ΔI_{IB}	— —	— —	0.8 0.5	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$)	V_n	—	100	—	μV
Ripple Rejection (T suffix only) ($I_O = 100\text{ mA}$, $f = 120\text{ Hz}$, $22\text{ V} \leq V_I \leq 32\text{ V}$) ($I_O = 300\text{ mA}$, $f = 120\text{ Hz}$, $22\text{ V} \leq V_I \leq 32\text{ V}$, $T_J = 25^\circ\text{C}$)	RR	53 53	— 70	— —	dB
Dropout Voltage ($T_J = +25^\circ\text{C}$)	$V_I - V_O$	—	2.0	—	Vdc
Short Circuit Current Limit ($T_J = +25^\circ\text{C}$, $V_I = 35\text{ V}$)	I_{OS}	—	50	—	mA
Average Temperature Coefficient of Output Voltage ($I_O = 5.0\text{ mA}$)	$\Delta V_O / \Delta T$	—	± 0.3	—	$\text{mV}/^\circ\text{C}$
Peak Output Current ($T_J = 25^\circ\text{C}$)	I_O	—	700	—	mA

MC78M20C ELECTRICAL CHARACTERISTICS ($V_I = 29\text{ V}$, $I_O = 350\text{ mA}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$, $P_D \leq 5.0\text{ W}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	19.2	20	20.8	Vdc
Line Regulation ($T_J = +25^\circ\text{C}$, $23\text{ Vdc} \leq V_I \leq 35\text{ Vdc}$, $I_O = 200\text{ mA}$)	Reg_{line}	—	10	50	mV
Load Regulation ($T_J = +25^\circ\text{C}$, $5.0\text{ mA} \leq I_O \leq 500\text{ mA}$) ($T_J = +25^\circ\text{C}$, $5.0\text{ mA} \leq I_O \leq 200\text{ mA}$)	Reg_{load}	— —	30 10	400 200	mV
Output Voltage ($23\text{ Vdc} \leq V_I \leq 35\text{ Vdc}$, $5.0\text{ mA} \leq I_O \leq 350\text{ mA}$)	V_O	19	—	21	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$)	I_{IB}	—	3.2	6.5	mA
Quiescent Current Change ($23\text{ Vdc} \leq V_I \leq 35\text{ Vdc}$, $I_O = 200\text{ mA}$) ($5.0\text{ mA} \leq I_O \leq 350\text{ mA}$)	ΔI_{IB}	— —	— —	0.8 0.5	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$)	V_n	—	110	—	μV
Ripple Rejection (T suffix only) ($I_O = 100\text{ mA}$, $f = 120\text{ Hz}$, $24\text{ V} \leq V_I \leq 34\text{ V}$) ($I_O = 300\text{ mA}$, $f = 120\text{ Hz}$, $24\text{ V} \leq V_I \leq 34\text{ V}$, $T_J = 25^\circ\text{C}$)	RR	52 52	— 70	— —	dB
Dropout Voltage ($T_J = +25^\circ\text{C}$)	$V_I - V_O$	—	2.0	—	Vdc
Short Circuit Current Limit ($T_J = +25^\circ\text{C}$, $V_I = 35\text{ V}$)	I_{OS}	—	50	—	mA
Average Temperature Coefficient of Output Voltage ($I_O = 5.0\text{ mA}$)	$\Delta V_O / \Delta T$	—	± 0.5	—	$\text{mV}/^\circ\text{C}$
Peak Output Current ($T_J = 25^\circ\text{C}$)	I_O	—	700	—	mA

MC78M00 Series

MC78M24C ELECTRICAL CHARACTERISTICS ($V_I = 33\text{ V}$, $I_O = 350\text{ mA}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$, $P_D \leq 5.0\text{ W}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	23	24	25	Vdc
Line Regulation ($T_J = +25^\circ\text{C}$, $27\text{ Vdc} \leq V_I \leq 38\text{ Vdc}$, $I_O = 200\text{ mA}$)	Regline	—	10	50	mV
Load Regulation ($T_J = +25^\circ\text{C}$, $5.0\text{ mA} \leq I_O \leq 500\text{ mA}$) ($T_J = +25^\circ\text{C}$, $5.0\text{ mA} \leq I_O \leq 200\text{ mA}$)	Regload	— —	30 10	480 240	mV
Output Voltage ($27\text{ Vdc} \leq V_I \leq 38\text{ Vdc}$, $5.0\text{ mA} \leq I_O \leq 350\text{ mA}$)	V_O	22.8	—	25.2	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$)	I_{IB}	—	3.2	7.0	mA
Quiescent Current Change ($27\text{ Vdc} \leq V_I \leq 38\text{ Vdc}$, $I_O = 200\text{ mA}$) ($5.0\text{ mA} \leq I_O \leq 350\text{ mA}$)	ΔI_{IB}	— —	— —	0.8 0.5	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$)	V_n	—	170	—	μV
Ripple Rejection (T suffix only) ($I_O = 100\text{ mA}$, $f = 120\text{ Hz}$, $28\text{ V} \leq V_I \leq 38\text{ V}$) ($I_O = 300\text{ mA}$, $f = 120\text{ Hz}$, $28\text{ V} \leq V_I \leq 38\text{ V}$, $T_J = 25^\circ\text{C}$)	RR	50 50	— 70	— —	dB
Dropout Voltage ($T_J = +25^\circ\text{C}$)	$V_I - V_O$	—	2.0	—	Vdc
Short Circuit Current Limit ($T_J = +25^\circ\text{C}$)	I_{OS}	—	50	—	mA
Average Temperature Coefficient of Output Voltage ($I_O = 5.0\text{ mA}$)	$\Delta V_O / \Delta T$	—	± 0.5	—	$\text{mV}/^\circ\text{C}$
Peak Output Current ($T_J = 25^\circ\text{C}$)	I_O	—	700	—	mA

DEFINITIONS

Line Regulation — The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation — The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation — The maximum total device dissipation for which the regulator will operate within specifications.

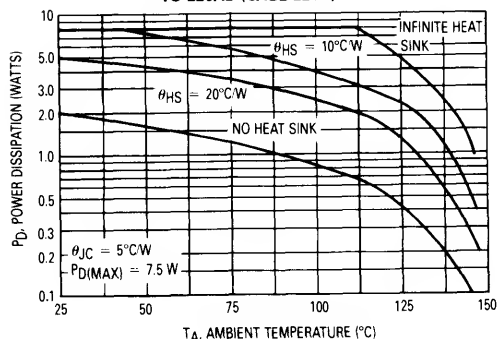
Input Bias Current — That part of the input current that is not delivered to the load.

Output Noise Voltage — The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

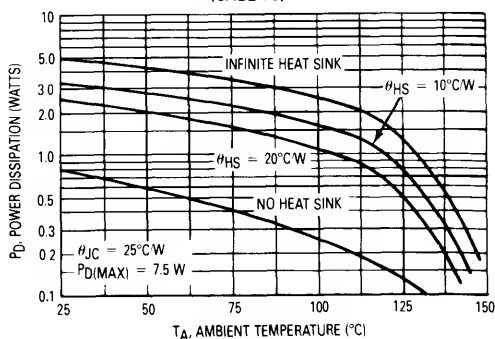
Long Term Stability — Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.

TYPICAL PERFORMANCE CURVES

**FIGURE 1 — WORST CASE POWER DISSIPATION
versus AMBIENT TEMPERATURE
TO-220AB (CASE 221A)**



**FIGURE 2 — WORST CASE POWER DISSIPATION
versus AMBIENT TEMPERATURE
(CASE 79)**



MC78M00 Series

TYPICAL PERFORMANCE CURVES

FIGURE 3 — PEAK OUTPUT CURRENT versus DROPOUT VOLTAGE

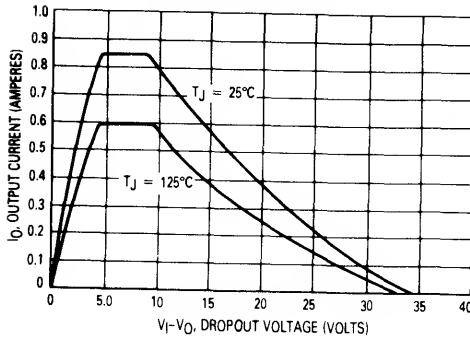


FIGURE 4 — DROPOUT VOLTAGE versus JUNCTION TEMPERATURE

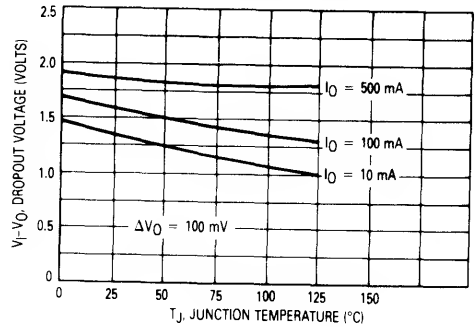


FIGURE 5 — RIPPLE REJECTION versus FREQUENCY

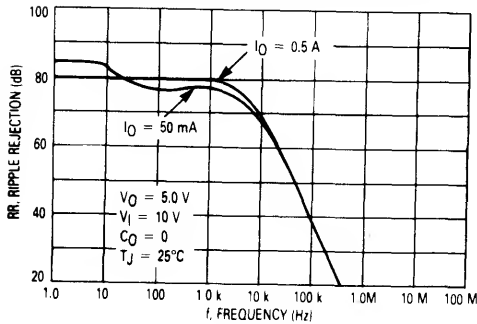


FIGURE 6 — RIPPLE REJECTION versus OUTPUT CURRENT

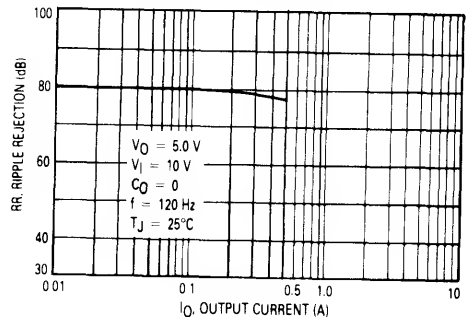


FIGURE 7 — BIAS CURRENT versus INPUT VOLTAGE

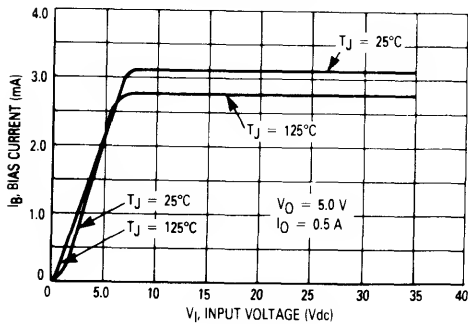
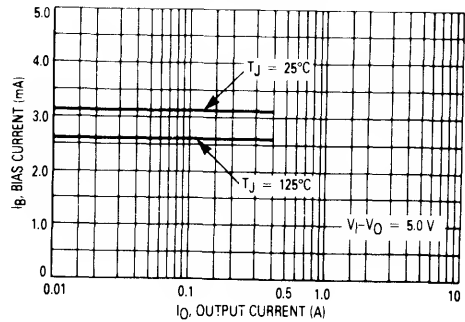


FIGURE 8 — BIAS CURRENT versus OUTPUT CURRENT



APPLICATIONS INFORMATION

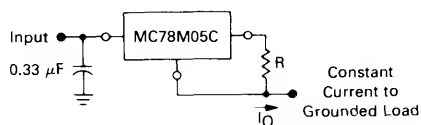
DESIGN CONSIDERATIONS

The MC78M00 Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power sup-

ply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

FIGURE 9 — CURRENT REGULATOR



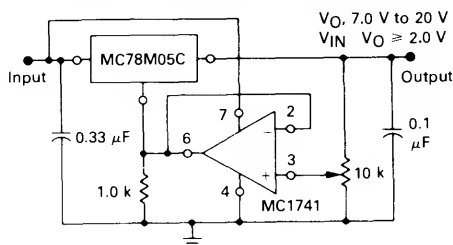
The MC78M00 regulators can also be used as a current source when connected as above. In order to minimize dissipation the MC78M05C is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5.0 \text{ V}}{R} + I_{IB}$$

$I_{IB} = 1.5 \text{ mA}$ over line and load changes

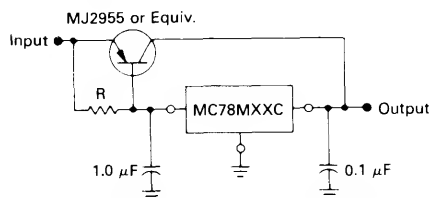
For example, a 500 mA current source would require R to be a 10 ohm, 10 W resistor and the output voltage compliance would be the input voltage less 7.0 volts.

FIGURE 10 — ADJUSTABLE OUTPUT REGULATOR



The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 2.0 volts greater than the regulator voltage.

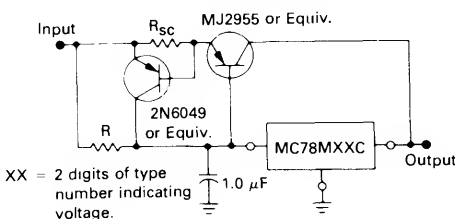
FIGURE 11 — CURRENT BOOST REGULATOR



XX = 2 digits of type number indicating voltage.

The MC78M00 series can be current boosted with a PNP transistor. The MJ2955 provides current to 5.0 amperes. Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short circuit proof. Input output differential voltage minimum is increased by V_{BE} of the pass transistor.

FIGURE 12 — CURRENT BOOST WITH SHORT-CIRCUIT PROTECTION



The circuit of Figure 7 can be modified to provide supply protection against short circuits by adding a short circuit sense resistor, R_{SC} , and an additional PNP transistor. The current sensing PNP must be able to handle the short-circuit current of the three-terminal regulator. Therefore, a two-ampere plastic power transistor is specified.

THREE-AMPERE POSITIVE VOLTAGE REGULATORS

This family of fixed voltage regulators are monolithic integrated circuits capable of driving loads in excess of 3.0 amperes. These three-terminal regulators employ internal current limiting, thermal shutdown, and safe-area compensation. Devices are available with improved specifications, including a 2% output voltage tolerance, on AC-suffix 5.0, 12 and 15 volt device types.

Although designed primarily as a fixed voltage regulator, these devices can be used with external components to obtain adjustable voltages and currents. This series of devices can be used with a series-pass transistor to supply up to 15 amperes at the nominal output voltage.

- Output Current in Excess of 3.0 Amperes
- Power Dissipation: 30 W (K-Suffix), 25 W (T-Suffix)
- No External Components Required
- Output Voltage Offered in 2% and 4% Tolerance*
- Thermal Regulation is Specified
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (5.0 V–12 V) (15 V)	V_{in}	35 40	Vdc
Power Dissipation and Thermal Characteristics			
Plastic Package (Note 1)			
$T_A = +25^\circ\text{C}$	P_D	Internally Limited	
Thermal Resistance, Junction to Air	$R_{\theta JA}$	65	$^\circ\text{C/W}$
$T_C = +25^\circ\text{C}$	P_D	Internally Limited	
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	$^\circ\text{C/W}$
Metal Package (Note 1)			
$T_A = +25^\circ\text{C}$	P_D	Internally Limited	
Thermal Resistance, Junction to Air	$R_{\theta JA}$	35	$^\circ\text{C/W}$
$T_C = +25^\circ\text{C}$	P_D	Internally Limited	
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	$^\circ\text{C/W}$
Storage Junction Temperature Range	T_{stg}	–65 to +150	$^\circ\text{C}$
Operating Junction Temperature Range MC78T00C, AC	T_J	0 to +150	$^\circ\text{C}$

NOTE:

- Although power dissipation is internally limited, specifications apply only for $P_O \leq P_{max}$.
 $P_{max} = 30\text{ W}$ for K package
 $P_{max} = 25\text{ W}$ for T package.

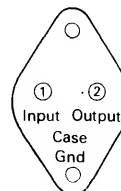
TYPE NO./VOLTAGE			
MC78T05	5.0 Volts	MC78T12	12 Volts
MC78T08	8.0 Volts	MC78T15	15 Volts

MC78T00 Series

THREE-AMPERE POSITIVE FIXED VOLTAGE REGULATORS

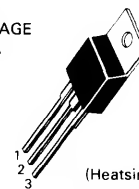
SILICON MONOLITHIC INTEGRATED CIRCUIT

K SUFFIX METAL PACKAGE CASE 1



(Bottom View)

T SUFFIX PLASTIC PACKAGE CASE 221A



PIN 1. INPUT
2. GROUND
3. OUTPUT

(Heatsink surface
connected to
Pin 2)

ORDERING INFORMATION

Device	Output Voltage Tolerance	Tested Operating Junction Temp. Range	Package
MC78TXXCK MC78TXXACK	4% 2%*	0 to +125 $^\circ\text{C}$	Metal Power
MC78TXXCT MC78TXXACT	4% 2%*		Plastic Power
MC78TXXBT# MC78TXXABT#	4% 2%*	–40 to +125 $^\circ\text{C}$	Plastic Power

XX Indicates nominal voltage.

* 2% regulators are available in 5, 12 and 15 volt devices.

Automotive temperature range selections are available with special test conditions and additional tests. Contact your local Motorola sales office for information.

MC78T00 Series

MC78T05AC, C

ELECTRICAL CHARACTERISTICS ($V_{in} = 10\text{ V}$, $I_O = 3.0\text{ A}$, $0^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$, $P_O \leq P_{max}$ [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC78T05AC			MC78T05C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($5.0\text{ mA} \leq I_O \leq 3.0\text{ A}$, $T_J = +25^\circ\text{C}$) ($5.0\text{ mA} \leq I_O \leq 3.0\text{ A}$; $5.0\text{ mA} \leq I_O \leq 2.0\text{ A}$, $7.3\text{ Vdc} \leq V_{in} \leq 20\text{ Vdc}$)	V_O	4.9 4.8	5.0 5.0	5.1 5.2	4.8 4.75	5.0 5.0	5.2 5.25	Vdc
Line Regulation (Note 2) ($7.2\text{ Vdc} \leq V_{in} \leq 35\text{ Vdc}$, $I_O = 5.0\text{ mA}$, $T_J = +25^\circ\text{C}$; $7.2\text{ Vdc} \leq V_{in} \leq 35\text{ Vdc}$, $I_O = 1.0\text{ A}$, $T_J = +25^\circ\text{C}$; $8.0\text{ Vdc} \leq V_{in} \leq 12\text{ Vdc}$, $I_O = 3.0\text{ A}$, $T_J = +25^\circ\text{C}$; $7.5\text{ Vdc} \leq V_{in} \leq 20\text{ Vdc}$, $I_O = 1.0\text{ A}$)	Regline	—	3.0	25	—	3.0	25	mV
Load Regulation (Note 2) ($5.0\text{ mA} \leq I_O \leq 3.0\text{ A}$, $T_J = +25^\circ\text{C}$) ($5.0\text{ mA} \leq I_O \leq 3.0\text{ A}$)	Regload	— —	10 15	30 80	— —	10 15	30 80	mV
Thermal Regulation (Pulse = 10 ms, $P = 20\text{ W}$, $T_A = +25^\circ\text{C}$)	Regtherm	—	0.001	0.01	—	0.002	0.03	% V_O /W
Quiescent Current ($5.0\text{ mA} \leq I_O \leq 3.0\text{ A}$, $T_J = +25^\circ\text{C}$) ($5.0\text{ mA} \leq I_O \leq 3.0\text{ A}$)	I_B	— —	3.5 4.0	5.0 6.0	— —	3.5 4.0	5.0 6.0	mA
Quiescent Current Change ($7.2\text{ Vdc} \leq V_{in} \leq 35\text{ Vdc}$, $I_O = 5.0\text{ mA}$, $T_J = +25^\circ\text{C}$; $5.0\text{ mA} \leq I_O \leq 3.0\text{ A}$, $T_J = +25^\circ\text{C}$; $7.5\text{ Vdc} \leq V_{in} \leq 20\text{ Vdc}$, $I_O = 1.0\text{ A}$)	ΔI_B	—	0.3	1.0	—	0.3	1.0	mA
Ripple Rejection ($8.0\text{ Vdc} \leq V_{in} \leq 18\text{ Vdc}$, $f = 120\text{ Hz}$, $I_O = 2.0\text{ A}$, $T_J = 25^\circ\text{C}$)	RR	62	75	—	62	75	—	dB
Dropout Voltage ($I_O = 3.0\text{ A}$, $T_J = +25^\circ\text{C}$)	$V_{in}-V_O$	—	2.2	2.5	—	2.2	2.5	Vdc
Output Noise Voltage ($10\text{ Hz} \leq f \leq 100\text{ kHz}$, $T_J = +25^\circ\text{C}$)	V_n	—	10	—	—	10	—	$\mu\text{V}/V_O$
Output Resistance ($f = 1.0\text{ kHz}$)	R_O	—	2.0	—	—	2.0	—	$\text{m}\Omega$
Short Circuit Current Limit ($V_{in} = 35\text{ Vdc}$, $T_J = +25^\circ\text{C}$)	I_{SC}	—	1.5	—	—	1.5	—	A
Peak Output Current ($T_J = +25^\circ\text{C}$)	I_{max}	—	5.0	—	—	5.0	—	A
Average Temperature Coefficient of Output Voltage ($I_O = 5.0\text{ mA}$)	TCV_O	—	0.2	—	—	0.2	—	$\text{mV}/^\circ\text{C}$

NOTES:

- Although power dissipation is internally limited, specifications apply only for $P_O \leq P_{max}$:
 $P_{max} = 30\text{ W}$ for K package
 $P_{max} = 25\text{ W}$ for T package
- Line and load regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC78T00 Series

MC78T08C

ELECTRICAL CHARACTERISTICS ($V_{in} = 13\text{ V}$, $I_O = 3.0\text{ A}$, $0^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$, $P_O \leq P_{max}$ [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC78T08C			Unit
		Min	Typ	Max	
Output Voltage ($5.0\text{ mA} \leq I_O \leq 3.0\text{ A}$, $T_J = +25^\circ\text{C}$) ($5.0\text{ mA} \leq I_O \leq 3.0\text{ A}$; $5.0\text{ mA} \leq I_O \leq 2.0\text{ A}$, $10.4\text{ Vdc} \leq V_{in} \leq 23\text{ Vdc}$)	V_O	7.7 7.6	8.0 8.0	8.3 8.4	Vdc
Line Regulation (Note 2) ($10.3\text{ Vdc} \leq V_{in} \leq 35\text{ Vdc}$, $I_O = 5.0\text{ mA}$, $T_J = +25^\circ\text{C}$; $10.3\text{ Vdc} \leq V_{in} \leq 35\text{ Vdc}$, $I_O = 1.0\text{ A}$, $T_J = +25^\circ\text{C}$; $11\text{ Vdc} \leq V_{in} \leq 17\text{ Vdc}$, $I_O = 3.0\text{ A}$, $T_J = +25^\circ\text{C}$; $10.7\text{ Vdc} \leq V_{in} \leq 23\text{ Vdc}$, $I_O = 1.0\text{ A}$)	Reg _{line}	—	4.0	35	mV
Load Regulation (Note 2) ($5.0\text{ mA} \leq I_O \leq 3.0\text{ A}$, $T_J = +25^\circ\text{C}$) ($5.0\text{ mA} \leq I_O \leq 3.0\text{ A}$)	Reg _{load}	— —	10 15	30 80	mV
Thermal Regulation (Pulse = 10 ms, $P = 20\text{ W}$, $T_A = +25^\circ\text{C}$)	Reg _{therm}	—	0.002	0.03	% V_O/W
Quiescent Current ($5.0\text{ mA} \leq I_O \leq 3.0\text{ A}$, $T_J = +25^\circ\text{C}$) ($5.0\text{ mA} \leq I_O \leq 3.0\text{ A}$)	I_B	— —	3.5 4.0	5.0 6.0	mA
Quiescent Current Change ($10.3\text{ Vdc} \leq V_{in} \leq 35\text{ Vdc}$, $I_O = 5.0\text{ mA}$, $T_J = +25^\circ\text{C}$; $5.0\text{ mA} \leq I_O \leq 3.0\text{ A}$, $T_J = +25^\circ\text{C}$; $10.7\text{ Vdc} \leq V_{in} \leq 23\text{ Vdc}$, $I_O = 1.0\text{ A}$)	ΔI_B	—	0.3	1.0	mA
Ripple Rejection ($11\text{ Vdc} \leq V_{in} \leq 21\text{ Vdc}$, $f = 120\text{ Hz}$, $I_O = 2.0\text{ A}$, $T_J = 25^\circ\text{C}$)	RR	60	71	—	dB
Dropout Voltage ($I_O = 3.0\text{ A}$, $T_J = +25^\circ\text{C}$)	$V_{in}-V_O$	—	2.2	2.5	Vdc
Output Noise Voltage ($10\text{ Hz} \leq f \leq 100\text{ kHz}$, $T_J = +25^\circ\text{C}$)	V_n	—	10	—	$\mu\text{V}/V_O$
Output Resistance ($f = 1.0\text{ kHz}$)	R_O	—	2.0	—	$\text{m}\Omega$
Short Circuit Current Limit ($V_{in} = 35\text{ Vdc}$, $T_J = +25^\circ\text{C}$)	I_{SC}	—	1.5	—	A
Peak Output Current ($T_J = +25^\circ\text{C}$)	I_{max}	—	5.0	—	A
Average Temperature Coefficient of Output Voltage ($I_O = 5.0\text{ mA}$)	TCV_O	—	0.3	—	$\text{mV}/^\circ\text{C}$

NOTES:

- Although power dissipation is internally limited, specifications apply only for $P_O \leq P_{max}$.
 $P_{max} = 30\text{ W}$ for K package $P_{max} = 25\text{ W}$ for T package
- Line and load regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC78T00 Series

MC78T12AC, C

ELECTRICAL CHARACTERISTICS ($V_{in} = 17\text{ V}$, $I_O = 3.0\text{ A}$, $0^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$, $P_O \leq P_{max}$ [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC78T12AC			MC78T12C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($5.0\text{ mA} \leq I_O \leq 3.0\text{ A}$, $T_J = +25^\circ\text{C}$) ($5.0\text{ mA} \leq I_O \leq 3.0\text{ A}$; $5.0\text{ mA} \leq I_O \leq 2.0\text{ A}$, $14.5\text{ Vdc} \leq V_{in} \leq 27\text{ Vdc}$)	V_O	11.75 11.5	12 12	12.25 12.5	11.5 11.4	12 12	12.5 12.6	Vdc
Line Regulation (Note 2) ($14.5\text{ Vdc} \leq V_{in} \leq 35\text{ Vdc}$, $I_O = 5.0\text{ mA}$, $T_J = +25^\circ\text{C}$; $14.5\text{ Vdc} \leq V_{in} \leq 35\text{ Vdc}$, $I_O = 1.0\text{ A}$, $T_J = +25^\circ\text{C}$; $16\text{ Vdc} \leq V_{in} \leq 22\text{ Vdc}$, $I_O = 3.0\text{ A}$, $T_J = +25^\circ\text{C}$; $14.9\text{ Vdc} \leq V_{in} \leq 27\text{ Vdc}$, $I_O = 1.0\text{ A}$)	Regline	—	6.0	45	—	6.0	45	mV
Load Regulation (Note 2) ($5.0\text{ mA} \leq I_O \leq 3.0\text{ A}$, $T_J = +25^\circ\text{C}$) ($5.0\text{ mA} \leq I_O \leq 3.0\text{ A}$)	Regload	— —	10 15	30 80	— —	10 15	30 80	mV
Thermal Regulation (Pulse = 10 ms, $P = 20\text{ W}$, $T_A = +25^\circ\text{C}$)	Regtherm	—	0.001	0.01	—	0.002	0.03	% V_O /W
Quiescent Current ($5.0\text{ mA} \leq I_O \leq 3.0\text{ A}$, $T_J = +25^\circ\text{C}$) ($5.0\text{ mA} \leq I_O \leq 3.0\text{ A}$)	I_B	— —	3.5 4.0	5.0 6.0	— —	3.5 4.0	5.0 6.0	mA
Quiescent Current Change ($14.5\text{ Vdc} \leq V_{in} \leq 35\text{ Vdc}$, $I_O = 5.0\text{ mA}$, $T_J = +25^\circ\text{C}$; $5.0\text{ mA} \leq I_O \leq 3.0\text{ A}$, $T_J = +25^\circ\text{C}$; $14.9\text{ Vdc} \leq V_{in} \leq 27\text{ Vdc}$, $I_O = 1.0\text{ A}$)	ΔI_B	—	0.3	1.0	—	0.3	1.0	mA
Ripple Rejection ($15\text{ Vdc} \leq V_{in} \leq 25\text{ Vdc}$, $f = 120\text{ Hz}$, $I_O = 2.0\text{ A}$, $T_J = 25^\circ\text{C}$)	RR	57	67	—	57	67	—	dB
Dropout Voltage ($I_O = 3.0\text{ A}$, $T_J = +25^\circ\text{C}$)	$V_{in}-V_O$	—	2.2	2.5	—	2.2	2.5	Vdc
Output Noise Voltage ($10\text{ Hz} \leq f \leq 100\text{ kHz}$, $T_J = +25^\circ\text{C}$)	V_n	—	10	—	—	10	—	$\mu\text{V}/V_O$
Output Resistance ($f = 1.0\text{ kHz}$)	R_O	—	2.0	—	—	2.0	—	$\text{m}\Omega$
Short Circuit Current Limit ($V_{in} = 35\text{ Vdc}$, $T_J = +25^\circ\text{C}$)	I_{SC}	—	1.5	—	—	1.5	—	A
Peak Output Current ($T_J = +25^\circ\text{C}$)	I_{max}	—	5.0	—	—	5.0	—	A
Average Temperature Coefficient of Output Voltage ($I_O = 5.0\text{ mA}$)	TCV_O	—	0.5	—	—	0.5	—	$\text{mV}/^\circ\text{C}$

NOTES:

- Although power dissipation is internally limited, specifications apply only for $P_O \leq P_{max}$.
 $P_{max} = 30\text{ W}$ for K package
 $P_{max} = 25\text{ W}$ for T package
- Line and load regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC78T00 Series

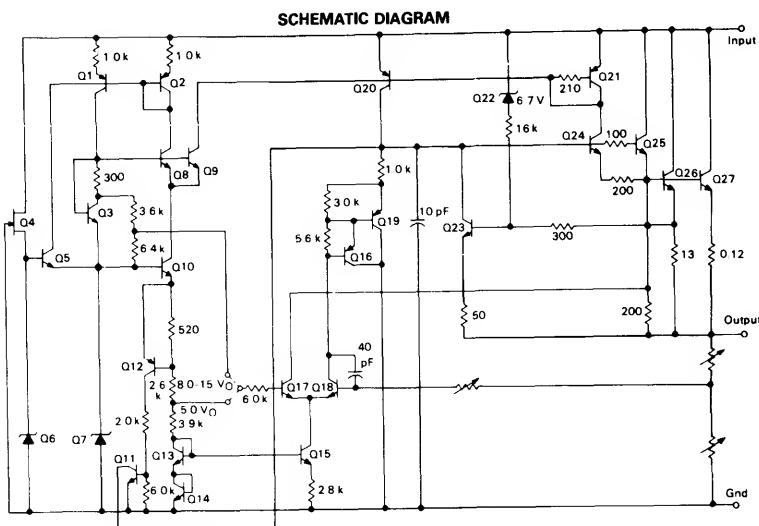
MC78T15AC, C

ELECTRICAL CHARACTERISTICS ($V_{in} = 20\text{ V}$, $I_O = 3.0\text{ A}$, $0^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$, $P_O \leq P_{max}$ [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC78T15AC			MC78T15C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($5.0\text{ mA} \leq I_O \leq 3.0\text{ A}$, $T_J = +25^\circ\text{C}$) ($5.0\text{ mA} \leq I_O \leq 3.0\text{ A}$; $5.0\text{ mA} \leq I_O \leq 2.0\text{ A}$, $17.5\text{ Vdc} \leq V_{in} \leq 30\text{ Vdc}$)	V_O	14.7 14.4	15 15	15.3 15.6	14.4 14.25	15 15	15.6 15.75	Vdc
Line Regulation (Note 2) ($17.6\text{ Vdc} \leq V_{in} \leq 40\text{ Vdc}$, $I_O = 5.0\text{ mA}$, $T_J = +25^\circ\text{C}$; $17.6\text{ Vdc} \leq V_{in} \leq 40\text{ Vdc}$, $I_O = 1.0\text{ A}$, $T_J = +25^\circ\text{C}$; $20\text{ Vdc} \leq V_{in} \leq 26\text{ Vdc}$, $I_O = 3.0\text{ A}$, $T_J = +25^\circ\text{C}$; $18\text{ Vdc} \leq V_{in} \leq 30\text{ Vdc}$, $I_O = 1.0\text{ A}$)	Regline	—	7.5	55	—	7.5	55	mV
Load Regulation (Note 2) ($5.0\text{ mA} \leq I_O \leq 3.0\text{ A}$, $T_J = +25^\circ\text{C}$) ($5.0\text{ mA} \leq I_O \leq 3.0\text{ A}$)	Regload	— —	10 15	30 80	— —	10 15	30 80	mV
Thermal Regulation (Pulse = 10 ms, $P = 20\text{ W}$, $T_A = +25^\circ\text{C}$)	Regtherm	—	0.001	0.01	—	0.002	0.03	% V_O /W
Quiescent Current ($5.0\text{ mA} \leq I_O \leq 3.0\text{ A}$, $T_J = +25^\circ\text{C}$) ($5.0\text{ mA} \leq I_O \leq 3.0\text{ A}$)	I_B	— —	3.5 4.0	5.0 6.0	— —	3.5 4.0	5.0 6.0	mA
Quiescent Current Change ($17.6\text{ Vdc} \leq V_{in} \leq 40\text{ Vdc}$, $I_O = 5.0\text{ mA}$, $T_J = +25^\circ\text{C}$; $5.0\text{ mA} \leq I_O \leq 3.0\text{ A}$, $T_J = +25^\circ\text{C}$; $18\text{ Vdc} \leq V_{in} \leq 30\text{ Vdc}$, $I_O = 1.0\text{ A}$)	ΔI_B	—	0.3	1.0	—	0.3	1.0	mA
Ripple Rejection ($18.5\text{ Vdc} \leq V_{in} \leq 28.5\text{ Vdc}$, $f = 120\text{ Hz}$, $I_O = 2.0\text{ A}$, $T_J = 25^\circ\text{C}$)	RR	55	65	—	55	65	—	dB
Dropout Voltage ($I_O = 3.0\text{ A}$, $T_J = +25^\circ\text{C}$)	$V_{in}-V_O$	—	2.2	2.5	—	2.2	2.5	Vdc
Output Noise Voltage ($10\text{ Hz} \leq f \leq 100\text{ kHz}$, $T_J = +25^\circ\text{C}$)	V_n	—	10	—	—	10	—	$\mu\text{V}/V_O$
Output Resistance ($f = 1.0\text{ kHz}$)	R_O	—	2.0	—	—	2.0	—	m Ω
Short Circuit Current Limit ($V_{in} = 40\text{ Vdc}$, $T_J = +25^\circ\text{C}$)	I_{SC}	—	1.0	—	—	1.0	—	A
Peak Output Current ($T_J = +25^\circ\text{C}$)	I_{max}	—	5.0	—	—	5.0	—	A
Average Temperature Coefficient of Output Voltage ($I_O = 5.0\text{ mA}$)	TCV_O	—	0.6	—	—	0.6	—	mV/ $^\circ\text{C}$

NOTES:

- Although power dissipation is internally limited, specifications apply only for $P_O \leq P_{max}$.
 $P_{max} = 30\text{ W}$ for K package $P_{max} = 25\text{ W}$ for T package
- Line and load regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.



VOLTAGE REGULATOR PERFORMANCE

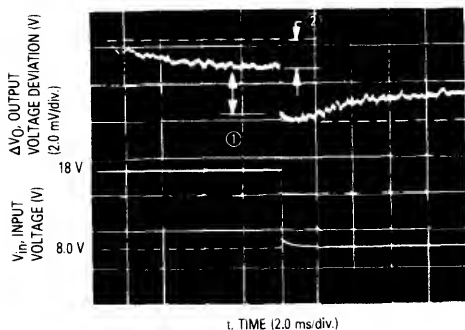
The performance of a voltage regulator is specified by its immunity to changes in load, input voltage, power dissipation, and temperature. Line and load regulation are tested with a pulse of short duration ($< 100 \mu\text{s}$) and are strictly a function of electrical gain. However, pulse widths of longer duration ($> 1.0 \text{ ms}$) are sufficient to affect temperature gradients across the die. These temperature gradients can cause a change in the output voltage, in addition to changes caused by line and load regulation. Longer pulse widths and thermal gradients make it desirable to specify thermal regulation.

Thermal regulation is defined as the change in output voltage caused by a change in dissipated power for a specified time, and is expressed as a percentage output

voltage change per watt. The change in dissipated power can be caused by a change in either the input voltage or the load current. Thermal regulation is a function of I.C. layout and die attach techniques, and usually occurs within 10 ms of a change in power dissipation. After 10 ms, additional changes in the output voltage are due to the temperature coefficient of the device.

Figure 1 shows the line and thermal regulation response of a typical MC78T05AC to a 20 watt input pulse. The variation of the output voltage due to line regulation is labeled ① and the thermal regulation component is labeled ②. Figure 2 shows the load and thermal regulation response of a typical MC78T05AC to a 20 watt load pulse. The output voltage variation due to load regulation is labeled ① and the thermal regulation component is labeled ②.

FIGURE 1 — LINE AND THERMAL REGULATION



MC78T05AC

$V_O = 5.0 \text{ V}$

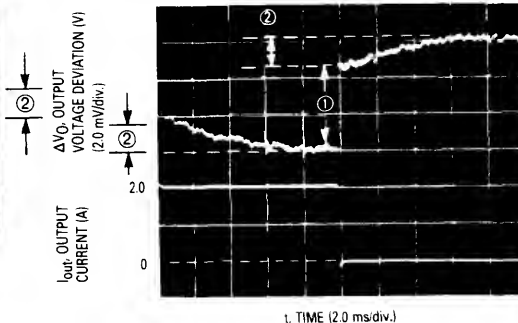
$V_{in} = 8.0 \text{ V} \rightarrow 18 \text{ V} \rightarrow 8.0 \text{ V}$

$I_{out} = 2.0 \text{ A}$

① = $\text{Reg}_{line} = 2.4 \text{ mV}$

② = $\text{Reg}_{therm} = 0.0015\%V_O/W$

FIGURE 2 — LOAD AND THERMAL REGULATION



MC78T05AC

$V_O = 5.0 \text{ V}$

$V_{in} = 15$

$I_{out} = 0 \text{ A} \rightarrow 2.0 \text{ A} \rightarrow 0 \text{ A}$

① = $\text{Reg}_{load} = 4.4 \text{ mV}$

② = $\text{Reg}_{therm} = 0.0015\%V_O/W$

MC78T00 Series

3

FIGURE 3 — TEMPERATURE STABILITY

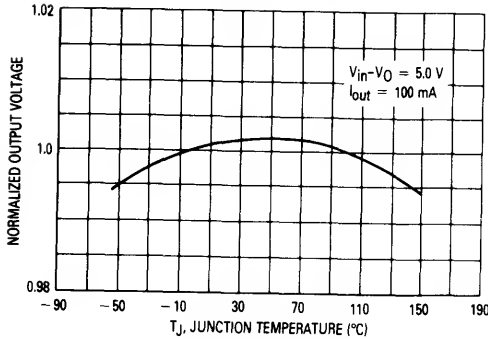


FIGURE 4 — OUTPUT IMPEDANCE

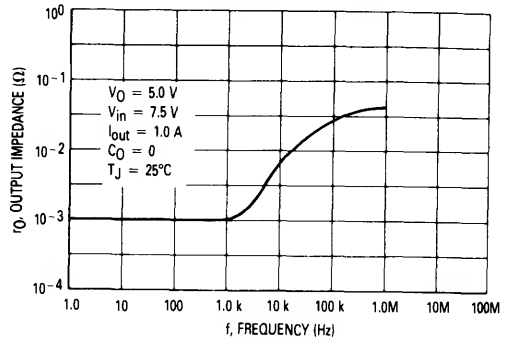


FIGURE 5 — RIPPLE REJECTION versus FREQUENCY

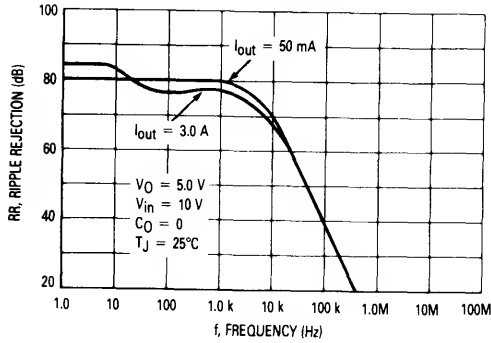


FIGURE 6 — RIPPLE REJECTION versus OUTPUT CURRENT

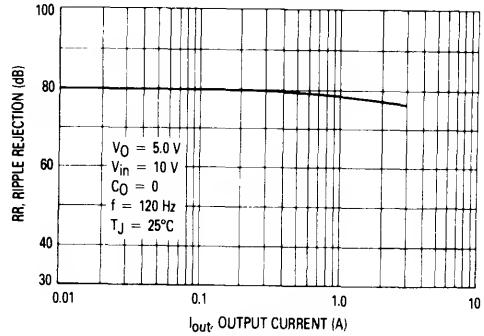


FIGURE 7 — QUIESCENT CURRENT versus INPUT VOLTAGE

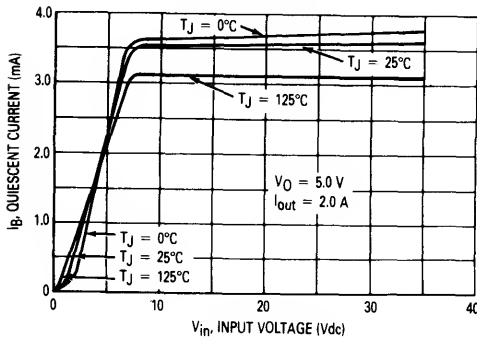
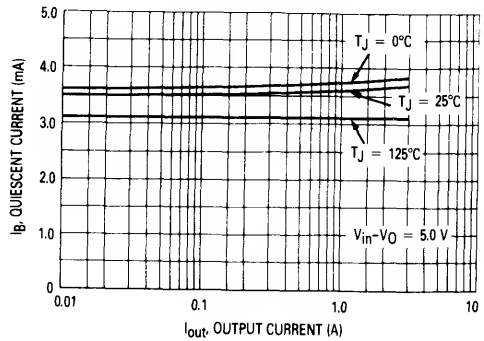


FIGURE 8 — QUIESCENT CURRENT versus OUTPUT CURRENT



MC78T00 Series

3

FIGURE 9 — DROPOUT VOLTAGE

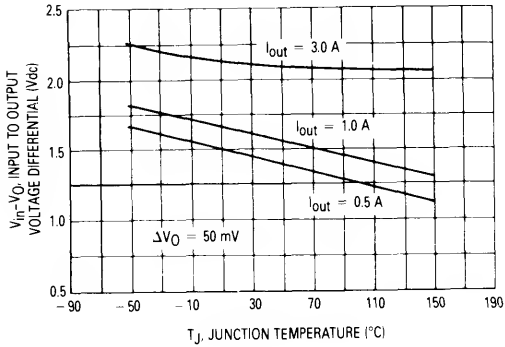


FIGURE 10 — PEAK OUTPUT CURRENT

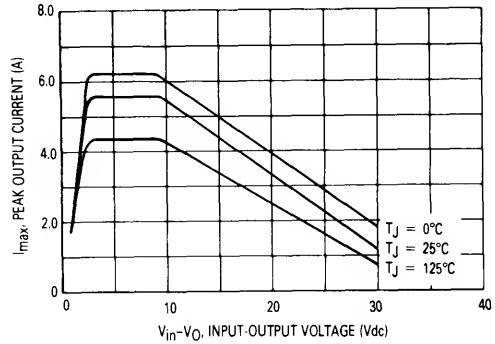


FIGURE 11 — LINE TRANSIENT RESPONSE

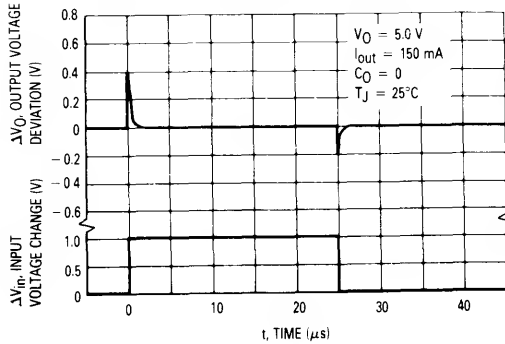


FIGURE 12 — LOAD TRANSIENT RESPONSE

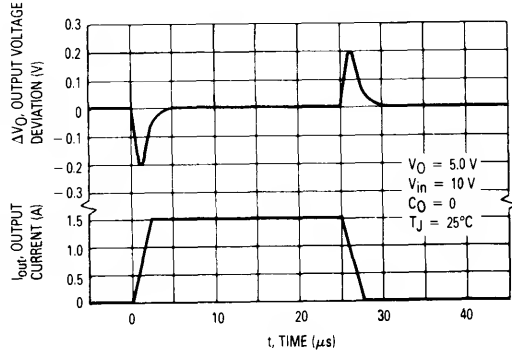


FIGURE 13 — MAXIMUM AVERAGE POWER DISSIPATION FOR MC78T00CK, ACK

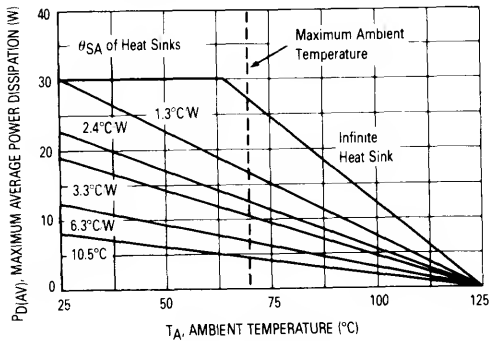
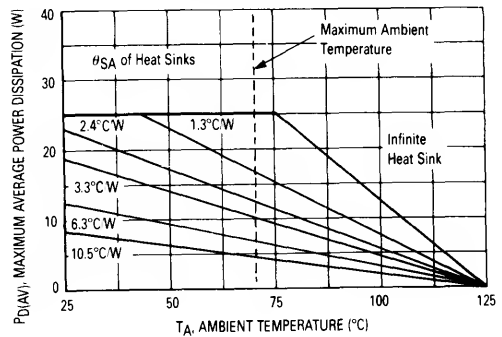


FIGURE 14 — MAXIMUM AVERAGE POWER DISSIPATION FOR MC78T00CT, ACT



APPLICATIONS INFORMATION

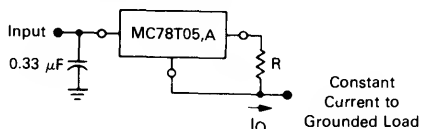
DESIGN CONSIDERATIONS

The MC78T00,A Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a

capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulator's input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

FIGURE 15 — CURRENT REGULATOR



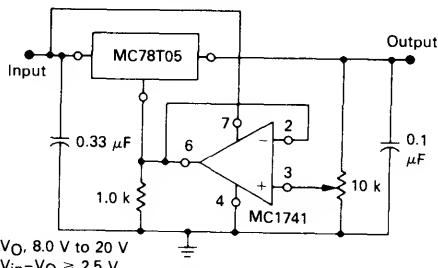
The MC78T05 regulator can also be used as a current source when connected as above. In order to minimize dissipation, the MC78T05 is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5.0 \text{ V}}{R} + I_B$$

$\Delta I_B \approx 0.7 \text{ mA}$ over line, load and temperature changes
 $I_B \approx 3.5 \text{ mA}$

For example, a 2-ampere current source would require R to be a 2.5 ohm, 15 W resistor and the output voltage compliance would be the input voltage less 7.5 volts.

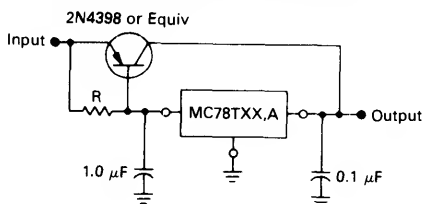
FIGURE 16 — ADJUSTABLE OUTPUT REGULATOR



V_O , 8.0 V to 20 V
 $V_{in} - V_O \geq 2.5 \text{ V}$

The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 3.0 volts greater than the regulator voltage.

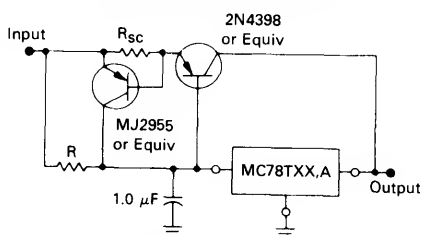
FIGURE 17 — CURRENT BOOST REGULATOR



XX = 2 digits of type number indicating voltage.

The MC78T00,A series can be current boosted with a PNP transistor. The 2N4398 provides current to 15 amperes. Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short-circuit proof. Input-output differential voltage minimum is increased by the V_{BE} of the pass transistor.

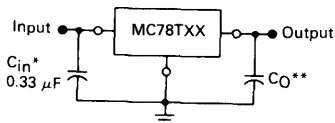
FIGURE 18 — CURRENT BOOST WITH SHORT-CIRCUIT PROTECTION



XX = 2 digits of type number indicating voltage.

The circuit of Figure 17 can be modified to provide supply protection against short circuits by adding a short-circuit sense resistor, R_{SC} , and an additional PNP transistor. The current sensing PNP must be able to handle the short-circuit current of the three-terminal regulator. Therefore, an eight-ampere power transistor is specified.

FIGURE 19 — STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.2 V above the output voltage even during the low point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = C_{IN} is required if regulator is located an appreciable distance from power supply filter. (See Applications Information for details.)

** = C_O is not needed for stability; however, it does improve transient response.

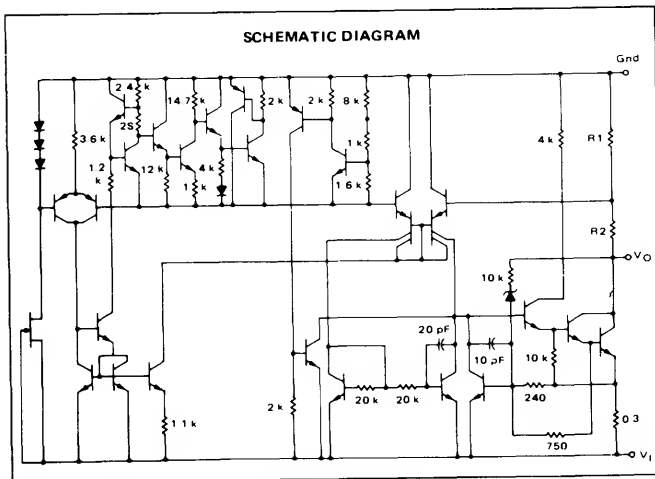
THREE-TERMINAL NEGATIVE VOLTAGE REGULATORS

The MC7900 Series of fixed output negative voltage regulators are intended as complements to the popular MC7800 Series devices. These negative regulators are available in the same seven-voltage options as the MC7800 devices. In addition, one extra voltage option commonly employed in MECL systems is also available in the negative MC7900 Series.

Available in fixed output voltage options from -5.0 to -24 volts, these regulators employ current limiting, thermal shut-down, and safe-area compensation — making them remarkably rugged under most operating conditions. With adequate heat-sinking they can deliver output currents in excess of 1.0 ampere.

- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Available in 2% Voltage Tolerance (See Ordering Information)

SCHEMATIC DIAGRAM



ORDERING INFORMATION

Device	Output Voltage Tolerance	Tested Operating Junction Temp. Range	Package
MC79XXCK	4%	$T_J = 0^{\circ}\text{C to } +125^{\circ}\text{C}$	Metal Power**
MC79XXACK*	2%		Plastic Power
MC79XXCT	4%	$T_J = -40^{\circ}\text{C to } +125^{\circ}\text{C}$	
MC79XXACT*	2%		
MC79XXRT#	4%		

XX indicates nominal voltage.

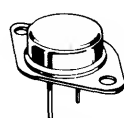
*2% output voltage tolerance available in 5, 12 and 15 volt devices.

**Metal power package available in 5, 12 and 15 volt devices.

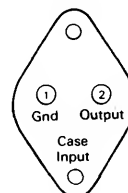
#Automotive temperature range selections are available with special test conditions and additional tests in 5, 12 and 15 volt devices. Contact your local Motorola sales office for information.

MC7900 Series

THREE-TERMINAL NEGATIVE FIXED VOLTAGE REGULATORS



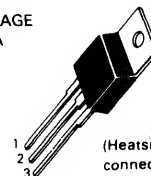
**K SUFFIX
METAL PACKAGE
CASE 1**



(Bottom View)

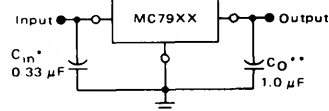
**T SUFFIX
PLASTIC PACKAGE
CASE 221A**

PIN 1. GROUND
2. INPUT
3. OUTPUT



(Heatsink surface connected to Pin 2)

STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V more negative even during the high point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* C_{in} is required if regulator is located an appreciable distance from power supply filter.

** C_O improves stability and transient response.

DEVICE TYPE/NOMINAL OUTPUT VOLTAGE

MC7905	5.0 Volts	MC7912	12 Volts
MC7905.2	5.2 Volts	MC7915	15 Volts
MC7906	6.0 Volts	MC7918	18 Volts
MC7908	8.0 Volts	MC7924	24 Volts

MC7900 Series

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (-5.0 V ≥ V _O ≥ -18 V) (24 V)	V _I	-35 -40	Vdc
Power Dissipation Plastic Package T _A = +25°C Derate above T _A = +25°C T _C = +25°C Derate above T _C = +95°C (See Figure 1)	P _D 1/R _{θJA} P _D 1/R _{θJC}	Internally Limited 15.4 Internally Limited 200	Watts mW/°C Watts mW/°C
Metal Package T _A = +25°C Derate above T _A = +25°C T _C = +25°C Derate above T _C = +65°C	P _D 1/R _{θJA} P _D 1/R _{θJC}	Internally Limited 22.2 Internally Limited 182	Watts mW/°C Watts mW/°C
Storage Junction Temperature Range	T _{stg}	-65 to +150	°C
Junction Temperature Range	T _J	0 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient — Plastic Package — Metal Package	R _{θJA}	65 45	°C/W
Thermal Resistance, Junction to Case — Plastic Package — Metal Package	R _{θJC}	5.0 5.5	°C/W

MC7905C ELECTRICAL CHARACTERISTICS (V_I = -10 V, I_O = 500 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T _J = +25°C)	V _O	-4.8	-5.0	-5.2	Vdc
Line Regulation (Note 1) (T _J = +25°C, I _O = 100 mA) -7.0 Vdc ≥ V _I ≥ -25 Vdc -8.0 Vdc ≥ V _I ≥ -12 Vdc (T _J = +25°C, I _O = 500 mA) -7.0 Vdc ≥ V _I ≥ -25 Vdc -8.0 Vdc ≥ V _I ≥ -12 Vdc	Reg _{line}	— — — —	7.0 2.0 35 8.0	50 25 100 50	mV
Load Regulation (T _J = +25°C) (Note 1) 5.0 mA ≤ I _O ≤ 1.5 A 250 mA ≤ I _O ≤ 750 mA	Reg _{load}	— —	11 4.0	100 50	mV
Output Voltage -7.0 Vdc ≥ V _I ≥ -20 Vdc, 5.0 mA ≤ I _O ≤ 1.0 A, P ≤ 15 W	V _O	-4.75	—	-5.25	Vdc
Input Bias Current (T _J = +25°C)	I _{IB}	—	4.3	8.0	mA
Input Bias Current Change -7.0 Vdc ≥ V _I ≥ -25 Vdc 5.0 mA ≤ I _O ≤ 1.5 A	ΔI _{IB}	— —	— —	1.3 0.5	mA
Output Noise Voltage (T _A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e _{on}	—	40	—	μV
Ripple Rejection (I _O = 20 mA, f = 120 Hz)	RR	—	70	—	dB
Dropout Voltage I _O = 1.0 A, T _J = +25°C	V _I - V _O	—	2.0	—	Vdc
Average Temperature Coefficient of Output Voltage I _O = 5.0 mA, 0°C ≤ T _J ≤ +125°C	ΔV _O /ΔT	—	-1.0	—	mV/°C

Note

1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7900 Series

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MC7905AC ELECTRICAL CHARACTERISTICS ($V_I = -10\text{ V}$, $I_O = 500\text{ mA}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	-4.9	-5.0	-5.1	Vdc
Line Regulation (Note 1)	Reg _{line}	—	2.0	25	mV
-8.0 Vdc $\geq V_I \geq -12\text{ Vdc}$; $I_O = 1.0\text{ A}$, $T_J = 25^\circ\text{C}$		—	7.0	50	
-8.0 Vdc $\geq V_I \geq -12\text{ Vdc}$; $I_O = 1.0\text{ A}$		—	7.0	50	
-7.5 Vdc $\geq V_I \geq -25\text{ Vdc}$; $I_O = 500\text{ mA}$		—	6.0	50	
-7.0 Vdc $\geq V_I \geq -20\text{ Vdc}$; $I_O = 1.0\text{ A}$, $T_J = +25^\circ\text{C}$		—			
Load Regulation (Note 1)	Reg _{load}	—	11	100	mV
5.0 mA $\leq I_O \leq 1.5\text{ A}$, $T_J = +25^\circ\text{C}$		—	4.0	50	
250 mA $\leq I_O \leq 750\text{ mA}$		—	9.0	100	
5.0 mA $\leq I_O \leq 1.0\text{ A}$		—			
Output Voltage	V_O	-4.80	—	-5.20	Vdc
-7.5 Vdc $\geq V_I \geq -20\text{ Vdc}$, 5.0 mA $\leq I_O \leq 1.0\text{ A}$, $P \leq 15\text{ W}$		—	4.4	8.0	mA
Input Bias Current	I_{IB}	—	—	—	mA
Input Bias Current Change	ΔI_{IB}	—	—	1.3	mA
-7.5 Vdc $\geq V_I \geq -25\text{ Vdc}$		—	—	0.5	
5.0 mA $\leq I_O \leq 1.0\text{ A}$		—	—	0.5	
5.0 mA $\leq I_O \leq 1.5\text{ A}$, $T_J = 25^\circ\text{C}$		—			
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$)	e_{on}	—	40	—	μV
Ripple Rejection ($I_O = 20\text{ mA}$, $f = 120\text{ Hz}$)	RR	—	70	—	dB
Dropout Voltage	$V_I - V_O$	—	2.0	—	Vdc
$I_O = 1.0\text{ A}$, $T_J = +25^\circ\text{C}$		—			
Average Temperature Coefficient of Output Voltage	$\Delta V_O / \Delta T$	—	-1.0	—	mV/ $^\circ\text{C}$
$I_O = 5.0\text{ mA}$, $0^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$					

MC7905.2C ELECTRICAL CHARACTERISTICS ($V_I = -10\text{ V}$, $I_O = 500\text{ mA}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	-5.0	-5.2	-5.4	Vdc
Line Regulation (Note 1)	Reg _{line}	—	8.0	52	mV
($T_J = +25^\circ\text{C}$, $I_O = 100\text{ mA}$)		—	2.2	27	
-7.2 Vdc $\geq V_I \geq -25\text{ Vdc}$		—	37	105	
-8.0 Vdc $\geq V_I \geq -12\text{ Vdc}$		—	8.5	52	
($T_J = +25^\circ\text{C}$, $I_O = 500\text{ mA}$)		—			
-7.2 Vdc $\geq V_I \geq -25\text{ Vdc}$		—			
-8.0 Vdc $\geq V_I \geq -12\text{ Vdc}$		—			
Load Regulation ($T_J = +25^\circ\text{C}$) (Note 1)	Reg _{load}	—	12	105	mV
5.0 mA $\leq I_O \leq 1.5\text{ A}$		—	4.5	52	
250 mA $\leq I_O \leq 750\text{ mA}$		—			
Output Voltage	V_O	-4.95	—	-5.45	Vdc
-7.2 Vdc $\geq V_I \geq -20\text{ Vdc}$, 5.0 mA $\leq I_O \leq 1.0\text{ A}$, $P \leq 15\text{ W}$		—	4.3	8.0	mA
Input Bias Current ($T_J = +25^\circ\text{C}$)	I_{IB}	—	—	—	mA
Input Bias Current Change	ΔI_{IB}	—	—	1.3	mA
-7.2 Vdc $\geq V_I \geq -25\text{ Vdc}$		—	—	0.5	
5.0 mA $\leq I_O \leq 1.5\text{ A}$		—			
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$)	e_{on}	—	42	—	μV
Ripple Rejection ($I_O = 20\text{ mA}$, $f = 120\text{ Hz}$)	RR	—	68	—	dB
Dropout Voltage	$V_I - V_O$	—	2.0	—	Vdc
$I_O = 1.0\text{ A}$, $T_J = +25^\circ\text{C}$		—			
Average Temperature Coefficient of Output Voltage	$\Delta V_O / \Delta T$	—	-1.0	—	mV/ $^\circ\text{C}$
$I_O = 5.0\text{ mA}$, $0^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$					

Note

1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7900 Series

MC7906C ELECTRICAL CHARACTERISTICS ($V_I = -11\text{ V}$, $I_O = 500\text{ mA}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	-5.75	-6.0	-6.25	Vdc
Line Regulation (Note 1) ($T_J = +25^\circ\text{C}$, $I_O = 100\text{ mA}$) -8.0 Vdc $\geq V_I \geq -25\text{ Vdc}$ -9.0 Vdc $\geq V_I \geq -13\text{ Vdc}$ ($T_J = +25^\circ\text{C}$, $I_O = 500\text{ mA}$) -8.0 Vdc $\geq V_I \geq -25\text{ Vdc}$ -9.0 Vdc $\geq V_I \geq -13\text{ Vdc}$	Reg_{line}	— — — —	9.0 3.0 43 10	60 30 120 60	mV
Load Regulation ($T_J = +25^\circ\text{C}$) (Note 1) 5.0 mA $\leq I_O \leq 1.5\text{ A}$ 250 mA $\leq I_O \leq 750\text{ mA}$	Reg_{load}	— —	13 5.0	120 60	mV
Output Voltage -8.0 Vdc $\geq V_I \geq -21\text{ Vdc}$, 5.0 mA $\leq I_O \leq 1.0\text{ A}$, $P \leq 15\text{ W}$	V_O	-5.7	—	-6.3	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$)	I_{IB}	—	4.3	8.0	mA
Input Bias Current Change -8.0 Vdc $\geq V_I \geq -25\text{ Vdc}$ 5.0 mA $\leq I_O \leq 1.5\text{ A}$	ΔI_{IB}	— —	— —	1.3 0.5	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, 10 Hz $\leq f \leq 100\text{ kHz}$)	e_{on}	—	45	—	μV
Ripple Rejection ($I_O = 20\text{ mA}$, $f = 120\text{ Hz}$)	RR	—	65	—	dB
Dropout Voltage $I_O = 1.0\text{ A}$, $T_J = +25^\circ\text{C}$	$V_I - V_O$	—	2.0	—	Vdc
Average Temperature Coefficient of Output Voltage $I_O = 5.0\text{ mA}$, $0^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$	$\Delta V_O / \Delta T$	—	-1.0	—	mV/ $^\circ\text{C}$

MC7908C ELECTRICAL CHARACTERISTICS ($V_I = -14\text{ V}$, $I_O = 500\text{ mA}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	-7.7	-8.0	-8.3	Vdc
Line Regulation (Note 1) ($T_J = +25^\circ\text{C}$, $I_O = 100\text{ mA}$) -10.5 Vdc $\geq V_I \geq -25\text{ Vdc}$ -11 Vdc $\geq V_I \geq -17\text{ Vdc}$ ($T_J = +25^\circ\text{C}$, $I_O = 500\text{ mA}$) -10.5 Vdc $\geq V_I \geq -25\text{ Vdc}$ -11 Vdc $\geq V_I \geq -17\text{ Vdc}$	Reg_{line}	— — — —	12 5.0 50 22	80 40 160 80	mV
Load Regulation ($T_J = +25^\circ\text{C}$) (Note 1) 5.0 mA $\leq I_O \leq 1.5\text{ A}$ 250 mA $\leq I_O \leq 750\text{ mA}$	Reg_{load}	— —	26 9.0	160 80	mV
Output Voltage -10.5 Vdc $\geq V_I \geq -23\text{ Vdc}$, 5.0 mA $\leq I_O \leq 1.0\text{ A}$, $P \leq 15\text{ W}$	V_O	-7.6	—	-8.4	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$)	I_{IB}	—	4.3	8.0	mA
Input Bias Current Change -10.5 Vdc $\geq V_I \geq -25\text{ Vdc}$ 5.0 mA $\leq I_O \leq 1.5\text{ A}$	ΔI_{IB}	— —	— —	1.0 0.5	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, 10 Hz $\leq f \leq 100\text{ kHz}$)	e_{on}	—	52	—	μV
Ripple Rejection ($I_O = 20\text{ mA}$, $f = 120\text{ Hz}$)	RR	—	62	—	dB
Dropout Voltage $I_O = 1.0\text{ A}$, $T_J = +25^\circ\text{C}$	$V_I - V_O$	—	2.0	—	Vdc
Average Temperature Coefficient of Output Voltage $I_O = 5.0\text{ mA}$, $0^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$	$\Delta V_O / \Delta T$	—	-1.0	—	mV/ $^\circ\text{C}$

Note

- 1 Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7900 Series

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MC7915C ELECTRICAL CHARACTERISTICS ($V_I = -23\text{ V}$, $I_O = 500\text{ mA}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	-14.4	-15	-15.6	Vdc
Line Regulation (Note 1) ($T_J = +25^\circ\text{C}$, $I_O = 100\text{ mA}$) -17.5 Vdc $\geq V_I \geq$ -30 Vdc -20 Vdc $\geq V_I \geq$ -26 Vdc ($T_J = +25^\circ\text{C}$, $I_O = 500\text{ mA}$) -17.5 Vdc $\geq V_I \geq$ -30 Vdc -20 Vdc $\geq V_I \geq$ -26 Vdc	Reg _{line}	— — — —	14 6.0 57 27	150 75 300 150	mV
Load Regulation ($T_J = +25^\circ\text{C}$) (Note 1) 5.0 mA $\leq I_O \leq$ 1.5 A 250 mA $\leq I_O \leq$ 750 mA	Reg _{load}	— —	68 25	300 150	mV
Output Voltage -17.5 Vdc $\geq V_I \geq$ -30 Vdc, 5.0 mA $\leq I_O \leq$ 1.0 A, $P \leq$ 15 W	V_O	-14.25	—	-15.75	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$)	I_{IB}	—	4.4	8.0	mA
Input Bias Current Change -17.5 Vdc $\geq V_I \geq$ -30 Vdc 5.0 mA $\leq I_O \leq$ 1.5 A	ΔI_{IB}	— —	— —	1.0 0.5	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, 10 Hz $\leq f \leq$ 100 kHz)	e_{on}	—	90	—	μV
Ripple Rejection ($I_O = 20\text{ mA}$, $f = 120\text{ Hz}$)	RR	—	60	—	dB
Dropout Voltage $I_O = 1.0\text{ A}$, $T_J = +25^\circ\text{C}$	$V_I - V_O$	—	2.0	—	Vdc
Average Temperature Coefficient of Output Voltage $I_O = 5.0\text{ mA}$, $0^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$	$\Delta V_O / \Delta T$	—	-1.0	—	mV/ $^\circ\text{C}$

MC7915AC ELECTRICAL CHARACTERISTICS ($V_I = -23\text{ V}$, $I_O = 500\text{ mA}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	-14.7	-15	-15.3	Vdc
Line Regulation (Note 1) -20 Vdc $\geq V_I \geq$ -26 Vdc, $I_O = 1.0\text{ A}$, $T_J = 25^\circ\text{C}$ -20 Vdc $\geq V_I \geq$ -26 Vdc, $I_O = 1.0\text{ A}$ -17.9 Vdc $\geq V_I \geq$ -30 Vdc, $I_O = 500\text{ mA}$ -17.5 Vdc $\geq V_I \geq$ -30 Vdc, $I_O = 1.0\text{ A}$, $T_J = 25^\circ\text{C}$	Reg _{line}	— — — —	27 57 57 57	75 150 150 150	mV
Load Regulation (Note 1) 5.0 mA $\leq I_O \leq$ 1.5 A, $T_J = 25^\circ\text{C}$ 250 mA $\leq I_O \leq$ 750 mA 5.0 mA $\leq I_O \leq$ 1.0 A	Reg _{load}	— — —	68 25 40	150 75 150	mV
Output Voltage -17.9 Vdc $\geq V_I \geq$ -30 Vdc, 5.0 mA $\leq I_O \leq$ 1.0 A, $P \leq$ 15 W	V_O	-14.4	—	-15.6	Vdc
Input Bias Current	I_{IB}	—	4.4	8.0	mA
Input Bias Current Change -17.5 Vdc $\geq V_I \geq$ -30 Vdc 5.0 mA $\leq I_O \leq$ 1.0 A 5.0 mA $\leq I_O \leq$ 1.5 A, $T_J = 25^\circ\text{C}$	ΔI_{IB}	— — —	— — —	0.8 0.5 0.5	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, 10 Hz $\leq f \leq$ 100 kHz)	e_{on}	—	90	—	μV
Ripple Rejection ($I_O = 20\text{ mA}$, $f = 120\text{ Hz}$)	RR	—	60	—	dB
Dropout Voltage $I_O = 1.0\text{ A}$, $T_J = +25^\circ\text{C}$	$V_I - V_O$	—	2.0	—	Vdc
Average Temperature Coefficient of Output Voltage $I_O = 5.0\text{ mA}$, $0^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$	$\Delta V_O / \Delta T$	—	-1.0	—	mV/ $^\circ\text{C}$

Note

1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7900 Series

MC7912C ELECTRICAL CHARACTERISTICS ($V_I = -19\text{ V}$, $I_O = 500\text{ mA}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	-11.5	-12	-12.5	Vdc
Line Regulation (Note 1) ($T_J = +25^\circ\text{C}$, $I_O = 100\text{ mA}$) -14.5 Vdc $\geq V_I \geq -30\text{ Vdc}$ -16 Vdc $\geq V_I \geq -22\text{ Vdc}$ ($T_J = +25^\circ\text{C}$, $I_O = 500\text{ mA}$) -14.5 Vdc $\geq V_I \geq -30\text{ Vdc}$ -16 Vdc $\geq V_I \geq -22\text{ Vdc}$	Regline	— — — —	13 6.0 55 24	120 60 240 120	mV
Load Regulation ($T_J = +25^\circ\text{C}$) (Note 1) 5.0 mA $\leq I_O \leq 1.5\text{ A}$ 250 mA $\leq I_O \leq 750\text{ mA}$	Regload	— —	46 17	240 120	mV
Output Voltage -14.5 Vdc $\geq V_I \geq -27\text{ Vdc}$, 5.0 mA $\leq I_O \leq 1.0\text{ A}$, $P \leq 15\text{ W}$	V_O	-11.4	—	-12.6	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$)	I_{IB}	—	4.4	8.0	mA
Input Bias Current Change -14.5 Vdc $\geq V_I \geq -30\text{ Vdc}$ 5.0 mA $\leq I_O \leq 1.5\text{ A}$	ΔI_{IB}	— —	— —	1.0 0.5	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, 10 Hz $\leq f \leq 100\text{ kHz}$)	e_{on}	—	75	—	μV
Ripple Rejection ($I_O = 20\text{ mA}$, $f = 120\text{ Hz}$)	RR	—	61	—	dB
Dropout Voltage $I_O = 1.0\text{ A}$, $T_J = +25^\circ\text{C}$	$V_I - V_O$	—	2.0	—	Vdc
Average Temperature Coefficient of Output Voltage $I_O = 5.0\text{ mA}$, $0^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$	$\Delta V_O / \Delta T$	—	-1.0	—	mV/ $^\circ\text{C}$

MC7912AC ELECTRICAL CHARACTERISTICS ($V_I = -19\text{ V}$, $I_O = 500\text{ mA}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	-11.75	-12	-12.25	Vdc
Line Regulation (Note 1) -16 Vdc $\geq V_I \geq -22\text{ Vdc}$, $I_O = 1.0\text{ A}$, $T_J = 25^\circ\text{C}$ -16 Vdc $\geq V_I \geq -22\text{ Vdc}$, $I_O = 1.0\text{ A}$ -14.8 Vdc $\geq V_I \geq -30\text{ Vdc}$, $I_O = 500\text{ mA}$ -14.5 Vdc $\geq V_I \geq -27\text{ Vdc}$, $I_O = 1.0\text{ A}$, $T_J = 25^\circ\text{C}$	Regline	— — — —	6.0 24 24 13	60 120 120 120	mV
Load Regulation (Note 1) 5.0 mA $\leq I_O \leq 1.5\text{ A}$, $T_J = 25^\circ\text{C}$ 250 mA $\leq I_O \leq 750\text{ mA}$ 5.0 mA $\leq I_O \leq 1.0\text{ A}$	Regload	— — —	46 17 35	150 75 150	mV
Output Voltage -14.8 Vdc $\geq V_I \geq -27\text{ Vdc}$, 5.0 mA $\leq I_O \leq 1.0\text{ A}$, $P \leq 15\text{ W}$	V_O	-11.5	—	-12.5	Vdc
Input Bias Current	I_{IB}	—	4.4	8.0	mA
Input Bias Current Change -15 Vdc $\geq V_I \geq -30\text{ Vdc}$ 5.0 mA $\leq I_O \leq 1.0\text{ A}$ 5.0 mA $\leq I_O \leq 1.5\text{ A}$, $T_J = 25^\circ\text{C}$	ΔI_{IB}	— — —	— — —	0.8 0.5 0.5	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, 10 Hz $\leq f \leq 100\text{ kHz}$)	e_{on}	—	75	—	μV
Ripple Rejection ($I_O = 20\text{ mA}$, $f = 120\text{ Hz}$)	RR	—	61	—	dB
Dropout Voltage $I_O = 1.0\text{ A}$, $T_J = +25^\circ\text{C}$	$V_I - V_O$	—	2.0	—	Vdc
Average Temperature Coefficient of Output Voltage $I_O = 5.0\text{ mA}$, $0^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$	$\Delta V_O / \Delta T$	—	-1.0	—	mV/ $^\circ\text{C}$

Note

1 Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7900 Series

MC7918C ELECTRICAL CHARACTERISTICS ($V_I = -27\text{ V}$, $I_O = 500\text{ mA}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	-17.3	-18	-18.7	Vdc
Line Regulation (Note 1) ($T_J = +25^\circ\text{C}$, $I_O = 100\text{ mA}$) -21 Vdc $\geq V_I \geq$ -33 Vdc -24 Vdc $\geq V_I \geq$ -30 Vdc ($T_J = +25^\circ\text{C}$, $I_O = 500\text{ mA}$) -21 Vdc $\geq V_I \geq$ -33 Vdc -24 Vdc $\geq V_I \geq$ -30 Vdc	Reg _{line}	—	25 10	180 90	mV
Load Regulation ($T_J = +25^\circ\text{C}$) (Note 1) 5.0 mA $\leq I_O \leq$ 1.5 A 250 mA $\leq I_O \leq$ 750 mA	Reg _{load}	—	110 55	360 180	mV
Output Voltage -21 Vdc $\geq V_I \geq$ -33 Vdc, 5.0 mA $\leq I_O \leq$ 1.0 A, $P \leq$ 15 W	V_O	-17.1	—	-18.9	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$)	I_{IB}	—	4.5	8.0	mA
Input Bias Current Change -21 Vdc $\geq V_I \geq$ -33 Vdc 5.0 mA $\leq I_O \leq$ 1.5 A	ΔI_{IB}	—	—	1.0 0.5	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, 10 Hz $\leq f \leq$ 100 kHz)	e_{on}	—	110	—	μV
Ripple Rejection ($I_O = 20\text{ mA}$, $f = 120\text{ Hz}$)	RR	—	59	—	dB
Dropout Voltage $I_O = 1.0\text{ A}$, $T_J = +25^\circ\text{C}$	$V_I - V_O$	—	2.0	—	Vdc
Average Temperature Coefficient of Output Voltage $I_O = 5.0\text{ mA}$, $0^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$	$\Delta V_O / \Delta T$	—	-1.0	—	mV/ $^\circ\text{C}$

MC7924C ELECTRICAL CHARACTERISTICS ($V_I = -33\text{ V}$, $I_O = 500\text{ mA}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	-23	-24	-25	Vdc
Line Regulation (Note 1) ($T_J = +25^\circ\text{C}$, $I_O = 100\text{ mA}$) -27 Vdc $\geq V_I \geq$ -38 Vdc -30 Vdc $\geq V_I \geq$ -36 Vdc ($T_J = +25^\circ\text{C}$, $I_O = 500\text{ mA}$) -27 Vdc $\geq V_I \geq$ -38 Vdc -30 Vdc $\geq V_I \geq$ -36 Vdc	Reg _{line}	—	31 14	240 120	mV
Load Regulation ($T_J = +25^\circ\text{C}$) (Note 1) 5.0 mA $\leq I_O \leq$ 1.5 A 250 mA $\leq I_O \leq$ 750 mA	Reg _{load}	—	150 85	480 240	mV
Output Voltage -27 Vdc $\geq V_I \geq$ -38 Vdc, 5.0 mA $\leq I_O \leq$ 1.0 A, $P \leq$ 15 W	V_O	-22.8	—	-25.2	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$)	I_{IB}	—	4.6	8.0	mA
Input Bias Current Change -27 Vdc $\geq V_I \geq$ -38 Vdc 5.0 mA $\leq I_O \leq$ 1.5 A	ΔI_{IB}	—	—	1.0 0.5	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, 10 Hz $\leq f \leq$ 100 kHz)	e_{on}	—	170	—	μV
Ripple Rejection ($I_O = 20\text{ mA}$, $f = 120\text{ Hz}$)	RR	—	56	—	dB
Dropout Voltage $I_O = 1.0\text{ A}$, $T_J = +25^\circ\text{C}$	$V_I - V_O$	—	2.0	—	Vdc
Average Temperature Coefficient of Output Voltage $I_O = 5.0\text{ mA}$, $0^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$	$\Delta V_O / \Delta T$	—	-1.0	—	mV/ $^\circ\text{C}$

Note:

1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7900 Series

TYPICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 1 – WORST CASE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE

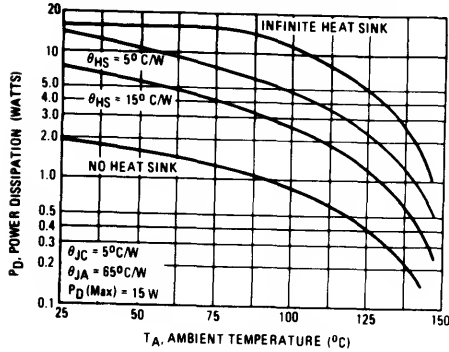


FIGURE 2 – WORST CASE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE

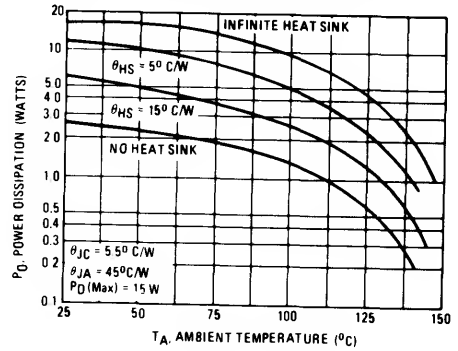


FIGURE 3 – PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE

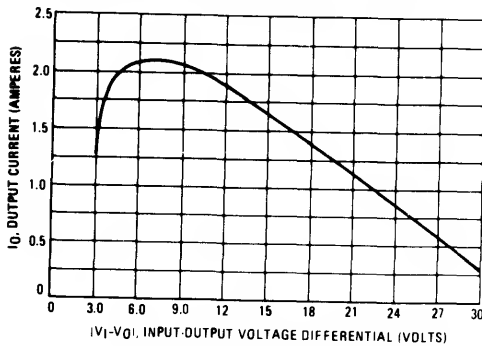


FIGURE 4 – RIPPLE REJECTION AS A FUNCTION OF FREQUENCY

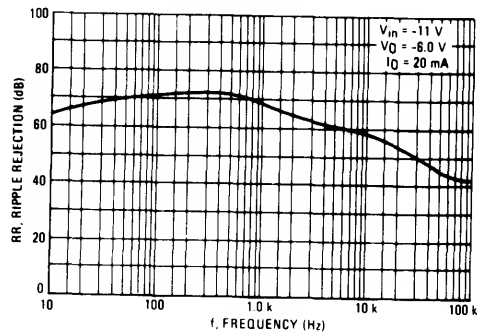


FIGURE 5 – RIPPLE REJECTION AS A FUNCTION OF OUTPUT VOLTAGES

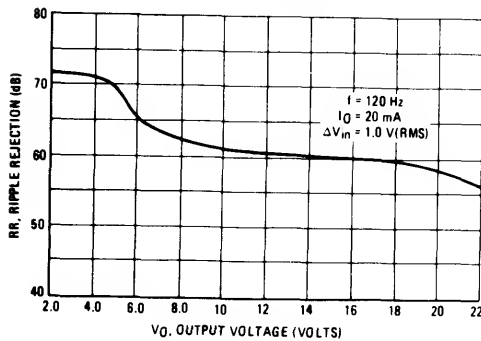
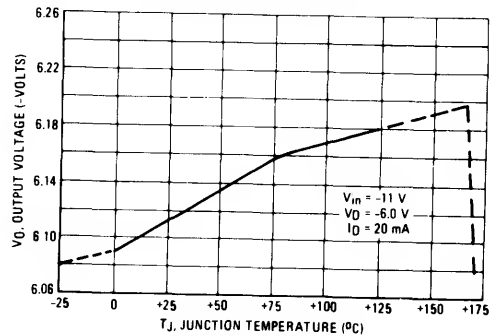


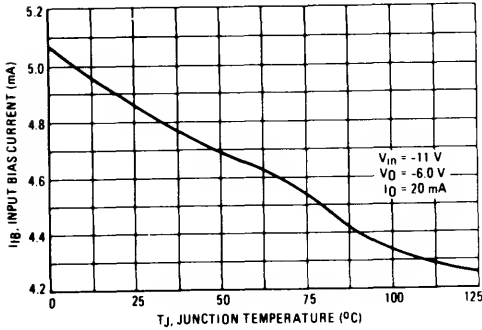
FIGURE 6 – OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



MC7900 Series

TYPICAL CHARACTERISTICS (continued)

FIGURE 7 — QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE



DEFINITIONS

Line Regulation The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation The maximum total device dissipation for which the regulator will operate within specifications.

Input Bias Current That part of the input current that is not delivered to the load.

Output Noise Voltage The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long Term Stability Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.

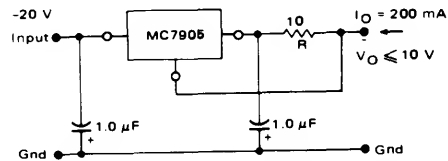
APPLICATIONS INFORMATION

Design Considerations

The MC7900 Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high frequency characteristics to insure stable operation under all load conditions. A 0.33 μ F or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.

FIGURE 8 — CURRENT REGULATOR

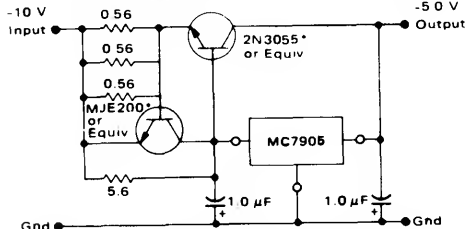


The MC7905, -5.0 V regulator can be used as a constant current source when connected as above. The output current is the sum of resistor R current and quiescent bias current as follows:

$$I_O = \frac{5.0 \text{ V}}{R} + I_B$$

The quiescent current for this regulator is typically 4.3 mA. The 5.0 volt regulator was chosen to minimize dissipation and to allow the output voltage to operate to within 6.0 V below the input voltage.

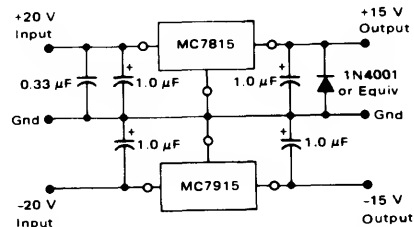
FIGURE 9 — CURRENT BOOST REGULATOR
(-5.0 V @ 4.0 A, with 5.0 A current limiting)



*Mounted on common heat sink. Motorola MS-10 or equivalent.

When a boost transistor is used, short-circuit currents are equal to the sum of the series pass and regulator limits, which are measured at 3.2 A and 1.8 A respectively in this case. Series pass limiting is approximately equal to 0.6 V/R_{SC}. Operation beyond this point to the peak current capability of the MC7905C is possible if the regulator is mounted on a heat sink; otherwise thermal shutdown will occur when the additional load current is picked up by the regulator.

FIGURE 10 — OPERATIONAL AMPLIFIER SUPPLY
(± 15 V @ 1.0 A)



The MC7815 and MC7915 positive and negative regulators may be connected as shown to obtain a dual power supply for operational amplifiers. A clamp diode should be used at the output of the MC7815 to prevent potential latch-up problems whenever the output of the positive regulator (MC7815) is drawn below ground with an output current greater than 200 mA.

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

3

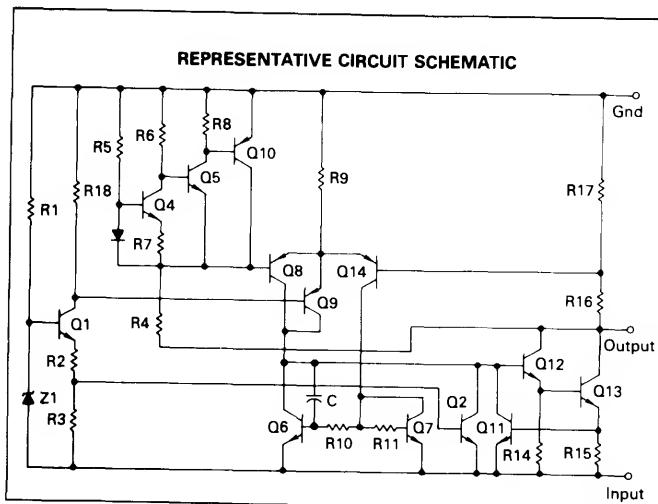
THREE-TERMINAL LOW CURRENT NEGATIVE VOLTAGE REGULATORS

The MC79L00 Series negative voltage regulators are inexpensive, easy-to-use devices suitable for numerous applications requiring up to 100 mA. Like the higher powered MC7900 Series negative regulators, this series features thermal shutdown and current limiting, making them remarkably rugged. In most applications, no external components are required for operation.

The MC79L00 devices are useful for on-card regulation or any other application where a regulated negative voltage at a modest current level is needed. These regulators offer substantial advantage over the common resistor/zener diode approach.

- No External Components Required
- Internal Short-Circuit Current Limiting
- Internal Thermal Overload Protection
- Low Cost
- Complementary Positive Regulators Offered (MC78L00 Series)
- Available in Either $\pm 5\%$ (AC) or $\pm 10\%$ (C) Selections

REPRESENTATIVE CIRCUIT SCHEMATIC



Device No. $\pm 10\%$	Device No. $\pm 5\%$	Nominal Voltage
MC79L05C	MC79L05AC	-5.0
MC79L12C	MC79L12AC	-12
MC79L15C	MC79L15AC	-15
MC79L18C	MC79L18AC	-18
MC79L24C	MC79L24AC	-24

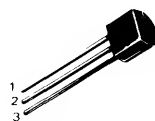
#Automotive temperature range selections are available with special test conditions and additional tests in 5, 12 and 15 volt devices. Contact your local Motorola sales office for information.

MC79L00,A Series

THREE-TERMINAL LOW CURRENT NEGATIVE FIXED VOLTAGE REGULATORS

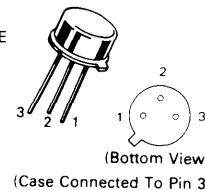
P SUFFIX PLASTIC PACKAGE CASE 29

PIN 1 GROUND
2 INPUT
3 OUTPUT



G SUFFIX METAL PACKAGE CASE 79

PIN 1 GROUND
2 OUTPUT
3 INPUT



D SUFFIX PLASTIC PACKAGE CASE 751 (SOP-8)

PIN 1 V_{OUT} 5 GND
2 V_{IN} 6 V_{IN}
3 V_{IN} 7 V_{IN}
4 NC 8 NC

SOP-8 is an internally modified SO-8 Package. Pins 2, 3, 6 and 7 are electrically common to the die attach flag. This internal lead frame modification decreases package thermal resistance and increases power dissipation capability when appropriately mounted on a printed circuit board. SOP-8 conforms to all external dimensions of the standard SO-8 Package.

ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
MC79LXXACD*	$T_J = 0^\circ\text{C to } +125^\circ\text{C}$	SOP-8
MC79LXXACG*		Metal Can
MC79LXXACP		Plastic Power
MC79LXXCG*		Metal Can
MC79LXXCP		Plastic Power
MC79LXXABP#	$T_J = -40^\circ\text{C to } +125^\circ\text{C}$	
XX indicates nominal voltage		
*Available in 5, 12 and 15 volt devices		

MC79L00,A Series

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MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (-5 V) (-12, -15, -18 V) (-24 V)	V _I	-30 -35 -40	Vdc
Storage Temperature Range	T _{stg}	-65 to +150	°C
Junction Temperature Range	T _J	0 to +150	°C

MC79L05C, AC Series ELECTRICAL CHARACTERISTICS (V_I = -10 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	MC79L05C			MC79L05AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T _J = +25°C)	V _O	-4.6	-5.0	-5.4	-4.8	-5.0	-5.2	Vdc
Input Regulation (T _J = +25°C) -7.0 Vdc ≥ V _I ≥ -20 Vdc -8.0 Vdc ≥ V _I ≥ -20 Vdc	Reg _{line}	—	—	200 150	—	—	150 100	mV
Load Regulation T _J = +25°C, 1.0 mA ≤ I _O ≤ 100 mA 1.0 mA ≤ I _O ≤ 40 mA	Reg _{load}	—	—	60 30	—	—	60 30	mV
Output Voltage -7.0 Vdc ≥ V _I ≥ -20 Vdc, 1.0 mA ≤ I _O ≤ 40 mA V _I = -10 Vdc, 1.0 mA ≤ I _O ≤ 70 mA	V _O	-4.5 -4.5	—	-5.5 -5.5	-4.75 -4.75	—	-5.25 -5.25	Vdc
Input Bias Current (T _J = +25°C) (T _J = +125°C)	I _{IB}	—	—	6.0 5.5	—	—	6.0 5.5	mA
Input Bias Current Change -8.0 Vdc ≥ V _I ≥ -20 Vdc 1.0 mA ≤ I _O ≤ 40 mA	I _{IB}	—	—	1.5 0.2	—	—	1.5 0.1	mA
Output Noise Voltage (T _A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V _n	—	40	—	—	40	—	μV
Ripple Rejection (-8.0 > V _I > -18 Vdc, f = 120 Hz, T _J = 25°C)	RR	40	49	—	41	49	—	dB
Dropout Voltage I _O = 40 mA, T _J = +25°C	V _I - V _O	—	1.7	—	—	1.7	—	Vdc

MC79L12C, AC ELECTRICAL CHARACTERISTICS (V_I = -19 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	MC79L12C			MC79L12AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T _J = +25°C)	V _O	-11.1	-12	-12.9	-11.5	-12	-12.5	Vdc
Input Regulation (T _J = +25°C) -14.5 Vdc ≥ V _I ≥ -27 Vdc -16 Vdc ≥ V _I ≥ -27 Vdc	Reg _{line}	—	—	250 200	—	—	250 200	mV
Load Regulation T _J = +25°C, 1.0 mA ≤ I _O ≤ 100 mA 1.0 mA ≤ I _O ≤ 40 mA	Reg _{load}	—	—	100 50	—	—	100 50	mV
Output Voltage -14.5 Vdc ≥ V _I ≥ -27 Vdc, 1.0 mA ≤ I _O ≤ 40 mA V _I = -19 Vdc, 1.0 mA ≤ I _O ≤ 70 mA	V _O	-10.8 -10.8	—	-13.2 -13.2	-11.4 -11.4	—	-12.6 -12.6	Vdc
Input Bias Current (T _J = +25°C) (T _J = +125°C)	I _{IB}	—	—	6.5 6.0	—	—	6.5 6.0	mA
Input Bias Current Change -16 Vdc ≥ V _I ≥ -27 Vdc 1.0 mA ≤ I _O ≤ 40 mA	I _{IB}	—	—	1.5 0.2	—	—	1.5 0.1	mA
Output Noise Voltage (T _A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V _n	—	80	—	—	80	—	μV
Ripple Rejection (-15 ≤ V _I ≤ -25 Vdc, f = 120 Hz, T _J = +25°C)	RR	36	42	—	37	42	—	dB
Dropout Voltage I _O = 40 mA, T _J = +25°C	V _I - V _O	—	1.7	—	—	1.7	—	Vdc

MC79L00,A Series

MC79L15C, AC ELECTRICAL CHARACTERISTICS ($V_I = -23 \text{ V}$, $I_O = 40 \text{ mA}$, $C_I = 0.33 \mu\text{F}$, $C_O = 0.1 \mu\text{F}$,
 $0^\circ\text{C} < T_J < +125^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	MC79L15C			MC79L15AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	-13.8	-15	-16.2	-14.4	-15	-15.6	Vdc
Input Regulation ($T_J = +25^\circ\text{C}$) -17.5 Vdc $\geq V_I \geq -30 \text{ Vdc}$ -20 Vdc $\geq V_I \geq -30 \text{ Vdc}$	Regline	—	—	300 250	—	—	300 250	mV
Load Regulation $T_J = +25^\circ\text{C}$, $1.0 \text{ mA} \leq I_O \leq 100 \text{ mA}$ $1.0 \text{ mA} \leq I_O \leq 40 \text{ mA}$	Regload	—	—	150 75	—	—	150 75	mV
Output Voltage -17.5 Vdc $\geq V_I \geq -30 \text{ Vdc}$, $1.0 \text{ mA} \leq I_O \leq 40 \text{ mA}$ $V_I = -23 \text{ Vdc}$, $1.0 \text{ mA} \leq I_O \leq 70 \text{ mA}$	V_O	-13.5 -13.5	—	-16.5 -16.5	-14.25 -14.25	—	-15.75 -15.75	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$) ($T_J = +125^\circ\text{C}$)	I_{IB}	— —	— —	6.5 6.0	— —	— —	6.5 6.0	mA
Input Bias Current Change -20 Vdc $\geq V_I \geq -30 \text{ Vdc}$ $1.0 \text{ mA} \leq I_O \leq 40 \text{ mA}$	ΔI_{IB}	— —	— —	1.5 0.2	— —	— —	1.5 0.1	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10 \text{ Hz} \leq f \leq 100 \text{ kHz}$)	V_n	—	90	—	—	90	—	μV
Ripple Rejection (-18.5 $\leq V_I \leq -28.5 \text{ Vdc}$, $f = 120 \text{ Hz}$)	RR	33	39	—	34	39	—	dB
Dropout Voltage $I_O = 40 \text{ mA}$, $T_J = +25^\circ\text{C}$	$ V_I - V_O $	—	1.7	—	—	1.7	—	Vdc

MC79L18C, AC ELECTRICAL CHARACTERISTICS ($V_I = -27 \text{ V}$, $I_O = 40 \text{ mA}$, $C_I = 0.33 \mu\text{F}$, $C_O = 0.1 \mu\text{F}$,
 $0^\circ\text{C} < T_J < +125^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	MC79L18C			MC79L18AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	-16.6	-18	-19.4	-17.3	-18	-18.7	Vdc
Input Regulation ($T_J = +25^\circ\text{C}$) -20.7 Vdc $\geq V_I \geq -33 \text{ Vdc}$ -21.4 Vdc $\geq V_I \geq -33 \text{ Vdc}$ -22 Vdc $\geq V_I \geq -33 \text{ Vdc}$ -21 Vdc $\geq V_I \geq -33 \text{ Vdc}$	Regline	— — — —	— — — —	— 325 275 —	— — — —	— — — —	325 — — 275	mV
Load Regulation $T_J = +25^\circ\text{C}$, $1.0 \text{ mA} \leq I_O \leq 100 \text{ mA}$ $1.0 \text{ mA} \leq I_O \leq 40 \text{ mA}$	Regload	— —	— —	170 85	— —	— —	170 85	mV
Output Voltage -20.7 Vdc $\geq V_I \geq -33 \text{ Vdc}$, $1.0 \text{ mA} \leq I_O \leq 40 \text{ mA}$ -21.4 Vdc $\geq V_I \geq -33 \text{ Vdc}$, $1.0 \text{ mA} \leq I_O \leq 40 \text{ mA}$ $V_I = -27 \text{ Vdc}$, $1.0 \text{ mA} \leq I_O \leq 70 \text{ mA}$	V_O	— -16.2 -16.2	— — —	— -19.8 -19.8	-17.1 — -17.1	— — —	-18.9 — -18.9	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$) ($T_J = +125^\circ\text{C}$)	I_{IB}	— —	— —	6.5 6.0	— —	— —	6.5 6.0	mA
Input Bias Current Change -21 Vdc $\geq V_I \geq -33 \text{ Vdc}$ -27 Vdc $\geq V_I \geq -33 \text{ Vdc}$ $1.0 \text{ mA} \leq I_O \leq 40 \text{ mA}$	ΔI_{IB}	— — —	— — —	— 1.5 0.2	— — —	— — —	1.5 — 0.1	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10 \text{ Hz} \leq f \leq 100 \text{ kHz}$)	V_n	—	150	—	—	150	—	μV
Ripple Rejection (-23 $\leq V_I \leq -33 \text{ Vdc}$, $f = 120 \text{ Hz}$, $T_J = +25^\circ\text{C}$)	RR	32	46	—	33	48	—	dB
Dropout Voltage $I_O = 40 \text{ mA}$, $T_J = +25^\circ\text{C}$	$ V_I - V_O $	—	1.7	—	—	1.7	—	Vdc

MC79L00,A Series

MC79L24C, AC ELECTRICAL CHARACTERISTICS ($V_I = -33\text{ V}$, $I_O = 40\text{ mA}$, $C_I = 0.33\text{ }\mu\text{F}$, $C_O = 0.1\text{ }\mu\text{F}$,
 $0^\circ\text{C} < T_J < +125^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	MC79L24C			MC79L24AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	-22.1	-24	-25.9	-23	-24	-25	Vdc
Input Regulation ($T_J = +25^\circ\text{C}$)	Reg_{line}							mV
-27 Vdc $\geq V_I \geq -38\text{ V}$		—	—	—	—	—	350	
-27.5 Vdc $\geq V_I \geq -38\text{ Vdc}$		—	—	350	—	—	—	
-28 Vdc $\geq V_I \geq -38\text{ Vdc}$		—	—	300	—	—	300	
Load Regulation $T_J = +25^\circ\text{C}$, $1.0\text{ mA} \leq I_O \leq 100\text{ mA}$ $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$	Reg_{load}	—	—	200	—	—	200	mV
		—	—	100	—	—	100	
Output Voltage -27 Vdc $\geq V_I \geq -38\text{ V}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$ -28 Vdc $\geq V_I \geq -38\text{ Vdc}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$ $V_I = -33\text{ Vdc}$, $1.0\text{ mA} \leq I_O \leq 70\text{ mA}$	V_O	—	—	—	-22.8	—	-25.2	Vdc
		-21.4	—	-26.4	—	—	—	
		-21.4	—	-26.4	-22.8	—	-25.2	
Input Bias Current ($T_J = +25^\circ\text{C}$) ($T_J = +125^\circ\text{C}$)	I_{IB}	—	—	6.5	—	—	6.5	mA
		—	—	6.0	—	—	6.0	
Input Bias Current Change -28 Vdc $\geq V_I \geq -38\text{ Vdc}$ $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$	ΔI_{IB}	—	—	1.5	—	—	1.5	mA
		—	—	0.2	—	—	0.1	
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$)	V_n	—	200	—	—	200	—	μV
Ripple Rejection ($-29 \leq V_I \leq -35\text{ Vdc}$, $f = 120\text{ Hz}$, $T_J = 25^\circ\text{C}$)	RR	30	43	—	31	47	—	dB
Dropout Voltage $I_O = 40\text{ mA}$, $T_J = +25^\circ\text{C}$	$ V_I - V_O $	—	1.7	—	—	1.7	—	Vdc

APPLICATIONS INFORMATION

Design Considerations

The MC79L00 Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance

is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A $0.33\text{ }\mu\text{F}$ or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulator's input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.

FIGURE 1 — POSITIVE AND NEGATIVE REGULATOR

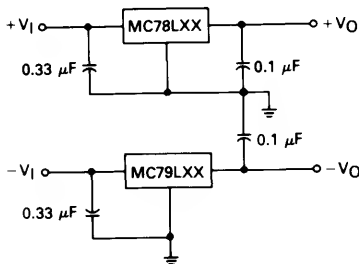
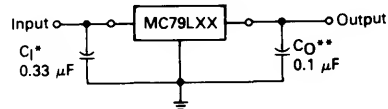


FIGURE 2 — STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

* = C_I is required if regulator is located an appreciable distance from power supply filter.

** = C_O improves stability and transient response.

MC79L00,A Series

TYPICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 3 — DROPOUT CHARACTERISTICS

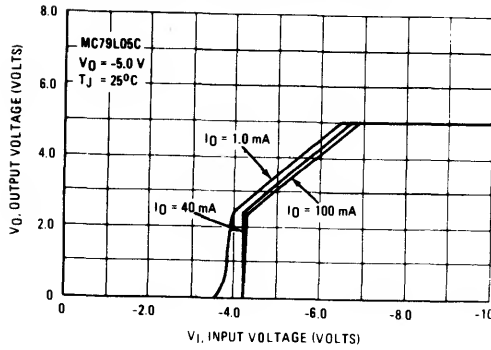


FIGURE 4 — DROPOUT VOLTAGE versus JUNCTION TEMPERATURE

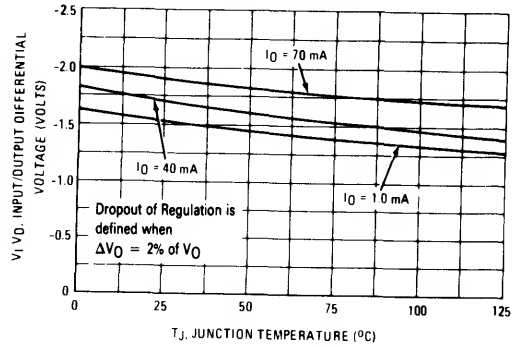


FIGURE 5 — INPUT BIAS CURRENT versus AMBIENT TEMPERATURE

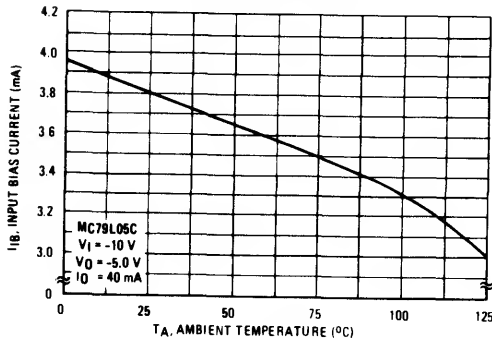


FIGURE 6 — INPUT BIAS CURRENT versus INPUT VOLTAGE

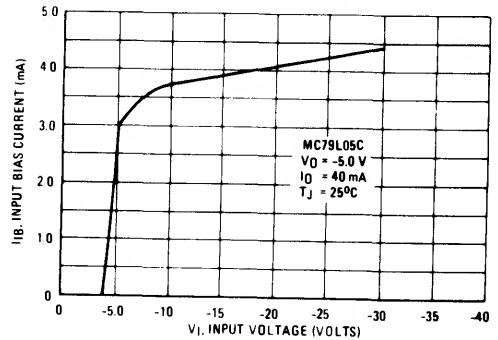


FIGURE 7 — MAXIMUM AVERAGE POWER DISSIPATION versus AMBIENT TEMPERATURE — TO-92 Type Package

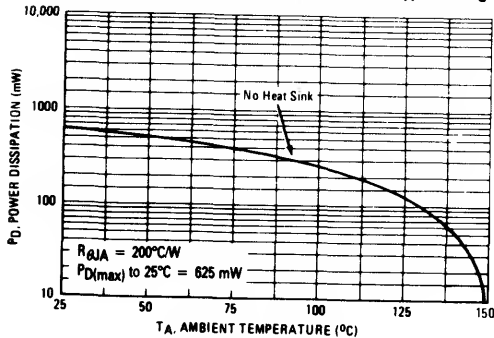
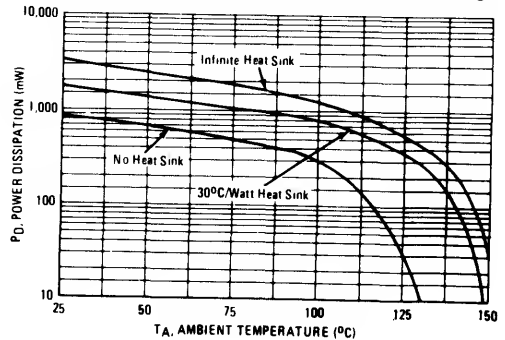


FIGURE 8 — MAXIMUM AVERAGE POWER DISSIPATION versus AMBIENT TEMPERATURE — TO-39 Type Package



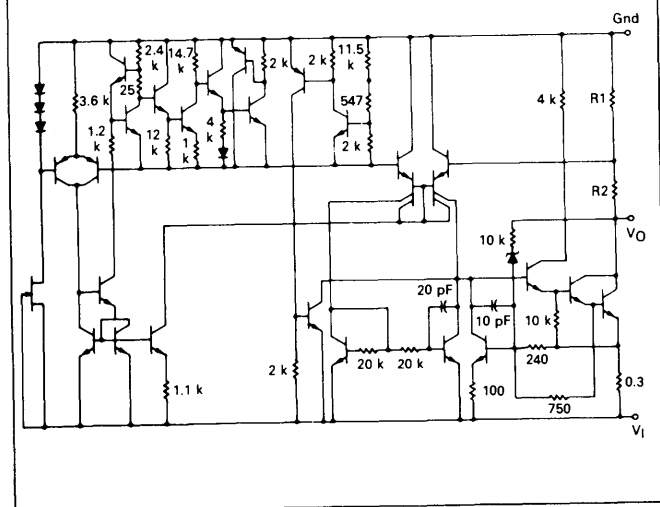
**THREE-TERMINAL
NEGATIVE VOLTAGE REGULATORS**

The MC79M00 Series of fixed output negative voltage regulators are intended as complements to the popular MC78M00 Series devices.

Available in fixed output voltage options of -5.0, -12 and -15 volts, these regulators employ current limiting, thermal shut-down, and safe-area compensation — making them remarkably rugged under most operating conditions. With adequate heat-sinking they can deliver output currents in excess of 0.5 ampere.

- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation

EQUIVALENT SCHEMATIC DIAGRAM



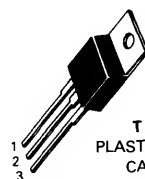
ORDERING INFORMATION

ORDERING INFORMATION			
Device	Output Voltage	Tested Operating Junction Temp. Range	Package
MC79M05CDT, CDT-1	- 5.0 Volts	0°C to +125°C	DPAK
MC79M05CT			Plastic Power
MC79M12CDT, CDT-1	- 12 Volts		DPAK
MC79M12CT			Plastic Power
MC79M15CDT, CDT-1	- 15 Volts		DPAK
MC79M15CT			Plastic Power

**MC79M00
Series**

**THREE-TERMINAL
NEGATIVE FIXED
VOLTAGE REGULATORS**

**SILICON MONOLITHIC
INTEGRATED CIRCUITS**



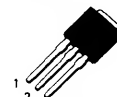
T SUFFIX
PLASTIC PACKAGE
CASE 221A

- PIN 1. GROUND
2. INPUT
3. OUTPUT

(Heatsink surface connected to Pin 2)

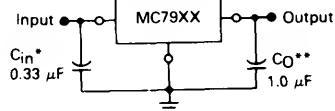


DT SUFFIX
PLASTIC PACKAGE
CASE 369A
(DPAK)



DT-1 SUFFIX
PLASTIC PACKAGE
CASE 369
(DPAK)

STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 1.1 V more negative even during the high point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_0 improves stability and transient response.

MC79M00 Series

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage	V _I	-35	Vdc
Power Dissipation Plastic Package, T-Suffix T _A = +25°C Derate above T _A = +25°C T _C = +25°C Derate above T _C = +95°C	P _D 1/R _{θJA} P _D 1/R _{θJC}	Internally Limited 14.2 Internally Limited 200	Watts mW/°C Watts mW/°C
Storage Junction Temperature Range	T _{stg}	-65 to +150	°C
Junction Temperature Range	T _J	0 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	R _{θJA}	65	°C/W
Thermal Resistance, Junction to Case	R _{θJC}	5.0	°C/W

MC79M05C ELECTRICAL CHARACTERISTICS (V_I = -10 V, I_O = 350 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T _J = +25°C)	V _O	-4.8	-5.0	-5.2	Vdc
Line Regulation (T _J = +25°C) (Note 1) -7.0 Vdc ≥ V _I ≥ -25 Vdc -8.0 Vdc ≥ V _I ≥ -18 Vdc	Reg _{line}	—	7.0 2.0	50 30	mV
Load Regulation (T _J = +25°C) (Note 1) 5.0 mA ≤ I _O ≤ 500 mA	Reg _{load}	—	30	100	mV
Output Voltage -7.0 Vdc ≥ V _I ≥ -25 Vdc, 5.0 mA ≤ I _O ≤ 350 mA	V _O	-4.75	—	-5.25	Vdc
Input Bias Current (T _J = +25°C)	I _{IB}	—	4.3	8.0	mA
Input Bias Current Change -8.0 Vdc ≥ V _I ≥ -25 Vdc, I _O = 350 mA 5.0 mA ≤ I _O ≤ 350 mA, V _I = -10 V	ΔI _{IB}	—	—	0.4 0.4	mA
Output Noise Voltage (T _A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V _n	—	40	—	μV
Ripple Rejection (f = 120 Hz)	RR	54	66	—	dB
Dropout Voltage I _O = 500 mA, T _J = +25°C	V _I -V _O	—	1.1	—	Vdc
Average Temperature Coefficient of Output Voltage I _O = 5.0 mA, 0°C ≤ T _J ≤ +125°C	ΔV _O /ΔT	—	0.2	—	mV/°C

Note:

1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC79M00 Series

3

MC79M12C ELECTRICAL CHARACTERISTICS ($V_I = -19\text{ V}$, $I_O = 350\text{ mA}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	-11.5	-12	-12.5	Vdc
Line Regulation ($T_J = +25^\circ\text{C}$) (Note 1) -14.5 Vdc $\geq V_I \geq -30\text{ Vdc}$ -15 Vdc $\geq V_I \geq -25\text{ Vdc}$	Reg _{line}	—	5.0 3.0	80 50	mV mV
Load Regulation ($T_J = +25^\circ\text{C}$) (Note 1) 5.0 mA $\leq I_O \leq 500\text{ mA}$	Reg _{load}	—	30	240	mV
Output Voltage -14.5 Vdc $\geq V_I \geq -30\text{ Vdc}$, 5.0 mA $\leq I_O \leq 350\text{ mA}$	V_O	-11.4	—	-12.6	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$)	I_{IB}	—	4.4	8.0	mA
Input Bias Current Change -14.5 Vdc $\geq V_I \geq -30\text{ Vdc}$, $I_O = 350\text{ mA}$ 5.0 mA $\leq I_O \leq 350\text{ mA}$, $V_I = -19\text{ V}$	ΔI_{IB}	—	—	0.4 0.4	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$)	V_n	—	75	—	μV
Ripple Rejection ($f = 120\text{ Hz}$)	RR	54	60	—	dB
Dropout Voltage $I_O = 500\text{ mA}$, $T_J = +25^\circ\text{C}$	$V_I - V_O$	—	1.1	—	Vdc
Average Temperature Coefficient of Output Voltage $I_O = 5.0\text{ mA}$, $0^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$	$\Delta V_O / \Delta T$	—	-0.8	—	mV/ $^\circ\text{C}$

MC79M15C ELECTRICAL CHARACTERISTICS ($V_I = -23\text{ V}$, $I_O = 350\text{ mA}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	-14.4	-15	-15.6	Vdc
Line Regulation ($T_J = +25^\circ\text{C}$) (Note 1) -17.5 Vdc $\geq V_I \geq -30\text{ Vdc}$ -18 Vdc $\geq V_I \geq -28\text{ Vdc}$	Reg _{line}	—	5.0 3.0	80 50	mV mV
Load Regulation ($T_J = +25^\circ\text{C}$) (Note 1) 5.0 mA $\leq I_O \leq 500\text{ mA}$	Reg _{load}	—	30	240	mV
Output Voltage -17.5 Vdc $\geq V_I \geq -30\text{ Vdc}$, 5.0 mA $\leq I_O \leq 350\text{ mA}$	V_O	-14.25	—	-15.75	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$)	I_{IB}	—	4.4	8.0	mA
Input Bias Current Change -17.5 Vdc $\geq V_I \geq -30\text{ Vdc}$, $I_O = 350\text{ mA}$ 5.0 mA $\leq I_O \leq 350\text{ mA}$, $V_I = -23\text{ V}$	ΔI_{IB}	—	—	0.4 0.4	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$)	V_n	—	90	—	μV
Ripple Rejection ($f = 120\text{ Hz}$)	RR	54	60	—	dB
Dropout Voltage $I_O = 500\text{ mA}$, $T_J = +25^\circ\text{C}$	$V_I - V_O$	—	1.1	—	Vdc
Average Temperature Coefficient of Output Voltage $I_O = 5.0\text{ mA}$, $0^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$	$\Delta V_O / \Delta T$	—	-1.0	—	mV/ $^\circ\text{C}$

Note:

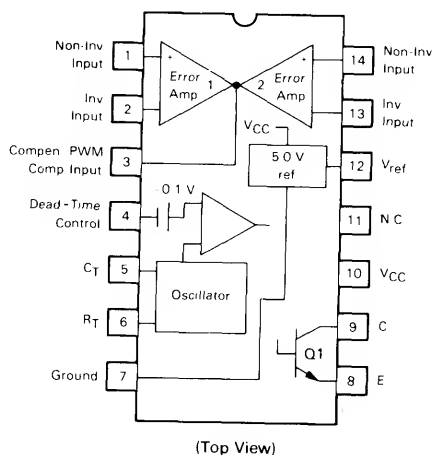
1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

**SWITCHMODE PULSE WIDTH MODULATION
CONTROL CIRCUITS**

The MC35060 and MC34060 are low cost fixed frequency, pulse width modulation control circuits designed primarily for single ended SWITCHMODE power supply control. These devices feature:

- Complete Pulse Width Modulation Control Circuitry
- On-Chip Oscillator With Master or Slave Operation
- On-Chip Error Amplifiers
- On-Chip 5.0 Volt Reference
- Adjustable Dead Time Control
- Uncommitted Output Transistor for 200 mA Source or Sink

PIN CONNECTIONS



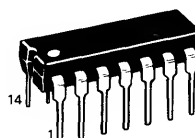
The MC34060 is specified over the commercial operating range of 0°C to +70°C. The MC35060 is specified over the full military range of -55 to +125°C.

SWITCHMODE is a trademark of Motorola Inc

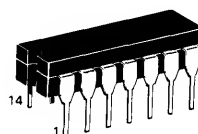
MC34060
MC35060

**SWITCHMODE
PULSE WIDTH MODULATION
CONTROL CIRCUITS**

**SILICON MONOLITHIC
INTEGRATED CIRCUITS**



P SUFFIX
PLASTIC PACKAGE
CASE 646



L SUFFIX
CERAMIC PACKAGE
CASE 632

ORDERING INFORMATION

Device	Temperature Range	Package
MC35060L	-55 to +125°C	Ceramic DIP
MC34060P	0 to +70°C	Plastic DIP
MC34060L	0 to +70°C	Ceramic DIP

MC34060, MC35060

FIGURE 1 — BLOCK DIAGRAM

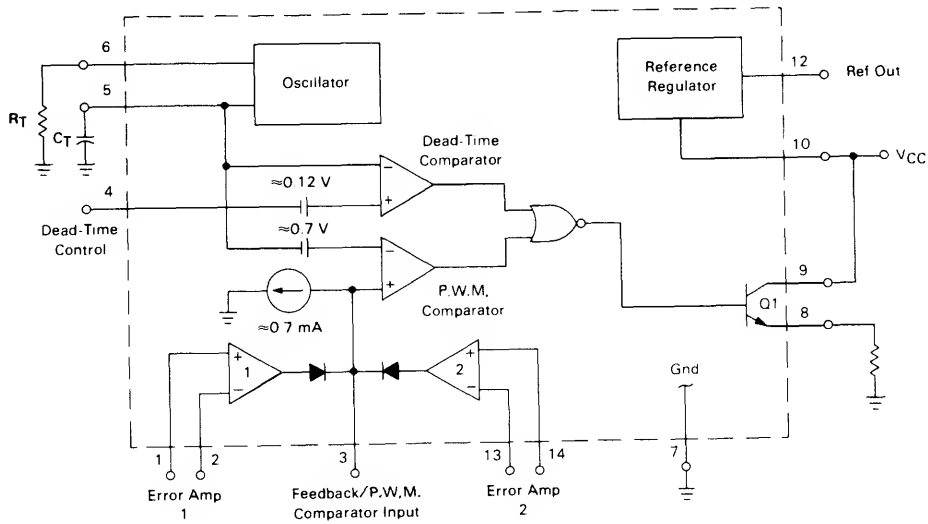
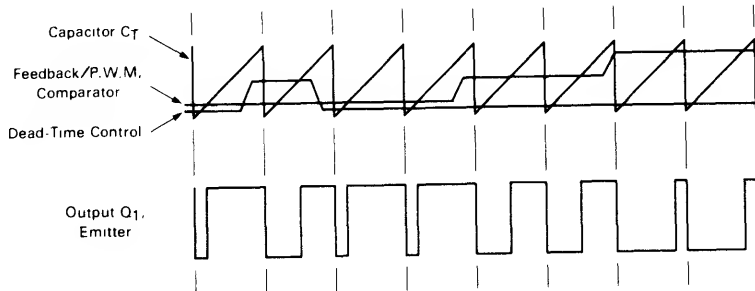


FIGURE 2 — TIMING DIAGRAM



Description

The MC35060/34060 is a fixed-frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply. (See Figure 1.) An internal-linear sawtooth oscillator is frequency-programmable by two external components, R_T and C_T . The approximate oscillator frequency is determined by:

$$f_{osc} \cong \frac{1.1}{R_T \bullet C_T}$$

For more information refer to Figure 3.

Output pulse width modulation is accomplished by comparison of the positive sawtooth waveform across capacitor C_T to either of two control signals. The output is enabled only during that portion of time when the sawtooth voltage is greater than the control signals. Therefore, an increase in control signal amplitude causes a corresponding linear decrease of output pulse width. (Refer to the timing diagram shown in Figure 2.)

The control signals are external inputs that can be fed into the dead-time control, the error amplifier inputs, or the feed-back input. The dead-time control comparator has an effective 120 mV input offset which limits the minimum output dead time to approximately the first 4% of the sawtooth-cycle time. This would result in a maximum duty cycle of 96%. Additional dead time may be imposed on the output by setting the dead time-control input to a fixed voltage, ranging between 0 to 3.3 V.

The pulse width modulator comparator provides a means for the error amplifiers to adjust the output pulse width from the maximum percent on-time, established by the dead time control input, down to zero, as the voltage at the feedback pin varies from 0.5 to 3.5 V. Both

error amplifiers have a common-mode input range from -0.3 V to $(V_{CC} - 2\text{ V})$, and may be used to sense power supply output voltage and current. The error-amplifier outputs are active high and are ORed together at the non-inverting input of the pulse-width modulator comparator. With this configuration, the amplifier that demands minimum output on time, dominates control of the loop.

The MC35060/34060 has an internal 5.0 V reference capable of sourcing up to 10 mA of load currents for external bias circuits. The reference has an internal accuracy of $\pm 5\%$ with a typical thermal drift of less than 50 mV over an operating temperature range of 0 to $+70^\circ\text{C}$.

MAXIMUM RATINGS (Full operating ambient temperature range applies unless otherwise noted)

Rating	Symbol	MC35060	MC34060	Unit
Power Supply Voltage	V_{CC}	42	42	V
Collector Output Voltage	V_C	42	42	V
Collector Output Current	I_C	250	250	mA
Amplifier Input Voltage	V_{in}	$V_{CC} + 0.3$	$V_{CC} + 0.3$	V
Power Dissipation @ $T_A \leq 45^\circ\text{C}$	P_D	1000	1000	mW
Operating Junction Temperature Plastic Package Ceramic Package	T_J	— 150	125 150	$^\circ\text{C}$
Operating Ambient Temperature Range	T_A	-55 to 125	0 to 70	$^\circ\text{C}$
Storage Temperature Range Plastic Package Ceramic Package	T_{stg}	— -65 to 150	-55 to 125 -65 to 150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	L Suffix Ceramic Package	P Suffix Plastic Package	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	100	80	$^\circ\text{C}/\text{W}$
Power Derating Factor	$1/R_{\theta JA}$	10	12.5	$\text{mW}/^\circ\text{C}$
Derating Ambient Temperature	T_A	50	45	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS

Condition	Symbol	MC35060/MC34060			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	7.0	15	40	V
Collector Output Voltage	V_C	—	30	40	V
Collector Output Current	I_C	—	—	200	mA
Amplifier Input Voltage	V_{in}	-0.3	—	$V_{CC} - 2$	V
Current Into Feedback Terminal	I_{fb}	—	—	0.3	mA
Reference Output Current	I_{ref}	—	—	10	mA
Timing Resistor	R_T	1.8	47	500	k Ω
Timing Capacitor	C_T	0.00047	0.001	10	μF
Oscillator Frequency	f_{osc}	1.0	25	200	kHz

MC34060, MC35060

ELECTRICAL CHARACTERISTICS $V_{CC} = 15\text{ V}$, $C_T = 0.01\text{ }\mu\text{F}$, $R_T = 12\text{ k}\Omega$ unless otherwise noted. For typical values $T_A = 25^\circ\text{C}$, for min/max values T_A is the operating ambient temperature range that applies unless otherwise noted.

Characteristic	Symbol	MC35060			MC34060			Unit
		Min	Typ	Max	Min	Typ	Max	

REFERENCE SECTION

Reference Voltage ($I_O = 1.0\text{ mA}$)	V_{ref}	4.75	5.0	5.25	4.75	5.0	5.25	V
Input Regulation ($V_{CC} = 7.0\text{ V to }40\text{ V}$)	Reg_{line}	—	2.0	25	—	2.0	25	mV
Output Regulation ($I_O = 1.0\text{ mA to }10\text{ mA}$)	Reg_{load}	—	3.0	15	—	3.0	15	mV
Short-Circuit Output Current ($V_{ref} = 0\text{ V}$)	I_{SC}	15	35	75	15	35	75	mA

OUTPUT SECTION

Collector Off-State Current ($V_{CC} = 40\text{ V}$, $V_{CE} = 40\text{ V}$)	$I_{C(off)}$	—	2.0	100	—	2.0	100	μA
Emitter Off-State Current ($V_{CC} = 40\text{ V}$, $V_C = 40\text{ V}$, $V_E = 0\text{ V}$)	$I_{E(off)}$	—	—	-150	—	—	-100	μA
Collector-Emitter Saturation Voltage Common-Emitter ($V_E = 0\text{ V}$, $I_C = 200\text{ mA}$)	$V_{sat(C)}$	—	1.1	1.5	—	1.1	1.3	V
Emitter-Follower ($V_C = 15\text{ V}$, $I_E = -200\text{ mA}$)	$V_{sat(E)}$	—	1.5	2.5	—	1.5	2.5	V
Output Voltage Rise Time ($T_A = 25^\circ\text{C}$) Common-Emitter (See Figure 12)	t_r	—	100	200	—	100	200	ns
Emitter-Follower (See Figure 13)		—	100	200	—	100	200	ns
Output Voltage Fall Time ($T_A = 25^\circ\text{C}$) Common-Emitter (See Figure 12)	t_f	—	25	100	—	25	100	ns
Emitter-Follower (See Figure 13)		—	40	100	—	40	100	ns

Characteristic	Symbol	MC35060 / MC34060			Unit
		Min	Typ	Max	

ERROR AMPLIFIER SECTIONS

Input Offset Voltage ($V_{O(Pin\ 3)} = 2.5\text{ V}$)	V_{IO}	—	2.0	10	mV
Input Offset Current ($V_{C(Pin\ 3)} = 2.5\text{ V}$)	I_{IO}	—	5.0	250	nA
Input Bias Current ($V_{O(Pin\ 3)} = 2.5\text{ V}$)	I_{IB}	—	-0.1	-1.0	μA
Input Common-Mode Voltage Range ($V_{CC} = 40\text{ V}$, $T_A = 25^\circ\text{C}$)	V_{ICR}	-0.3 to $V_{CC} - 2.0$	—	—	V
Open Loop Voltage Gain ($\Delta V_O = 3.0\text{ V}$, $V_O = 0.5\text{ to }3.5\text{ V}$, $R_L = 2.0\text{ k}\Omega$)	A_{VOL}	70	95	—	dB

3

MC34060, MC35060

ELECTRICAL CHARACTERISTICS $V_{CC} = 15\text{ V}$, $C_T = 0.01\text{ }\mu\text{F}$, $R_T = 12\text{ k}\Omega$ unless otherwise noted. For typical values $T_A = 25^\circ\text{C}$, for min/max values T_A is the operating ambient temperature range that applies unless otherwise noted.

Characteristic	Symbol	MC35060/MC34060			Unit
		Min.	Typ.	Max.	
ERROR AMPLIFIER SECTIONS (Continued)					
Unity-Gain Crossover Frequency ($V_O = 0.5$, to 3.5 V , $R_L = 2.0\text{ k}\Omega$)	f_c	—	350	—	kHz
Phase Margin at Unity-Gain ($V_O = 0.5$ to 3.5 V , $R_L = 2.0\text{ k}\Omega$)	ϕ_m	—	65	—	deg.
Common-Mode Rejection Ratio ($V_{CC} = 40\text{ V}$)	CMRR	65	90	—	dB
Power Supply Rejection Ratio ($\Delta V_{CC} = 33\text{ V}$, $V_O = 2.5\text{ V}$, $R_L = 2.0\text{ k}\Omega$)	PSRR	—	100	—	dB
Output Sink Current ($V_O[\text{Pin } 3] = 0.7\text{ V}$)	I_{O-}	0.3	0.7	—	mA
Output Source Current ($V_O[\text{Pin } 3] = 3.5\text{ V}$)	I_{O+}	-2.0	-4.0	—	mA

PWM COMPARATOR SECTION (Test circuit Figure 11)

Input Threshold Voltage (Zero Duty Cycle)	V_{TH}	—	3.5	4.5	V
Input Sink Current ($V[\text{Pin } 3] = 0.7\text{ V}$)	I_{I-}	0.3	0.7	—	mA

DEAD-TIME CONTROL SECTION (Test Circuit Figure 11)

Input Bias Current (Pin 4) ($V_{in} = 0$ to 5.25 V)	$I_{IB(DT)}$	—	-2.0	-10	μA
Maximum Output Duty Cycle ($V_{in} = 0\text{ V}$, $C_T = 0.01\text{ }\mu\text{F}$, $R_T = 12\text{ k}\Omega$) ($V_{in} = 0\text{ V}$, $C_T = 0.001\text{ }\mu\text{F}$, $R_T = 47\text{ k}\Omega$)	DC_{max}	90 —	96 92	100 100	%
Input Threshold Voltage (Pin 4) (Zero Duty Cycle) (Maximum Duty Cycle)	V_{TH}	— 0	2.8 —	3.3 —	V

OSCILLATOR SECTION

Frequency ($C_T = 0.001\text{ }\mu\text{F}$, $R_T = 47\text{ k}\Omega$)	f_{osc}	—	25	—	kHz
Standard Deviation of Frequency* ($C_T = 0.001\text{ }\mu\text{F}$, $R_T = 47\text{ k}\Omega$)	σf_{osc}	—	3.0	—	%
Frequency Change with Voltage ($V_{CC} = 7.0\text{ V}$ to 40 V , $T_A = 25^\circ\text{C}$)	$\Delta f_{osc}(\Delta V)$	—	0.1	—	%
Frequency Change with Temperature ($\Delta T_A = T_{low}$ to T_{high}) ($C_T = 0.01\text{ }\mu\text{F}$, $R_T = 12\text{ k}\Omega$)	$\Delta f_{osc}(\Delta T)$	— —	— —	12	%

TOTAL DEVICE

Standby Supply Current (Pin 6 at V_{ref} , all other inputs and outputs open) ($V_{CC} = 15\text{ V}$) ($V_{CC} = 40\text{ V}$)	I_{CC}	— —	5.5 7.0	10 15	mA
Average Supply Current ($V[\text{Pin } 4] = 2.0\text{ V}$, $C_T = 0.001$, $R_T = 47\text{ k}\Omega$). See Figure 11.	I_S	—	7.0	—	mA

*Standard deviation is a measure of the statistical distribution about the mean as derived from the formula, $\sigma = \sqrt{\frac{\sum_{n=1}^N (X_n - \bar{x})^2}{N - 1}}$

$$\sigma = \sqrt{\frac{\sum_{n=1}^N (X_n - \bar{x})^2}{N - 1}}$$

FIGURE 3 — OSCILLATOR FREQUENCY
versus TIMING RESISTANCE

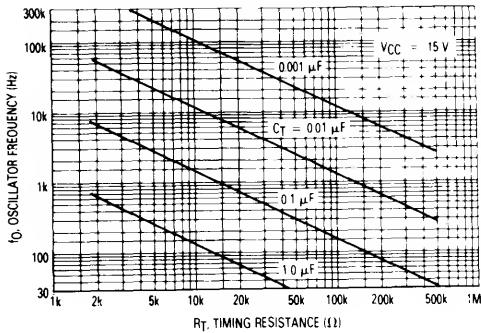


FIGURE 4 — OPEN LOOP VOLTAGE GAIN AND PHASE
versus FREQUENCY

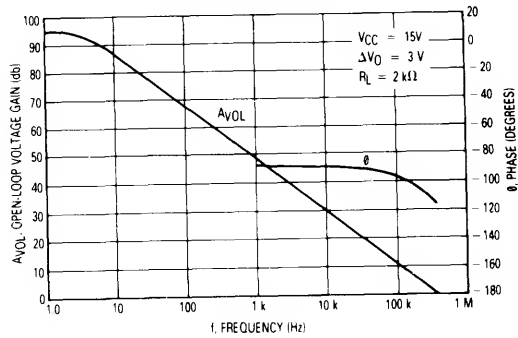


FIGURE 5 — PERCENT DEAD-TIME versus
OSCILLATOR FREQUENCY

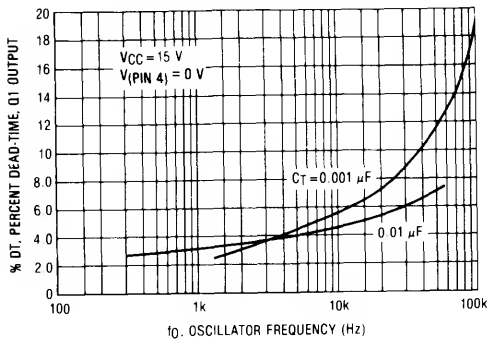


FIGURE 6 — PERCENT DUTY CYCLE versus
DEAD-TIME CONTROL VOLTAGE

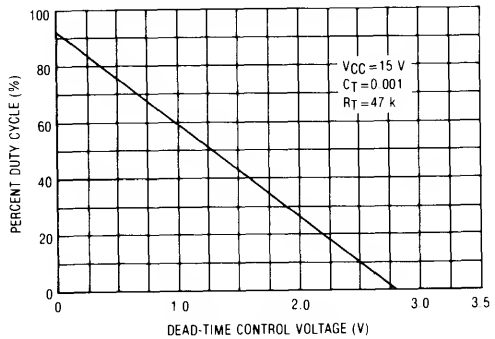


FIGURE 7 — EMITTER FOLLOWER CONFIGURATION
OUTPUT-SATURATION VOLTAGE versus
EMITTER CURRENT

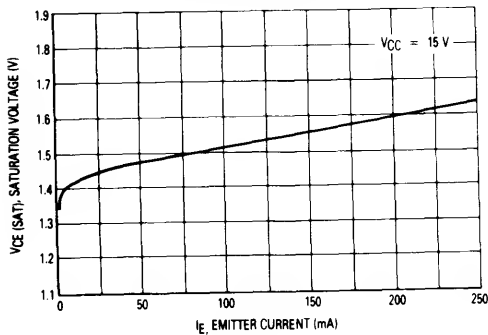


FIGURE 8 — COMMON EMITTER CONFIGURATION
OUTPUT-SATURATION VOLTAGE versus
COLLECTOR CURRENT

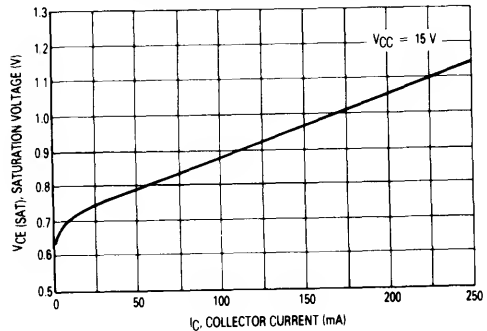


FIGURE 9 — STANDBY-SUPPLY CURRENT
versus SUPPLY VOLTAGE

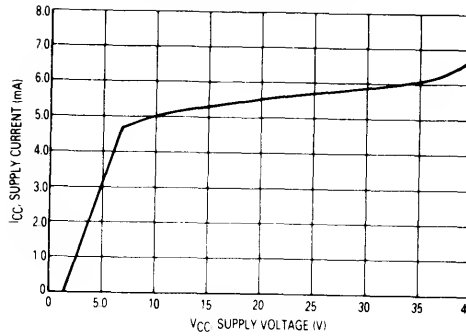


FIGURE 10 — ERROR AMPLIFIER CHARACTERISTICS

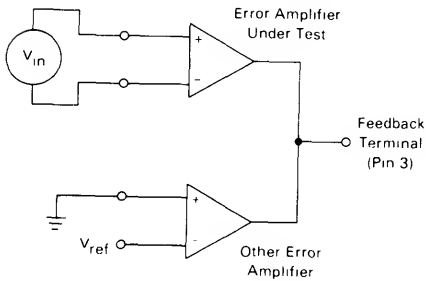


FIGURE 11 — DEAD-TIME AND FEEDBACK CONTROL
TEST CIRCUIT

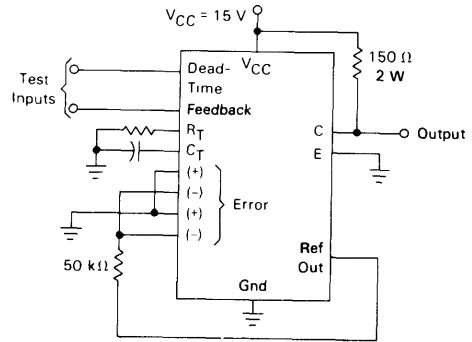


FIGURE 12 — COMMON-EMITTER CONFIGURATION
TEST CIRCUIT AND WAVEFORM

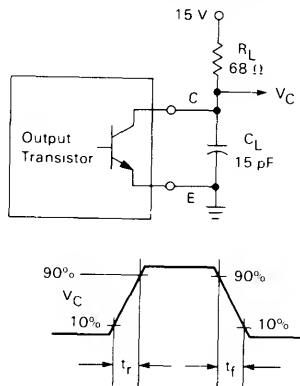


FIGURE 13 — EMITTER-FOLLOWER CONFIGURATION
TEST CIRCUIT AND WAVEFORM

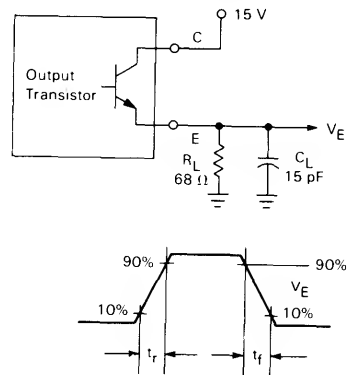


FIGURE 14 — ERROR AMPLIFIER SENSING TECHNIQUES

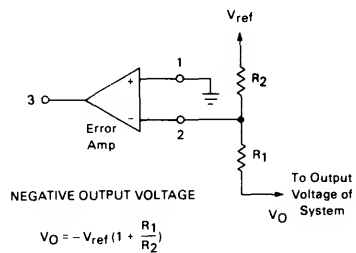
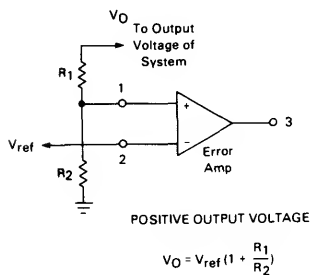


FIGURE 15 — DEAD-TIME CONTROL CIRCUIT

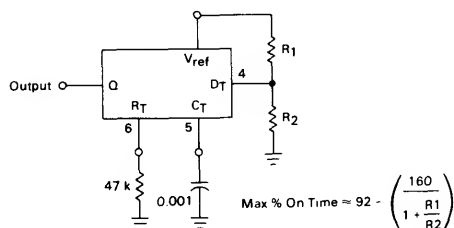


FIGURE 16 — SOFT-START CIRCUIT

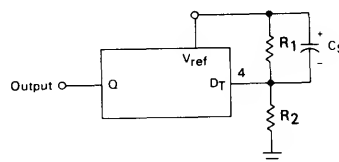
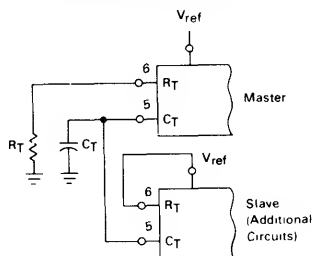
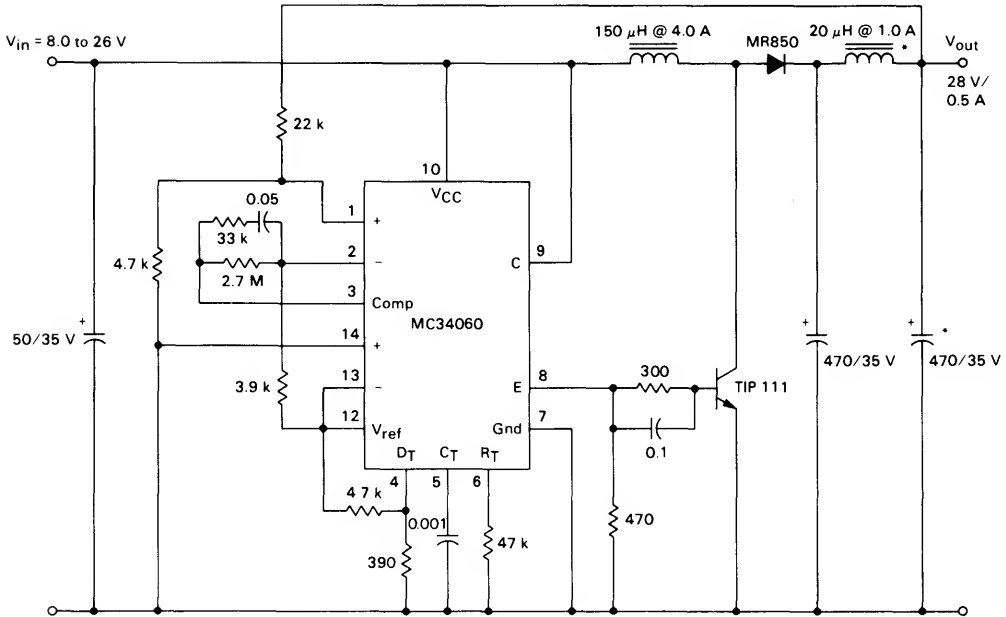


FIGURE 17 — SLAVING TWO OR MORE CONTROL CIRCUITS



MC34060, MC35060

FIGURE 19 — STEP-UP CONVERTER

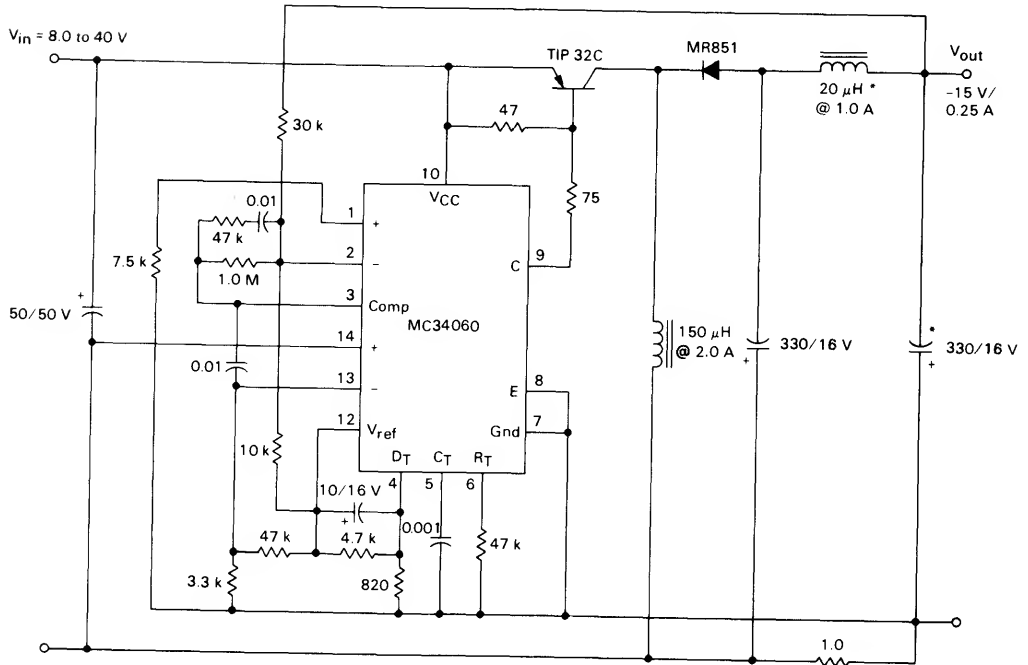


TEST	CONDITIONS	RESULTS
Line Regulation	$V_{in} = 8.0 \text{ V to } 26 \text{ V}$, $I_O = 0.5 \text{ A}$	40 mV 0.14%
Load Regulation	$V_{in} = 12 \text{ V}$, $I_O = 1.0 \text{ mA to } 0.5 \text{ A}$	5.0 mV 0.18%
Output Ripple	$V_{in} = 12 \text{ V}$, $I_O = 0.5 \text{ A}$	24 mV p-p P.A.R.D.
Efficiency	$V_{in} = 12 \text{ V}$, $I_O = 0.5 \text{ A}$	75%

* Optional circuit to minimize output ripple.

MC34060, MC35060

FIGURE 20 — STEP-UP/DOWN VOLTAGE INVERTING
CONVERTER WITH SOFT-START AND
CURRENT LIMITING



TEST	CONDITIONS	RESULTS
Line Regulation	$V_{in} = 8.0 \text{ V to } 40 \text{ V}$, $I_O = 250 \text{ mA}$	52 mV 0.35%
Load Regulation	$V_{in} = 12 \text{ V}$, $I_O = 1 \text{ mA to } 250 \text{ mA}$	47 mV 0.32%
Output Ripple	$V_{in} = 12 \text{ V}$, $I_O = 250 \text{ mA}$	10 mV p.p. P.A.R.D.
Short Circuit Current	$V_{in} = 12 \text{ V}$, $R_L = 0.1 \Omega$	330 mA
Efficiency	$V_{in} = 12 \text{ V}$, $I_O = 250 \text{ mA}$	86%

* Optional circuit to minimize output ripple

FIGURE 21 — 35 WATT FULL-POWER BIFILAR TRANSFORMER WITH SOFT-START AND PRIMARY POWER LIMITING

3 each
0.0047 UL CSA

115 Vac
20°

10 A

15 Ω Cold

3.200 Vac

1N4003

1N4001

1N4742

180 200 V

2.2 M

33 k

0.01

7.5 k

8.2 k

1.5 k

27 k

11 k

0.001

47 k

47 k

200

47

1.0

1N4148

MC34060

Comp

V_{CC}

9

10

1

2

3

14

13

12

DT

V_{ref}

4

5

6

7

8

CT

RT

Gnd

E

MPS A05

MJE 13005

10.25 V

MPS A55

1N4934

47/25 V

1N4934

2200 10 V

1N5824

L₁

5.0 V/3.0 A

12 0.75 A

Common

1000/25 V

10.35 V

1N4934

1000/25 V

10.35 V

L₂

10/35 V

10/35 V

L₃

-12/0.75 A

1N4937

T1 Colicraft W2961

T2 Core: Colicraft 11-464-16, 0.025" gap in each leg

Bobbin: Colicraft 37-573

Windings: 75 turns #26 Awg Bifilar wound

Primary, 2 each: 15 turns #26 Awg

Secondary, 5.0 V: 6 turns #22 Awg Bifilar wound

Secondary, 2 each: 14 turns #24 Awg Bifilar wound

Optional RFI Filter

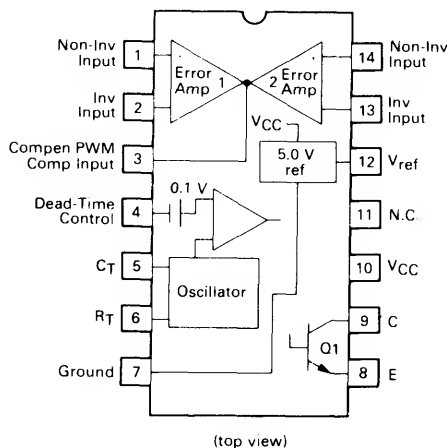
TEST	CONDITIONS	RESULTS
Line Regulation 5.0 V	$V_{in} = 95$ to 135 Vac, $I_O = 3.0$ A	20 mV 0.40%
Line Regulation ± 12 V	$V_{in} = 95$ to 135 Vac, $I_O = +0.75$ A	52 mV 0.26%
Load Regulation 5.0 V	$V_{in} = 115$ Vac, $I_O = 1.0$ to 4.0 A	476 mV 9.5%
Load Regulation ± 12 V	$V_{in} = 115$ Vac, $I_O = +0.4$ to ± 0.9 A	300 mV 2.5%
Output Ripple 5.0 V	$V_{in} = 115$ Vac, $I_O = 3.0$ A	45 mV p-p PARD
Output Ripple ± 12 V	$V_{in} = 115$ Vac, $I_O = +0.75$ A	75 mV p-p PARD
Efficiency	$V_{in} = 115$ Vac, $I_O 5.0$ V = 3.0 A $I_O \pm 12 = \pm 0.75$ A	74%

**PRECISION SWITCHMODE
PULSE WIDTH MODULATION
CONTROL CIRCUITS**

The MC35060A/MC34060A/MC33060A are low cost fixed frequency, pulse width modulation control circuits designed primarily for single ended SWITCHMODE power supply control. These devices feature:

- The MC34060A is specified over the commercial operating range of 0° to +70°C. The MC35060A is specified over the full military range of -55 to +125°C. The MC33060A is specified over the vehicular temperature range of -40° to +85°C.
- Complete Pulse Width Modulation Control Circuitry
- On-Chip Oscillator With Master or Slave Operation
- On-Chip Error Amplifiers
- On-Chip 5.0 Volt Reference, 1.5% Accuracy
- Adjustable Dead Time Control
- Uncommitted Output Transistor Rated to 500 mA Source or Sink
- Undervoltage Lockout
- Available in Surface Mount Package

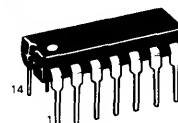
PIN CONNECTIONS



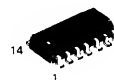
MC34060A
MC35060A
MC33060A

**PRECISION SWITCHMODE
PULSE WIDTH MODULATION
CONTROL CIRCUITS**

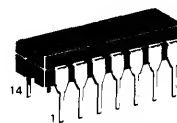
**SILICON MONOLITHIC
INTEGRATED CIRCUITS**



P SUFFIX
PLASTIC PACKAGE
CASE 646



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)



L SUFFIX
CERAMIC PACKAGE
CASE 632

ORDERING INFORMATION

Device	Temperature Range	Package
MC35060AL	-55° to +125°C	Ceramic DIP
MC34060AD	0° to +70°C	SO-14 Plastic DIP
MC34060AP		Plastic DIP
MC33060AD	-40° to +85°C	SO-14 Plastic DIP
MC33060AP		Plastic DIP

MC34060A, MC35060A, MC33060A

FIGURE 1 — BLOCK DIAGRAM

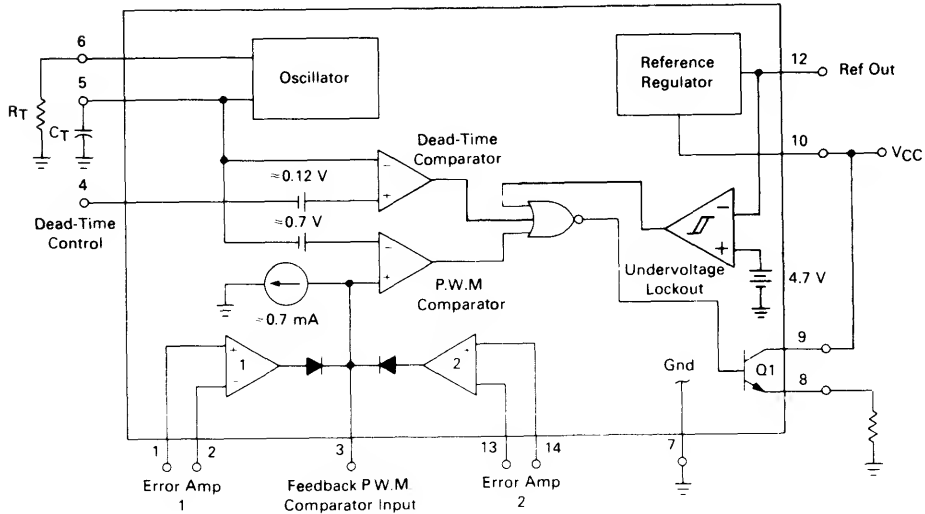
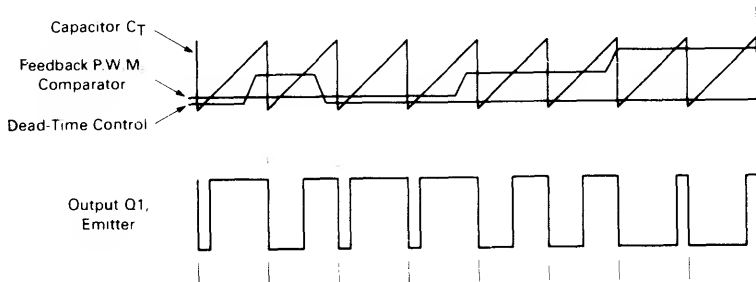


FIGURE 2 — TIMING DIAGRAM



Description

The MC35060A/34060A/33060A is a fixed-frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply. (See Figure 1.) An internal-linear sawtooth oscillator is frequency-programmable by two external components, R_T and C_T . The approximate oscillator frequency is determined by:

$$f_{osc} \approx \frac{1.2}{R_T \bullet C_T}$$

For more information refer to Figure 3.

Output pulse width modulation is accomplished by comparison of the positive sawtooth waveform across capacitor C_T to either of two control signals. The output is enabled only during that portion of time when the sawtooth voltage is greater than the control signals. Therefore, an increase in control-signal amplitude causes a corresponding linear decrease of output pulse width. (Refer to the timing diagram shown in Figure 2.)

MC34060A, MC35060A, MC33060A

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The control signals are external inputs that can be fed into the dead-time control, the error amplifier inputs, or the feedback input. The dead-time control comparator has an effective 120 mV input offset which limits the minimum output dead time to approximately the first 4% of the sawtooth-cycle time. This would result in a maximum duty cycle of 96%. Additional dead time may be imposed on the output by setting the dead time-control input to a fixed voltage, ranging between 0 to 3.3 V.

The pulse width modulator comparator provides a means for the error amplifiers to adjust the output pulse width from the maximum percent on-time, established by the dead time control input, down to zero, as the voltage at the feedback pin varies from 0.5 to 3.5 V. Both

error amplifiers have a common-mode input range from -0.3 V to $(V_{CC} - 2.0\text{ V})$, and may be used to sense power supply output voltage and current. The error-amplifier outputs are active high and are ORed together at the non-inverting input of the pulse-width modulator comparator. With this configuration, the amplifier that demands minimum output on time, dominates control of the loop.

The MC35060A/34060A/33060A has an internal 5.0 V reference capable of sourcing up to 10 mA of load currents for external bias circuits. The reference has an internal accuracy of $\pm 1.5\%$ with a typical thermal drift of less than 50 mV over an operating temperature range of 0° to $+70^\circ\text{C}$.

MAXIMUM RATINGS (Full operating ambient temperature range applies unless otherwise noted)

Rating	Symbol	MC35060A	MC34060A	MC33060A	Unit
Power Supply Voltage	V_{CC}	42	42	42	V
Collector Output Voltage	V_C	42	42	42	V
Collector Output Current (Note 1)	I_C	500	500	500	mA
Amplifier Input Voltage Range	V_{IR}	-0.3 to $+42$	-0.3 to $+42$	-0.3 to $+42$	V
Power Dissipation @ $T_A \leq 45^\circ\text{C}$	P_D	1000	1000	1000	mW
Operating Junction Temperature	T_J	—	125	125	$^\circ\text{C}$
Plastic Package		150	—	—	
Ceramic Package		—	—	—	
Operating Ambient Temperature Range	T_A	-55 to $+125$	0 to $+70$	-40 to $+85$	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	—	-55 to $+125$	-55 to $+125$	$^\circ\text{C}$
Plastic Package		-65 to $+150$	—	—	
Ceramic Package		—	—	—	

THERMAL CHARACTERISTICS

Characteristic	Symbol	L Suffix Ceramic Package	P Suffix Plastic Package	D Suffix Plastic Package	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	100	80	120	$^\circ\text{C}/\text{W}$
Derating Ambient Temperature	T_A	50	45	45	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS

Condition	Symbol	MC35060A/MC34060A/MC33060A			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	7.0	15	40	V
Collector Output Voltage	V_C	—	30	40	V
Collector Output Current	I_C	—	—	200	mA
Amplifier Input Voltage	V_{in}	-0.3	—	$V_{CC} - 2$	V
Current Into Feedback Terminal	I_{fb}	—	—	0.3	mA
Reference Output Current	I_{ref}	—	—	10	mA
Timing Resistor	R_T	1.8	47	500	$k\Omega$
Timing Capacitor	C_T	0.00047	0.001	10	μF
Oscillator Frequency	f_{osc}	1.0	25	200	kHz
PWM Input Voltage (Pins 3 and 4)	—	-0.3	—	5.3	V

Note 1. Maximum thermal limits must be observed.

MC34060A, MC35060A, MC33060A

ELECTRICAL CHARACTERISTICS ($V_{CC} = 15\text{ V}$, $C_T = 0.01\text{ }\mu\text{F}$, $R_T = 12\text{ k}\Omega$) unless otherwise noted. For typical values $T_A = 25^\circ\text{C}$, for min/max values T_A is the operating ambient temperature range that applies unless otherwise noted.

Characteristic	Symbol	MC35060A/MC34060A/MC33060A			Unit
		Min	Typ	Max	

REFERENCE SECTION

Reference Voltage ($I_O = 1.0\text{ mA}$, $T_A = 25^\circ\text{C}$) ($I_O = 1.0\text{ mA}$)	V_{ref}	4.925 4.9	5.0 —	5.075 5.1	V
Line Regulation ($V_{CC} = 7.0\text{ V to }40\text{ V}$, $I_O = 1.0\text{ mA}$)	Reg_{line}	—	2.0	25	mV
Load Regulation ($I_O = 1.0\text{ mA to }10\text{ mA}$)	Reg_{load}	—	2.0	15	mV
Short-Circuit Output Current ($V_{ref} = 0\text{ V}$)	I_{SC}	15	35	75	mA

OUTPUT SECTION

Collector Off-State Current ($V_{CC} = 40\text{ V}$, $V_{CE} = 40\text{ V}$)	$I_{C(off)}$	—	2.0	100	μA
Emitter Off-State Current ($V_{CC} = 40\text{ V}$, $V_C = 40\text{ V}$, $V_E = 0\text{ V}$)	$I_{E(off)}$	—	—	100	μA
Collector-Emitter Saturation Voltage (Note 2) Common-Emitter ($V_E = 0\text{ V}$, $I_C = 200\text{ mA}$) Emitter-Follower ($V_C = 15\text{ V}$, $I_E = -200\text{ mA}$)	$V_{sat(C)}$	—	1.1	1.5	V
	$V_{sat(E)}$	—	1.5	2.5	
Output Voltage Rise Time ($T_A = 25^\circ\text{C}$) Common-Emitter (See Figure 12) Emitter-Follower (See Figure 13)	t_r	—	100	200	ns
		—	100	200	
Output Voltage Fall Time ($T_A = 25^\circ\text{C}$) Common-Emitter (See Figure 12) Emitter-Follower (See Figure 13)	t_f	—	40	100	ns
		—	40	100	

Characteristic	Symbol	MC35060A/MC34060A/MC33060A			Unit
		Min	Typ	Max	

ERROR AMPLIFIER SECTIONS

Input Offset Voltage ($V_O[\text{Pin } 3] = 2.5\text{ V}$)	V_{IO}	—	2.0	10	mV
Input Offset Current ($V_C[\text{Pin } 3] = 2.5\text{ V}$)	I_{IO}	—	5.0	250	nA
Input Bias Current ($V_O[\text{Pin } 3] = 2.5\text{ V}$)	I_{IB}	—	0.1	2.0	μA
Input Common-Mode Voltage Range ($V_{CC} = 40\text{ V}$)	V_{ICR}	0 to $V_{CC} - 2.0$	—	—	V
Inverting Input Voltage Range	$V_{IR(INV)}$	0.3 to $V_{CC} - 2.0$	—	—	V
Open Loop Voltage Gain ($\Delta V_O = 3.0\text{ V}$, $V_O = 0.5\text{ to }3.5\text{ V}$, $R_L = 2.0\text{ k}\Omega$)	A_{VOL}	70	95	—	dB

Note 2: Low duty cycle techniques are used during test to maintain junction temperature as close to ambient temperatures as possible.

3

MC34060A, MC35060A, MC33060A

ELECTRICAL CHARACTERISTICS ($V_{CC} = 15\text{ V}$, $C_T = 0.01\text{ }\mu\text{F}$, $R_T = 12\text{ k}\Omega$ unless otherwise noted. For typical values $T_A = 25^\circ\text{C}$, for min/max values T_A is the operating ambient temperature range that applies unless otherwise noted.)

Characteristic	Symbol	MC35060A/MC34060A/MC33060A			Unit
		Min	Typ	Max	
ERROR AMPLIFIER SECTIONS (Continued)					
Unity-Gain Crossover Frequency ($V_O = 0.5$ to 3.5 V, $R_L = 2.0$ k Ω)	f_c	—	600	—	kHz
Phase Margin at Unity-Gain ($V_O = 0.5$ to 3.5 V, $R_L = 2.0$ k Ω)	ϕ_m	—	65	—	deg.
Common-Mode Rejection Ratio ($V_{CC} = 40$ V, $V_{in} = 0$ V to 38 V)	CMRR	65	90	—	dB
Power Supply Rejection Ratio ($\Delta V_{CC} = 33$ V, $V_O = 2.5$ V, $R_L = 2.0$ k Ω)	PSRR	—	100	—	dB
Output Sink Current ($V_O[\text{Pin } 3] = 0.7$ V)	I_O	0.3	0.7	—	mA
Output Source Current ($V_O[\text{Pin } 3] = 3.5$ V)	I_O	2.0	4.0	—	mA

PWM COMPARATOR SECTION (Test circuit Figure 11)

Input Threshold Voltage (Zero Duty Cycle)	V_{TH}	—	3.5	4.5	V
Input Sink Current ($V[\text{Pin } 3] = 0.7\text{ V}$)	I_I	0.3	0.7	—	mA

DEAD-TIME CONTROL SECTION (Test Circuit Figure 11)

Input Bias Current (Pin 4) ($V_{in} = 0\text{ to }5.25\text{ V}$)	I_{IBIDT}	—	1.0	10	μA
Maximum Output Duty Cycle ($V_{in} = 0\text{ V}$, $C_T = 0.01\text{ }\mu\text{F}$, $R_T = 12\text{ k}\Omega$) ($V_{in} = 0\text{ V}$, $C_T = 0.001\text{ }\mu\text{F}$, $R_T = 47\text{ k}\Omega$)	DC_{max}	90 —	96 92	100 —	%
Input Threshold Voltage (Pin 4) (Zero Duty Cycle) (Maximum Duty Cycle)	V_{TH}	— 0	2.8 —	3.3 —	V

OSCILLATOR SECTION

Frequency ($C_T = 0.01\text{ }\mu\text{F}$, $R_T = 12\text{ k}\Omega$) $T_A = 25^\circ\text{C}$ $T_A = T_{low}\text{ to }T_{high}$ ($C_T = 0.001\text{ }\mu\text{F}$, $R_T = 47\text{ k}\Omega$)	f_{osc}	9.7 9.5 —	10.5 — 25	11.3 12.5 —	kHz
Standard Deviation of Frequency* ($C_T = 0.001\text{ }\mu\text{F}$, $R_T = 47\text{ k}\Omega$)	σf_{osc}	—	1.5	—	%
Frequency Change with Voltage ($V_{CC} = 7.0\text{ V to }40\text{ V}$)	$\Delta f_{osc}(\Delta V)$	—	0.5	2.0	%
Frequency Change with Temperature ($\Delta T_A = T_{low}\text{ to }T_{high}$) ($C_T = 0.01\text{ }\mu\text{F}$, $R_T = 12\text{ k}\Omega$)	$\Delta f_{osc}(\Delta T)$	— —	4.0 —	— —	%

UNDERVOLTAGE LOCKOUT SECTION

Turn-On Threshold (V_{CC} increasing, $I_{ref} = 1.0\text{ mA}$)	V_{th}	4.0	4.7	5.5	V
Hysteresis	V_H	50	150	300	mV

TOTAL DEVICE

Standby Supply Current (Pin 6 at V_{ref} , all other inputs and outputs open) ($V_{CC} = 15\text{ V}$) ($V_{CC} = 40\text{ V}$)	I_{CC}	— —	5.5 7.0	10 15	mA
Average Supply Current ($V[\text{Pin } 4] = 2.0\text{ V}$, $C_T = 0.001\text{ }\mu\text{F}$, $R_T = 47\text{ k}\Omega$). See Figure 11.	I_S	—	7.0	—	mA

*Standard deviation is a measure of the statistical distribution about the mean as derived from the formula; σ

$$\sigma = \sqrt{\frac{\sum_{n=1}^N (x_n - \bar{x})^2}{N - 1}}$$

FIGURE 3 — OSCILLATOR FREQUENCY
versus TIMING RESISTANCE

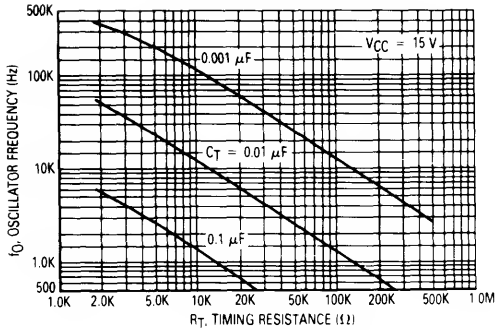


FIGURE 4 — OPEN-LOOP VOLTAGE GAIN AND PHASE
versus FREQUENCY

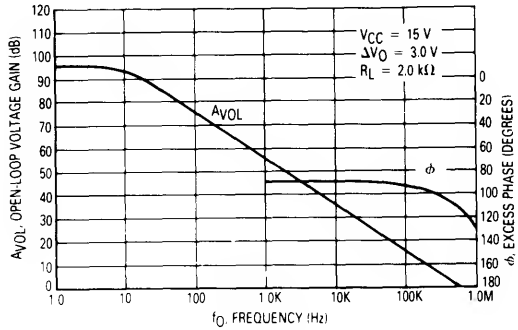


FIGURE 5 — PERCENT DEAD-TIME versus
OSCILLATOR FREQUENCY

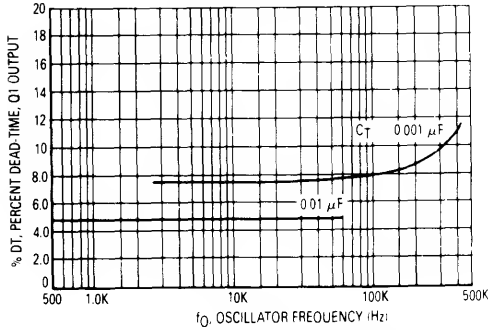


FIGURE 6 — PERCENT DUTY CYCLE versus
DEAD-TIME CONTROL VOLTAGE

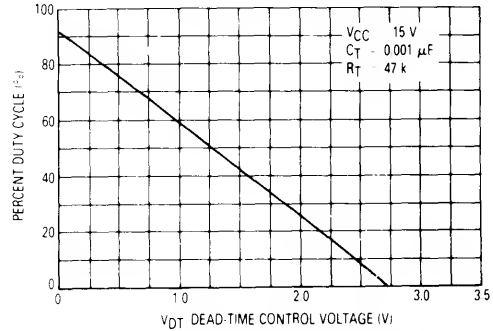


FIGURE 7 — EMITTER FOLLOWER CONFIGURATION
OUTPUT SATURATION VOLTAGE versus
EMITTER CURRENT

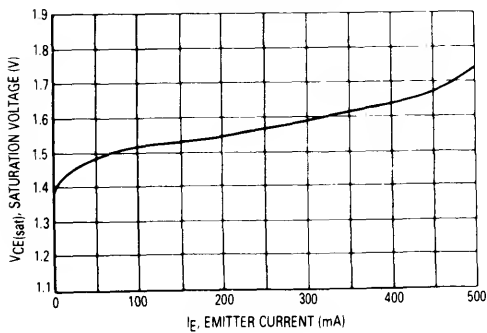


FIGURE 8 — COMMON EMITTER CONFIGURATION
OUTPUT SATURATION VOLTAGE versus
COLLECTOR CURRENT

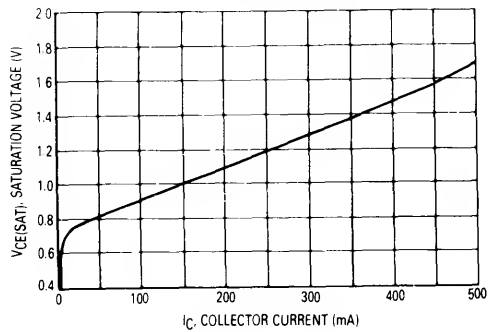


FIGURE 9 — STANDBY SUPPLY CURRENT
versus SUPPLY VOLTAGE

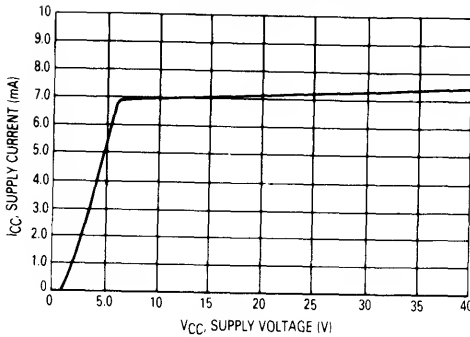


FIGURE 10 — UNDERVOLTAGE LOCKOUT THRESHOLDS
versus REFERENCE LOAD CURRENT

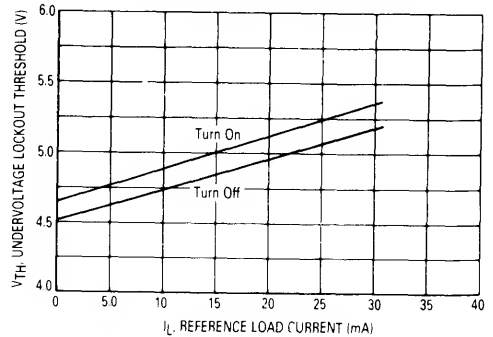


FIGURE 11 — ERROR AMPLIFIER CHARACTERISTICS

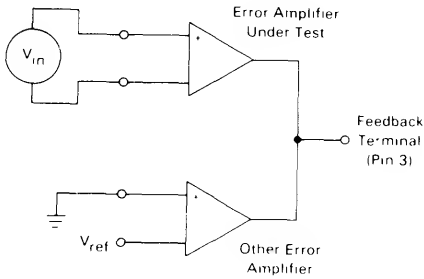


FIGURE 12 — DEAD-TIME AND FEEDBACK CONTROL
TEST CIRCUIT

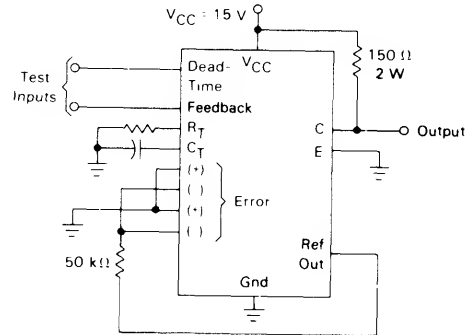


FIGURE 13 — COMMON-EMITTER CONFIGURATION
TEST CIRCUIT AND WAVEFORM

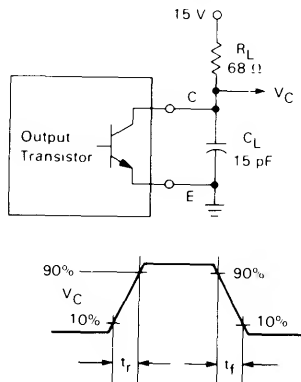


FIGURE 14 — EMITTER-FOLLOWER CONFIGURATION
TEST CIRCUIT AND WAVEFORM

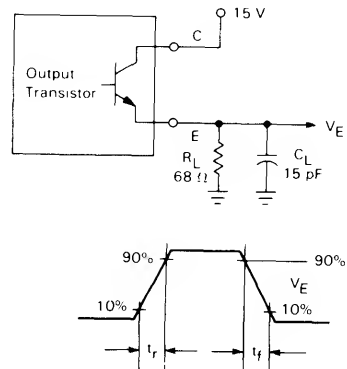


FIGURE 15 — ERROR AMPLIFIER SENSING TECHNIQUES

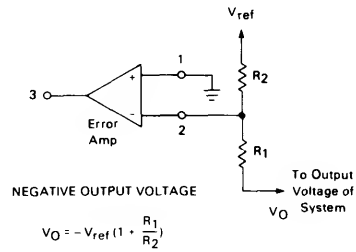
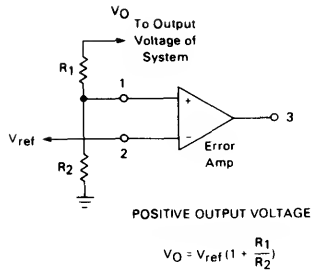
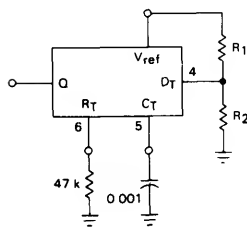


FIGURE 16 — DEAD-TIME CONTROL CIRCUIT



$$\text{Max \% On Time} \approx 92 - \left(\frac{160}{1 + \frac{R_1}{R_2}} \right)$$

FIGURE 17 — SOFT-START CIRCUIT

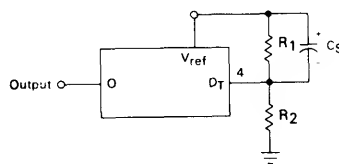
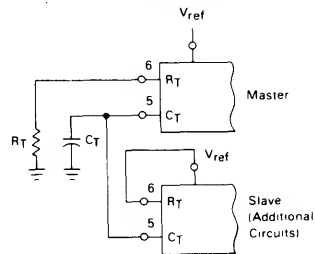
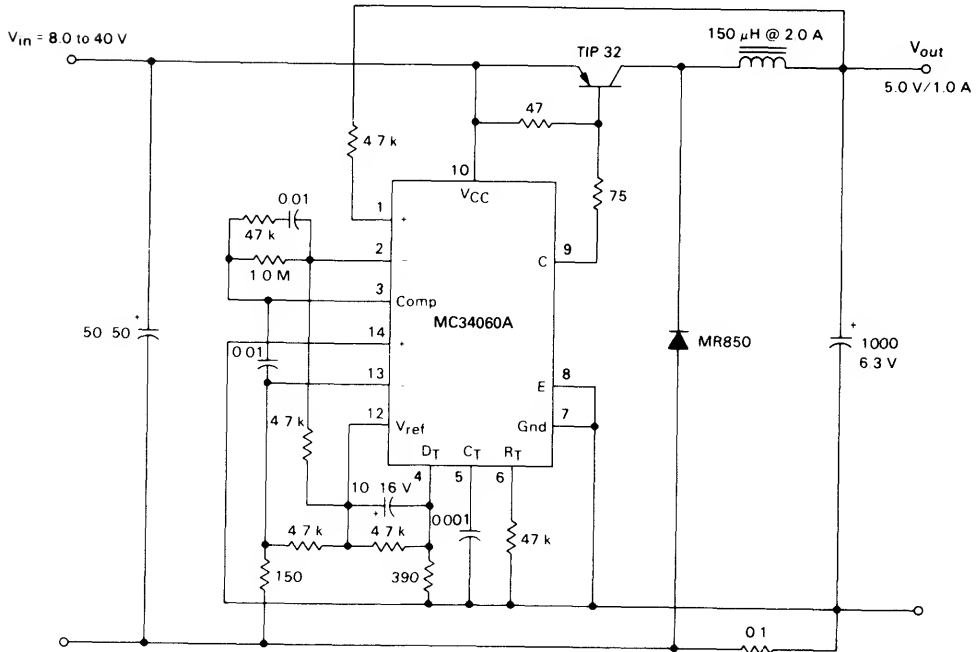


FIGURE 18 — SLAVING TWO OR MORE CONTROL CIRCUITS



MC34060A, MC35060A, MC33060A

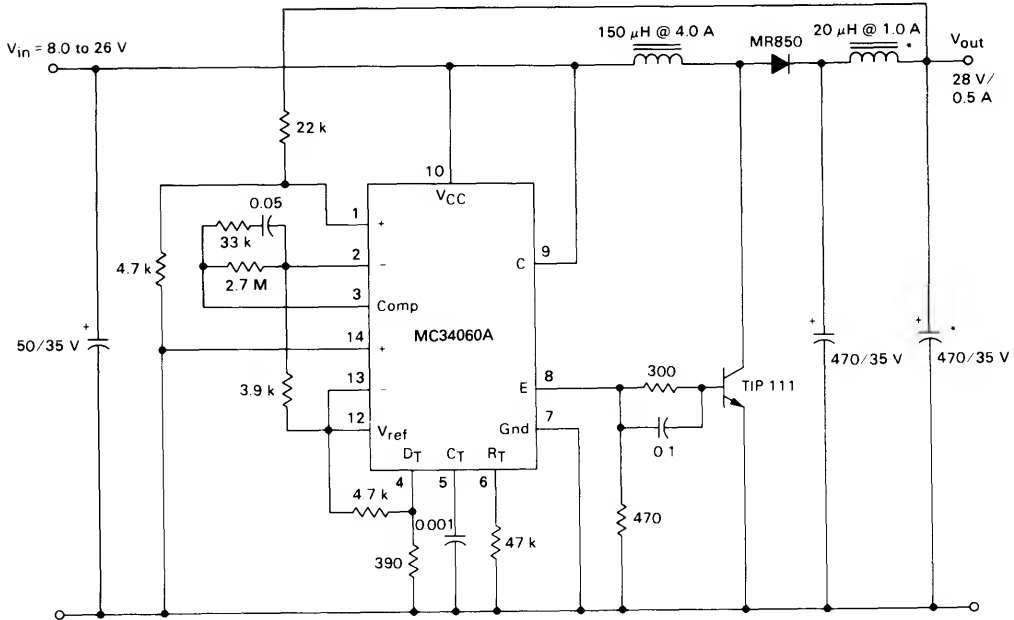
FIGURE 19 — STEP-DOWN CONVERTER WITH SOFT-START AND OUTPUT CURRENT LIMITING



Test	Conditions	Results
Line Regulation	$V_{in} = 8.0 \text{ V to } 40 \text{ V}$, $I_O = 1.0 \text{ A}$	25 mV 0.5%
Load Regulation	$V_{in} = 12 \text{ V}$, $I_O = 1.0 \text{ mA to } 1.0 \text{ A}$	3.0 mV 0.06%
Output Ripple	$V_{in} = 12 \text{ V}$, $I_O = 1.0 \text{ A}$	75 mVp-p P.A.R.D.
Short Circuit Current	$V_{in} = 12 \text{ V}$, $R_L = 0.1 \Omega$	1.6 A
Efficiency	$V_{in} = 12 \text{ V}$, $I_O = 1.0 \text{ A}$	73%

MC34060A, MC35060A, MC33060A

FIGURE 20 — STEP-UP CONVERTER

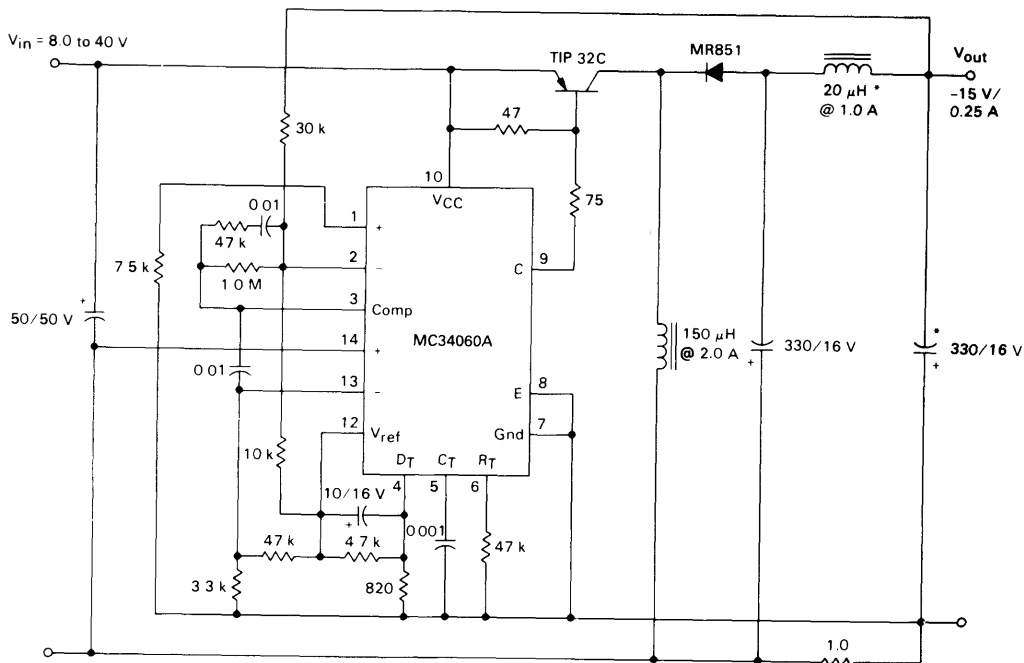


TEST	CONDITIONS	RESULTS
Line Regulation	$V_{in} = 8.0 \text{ V to } 26 \text{ V}, I_O = 0.5 \text{ A}$	40 mV 0.14%
Load Regulation	$V_{in} = 12 \text{ V}, I_O = 10 \text{ mA to } 0.5 \text{ A}$	5.0 mV 0.18%
Output Ripple	$V_{in} = 12 \text{ V}, I_O = 0.5 \text{ A}$	24 mV p-p A R D
Efficiency	$V_{in} = 12 \text{ V}, I_O = 0.5 \text{ A}$	75%

* Optional circuit to minimize output ripple

MC34060A, MC35060A, MC33060A

FIGURE 21 — STEP-UP/DOWN VOLTAGE INVERTING CONVERTER WITH SOFT-START AND CURRENT LIMITING



TEST	CONDITIONS	RESULTS
Line Regulation	$V_{in} = 8.0 \text{ V to } 40 \text{ V}$, $I_O = 250 \text{ mA}$	52 mV 0.35%
Load Regulation	$V_{in} = 12 \text{ V}$, $I_O = 1 \text{ mA to } 250 \text{ mA}$	47 mV 0.32%
Output Ripple	$V_{in} = 12 \text{ V}$, $I_O = 250 \text{ mA}$	10 mV p p P.A.R.D.
Short Circuit Current	$V_{in} = 12 \text{ V}$, $R_L = 0.1 \Omega$	330 mA
Efficiency	$V_{in} = 12 \text{ V}$, $I_O = 250 \text{ mA}$	86%

* Optional circuit to minimize output ripple

[illegible]

TEST	CONDITIONS	RESULTS
Line Regulation 50 V	V_{in} 95 to 135 Vac, I_O 30 A	20 mV 0.40%
Line Regulation 12 V	V_{in} 95 to 135 Vac, I_O -0.75 A	52 mV 0.26%
Load Regulation 50 V	V_{in} 115 Vac, I_O 10 to 40 A	476 mV 9.5%
Load Regulation 12 V	V_{in} = 115 Vac, I_O = ± 0.4 to ± 0.9 A	300 mV 2.5%
Output Ripple 50 V	V_{in} 115 Vac, I_O 30 A	45 mV p p P A R D
Output Ripple 12 V	V_{in} 115 Vac, I_O 30.75 A	75 mV p p P A R D
Efficiency	V_{in} = 115 Vac, I_O 50 V = 30 A I_O ± 12 = ± 0.75 A	74%

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

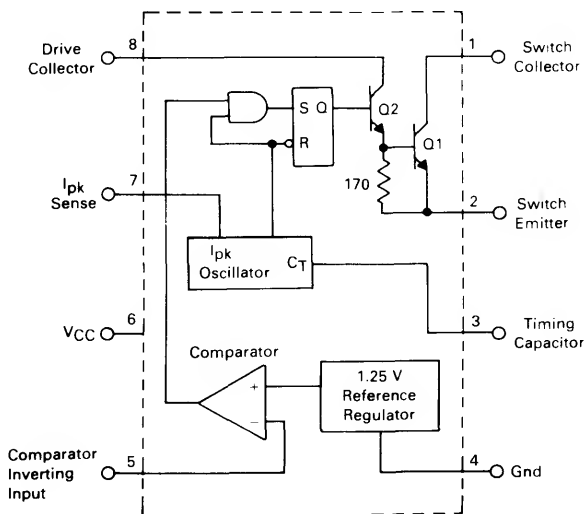
3

DC-TO-DC CONVERTER CONTROL CIRCUITS

The MC34063 Series is a monolithic control circuit containing the primary functions required for dc-to-dc converters. The device consists of an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active current limit circuit, driver and high current output switch. This series was specifically designed to be incorporated in Step-Down and Step-Up and Voltage-Inverting applications with a minimum number of external components.

- Operation from 2.5 V to 40 V Input
- Low Standby Current
- Current Limiting
- Output Switch Current of 1.5 A
- Output Voltage Adjustable from 1.25 to 40 V
- Frequency of Operation to 100 kHz

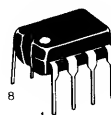
FUNCTIONAL BLOCK DIAGRAM



MC34063
MC35063
MC33063

DC-TO-DC CONVERTER CONTROL CIRCUITS

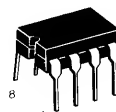
SILICON MONOLITHIC
INTEGRATED CIRCUITS



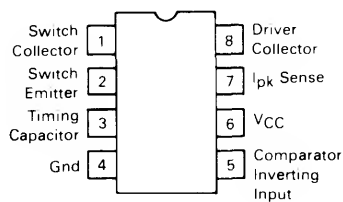
P1 SUFFIX
PLASTIC PACKAGE
CASE 626

"NOT FOR NEW DESIGN-INS"

U SUFFIX
CERAMIC PACKAGE
CASE 693



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC35063U	-55 to +125°C	Ceramic DIP
MC33063U	-55 to +125°C	Ceramic DIP
MC33063P1	-40 to +85°C	Plastic DIP
MC34063U	0 to +70°C	Ceramic DIP
MC34063P1	0 to +70°C	Plastic DIP

MC34063, MC35063, MC33063

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	Vdc
Comparator Input Voltage Range	V_{IR}	-0.3 to +40	Vdc
Switch Collector Voltage	$V_{C(switch)}$	40	Vdc
Switch Emitter Voltage	$V_{E(switch)}$	40	Vdc
Switch Collector to Emitter Voltage	$V_{CE(switch)}$	40	Vdc
Driver Collector Voltage	$V_{C(driver)}$	40	Vdc
Switch Current	I_{SW}	1.5	Amps
Power Dissipation and Thermal Characteristics			
Ceramic Package $T_A = +25^\circ\text{C}$ Derate above $T_A = +25^\circ\text{C}$	P_D $1/\theta_{JA}$	1.25 10	W mW/°C
Plastic Package $T_A = +25^\circ\text{C}$ Derate above $T_A = +25^\circ\text{C}$	P_D $1/\theta_{JA}$	1.0 10	W mW/°C
Operating Junction Temperature	T_J	+150 +125	°C
Operating Ambient Temperature Range	T_A	-55 to +125 -40 to +85 0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

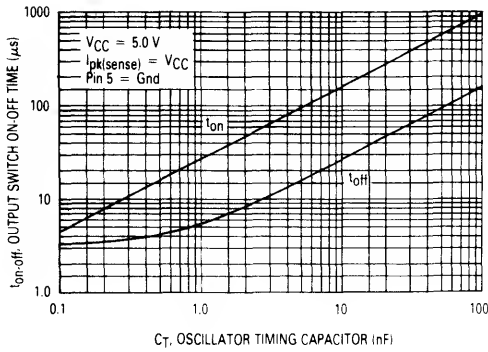
ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0\text{ V}$; $T_A = T_{low}$ to T_{high} [Note 1] unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Charging Current ($5.0\text{ V} \leq V_{CC} \leq 40\text{ V}$, $T_A = 25^\circ\text{C}$)	I_{chg}	20	35	50	μA
Discharge current ($5.0\text{ V} \leq V_{CC} \leq 40\text{ V}$; $T_A = 25^\circ\text{C}$)	I_{dischg}	150	200	250	μA
Voltage Swing ($T_A = 25^\circ\text{C}$)	V_{osc}	—	0.5	—	V _{p-p}
Discharge to Charge Current Ratio ($I_{pk(sense)} = V_{CC}$, $T_A = 25^\circ\text{C}$)	I_{dischg}/I_{chg}	—	6.0	—	—
Current Limit Sense Voltage $I_{chg} = I_{dischg}$, $T_A = 25^\circ\text{C}$	$V_{Ipk(sense)}$	250	300	350	mV
OUTPUT SWITCH (Note 2)					
Saturation Voltage, Darlington Connection $I_{SW} = 1.0\text{ A}$; $V_{C(driver)} = V_{C(switch)}$	$V_{CE(sat)}$	—	1.0	1.3	V
Saturation Voltage $I_{SW} = 1.0\text{ A}$; $I_{C(driver)} = 50\text{ mA}$, (Forced B ≈ 20)	$V_{CE(sat)}$	—	0.45	0.7	V
DC Current Gain $I_{SW} = 1.0\text{ A}$; $V_{CE} = 5.0\text{ V}$; $T_A = 25^\circ\text{C}$	h_{FE}	35	120	—	—
Collector Off-State Current ($V_{CE} = 40\text{ V}$; $T_A = 25^\circ\text{C}$)	$I_{C(off)}$	—	10	—	nA
COMPARATOR					
Threshold Voltage	V_{th}	1.18	1.25	1.32	V
Threshold Voltage Line Regulation ($3.0\text{ V} \leq V_{CC} \leq 40\text{ V}$)	Reg_{line}	—	0.04	0.2	mV/V
Input Bias Current ($V_{in} = 0\text{ V}$)	I_{IB}	—	40	400	nA
TOTAL DEVICE					
Supply Current $5.0\text{ V} \leq V_{CC} \leq 40\text{ V}$, $C_T = 0.001\text{ }\mu\text{F}$ $I_{pk(sense)} = V_{CC}$, V pin 5 > V_{th} , Pin 2 = Gnd, Remaining pins open	I_{CC}	—	2.4	3.5	mA

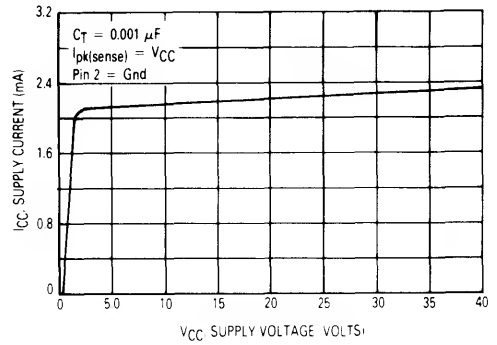
NOTES:

- $T_{low} = -55^\circ\text{C}$ for MC35063 $T_{high} = +125^\circ\text{C}$ for MC35063
 -40°C for MC33063 $+85^\circ\text{C}$ for MC33063
 0°C for MC34063 $+70^\circ\text{C}$ for MC34063
- Output switch tests are performed under pulsed conditions to minimize power dissipation.

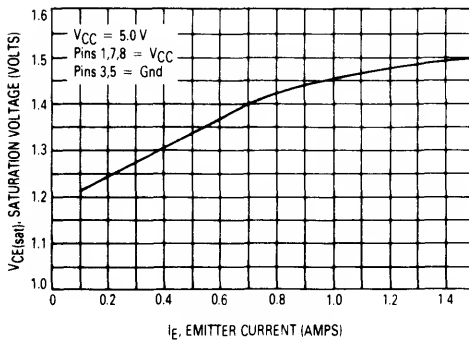
**FIGURE 1 — OUTPUT SWITCH ON-OFF TIME
versus OSCILLATOR TIMING
CAPACITOR**



**FIGURE 2 — STANDBY SUPPLY CURRENT
versus SUPPLY VOLTAGE**



**FIGURE 3 — EMITTER-FOLLOWER CONFIGURATION
OUTPUT SWITCH SATURATION VOLTAGE
versus EMITTER CURRENT**



**FIGURE 4 — COMMON-EMITTER CONFIGURATION
OUTPUT SWITCH SATURATION VOLTAGE
versus COLLECTOR CURRENT**

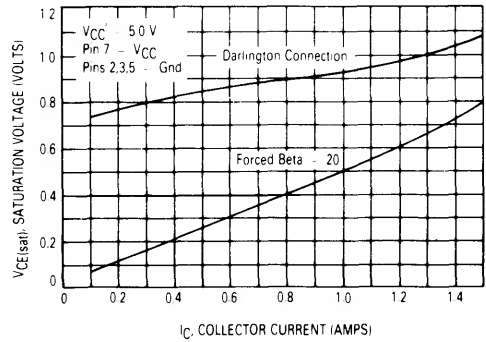
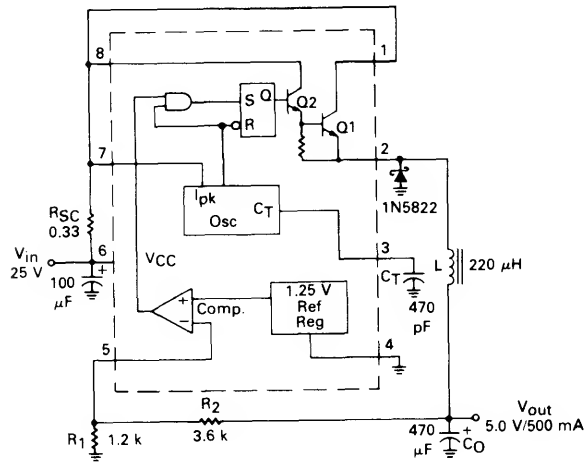


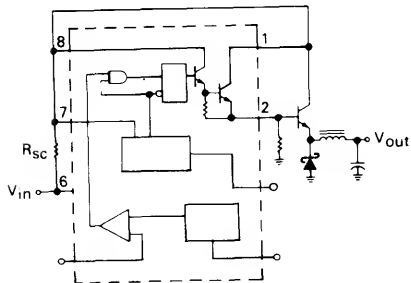
FIGURE 5 — STEP-DOWN CONVERTER



Test	Conditions	Results
Line Regulation	$V_{in} = 15 \text{ to } 25 \text{ V}, I_o = 500 \text{ mA}$	15 mV
Load Regulation	$V_{in} = 25 \text{ V}, I_o = 50 \text{ to } 500 \text{ mA}$	5.0 mV
Output Ripple	$V_{in} = 25 \text{ V}, I_o = 500 \text{ mA}$	40 mV _{p-p}
Short Circuit Current	$V_{in} = 25 \text{ V}, R_L = 0.1 \Omega$	2.3 A
Efficiency	$V_{in} = 25 \text{ V}, I_o = 500 \text{ mA}$	84.7%

FIGURE 6 — EXTERNAL CURRENT BOOST CONNECTIONS
FOR I_C PEAK GREATER THAN 1.5 A

6A — EXTERNAL NPN SWITCH



6B — EXTERNAL PNP SATURATED SWITCH

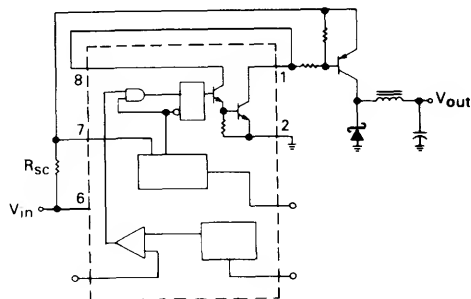
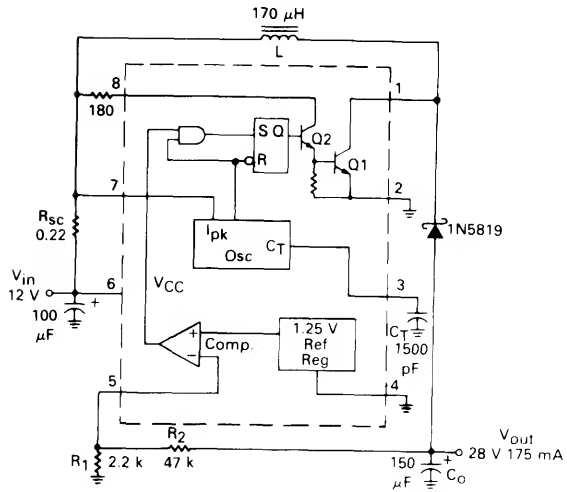


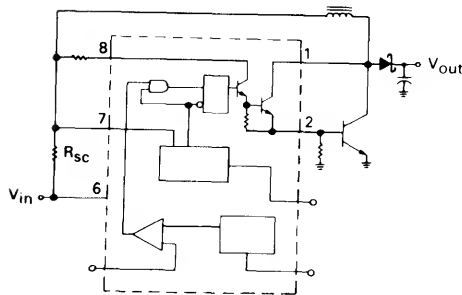
FIGURE 7 — STEP-UP CONVERTER



Test	Conditions	Results
Line Regulation	$V_{in} = 8.0 \text{ to } 16 \text{ V}$, $I_o = 175 \text{ mA}$	12 mV
Load Regulation	$V_{in} = 12 \text{ V}$, $I_o = 75 \text{ to } 175 \text{ mA}$	45 mV
Output Ripple	$V_{in} = 12 \text{ V}$, $I_o = 175 \text{ mA}$	150 mV _{p-p}
Efficiency	$V_{in} = 12 \text{ V}$, $I_o = 175 \text{ mA}$	93%

FIGURE 8 — EXTERNAL CURRENT BOOST CONNECTIONS
FOR I_C PEAK GREATER THAN 1.5 A

8A — EXTERNAL NPN SWITCH



8B — EXTERNAL NPN SATURATED SWITCH

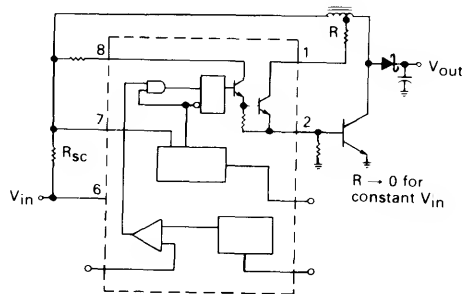


FIGURE 9 — DESIGN FORMULA TABLE

Calculation	Step-Down	Step-Up
$\frac{t_{on}}{t_{off}}$	$\frac{V_{out} + V_F}{V_{in(min)} - V_{sat} - V_{out}}$	$\frac{V_{out} + V_F - V_{in(min)}}{V_{in(min)} - V_{sat}}$
$(t_{on} + t_{off})_{max}$	$\frac{1}{f_{min}}$	$\frac{1}{f_{min}}$
C_T	$4 \times 10^{-5} t_{on}$	$4 \times 10^{-5} t_{on}$
$I_{pk(switch)}$	$2I_{out(max)}$	$2I_{out(max)} \left(\frac{t_{on}}{t_{off}} + 1 \right)$
R_{SC}	$0.33/I_{pk(switch)}$	$0.33/I_{pk(switch)}$
$L_{(min)}$	$\left(\frac{V_{in(min)} - V_{sat} - V_{out}}{I_{pk(switch)}} \right) t_{on(max)}$	$\left(\frac{V_{in(min)} - V_{sat}}{I_{pk(switch)}} \right) t_{on(max)}$
C_o	$\frac{I_{pk(switch)} (t_{on} + t_{off})}{8 V_{ripple(p-p)}}$	$\approx \frac{I_{out} t_{on}}{V_{ripple(p-p)}}$

 V_{sat} = Saturation voltage of the output switch. V_F = Forward voltage drop of the ringback rectifier.**The following power supply characteristics must be chosen:**

V_{in} — Nominal input voltage. If this voltage is not constant, then use $V_{in(max)}$ for step-down and $V_{in(min)}$ for step-up converter.

V_{out} — Desired output voltage, $V_{out} = 1.25 \left(1 + \frac{R_2}{R_1} \right)$.

I_{out} — Desired output current.

f_{min} — Minimum desired output switching frequency at the selected values for V_{in} and I_o .

$V_{ripple(p-p)}$ — Desired peak-to-peak output ripple voltage. In practice, the calculated value will need to be increased due to the capacitor's equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly effect the line and load regulation.

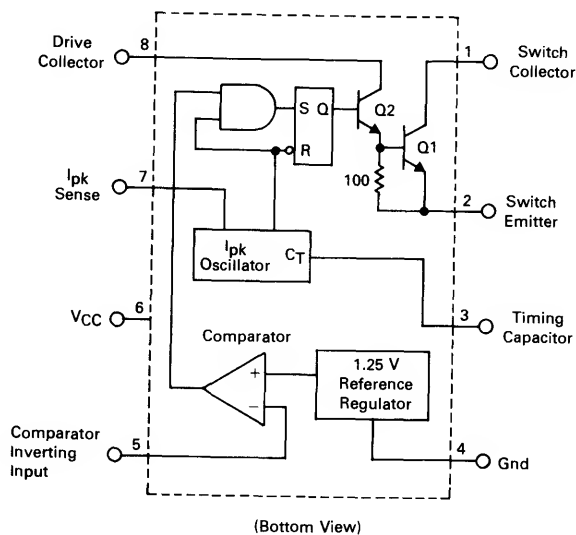
Note: For further information refer to application note AN920 Rev. 2.

DC-TO-DC CONVERTER CONTROL CIRCUITS

The MC34063A Series is a monolithic control circuit containing the primary functions required for DC-to-DC converters. These devices consist of an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active current limit circuit, driver and high current output switch. This series was specifically designed to be incorporated in Step-Down and Step-Up and Voltage-Inverting applications with a minimum number of external components. Refer to Application Note AN920R2 for additional design information.

- Operation from 3.0 V to 40 V Input
- Low Standby Current
- Current Limiting
- Output Switch Current to 1.5 A
- Output Voltage Adjustable
- Frequency Operation to 100 kHz
- Precision 2% Reference

FUNCTIONAL BLOCK DIAGRAM

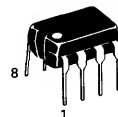


MC34063A
MC35063A
MC33063A

DC-TO-DC CONVERTER CONTROL CIRCUITS

SILICON MONOLITHIC INTEGRATED CIRCUITS

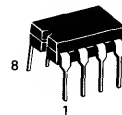
P1 SUFFIX
PLASTIC PACKAGE
CASE 626



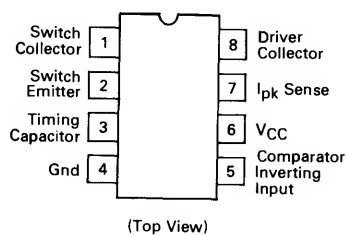
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)



**U SUFFIX
CERAMIC PACKAGE
CASE 693**



PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
MC35063AU	-55 to +125°C	Ceramic DIP
MC33063AD	-40 to +85°C	Plastic SOIC
MC33063AP1		Plastic DIP
MC34063AD	0 to +70°C	Plastic SOIC
MC34063AP1		Plastic DIP

MC34063A, MC35063A, MC33063A

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	Vdc
Comparator Input Voltage Range	V_{IR}	-0.3 to +40	Vdc
Switch Collector Voltage	$V_{C(switch)}$	40	Vdc
Switch Emitter Voltage ($V_{Pin\ 1} = 40\text{ V}$)	$V_{E(switch)}$	40	Vdc
Switch Collector to Emitter Voltage	$V_{CE(switch)}$	40	Vdc
Driver Collector Voltage	$V_{C(driver)}$	40	Vdc
Driver Collector Current (Note 1)	$I_{C(driver)}$	100	mA
Switch Current	I_{SW}	1.5	Amps
Power Dissipation and Thermal Characteristics			
Ceramic Package, U Suffix $T_A = +25^\circ\text{C}$ Thermal Resistance	P_D $R_{\theta JA}$	1.25 100	W $^\circ\text{C/W}$
Plastic Package, P Suffix $T_A = +25^\circ\text{C}$ Thermal Resistance	P_D $R_{\theta JA}$	1.25 100	W $^\circ\text{C/W}$
SOIC Package, D Suffix $T_A = +25^\circ\text{C}$ Thermal Resistance	P_D $R_{\theta JA}$	625 160	mW $^\circ\text{C/W}$
Operating Junction Temperature	T_J	+150	$^\circ\text{C}$
Operating Ambient Temperature Range MC35063A MC33063A MC34063A	T_A	-55 to +125 -40 to +85 0 to +70	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0\text{ V}$; $T_A = T_{low}$ to T_{high} [Note 2] unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Units
OSCILLATOR					
Frequency ($V_{Pin\ 5} = 0\text{ V}$, $C_T = 1.0\text{ nF}$, $T_A = 25^\circ\text{C}$)	f_{OSC}	24	33	42	kHz
Charge Current ($V_{CC} = 5.0\text{ V}$ to 40 V , $T_A = 25^\circ\text{C}$)	I_{chg}	24	33	42	μA
Discharge Current ($V_{CC} = 5.0\text{ V}$ to 40 V , $T_A = 25^\circ\text{C}$)	I_{dischg}	140	200	260	μA
Discharge to Charge Current Ratio ($Pin\ 7 = V_{CC}$, $T_A = 25^\circ\text{C}$)	I_{dischg}/I_{chg}	5.2	6.2	7.5	—
Current Limit Sense Voltage ($I_{chg} = I_{dischg}$, $T_A = 25^\circ\text{C}$)	$V_{ipk(sense)}$	250	300	350	mV

NOTES:

- Maximum package power dissipation limits must be observed.
- $T_{low} = -55^\circ\text{C}$ for MC35063A $T_{high} = +125^\circ\text{C}$ for MC35063A
 -40°C for MC33063A $+85^\circ\text{C}$ for MC33063A
 0°C for MC34063A $+70^\circ\text{C}$ for MC34063A

MC34063A, MC35063A, MC33063A

ELECTRICAL CHARACTERISTICS — continued ($V_{CC} = 5.0 \text{ V}$; $T_A = T_{\text{low}}$ to T_{high} unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Units
OUTPUT SWITCH (Note 3)					
Saturation Voltage, Darlington Connection ($I_{SW} = 1.0 \text{ A}$, Pins 1, 8 connected)	$V_{CE(\text{sat})}$	—	1.0	1.3	V
Saturation Voltage ($I_{SW} = 1.0 \text{ A}$, $R_{\text{Pin } 8} = 82 \Omega$ to V_{CC} , Forced $\beta = 20$)	$V_{CE(\text{sat})}$	—	0.45	0.7	V
DC Current Gain ($I_{SW} = 1.0 \text{ A}$, $V_{CE} = 5.0 \text{ V}$, $T_A = 25^\circ\text{C}$)	h_{FE}	50	120	—	—
Collector Off-State Current ($V_{CE} = 40 \text{ V}$)	$I_{C(\text{off})}$	—	0.01	100	μA
COMPARATOR					
Threshold Voltage ($T_A = 25^\circ\text{C}$) ($T_A = T_{\text{low}}$ to T_{high})	V_{th}	1.225 1.21	1.25 —	1.275 1.29	V
Threshold Voltage Line Regulation ($V_{CC} = 3.0 \text{ V}$ to 40 V)	Reg_{line}	—	1.4	5.0	mV
Input Bias Current ($V_{in} = 0 \text{ V}$)	I_{IB}	—	-40	-400	nA
TOTAL DEVICE					
Supply Current ($V_{CC} = 5.0 \text{ V}$ to 40 V , $C_T = 1.0 \text{ nF}$, Pin 7 = V_{CC} , $V_{\text{Pin } 5} > V_{th}$, Pin 2 = Gnd, Remaining pins open)	I_{CC}	—	2.5	4.0	mA

NOTES:

- Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.
- If the output switch is driven into hard saturation (non-Darlington configuration) at low switch currents ($\leq 300 \text{ mA}$) and high driver currents ($\geq 30 \text{ mA}$), it may take up to $2.0 \mu\text{s}$ to come out of saturation. This condition will shorten the "off" time at frequencies $\leq 30 \text{ kHz}$, and is magnified at high temperatures. This condition does not occur with a Darlington configuration, since the output switch cannot saturate. If a non-Darlington configuration is used, the following output drive condition is recommended:

$$\text{Forced } \beta \text{ of output switch} = I_{C, \text{ output}} / (I_{C, \text{ driver}} - 7.0 \text{ mA}^*) \geq 10$$

*The 100Ω resistor in the emitter of the driver device requires about 7.0 mA before the output switch conducts.

MC34063A, MC35063A, MC33063A

FIGURE 1 — OUTPUT SWITCH ON-OFF TIME versus OSCILLATOR TIMING CAPACITOR

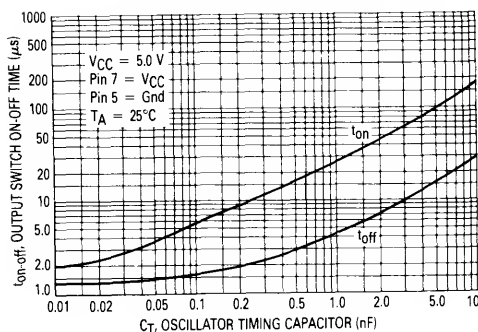


FIGURE 2 — TIMING CAPACITOR WAVEFORM

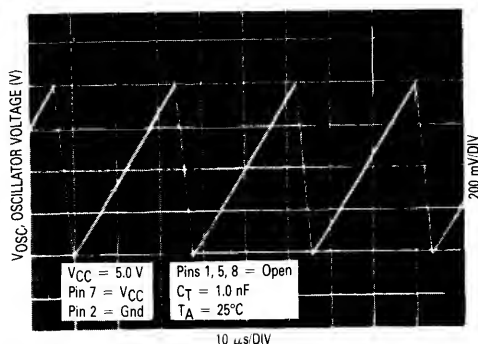


FIGURE 3 — EMITTER FOLLOWER CONFIGURATION OUTPUT SATURATION VOLTAGE versus EMITTER CURRENT

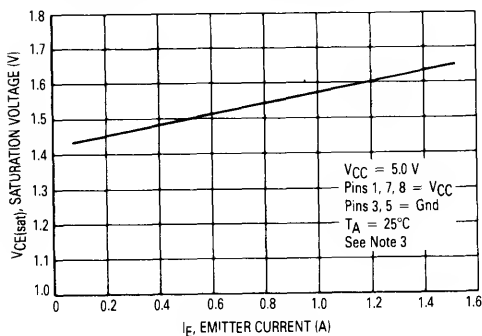


FIGURE 4 — COMMON EMITTER CONFIGURATION OUTPUT SWITCH SATURATION VOLTAGE versus COLLECTOR CURRENT

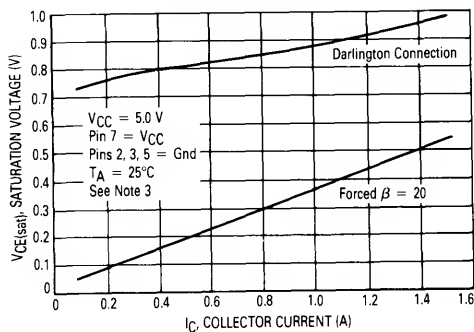


FIGURE 5 — CURRENT LIMIT SENSE VOLTAGE versus TEMPERATURE

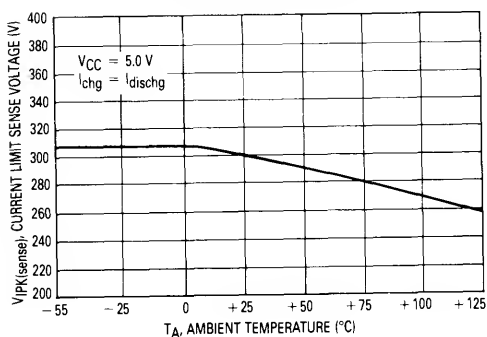
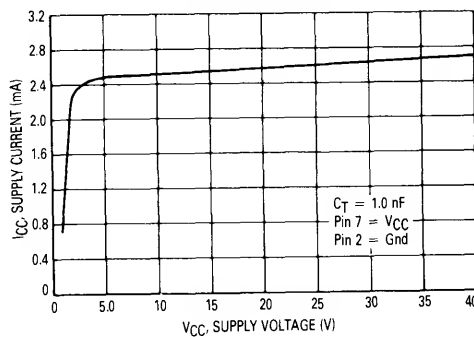
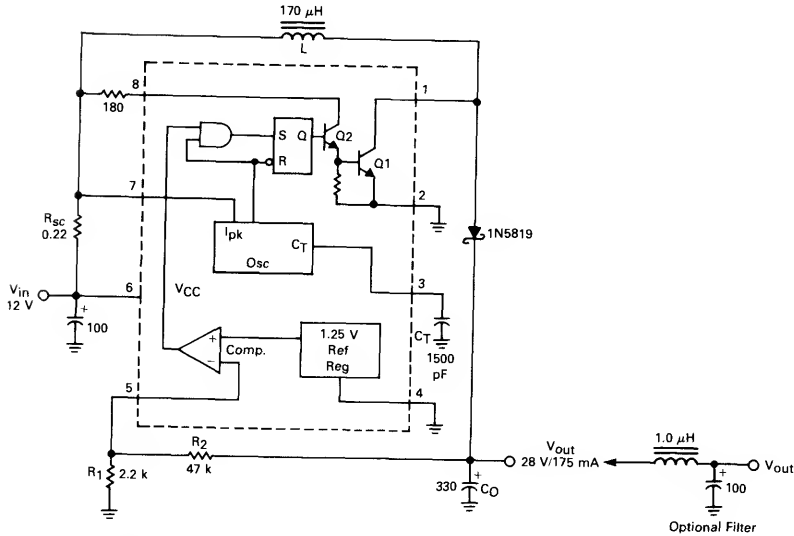


FIGURE 6 — STANDBY SUPPLY CURRENT versus SUPPLY VOLTAGE



MC34063A, MC35063A, MC33063A

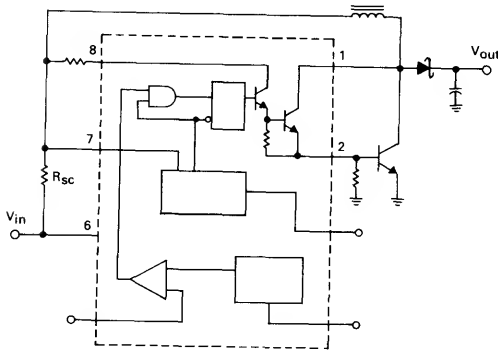
FIGURE 7 — STEP-UP CONVERTER



Test	Conditions	Results
Line Regulation	$V_{in} = 8.0 \text{ V to } 16 \text{ V}, I_O = 175 \text{ mA}$	$30 \text{ mV} = \pm 0.05\%$
Load Regulation	$V_{in} = 12 \text{ V}, I_O = 75 \text{ to } 175 \text{ mA}$	$10 \text{ mV} = \pm 0.017\%$
Output Ripple	$V_{in} = 12 \text{ V}, I_O = 175 \text{ mA}$	400 mVp-p
Efficiency	$V_{in} = 12 \text{ V}, I_O = 175 \text{ mA}$	89.2%
Output Ripple With Optional Filter	$V_{in} = 12 \text{ V}, I_O = 175 \text{ mA}$	40 mVp-p

FIGURE 8 — EXTERNAL CURRENT BOOST CONNECTIONS
FOR I_C PEAK GREATER THAN 1.5 A

8A — EXTERNAL NPN SWITCH



8B — EXTERNAL NPN SATURATED SWITCH
(REFER TO NOTE 4)

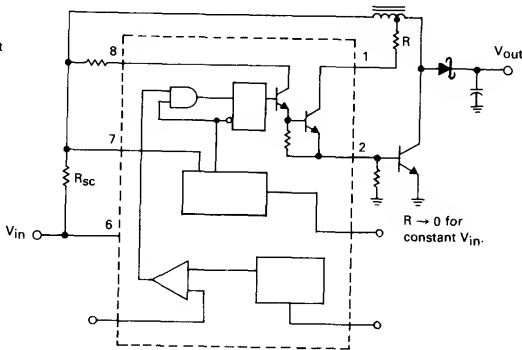
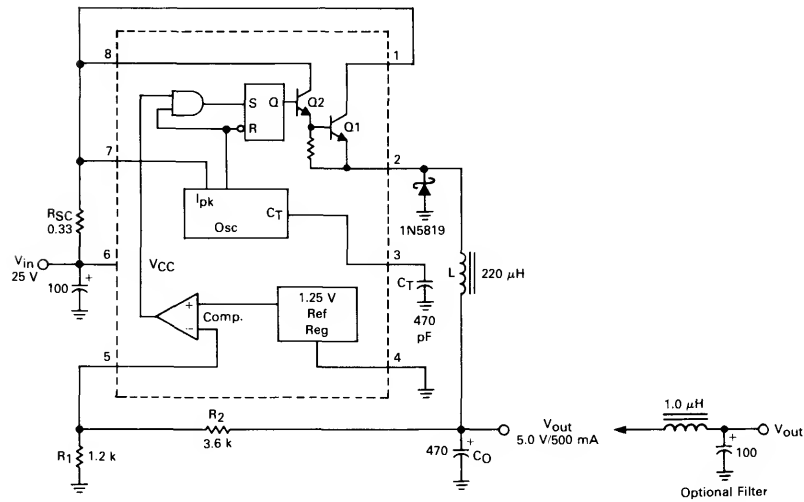


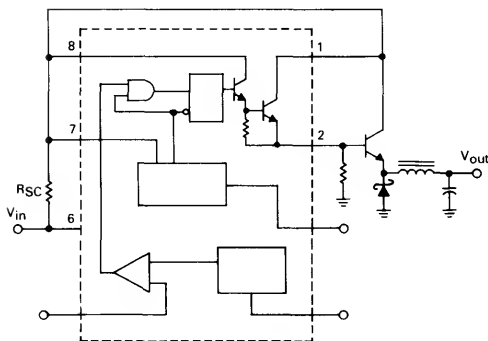
FIGURE 9 — STEP-DOWN CONVERTER



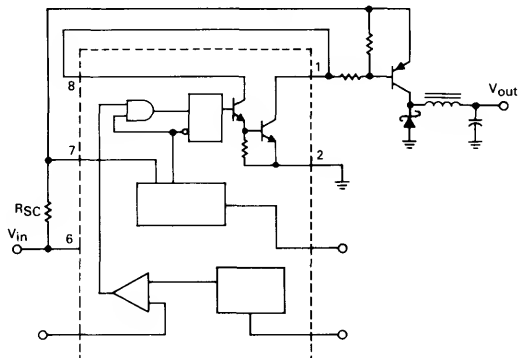
Test	Conditions	Results
Line Regulation	$V_{in} = 15 \text{ V to } 25 \text{ V}, I_O = 500 \text{ mA}$	$12 \text{ mV} = \pm 0.12\%$
Load Regulation	$V_{in} = 25 \text{ V}, I_O = 50 \text{ to } 500 \text{ mA}$	$3.0 \text{ mV} = \pm 0.03\%$
Output Ripple	$V_{in} = 25 \text{ V}, I_O = 500 \text{ mA}$	120 mVp-p
Short Circuit Current	$V_{in} = 25 \text{ V}, R_L = 0.1 \Omega$	1.1 A
Efficiency	$V_{in} = 25 \text{ V}, I_O = 500 \text{ mA}$	82.5%
Output Ripple With Optional Filter	$V_{in} = 25 \text{ V}, I_O = 500 \text{ mA}$	40 mVp-p

FIGURE 10 — EXTERNAL CURRENT BOOST CONNECTIONS
FOR I_C PEAK GREATER THAN 1.5 A

10A — EXTERNAL NPN SWITCH

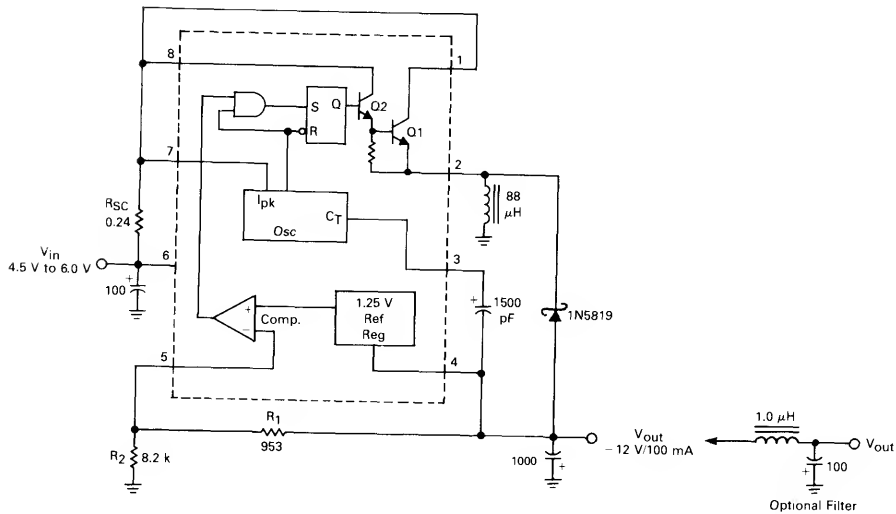


10B — EXTERNAL PNP SATURATED SWITCH



MC34063A, MC35063A, MC33063A

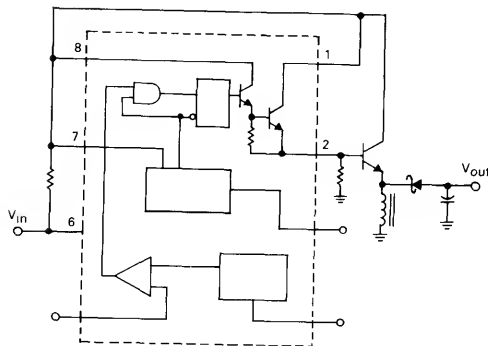
FIGURE 11 — VOLTAGE INVERTING CONVERTER



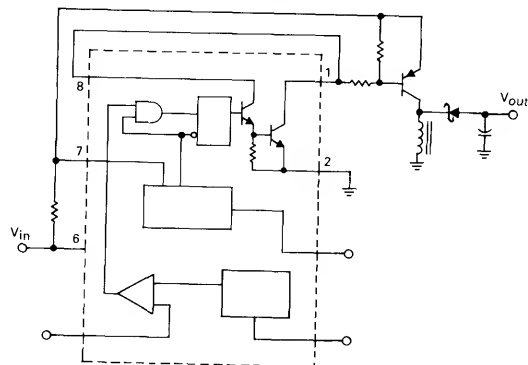
Test	Conditions	Results
Line Regulation	$V_{in} = 4.5 \text{ V to } 6.0 \text{ V}, I_O = 100 \text{ mA}$	$3.0 \text{ mV} = \pm 0.012\%$
Load Regulation	$V_{in} = 5.0 \text{ V}, I_O = 10 \text{ to } 100 \text{ mA}$	$0.022 \text{ V} = \pm 0.09\%$
Output Ripple	$V_{in} = 5.0 \text{ V}, I_O = 100 \text{ mA}$	500 mVp-p
Short Circuit Current	$V_{in} = 5.0 \text{ V}, R_L = 0.1 \Omega$	910 mA
Efficiency	$V_{in} = 5.0 \text{ V}, I_O = 100 \text{ mA}$	64.5%
Output Ripple With Optional Filter	$V_{in} = 5.0 \text{ V}, I_O = 100 \text{ mA}$	70 mVp-p

FIGURE 12 — EXTERNAL CURRENT BOOST CONNECTIONS
FOR I_C PEAK GREATER THAN 1.5 A

12A — EXTERNAL NPN SWITCH

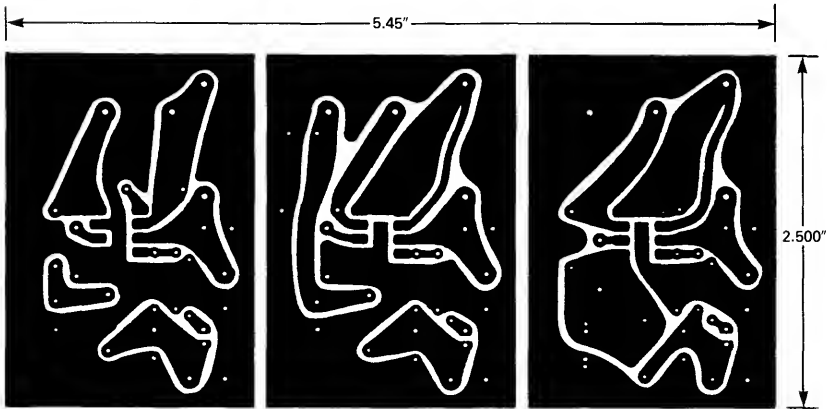


12B — EXTERNAL PNP SATURATED SWITCH

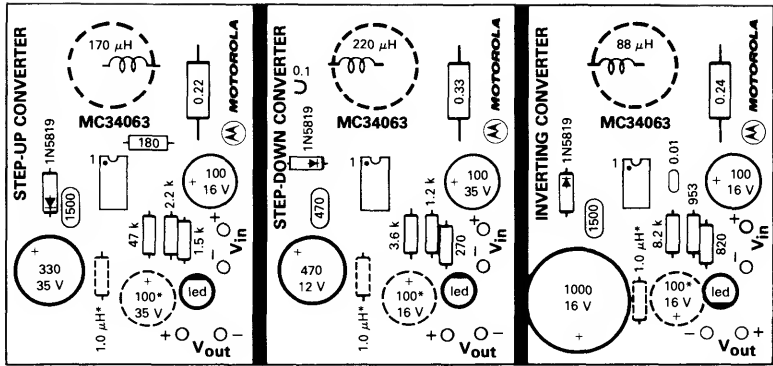


MC34063A, MC35063A, MC33063A

FIGURE 13 — PRINTED CIRCUIT BOARD AND COMPONENT LAYOUT
(CIRCUITS OF FIGURES 7, 9, 11)



(Top view, copper foil as seen through the board from the component side)



Top View, Component Side

*Optional Filter.

INDUCTOR DATA

Converter	Inductance (μH)	Turns/Wire
Step-Up	170	38 Turns of #22 AWG
Step-Down	220	48 Turns of #22 AWG
Voltage-Inverting	88	28 Turns of #22 AWG

All inductors are wound on Magnetics Inc. 55117 toroidal core.

FIGURE 14 — DESIGN FORMULA TABLE

Calculation	Step-Up	Step-Down	Voltage-Inverting
t_{on}/t_{off}	$\frac{V_{out} + V_F - V_{in(min)}}{V_{in(min)} - V_{sat}}$	$\frac{V_{out} + V_F}{V_{in(min)} - V_{sat} - V_{out}}$	$\frac{ V_{out} + V_F}{V_{in} - V_{sat}}$
$(t_{on} + t_{off})_{max}$	$\frac{1}{f_{min}}$	$\frac{1}{f_{min}}$	$\frac{1}{f_{min}}$
C_T	$4.8 \times 10^{-5} t_{on}$	$4.8 \times 10^{-5} t_{on}$	$4.8 \times 10^{-5} t_{on}$
$I_{pk(switch)}$	$2I_{out(max)} \left(\frac{t_{on}}{t_{off}} + 1 \right)$	$2I_{out(max)}$	$2I_{out(max)} \left(\frac{t_{on}}{t_{off}} + 1 \right)$
RSC	$0.3/I_{pk(switch)}$	$0.3/I_{pk(switch)}$	$0.3/I_{pk(switch)}$
$L_{(min)}$	$\left(\frac{V_{in(min)} - V_{sat}}{I_{pk(switch)}} \right) t_{on(max)}$	$\left(\frac{V_{in(min)} - V_{sat} - V_{out}}{I_{pk(switch)}} \right) t_{on(max)}$	$\left(\frac{V_{in(min)} - V_{sat}}{I_{pk(switch)}} \right) t_{on(max)}$
C_O	$\approx \frac{I_{out} t_{on}}{V_{ripple(p-p)}}$	$\frac{I_{pk(switch)}(t_{on} + t_{off})}{8 V_{ripple(p-p)}}$	$\approx \frac{I_{out} t_{on}}{V_{ripple(p-p)}}$

V_{sat} = Saturation voltage of the output switch.
 V_F = Forward voltage drop of the output rectifier.

The following power supply characteristics must be chosen:

V_{in} — Nominal input voltage.

V_{out} — Desired output voltage, $|V_{out}| = 1.25 \left(1 + \frac{R_2}{R_1} \right)$

I_{out} — Desired output current.

f_{min} — Minimum desired output switching frequency at the selected values of V_{in} and I_O .

$V_{ripple(p-p)}$ — Desired peak-to-peak output ripple voltage. In practice, the calculated capacitor value will need to be increased due to its equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly affect the line and load regulation.

NOTE:

For further information refer to Application Note AN920 Rev. 2

Advance Information

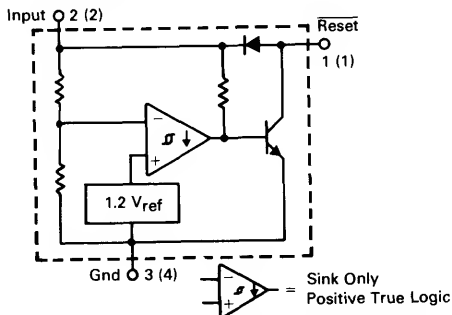
UNDervoltage SENSING CIRCUIT

The MC34064 is an undervoltage sensing circuit specifically designed for use as a reset controller in microprocessor-based systems. It offers the designer an economical solution for low voltage detection with a single external resistor. The MC34064 features a trimmed-in-package bandgap reference, and a comparator with precise thresholds and built-in hysteresis to prevent erratic reset operation. The open collector reset output is capable of sinking in excess of 10 mA, and operation is guaranteed down to 1.0 volt input with low standby current. These devices are packaged in 3-pin TO-226AA and 8-pin surface mount packages.

Applications include direct monitoring of the 5.0 Volt MPU/logic power supply used in appliance, automotive, consumer and industrial equipment.

- Trimmed-In-Package Temperature Compensated Reference
- Comparator Threshold of 4.6 V at 25°C
- Precise Comparator Thresholds Guaranteed Over Temperature
- Comparator Hysteresis Prevents Erratic Reset
- Reset Output Capable of Sinking in Excess of 10 mA
- Internal Clamp Diode for Discharging Delay Capacitor
- Guaranteed Reset Operation with 1.0 Volt Input
- Low Standby Current
- Economical TO-226AA and SO-8 Surface Mount Packages

REPRESENTATIVE BLOCK DIAGRAM



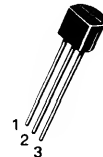
Pin numbers adjacent to terminals are for the 3-pin TO-226AA package.
 Pin numbers in parenthesis are for the D suffix SO-8 package.

MC34064
MC33064

UNDervoltage SENSING CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT

P SUFFIX
PLASTIC PACKAGE
CASE 29
(TO-226AA)



PIN 1. RESET
2. INPUT
3. GROUND

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)



PIN 1. RESET
2. INPUT
3. N.C.
4. GROUND
5. N.C.
6. N.C.
7. N.C.
8. N.C.

ORDERING INFORMATION

Device	Temperature Range	Package
MC34064D-5	0°C to +70°C	Plastic SO-8
MC34064P-5		Plastic TO-226AA
MC33064D-5	-40°C to +85°C	Plastic SO-8
MC33064P-5		Plastic TO-226AA

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Input Supply Voltage	V_{in}	-1.0 to 10	V
Reset Output Voltage	V_O	10	V
Reset Output Sink Current (Note 1)	I_{Sink}	Internally Limited	mA
Clamp Diode Forward Current, Pin 1 to 2 (Note 1)	I_F	100	mA
Power Dissipation and Thermal Characteristics P Suffix, Plastic Package Maximum Power Dissipation (α $T_A = 25^\circ\text{C}$) Thermal Resistance, Junction to Air	P_D $R_{\theta JA}$	625 200	mW $^\circ\text{C/W}$
D Suffix, Plastic Package Maximum Power Dissipation (α $T_A = 25^\circ\text{C}$) Thermal Resistance Junction to Air	P_D $R_{\theta JA}$	625 200	mW $^\circ\text{C/W}$
Operating Junction Temperature	T_J	+150	$^\circ\text{C}$
Operating Ambient Temperature MC34064 MC33064	T_A	0 to +70 -40 to +85	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS For typical values $T_A = 25^\circ\text{C}$, for min/max values T_A is the operating ambient temperature range that applies (Notes 2 and 3).

Characteristic	Symbol	Min	Typ	Max	Unit
COMPARATOR					
Threshold Voltage					V
High State Output (V_{in} Increasing)	V_{IH}	4.5	4.61	4.7	
Low State Output (V_{in} Decreasing)	V_{IL}	4.5	4.59	4.7	
Hysteresis	V_H	0.01	0.02	0.05	

RESET OUTPUT

Output Sink Saturation ($V_{in} = 4.0\text{ V}$, $I_{Sink} = 8.0\text{ mA}$) ($V_{in} = 4.0\text{ V}$, $I_{Sink} = 2.0\text{ mA}$) ($V_{in} = 1.0\text{ V}$, $I_{Sink} = 0.1\text{ mA}$)	V_{OL}	— — —	0.46 0.15 —	1.0 0.4 0.1	V
Output Sink Current (V_{in} , Reset = 4.0 V)	I_{Sink}	10	27	60	mA
Output Off-State Leakage (V_{in} , Reset = 5.0 V)	I_{OH}	—	0.02	0.5	μA
Clamp Diode Forward Voltage, Pin 1 to 2 ($I_F = 10\text{ mA}$)	V_F	0.6	0.9	1.2	V

TOTAL DEVICE

Operating Input Voltage Range	V_{in}	1.0 to 6.5	—	—	V
Quiescent Input Current ($V_{in} = 5.0\text{ V}$)	I_{in}	—	390	500	μA

NOTES:

- Maximum package power dissipation limits must be observed.
- Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
- $T_{low} = 0^\circ\text{C}$ for MC34064
 $T_{high} = +70^\circ\text{C}$ for MC34064
 $= -40^\circ\text{C}$ for MC33064
 $= +85^\circ\text{C}$ for MC33064

FIGURE 1 — RESET OUTPUT VOLTAGE versus INPUT VOLTAGE

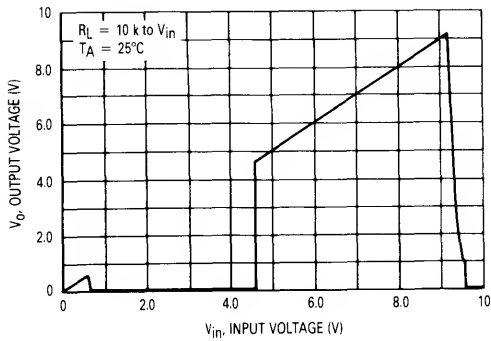


FIGURE 2 — RESET OUTPUT VOLTAGE versus INPUT VOLTAGE

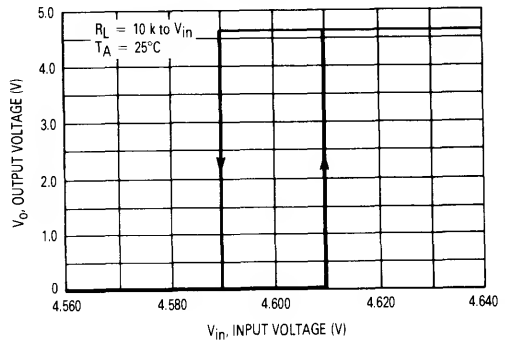


FIGURE 3 — COMPARATOR THRESHOLD VOLTAGE versus TEMPERATURE

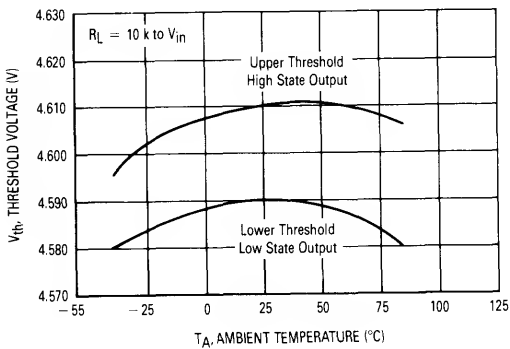


FIGURE 4 — INPUT CURRENT versus INPUT VOLTAGE

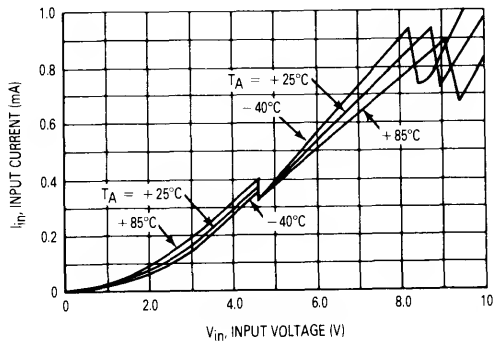


FIGURE 5 — RESET OUTPUT SATURATION versus SINK CURRENT

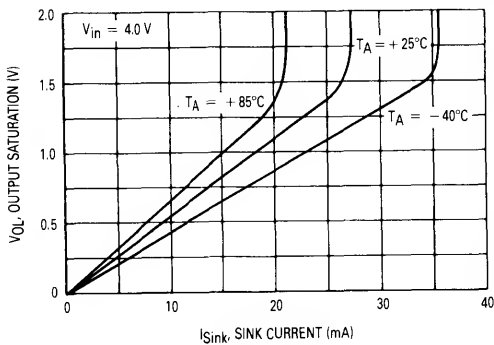


FIGURE 6 — RESET DELAY TIME

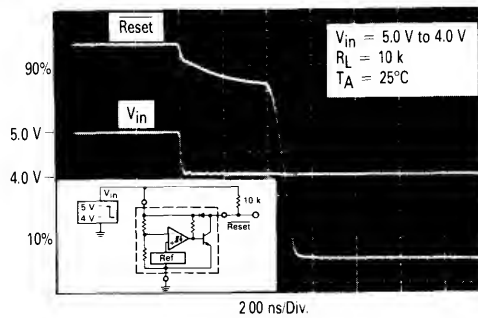


FIGURE 7 — CLAMP DIODE FORWARD CURRENT
versus VOLTAGE

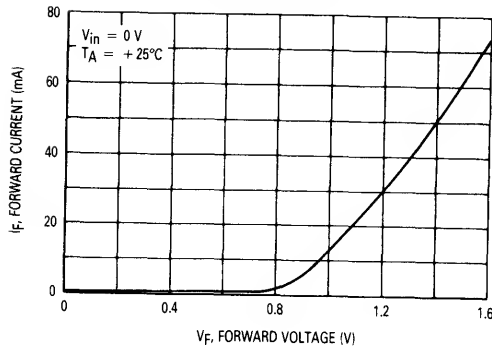


FIGURE 8 — LOW VOLTAGE MICROPROCESSOR RESET

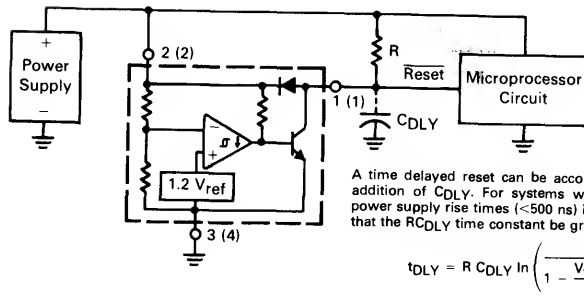
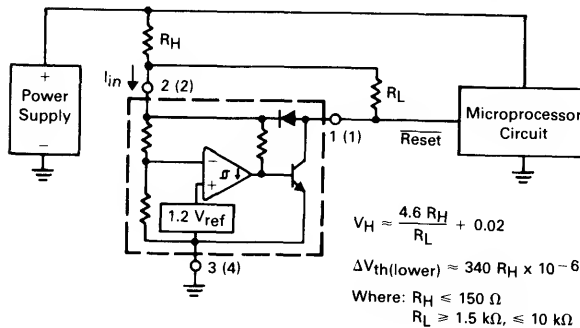


FIGURE 9 — LOW VOLTAGE MICROPROCESSOR RESET WITH ADDITIONAL HYSTERESIS



Comparator hysteresis can be increased with the addition of resistor R_H . The hysteresis equation has been simplified and does not account for the change of input current I_{in} as V_{CC} crosses the comparator threshold (Figure 4). An increase of the lower threshold $\Delta V_{th}(\text{lower})$ will be observed due to I_{in} which is typically $340\text{ }\mu\text{A}$ at 4.59 V . The equations are accurate to $\pm 10\%$ with R_H less than $150\text{ }\Omega$ and R_L between $1.5\text{ k}\Omega$ and $10\text{ k}\Omega$.

TEST DATA				
V_H (mV)	ΔV_{th} (mV)	R_H (Ω)	R_L ($\text{k}\Omega$)	
20	0	0	0	
51	3.4	10	1.5	
40	6.8	20	4.7	
81	6.8	20	1.5	
71	10	30	2.7	
112	10	30	1.5	
100	16	47	2.7	
164	16	47	1.5	
190	34	100	2.7	
327	34	100	1.5	
276	51	150	2.7	
480	51	150	1.5	

FIGURE 10 — VOLTAGE MONITOR

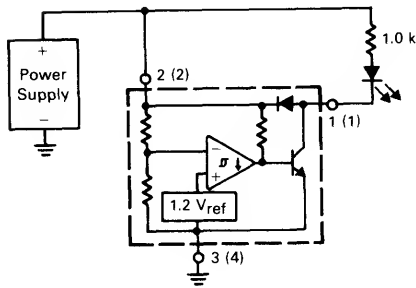


FIGURE 11 — SOLAR POWERED BATTERY CHARGER

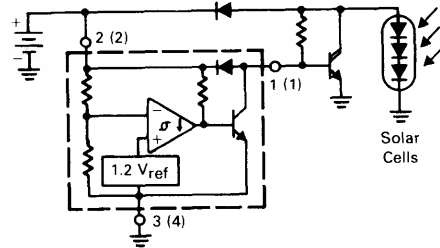
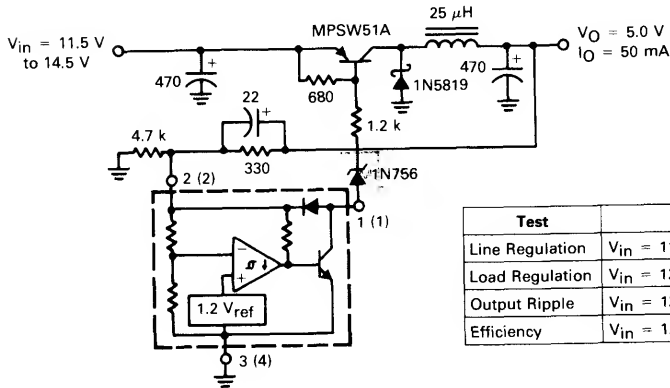
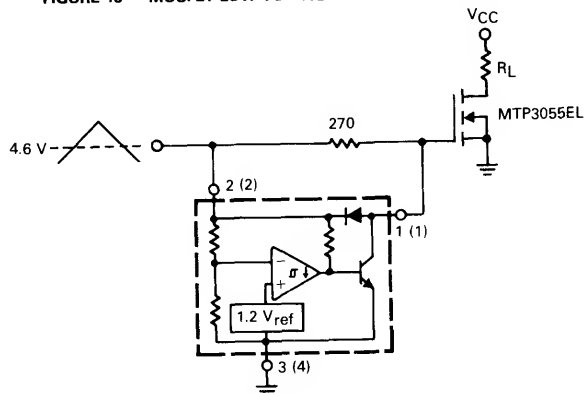


FIGURE 12 — LOW POWER SWITCHING REGULATOR



Test	Conditions	Results
Line Regulation	$V_{in} = 11.5 \text{ V to } 14.5 \text{ V}, I_O = 50 \text{ mA}$	35 mV
Load Regulation	$V_{in} = 12.6 \text{ V}, I_O = 0 \text{ mA to } 50 \text{ mA}$	12 mV
Output Ripple	$V_{in} = 12.6 \text{ V}, I_O = 50 \text{ mA}$	60 mV _{p-p}
Efficiency	$V_{in} = 12.6 \text{ V}, I_O = 50 \text{ mA}$	77%

FIGURE 13 — MOSFET LOW VOLTAGE GATE DRIVE PROTECTION



Overheating of the logic level power MOSFET due to insufficient gate voltage can be prevented with the above circuit. When the input signal is below the 4.6 volt threshold of the MC34064, its output grounds the gate of the L2 MOSFET.

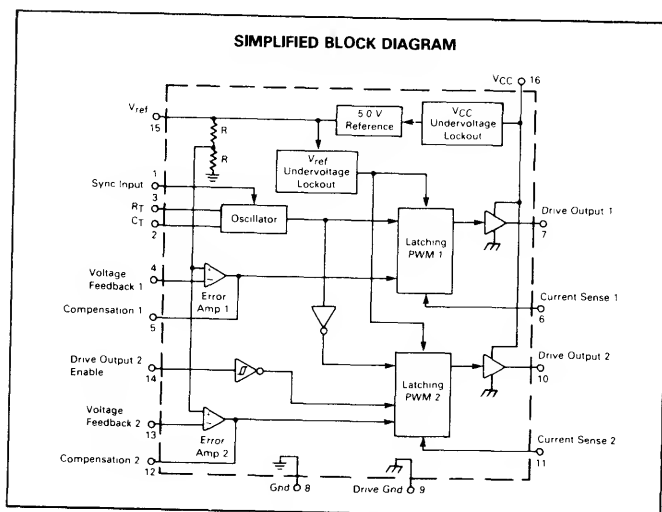
**HIGH PERFORMANCE DUAL CHANNEL
CURRENT MODE CONTROLLER**

The MC34065 series are high performance, fixed frequency, dual current mode controllers. They are specifically designed for Off-Line and DC-to-DC converter applications offering the designer a cost effective solution with minimal external components. These integrated circuits feature a unique oscillator for precise duty cycle limit and frequency control, a temperature compensated reference, two high gain error amplifiers, two current sensing comparators, drive output 2 enable pin, and two high current totem pole outputs ideally suited for driving power MOSFETs.

Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle-by-cycle current limiting, and a latch for single pulse metering of each output.

These devices are available in dual-in-line and surface mount packages.

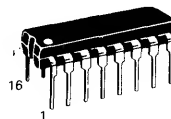
- Unique Oscillator for Precise Duty Cycle Limit and Frequency Control
- Current Mode Operation to 500 kHz
- Automatic Feed Forward Compensation
- Separate Latching PWMs for Cycle-By-Cycle Current Limiting
- Internally Trimmed Reference with Undervoltage Lockout
- Drive Output 2 Enable Pin
- Two High Current Totem Pole Outputs
- Input Undervoltage Lockout with Hysteresis
- Low Start-Up and Operating Current
- Direct Interface with Motorola SENSEFET Products



MC34065
MC33065

**HIGH PERFORMANCE
DUAL CHANNEL
CURRENT MODE CONTROLLER**

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**

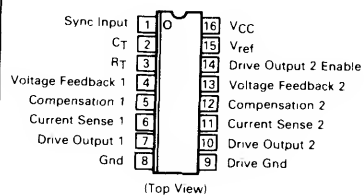


P SUFFIX
PLASTIC PACKAGE
CASE 648



DW SUFFIX
PLASTIC PACKAGE
CASE 751G
(SO-16L)

PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
MC34065DW	0° to +70°C	SO-16L
MC34065P		Plastic DIP
MC33065DW	-40° to +85°C	SO-16L
MC33065P		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Total Power Supply and Zener Current	$(I_{CC} + I_Z)$	50	mA
Output Current, Source or Sink (Note 1)	I_O	1.0	A
Output Energy (Capacitive Load per Cycle)	W	5.0	μ J
Current Sense, Enable, and Voltage Feedback Inputs	V_{in}	-0.3 to +5.5	V
Sync Input — High State (Voltage)	V_{IH}	5.5	V
— Low State (Reverse Current)	I_{IL}	-5.0	mA
Error Amp Output Sink Current	I_O	10	mA
Power Dissipation and Thermal Characteristics			
DW Suffix Package SO-16 Case 751G-01			
Maximum Power Dissipation ($\theta_A = 25^\circ\text{C}$)	P_D	862	mW
Thermal Resistance Junction to Air	$R_{\theta JA}$	145	$^\circ\text{C/W}$
P Suffix Package Case 648-06			
Maximum Power Dissipation ($\theta_A = 25^\circ\text{C}$)	P_D	1.25	W
Thermal Resistance Junction to Air	$R_{\theta JA}$	100	$^\circ\text{C/W}$
Operating Junction Temperature	T_J	+150	$^\circ\text{C}$
Operating Ambient Temperature MC34065	T_A	0 to +70	$^\circ\text{C}$
MC33065		-40 to +85	
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($V_{CC} = 15\text{ V}$ [Note 2], $R_T = 8.2\text{ k}\Omega$, $C_T = 3.3\text{ nF}$, for typical values $T_A = 25^\circ\text{C}$, for min/max values T_A is the operating ambient temperature range that applies [Note 3].)

Characteristic	Symbol	Min	Typ	Max	Unit
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REFERENCE SECTION

Reference Output Voltage ($I_O = 1.0\text{ mA}$, $T_J = 25^\circ\text{C}$)	V_{ref}	4.9	5.0	5.1	V
Line Regulation ($V_{CC} = 11\text{ V to }15\text{ V}$)	Reg_{line}	—	2.0	20	mV
Load Regulation ($I_O = 1.0\text{ mA to }10\text{ mA}$)	Reg_{load}	—	3.0	25	mV
Total Output Variation over Line, Load, and Temperature	V_{ref}	4.85	—	5.15	V
Output Short Circuit Current	I_{SC}	30	100	—	mA

OSCILLATOR and PWM SECTIONS

Total Frequency Variation over Line and Temperature ($V_{CC} = 11\text{ V to }15\text{ V}$, $T_A = T_{low}$ to T_{high})	MC34065 MC33065	f_{OSC}	46.5 45	49 49	51.5 53	kHz
Frequency Change with Voltage ($V_{CC} = 11\text{ V to }15\text{ V}$)		$\Delta f_{OSC}/\Delta V$	—	0.2	1.0	%
Duty Cycle at each Output — Maximum		DC_{max}	46	49.5	52	%
— Minimum		DC_{min}	—	—	0	
Sync Input Current — High State ($V_{in} = 2.4\text{ V}$)		I_{IH}	—	170	250	μ A
— Low State ($V_{in} = 0.8\text{ V}$)		I_{IL}	—	80	160	

ERROR AMPLIFIERS

Voltage Feedback Input ($V_O = 2.5\text{ V}$)		V_{FB}	2.42	2.5	2.58	V
Input Bias Current ($V_{FB} = 5.0\text{ V}$)		I_{IB}	—	-0.1	-1.0	μ A
Open-Loop Voltage Gain ($V_O = 2.0$ to 4.0 V)		A_{VOL}	65	100	—	dB
Unity Gain Bandwidth ($T_J = 25^\circ\text{C}$)		BW	0.7	1.0	—	MHz
Power Supply Rejection Ratio ($V_{CC} = 11\text{ V to }15\text{ V}$)		PSRR	60	90	—	dB
Output Current — Source ($V_O = 3.0\text{ V}$, $V_{FB} = 2.3\text{ V}$)		I_{Source}	-0.45	-1.0	—	mA
— Sink ($V_O = 1.2\text{ V}$, $V_{FB} = 2.7\text{ V}$)		I_{Sink}	2.0	12	—	
Output Voltage Swing — High State ($R_L = 15\text{ k}$ to ground, $V_{FB} = 2.3\text{ V}$)		V_{OH}	5.0	6.2	—	V
— Low State ($R_L = 15\text{ k}$ to V_{ref} , $V_{FB} = 2.7\text{ V}$)		V_{OL}	—	0.8	1.1	

- Notes: 1. Maximum package power dissipation limits must be observed.
 2. Adjust V_{CC} above the Start-Up threshold before setting to 15 V.
 3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
 $T_{low} = 0^\circ\text{C}$ for the MC34065 $T_{high} = +70^\circ\text{C}$ for MC34065
 $T_{low} = -40^\circ\text{C}$ for MC33065 $T_{high} = +85^\circ\text{C}$ for MC33065

MC34065 MC33065

ELECTRICAL CHARACTERISTICS ($V_{CC} = 15\text{ V}$ [Note 2], $R_T = 8.2\text{ k}\Omega$, $C_T = 3.3\text{ nF}$, for typical values $T_A = 25^\circ\text{C}$, for min/max values T_A is the operating ambient temperature range that applies [Note 3].)

Characteristic	Symbol	Min	Typ	Max	Unit
CURRENT SENSE SECTION					
Current Sense Input Voltage Gain (Notes 4 and 5)	A_V	2.75	3.0	3.25	V/V
Maximum Current Sense Input Threshold (Note 4)	V_{th}	430	480	530	mV
Input Bias Current	I_{IB}	—	-2.0	-10	μA
Propagation Delay (Current Sense Input to Output)	$t_{PLN(IN/OUT)}$	—	150	300	ns
DRIVE OUTPUT 2 ENABLE PIN					
Enable Pin Voltage					V
High State (Output 2 Enabled)	V_{IH}	3.5	—	V_{ref}	
Low State (Output 2 Disabled)	V_{IL}	0	—	1.5	
Low State Input Current ($V_{IL} = 0\text{ V}$)	I_{IB}	100	250	400	μA
DRIVE OUTPUTS					
Output Voltage					V
Low State ($I_{Sink} = 20\text{ mA}$)	V_{OL}	—	0.1	0.4	
($I_{Sink} = 200\text{ mA}$)		—	0.8	2.5	
High State ($I_{Source} = 20\text{ mA}$)	V_{OH}	13	13.5	—	
($I_{Source} = 200\text{ mA}$)		12	13.4	—	
Output Voltage with UVLO Activated ($V_{CC} = 6.0\text{ V}$, $I_{Sink} = 1.0\text{ mA}$)	$V_{OL(UVLO)}$	—	0.1	1.1	V
Output Voltage Rise Time ($C_L = 1.0\text{ nF}$)	t_r	—	28	150	ns
Output Voltage Fall Time ($C_L = 1.0\text{ nF}$)	t_f	—	25	150	ns
UNDERVOLTAGE LOCKOUT SECTION					
Start-Up Threshold	V_{th}	13	14	15	V
Minimum Operating Voltage After Turn-On	$V_{CC(min)}$	9.0	10	11	V
TOTAL DEVICE					
Power Supply Current	I_{CC}	—	0.6	1.0	mA
Start-Up ($V_{CC} = 12\text{ V}$)		—	20	25	
Operating (Note 2)					
Power Supply Zener Voltage ($I_{CC} = 30\text{ mA}$)	V_Z	15.5	17	19	V

- Notes: 1. Maximum package power dissipation limits must be observed.
 2. Adjust V_{CC} above the Start-Up threshold before setting to 15 V.
 3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
 $T_{low} = 0^\circ\text{C}$ for the MC34065 $T_{high} = +70^\circ\text{C}$ for MC34065
 $T_{low} = -40^\circ\text{C}$ for MC33065 $T_{high} = +85^\circ\text{C}$ for MC33065
 4. This parameter is measured at the latch trip point with $V_{fb} = 0\text{ V}$.
 5. Comparator gain is defined as $A_V = \frac{\Delta V_{Compensation}}{\Delta V_{Current Sense}}$

FIGURE 1 — TIMING RESISTOR versus OSCILLATOR FREQUENCY

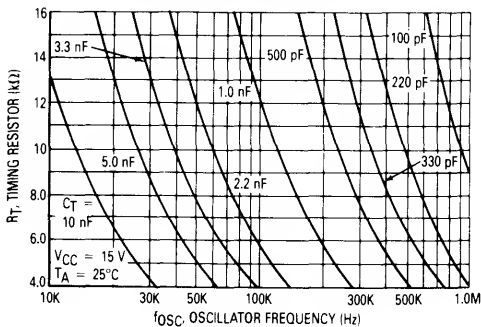


FIGURE 2 — MAXIMUM OUTPUT DUTY CYCLE versus OSCILLATOR FREQUENCY

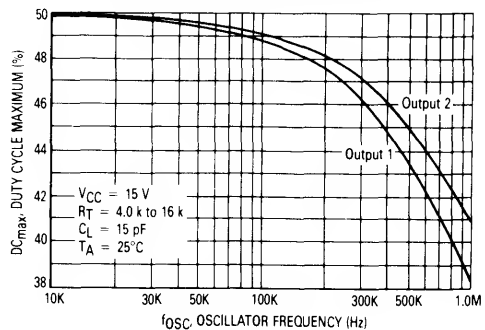


FIGURE 3 — ERROR AMP SMALL-SIGNAL
TRANSIENT RESPONSE

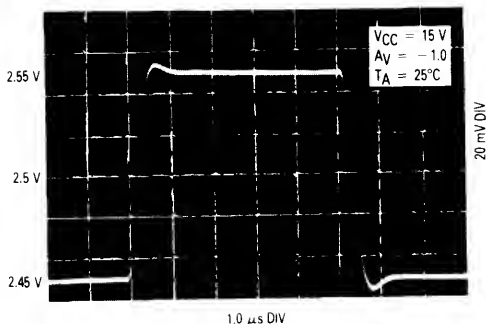


FIGURE 4 — ERROR AMP LARGE-SIGNAL
TRANSIENT RESPONSE

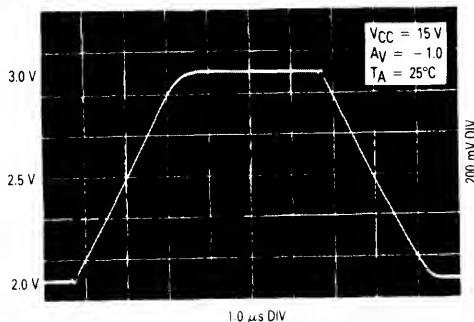


FIGURE 5 — ERROR AMP OPEN-LOOP GAIN AND
PHASE versus FREQUENCY

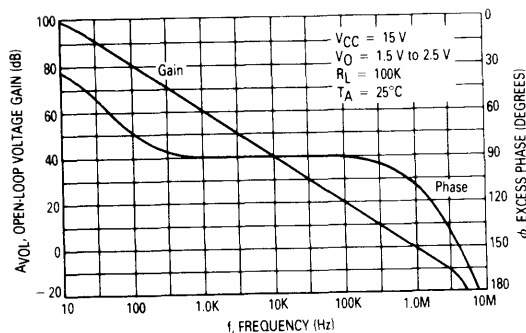


FIGURE 6 — CURRENT SENSE INPUT THRESHOLD
versus ERROR AMP OUTPUT VOLTAGE

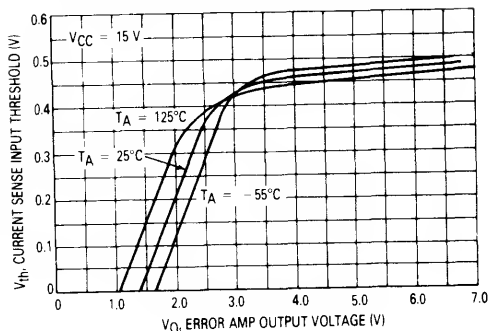


FIGURE 7 — REFERENCE VOLTAGE CHANGE
versus SOURCE CURRENT

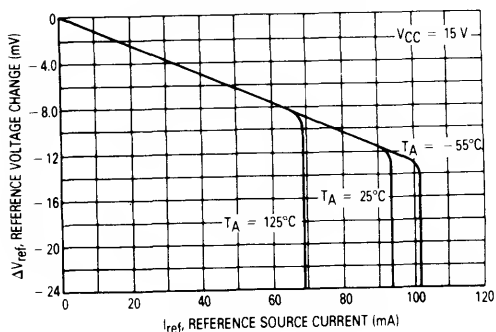


FIGURE 8 — REFERENCE SHORT CIRCUIT CURRENT
versus TEMPERATURE

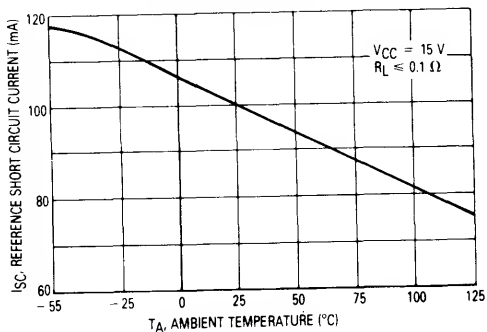


FIGURE 9 — REFERENCE LOAD REGULATION

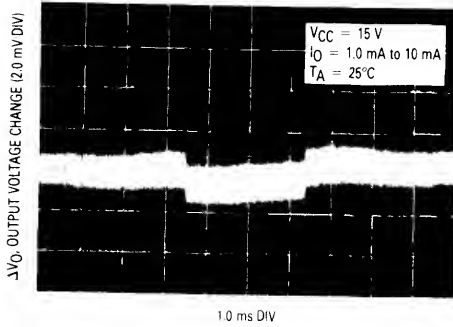


FIGURE 10 — REFERENCE LINE REGULATION

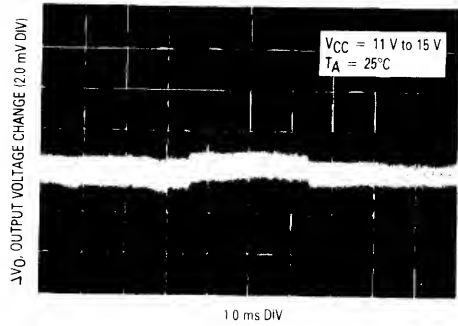


FIGURE 11 — OUTPUT SATURATION VOLTAGE versus LOAD CURRENT

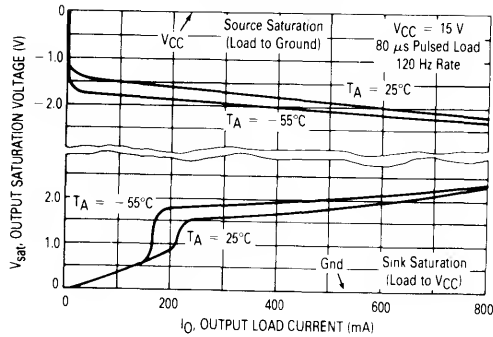


FIGURE 12 — OUTPUT WAVEFORM

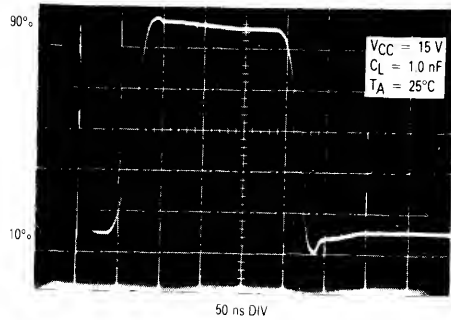


FIGURE 13 — OUTPUT CROSS-CONDUCTION

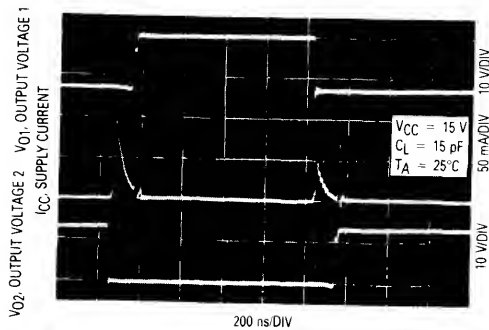
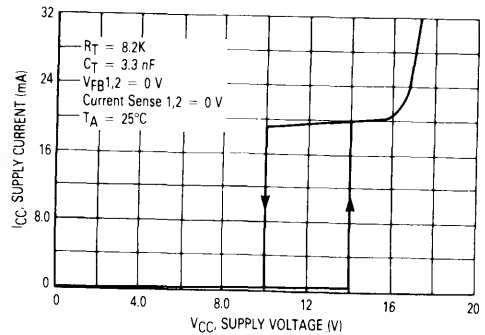


FIGURE 14 — SUPPLY CURRENT versus SUPPLY VOLTAGE



OPERATING DESCRIPTION

The MC34065 series are high performance, fixed frequency, dual channel current mode controllers specifically designed for Off-Line and DC-to-DC converter applications. These devices offer the designer a cost effective solution with minimal external components where independent regulation of two power converters is required. The Representative Block Diagram is shown in Figure 15. Each channel contains a high gain error amplifier, current sensing comparator, pulse width modulator latch, and totem pole output driver. The oscillator, reference regulator, and undervoltage lock-out circuits are common to both channels.

Oscillator

The unique oscillator configuration employed features precise frequency and duty cycle control. The frequency is programmed by the values selected for the timing components R_T and C_T . Capacitor C_T is charged and discharged by an equal magnitude internal current source and sink, generating a symmetrical 50 percent duty cycle waveform at Pin 2. The oscillator peak and valley thresholds are 3.5 V and 1.6 V respectively. The source/sink current magnitude is controlled by resistor R_T . For proper operation over temperature it must be in the range of 4.0 k Ω to 16 k Ω as shown in Figure 1.

As C_T charges and discharges, an internal blanking pulse is generated that alternately drives the center inputs of the upper and lower NOR gates high. This, in conjunction with a precise amount of delay time introduced into each channel, produces well defined non-overlapping output duty cycles. Output 2 is enabled while C_T is charging, and Output 1 is enabled during the discharge. Figure 2 shows the Maximum Output Duty Cycle versus Oscillator Frequency. Note that even at 500 kHz, each output is capable of approximately 44% on-time, making this controller suitable for high frequency power conversion applications.

In many noise sensitive applications it may be desirable to frequency-lock the converter to an external system clock. This can be accomplished by applying a clock signal as shown in Figure 17. For reliable locking, the free-running oscillator frequency should be set about 10% less than the clock frequency. Referring to the timing diagram shown in Figure 16, the rising edge of the clock signal applied to the Sync input, terminates charging of C_T and Drive Output 2 conduction. By tailoring the clock waveform symmetry, accurate duty cycle clamping of either output can be achieved. A circuit method for this, and multi unit synchronization, is shown in Figure 18.

Error Amplifier

Each channel contains a fully-compensated Error Amplifier with access to the inverting input and output. The amplifier features a typical dc voltage gain of 100 dB, and a unity gain bandwidth of 1.0 MHz with 71 degrees of phase margin (Figure 5). The non-inverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input through a resistor divider. The maximum input bias current is $-1.0 \mu\text{A}$ which will cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp output (Pin 5, 12) is provided for external loop compensation. The output voltage is offset by two diode drops ($\approx 1.4 \text{ V}$) and divided by three before it connects to the inverting input of the Current Sense Comparator. This guarantees that no pulses appear at the Drive Output (Pin 7, 10) when the error amplifier output is at its lowest state (V_{OL}). This occurs when the power supply is operating and the load is removed, or at the beginning of a soft-start interval (Figures 20, 21).

The minimum allowable Error Amp feedback resistance is limited by the amplifier's source current (0.5 mA) and the output voltage (V_{OH}) required to reach the comparator's 0.5 V clamp level with the inverting input at ground. This condition happens during initial system startup or when the sensed output is shorted:

$$R_f(\text{MIN}) = \frac{3.0 (0.5 \text{ V}) + 1.4 \text{ V}}{0.5 \text{ mA}} = 5800 \Omega$$

Current Sense Comparator and PWM Latch

The MC34065 operates as a current mode controller, whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier output. Thus the error signal controls the peak inductor current on a cycle-by-cycle basis. The Current Sense Comparator-PWM Latch configuration used ensures that only a single pulse appears at the Drive Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting a ground-referenced sense resistor R_S in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input (Pin 6, 11) and compared to a level derived from the Error Amp output. The peak inductor current under normal operating conditions is controlled by the voltage at Pin 5, 12 where:

$$I_{pk} = \frac{V(\text{Pin } 5, 12) - 1.4 \text{ V}}{3 R_S}$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the Current Sense Comparator threshold will be internally clamped to 0.5 V. Therefore the maximum peak switch current is:

$$I_{pk}(\text{max}) = \frac{0.5 \text{ V}}{R_S}$$

When designing a high power switching regulator it may be desirable to reduce the internal clamp voltage in order to keep the power dissipation of R_S to a reasonable level. A simple method to adjust this voltage is shown in Figure 19. The two external diodes are used to compensate the internal diodes, yielding a constant clamp voltage over temperature. Erratic operation due to noise pickup can result if there is an excessive reduction of the $I_{pk}(\text{max})$ clamp voltage.

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Current Sense input with a time constant that approximates the spike duration will usually eliminate the instability; refer to Figure 24.

FIGURE 15 — REPRESENTATIVE BLOCK DIAGRAM

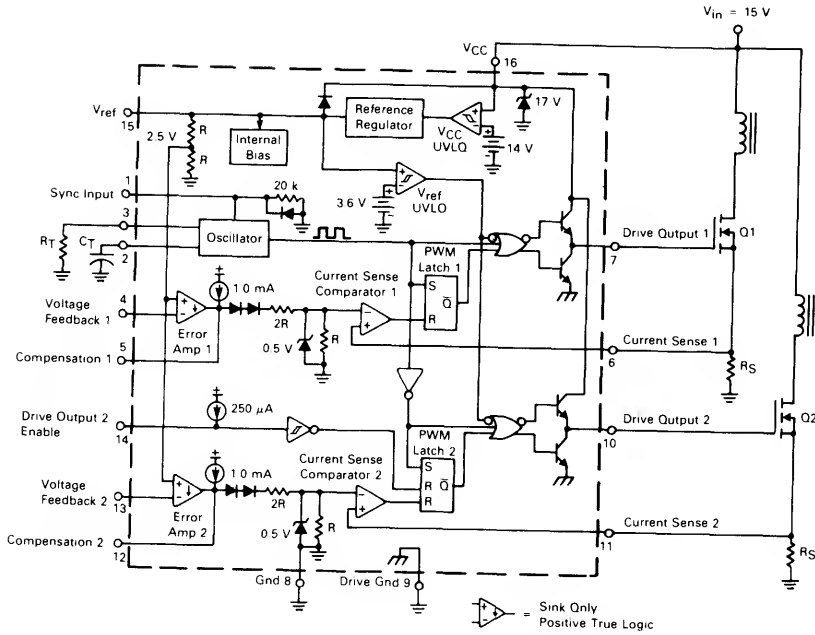
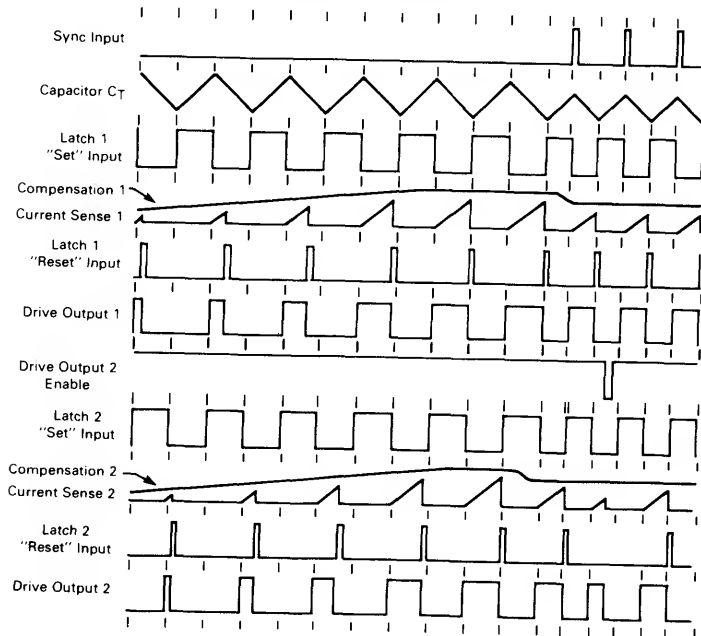


FIGURE 16 — TIMING DIAGRAM



Undervoltage Lockout

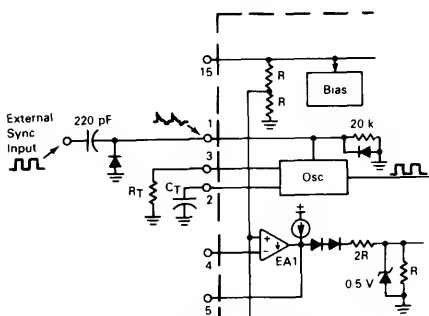
Two Undervoltage Lockout comparators have been incorporated to guarantee that the IC is fully functional before the output stages are enabled. The positive power supply terminal (V_{CC}) and the reference output (V_{ref}) are each monitored by separate comparators. Each has built-in hysteresis to prevent erratic output behavior as their respective thresholds are crossed. The V_{CC} comparator upper and lower thresholds are 14 V and 10 V respectively. The hysteresis and low start-up current makes these devices ideally suited to off-line converter applications where efficient bootstrap start-up techniques are required (Figure 28). The V_{ref} comparator disables the Drive Outputs until the internal circuitry is functional. This comparator has upper and lower thresholds of 3.6 V and 3.4 V. A 17 V zener is connected as a shunt regulator from V_{CC} to ground. Its purpose is to protect the IC and power MOSFET gate from excessive voltage that can occur during system start-up. The guaranteed minimum operating voltage after turn-on is 11 V.

Drive Outputs and Drive Ground

Each channel contains a single totem-pole output stage that is specifically designed for direct drive of power MOSFET's. The Drive Outputs are capable of up to ± 1.0 A peak current and have a typical rise and fall times of 28 ns with a 1.0 nF load. Internal circuitry has been added to keep the outputs in a sinking mode whenever an Undervoltage Lockout is active. This characteristic eliminates the need for an external pull-down resistor. Cross-conduction current in the totem-pole output stage has been minimized for high speed operation, as shown in Figure 13. The average added power due to cross-conduction with $V_{CC} = 15$ V is only 60 mW at 500 kHz.

Although the Drive Outputs were optimized for MOSFETs, they can easily supply the negative base current required by bipolar NPN transistors for enhanced turn-off (Figure 25). The outputs do not contain internal current limiting, therefore an external series resistor may be required to prevent the peak output current from exceeding the ± 1.0 A maximum rating. The sink saturation (V_{OL}) is less than 0.4 V at 100 mA.

FIGURE 17 — EXTERNAL CLOCK SYNCHRONIZATION



The external diode clamp is required if the negative Sync current is greater than -5.0 mA.

A separate Drive Ground pin is provided and, with proper implementation, will significantly reduce the level of switching transient noise imposed on the control circuitry. This becomes particularly useful when reducing the $I_{pk(max)}$ clamp level. Figure 23 shows the proper ground connections required for current sensing power MOSFET applications.

Drive Output 2 Enable Pin

This input is used to enable Drive Output 2. Drive Output 1 can be used to control circuitry that must run continuously such as volatile memory and the system clock, or a remote controlled receiver, while Drive Output 2 controls the high power circuitry that is occasionally turned off.

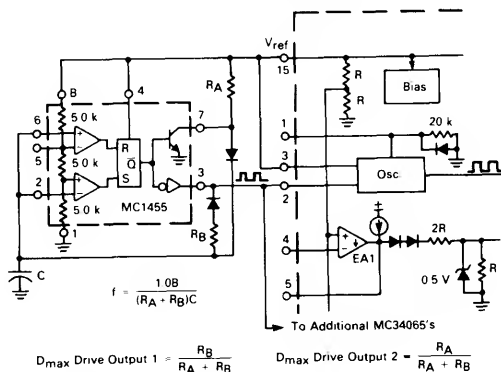
Reference

The 5.0 V bandgap reference is trimmed to $\pm 2.0\%$ tolerance at $T_J = 25^\circ\text{C}$. The reference has short circuit protection and is capable of providing in excess of 30 mA for powering any additional control system circuitry.

Design Considerations

Do not attempt to construct the converter on wire-wrap or plug-in prototype boards. High frequency circuit layout techniques are imperative to prevent pulse-width jitter. This is usually caused by excessive noise pick-up imposed on the Current Sense or Voltage Feedback inputs. Noise immunity can be improved by lowering circuit impedances at these points. The printed circuit layout should contain a ground plane with low current signal and high current switch and output grounds returning on separate paths back to the input filter capacitor. Ceramic bypass capacitors (0.1 μF) connected directly to V_{CC} and V_{ref} may be required depending upon circuit layout. This provides a low impedance path for filtering the high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI. The Error Amp compensation circuitry and the converter output voltage-divider should be located close to the IC and as far as possible from the power switch and other noise generating components.

FIGURE 18 — EXTERNAL DUTY CYCLE CLAMP AND MULTI UNIT SYNCHRONIZATION



$$D_{\max} \text{ Drive Output 1} = \frac{R_B}{R_A + R_B}$$

$$D_{\max} \text{ Drive Output 2} = \frac{R_A}{R_A + R_B}$$

FIGURE 19 — ADJUSTABLE REDUCTION OF CLAMP LEVEL

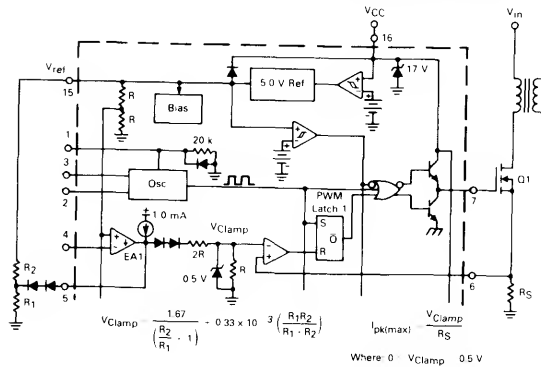


FIGURE 20 — SOFT-START CIRCUIT

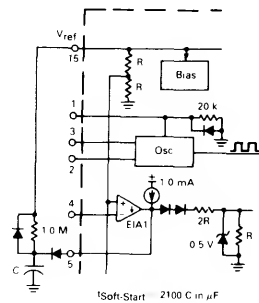


FIGURE 21 — ADJUSTABLE REDUCTION OF CLAMP LEVEL WITH SOFT-START

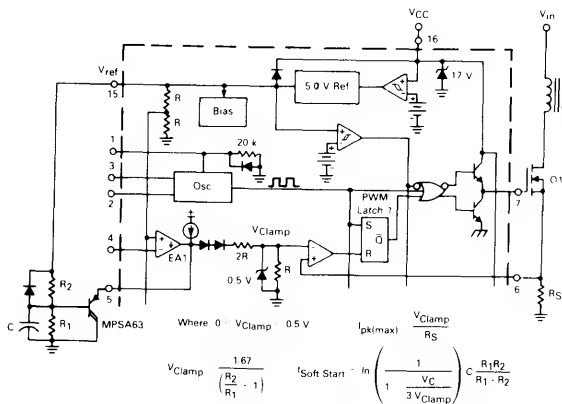


FIGURE 22 — MOSFET PARASITIC OSCILLATIONS

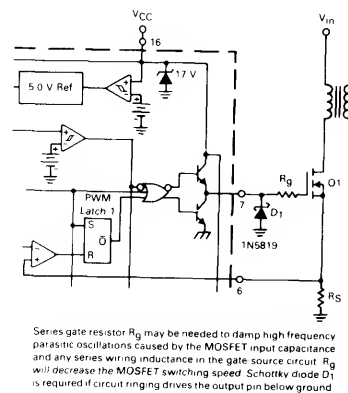


FIGURE 23 — CURRENT SENSING POWER MOSFET

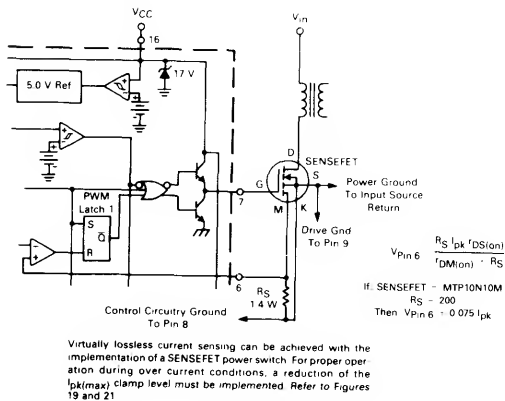


FIGURE 24 — CURRENT WAVEFORM SPIKE SUPPRESSION

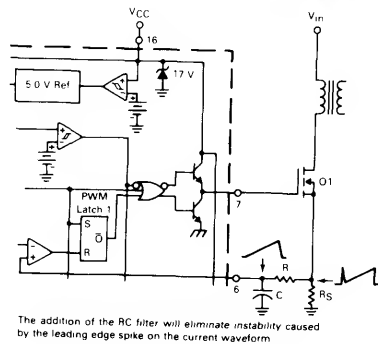
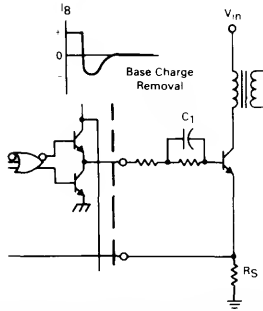
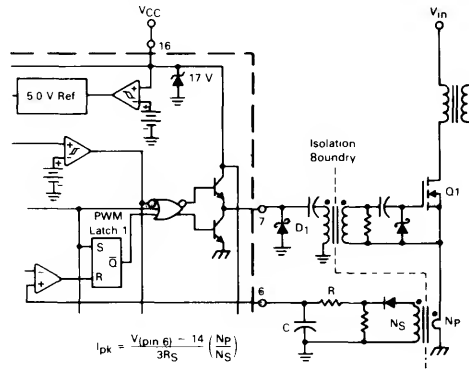


FIGURE 25 — BIPOLAR TRANSISTOR DRIVE



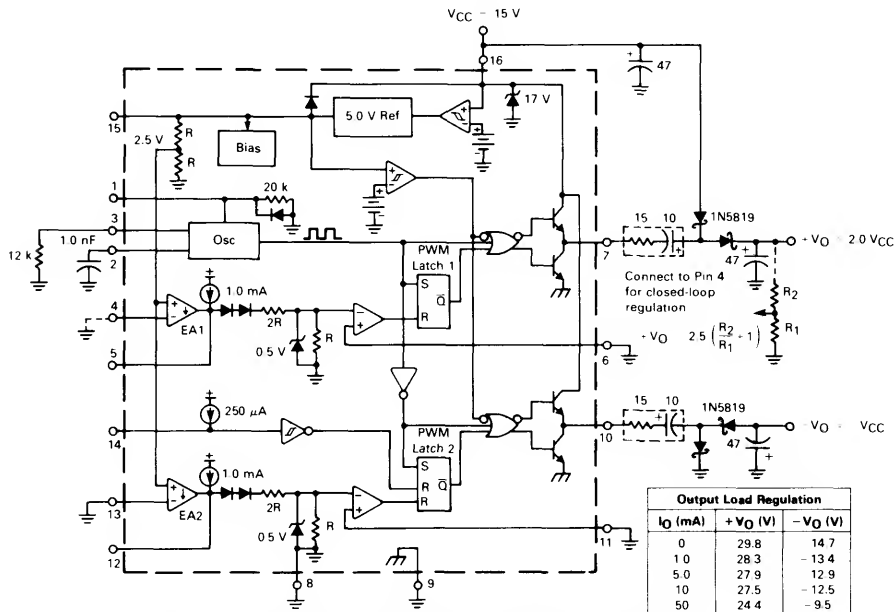
The totem-pole outputs can furnish negative base current for enhanced transistor turn-off, with the addition of capacitor C₁.

FIGURE 26 — ISOLATED MOSFET DRIVE



$$I_{pk} = \frac{V_{(pin 6)} - 14}{3R_S} \left(\frac{N_p}{N_S} \right)$$

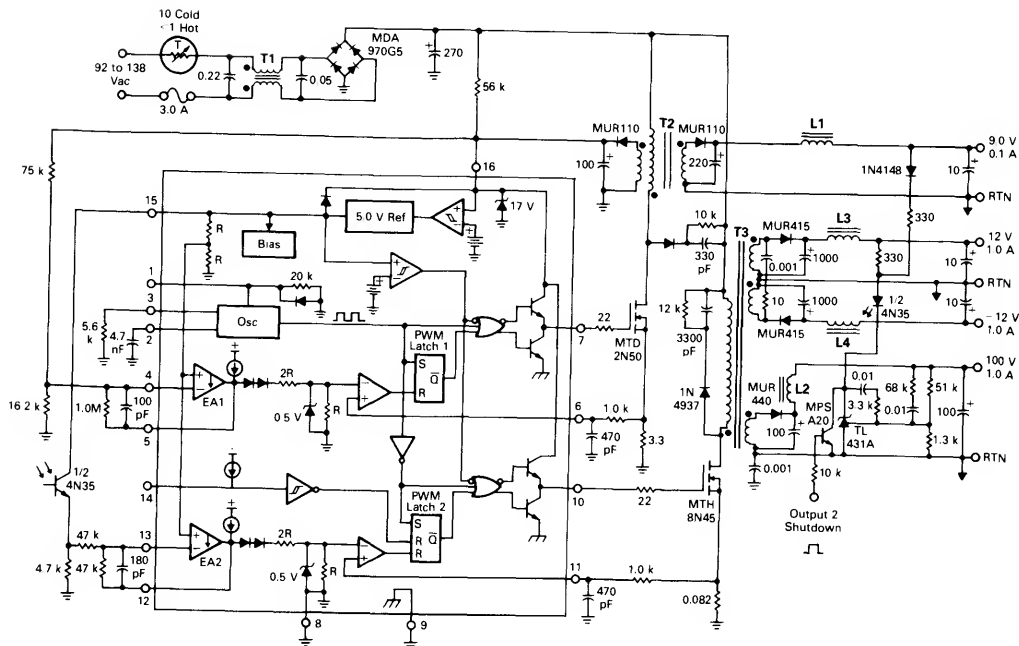
FIGURE 27 — DUAL CHARGE PUMP CONVERTER



Output Load Regulation		
I _O (mA)	+V _O (V)	-V _O (V)
0	29.8	14.7
1.0	28.3	-13.4
5.0	27.9	12.9
10	27.5	-12.5
50	24.4	-9.5

The capacitor's equivalent series resistance must limit the Drive Output current to 1.0 A. An additional series resistor may be required when using tantalum or other low ESR capacitors. The positive output can provide excellent line and load regulation by connecting the R₂/R₁ resistor divider as shown.

FIGURE 28 — 125 WATT OFF-LINE CONVERTER

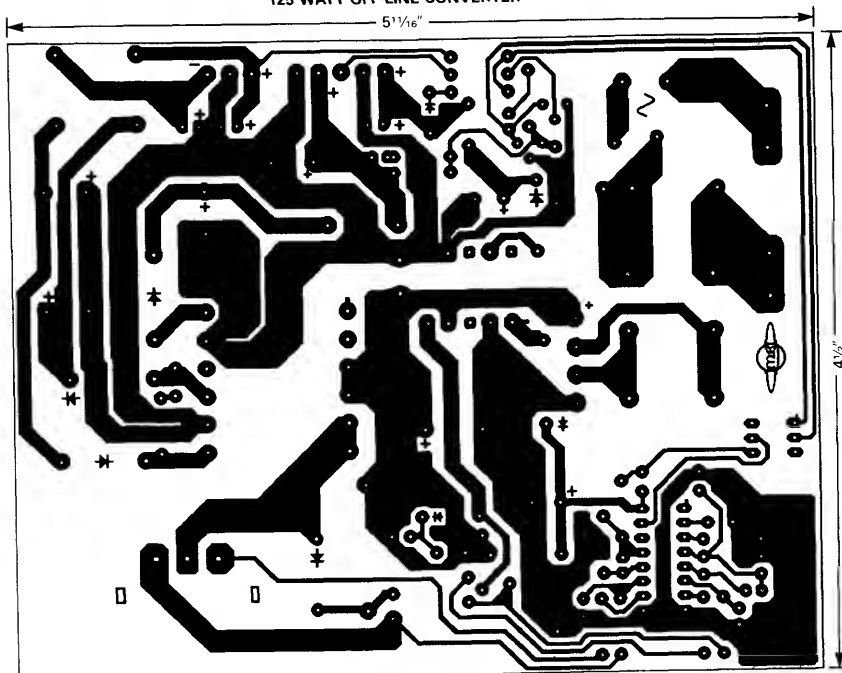


Test	Conditions	Results
Line Regulation 100 V Output ± 12 V Outputs 9.0 V Output	$V_{in} = 92 \text{ to } 138 \text{ Vac}$ $I_O = 1.0 \text{ A}$ $I_O = \pm 1.0 \text{ A}$ $I_O = 0.1 \text{ A}$	$\Delta = 40 \text{ mV or } \pm 0.02\%$ $\Delta = 32 \text{ mV or } \pm 0.13\%$ $\Delta = 55 \text{ mV or } \pm 0.31\%$
Load Regulation 100 V Output ± 12 V Outputs 9.0 V Output	$V_{in} = 115 \text{ Vac}$ $I_O = 0.25 \text{ A to } 1.0 \text{ A}$ $I_O = \pm 0.25 \text{ A to } \pm 1.0 \text{ A}$ $I_O = 0.08 \text{ A to } 0.1 \text{ A}$	$\Delta = 50 \text{ mV or } \pm 0.025\%$ $\Delta = 320 \text{ mV or } \pm 1.2\%$ $\Delta = 234 \text{ mV or } \pm 1.3\%$
Output Ripple 100 V Output ± 12 V Outputs 9.0 V Output	$V_{in} = 115 \text{ Vac}$ $I_O = 1.0 \text{ A}$ $I_O = \pm 1.0 \text{ A}$ $I_O = 0.1 \text{ A}$	40 mVp-p 100 mVp-p 60 mVp-p
Short Circuit Current 100 V Output ± 12 V Outputs 9.0 V Output	$V_{in} = 115 \text{ Vac, } R_L = 0.1 \Omega$	4.3 A 17 A Output Hiccups
Efficiency	$V_{in} = 115 \text{ Vac, } P_O = 125 \text{ W}$	86%

T1 — 468 μH per section at 2.5 A,
Coilcraft E3496A
T2 — Primary: 156 Turns, #34 AWG
Primary Feedback: 19 Turns,
#34 AWG
Secondary: 17 Turns, #28 AWG
Core: TDK H7C1E22-Z
Bobbin: BE22-6H
Gap: $\sim 0.001"$ for a primary
inductance of 6.8 mH
T3 — Primary: 56 Turns, #23 AWG
(2 strands) Bifilar Wound
Secondary: $\pm 12 \text{ V}$: 4 Turns,
#23 AWG (4 strands)
Quadrifilar Wound
Secondary 100 V: 32 Turns,
#23 AWG (2 strands) Bifilar
Wound
Core: Ferroxcube EEC 40-3C8
Bobbin: Ferroxcube 40-1112CP
Gap: $\sim 0.030"$ for a primary
inductance of 212 μH
L1, L3, L4 — 25 μH at 1.0 A,
Coilcraft Z7157
L2 — 10 μH at 3.0 A, Coilcraft
PCV-0-010-03.

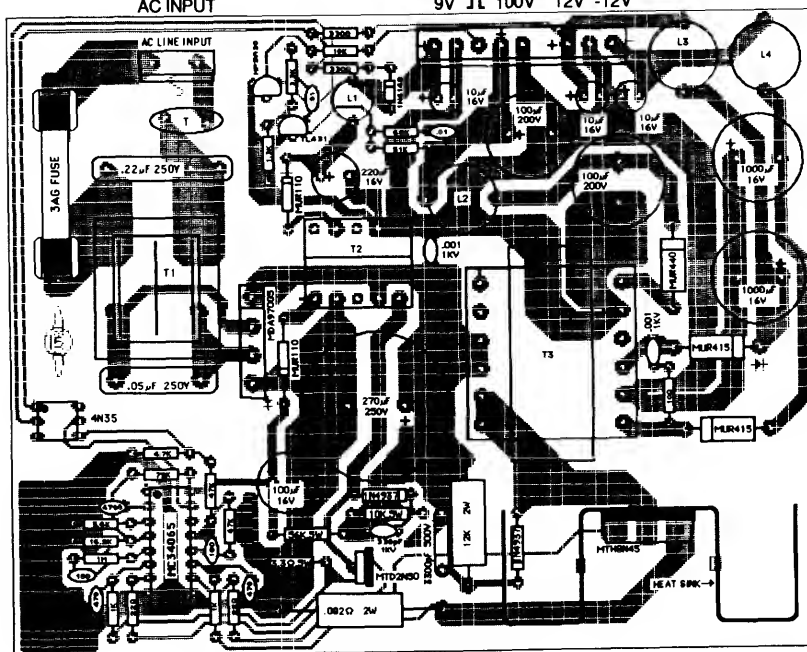
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• 5 11/16"



AC INPUT

9V Π^* 100V 12V -12V



COMPONENT VIEW

• 100 V & ± 12 V Shutdown

PIN FUNCTION DESCRIPTION

Pin #	Function	Description
1	Sync Input	A narrow rectangular waveform applied to this input will synchronize the Oscillator. A dc voltage within the range of 2.4 V to 5.5 V will inhibit the Oscillator.
2	C_T	Timing capacitor C_T connects from this pin to ground setting the free-running Oscillator frequency range.
3	R_T	Resistor R_T connects from this pin to ground precisely setting the charge current for C_T . R_T must be between 4.0 k and 16 k.
4	Voltage Feedback 1	This pin is the inverting input of Error Amplifier 1. It is normally connected to the switching power supply output through a resistor divider.
5	Compensation 1	This pin is the output of Error Amplifier 1 and is made available for loop compensation.
6	Current Sense 1	A voltage proportional to the inductor current is connected to this input. PWM 1 uses this information to terminate conduction of output switch Q1.
7	Drive Output 1	This pin directly drives the gate of a power MOSFET Q1. Peak currents up to 1.0 A are sourced and sunk by this pin.
8	Gnd	This pin is the control circuitry ground return and is connected back to the source ground.
9	Drive Gnd	This pin is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
10	Drive Output 2	This pin directly drives the gate of a power MOSFET Q2. Peak currents up to 1.0 A are sourced and sunk by this pin.
11	Current Sense 2	A voltage proportional to inductor current is connected to this input. PWM 2 uses this information to terminate conduction of output switch Q2.
12	Compensation 2	This pin is the output of Error Amplifier 2 and is made available for loop compensation.
13	Voltage Feedback 2	This pin is the inverting input of Error Amplifier 2. It is normally connected to the switching power supply output through a resistor divider.
14	Drive Output 2 Enable	A logic low at this input disables Drive Output 2.
15	V_{ref}	This is the 5.0 V reference output. It can provide bias for any additional system circuitry.
16	V_{CC}	This pin is the positive supply of the control IC. The minimum operating voltage range after start-up is 11 V to 15.5 V.

Product Preview

HIGH PERFORMANCE RESONANT MODE CONTROLLER

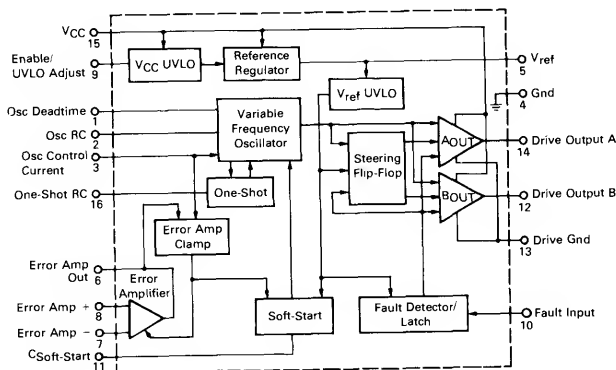
The MC34066 series are high performance resonant mode controllers designed for Off-Line and DC-to-DC converter applications that utilize frequency modulated constant on-time or constant off-time control. These integrated circuits feature a variable frequency oscillator with programmable deadtime, precision retriggerable one-shot timer, temperature compensated reference, high gain wide-bandwidth error amplifier with a precision output clamp, steering flip-flop, and dual high current totem pole outputs ideally suited for driving power MOSFETs.

Also included are protective features consisting of a high speed fault comparator and latch, programmable soft-start circuitry, input undervoltage lockout with selectable thresholds, and reference undervoltage lockout.

These devices are available in dual-in-line and surface mount packages.

- Variable Frequency Oscillator with a Control Range Exceeding 1000:1
- Programmable Oscillator Deadtime allows Constant Off-Time Operation
- Precision Retriggerable One-Shot Timer
- Internally Trimmed Bandgap Reference
- 5.0 MHz Error Amplifier with Precision Output Clamp
- Dual High Current Totem Pole Outputs
- Selectable Undervoltage Lockout Thresholds with Hysteresis
- Enable Input
- Programmable Soft-Start Circuitry
- Low Start-Up Current for Off-Line Operation

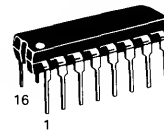
SIMPLIFIED BLOCK DIAGRAM



MC34066
MC33066

HIGH PERFORMANCE RESONANT MODE CONTROLLER

**SILICON MONOLITHIC
 INTEGRATED CIRCUIT**

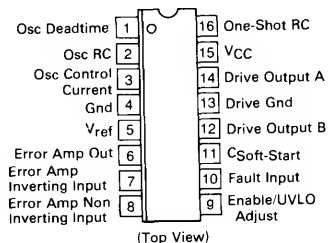


P SUFFIX
PLASTIC PACKAGE
CASE 648



DW SUFFIX
PLASTIC PACKAGE
CASE 751G
(SO-16)

PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
MC34066DW	0 to +70°C	SO-16
MC34066P		Plastic DIP
MC33066DW	-40 to +85°C	SO-16
MC33066P		Plastic DIP

This document contains information on a new product under development. Motorola reserves the right to change or discontinue the product without notice.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	20	V
Drive Output Current, Source or Sink (Note 1) Continuous Pulsed (0.5 μ s, 25% Duty Cycle)	I_O	0.3 1.5	A
Error Amplifier, Fault, One-Shot, Oscillator, and Soft-Start Inputs	V_{in}	-1.0 to +6.0	V
UVLO Adjust Input	$V_{in}(UVLO)$	-1.0 to V_{CC}	V
Power Dissipation and Thermal Characteristics DW Suffix Package SO-16 Case 751G Maximum Power Dissipation @ $T_A = 25^\circ\text{C}$ Thermal Resistance Junction to Air P Suffix Package Case 648 Maximum Power Dissipation @ $T_A = 25^\circ\text{C}$ Thermal Resistance Junction to Air	P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	862 145 1.25 100	mW $^\circ\text{C/W}$ W $^\circ\text{C/W}$
Operating Junction Temperature	T_J	+150	$^\circ\text{C}$
Operating Ambient Temperature MC34066 MC33066	T_A	0 to +70 -40 to +85	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($V_{CC} = 12\text{ V}$ [Note 2], $R_{OSC} = 95.3\text{ k}$, $R_{DT} = 0\ \Omega$, $R_{VFO} = 5.62\text{ k}$, $C_{OSC} = 300\text{ pF}$, $R_T = 14.3\text{ k}$, $C_T = 300\text{ pF}$, $C_L = 1.0\text{ nF}$, for typical values $T_A = 25^\circ\text{C}$, for min/max values T_A is the operating ambient temperature range that applies [Note 3] unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Output Voltage ($I_O = 0\text{ mA}$, $T_A = 25^\circ\text{C}$)	V_{ref}	5.0	5.1	5.2	V
Line Regulation ($V_{CC} = 10\text{ V to }18\text{ V}$)	Reg_{line}	—	1.0	20	mV
Load Regulation ($I_O = 0\text{ mA to }10\text{ mA}$)	Reg_{load}	—	1.0	20	mV
Total Output Variation Over Line, Load, and Temperature	V_{ref}	4.9	—	5.3	mV
Output Short Circuit Current	I_O	25	100	190	mA
Reference Undervoltage Lockout Threshold	V_{th}	3.8	4.3	4.8	V

ERROR AMPLIFIER

Input Offset Voltage ($V_{CM} = 1.5\text{ V}$)	V_{IO}	—	1.0	10	mV
Input Bias Current ($V_{CM} = 1.5\text{ V}$)	I_{IB}	—	0.2	1.0	μA
Input Offset Current ($V_{CM} = 1.5\text{ V}$)	I_{IO}	—	0	0.5	μA
Open-Loop Voltage Gain ($V_{CM} = 1.5\text{ V}$, $V_O = 2.0\text{ V}$)	A_{VOL}	70	100	—	dB
Gain Bandwidth Product ($f = 100\text{ kHz}$)	GBW	2.5	4.2	—	MHz
Input Common Mode Rejection Ratio ($V_{CM} = 1.5\text{ V to }5.0\text{ V}$)	CMRR	70	95	—	dB
Power Supply Rejection Ratio ($V_{CC} = 10\text{ V to }18\text{ V}$, $f = 120\text{ Hz}$)	PSRR	80	100	—	dB
Output Voltage Swing High State with respect to Pin 3 ($I_{Source} = 2.0\text{ mA}$) Low State with respect to ground ($I_{Sink} = 1.0\text{ mA}$)	V_{OH} V_{OL}	2.1 —	2.5 0.4	2.9 0.6	V

- NOTES:**
- Maximum package power dissipation limits must be observed.
 - Adjust V_{CC} above the Start-Up threshold before setting to 12 V.
 - Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
 $T_{low} = 0^\circ\text{C}$ for MC34066 $T_{high} = +70^\circ\text{C}$ for MC34066
 $\quad\quad\quad = -40^\circ\text{C}$ for MC33066 $\quad\quad\quad = +85^\circ\text{C}$ for MC33066

MC34066, MC33066

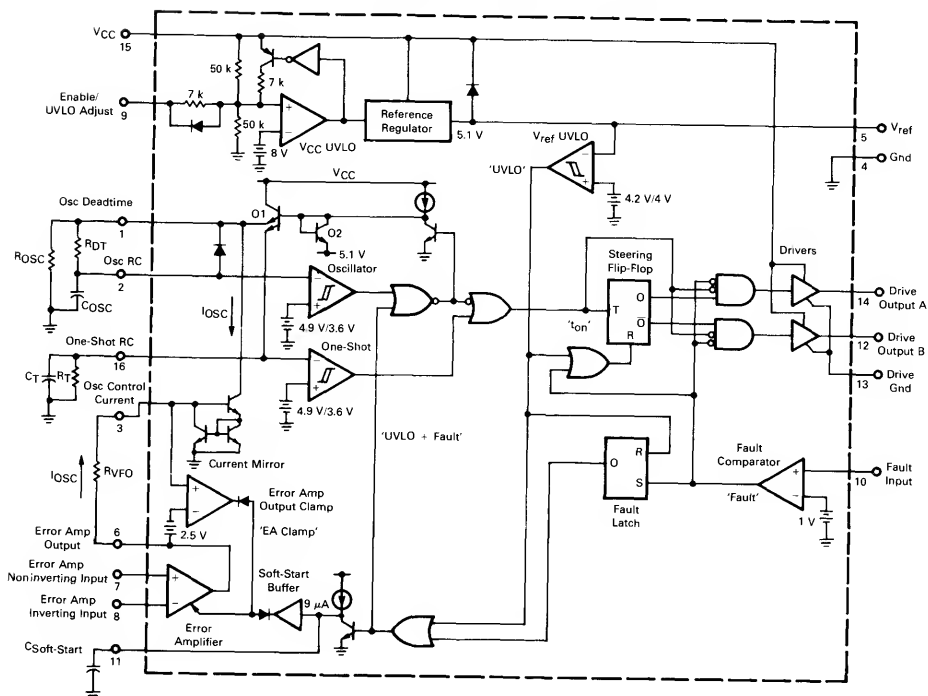
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ELECTRICAL CHARACTERISTICS (continued) ($V_{CC} = 12\text{ V}$ [Note 2], $R_{OSC} = 95.3\text{ k}$, $R_{DT} = 0\ \Omega$, $R_{VFO} = 5.62\text{ k}$, $C_{OSC} = 300\text{ pF}$, $R_T = 14.3\text{ k}$, $C_T = 300\text{ pF}$, $C_L = 1.0\text{ nF}$, for typical values $T_A = 25^\circ\text{C}$, for min/max values T_A is the operating ambient temperature range that applies [Note 3] unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Frequency (Error Amp Output Low) $T_A = 25^\circ\text{C}$ Total Variation ($V_{CC} = 10\text{ V to } 18\text{ V}$, $T_A = T_{Low}\text{ to } T_{High}$)	$f_{OSC(low)}$	90 85	100 —	110 115	kHz
Frequency (Error Amp Output High) $T_A = 25^\circ\text{C}$ Total Variation ($V_{CC} = 10\text{ V to } 18\text{ V}$, $T_A = T_{Low}\text{ to } T_{High}$)	$f_{OSC(high)}$	900 850	1000 —	1100 1150	kHz
Oscillator Control Input Voltage, Pin 3 ($I_{Sink} = 0.5\text{ mA}$, $T_A = 25^\circ\text{C}$)	V_{in}	1.3	1.4	1.5	V
Output Deadtime (Error Amp Output High) $R_{DT} = 0\ \Omega$ $R_{DT} = 1.0\text{ k}$	DT	— 600	70 700	100 800	ns
ONE-SHOT					
Drive Output On-Time ($R_{DT} = 1.0\text{ k}$) $T_A = 25^\circ\text{C}$ Total Variation ($V_{CC} = 10\text{ V to } 18\text{ V}$, $T_A = T_{Low}\text{ to } T_{High}$)	t_{ON}	1.43 1.4	1.5 —	1.57 1.6	μs
DRIVE OUTPUTS					
Output Voltage Low State ($I_{Sink} = 20\text{ mA}$) ($I_{Sink} = 200\text{ mA}$) High State ($I_{Source} = 20\text{ mA}$) ($I_{Source} = 200\text{ mA}$)	V_{OL} V_{OH}	— — 9.5 9.0	0.8 1.5 10.3 9.8	1.2 2.0 — —	V
Output Voltage with UVLO Activated ($V_{CC} = 6.0\text{ V}$, $I_{Sink} = 1.0\text{ mA}$)	$V_{OL(UVLO)}$	—	0.8	1.2	V
Output Voltage Rise Time ($C_L = 1.0\text{ nF}$)	t_r	—	20	50	ns
Output Voltage Fall Time ($C_L = 1.0\text{ nF}$)	t_f	—	20	50	ns
FAULT COMPARATOR					
Input Threshold	V_{th}	0.95	1.0	1.05	V
Input Bias Current ($V_{Pin\ 10} = 0\text{ V}$)	I_B	—	—2.0	—10	μA
Propagation Delay to Drive Outputs (100 mV Overdrive)	$t_{PLH(IN/OUT)}$	—	60	100	ns
SOFT-START					
Capacitor Charge Current ($V_{Pin\ 11} = 2.5\text{ V}$)	I_{chg}	4.5	9.0	14	μA
Capacitor Discharge Current ($V_{Pin\ 11} = 2.5\text{ V}$)	I_{dchg}	1.0	8.0	—	mA
UNDERVOLTAGE LOCKOUT					
Start-Up Threshold, V_{CC} Increasing Enable/UVLO Adjust Pin Open Enable/UVLO Adjust Pin Connected to V_{CC}	$V_{th(UVLO)}$	14.8 8.0	16 9.0	17.2 10	V
Minimum Operating Voltage After Turn-On Enable/UVLO Adjust Pin Open Enable/UVLO Adjust Pin Connected to V_{CC}	$V_{CC(min)}$	8.0 7.6	9.0 8.6	10 9.6	V
Enable/UVLO Adjust Shutdown Threshold Voltage	$V_{th(Enable)}$	6.0	7.0	—	V
Enable/UVLO Adjust Input Current (Pin 9 = 0 V)	$I_{in(Enable)}$	—	—0.2	—1.0	mA
TOTAL DEVICE					
Power Supply Current (Enable/UVLO Adjust Pin Open) Start-Up ($V_{CC} = 13.5\text{ V}$) Operating ($f_{OSC} = 100\text{ kHz}$, Note 2)	I_{CC}	— —	0.45 21	0.6 30	mA

NOTE 2. Adjust V_{CC} above the Start-Up threshold before setting to 12 V.

FIGURE 1 — MC34066 FUNCTIONAL BLOCK DIAGRAM



INTRODUCTION

As power supply designers have strived to increase power conversion efficiency and reduce passive component size, high frequency resonant mode power converters have emerged as attractive alternatives to conventional square-wave control. When compared to square-wave converters, resonant mode control offers several benefits including lower switching losses, higher efficiency, lower EMI emission, and smaller size. This integrated circuit has been developed to support new trends in power supply design. The MC34066 Resonant Mode Controller is a high performance bipolar IC dedicated to variable frequency power control at frequencies exceeding 1.0 MHz. This integrated circuit provides the features, performance and flexibility for a wide variety of resonant mode power supply applications.

The primary purpose of the control chip is to supply precise pulses to the gates of external power MOSFETs at a repetition rate regulated by a feedback control loop. The MC34066 can be operated in any of three modes as follows: 1) fixed on-time, variable frequency; 2) fixed off-time, variable frequency; and 3) combinations of 1 and 2 that change from fixed on-time to fixed off-time as the frequency increases. Additional features of the IC ensure that system start-up and fault conditions are administered in a safe, controlled manner.

A simplified block diagram of the IC is shown on the

first page of this data sheet, which identifies the main functional blocks and the block-to-block interconnects. Figure 1 is a detailed functional diagram which accurately represents the internal circuitry. The various functions can be divided into two sections. The first section includes the primary control path which produces precise output pulses at the desired frequency. Included in this section are a variable frequency Oscillator, a One-Shot, a pulse Steering Flip-Flop, a pair of power MOSFET Drivers, and a wide bandwidth Error Amplifier. The second section provides several peripheral voltage functions including a voltage reference, undervoltage lockout, Soft-Start circuit, and a fault detector.

PRIMARY CONTROL PATH

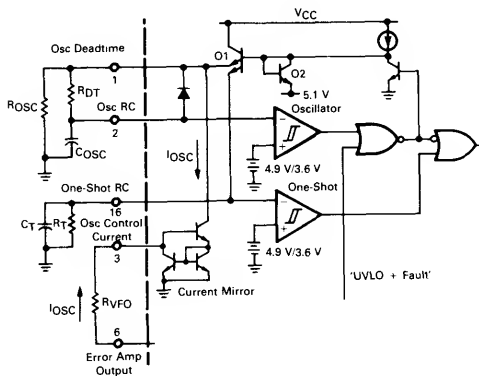
The output pulse width and repetition rate are regulated through the interaction of the variable frequency Oscillator, One-Shot timer and Error Amplifier. The Oscillator triggers the One-Shot which generates a pulse that is alternately steered to a pair of totem-pole output drivers by a toggle Flip-Flop. The Error Amplifier monitors the output of the regulator and modulates the frequency of the Oscillator. High-speed Schottky logic is used throughout the primary control channel to minimize delays and enhance high frequency characteristics.

Oscillator

The characteristics of the variable frequency Oscillator are crucial for precise controller performance at high operating frequencies. In addition to triggering the One-Shot timer and initiating the output pulse, the Oscillator also determines the initial voltage for the One-Shot capacitor and defines the minimum deadtime between output pulses. The Oscillator is designed to operate at frequencies exceeding 1.0 MHz. The Error Amplifier can control the oscillator frequency over a 1000:1 frequency range, and both the minimum and maximum frequencies are easily and accurately programmed by the proper selection of external components. The Oscillator also includes an adjustable deadtime feature for applications requiring additional time between output pulses.

The functional diagram of the Oscillator and One-Shot timer is shown in Figure 2. The oscillator capacitor C_{OSC} is initially charged by transistor Q1 through the optional deadtime resistor R_{DT} . When C_{OSC} exceeds the 4.9 V upper threshold of the oscillator comparator, the base of Q1 is pulled low allowing C_{OSC} to discharge through the external resistors and the internal Current Mirror. When the voltage on C_{OSC} falls below the comparator's 3.6 V lower threshold, Q1 turns on and again charges C_{OSC} .

FIGURE 2 — OSCILLATOR AND ONE-SHOT TIMER



If R_{DT} is zero ohms, C_{OSC} charges from 3.6 V to 5.1 V in less than 50 ns. The high slew rate of C_{OSC} and the propagation delay of the comparator make it difficult to control the peak voltage. This accuracy issue is overcome by clamping the base of Q1 through diode Q2 to a voltage reference. The peak voltage of the oscillator waveform is thereby precisely set at 5.1 V.

The frequency of the Oscillator is modulated by varying the current I_{OSC} flowing through R_{VFO} into the Osc Control Current pin. The control current drives a unity gain Current Mirror which pulls an identical current from the C_{OSC} capacitor. As I_{OSC} increases, C_{OSC} discharges faster thus decreasing the Oscillator period and increasing the frequency. The maximum frequency occurs when the Error Amplifier output is at the upper clamp level, nominally 2.5 V above the voltage at the Osc Control Current pin. The minimum discharge time

for C_{OSC} , which corresponds to the maximum oscillator frequency, is given by Equation 1.

$$t_{dchg(min)} = (R_{DT} + R_{OSC}) C_{OSC} \ln \left[\frac{2.5 R_{OSC} + 5.1}{R_{VFO}} \right] \quad (1)$$

The minimum oscillator frequency will result when the I_{OSC} current is zero, and C_{OSC} is discharged through the external resistors R_{OSC} and R_{DT} . This occurs when the Error Amplifier output voltage is less than the two diode drops required to bias the input of the Current Mirror. The maximum oscillator discharge time is given by Equation 2.

$$t_{dchg(max)} = (R_{DT} + R_{OSC}) C_{OSC} \ln \left(\frac{5.1}{3.6} \right) \quad (2)$$

The outputs of the control IC are off whenever the oscillator capacitor C_{OSC} is being charged by transistor Q1. The minimum time between output pulses (deadtime) can be programmed by controlling the charge time of C_{OSC} . Resistor R_{DT} reduces the current delivered by Q1 to C_{OSC} , thus increasing the charge time and the output deadtime. Varying R_{DT} from 0 to 1000 ohms will increase the output deadtime from 80 ns to 680 ns with C_{OSC} equal to 300 pF. The general expression for the oscillator charge time is given by Equation 3.

$$t_{chg} = R_{DT} C_{OSC} \ln \left(\frac{5.1 - 3.6}{5.1 - 4.9} \right) + 80 \text{ ns} \quad (3)$$

The minimum and maximum oscillator frequencies are programmed by the proper selection of resistor R_{OSC} and R_{VFO} . After selecting R_{DT} for the desired deadtime, the minimum frequency is programmed by R_{OSC} using Equations 2 and 3 in Equation 4:

$$\frac{1}{f_{OSC(min)}} = t_{dchg(max)} + t_{chg} \quad (4)$$

The maximum oscillator frequency is set by resistor R_{VFO} in a similar fashion using Equations 1 and 3 in Equation 5:

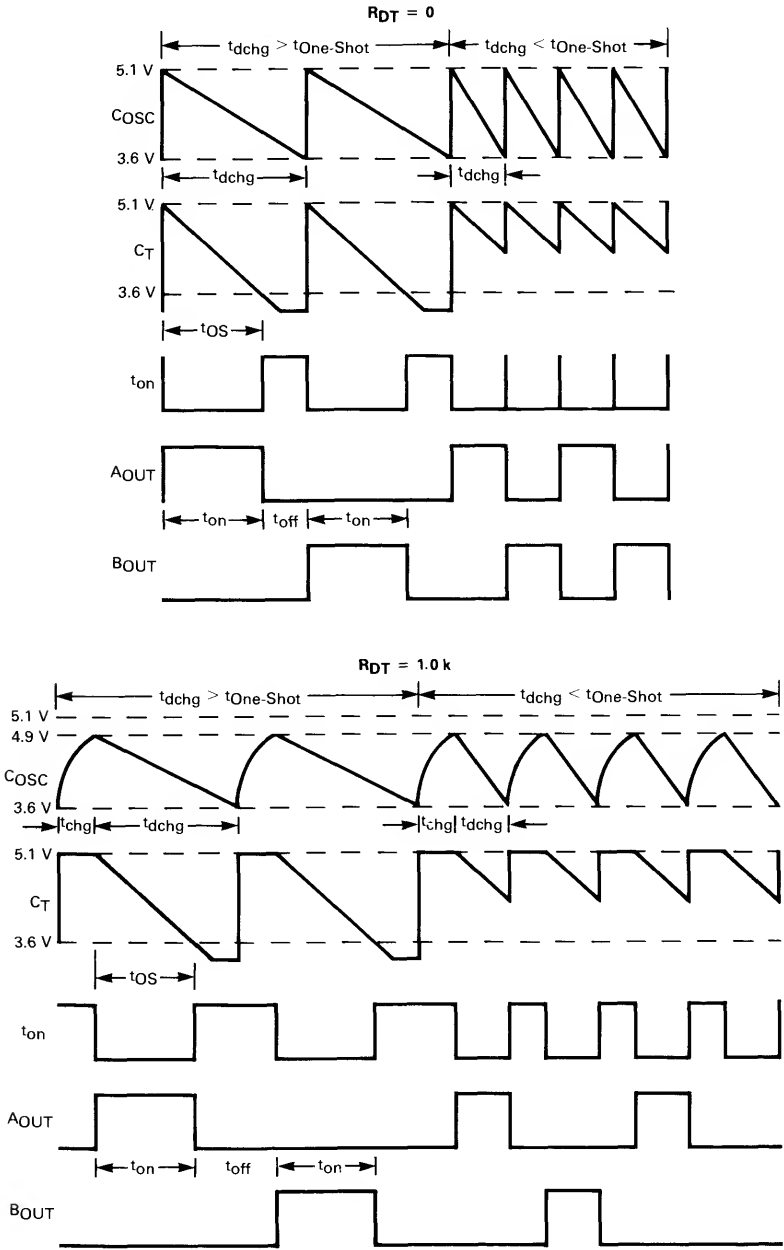
$$\frac{1}{f_{OSC(max)}} = t_{dchg(min)} + t_{chg} \quad (5)$$

The value chosen for resistor R_{DT} will affect the peak voltage of the oscillator waveform. As R_{DT} is increased from zero, the time required to charge C_{OSC} becomes large with respect to the propagation delay through the oscillator comparator. Consequently, the overshoot of the upper threshold is reduced and the peak voltage on the oscillator waveform drops from 5.1 V to 4.9 V. The best frequency accuracy is achieved when R_{DT} is zero ohms.

One-Shot Timer

The One-Shot capacitor C_T is charged concurrently with the oscillator capacitor by transistor Q1, as shown in Figure 2. The One-Shot period begins when the oscillator comparator turns off Q1, allowing C_T to discharge. The period ends when resistor R_T discharges C_T to the threshold of the One-Shot comparator. Discharging C_T from an initial voltage of 5.1 V to a threshold voltage of 3.6 V results in the One-Shot period given by Equation 6.

FIGURE 3 — TIMING WAVEFORMS



$$t_{OS} = R_T C_T \ln \left(\frac{5.1}{3.6} \right) = 0.348 R_T C_T \quad (6)$$

Errors in the threshold voltage and propagation delays through the output drivers will affect the One-Shot period. To guarantee accuracy, the output pulse of the control chip is trimmed to within 5% of 1.5 μ s with nominal values of R_T and C_T .

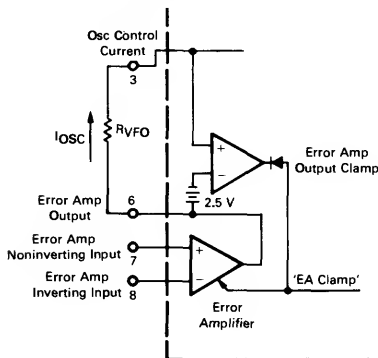
The outputs of the Oscillator and One-Shot comparators are OR'd together to produce the pulse 'ton', which drives the Flip-Flop and output drivers. The output pulse 'ton' is initiated by the Oscillator, but either the oscillator comparator or the One-Shot comparator can terminate the pulse. When the oscillator discharge time exceeds the one-shot period, the complete one-shot period is delivered to the output section. If the oscillator discharge time is less than the one-shot period, then the oscillator comparator terminates the pulse prematurely and retriggers the One-Shot. The waveforms on the left side of Figure 3 correspond to nonretriggered operation with constant on-time and variable off-times. The right side of Figure 3 represents retriggered operation with variable on-time and constant off-time.

Error Amplifier

A fully accessible high performance Error Amplifier is provided for feedback control of the power supply system. The Error Amplifier is internally compensated and features DC open loop gain greater than 70 dB, input offset voltage less than 10 mV and guaranteed minimum gain-bandwidth product of 2.5 MHz. The input common mode range extends from 1.5 V to 5.1 V, which includes the reference voltage. For common mode voltages below 1.5 V, the Error Amplifier output is forced low providing minimum oscillator frequency.

The Oscillator Control Current pin is biased by the Error Amplifier output voltage through R_{VFO} as illustrated in Figure 4. The output swing of the Error Amplifier is restricted by a clamp circuit to limit the maximum oscillator frequency. The clamp circuit limits the voltage across R_{VFO} to 2.5 V, thus limiting I_{OSC} to 2.5 V/ R_{VFO} . Oscillator accuracy is improved by trimming the clamp voltage to obtain the $f_{OSC}(\text{high})$ specification of 1.0 MHz with nominal value external components.

FIGURE 4 — ERROR AMPLIFIER AND CLAMP

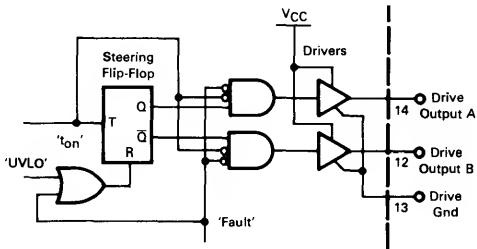


Output Section

The pulse, 'ton', generated by the Oscillator and One-Shot timer is gated to dual totem pole output drives by the Steering Flip-Flop shown in Figure 5. Positive transitions of 'ton' toggle the Flip-Flop, which causes the pulses to alternate between Output A and Output B. The flip-flop is reset by the undervoltage lockout circuit during start-up to guarantee that the first pulse appears at Output A.

The totem-pole output drivers are ideally suited for driving power MOSFETs and are capable of sourcing and sinking 1.5 Amps. Rise and fall times are typically 20 ns when driving a 1.0 nF load. High source/sink capability in a totem-pole driver normally increases the risk of high cross conduction current during output transitions. The MC34066 utilizes a unique design that virtually eliminates cross conduction, thus controlling the chip power dissipation at high frequencies. A separate ground terminal is provided for the output drivers to isolate the sensitive analog circuitry from large transient currents.

FIGURE 5 — STEERING FLIP-FLOP AND OUTPUT DRIVERS



PERIPHERAL SUPPORT FUNCTIONS

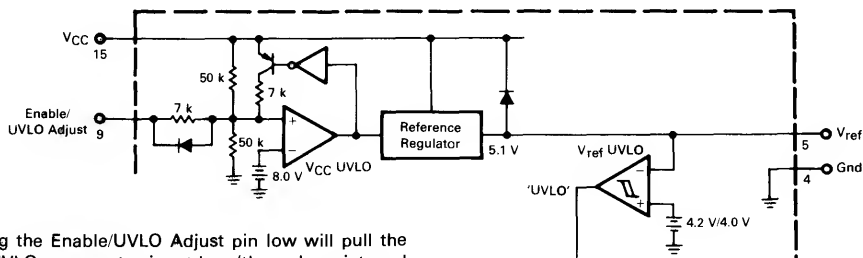
The MC34066 Resonant Controller provides a number of support and protection functions including a precision voltage reference, undervoltage lockout comparators, soft-start circuitry, and a fault detector. These peripheral circuits ensure that the power supply can be turned on and off in a safe, controlled manner and that the system will be quickly disabled when a fault condition occurs.

Undervoltage Lockout and Voltage Reference

Separate undervoltage lockout comparators sense the input V_{CC} voltage and the regulated reference voltage as illustrated in Figure 6. When V_{CC} increases to the upper threshold voltage, the V_{CC} UVLO comparator enables the Reference Regulator. After the V_{ref} output of the Reference Regulator rises to 4.2 V, the V_{ref} UVLO comparator switches the 'UVLO' signal to a logic zero state enabling the primary control path. Reducing V_{CC} to the lower threshold voltage causes the V_{CC} UVLO comparator to disable the Reference Regulator. The V_{ref} UVLO comparator then switches the 'UVLO' output to a logic one state disabling the controller.

The Enable/UVLO Adjust terminal allows the power supply designer to select the V_{CC} UVLO threshold voltages. When this pin is open, the comparator switches the controller on at 16 V and off at 9.0 V. If this pin is connected to the V_{CC} terminal, the upper and lower thresholds are reduced to 9.0 V and 8.6 V, respectively.

FIGURE 6 — UNDERVOLTAGE LOCKOUT AND REFERENCE



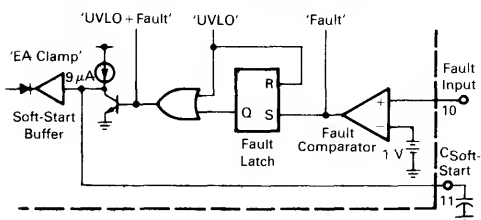
Forcing the Enable/UVLO Adjust pin low will pull the VCC UVLO comparator input low (through an internal diode) turning off the controller.

The Reference Regulator provides a precise 5.1 V reference to internal circuitry and can deliver up to 10 mA to external loads. The reference is trimmed to better than 2% initial accuracy and includes active short circuit protection.

Fault Detector

The high-speed Fault Comparator and Latch illustrated in Figure 7 can protect a power supply from destruction under fault conditions. The Fault Input pin connects to the input of the Fault Comparator. If this input exceeds the 1.0 V threshold of the comparator, the Fault Latch is set and two logic signals simultaneously disable the primary control path. The signal labeled 'Fault' at the output of the Fault Comparator is connected directly to the output drivers. This direct path reduces the propagation delay from the Fault Input to the A and B outputs to typically 70 ns. The Fault Latch output is OR'd with the 'UVLO' output from the Vref UVLO comparator to produce the logic output labeled 'UVLO + Fault.' This signal disables the Oscillator and One-Shot by forcing both the C_OSC and C_T capacitors to be continually charged.

FIGURE 7 — FAULT DETECTOR AND SOFT-START



The Fault Latch is reset during start-up by a logic one at the 'UVLO' output of the Vref UVLO comparator. The latch can also be reset after start-up by pulling the Enable/UVLO Adjust pin momentarily low to disable the Reference Regulator.

Soft-Start Circuit

The Soft-Start circuit shown in Figure 7 forces the variable frequency Oscillator to start at the minimum

frequency and ramp upward until regulated by the feedback control loop. The external capacitor at the C_{Soft-Start} terminal is initially discharged by the 'UVLO + Fault' signal. The low voltage on the capacitor passes through the Soft-Start Buffer to hold the Error Amplifier output low. After 'UVLO + Fault' switches to a logic zero, the soft-start capacitor is charged by a 9.0 μ A current source. The buffer allows the Error Amplifier output to follow the soft-start capacitor until it is regulated by the Error Amplifier inputs (or reaches the 2.5 V clamp). The soft-start function is generally applicable to controllers operating below resonance and can be disabled by simply opening the C_{Soft-Start} terminal.

APPLICATIONS

The MC34066 can be used for the control of series, parallel or higher order half/full bridge resonant converters. The IC is designed to provide control in discontinuous conduction mode (DCM) or continuous conduction mode (CCM) or a combination of the two. For example, in a parallel resonant converter (PRC) operating in the DCM, the IC is programmed to operate in fixed on-time, variable frequency mode of operation. For a PRC operating in the CCM, the IC can be programmed to operate in the variable frequency mode with a fixed off-time.

When operating with a wide input voltage range, such as a universal input power supply, a PRC can operate in the DCM for high input voltage and in the CCM for low input voltage. In this particular case, on-time is programmed corresponding to DCM. The deadtime of the chip is programmed to provide the desired off-time in the CCM. The frequency range is chosen to cover the complete frequency range from the DCM to the CCM. When programmed as such, the controller will operate in the fixed on-time, variable frequency mode at low frequencies. At the frequency which causes the Oscillator to retrigger the One-Shot, the control law changes to variable frequency with fixed off-time. At higher frequencies the supply will operate in the CCM with this control law.

Although the IC is designed and optimized for double ended push-pull type converters, it can also be used for single ended applications, such as forward and flyback resonant converters.

MC34129
MC33129

**HIGH PERFORMANCE
CURRENT MODE CONTROLLER**

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**

3

HIGH PERFORMANCE CURRENT MODE CONTROLLER

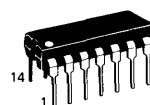
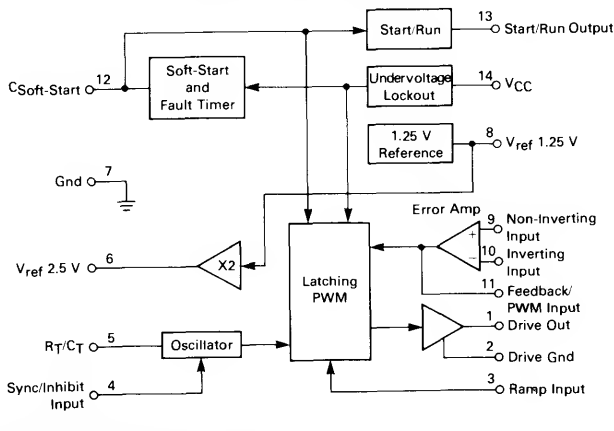
The MC34129 series are high performance current mode switching regulators specifically designed for use in low power digital telephone applications. These integrated circuits feature a unique internal fault timer that provides automatic restart for overload recovery. For enhanced system efficiency, a start/run comparator is included to implement bootstrapped operation of V_{CC} . Other functions contained are a temperature compensated reference, reference amplifier, fully accessible error amplifier, sawtooth oscillator with sync input, pulse width modulator comparator, and a high current totem pole driver ideally suited for driving a power MOSFET.

Also included are protective features consisting of soft-start, undervoltage lockout, cycle-by-cycle current limiting, adjustable dead time, and a latch for single pulse metering.

Although these devices are primarily intended for use in digital telephone systems, they can be used cost effectively in many other applications.

- Current Mode Operation to 300 kHz
- Automatic Feed Forward Compensation
- Latching PWM for Cycle-By-Cycle Current Limiting
- Continuous Retry after Fault Timeout
- Soft-Start with Maximum Peak Switch Current Clamp
- Internally Trimmed 2% Bandgap Reference
- High Current Totem Pole Driver
- Input Undervoltage Lockout
- Low Start-Up and Operating Current
- Direct Interface with Motorola SENSEFET Products

SIMPLIFIED BLOCK DIAGRAM

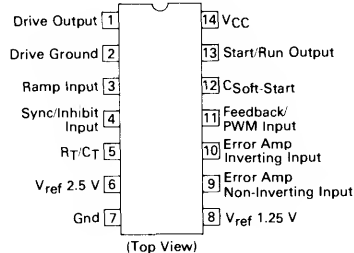


**P SUFFIX
PLASTIC PACKAGE
CASE 646**



**D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)**

PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
MC34129D	0 to +70°C	SO-14 Plastic DIP
MC34129P	0 to +70°C	Plastic DIP
MC33129D	-40 to +85°C	SO-14 Plastic DIP
MC33129P	-40 to +85°C	Plastic DIP

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MAXIMUM RATING

Rating	Symbol	Value	Unit
V _{CC} Zener Current	I _{Z(VCC)}	50	mA
Start/Run Output Zener Current	I _{Z(Start/Run)}	50	mA
Analog Inputs (Pins 3, 5, 9, 10, 11, 12)	—	−0.3 to 5.5	V
Sync Input Voltage	V _{sync}	−0.3 to V _{CC}	V
Drive Output Current, Source or Sink	I _{DRV}	1.0	A
Current, Reference Outputs (Pins 6, 8)	I _{ref}	20	mA
Power Dissipation and Thermal Characteristics D Suffix Package SO-14 Case 751A-01 Maximum Power Dissipation @ T _A = 70°C Thermal Resistance Junction to Air P Suffix Package Case 646-06 Maximum Power Dissipation @ T _A = 70°C Thermal Resistance Junction to Air	P _D R _{θJA} P _D R _{θJA}	552 145 800 100	mW °C/W mW °C/W
Operating Junction Temperature	T _J	+150	°C
Operating Ambient Temperature MC34129 MC33129	T _A	0 to +70 −40 to +85	°C
Storage Temperature Range	T _{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 10 V, T_A = 25°C [Note 1] unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
REFERENCE SECTIONS					
Reference Output Voltage, T _A = 25°C 1.25 V Ref., I _L = 0 mA 2.50 V Ref., I _L = 1.0 mA	V _{ref}	1.225 2.375	1.250 2.500	1.275 2.625	V
Reference Output Voltage, T _A = T _{low} to T _{high} 1.25 V Ref., I _L = 0 mA 2.50 V Ref., I _L = 1.0 mA	V _{ref}	1.200 2.250	— —	1.300 2.750	V
Line Regulation (V _{CC} = 4.0 V to 12 V) 1.25 V Ref., I _L = 0 mA 2.50 V Ref., I _L = 1.0 mA	Reg _{line}	— —	2.0 10	12 50	mV
Load Regulation 1.25 V Ref., I _L = −10 to +500 μA 2.50 V Ref., I _L = −0.1 to +1.0 mA	Reg _{load}	— —	1.0 3.0	12 25	mV

ERROR AMPLIFIER

Input Offset Voltage (V _{in} = 1.25 V) T _A = 25°C T _A = T _{low} to T _{high}	V _{IO}	— —	1.5 —	— 10	mV
Input Offset Current (V _{in} = 1.25 V)	I _{IO}	—	10	—	nA
Input Bias Current (V _{in} = 1.25 V) T _A = 25°C T _A = T _{low} to T _{high}	I _{IB}	— —	25 —	— 200	nA
Input Common-Mode Voltage Range	V _{ICR}	—	0.5 to 5.5	—	V
Open-Loop Voltage Gain (V _O = 1.25 V)	AVOL	65	87	—	dB
Gain Bandwidth Product (V _O = 1.25 V, f = 100 kHz)	GBW	500	750	—	kHz
Power Supply Rejection Ratio (V _{CC} = 5.0 to 10 V)	PSRR	65	85	—	dB
Output Source Current (V _O = 1.5 V)	I _{Source}	40	80	—	μA
Output Voltage Swing High State (I _{Source} = 0 μA) Low State (I _{Sink} = 500 μA)	V _{OH} V _{OL}	1.75 —	1.96 0.1	2.25 0.15	V

Note 1. T_{low} = 0°C for MC34129
= −40°C for MC33129

T_{high} = +70°C for MC34129
= +85°C for MC33129

MC34129, MC33129

ELECTRICAL CHARACTERISTICS ($V_{CC} = 10\text{ V}$, $T_A = 25^\circ\text{C}$ [Note 1] unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
PWM COMPARATOR					
Input Offset Voltage ($V_{in} = 1.25\text{ V}$)	V_{IO}	150	275	400	mV
Input Bias Current	I_{IB}	—	—120	—250	μA
Propagation Delay, Ramp Input to Drive Output	$t_{PLH}(IN/DRV)$	—	250	—	ns
SOFT-START					
Capacitor Charge Current (Pin 12 = 0 V)	I_{chg}	0.75	1.2	1.50	μA
Buffer Input Offset Voltage ($V_{in} = 1.25\text{ V}$)	V_{IO}	—	15	40	mV
Buffer Output Voltage ($I_{Sink} = 100\text{ }\mu\text{A}$)	V_{OL}	—	0.15	0.225	V
FAULT TIMER					
Restart Delay Time	t_{DLY}	200	400	600	μs
START/RUN COMPARATOR					
Threshold Voltage (Pin 12)	V_{th}	—	2.0	—	V
Threshold Hysteresis Voltage (Pin 12)	V_H	—	350	—	mV
Output Voltage ($I_{Sink} = 500\text{ }\mu\text{A}$)	V_{OL}	9.0	10	10.3	V
Output Off-State Leakage Current ($V_{OH} = 15\text{ V}$)	$I_{S/R}(leak)$	—	0.4	2.0	μA
Output Zener Voltage ($I_Z = 10\text{ mA}$)	V_Z	—	($V_{CC} + 7.6$)	—	V
OSCILLATOR					
Frequency ($R_T = 25.5\text{ k}\Omega$, $C_T = 390\text{ pF}$)	f_{OSC}	80	100	120	kHz
Capacitor C_T Discharge Current (Pin 5 = 1.2 V)	I_{dischg}	240	350	460	μA
Sync Input Current High State ($V_{in} = 2.0\text{ V}$) Low State ($V_{in} = 0.8\text{ V}$)	I_{IH} I_{IL}	— —	40 15	125 35	μA
Sync Input Resistance	R_{in}	12.5	32	50	k Ω
DRIVE OUTPUT					
Output Voltage High State ($I_{Source} = 200\text{ mA}$) Low State ($I_{Sink} = 200\text{ mA}$)	V_{OH} V_{OL}	8.3 —	8.9 1.4	— 1.8	V
Low State Holding Current	I_H	—	225	—	μA
Output Voltage Rise Time ($C_L = 500\text{ pF}$)	t_r	—	390	—	ns
Output Voltage Fall Time ($C_L = 500\text{ pF}$)	t_f	—	30	—	ns
Output Pull-Down Resistance	R_{PD}	100	225	350	k Ω
UNDERVOLTAGE LOCKOUT					
Start-Up Threshold	V_{th}	3.0	3.6	4.2	V
Hysteresis	V_H	5.0	10	15	%
TOTAL DEVICE					
Power Supply Current $R_T = 25.5\text{ k}\Omega$, $C_T = 390\text{ pF}$, $C_L = 500\text{ pF}$	I_{CC}	1.0	2.5	4.0	mA
Power Supply Zener Voltage ($I_Z = 10\text{ mA}$)	V_Z	12	14.3	—	V

Note 1. $T_{low} = 0^\circ\text{C}$ for MC34129
= -40°C for MC33129

$T_{high} = +70^\circ\text{C}$ for MC34129
= $+85^\circ\text{C}$ for MC33129

FIGURE 1 — TIMING RESISTOR versus OSCILLATOR FREQUENCY

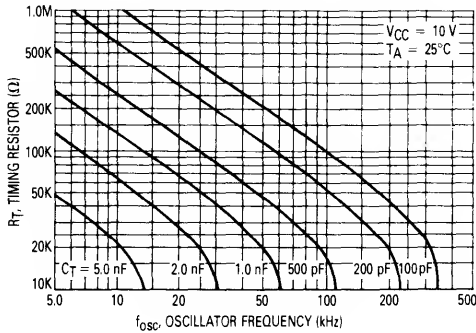


FIGURE 2 — OUTPUT DEAD-TIME versus OSCILLATOR FREQUENCY

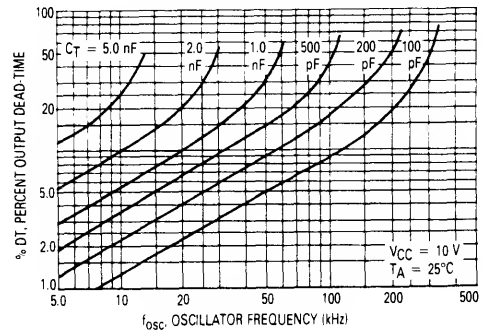


FIGURE 3 — OSCILLATOR FREQUENCY CHANGE versus TEMPERATURE

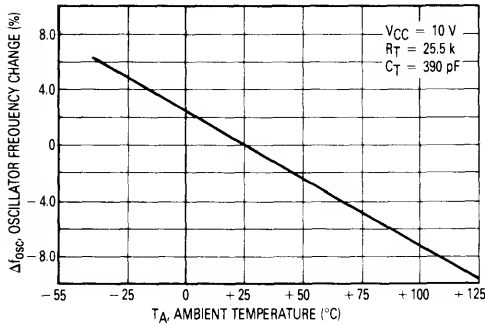


FIGURE 4 — ERROR AMP OPEN-LOOP GAIN AND PHASE versus FREQUENCY

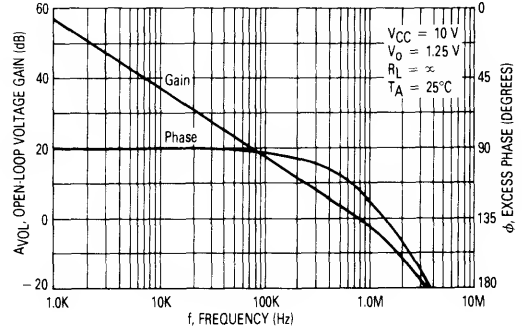


FIGURE 5 — ERROR AMP SMALL-SIGNAL TRANSIENT RESPONSE

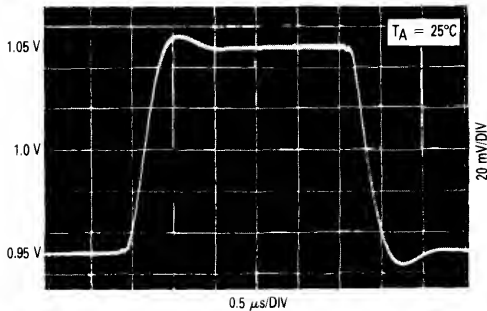


FIGURE 6 — ERROR AMP LARGE-SIGNAL TRANSIENT RESPONSE

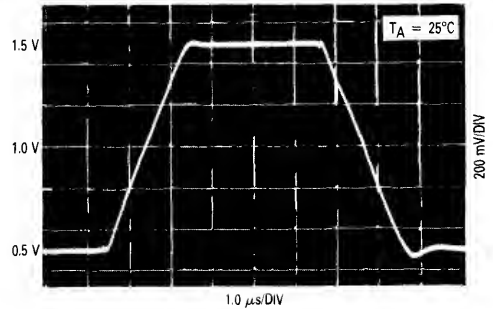


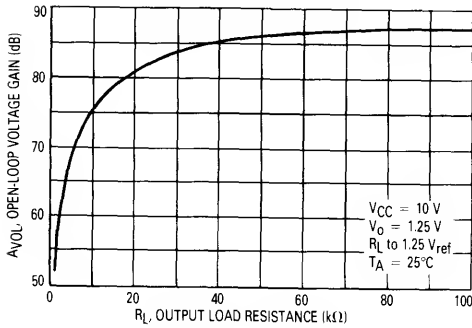
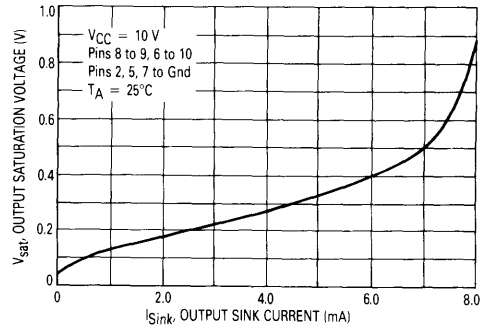
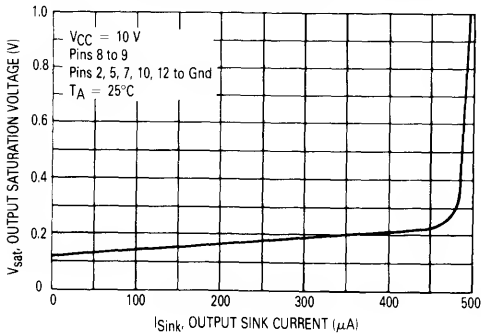
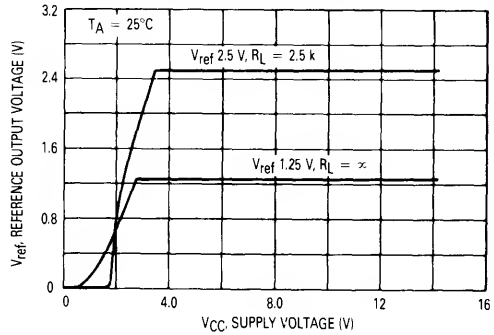
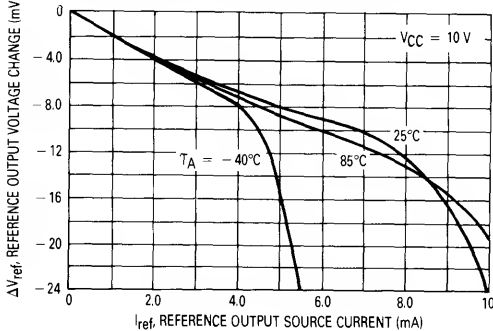
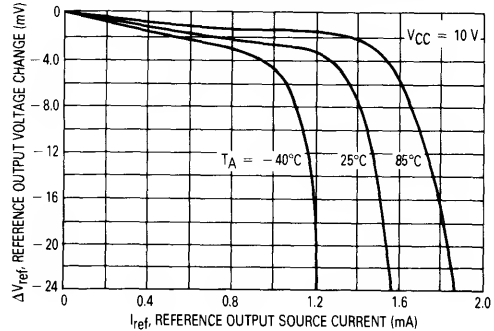
FIGURE 7 — ERROR AMP OPEN-LOOP DC GAIN
versus LOAD RESISTANCEFIGURE 8 — ERROR AMP OUTPUT SATURATION
versus SINK CURRENTFIGURE 9 — SOFT-START BUFFER OUTPUT SATURATION
versus SINK CURRENTFIGURE 10 — REFERENCE OUTPUT VOLTAGE versus
SUPPLY VOLTAGEFIGURE 11 — 1.25 V REFERENCE OUTPUT VOLTAGE
CHANGE versus SOURCE CURRENTFIGURE 12 — 2.5 V REFERENCE OUTPUT VOLTAGE
CHANGE versus SOURCE CURRENT

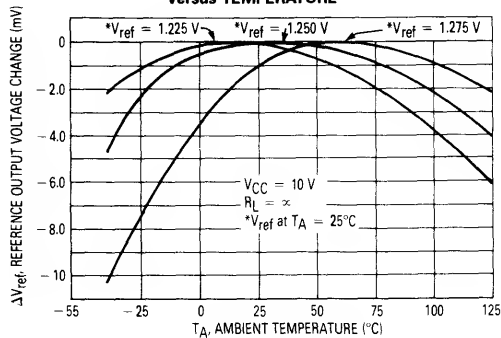
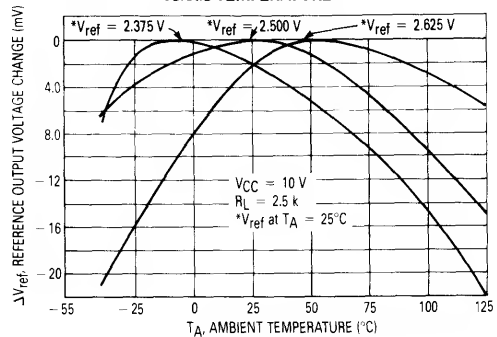
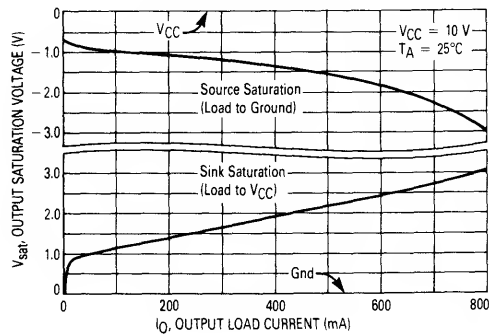
FIGURE 13 — 1.25 V REFERENCE OUTPUT VOLTAGE
versus TEMPERATUREFIGURE 14 — 2.5 V REFERENCE OUTPUT VOLTAGE
versus TEMPERATUREFIGURE 15 — DRIVE OUTPUT SATURATION
versus LOAD CURRENT

FIGURE 16 — DRIVE OUTPUT WAVEFORM

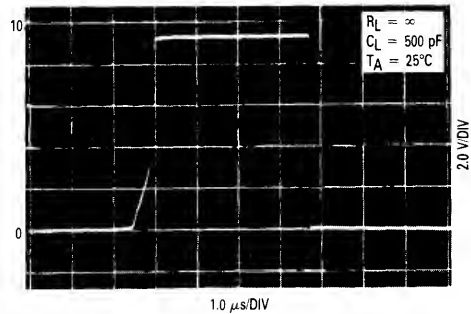
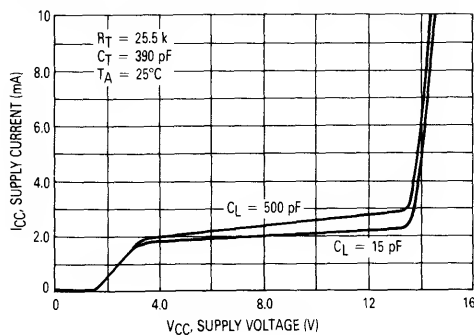


FIGURE 17 — SUPPLY CURRENT versus SUPPLY VOLTAGE



PIN FUNCTION DESCRIPTION

3

Pin No.	Function	Description
1	Drive Output	This output directly drives the gate of a power MOSFET. Peak currents up to 1.0 A are sourced and sunk by this pin.
2	Drive Ground	This pin is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
3	Ramp Input	A voltage proportional to the inductor current is connected to this input. The PWM uses this information to terminate output switch conduction.
4	Sync/Inhibit Input	A rectangular waveform applied to this input will synchronize the Oscillator and limit the maximum Drive Output duty cycle. A dc voltage within the range of 2.0 V to V_{CC} will inhibit the controller.
5	R_T/C_T	The free-running Oscillator frequency and maximum Drive Output duty cycle are programmed by connecting resistor R_T to V_{ref} 2.5 V and capacitor C_T to Ground. Operation to 300 kHz is possible.
6	V_{ref} 2.50 V	This output is derived from V_{ref} 1.25 V. It provides charging current for capacitor C_T through resistor R_T .
7	Ground	This pin is the control circuitry ground return and is connected back to the source ground.
8	V_{ref} 1.25 V	This output furnishes a voltage reference for the Error Amplifier Non-Inverting Input.
9	Error Amp Non-Inverting Input	This is the non-inverting input of the Error Amplifier. It is normally connected to the 1.25 V reference.
10	Error Amp Inverting Input	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
11	Feedback/PWM Input	This pin is available for loop compensation. It is connected to the Error Amplifier and Soft-Start Buffer outputs, and the Pulse Width Modulator input.
12	$C_{Soft-Start}$	A capacitor $C_{Soft-Start}$ is connected from this pin to Ground for a controlled ramp-up of peak inductor current during start-up.
13	Start/Run Output	This output controls the state of an external bootstrap transistor. During the start mode, operating bias is supplied by the transistor from V_{in} . In the run mode, the transistor is switched off and bias is supplied by an auxiliary power transformer winding.
14	V_{CC}	This pin is the positive supply of the control IC. The controller is functional over a minimum V_{CC} range of 4.2 V to 12 V.

OPERATING DESCRIPTION

3

The MC34129 series are high performance current mode switching regulator controllers specifically designed for use in low power telecommunication applications. Implementation will allow remote digital telephones and terminals to shed their power cords and derive operating power directly from the twisted pair used for data transmission. Although these devices are primarily intended for use in digital telephone systems, they can be used cost effectively in a wide range of converter applications. A representative block diagram is shown in Figure 18.

OSCILLATOR

The oscillator frequency is programmed by the values selected for the timing components R_T and C_T . Capacitor C_T is charged from the 2.5 V reference through resistor R_T to approximately 1.25 V and discharged by an internal current sink to ground. During the discharge of C_T , the oscillator generates an internal blanking pulse that holds the lower input of the NOR gate high. This causes the Drive Output to be in a low state, thus producing a controlled amount of output deadtime. Figure 1 shows Oscillator Frequency versus R_T and Figure 2, Output Deadtime versus Frequency, both for given values of C_T . Note that many values of R_T and C_T will give the same oscillator frequency but only one combination will yield a specific output deadtime at a given frequency. In many noise sensitive applications it may be desirable to frequency-lock one or more switching regulators to an external system clock. This can be accomplished by applying the clock signal to the Sync/Inhibit Input. For reliable locking, the free-running oscillator frequency should be about 10% less than the clock frequency. Referring to the timing diagram shown in Figure 19, the rising edge of the clock signal applied to the Sync/Inhibit Input, terminates charging of C_T and Drive Output conduction. By tailoring the clock waveform, accurate duty cycle clamping of the Drive Output can be achieved. A circuit method is shown in Figure 20. The Sync/Inhibit Input may also be used as a means for system shutdown by applying a dc voltage that is within the range of 2.0 V to V_{CC} .

PWM COMPARATOR AND LATCH

The MC34129 operates as a current mode controller whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches a threshold level established by the output of the Error Amp or Soft-Start Buffer (Pin 11). Thus the error signal controls the peak inductor current on a cycle-by-cycle basis. The PWM Comparator-Latch configuration used, ensures that only a single pulse appears at the Drive Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting the ground-referenced resistor R_S in series with the source of output switch Q_1 . The Ramp Input adds an offset of 275 mV to this voltage to guarantee that no pulses appear at the Drive Output when Pin 11 is at its

lowest state. This occurs at the beginning of the soft-start interval or when the power supply is operating and the load is removed. The peak inductor current under normal operating conditions is controlled by the voltage at Pin 11 where:

$$I_{pk} = \frac{V(\text{Pin 11}) - 0.275 \text{ V}}{R_S}$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the voltage at Pin 11 will be internally clamped to 1.95 V by the output of the Soft-Start Buffer. Therefore the maximum peak switch current is:

$$I_{pk(\text{max})} = \frac{1.95 \text{ V} - 0.275}{R_S} = \frac{1.675 \text{ V}}{R_S}$$

When designing a high power switching regulator it becomes desirable to reduce the internal clamp voltage in order to keep the power dissipation of R_S to a reasonable level. A simple method which adjusts this voltage in discrete increments is shown in Figure 22. This method is possible because the Ramp Input bias current is always negative (typically $-120 \mu\text{A}$). A positive temperature coefficient equal to that of the diode string will be exhibited by $I_{pk(\text{max})}$. An adjustable method that is more precise and temperature stable is shown in Figure 23. Erratic operation due to noise pickup can result if there is an excessive reduction of the clamp voltage. In this situation, high frequency circuit layout techniques are imperative.

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Ramp Input with a time constant that approximates the spike duration will usually eliminate the instability; refer to Figure 25.

ERROR AMP AND SOFT-START BUFFER

A fully-compensated Error Amplifier with access to both inputs and output is provided for maximum design flexibility. The Error Amplifier output is common with that of the Soft-Start Buffer. These outputs are open-collector (sink only) and are ORed together at the inverting input of the PWM Comparator. With this configuration, the amplifier that demands lower peak inductor current dominates control of the loop. Soft-start is mandatory for stable start-up when power is provided through a high source impedance such as the long twisted pair used in telecommunications. It effectively removes the load from the output of the switching power supply upon initial start-up. The Soft-Start Buffer is configured as a unity gain follower with the non-inverting input connected to Pin 12. An internal $1.0 \mu\text{A}$

MC34129, MC33129

FIGURE 18 — REPRESENTATIVE BLOCK DIAGRAM

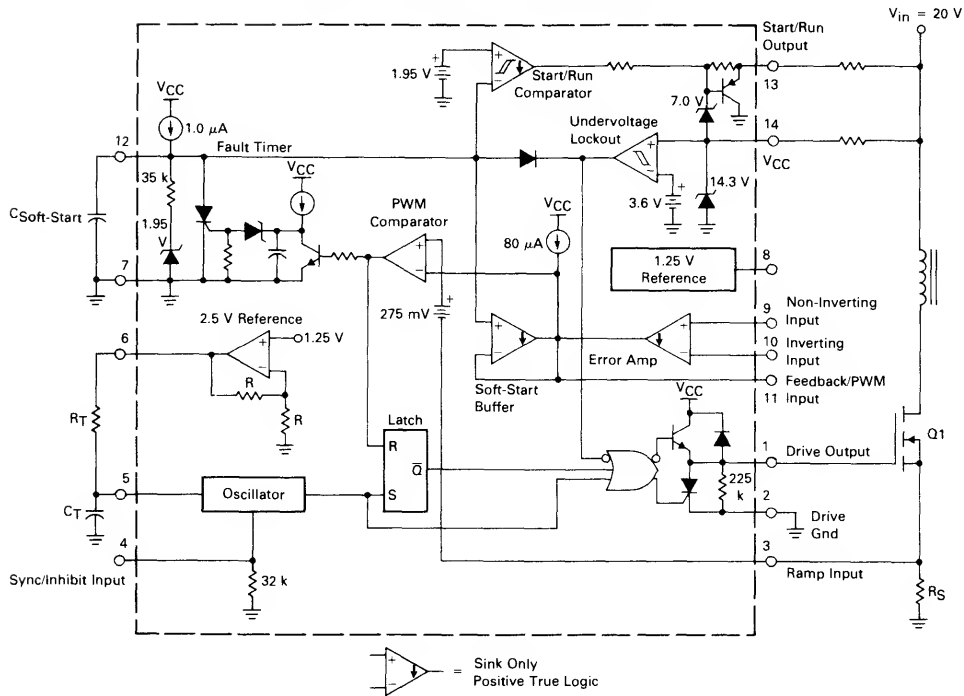
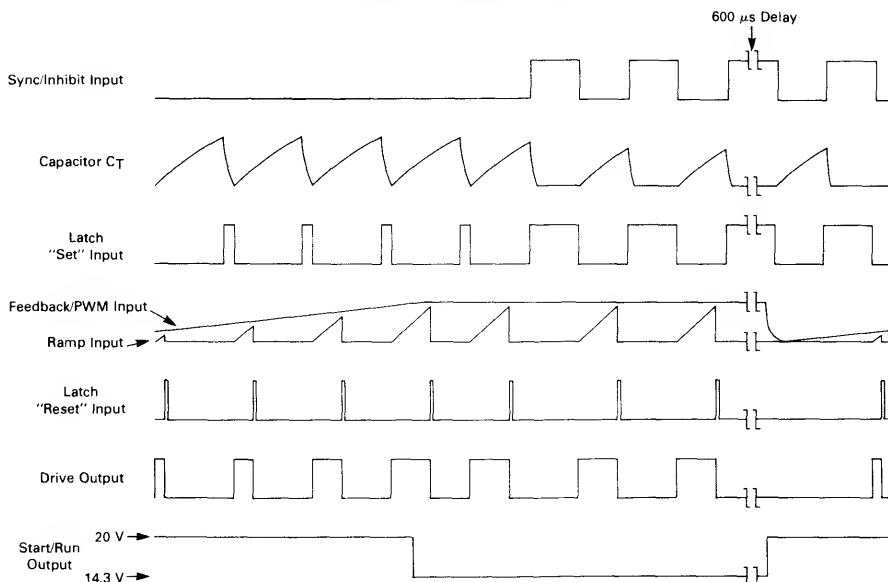


FIGURE 19 — TIMING DIAGRAM



OPERATING DESCRIPTION (continued)

current source charges the soft-start capacitor ($C_{\text{Soft-Start}}$) to an internally clamped level of 1.95 V. The rate of change of peak inductor current, during start-up, is programmed by the capacitor value selected. Either the Fault Timer or the Undervoltage Lockout can discharge the soft-start capacitor.

FAULT TIMER

This unique circuit prevents sustained operation in a lockout condition. This can occur with conventional switching control IC's when operating from a power source with a high series impedance. If the power required by the load is greater than that available from the source, the input voltage will collapse, causing the lockout condition. The Fault Timer provides automatic recovery when this condition is detected. Under normal operating conditions, the output of the PWM Comparator will reset the Latch and discharge the internal Fault Timer capacitor on a cycle-by-cycle basis. Under operating conditions where the required power into the load is greater than that available from the source (V_{IN}), the Ramp Input voltage (plus offset) will not reach the comparator threshold level (Pin 11), and the output of the PWM Comparator will remain low. If this condition persists for more than 600 μs , the Fault Timer will activate, discharging $C_{\text{Soft-Start}}$ and initiating a soft-start cycle. The power supply will operate in a skip cycle or hiccup mode until either the load power or source impedance is reduced. The minimum fault timeout is 200 μs , which limits the useful switching frequency to a minimum of 5.0 kHz.

START/RUN COMPARATOR

A bootstrap start-up circuit is included to improve system efficiency when operating from a high input voltage. The output of the Start/Run Comparator controls the state of an external transistor. A typical application is shown in Figure 21. While $C_{\text{Soft-Start}}$ is charging, start-up bias is supplied to V_{CC} (Pin 14) from V_{IN} through transistor Q2. When $C_{\text{Soft-Start}}$ reaches the 1.95 V clamp level, the Start-Run output switches low ($V_{\text{CC}} - 50 \text{ mV}$), turning off Q2. Operating bias is now derived from the auxiliary bootstrap winding of the transformer, and all drive power is efficiently converted down from V_{IN} . The start time must be long enough for the power supply output to reach regulation. This will ensure that there is sufficient bias voltage at the auxiliary bootstrap winding for sustained operation.

$$t_{\text{Start}} = \frac{1.95 \text{ V } C_{\text{Soft-Start}}}{1.0 \mu\text{A}} = 1.95 C_{\text{Soft-Start}} \text{ in } \mu\text{F}$$

The Start/Run Comparator has 350 mV of hysteresis.

The output off-state is clamped to $V_{\text{CC}} + 7.6 \text{ V}$ by the internal zener and PNP transistor base-emitter junction.

DRIVE OUTPUT AND DRIVE GROUND

The MC34129 contains a single totem-pole output stage that was specifically designed for direct drive of power MOSFETs. It is capable of up to $\pm 1.0 \text{ A}$ peak drive current and has a typical fall time of 30 ns with a 500 pF load. The totem-pole stage consists of an NPN transistor for turn-on drive and a high speed SCR for turn-off. The SCR design requires less average supply current (I_{CC}) when compared to conventional switching control IC's that use an all NPN totem-pole. The SCR accomplishes this during turn-off of the MOSFET, by utilizing the gate charge as regenerative on-bias, whereas the conventional all transistor design requires continuous base current. Conversion efficiency in low power applications is greatly enhanced with this reduction of I_{CC} . The SCR's low-state holding current (I_{H}) is typically 225 μA . An internal 225 k Ω pull-down resistor is included to shunt the Drive Output off-state leakage to ground when the Undervoltage Lockout is active. A separate Drive Ground is provided to reduce the effects of switching transient noise imposed on the Ramp Input. This feature becomes particularly useful when the $I_{\text{pk(max)}}$ clamp level is reduced. Figure 24 shows the proper implementation of the MC34129 with a current sensing power MOSFET.

UNDERVOLTAGE LOCKOUT

The Undervoltage Lockout comparator holds the Drive Output and $C_{\text{Soft-Start}}$ pins in the low state when V_{CC} is less than 3.6 V. This ensures that the MC34129 is fully functional before the output stage is enabled and a soft-start cycle begins. A built-in hysteresis of 350 mV prevents erratic output behavior as V_{CC} crosses the comparator threshold voltage. A 14.3 V zener is connected as a shunt regulator from V_{CC} to ground. Its purpose is to protect the MOSFET gate from excessive drive voltage during system start-up. An external 9.1 V zener is required when driving low threshold MOSFETs. Refer to Figure 21. The minimum operating voltage range of the IC is 4.2 V to 12 V.

REFERENCES

The 1.25 V bandgap reference is trimmed to $\pm 2.0\%$ tolerance at $T_A = 25^\circ\text{C}$. It is intended to be used in conjunction with the Error Amp. The 2.50 V reference is derived from the 1.25 V reference by an internal op amp with a fixed gain of 2.0. It has an output tolerance of $\pm 5.0\%$ at $T_A = 25^\circ\text{C}$ and its primary purpose is to supply charging current to the oscillator timing capacitor.

For further information, please refer to AN976.

FIGURE 20 — EXTERNAL DUTY CYCLE CLAMP AND MULTI UNIT SYNCHRONIZATION

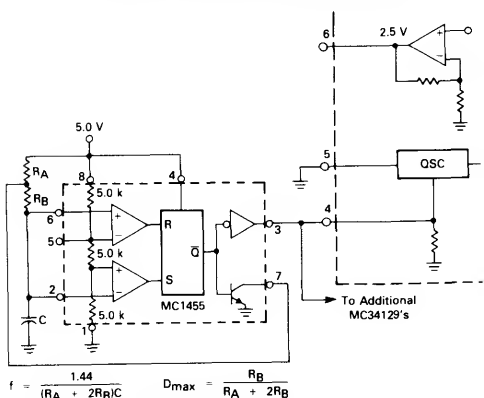


FIGURE 21 — BOOTSTRAP START-UP

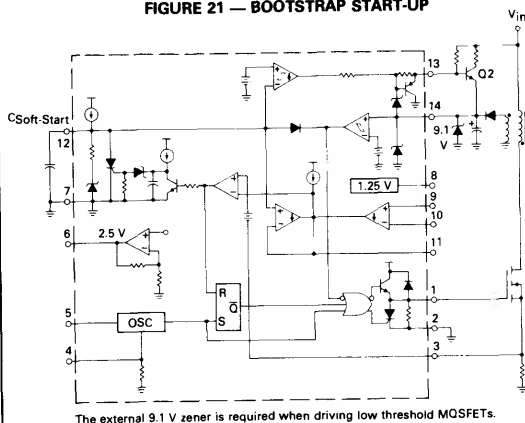


FIGURE 22 — DISCRETE STEP REDUCTION OF CLAMP LEVEL

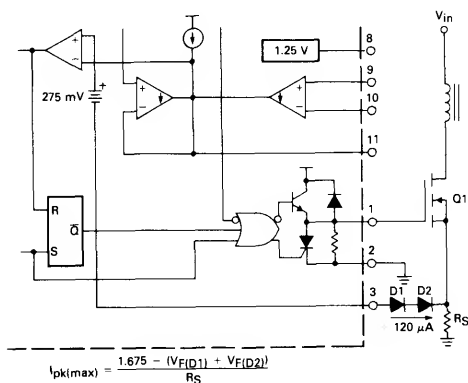


FIGURE 23 — ADJUSTABLE REDUCTION OF CLAMP LEVEL

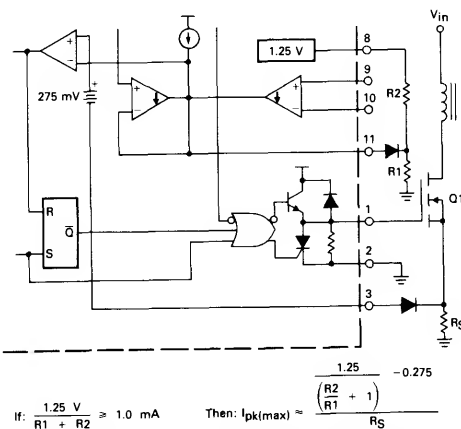
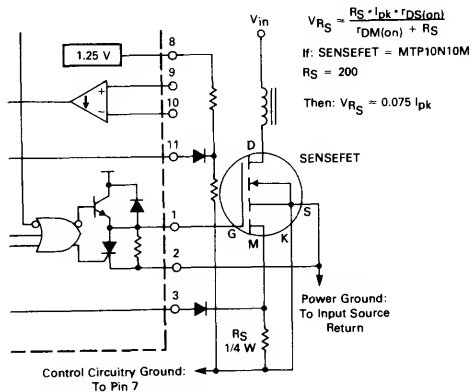
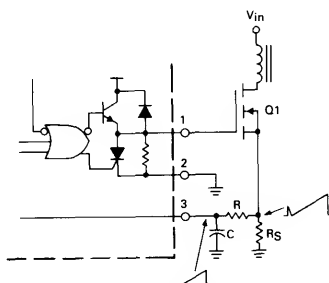


FIGURE 24 — CURRENT SENSING POWER MOSFET



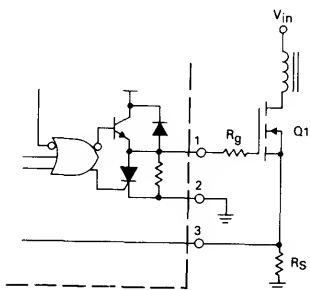
Virtually lossless current sensing can be achieved with the implementation of a SENSEFET power switch.

FIGURE 25 — CURRENT WAVEFORM SPIKE SUPPRESSION



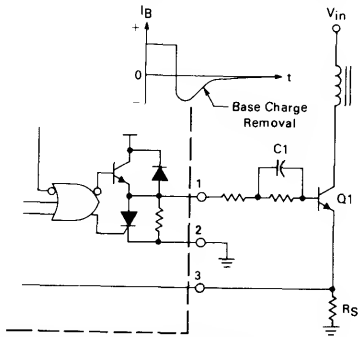
The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform.

FIGURE 26 — MOSFET PARASITIC OSCILLATIONS



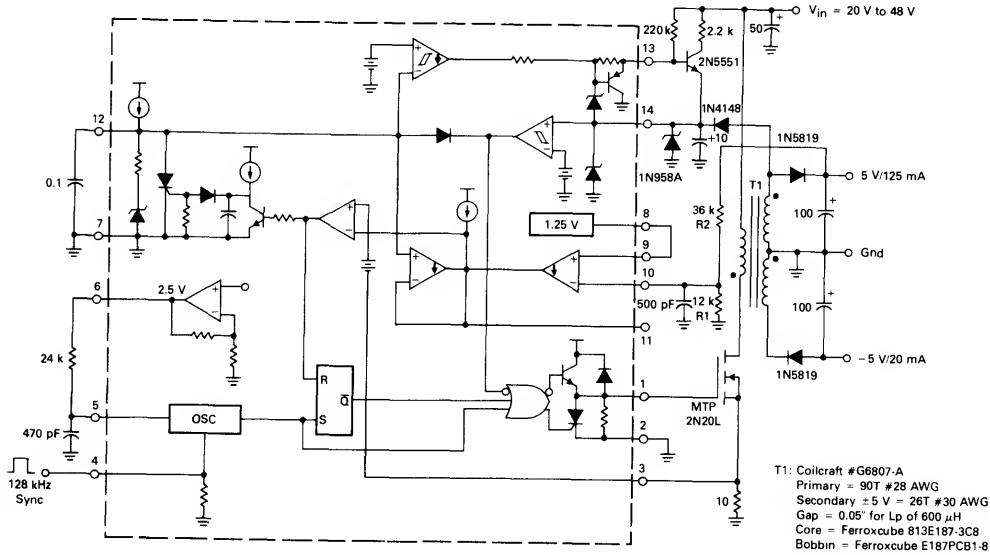
Series gate resistor R_g will damp any high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate-source circuit.

FIGURE 27 — BIPOLAR TRANSISTOR DRIVE



The totem-pole output can furnish negative base current for enhanced transistor turn-off, with the addition of capacitor C1.

FIGURE 28 — NON-ISOLATED 725 mW FLYBACK REGULATOR



T1: Coilcraft #G6807-A
Primary = 90T #28 AWG
Secondary = 5 V = 26T #30 AWG
Gap = 0.05" for Lp of 600 μ H
Core = Ferroxcube 813E187-3C8
Bobbin = Ferroxcube E187PCB1-8

Test	Conditions	Results
Line Regulation 5 V	$V_{in} = 20 \text{ V to } 40 \text{ V}$, $I_{out} 5 \text{ V} = 125 \text{ mA}$, $I_{out} -5 \text{ V} = 20 \text{ mA}$	$\Delta = 1.0 \text{ mV}$
Load Regulation 5 V	$V_{in} = 30 \text{ V}$, $I_{out} 5 \text{ V} = 0 \text{ mA to } 150 \text{ mA}$, $I_{out} -5 \text{ V} = 20 \text{ mA}$	$\Delta = 2.0 \text{ mV}$
Output Ripple 5 V	$V_{in} = 30 \text{ V}$, $I_{out} 5 \text{ V} = 125 \text{ mA}$, $I_{out} -5 \text{ V} = 20 \text{ mA}$	150 mVp-p
Efficiency	$V_{in} = 30 \text{ V}$, $I_{out} 5 \text{ V} = 125 \text{ mA}$, $I_{out} -5 \text{ V} = 20 \text{ mA}$	77%

$$V_{out} = 1.25 \left(\frac{R_2}{R_1} + 1 \right)$$

Advance Information

HIGH SPEED DUAL MOSFET DRIVERS

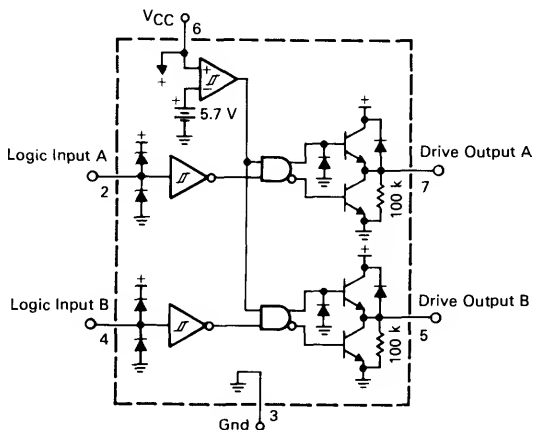
The MC34151/MC33151 is a dual inverting monolithic high speed driver specifically designed for applications that require low current digital circuitry to drive large capacitive loads with high slew rates. This device features low input current making it CMOS and LSTTL logic compatible, input hysteresis for fast output switching that is independent of input transition time, and two high current totem pole outputs ideally suited for driving power MOSFETs. Also included is an undervoltage lockout with hysteresis to prevent erratic system operation at low supply voltages.

Typical applications include switching power supplies, DC to DC converters, capacitor charge pump voltage doublers/inverters, and motor controllers.

These devices are available in dual-in-line and surface mount packages.

- Two Independent Channels with 1.5 A Totem Pole Outputs
- Output Rise and Fall Times of 15 ns with 1000 pF Load
- CMOS/LSTTL Compatible Inputs with Hysteresis
- Undervoltage Lockout with Hysteresis
- Low Standby Current
- Efficient High Frequency Operation
- Enhanced System Performance with Common Switching Regulator Control ICs
- Pin Out Equivalent to DS0026 and MMH0026

BLOCK DIAGRAM

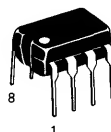


This document contains information on a new product. Specifications and information herein are subject to change without notice.

MC34151 MC33151

HIGH SPEED DUAL MOSFET DRIVERS

SILICON MONOLITHIC INTEGRATED CIRCUIT

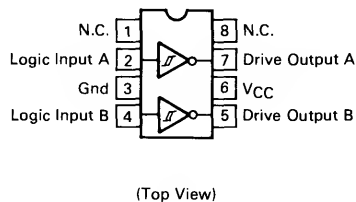


P SUFFIX
 PLASTIC PACKAGE
 CASE 626



D SUFFIX
 PLASTIC PACKAGE
 CASE 751
 (SO-8)

PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
MC34151D	0 to +70°C	SO-8 Plastic DIP
MC34151P	0 to +70°C	Plastic DIP
MC33151D	-40 to +85°C	SO-8 Plastic DIP
MC33151P	-40 to +85°C	Plastic DIP

MC34151, MC33151

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	20	V
Logic Inputs (Note 1)	V_{in}	-0.3 to V_{CC}	V
Drive Outputs (Note 2)			A
Totem Pole Sink or Source Current	I_O	1.5	
Diode Clamp Current (Drive Output to V_{CC})	$I_{O(clamp)}$	1.0	
Power Dissipation and Thermal Characteristics			
D Suffix SO-8 Package Case 751			
Maximum Power Dissipation ($\alpha T_A = 50^\circ\text{C}$)	P_D	0.56	W
Thermal Resistance Junction-to-Air	$R_{\theta JA}$	180	$^\circ\text{C/W}$
P Suffix 8-Pin Package Case 626			
Maximum Power Dissipation ($\alpha T_A = 50^\circ\text{C}$)	P_D	1.0	W
Thermal Resistance Junction-to-Air	$R_{\theta JA}$	100	$^\circ\text{C/W}$
Operating Junction Temperature	T_J	+150	$^\circ\text{C}$
Operating Ambient Temperature	T_A		$^\circ\text{C}$
MC34151		0 to +70	
MC33151		-40 to +85	
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($V_{CC} = 12\text{ V}$, for typical values $T_A = 25^\circ\text{C}$, for min/max values T_A is the operating ambient temperature range that applies [Note 3] unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
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LOGIC INPUTS

Input Threshold Voltage — High State Logic 1	V_{IH}	2.6	1.75	—	V
— Low State Logic 0	V_{IL}	—	1.58	0.8	
Input Current — High State ($V_{IH} = 2.6\text{ V}$)	I_{IH}	—	200	500	μA
— Low State ($V_{IL} = 0.8\text{ V}$)	I_{IL}	—	20	100	

DRIVE OUTPUT

Output Voltage — Low State ($I_{Sink} = 10\text{ mA}$)	V_{OL}	—	0.8	1.2	V
($I_{Sink} = 50\text{ mA}$)		—	1.1	1.5	
($I_{Sink} = 400\text{ mA}$)		—	1.7	2.5	
— High State ($I_{Source} = 10\text{ mA}$)	V_{OH}	10.5	11.2	—	
($I_{Source} = 50\text{ mA}$)		10.4	11.1	—	
($I_{Source} = 400\text{ mA}$)		9.5	10.9	—	
Output Pull-Down Resistor	R_{pD}	—	100	—	$k\Omega$

SWITCHING CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

Propagation Delay (10% Input to 10% Output, $C_L = 1.0\text{ nF}$)					ns
Logic Input to Drive Output Rise	$t_{PLH}(IN/OUT)$	—	35	100	
Logic Input to Drive Output Fall	$t_{PHL}(IN/OUT)$	—	36	100	
Drive Output Rise Time (10% to 90%) $C_L = 1.0\text{ nF}$	t_r	—	14	30	ns
$C_L = 2.5\text{ nF}$		—	31	—	
Drive Output Fall Time (90% to 10%) $C_L = 1.0\text{ nF}$	t_f	—	16	30	ns
$C_L = 2.5\text{ nF}$		—	32	—	

TOTAL DEVICE

Power Supply Current	I_{CC}				mA
Standby (Logic Inputs Grounded)		—	6.0	10	
Operating ($C_L = 1.0\text{ nF}$ Drive Outputs 1 and 2, $f = 100\text{ kHz}$)		—	10.5	15	
Operating Voltage	V_{CC}	6.5	—	18	V

NOTES:

- For optimum switching speed, the maximum input voltage should be limited to 10 V or V_{CC} , whichever is less.
- Maximum package power dissipation limits must be observed.
- Low duty cycle pulse techniques are used during test to maintain the junction temperature as close to ambient as possible.

$T_{low} = 0^\circ\text{C}$ for MC34151 $T_{high} = 70^\circ\text{C}$ for MC34151
 $= -40^\circ\text{C}$ for MC33151 $= 85^\circ\text{C}$ for MC33151

MC34151, MC33151

FIGURE 1 — SWITCHING CHARACTERISTICS TEST CIRCUIT

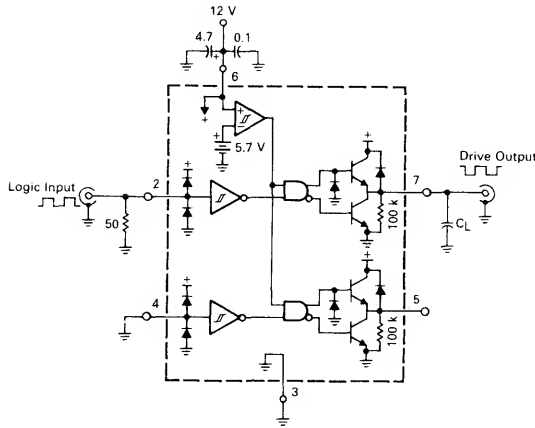


FIGURE 2 — SWITCHING WAVEFORM DEFINITIONS

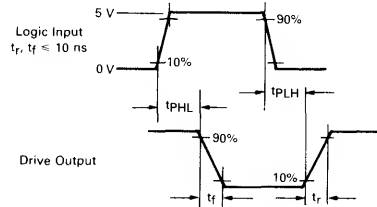


FIGURE 3 — LOGIC INPUT CURRENT versus INPUT VOLTAGE

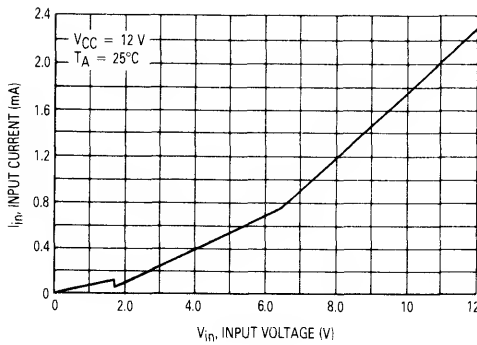


FIGURE 4 — LOGIC INPUT THRESHOLD VOLTAGE versus TEMPERATURE

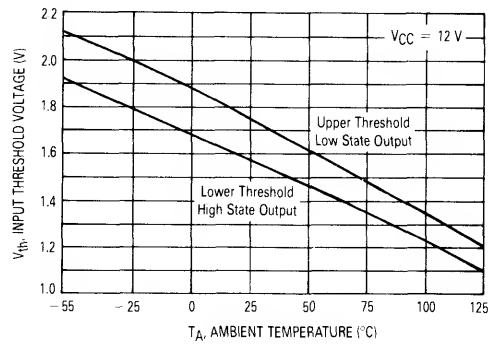


FIGURE 5 — DRIVE OUTPUT LOW TO HIGH PROPAGATION DELAY versus LOGIC INPUT OVERDRIVE VOLTAGE

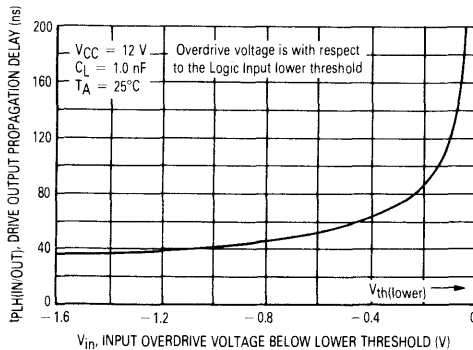


FIGURE 6 — DRIVE OUTPUT HIGH TO LOW PROPAGATION DELAY versus LOGIC INPUT OVERDRIVE VOLTAGE

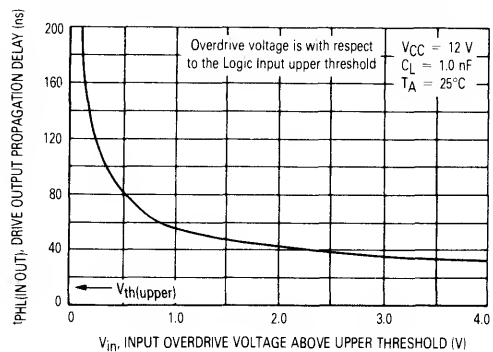


FIGURE 7 — PROPAGATION DELAY

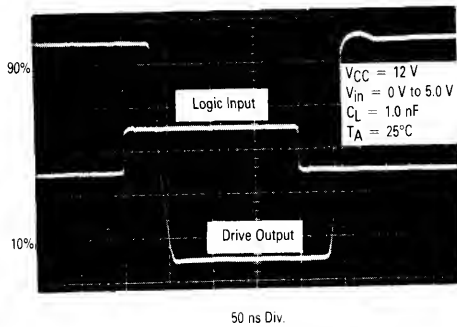


FIGURE 8 — DRIVE OUTPUT CLAMP VOLTAGE versus CLAMP CURRENT

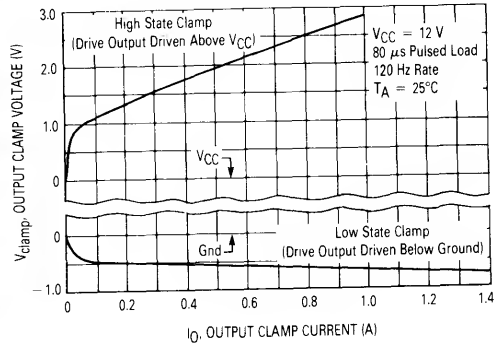


FIGURE 9 — DRIVE OUTPUT SATURATION VOLTAGE versus LOAD CURRENT

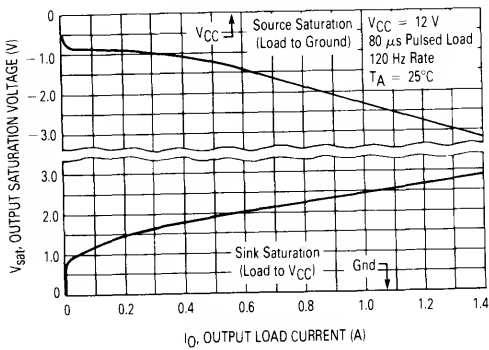


FIGURE 10 — DRIVE OUTPUT SATURATION VOLTAGE versus TEMPERATURE

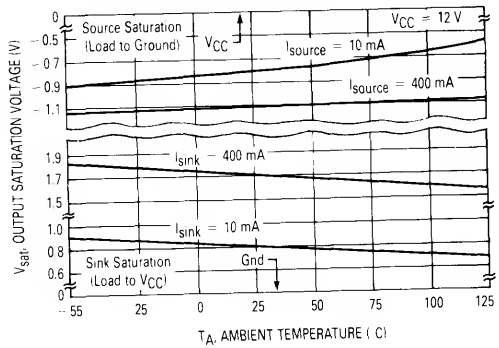


FIGURE 11 — DRIVE OUTPUT RISE TIME

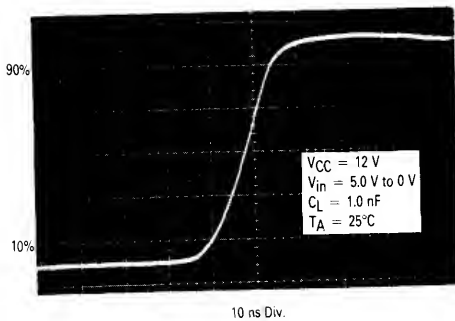


FIGURE 12 — DRIVE OUTPUT FALL TIME

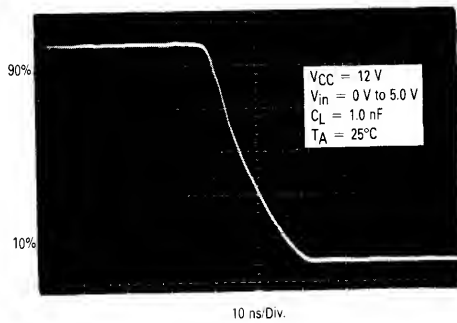


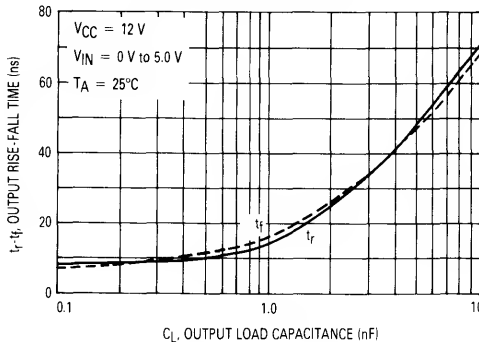
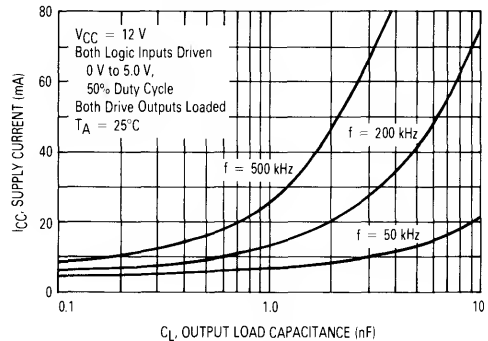
FIGURE 13 — DRIVE OUTPUT RISE AND FALL TIME
versus LOAD CAPACITANCEFIGURE 14 — SUPPLY CURRENT versus DRIVE OUTPUT
LOAD CAPACITANCE

FIGURE 15 — SUPPLY CURRENT versus INPUT FREQUENCY

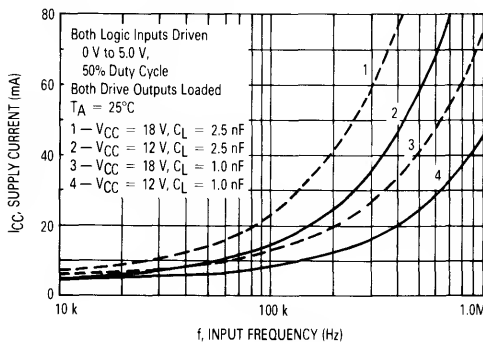
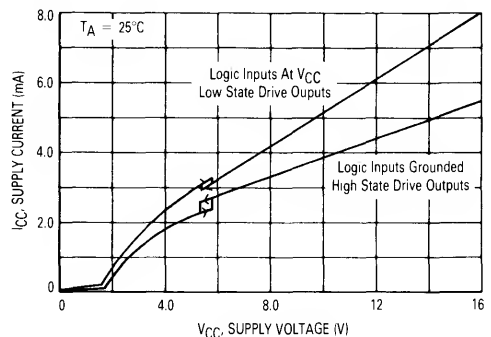


FIGURE 16 — SUPPLY CURRENT versus SUPPLY VOLTAGE



APPLICATIONS INFORMATION

Description

The MC34151 is a dual inverting high speed driver specifically designed to interface low current digital circuitry with power MOSFETs. This device is constructed with Schottky clamped Bipolar Analog technology which offers a high degree of performance and ruggedness in hostile industrial environments.

Input Stage

The Logic Inputs have 170 mV of hysteresis with the input threshold centered at 1.67 V. The input thresholds are insensitive to V_{CC} making this device directly compatible with CMOS and LSTTL logic families over its entire operating voltage range. Input hysteresis provides fast output switching that is independent of the input signal transition time, preventing output oscillations as the input thresholds are crossed. The inputs are designed to accept a signal amplitude ranging from ground to V_{CC} . This allows the output of one channel to directly drive the input of a second channel for master-slave operation.

Each input has a 30 k Ω pull-down resistor so that an unconnected open input will cause the associated Drive Output to be in a known high state.

Output Stage

Each totem pole Drive Output is capable of sourcing and sinking up to 1.5 A with a typical 'on' resistance of 2.4 Ω at 1.0 A. The low 'on' resistance allows high output currents to be attained at a lower V_{CC} than with comparative CMOS drivers. Each output has a 100 k Ω pull-down resistor to keep the MOSFET gate low when V_{CC} is less than 1.4 V. No over current or thermal protection has been designed into the device, so output shorting to V_{CC} or ground must be avoided.

Parasitic inductance in series with the load will cause the driver outputs to ring above V_{CC} during the turn-on transition, and below ground during the turn-off transition. With CMOS drivers, this mode of operation can cause a destructive output latch-up condition. The MC34151 is immune to output latch-up. The Drive Outputs contain an internal diode to V_{CC} for clamping positive voltage transients. When operating with V_{CC} at 18 volts, proper power supply bypassing must be observed

to prevent the output ringing from exceeding the maximum 20 volt device rating. Negative output transients are clamped by the internal NPN pull-up transistor. Since full supply voltage is applied across the NPN pull-up during the negative output transient, power dissipation at high frequencies can become excessive. Figures 19, 20, and 21 show a method of using external Schottky diode clamps to reduce driver power dissipation.

Undervoltage Lockout

An undervoltage lockout with hysteresis prevents erratic system operation at low supply voltages. The UVLO forces the Drive Outputs into a low state as V_{CC} rises from 1.4 V to the 5.8 V upper threshold. The lower UVLO threshold is 5.3 V, yielding about 500 mV of hysteresis.

Power Dissipation

Circuit performance and long term reliability are enhanced with reduced die temperature. Die temperature increase is directly related to the power that the integrated circuit must dissipate and the total thermal resistance from the junction to ambient. The formula for calculating the junction temperature with the package in free air is:

$$T_J = T_A + P_D (R_{\theta JA})$$

Where:

T_J = Junction Temperature
 T_A = Ambient Temperature
 P_D = Power Dissipation
 $R_{\theta JA}$ = Thermal Resistance Junction to Ambient

There are three basic components that make up total power to be dissipated when driving a capacitive load with respect to ground. They are:

$$P_D = P_Q + P_C + P_T$$

Where:

P_Q = Quiescent Power Dissipation
 P_C = Capacitive Load Power Dissipation
 P_T = Transition Power Dissipation

The quiescent power supply current depends on the supply voltage and duty cycle as shown in Figure 16. The device's quiescent power dissipation is:

$$P_Q = V_{CC} (I_{CCL} (1-D) + I_{CCH} (D))$$

Where:

I_{CCL} = Supply Current with Low State Drive Outputs
 I_{CCH} = Supply Current with High State Drive Outputs
 D = Output Duty Cycle

The capacitive load power dissipation is directly related to the load capacitance value, frequency, and Drive Output voltage swing. The capacitive load power dissipation per driver is:

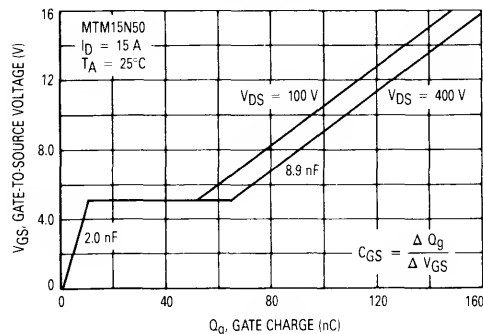
$$P_C = V_{CC} (V_{OH} - V_{OL}) C_L f$$

Where:

V_{OH} = High State Drive Output Voltage
 V_{OL} = Low State Drive Output Voltage
 C_L = Load Capacitance
 f = frequency

When driving a MOSFET, the calculation of capacitive load power P_C is somewhat complicated by the changing gate to source capacitance C_{GS} as the device switches. To aid in this calculation, power MOSFET manufacturers provide gate charge information on their data sheets. Figure 17 shows a curve of gate voltage versus gate charge for the Motorola MTM15N50. Note that there are three distinct slopes to the curve representing different input capacitance values. To completely switch the MOSFET 'on,' the gate must be brought to 10 V with respect to the source. The graph shows that a gate charge Q_g of 110 nC is required when operating the MOSFET with a drain to source voltage V_{DS} of 400 V.

FIGURE 17 — GATE-TO-SOURCE VOLTAGE versus GATE CHARGE



The capacitive load power dissipation is directly related to the required gate charge, and operating frequency. The capacitive load power dissipation per driver is:

$$P_C(\text{MOSFET}) = V_{CC} Q_g f$$

The flat region from 10 nC to 55 nC is caused by the drain-to-gate Miller capacitance, occurring while the MOSFET is in the linear region dissipating substantial amounts of power. The high output current capability of the MC34151 is able to quickly deliver the required gate charge for fast power efficient MOSFET switching. By operating the MC34151 at a higher V_{CC} , additional charge can be provided to bring the gate above 10 V. This will reduce the 'on' resistance of the MOSFET at the expense of higher driver dissipation at a given operating frequency.

The transition power dissipation is due to extremely short simultaneous conduction of internal circuit nodes when the Drive Outputs change state. The transition power dissipation per driver is approximately:

$$P_T \approx V_{CC} (1.08 V_{CC} C_L f - 8 \times 10^{-4})$$

P_T must be greater than zero.

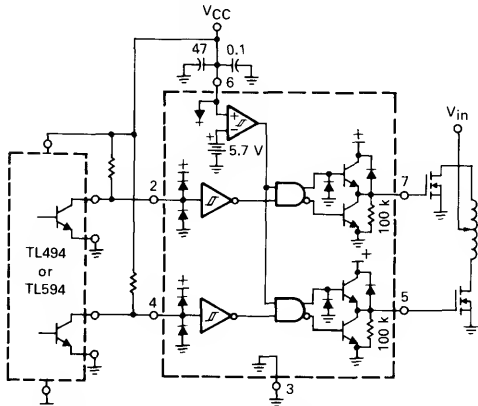
Switching time characterization of the MC34151 is performed with fixed capacitive loads. Figure 13 shows that for small capacitance loads, the switching speed is limited by transistor turn-on/off time and the slew rate of the internal nodes. For large capacitance loads, the switching speed is limited by the maximum output current capability of the integrated circuit.

Layout Considerations

High frequency printed circuit layout techniques are imperative to prevent excessive output ringing and overshoot. **Do not attempt to construct the driver circuit on wire-wrap or plug-in prototype boards.** When driving

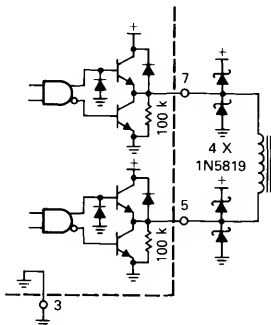
large capacitive loads, the printed circuit board must contain a low inductance ground plane to minimize the voltage spikes induced by the high ground ripple currents. All high current loops should be kept as short as possible using heavy copper runs to provide a low impedance high frequency path. For optimum drive performance, it is recommended that the initial circuit design contains dual power supply bypass capacitors connected with short leads as close to the V_{CC} pin and ground as the layout will permit. Suggested capacitors are a low inductance $0.1 \mu\text{F}$ ceramic in parallel with a $4.7 \mu\text{F}$ tantalum. Additional bypass capacitors may be required depending upon Drive Output loading and circuit layout. **Proper printed circuit board layout is extremely critical and cannot be over emphasized.**

FIGURE 18 — ENHANCED SYSTEM PERFORMANCE WITH COMMON SWITCHING REGULATORS



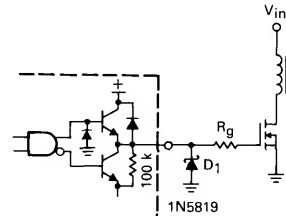
The MC34151 greatly enhances the drive capabilities of common switching regulators and CMOS/TTL logic devices.

FIGURE 20 — DIRECT TRANSFORMER DRIVE



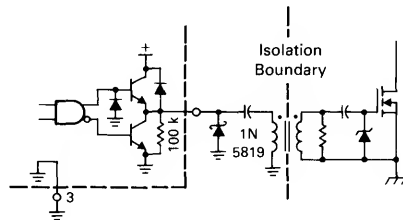
Output Schottky diodes are recommended when driving inductive loads at high frequencies. The diodes reduce the driver's power dissipation by preventing the output pins from being driven above V_{CC} and below ground.

FIGURE 19 — MOSFET PARASITIC OSCILLATIONS



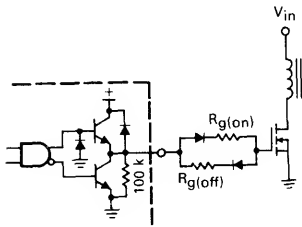
Series gate resistor R_g may be needed to damp high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate-source circuit. R_g will decrease the MOSFET switching speed. Schottky diode D_1 can reduce the driver's power dissipation due to excessive ringing, by preventing the output pin from being driven below ground.

FIGURE 21 — ISOLATED MOSFET DRIVE



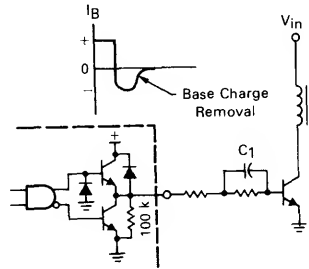
MC34151, MC33151

FIGURE 22 — CONTROLLED MOSFET DRIVE



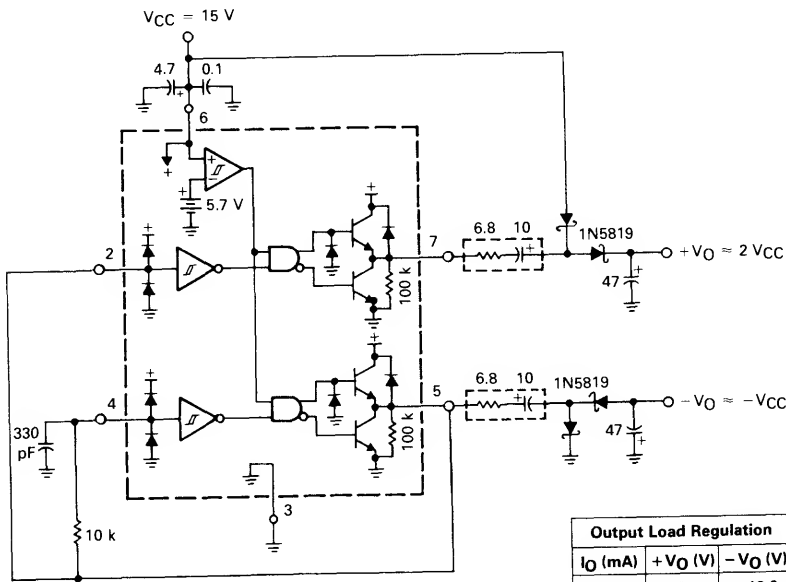
In noise sensitive applications, both conducted and radiated EMI can be reduced significantly by controlling the MOSFET's turn-on and turn-off times.

FIGURE 23 — BIPOLAR TRANSISTOR DRIVE



The totem-pole outputs can furnish negative base current for enhanced transistor turn-off, with the addition of capacitor C1.

FIGURE 24 — DUAL CHARGE PUMP CONVERTER



The capacitor's equivalent series resistance limits the Drive Output Current to 1.5 A. An additional series resistor may be required when using tantalum or other low ESR capacitors.

Output Load Regulation		
I_O (mA)	$+V_O$ (V)	$-V_O$ (V)
0	27.7	-13.3
1.0	27.4	-12.9
10	26.4	-11.9
20	25.5	-11.2
30	24.6	-10.5
50	22.6	-9.4

Product Preview

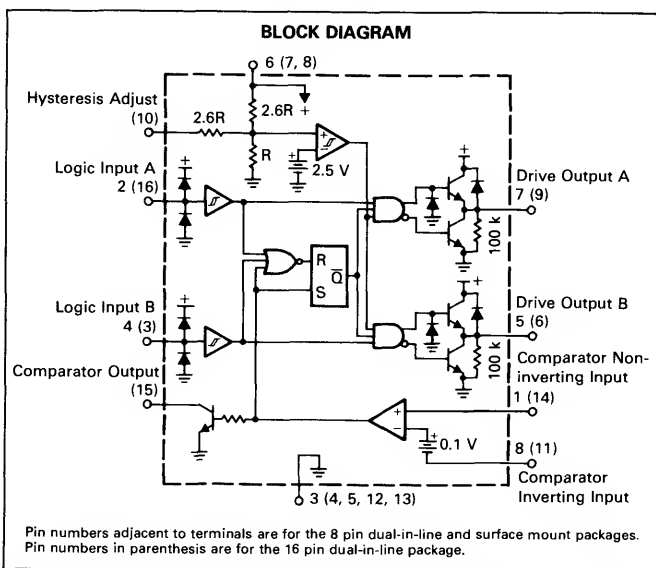
HIGH SPEED DUAL MOSFET DRIVERS

The MC34152, MC34153 series are dual high speed drivers specifically designed for applications in which low current digital signals must drive large capacitive loads with high slew rates. These devices feature low input current making them CMOS/LSTTL logic compatible, input hysteresis for fast output switching independent of input speed, and two high current totem pole outputs ideally suited for driving power MOSFETs. Also included are system protective features consisting of a latching comparator for cycle-by-cycle current limiting, and undervoltage lockout with hysteresis to prevent erratic operation at low supply voltages.

Typical applications include switching power supplies, DC-to-DC converters, capacitor charge pump voltage doublers/inverters, and motor controllers.

These devices are available in dual-in-line and surface mount packages.

- Two Independent Channels with 1.5 A Totem Pole Outputs
- Output Rise and Fall Times of 15 ns with 1000 pF Load
- CMOS/LSTTL Compatible Inputs with Hysteresis
- Latching Comparator for Cycle-By-Cycle Current Limiting
- Undervoltage Lockout with Hysteresis
- Low Standby Current
- Direct Interface with Motorola SENSEFET Products
- Enhanced System Performance with Common Switching Regulator Control ICs

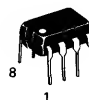


This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

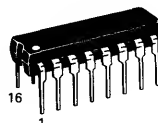
MC34152, MC33152 MC34153, MC33153

HIGH SPEED DUAL MOSFET DRIVERS

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
 PLASTIC PACKAGE
 CASE 626

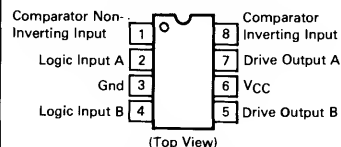


P SUFFIX
 PLASTIC PACKAGE
 CASE 648C

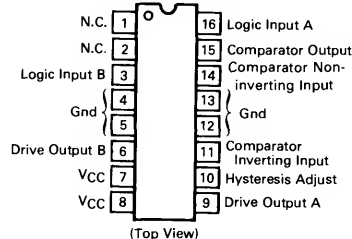


D SUFFIX
 PLASTIC PACKAGE
 CASE 751
 (SO-8)

PIN CONNECTIONS MC34152, MC33152



MC34153, MC33153



ORDERING INFORMATION

Device	Temperature Range	Package
MC34152D	0 to +70°C	SO-8 Plastic DIP
MC34152P	0 to +70°C	Plastic DIP
MC33152D	-40 to +85°C	SO-8 Plastic DIP
MC33152P	-40 to +85°C	Plastic DIP
MC34153P	0 to +70°C	Plastic DIP
MC33153P	-40 to +85°C	Plastic DIP

FIGURE 1 — SWITCHING CHARACTERISTIC TEST CIRCUIT

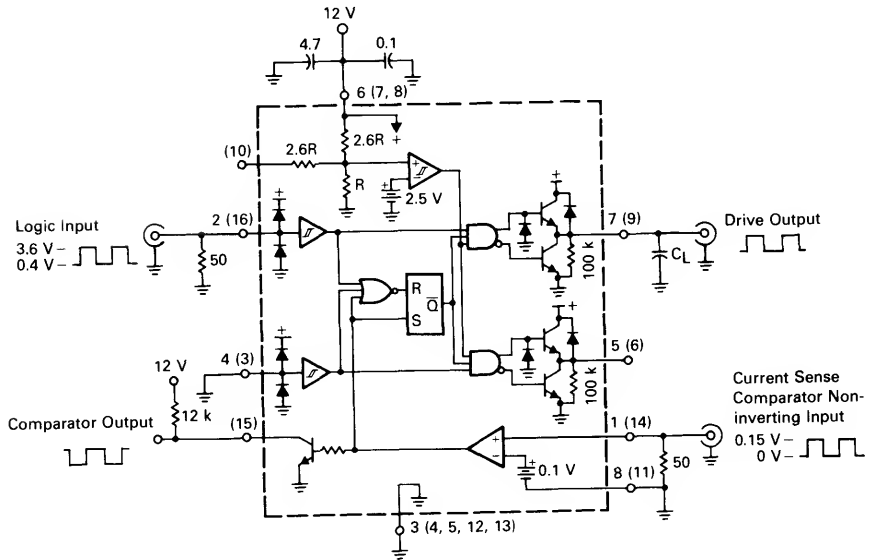


FIGURE 2 — SWITCHING WAVEFORM DEFINITIONS

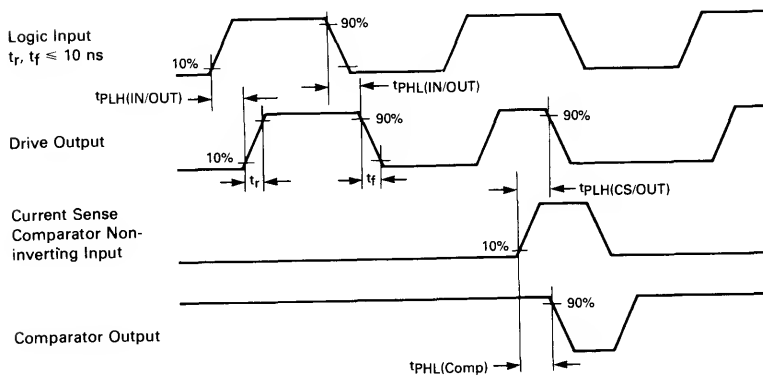


FIGURE 3 — ENHANCED SYSTEM PERFORMANCE WITH COMMON SWITCHING REGULATORS

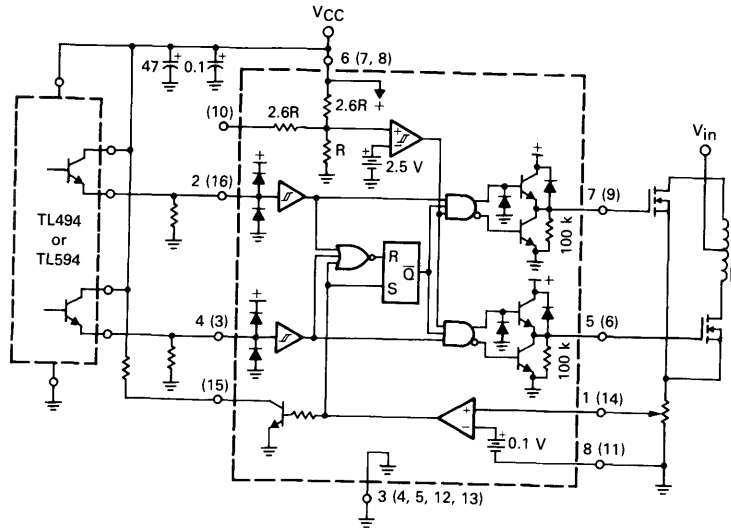


FIGURE 4 — TIMING DIAGRAM

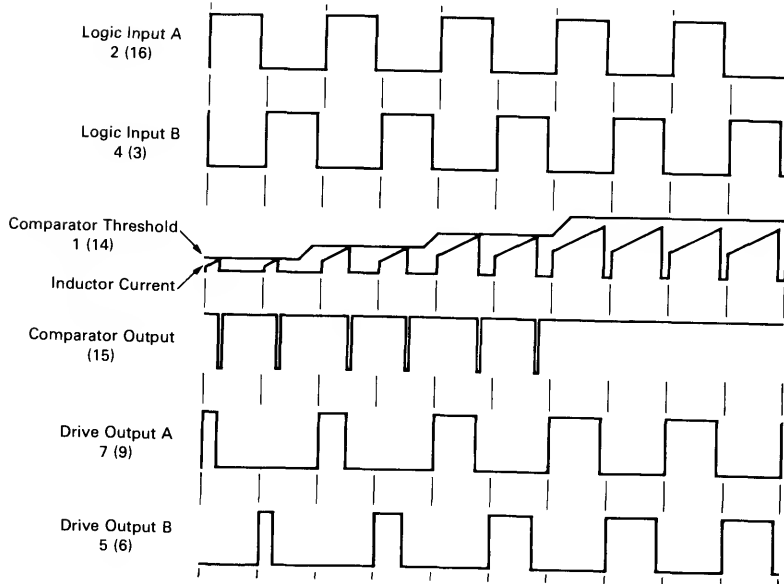
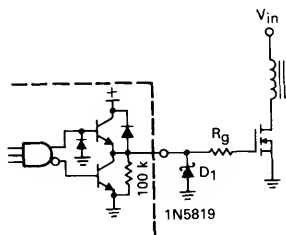
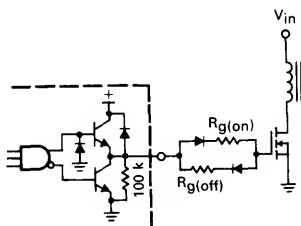


FIGURE 5 — MOSFET PARASITIC OSCILLATIONS



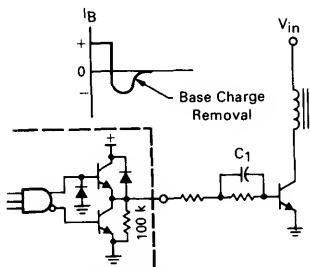
Series gate resistor R_g may be needed to damp high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate-source circuit. R_g will decrease the MOSFET switching speed. Schottky diode D_1 can reduce the driver's power dissipation due to excessive ringing, by preventing the output pin from being driven below ground.

FIGURE 7 — CONTROLLED MOSFET DRIVE



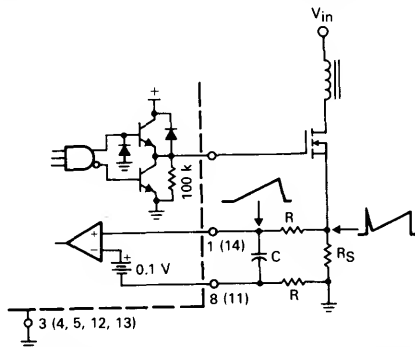
In noise sensitive applications, both conducted and radiated EMI can be reduced significantly by controlling the MOSFET's turn-on and turn-off times.

FIGURE 9 — BIPOLAR TRANSISTOR DRIVE



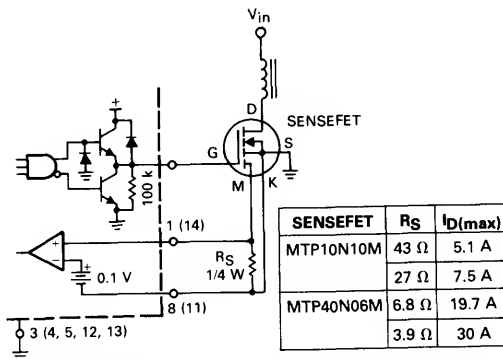
The totem-pole output can furnish negative base current for enhanced transistor turn-off, with the addition of capacitor C_1 .

FIGURE 6 — CURRENT WAVEFORM SPIKE SUPPRESSION



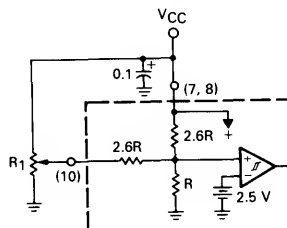
The addition of the RC filter will eliminate false triggering of the current sense comparator. The comparator inverting input must be connected to the ground side of R_S through R using a single point ground as shown. R_S must be a low inductance type resistor.

FIGURE 8 — CURRENT SENSING POWER MOSFET



Virtually lossless current sensing can be achieved with the implementation of a SENSEFET power switch. For proper operation, the mirror and Kelvin pins must be connected as shown.

FIGURE 10 — ADJUSTABLE UNDERVOLTAGE LOCKOUT THRESHOLD



The MC34153 undervoltage lockout threshold can be modified with resistor R_1 . The typical range is 5.7 V to 11.4 V.

FIGURE 11 — DIRECT TRANSFORMER DRIVE

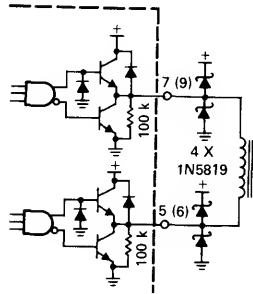
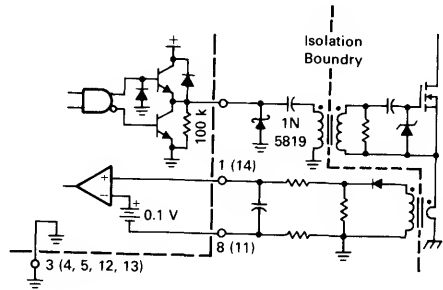
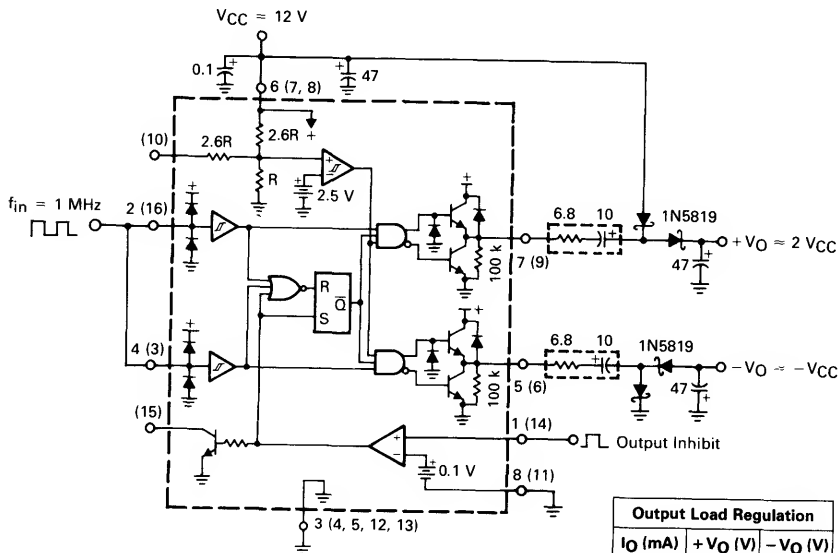


FIGURE 12 — ISOLATED MOSFET DRIVE



Output Schottky diodes are recommended when driving inductive loads at high frequencies. The diodes reduce the driver's power dissipation by preventing the output pins from being driven above V_{CC} and below ground.

FIGURE 13 — DUAL CHARGE PUMP CONVERTER



The capacitor's equivalent series resistance limits the Drive Output Current to 1.5 A. An additional series resistor may be required when using tantalum or other low ESR capacitors.

Output Load Regulation		
I_O (mA)	$+V_O$ (V)	$-V_O$ (V)
0	27.7	-13.3
1	27.4	-12.9
10	26.4	-11.9
20	25.5	-11.2
30	24.6	-10.5
50	22.6	-9.4

Advance Information

MICROPROCESSOR VOLTAGE REGULATOR AND SUPERVISORY CIRCUIT

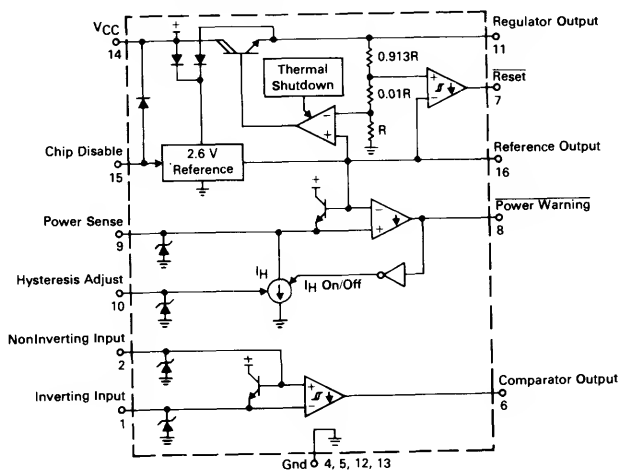
The MC34160 Series is a voltage regulator and supervisory circuit containing many of the necessary monitoring functions required in microprocessor based systems. It is specifically designed for appliance and industrial applications, offering the designer a cost effective solution with minimal external components. These integrated circuits feature a 5.0 V/100 mA regulator with short circuit current limiting, pinned out 2.6 V bandgap reference, low voltage reset comparator, power warning comparator with programmable hysteresis, and an uncommitted comparator with programmable hysteresis, and an uncommitted comparator ideally suited for microprocessor line synchronization.

Additional features include a chip disable input for low standby current, and internal thermal shutdown for over temperature protection.

These devices are contained in a 16 pin dual-in-line heat tab plastic package for improved thermal conduction.

- 5.0 Volt Regulator Output Current in Excess of 100 mA
- Internal Short Circuit Current Limiting
- Pinned Out 2.6 V Reference
- Low Voltage Reset Comparator
- Power Warning Comparator with Programmable Hysteresis
- Uncommitted Comparator
- Low Standby Current
- Internal Thermal Shutdown Protection
- Heat Tab Power Package

REPRESENTATIVE BLOCK DIAGRAM

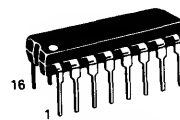


This document contains information on a new product. Specifications and information herein are subject to change without notice.

MC34160
MC33160

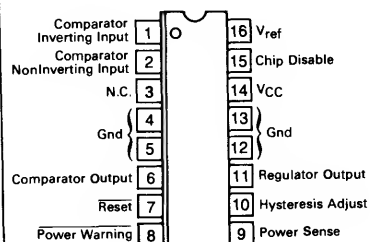
MICROPROCESSOR VOLTAGE REGULATOR/ SUPERVISORY CIRCUIT

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**



P SUFFIX
PLASTIC PACKAGE
CASE 648C

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC34160P	0°C to +70°C	Plastic DIP
MC33160P	-40°C to +85°C	Plastic DIP

MAXIMUM RATING

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	V
Chip Disable Input Voltage (Pin 15, Note 1)	V_{CD}	-0.3 to V_{CC}	V
Comparator Input Current (Pin 1, 2, 9)	I_{in}	-2.0 to +2.0	mA
Comparator Output Voltage (Pin 6, 7, 8)	V_O	40	V
Comparator Output Sink Current (Pin 6, 7, 8)	I_{Sink}	10	mA
Power Dissipation and Thermal Characteristics			
Maximum Power Dissipation @ $T_A = 70^\circ\text{C}$	P_D	1000	mW
Thermal Resistance Junction to Air	$R_{\theta JA}$	80	$^\circ\text{C/W}$
Thermal Resistance Junction to Case (Pin 4, 5, 12, 13)	$R_{\theta JC}$	15	$^\circ\text{C/W}$
Operating Junction Temperature	T_J	+150	$^\circ\text{C}$
Operating Ambient Temperature	T_A	0 to +70 -40 to +85	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($V_{CC} = 30\text{ V}$, $I_O = 10\text{ mA}$, $I_{ref} = 100\text{ }\mu\text{A}$) For typical values $T_A = 25^\circ\text{C}$, for min/max values T_A is the operating ambient temperature range that applies [Notes 2 and 3] unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
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REGULATOR SECTION

Total Output Variation ($V_{CC} = 7.0\text{ V to }40\text{ V}$, $I_O = 1.0\text{ mA to }100\text{ mA}$, $T_A = T_{low}\text{ to }T_{high}$)	V_O	4.75	5.0	5.25	V
Line Regulation ($V_{CC} = 7.0\text{ V to }40\text{ V}$, $T_A = 25^\circ\text{C}$)	Reg_{line}	—	5.0	40	mV
Load Regulation ($I_O = 1.0\text{ mA to }100\text{ mA}$, $T_A = 25^\circ\text{C}$)	Reg_{load}	—	20	50	mV
Ripple Rejection ($V_{CC} = 25\text{ V to }35\text{ V}$, $I_O = 40\text{ mA}$, $f = 120\text{ Hz}$, $T_A = 25^\circ\text{C}$)	RR	50	65	—	dB

REFERENCE SECTION

Total Output Variation ($V_{CC} = 7.0\text{ V to }40\text{ V}$, $I_O = 0.1\text{ mA to }2.0\text{ mA}$, $T_A = T_{low}\text{ to }T_{high}$)	V_{ref}	2.47	2.6	2.73	V
Line Regulation ($V_{CC} = 5.0\text{ V to }40\text{ V}$, $T_A = 25^\circ\text{C}$)	Reg_{line}	—	2.0	20	mV
Load Regulation ($I_O = 0.1\text{ mA to }2.0\text{ mA}$, $T_A = 25^\circ\text{C}$)	Reg_{load}	—	4.0	30	mV

RESET COMPARATOR

Threshold Voltage					
High State Output (Pin 11 Increasing)	V_{IH}	—	($V_O - 0.11$)	($V_O - 0.05$)	V
Low State Output (Pin 11 Decreasing)	V_{IL}	4.55	($V_O - 0.18$)	—	
Hysteresis	V_H	0.02	0.07	—	
Output Sink Saturation ($V_{CC} = 4.5\text{ V}$, $I_{Sink} = 2.0\text{ mA}$)	V_{OL}	—	—	0.4	V
Output Off-State Leakage ($V_{OH} = 40\text{ V}$)	I_{OH}	—	—	4.0	μA

Notes:

- The maximum voltage range is -0.3 V to V_{CC} or +35 V, whichever is less.
- $T_{low} = 0^\circ\text{C}$ for MC34160
= -40 $^\circ\text{C}$ for MC33160
 $T_{high} = +70^\circ\text{C}$ for MC34160
= +85 $^\circ\text{C}$ for MC33160
- Low duty cycle pulse testing techniques are used during test to maintain junction temperature as close to ambient as possible.

MC34160, MC33160

ELECTRICAL CHARACTERISTICS — Continued ($V_{CC} = 30\text{ V}$, $I_O = 10\text{ mA}$, $I_{ref} = 100\text{ }\mu\text{A}$) For typical values $T_A = 25^\circ\text{C}$, for min/max values T_A is the operating ambient temperature range that applies [Notes 2 and 3] unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER WARNING COMPARATOR					
Input Offset Voltage	V_{IO}	—	1.2	10	mV
Input Bias Current ($V_{Pin\ 9} = 3.0\text{ V}$)	I_{IB}	—	—	0.5	μA
Input Hysteresis Current ($V_{Pin\ 9} = V_{ref} - 100\text{ mV}$)	I_H	40	50	60	μA
$R_{Pin\ 10} = 24\text{ k}$		4.5	7.5	11	
$R_{Pin\ 10} = \infty$		—	—	—	
Output Sink Saturation ($I_{Sink} = 2.0\text{ mA}$)	V_{OL}	—	0.13	0.4	V
Output Off-State Leakage ($V_{OH} = 40\text{ V}$)	I_{OH}	—	—	4.0	μA
UNCOMMITTED COMPARATOR					
Input Offset Voltage (Output Transition Low to High)	V_{IO}	—	—	20	mV
Input Hysteresis Voltage (Output Transition High to Low)	I_H	140	200	260	mV
Input Bias Current ($V_{Pin\ 1, 2} = 2.6\text{ V}$)	I_{IB}	—	—	-1.0	μA
Input Common-Mode Voltage Range	V_{ICR}	0.6 to 5.0	—	—	V
Output Sink Saturation ($I_{Sink} = 2.0\text{ mA}$)	V_{OL}	—	0.13	0.4	V
Output Off-State Leakage ($V_{OH} = 40\text{ V}$)	I_{OH}	—	—	4.0	μA
TOTAL DEVICE					
Chip Disable Threshold Voltage (Pin 15)					V
High State (Chip Disabled)	V_{IH}	2.5	—	—	
Low State (Chip Enabled)	V_{IL}	—	—	0.8	
Chip Disable Input Current (Pin 15)					μA
High State ($V_{in} = 2.5\text{ V}$)	I_{IH}	—	—	100	
Low State ($V_{in} = 0.8\text{ V}$)	I_{IL}	—	—	30	
Chip Disable Input Resistance (Pin 15)	R_{in}	50	100	—	$\text{k}\Omega$
Operating Voltage Range	V_{CC}				V
V_O (Pin 11) Regulated		7.0 to 40	—	—	
V_{ref} (Pin 16) Regulated		5.0 to 40	—	—	
Power Supply Current	I_{CC}				mA
Standby (Chip Disable High State)		—	0.18	0.35	
Operating (Chip Disable Low State)		—	1.5	3.0	

FIGURE 1 — REGULATOR OUTPUT VOLTAGE CHANGE versus SOURCE CURRENT

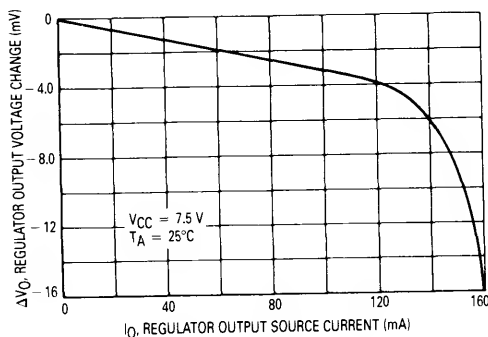


FIGURE 2 — REFERENCE AND REGULATOR OUTPUT versus SUPPLY VOLTAGE

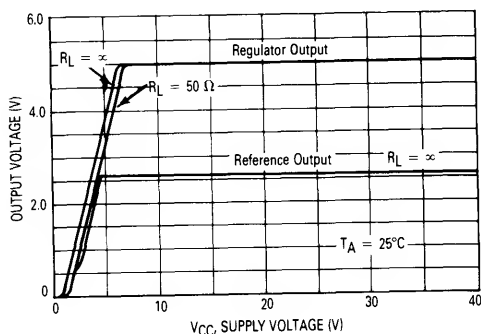


FIGURE 3 — REFERENCE OUTPUT VOLTAGE CHANGE versus SOURCE CURRENT

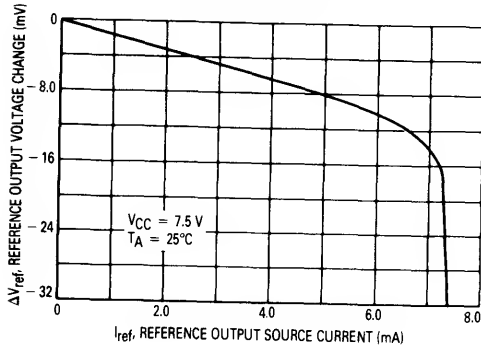


FIGURE 4 — POWER WARNING Hysteresis CURRENT versus PROGRAMMING RESISTOR

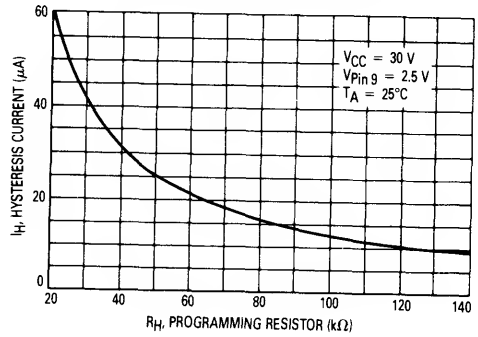


FIGURE 5 — POWER WARNING COMPARATOR DELAY versus TEMPERATURE

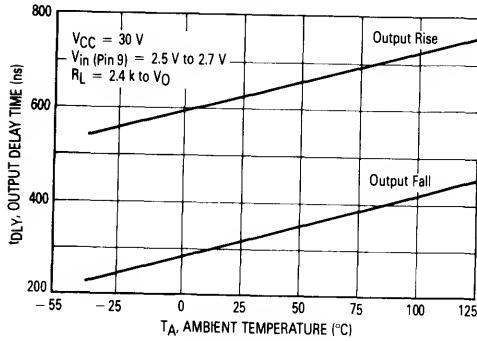


FIGURE 6 — UNCOMMITTED COMPARATOR DELAY versus TEMPERATURE

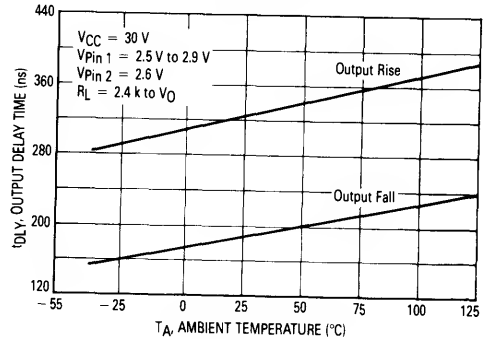


FIGURE 7 — COMPARATOR OUTPUT SATURATION versus SINK CURRENT

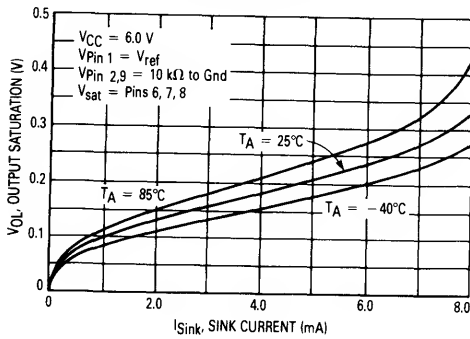
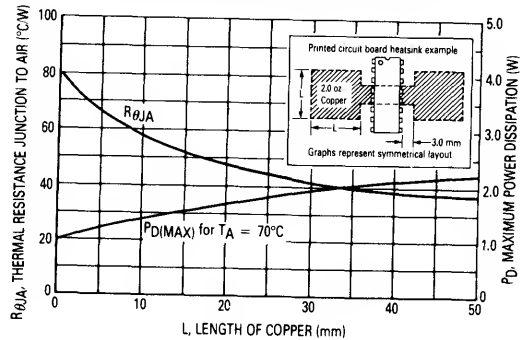


FIGURE 8 — THERMAL RESISTANCE AND MAXIMUM POWER DISSIPATION versus P.C.B. COPPER LENGTH



MC34160, MC33160

PIN FUNCTION DESCRIPTION

Pin No.	Function	Description
1	Comparator Inverting Input	This is the Uncommitted Comparator Inverting input. It is typically connected to a resistor divider to monitor a voltage.
2	Comparator Noninverting Input	This is the Uncommitted Comparator Noninverting input. It is typically connected to a reference voltage.
3	N.C.	No connection. This pin is not internally connected.
4,5,12,13	Gnd	These pins are the control circuit grounds and are connected to the source and load ground returns. They are part of the IC lead frame and can be used for heatsinking.
6	Comparator Output	This is the Uncommitted Comparator output. It is an open collector sink-only output requiring a pull-up resistor.
7	$\overline{\text{Reset}}$	This is the $\overline{\text{Reset}}$ Comparator output. It is an open collector sink-only output requiring a pull-up resistor.
8	$\overline{\text{Power Warning}}$	This is the $\overline{\text{Power Warning}}$ Comparator output. It is an open collector sink-only output requiring a pull-up resistor.
9	Power Sense	This is the $\overline{\text{Power Warning}}$ Comparator noninverting input. It is typically connected to a resistor divider to monitor the input power source voltage.
10	Hysteresis Adjust	The $\overline{\text{Power Warning}}$ Comparator hysteresis is programmed by a resistor connected from this pin to ground.
11	Regulator Output	This is the 5.0 V Regulator output.
14	V _{CC}	This pin is the positive supply input of the control IC.
15	Chip Disable	This input is used to switch the IC into a standby mode turning off all outputs.
16	V _{ref}	This is the 2.6 V Reference output. It is intended to be used in conjunction with the Power Warning and Uncommitted comparators.

3

OPERATING DESCRIPTION

The MC34160 series is a monolithic voltage regulator and supervisory circuit containing many of the necessary monitoring functions required in microprocessor based systems. It is specifically designed for appliance and industrial applications, offering the designer a cost effective solution with minimal external components. These devices are specified for operation over an input voltage of 7.0 V to 40 V, and with a junction temperature of -40°C to $+150^{\circ}\text{C}$. A typical microprocessor application is shown in Figure 9.

Regulator

The 5.0 V regulator is designed to source in excess of 100 mA output current and is short circuit protected. The output has a guaranteed tolerance of $\pm 5.0\%$ over line, load, and temperature. Internal thermal shutdown circuitry is included to limit the maximum junction temperature to a safe level. When activated, typically at 170°C , the regulator output turns off.

In specific situations a combination of input and output bypass capacitors may be required for regulator

stability. If the regulator is located an appreciable distance ($\geq 4"$) from the supply filter, an input bypass capacitor (C_{IN}) of 0.33 μF or greater is suggested. Output capacitance values of less than 5.0 nF may cause regulator instability at light load (≤ 1.0 mA) and cold temperature. An output bypass capacitor of 0.1 μF or greater is recommended to ensure stability under all load conditions. The capacitors selected must provide good high frequency characteristics.

Good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator does not have external sense inputs.

Reference

The 2.6 V bandgap reference is short circuit protected and has a guaranteed output tolerance of $\pm 5.0\%$ over line, load, and temperature. It is intended to be used in conjunction with the Power Warning and Uncommitted Comparator. The reference can source in excess of 2.0 mA and sink a maximum of 10 μA . For additional current sinking capability, an external load resistor to ground must be used.

Reference biasing is internally derived from either V_{CC} or V_O , allowing proper operation if either drops below nominal.

Chip Disable

This input is used to switch the IC into a standby mode. When activated, internal biasing for the entire die is removed causing all outputs to turn off. This reduces the power supply current (I_{CC}) to less than 0.3 mA.

Comparators

Three separate comparators are incorporated for voltage monitoring. Their outputs can provide diagnostic information to the microprocessor, preventing system malfunctions.

The Reset Comparator Inverting Input is internally connected to the 2.6 V reference while the Noninverting Input monitors V_O . The Reset Output is active low when V_O falls approximately 180 mV below its regulated voltage. To prevent erratic operation when crossing the comparator threshold, 70 mV of hysteresis is provided.

The Power Warning Comparator is typically used to detect an impending loss of system power. The Inverting Input is internally connected to the reference, fixing the threshold at 2.6 V. The input power source V_{IN} is monitored by the Noninverting Input through the R_1/R_2 divider (Figure 9). This input features an adjustable 10 μA to 50 μA current sink I_H that is programmed by the value selected for resistor R_H . A default current of 6.5 μA is provided if R_H is omitted. When the comparator input falls below 2.6 V, the current sink is activated.

This produces hysteresis if V_{IN} is monitored through a series resistor (R_1). The comparator thresholds are defined as follows:

$$V_{th(lower)} = V_{ref} \left(1 + \frac{R_1}{R_2} \right) - I_{IB} R_1$$

$$V_{th(upper)} = V_{ref} \left(1 + \frac{R_1}{R_2} \right) + I_H R_1$$

The nominal hysteresis current I_H equals 1.2 V/ R_H (Figure 4).

The Uncommitted Comparator can be used to synchronize the microprocessor with the ac line signal for timing functions, or for synchronous load switching. It can also be connected as a line loss detector as shown in Figure 10. The comparator contains 200 mV of hysteresis preventing erratic output behavior when crossing the input threshold.

The Power Warning and Uncommitted Comparators each have a transistor base-emitter connected across their inputs. The base input normally connects to a voltage reference while the emitter input connects to the voltage to be monitored. The transistor limits the negative excursion on the emitter input to -0.7 V below the base input by supplying current from V_{CC} . This clamp current will prevent forward biasing the IC substrate. Zener diodes are connected to the comparator inputs to enhance the IC's electrostatic discharge capability. Resistors R_1 and R_{IN} must limit the input current to a maximum of ± 2.0 mA.

Each comparator output consists of an open collector NPN transistor capable of sinking 2.0 mA with a saturation voltage less than 0.4 V, and standing off 40 V with minimal leakage. Internal bias for the Reset and Power Warning Comparators is derived from either V_{CC} or the regulator output to ensure functionality when either is below nominal.

Heat Tab Package

The MC34160 is contained in a 16 lead plastic dual-in-line package in which the die is mounted on a special Heat Tab copper alloy lead frame. This tab consists of the four center ground pins that are specifically designed to improve thermal conduction from the die to the surrounding air. The pictorial in Figure 8 shows a simple but effective method of utilizing the printed circuit board medium as a heat dissipator by soldering these tabs to an adequate area of copper foil. This permits the use of standard board layout and mounting practices while having the ability to more than halve the junction to air thermal resistance. The example and graph are for a symmetrical layout on a single sided board with one ounce per square foot copper.

FIGURE 9 — TYPICAL MICROPROCESSOR APPLICATION

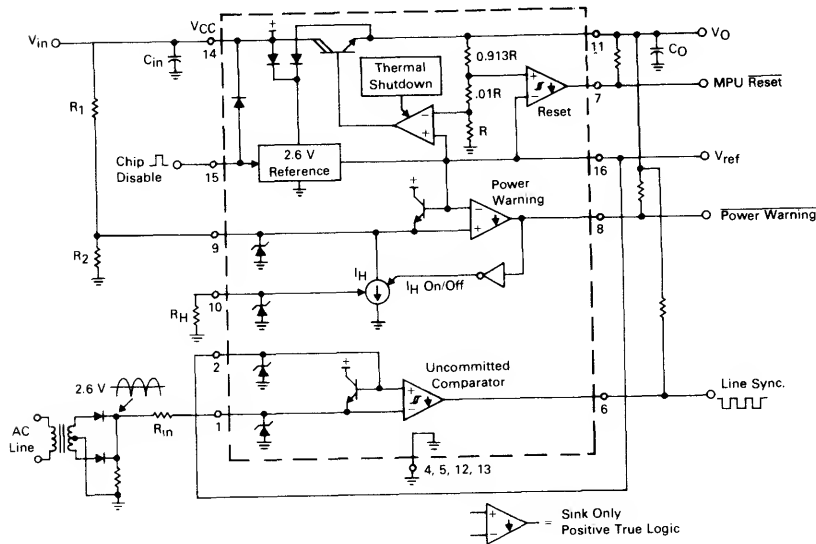
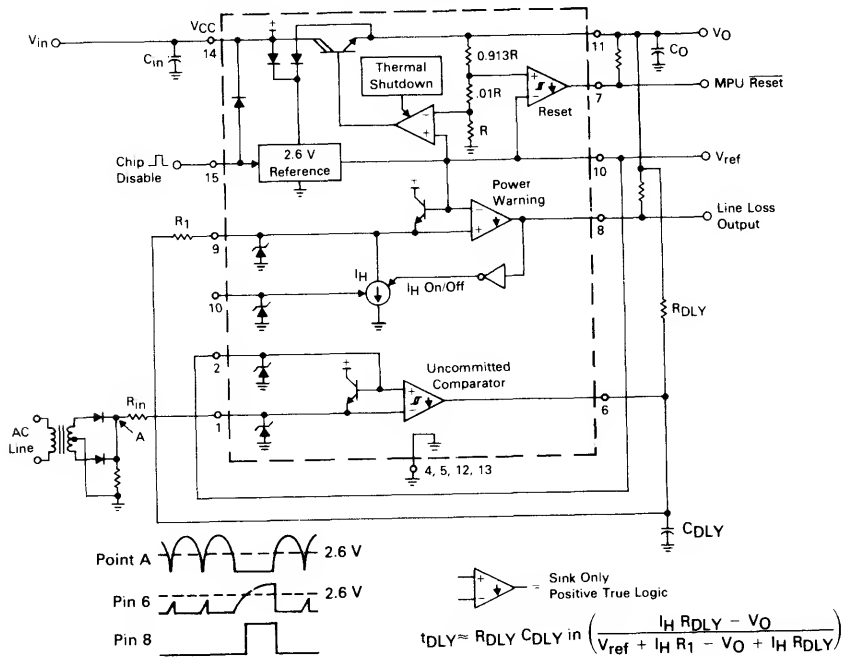
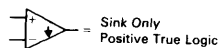


FIGURE 10 — LINE LOSS DETECTOR APPLICATION



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FIGURE 11 — TIME DELAYED MICROPROCESSOR RESET



Advance Information

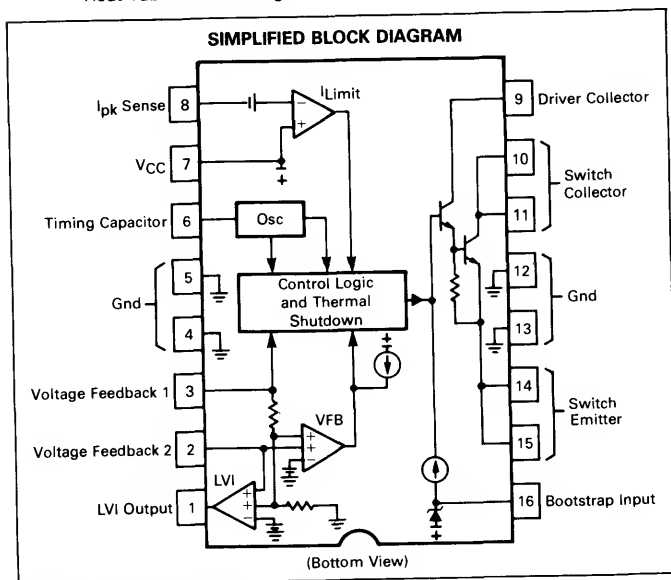
POWER SWITCHING REGULATORS

The MC34163 series are monolithic power switching regulators that contain the primary functions required for DC-to-DC converters. This series was specifically designed to be incorporated in Step-Up, Step-Down, and Voltage-Inverting applications with a minimum number of external components.

These devices consist of two high gain voltage feedback comparators, temperature compensated reference, controlled duty cycle oscillator, driver with bootstrap capability for increased efficiency, and a high current output switch. Protective features consist of cycle-by-cycle current limiting, and internal thermal shutdown. Also included is a low voltage indicator output designed to interface with microprocessor based systems.

These devices are contained in a 16 pin dual-in-line heat tab plastic package for improved thermal conduction.

- Output Switch Current in Excess of 3.0 A
- Operation from 2.5 V to 40 V Input
- Low Standby Current
- Precision 2% Reference
- Controlled Duty Cycle Oscillator
- Driver with Bootstrap Capability for Increased Efficiency
- Cycle-By-Cycle Current Limiting
- Internal Thermal Shutdown Protection
- Low Voltage Indicator Output for Direct Microprocessor Interface
- Heat Tab Power Package

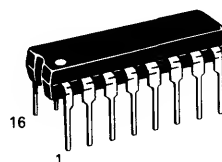


This document contains information on a new product. Specifications and information herein are subject to change without notice.

MC34163
MC33163

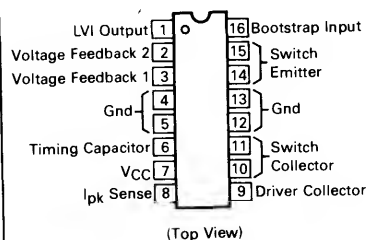
POWER SWITCHING REGULATORS

**SILICON MONOLITHIC
 INTEGRATED CIRCUIT**



P SUFFIX
 PLASTIC PACKAGE
 CASE 648C

PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
MC34163P	0 to +70°C	16 Plastic DIP
MC33163P	-40 to +85°C	16 Plastic DIP

MC34163, MC33163

MAXIMUM RATING

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	V
Switch Collector Voltage Range	$V_{C(switch)}$	-1.0 to +40	V
Switch Emitter Voltage Range	$V_{E(switch)}$	-2.0 to $V_{C(switch)}$	V
Switch Collector to Emitter Voltage	$V_{CE(switch)}$	40	V
Switch Current (Note 1)	I_{SW}	3.4	A
Driver Collector Voltage	$V_{C(driver)}$	-1.0 to +40	V
Driver Collector Current	$I_{C(driver)}$	150	mA
Bootstrap Input Current Range (Note 1)	I_{BS}	-100 to +100	mA
Current Sense Input Voltage Range	$V_{lpk(sense)}$	($V_{CC} - 7.0$) to ($V_{CC} + 1.0$)	V
Feedback, and Timing Capacitor Input Voltage Range	V_{in}	-1.0 to +7.0	V
Low Voltage Indicator Output Voltage Range	$V_{C(LVI)}$	-1.0 to +40	V
Low Voltage Indicator Output Sink Current	$I_{C(LVI)}$	10	mA
Power Dissipation and Thermal Characteristics P Suffix Package Case 648C-02 Maximum Power Dissipation @ $T_A = 25^\circ\text{C}$ Thermal Resistance Junction to Air Thermal Resistance Junction to Case (Pins 4, 5, 12, 13)	P_D $R_{\theta JA}$ $R_{\theta JC}$	1.56 80 15	W $^\circ\text{C/W}$ $^\circ\text{C/W}$
Operating Junction Temperature	T_J	+150	$^\circ\text{C}$
Operating Ambient Temperature (Note 3) MC34163 MC33163	T_A	0 to +70 -40 to +85	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS $V_{CC} = 15\text{ V}$, Pin 16 = V_{CC} , $C_T = 620\text{ pF}$, for typical values $T_A = 25^\circ\text{C}$, for min/max values T_A is the operating ambient temperature range that applies, (Note 3), unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Frequency $T_A = 25^\circ\text{C}$ Total Variation over $V_{CC} = 2.5\text{ V}$ to 40 V , and Temperature	f_{OSC}	46 45	50 —	54 55	kHz
Charge Current	I_{chg}	—	225	—	μA
Discharge Current	I_{dischg}	—	25	—	μA
Charge to Discharge Current Ratio	I_{chg}/I_{dischg}	8.0	9.0	10	—
Sawtooth Peak Voltage	$V_{OSC(P)}$	—	1.25	—	V
Sawtooth Valley Voltage	$V_{OSC(V)}$	—	0.55	—	V
FEEDBACK COMPARATOR 1					
Threshold Voltage $T_A = 25^\circ\text{C}$ Line Regulation ($V_{CC} = 2.5\text{ V}$ to 40 V , $T_A = 25^\circ\text{C}$) Total Variation over Line, and Temperature	$V_{th(FB1)}$	4.9 — 4.85	5.05 0.008 —	5.2 0.03 5.25	V %/V V
Input Bias Current ($V_{FB1} = 5.05\text{ V}$)	$I_{IB(FB1)}$	—	100	200	μA

NOTES:

- Maximum package power dissipation limits must be observed.
- $T_{low} = 0^\circ\text{C}$ for MC34163 $T_{high} = +70^\circ\text{C}$ for MC34163
= -40°C for MC33163 = $+85^\circ\text{C}$ for MC33163

MC34163, MC33163

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ELECTRICAL CHARACTERISTICS (continued) $V_{CC} = 15\text{ V}$, Pin 16 = V_{CC} , $C_T = 620\text{ pF}$, for typical values $T_A = 25^\circ\text{C}$, for min/max values T_A is the operating ambient temperature range that applies, (Note 3), unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
FEEDBACK COMPARATOR 2					
Threshold Voltage $T_A = 25^\circ\text{C}$ Line Regulation ($V_{CC} = 2.5\text{ V to } 40\text{ V}$, $T_A = 25^\circ\text{C}$) Total Variation over Line, and Temperature	$V_{th}(FB2)$	1.225 — 1.213	1.25 0.008 —	1.275 0.03 1.287	V %/V V
Input Bias Current ($V_{FB2} = 1.25\text{ V}$)	$I_{B}(FB2)$	-0.4	0	0.4	μA
CURRENT LIMIT COMPARATOR					
Threshold Voltage $T_A = 25^\circ\text{C}$ Total Variation over $V_{CC} = 2.5\text{ V to } 40\text{ V}$, and Temperature	$V_{th}(I_{pk}\text{ sense})$	— 230	250 —	— 270	mV
Input Bias Current ($V_{Ipk}(\text{sense}) = 15\text{ V}$)	$I_{B}(\text{sense})$	—	1.0	5.0	μA
DRIVER AND OUTPUT SWITCH (Note 2)					
Sink Saturation Voltage ($I_{SW} = 2.5\text{ A}$, Pins 14, 15 grounded) Non-Darlington Connection ($R_{Pin\ 9} = 110\ \Omega$ to V_{CC} , $I_{SW}/DRV \approx 20$) Darlington Connection (Pins 9, 10, 11 connected)	$V_{CE}(\text{sat})$	— —	1.3 1.5	1.7 2.2	V
Collector Off-State Leakage Current ($V_{CE} = 40\text{ V}$)	$I_{C}(\text{off})$	—	0.02	200	μA
Bootstrap Input Current Source ($V_{BS} = V_{CC} + 5.0\text{ V}$)	$I_{source}(\text{DRV})$	0.5	2.0	4.0	mA
Bootstrap Input Zener Clamp Voltage ($I_Z = 25\text{ mA}$)	V_Z	$(V_{CC} + 5.0)$	$(V_{CC} + 7.0)$	$(V_{CC} + 9.0)$	V
LOW VOLTAGE INDICATOR					
Input Threshold (V_{FB2} increasing)	V_{th}	1.07	1.125	1.18	V
Input Hysteresis (V_{FB2} decreasing)	V_H	—	15	—	mV
Output Sink Saturation Voltage ($I_{sink} = 2.0\text{ mA}$)	$V_{OL}(LVI)$	—	0.15	0.5	V
Output Off-State Leakage Current ($V_{OH} = 40\text{ V}$)	I_{OH}	—	0.01	10	μA
TOTAL DEVICE					
Standby Supply Current ($V_{CC} = 2.5\text{ V to } 40\text{ V}$, Pin 8 = V_{CC} , Pins 6, 14, 15 = Gnd, remaining pins open)	I_{CC}	—	6.0	10	mA

NOTES:

- Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
- $T_{low} = 0^\circ\text{C}$ for MC34163 $T_{high} = +70^\circ\text{C}$ for MC34163
 $= -40^\circ\text{C}$ for MC33163 $= +85^\circ\text{C}$ for MC33163

FIGURE 1 — OUTPUT SWITCH ON-OFF TIME versus OSCILLATOR TIMING CAPACITOR

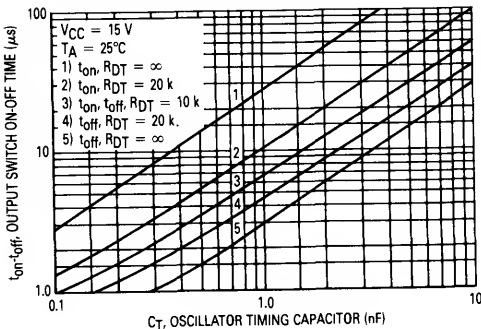


FIGURE 2 — OSCILLATOR FREQUENCY CHANGE versus TEMPERATURE

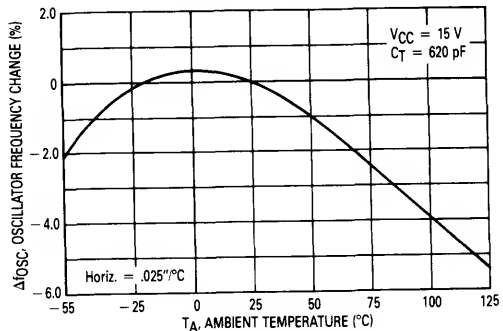


FIGURE 3 — FEEDBACK COMPARATOR 1 INPUT BIAS CURRENT versus TEMPERATURE

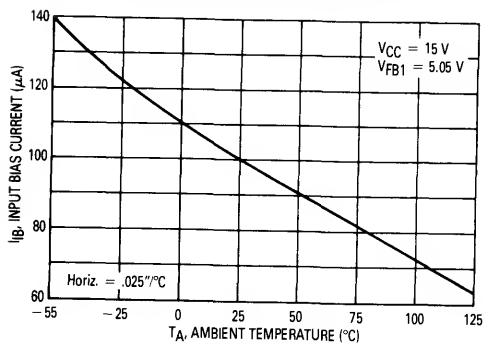


FIGURE 4 — FEEDBACK COMPARATOR 2 THRESHOLD VOLTAGE versus TEMPERATURE

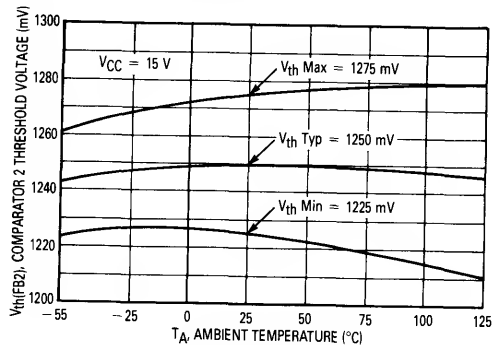


FIGURE 5 — BOOTSTRAP INPUT CURRENT SOURCE versus TEMPERATURE

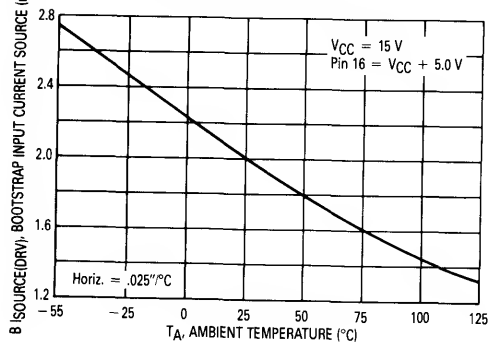


FIGURE 6 — BOOTSTRAP INPUT ZENER CLAMP VOLTAGE versus TEMPERATURE

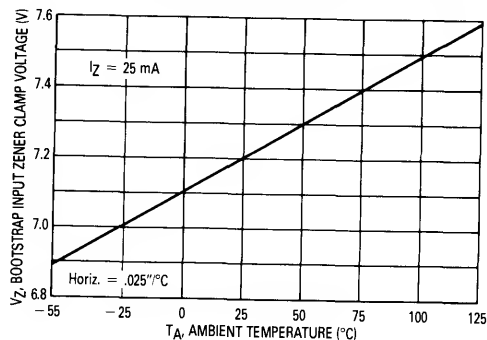


FIGURE 7 — OUTPUT SWITCH SOURCE SATURATION versus EMITTER CURRENT

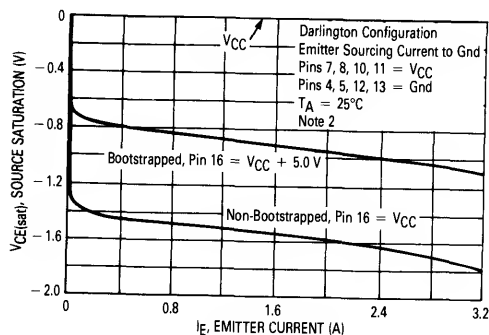


FIGURE 8 — OUTPUT SWITCH SINK SATURATION versus COLLECTOR CURRENT

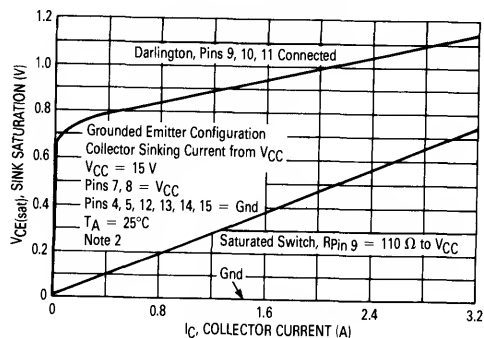


FIGURE 9 — OUTPUT SWITCH NEGATIVE EMITTER VOLTAGE versus TEMPERATURE

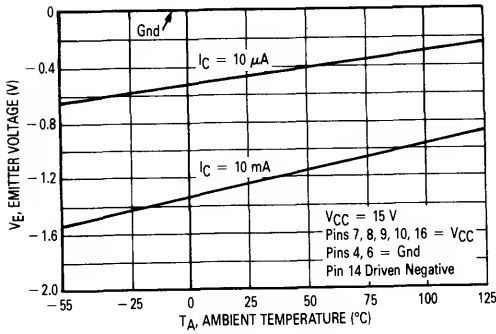
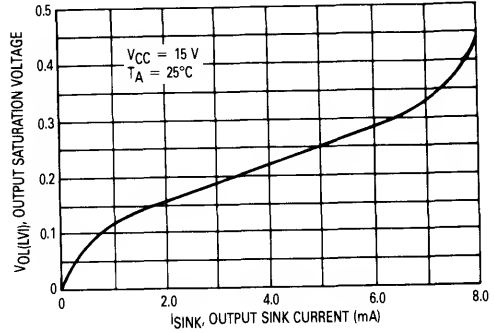


FIGURE 10 — LOW VOLTAGE INDICATOR OUTPUT SINK SATURATION VOLTAGE versus SINK CURRENT



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FIGURE 11 — CURRENT LIMIT COMPARATOR THRESHOLD VOLTAGE versus TEMPERATURE

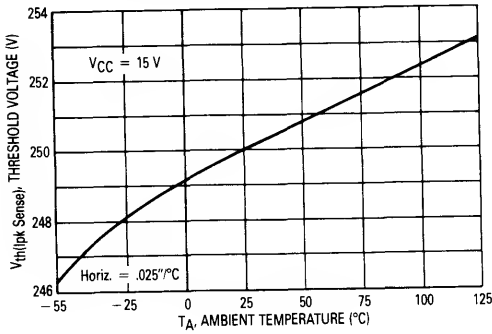


FIGURE 12 — CURRENT LIMIT COMPARATOR INPUT BIAS CURRENT versus TEMPERATURE

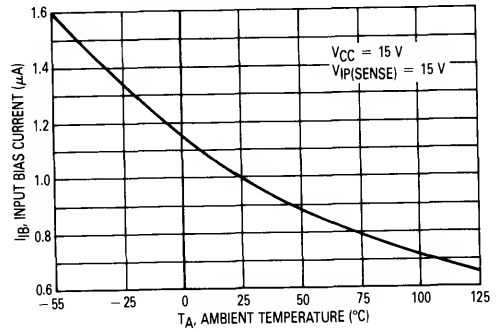


FIGURE 13 — STANDBY SUPPLY CURRENT versus SUPPLY VOLTAGE

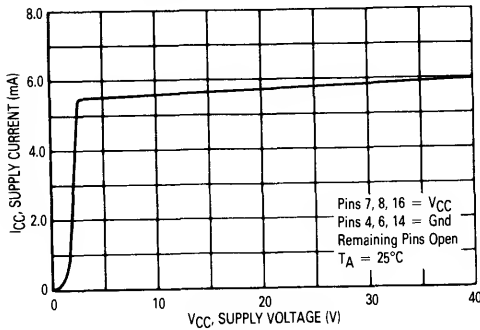
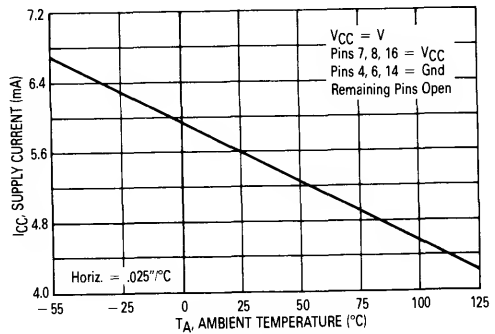


FIGURE 14 — STANDBY SUPPLY CURRENT versus TEMPERATURE



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FIGURE 15 — MINIMUM OPERATING SUPPLY VOLTAGE versus TEMPERATURE

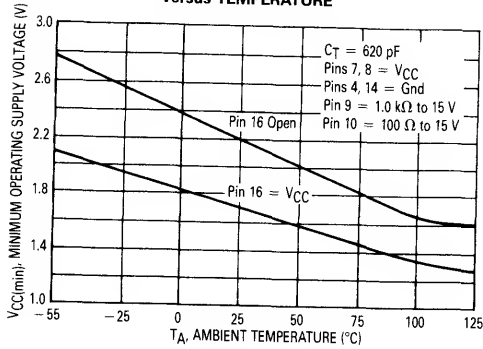


FIGURE 16 — THERMAL RESISTANCE AND MAXIMUM POWER DISSIPATION versus P.C.B. COPPER LENGTH

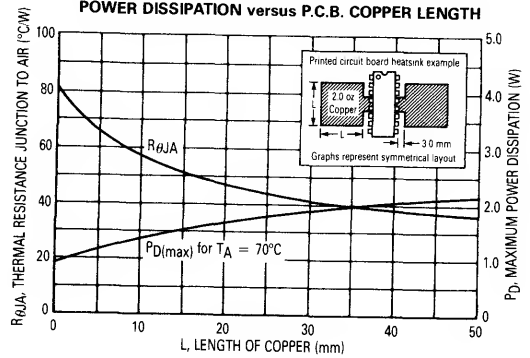


FIGURE 17 — REPRESENTATIVE BLOCK DIAGRAM

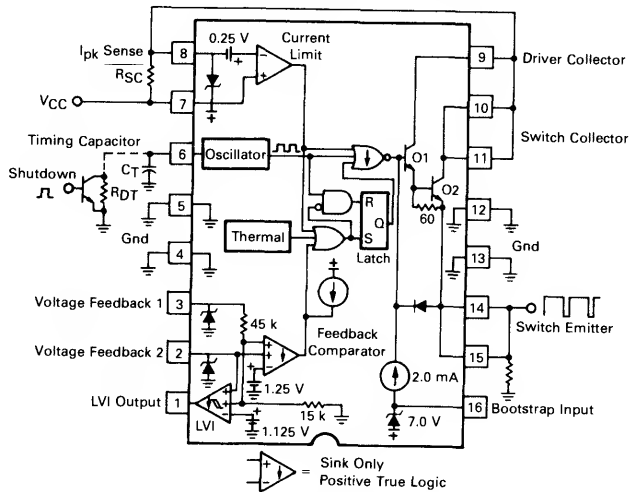
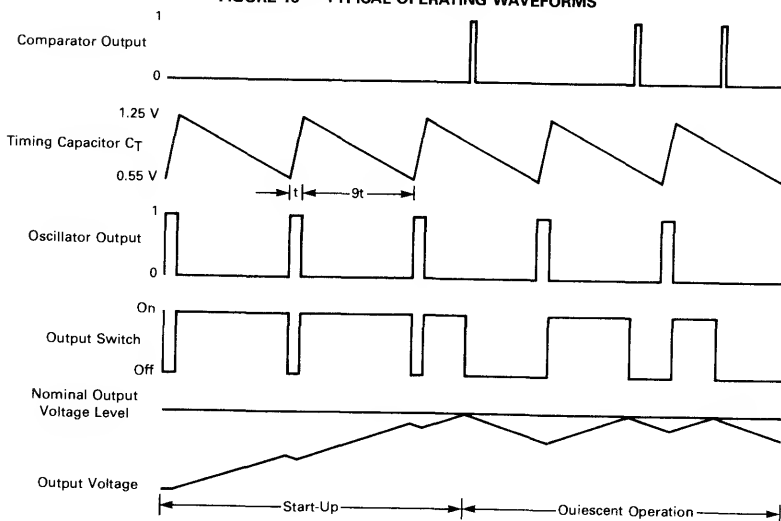
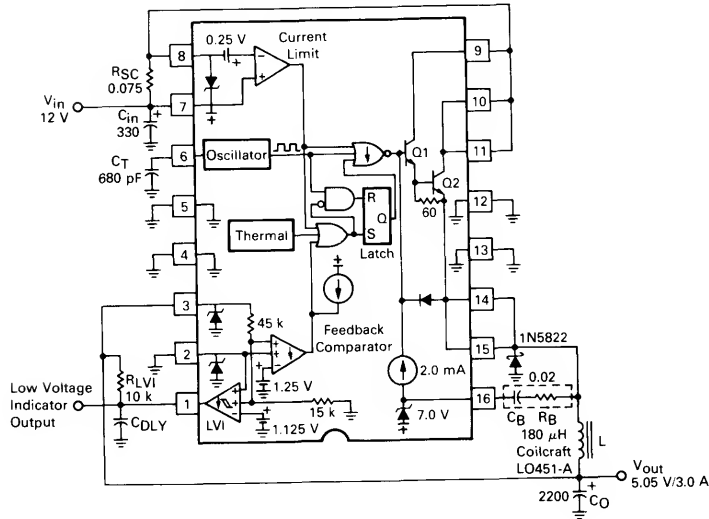


FIGURE 18 — TYPICAL OPERATING WAVEFORMS



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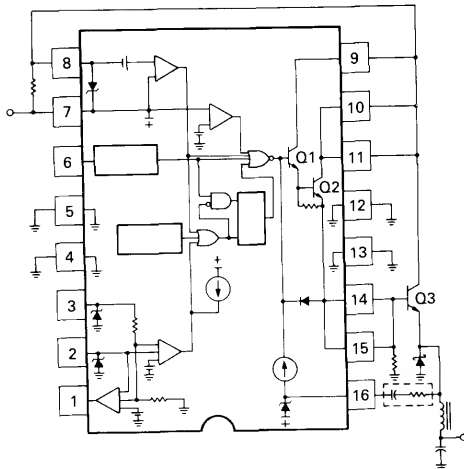
FIGURE 19 — STEP-DOWN CONVERTER



Test	Condition	Results
Line Regulation	$V_{in} = 8.0 \text{ V to } 24 \text{ V}$, $I_O = 3.0 \text{ A}$	$6.0 \text{ mV} = \pm 0.06\%$
Load Regulation	$V_{in} = 12 \text{ V}$, $I_O = 0.6 \text{ A to } 3.0 \text{ A}$	$2.0 \text{ mV} = \pm 0.02\%$
Output Ripple	$V_{in} = 12 \text{ V}$, $I_O = 3.0 \text{ A}$	36 mVp-p
Short Circuit Current	$V_{in} = 12 \text{ V}$, $R_L = 0.1 \Omega$	3.3 A
Efficiency, Without Bootstrap	$V_{in} = 12 \text{ V}$, $I_O = 3.0 \text{ A}$	76.7%
Efficiency, With Bootstrap	$V_{in} = 12 \text{ V}$, $I_O = 3.0 \text{ A}$	81.2%

FIGURE 20 — EXTERNAL CURRENT BOOST CONNECTIONS FOR $I_{pk}(\text{switch})$ GREATER THAN 3.4 A

20A — EXTERNAL NPN SWITCH



20B — EXTERNAL PNP SATURATED SWITCH

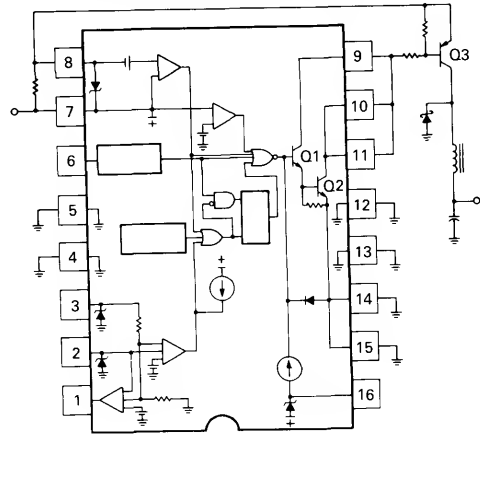
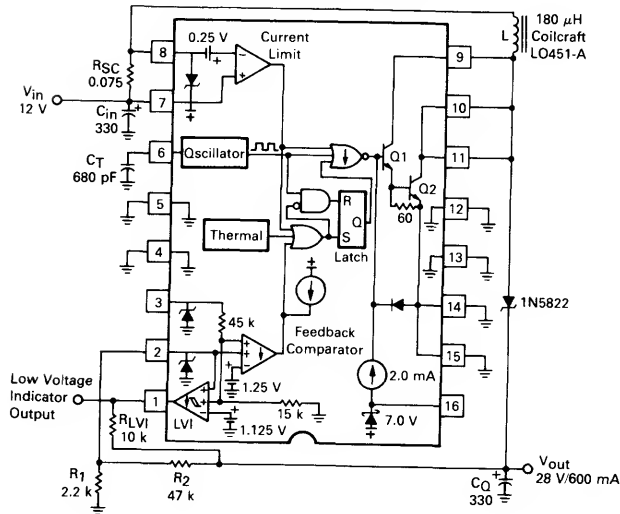


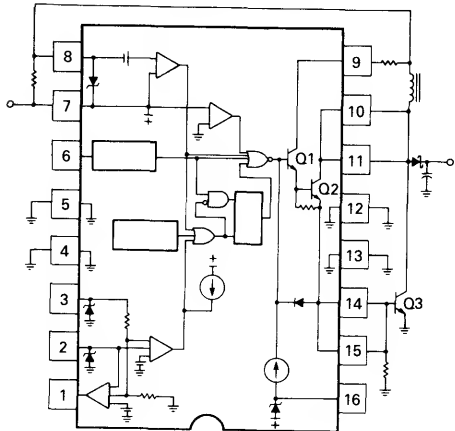
FIGURE 21 — STEP-UP CONVERTER



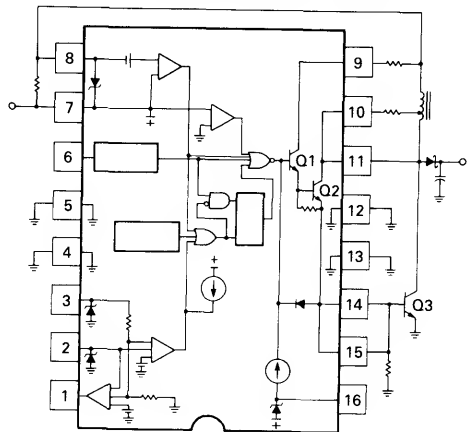
Test	Condition	Results
Line Regulation	$V_{in} = 9.0 \text{ V to } 16 \text{ V}, I_O = 0.6 \text{ A}$	$30 \text{ mV} = \pm 0.05\%$
Load Regulation	$V_{in} = 12 \text{ V}, I_O = 0.1 \text{ A to } 0.6 \text{ A}$	$50 \text{ mV} = \pm 0.09\%$
Output Ripple	$V_{in} = 12 \text{ V}, I_O = 0.6 \text{ A}$	140 mVp-p
Efficiency	$V_{in} = 12 \text{ V}, I_O = 0.6 \text{ A}$	88.1%

FIGURE 22 — EXTERNAL CURRENT BOOST CONNECTIONS FOR $I_{pk(switch)}$ GREATER THAN 3.4 A

22A — EXTERNAL NPN SWITCH

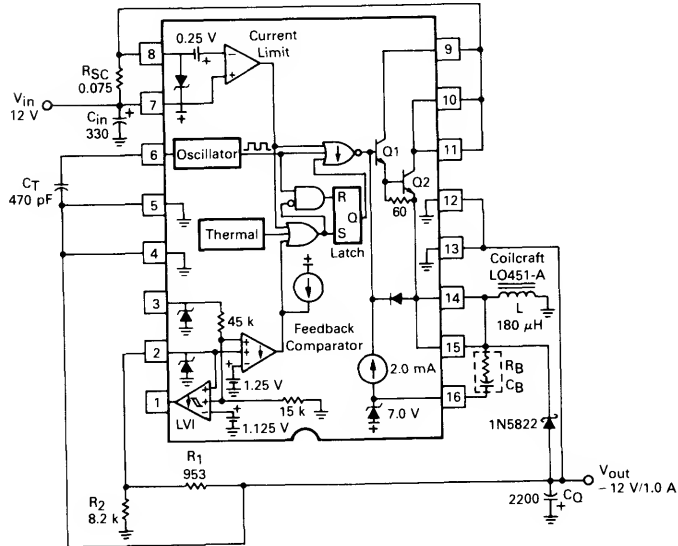


22B — EXTERNAL NPN SATURATED SWITCH



MC34163, MC33163

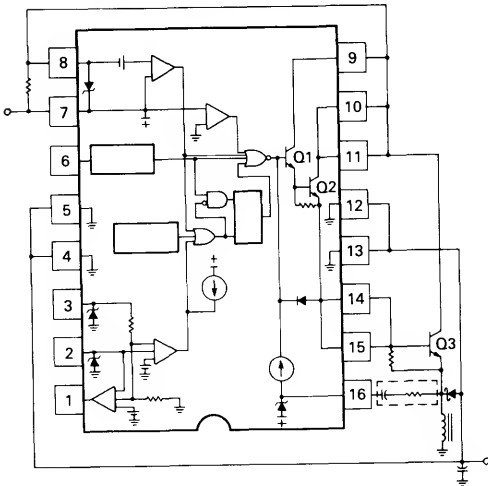
FIGURE 23 — VOLTAGE-INVERTING CONVERTER



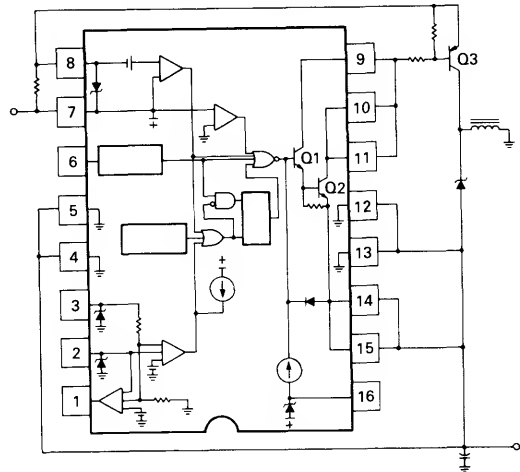
Test	Condition	Results
Line Regulation	$V_{in} = 9.0 \text{ V to } 16 \text{ V}$, $I_O = 1.0 \text{ A}$	$5.0 \text{ mV} = \pm 0.02\%$
Load Regulation	$V_{in} = 12 \text{ V}$, $I_O = 0.6 \text{ A to } 1.0 \text{ A}$	$2.0 \text{ mV} = \pm 0.01\%$
Output Ripple	$V_{in} = 12 \text{ V}$, $I_O = 1.0 \text{ A}$	130 mVp-p
Short Circuit Current	$V_{in} = 12 \text{ V}$, $R_L = 0.1 \Omega$	3.2 A
Efficiency, Without Bootstrap	$V_{in} = 12 \text{ V}$, $I_O = 1.0 \text{ A}$	73.1%
Efficiency, With Bootstrap	$V_{in} = 12 \text{ V}$, $I_O = 1.0 \text{ A}$	77.5%

FIGURE 24 — EXTERNAL CURRENT BOOST CONNECTIONS FOR $I_{pk(switch)}$ GREATER THAN 3.4 A

24A — EXTERNAL NPN SWITCH



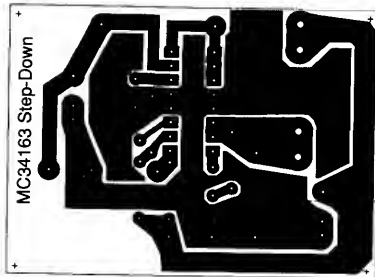
24B — EXTERNAL PNP SATURATED SWITCH



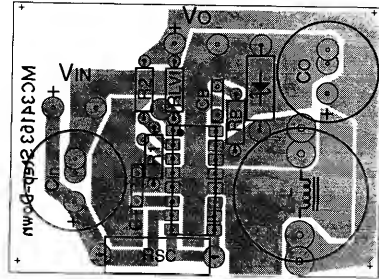
MC34163, MC33163

FIGURE 25 — PRINTED CIRCUIT BOARD AND COMPONENT LAYOUT
(CIRCUITS OF FIGURES 19, 21, 23)

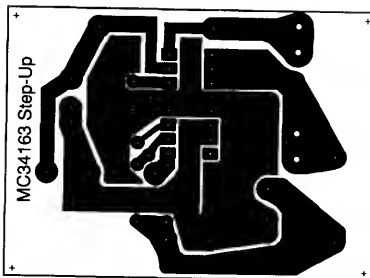
3



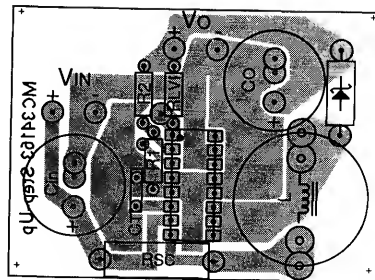
Bottom View



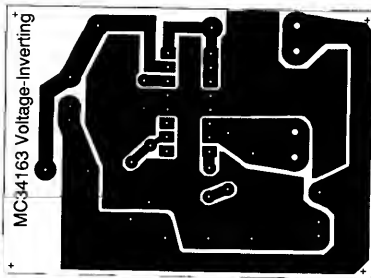
Top View



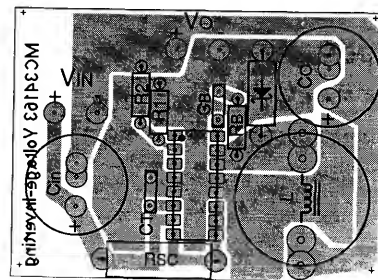
Bottom View



Top View



Bottom View



Top View

All printed circuit boards are 2.58" in width by 1.9" in height.

Advance Information

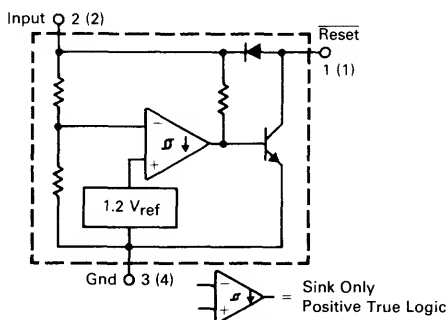
MICROPOWER UNDERVOLTAGE SENSING CIRCUIT

The MC34164 is an undervoltage sensing circuit specifically designed for use as a reset controller in portable microprocessor based systems where extended battery life is required. It offers the designer an economical solution for low voltage detection with a single external resistor. The MC34164 features a bandgap reference, a comparator with precise thresholds and built-in hysteresis to prevent erratic reset operation, an open collector reset output capable of sinking in excess of 7.0 mA, and guaranteed operation down to 1.0 V input with extremely low standby current. These devices are packaged in 3-pin TO-226AA and 8-pin surface mount packages.

Applications include direct monitoring of the 5.0 Volt MPU/logic power supply used in appliance, automotive, consumer, and industrial equipment.

- Temperature Compensated Reference
- Precise Comparator Thresholds Guaranteed Over Temperature
- Comparator Hysteresis Prevents Erratic Reset
- Reset Output Capable of Sinking in Excess of 7.0 mA
- Internal Clamp Diode for Discharging Delay Capacitor
- Guaranteed Reset Operation with 1.0 V Input
- Extremely Low Standby Current of 12 μ A
- Economical TO-226AA and Surface Mount Packages

REPRESENTATIVE BLOCK DIAGRAM



Pin numbers adjacent to terminals are for the 3-pin TO-226AA package.
 Pin numbers in parenthesis are for the D suffix SO-8 package.

MC34164
MC33164

MICROPOWER UNDERVOLTAGE SENSING CIRCUIT

**SILICON MONOLITHIC
 INTEGRATED CIRCUIT**



Pin 1. Reset
 2. Input
 3. Ground

P SUFFIX
 PLASTIC PACKAGE
 CASE 29
 (TO-226AA)



Pin 1. Reset
 2. Input
 3. N.C.
 4. Ground
 5. N.C.
 6. N.C.
 7. N.C.
 8. N.C.

D SUFFIX
 PLASTIC PACKAGE
 CASE 751
 (SO-8)

ORDERING INFORMATION

Device	Temperature Range	Package
MC34164D-5	0°C to +70°C	Plastic SO-8
MC34164P-5		Plastic TO-226AA
MC33164D-5	-40°C to +85°C	Plastic SO-8
MC33164P-5		Plastic TO-226AA

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MC34164, MC33164

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Input Supply Voltage	V_{in}	-1.0 to 12	V
Reset Output Voltage	V_O	-1.0 to 12	V
Reset Output Sink Current	I_{Sink}	Internally Limited	mA
Clamp Diode Forward Current, Pin 1 to 2 (Note 1)	I_F	100	mA
Power Dissipation and Thermal Characteristics			
P Suffix, Plastic Package			
Maximum Power Dissipation ($T_A = 25^\circ\text{C}$)	P_D	700	mW
Thermal Resistance Junction to Air	$R_{\theta JA}$	178	$^\circ\text{C/W}$
D Suffix, Plastic Package			
Maximum Power Dissipation ($T_A = 25^\circ\text{C}$)	P_D	700	mW
Thermal Resistance Junction to Air	$R_{\theta JA}$	178	$^\circ\text{C/W}$
Operating Junction Temperature	T_J	+150	$^\circ\text{C}$
Operating Ambient Temperature Range	T_A		$^\circ\text{C}$
MC34164		0 to +70	
MC33164		-40 to +85	
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS For typical values $T_A = 25^\circ\text{C}$, for min/max values T_A is the operating ambient temperature range that applies (Notes 2 & 3).

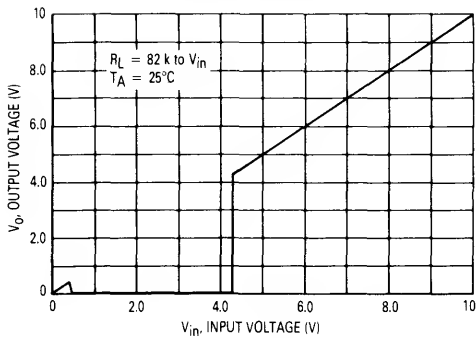
Characteristic	Symbol	Min	Typ	Max	Unit
COMPARATOR					
Threshold Voltage					V
High State Output (V_{in} Increasing)	V_{IH}	4.15	4.33	4.45	
Low State Output (V_{in} Decreasing)	V_{IL}	4.15	4.27	4.45	
Hysteresis ($I_{Sink} = 100 \mu\text{A}$)	V_H	0.02	0.06	—	
RESET OUTPUT					
Output Sink Saturation	V_{OL}				V
($V_{in} = 4.0 \text{ V}$, $I_{Sink} = 1.0 \text{ mA}$)		—	0.14	0.4	
($V_{in} = 1.0 \text{ V}$, $I_{Sink} = 0.25 \text{ mA}$)		—	0.1	0.3	
Output Sink Current (V_{in} , Reset = 4.0 V)	I_{Sink}	7.0	20	50	mA
Output Off-State Leakage	$I_{R(leak)}$				μA
(V_{in} , Reset = 5.0 V)		—	0.02	0.5	
(V_{in} , Reset = 10 V)		—	0.02	2.0	
Clamp Diode Forward Voltage, Pin 1 to 2 ($I_F = 5.0 \text{ mA}$)	V_F	0.6	0.9	1.2	V
TOTAL DEVICE					
Operating Input Voltage Range	V_{in}	1.0 to 10	—	—	V
Quiescent Input Current	I_{in}				μA
$V_{in} = 5.0 \text{ V}$		—	12	20	
$V_{in} = 10 \text{ V}$		—	32	50	

NOTES:

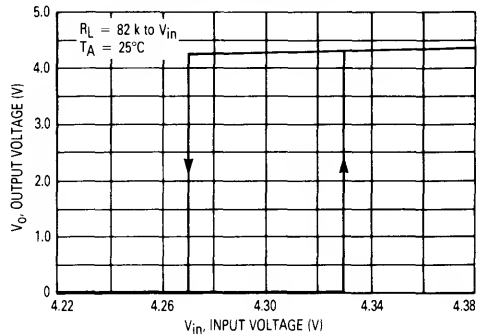
- Maximum Package power dissipation limits must be observed.
- Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
- $T_{low} = 0^\circ\text{C}$ for MC34164 $T_{high} = +70^\circ\text{C}$ for MC34164
 $T_{low} = -40^\circ\text{C}$ for MC33164 $T_{high} = +85^\circ\text{C}$ for MC33164

MC34164, MC33164

**FIGURE 1 — RESET OUTPUT VOLTAGE
versus INPUT VOLTAGE**



**FIGURE 2 — RESET OUTPUT VOLTAGE
versus INPUT VOLTAGE**



**FIGURE 3 — COMPARATOR THRESHOLD VOLTAGE
versus TEMPERATURE**

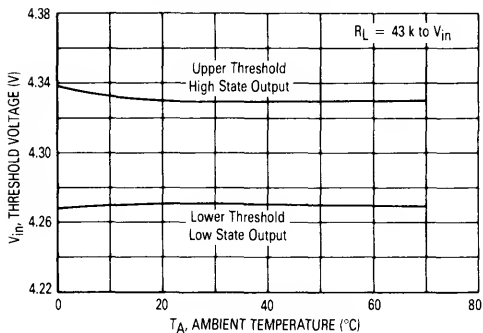
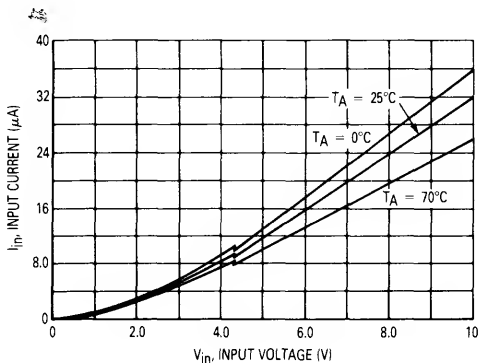


FIGURE 4 — INPUT CURRENT versus INPUT VOLTAGE



**FIGURE 5 — RESET OUTPUT SATURATION
versus SINK CURRENT**

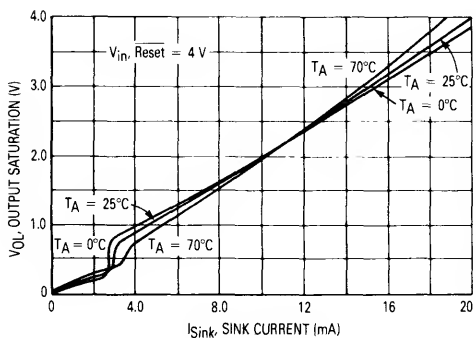
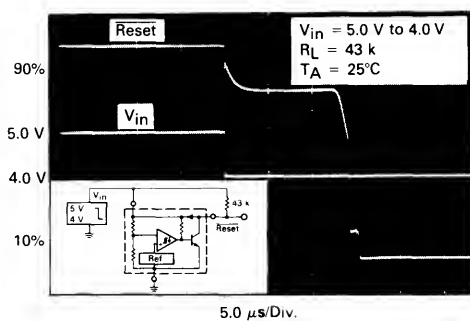


FIGURE 6 — RESET DELAY TIME



MC34164, MC33164

FIGURE 7 — CLAMP DIODE FORWARD CURRENT
versus VOLTAGE

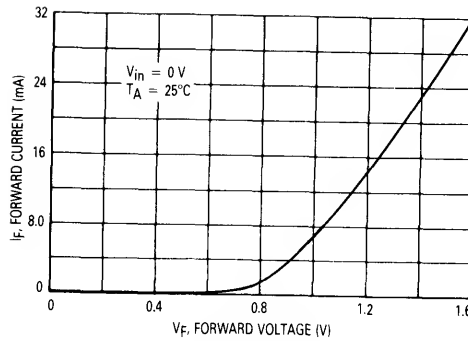
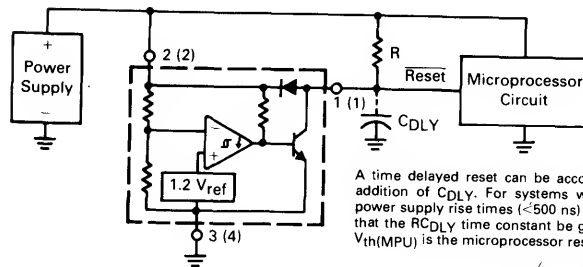
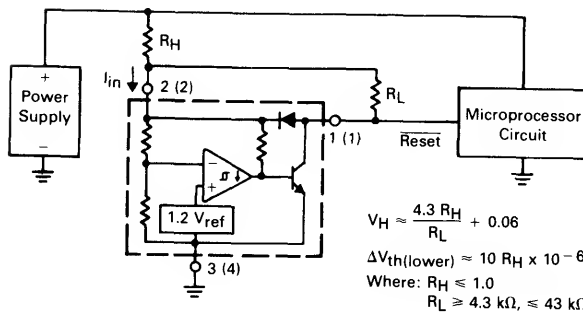


FIGURE 8 — LOW VOLTAGE MICROPROCESSOR RESET



$$t_{DLY} = R C_{DLY} \ln \left(\frac{1}{1 - \frac{V_{th(MPU)}}{V_{in}}} \right)$$

FIGURE 9 — LOW VOLTAGE MICROPROCESSOR RESET WITH ADDITIONAL HYSTERESIS



TEST DATA			
V_H (mV)	ΔV_{th} (mV)	R_H (Ω)	R_L (k Ω)
60	0	0	43
103	1.0	100	10
123	1.0	100	6.8
160	1.0	100	4.3
155	2.2	220	10
199	2.2	220	6.8
280	2.2	220	4.3
262	4.7	470	10
306	4.7	470	8.2
357	4.7	470	6.8
421	4.7	470	5.6
530	4.7	470	4.3

Comparator hysteresis can be increased with the addition of resistor R_H . The hysteresis equation has been simplified and does not account for the change of input current I_{in} as V_{CC} crosses the comparator threshold (Figure 4). An increase of the lower threshold $\Delta V_{th(lower)}$ will be observed due to I_{in} which is typically $10 \mu A$ at 4.3 V. The equations are accurate to $\pm 10\%$ with R_H less than $1.0 k\Omega$ and R_L between $4.3 k\Omega$ and $43 k\Omega$.

MC34164, MC33164

FIGURE 10 — VOLTAGE MONITOR

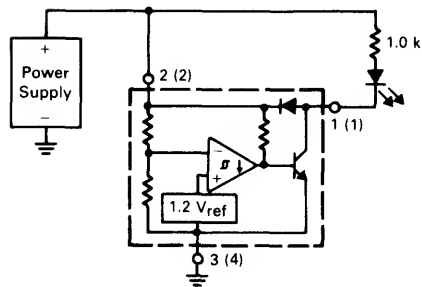


FIGURE 11 — SOLAR POWERED BATTERY CHARGER

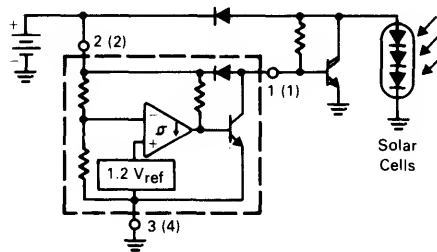
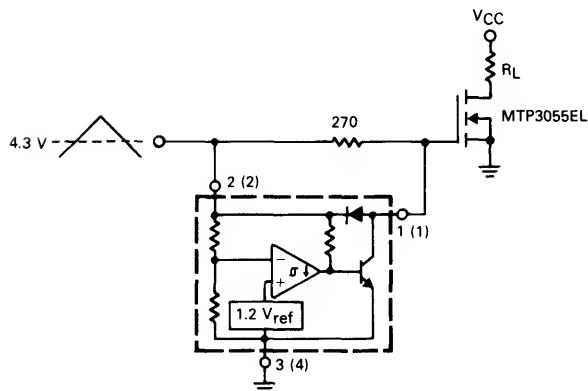


FIGURE 12 — MOSFET LOW VOLTAGE GATE DRIVE PROTECTION



Overheating of the logic level power MOSFET due to insufficient gate voltage can be prevented with the above circuit. When the input signal is below the 4.3 volt threshold of the MC34164, its output grounds the gate of the L² MOSFET.

Product Preview

POWER SWITCHING REGULATORS

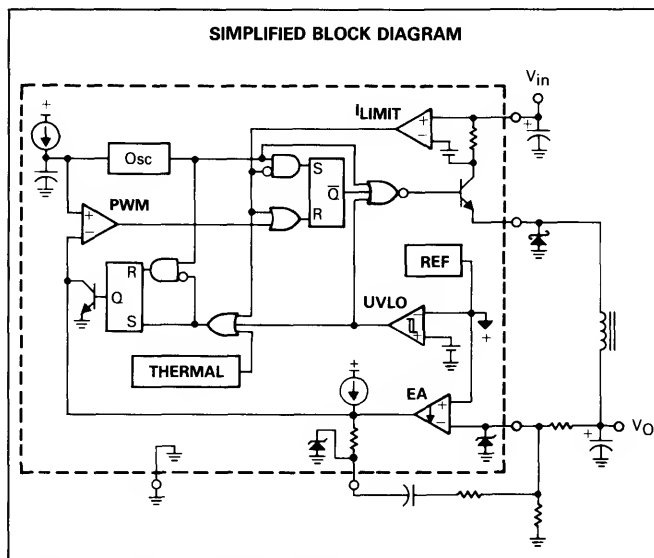
The MC34166, MC33166 series are high performance fixed frequency power switching regulators containing all the active functions required to implement standard DC-to-DC converter configurations. These devices feature an internal temperature compensated reference, fixed frequency oscillator with on-chip timing components, latching pulse width modulator for single pulse metering, high gain error amplifier, and a high current output switch.

Also included are protection features consisting of under-voltage lockout, cycle-by-cycle current limiting, and thermal shutdown.

This series was specifically designed to be incorporated in Step-Down and Voltage-Inverting configurations with a minimum number of external components and can also be used cost effectively in Step-Up applications.

- 8.0 V to 40 V Operation
- Output Switch Current in Excess of 3.0 A
- Fixed Frequency Oscillator with On-Chip Timing Components
- $5.05 \text{ V} \pm 2.0\%$ Reference
- High Gain Error Amplifier
- 0% to 95% Output Duty Cycle
- Cycle-By-Cycle Current Limiting
- Undervoltage Lockout with Hysteresis
- Internal Thermal Shutdown

SIMPLIFIED BLOCK DIAGRAM

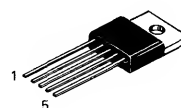


This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MC34166 MC33166

POWER SWITCHING REGULATORS

SILICON MONOLITHIC INTEGRATED CIRCUIT



T SUFFIX
PLASTIC PACKAGE
CASE 314D

PIN CONNECTIONS



- Pin 1. Voltage Feedback Input
 2. Switched Output
 3. Ground
 4. Input Voltage
 5. Compensation
 (Heatsink surface connected to Pin 3)

ORDERING INFORMATION

Device	Temperature Range	Package
MC34166T	0 to +70°C	Plastic Power
MC33166T	-40 to +85°C	Plastic Power

Product Preview

CURRENT MODE CONTROLLER OPTIMIZED FOR H.V. BIPOLAR SWITCH

The MC44602 series are high performance fixed frequency current mode controllers. They are specifically designed for Off-Line and DC-to-DC converter applications offering the designer a cost effective solution with minimal external components. These integrated circuits feature an oscillator, a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totem pole output ideally suited for driving a high voltage bipolar power transistor (MJE18004, MJE18008).

Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle-by-cycle current limiting, programmable output deadtime of 50% minimum, and a latch for single pulse metering.

These devices are available in an 8-pin dual-in-line plastic package as well as the 16-pin plastic heat tab power package which offers additional features.

FEATURES OF THE 8-PIN AND 16-PIN VERSION

- Duty Cycle Limited to 50% Maximum
- Current Mode Operation Up to 500 kHz
- Automatic Feed Forward Compensation
- Latching PWM for Cycle-By-Cycle Current Limiting
- Reference with Undervoltage Lockout
- High Current Totem Pole Output: 500 mA Source, 1.0 A Sink
- V_{CC} Undervoltage Lockout with Hysteresis
- Low Start-Up and Operating Current
- Direct Interface with Motorola SENSEFET Products
- Thermal Protection

ADDITIONAL FEATURES OF 16-PIN VERSION

- Efficient Power Supply Short Circuit Protection
- Synchronization Input, TTL Compatible
- Separated Sink and Source Outputs for Optimal Base Drive of Bipolar Power Transistor
- Power Ground for Negative Output Voltage

ORDERING INFORMATION

Device	Temperature Range	Package
MC44602P1	-25 to +85°C	8-Pin Plastic
MC44602P2		16-Pin Plastic

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SENSEFET is a trademark of Motorola Inc.

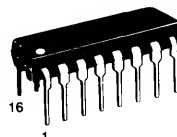
MC44602

CURRENT MODE CONTROLLER

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**

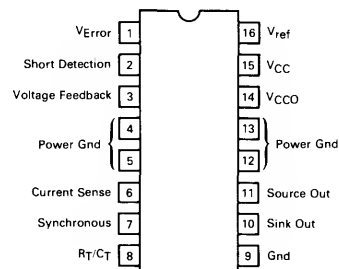
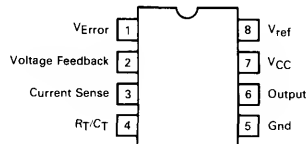


P1 SUFFIX
PLASTIC PACKAGE
CASE 626



P2 SUFFIX
PLASTIC PACKAGE
CASE 648C

PIN CONNECTIONS



Pins 4, 5, 12 and 13 are electrical power ground and heatsink pins for IC

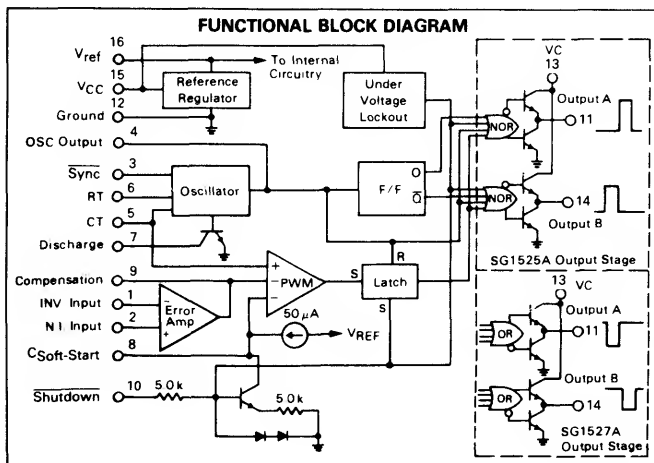
MOTOROLA SEMICONDUCTOR TECHNICAL DATA

3

PULSE WIDTH MODULATOR CONTROL CIRCUITS

The SG1525A/1527A series of pulse width modulator control-circuits offer improved performance and lower external parts count when implemented for controlling all types of switching power supplies. The on-chip +5.1 volt reference is trimmed to $\pm 1\%$ and the error amplifier has an input common-mode voltage range that includes the reference voltage, thus eliminating the need for external divider resistors. A sync input to the oscillator enables multiple units to be slaved or a single unit to be synchronized to an external system clock. A wide range of dead time can be programmed by a single resistor connected between the C_T and Discharge pins. These devices also feature built-in soft-start circuitry, requiring only an external timing capacitor. A shutdown pin controls both the soft-start circuitry and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft-start recycle with longer shutdown commands. The under voltage lockout inhibits the outputs and the changing of the soft-start capacitor when V_{CC} is below nominal. The output stages are totem-pole design capable of sinking and sourcing in excess of 200 mA. The output stage of the SG1525A series features NOR Logic resulting in a low output for an off state while the SG1527A series utilizes OR Logic which gives a high output when off. The devices are available in Military, Industrial and Commercial temperature ranges.

- 8.0 to 35 Volt Operation
- 5.1 Volt $\pm 1.0\%$ Trimmed Reference
- 100 Hz to 400 kHz Oscillator Range
- Separate Oscillator Sync Pin
- Adjustable Dead Time Control
- Input Undervoltage Lockout
- Latching PWM to Prevent Multiple Pulses
- Pulse-by-Pulse Shutdown
- Dual Source/Sink Outputs: ± 400 mA Peak

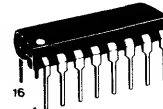
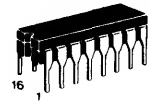


SG1525A/SG1527A SG2525A/SG2527A SG3525A/SG3527A

PULSE WIDTH MODULATOR CONTROL CIRCUITS

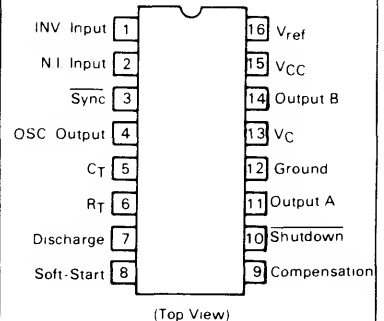
SILICON MONOLITHIC INTEGRATED CIRCUITS

J SUFFIX
CERAMIC PACKAGE
CASE 620



N SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
SG1525AJ SG1527AJ	-55 to +125°C	Ceramic DIP Ceramic DIP
SG2525AJ SG2527AJ SG2525AN SG2527AN	-25 to +85°C	Ceramic DIP Plastic DIP Ceramic DIP Plastic DIP
SG3525AJ SG3525AN SG3527AJ SG3527AN	0 to +70°C	Ceramic DIP Plastic DIP Ceramic DIP Plastic DIP

SG1525A, SG1527A, SG2525A, SG2527A, SG3525A, SG3527A

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	+40	Vdc
Collector Supply Voltage	V_C	+40	Vdc
Logic Inputs	—	-0.3 to +5.5	V
Analog Inputs	—	-0.3 to V_{CC}	V
Output Current, Source or Sink	I_O	±500	mA
Reference Output Current	I_{ref}	50	mA
Oscillator Charging Current	—	5.0	mA
Power Dissipation (Plastic & Ceramic Package) $T_A = +25^\circ\text{C}$ (Note 2) $T_C = +25^\circ\text{C}$ (Note 3)	P_D	1000 2000	mW
Thermal Resistance Junction to Air Plastic and Ceramic Package	$R_{\theta JA}$	100	$^\circ\text{C}/\text{W}$
Thermal Resistance Junction to Case Plastic and Ceramic Package	$R_{\theta JC}$	60	$^\circ\text{C}/\text{W}$
Operating Junction Temperature	T_J	+150	$^\circ\text{C}$
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}	-65 to +150 -55 to +125	$^\circ\text{C}$
Lead Temperature (Soldering, 10 Seconds)	T_{solder}	+300	$^\circ\text{C}$

NOTES

1. Values beyond which damage may occur.
2. Derate at 10 mW/ $^\circ\text{C}$ for ambient temperatures above +50 $^\circ\text{C}$.
3. Derate at 16 mW/ $^\circ\text{C}$ for case temperatures above +25 $^\circ\text{C}$.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min.	Max.	Unit
Supply Voltage	V_{CC}	+8.0	+35	Vdc
Collector Supply Voltage	V_C	+4.5	+35	Vdc
Output Sink/Source Current (Steady State) (Peak)	I_O	0 0	±100 ±400	mA
Reference Load Current	I_{ref}	0	20	mA
Oscillator Frequency Range	f_{osc}	0.1	400	kHz
Oscillator Timing Resistor	R_T	2.0	150	k Ω
Oscillator Timing Capacitor	C_T	0.001	0.2	μF
Deadtime Resistor Range	R_D	0	500	Ω
Operating Ambient Temperature Range SG1525A, SG1527A SG2525A, SG2527A SG3525A, SG3527A	T_A	-55 -25 0	+125 +85 +70	$^\circ\text{C}$

SG1525A, SG1527A, SG2525A, SG2527A, SG3525A, SG3527A

ELECTRICAL CHARACTERISTICS ($V_{CC} = +20 \text{ Vdc}$, $T_A = T_{\text{low}}$ to T_{high} (Note 4), unless otherwise specified)

Characteristic	Symbol	SG1525A/2525A SG1527A/2527A			SG3525A SG3527A			Unit
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION								
Reference Output Voltage ($T_J = +25^{\circ}\text{C}$)	V_{ref}	5.05	5.10	5.15	5.00	5.10	5.20	Vdc
Line Regulation ($+8.0\text{ V} \leq V_{\text{CC}} \leq +35\text{ V}$)	Reg_{line}	—	10	20	—	10	20	mV
Load Regulation ($0\text{ mA} \leq I_L \leq 20\text{ mA}$)	Reg_{load}	—	20	50	—	20	50	mV
Temperature Stability	$\Delta V_{\text{ref}}/\Delta T$	—	20	—	—	20	—	mV
Total Output Variation Includes Line and Load Regulation over Temperature	ΔV_{ref}	5.00	—	5.20	4.95	—	5.25	Vdc
Short Circuit Current ($V_{\text{ref}} = 0\text{ V}$, $T_J = +25^{\circ}\text{C}$)	I_{SC}	—	80	100	—	80	100	mA
Output Noise Voltage ($10\text{ Hz} \leq f \leq 10\text{ kHz}$, $T_J = +25^{\circ}\text{C}$)	V_n	—	40	200	—	40	200	μV_{rms}
Long Term Stability ($T_J = +125^{\circ}\text{C}$) (Note 5)	S	—	20	50	—	20	50	mV/khr
OSCILLATOR SECTION								

OSCILLATOR SECTION (Note 6, unless otherwise specified)

Initial Accuracy ($T_J = +25^\circ\text{C}$)	—	—	± 2.0	± 6.0	—	± 2.0	± 6.0	%
Frequency Stability with Voltage ($+8.0 \text{ V} \leq V_{CC} \leq +35 \text{ V}$)	$\frac{\Delta f_{\text{osc}}}{\Delta V_{CC}}$	—	± 0.3	± 1.0	—	± 1.0	± 2.0	%
Frequency Stability with Temperature	$\frac{\Delta f_{\text{osc}}}{\Delta T}$	—	± 3.0	—	—	± 3.0	—	%
Minimum Frequency ($R_T = 150 \text{ k}\Omega$, $C_T = 0.2 \text{ }\mu\text{F}$)	f_{min}	—	50	—	—	50	—	Hz
Maximum Frequency ($R_T = 2.0 \text{ k}\Omega$, $C_T = 1.0 \text{ nF}$)	f_{max}	400	—	—	400	—	—	kHz
Current Mirror ($I_{R_T} = 2.0 \text{ mA}$)	—	1.7	2.0	2.2	1.7	2.0	2.2	mA
Clock Amplitude	—	3.0	3.5	—	3.0	3.5	—	V
Clock Width ($T_J = +25^\circ\text{C}$)	—	0.3	0.5	1.0	0.3	0.5	1.0	μs
Sync Threshold	—	1.2	2.0	2.8	1.2	2.0	2.8	V
Sync Input Current (Sync Voltage = $+3.5 \text{ V}$)	—	—	1.0	2.5	—	1.0	2.5	mA

ERROR AMPLIFIER SECTION ($V_{CM} = +5.1 \text{ V}$)

Input Offset Voltage	V_{IO}	—	0.5	5.0	—	2.0	10	mV
Input Bias Current	I_{IB}	—	1.0	10	—	1.0	10	μA
Input Offset Current	I_{IO}	—	—	1.0	—	—	1.0	μA
DC Open Loop Gain ($R_L \geq 10 \text{ M}\Omega$)	A_{VOL}	60	75	—	60	75	—	dB
Low Level Output Voltage	V_{OL}	—	0.2	0.5	—	0.2	0.5	V
High Level Output Voltage	V_{OH}	3.8	5.6	—	3.8	5.6	—	V
Common Mode Rejection Ratio ($+1.5 \text{ V} \leq V_{CM} \leq +5.2 \text{ V}$)	CMRR	60	75	—	60	75	—	dB
Power Supply Rejection Ratio ($+8.0 \text{ V} \leq V_{CC} \leq +35 \text{ V}$)	PSRR	50	60	—	50	60	—	dB

PWM COMPARATOR SECTION

Minimum Duty Cycle	DC_{min}	—	—	0	—	—	0	%
Maximum Duty Cycle	DC_{max}	45	49	—	45	49	—	%
Input Threshold, Zero Duty Cycle (Note 6)	V_{TH}	0.6	0.9	—	0.6	0.9	—	V
Input Threshold, Maximum Duty Cycle (Note 6)	V_{TH}	—	3.3	3.6	—	3.3	3.6	V
Input Bias Current	I_{IB}	—	0.05	1.0	—	0.05	1.0	μA

SG1525A, SG1527A, SG2525A, SG2527A, SG3525A, SG3527A

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ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	SG1525A/2525A SG1527A/2527A			SG3525A SG3527A			Unit
		Min	Typ	Max	Min	Typ	Max	
SOFT-START SECTION								
Soft-Start Current ($V_{\text{shutdown}} = 0 \text{ V}$)	—	25	50	80	25	50	80	μA
Soft-Start Voltage ($V_{\text{shutdown}} = 2.0 \text{ V}$)	—	—	0.4	0.6	—	0.4	0.6	V
Shutdown Input Current ($V_{\text{shutdown}} = 2.5 \text{ V}$)	—	—	0.4	1.0	—	0.4	1.0	mA
OUTPUT DRIVERS (Each Output, $V_{\text{CC}} = +20 \text{ V}$)								
Output Low Level ($I_{\text{sink}} = 20 \text{ mA}$) ($I_{\text{sink}} = 100 \text{ mA}$)	V_{OL}	— —	0.2 1.0	0.4 2.0	— —	0.2 1.0	0.4 2.0	V
Output High Level ($I_{\text{source}} = 20 \text{ mA}$) ($I_{\text{source}} = 100 \text{ mA}$)	V_{OH}	18 17	19 18	— —	18 17	19 18	— —	V
Under Voltage Lockout (V_8 and $V_9 = \text{High}$)	V_{UL}	6.0	7.0	8.0	6.0	7.0	8.0	V
Collector Leakage, $V_{\text{C}} = +35 \text{ V}$ (Note 7)	$I_{\text{C(Leak)}}$	—	—	200	—	—	200	μA
Rise Time ($C_{\text{L}} = 1.0 \text{ nF}$, $T_{\text{J}} = 25^{\circ}\text{C}$)	t_{r}	—	100	600	—	100	600	ns
Fall Time ($C_{\text{L}} = 1.0 \text{ nF}$, $T_{\text{J}} = 25^{\circ}\text{C}$)	t_{f}	—	50	300	—	50	300	ns
Shutdown Delay ($V_{\text{SD}} = +3.0 \text{ V}$, $C_{\text{S}} = 0$, $T_{\text{J}} = +25^{\circ}\text{C}$)	t_{ds}	—	0.2	0.5	—	0.2	0.5	μs
Supply Current, ($V_{\text{CC}} = +35 \text{ V}$)	I_{CC}	—	14	20	—	14	20	mA

NOTES:

- $T_{\text{low}} = -55^\circ\text{C}$ for SG1525A/1527A
 -25°C for SG2525A/2527A
 0°C for SG3525A/3527A
 $T_{\text{high}} = +125^\circ\text{C}$ for SG1525A/1527A
 $+85^\circ\text{C}$ for SG2525A/2527A
 $+70^\circ\text{C}$ for SG3525A/3527A
- Since long term stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.
- Tested at $f_{\text{osc}} = 40 \text{ kHz}$ ($R_{\text{T}} = 3.6 \text{ k}\Omega$, $C_{\text{T}} = 0.01 \text{ }\mu\text{F}$, $R_{\text{D}} = 0 \text{ }\Omega$).
- Applies to SG1525A/2525A/3525A only, due to polarity of output pulses.

APPLICATION INFORMATION

SHUTDOWN OPTIONS

(See Block Diagram, front page)

Since both the compensation and soft-start terminals (Pins 9 and 8) have current source pull-ups, either can readily accept a pull-down signal which only has to sink a maximum of $100 \text{ }\mu\text{A}$ to turn off the outputs. This is subject to the added requirement of discharging whatever external capacitance may be attached to these pins.

An alternate approach is the use of the shutdown circuitry of Pin 10 which has been improved to enhance the available shutdown options. Activating this circuit by applying a positive signal on Pin 10 performs two

functions: the PWM latch is immediately set providing the fastest turn-off signal to the outputs; and a $150 \text{ }\mu\text{A}$ current sink begins to discharge the external soft-start capacitor. If the shutdown command is short, the PWM signal is terminated without significant discharge of the soft-start capacitor, thus, allowing, for example, a convenient implementation of pulse-by-pulse current limiting. Holding Pin 10 high for a longer duration, however, will ultimately discharge this external capacitor, recycling slow turn-on upon release.

Pin 10 should not be left floating as noise pickup could conceivably interrupt normal operation.

TYPICAL CHARACTERISTICS

FIGURE 1 — SG1525A OSCILLATOR SCHEMATIC

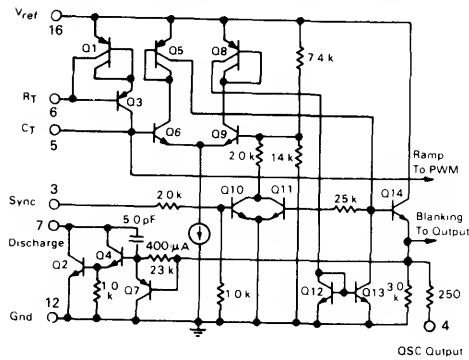


FIGURE 2 — OSCILLATOR CHARGE TIME versus R_T

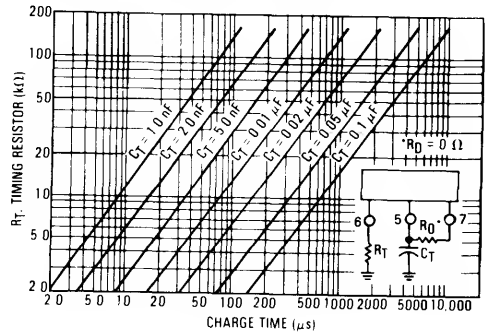


FIGURE 3 — OSCILLATOR DISCHARGE TIME versus R_D

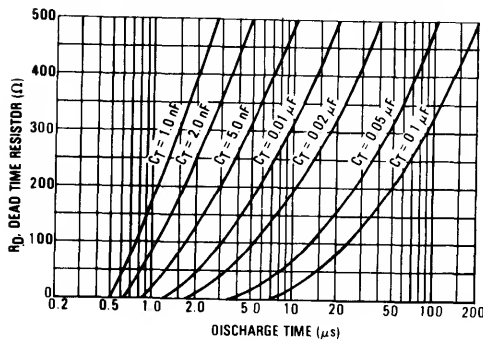


FIGURE 4 — SG1525A ERROR AMPLIFIER SCHEMATIC

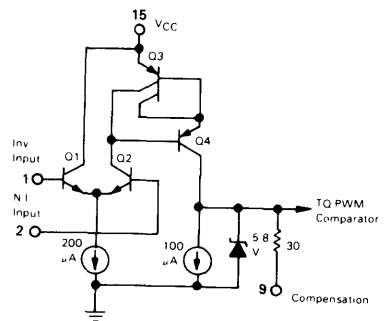


FIGURE 5 — ERROR AMPLIFIER OPEN-LOOP FREQUENCY RESPONSE

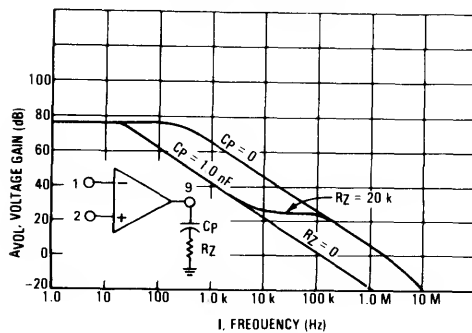


FIGURE 6 — SG1525A OUTPUT CIRCUIT (1/2 CIRCUIT SHOWN)

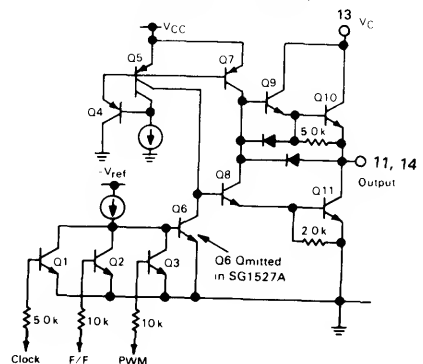


FIGURE 7 — SG1525A/2525A/3525A
OUTPUT SATURATION CHARACTERISTICS

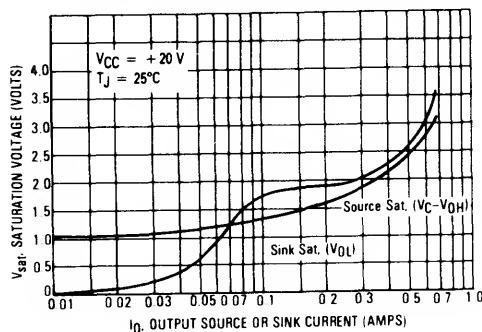
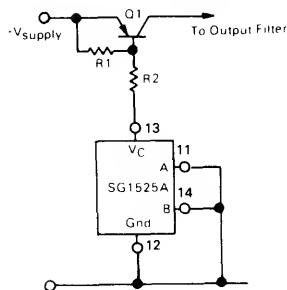
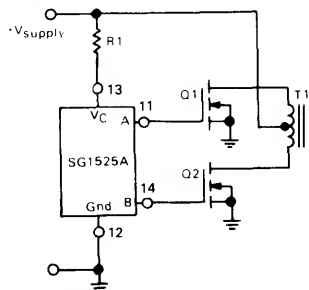


FIGURE 8 — SINGLE ENDED SUPPLY



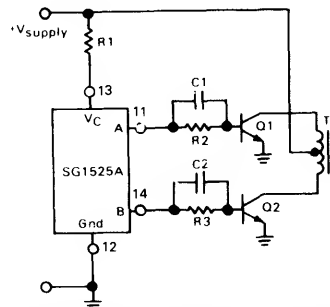
For single-ended supplies, the driver outputs are grounded. The V_C terminal is switched to ground by the totem-pole source transistors on alternate oscillator cycles.

FIGURE 10 — DRIVING POWER FETS



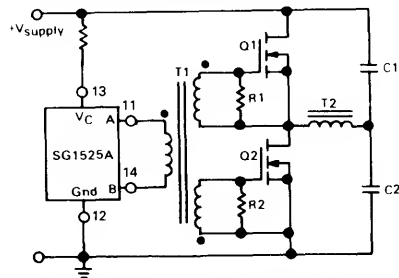
The low source impedance of the output drivers provides rapid charging of power FET input capacitance while minimizing external components.

FIGURE 9 — PUSH-PULL CONFIGURATION



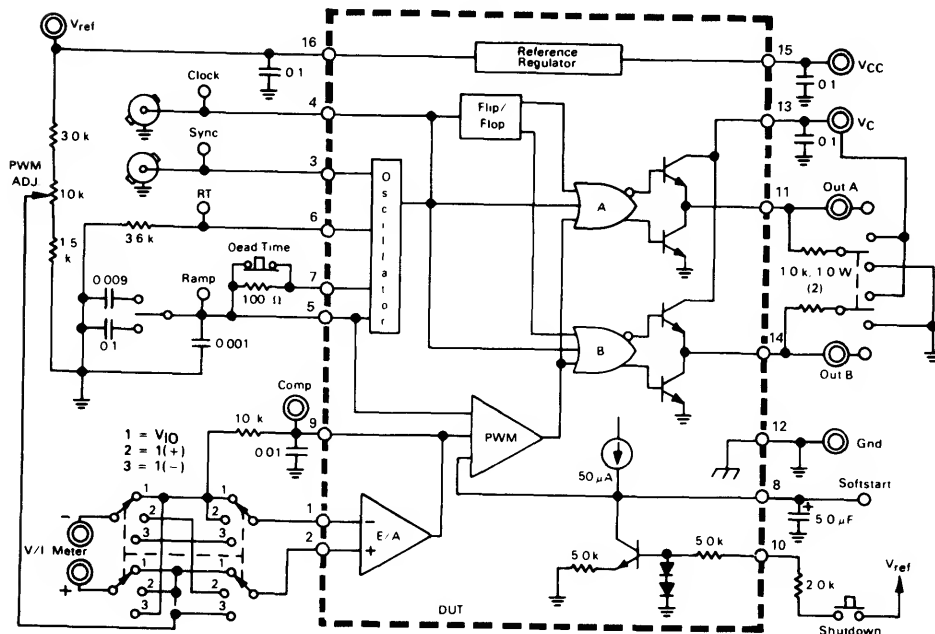
In conventional push-pull bipolar designs, forward base drive is controlled by R1-R3. Rapid turn-off times for the power devices are achieved with speed-up capacitors C1 and C2.

FIGURE 11 — DRIVING TRANSFORMERS IN A HALF-BRIDGE CONFIGURATION



Low power transformers can be driven directly by the SG1525A. Automatic reset occurs during deadtime, when both ends of the primary winding are switched to ground.

FIGURE 12 — LAB TEST FIXTURE



SG1526
SG2526
SG3526

3

PULSE WIDTH MODULATION CONTROL CIRCUIT

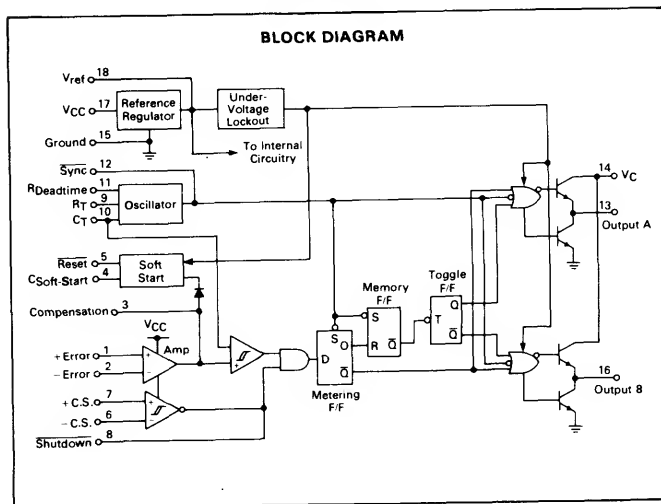
The SG1526 is a high performance pulse width modulator integrated circuit intended for fixed frequency switching regulators and other power control applications.

Functions included in this IC are a temperature compensated voltage reference, sawtooth oscillator, error amplifier, pulse width modulator, pulse metering and steering logic, and two high current totem pole outputs ideally suited for driving the capacitance of power FETs at high speeds.

Additional protective features include soft start and undervoltage lockout, digital current limiting, double pulse inhibit, adjustable dead time and a data latch for single pulse metering. All digital control ports are TTL and B-series CMOS compatible. Active low logic design allows easy wired-OR connections for maximum flexibility. The versatility of this device enables implementation in single-ended or push-pull switching regulators that are transformerless or transformer coupled. The SG1526 is specified over the full military junction temperature range of -55°C to $+150^{\circ}\text{C}$. The SG2526 is specified over a junction temperature range of -40°C to $+150^{\circ}\text{C}$ while the SG3526 is specified over a range of 0°C to $+125^{\circ}\text{C}$.

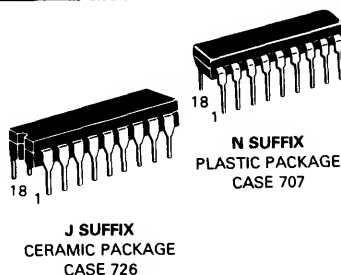
- 8.0 to 35 Volt Operation
- 5.0 Volt $\pm 1\%$ Trimmed Reference
- 1.0 Hz to 400 kHz Oscillator Range
- Dual Source/Sink Current Outputs: ± 100 mA
- Digital Current Limiting
- Programmable Dead Time
- Undervoltage Lockout
- Single Pulse Metering
- Programmable Soft Start
- Wide Current Limit Common Mode Range
- Guaranteed 6 Unit Synchronization

BLOCK DIAGRAM

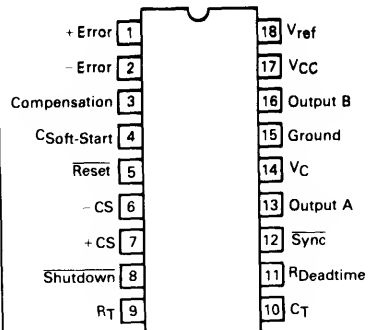


**PULSE WIDTH MODULATION
CONTROL CIRCUITS**

**SILICON MONOLITHIC
INTEGRATED CIRCUITS**



PIN CONNECTIONS



Top View

ORDERING INFORMATION

Device	Junction Temperature Range	Package
SG1526J	-55 to $+150^{\circ}\text{C}$	Ceramic DIP
SG2526J	-40 to $+150^{\circ}\text{C}$	Ceramic DIP
SG2526N	-40 to $+150^{\circ}\text{C}$	Plastic DIP
SG3526J	0 to $+125^{\circ}\text{C}$	Ceramic DIP
SG3526N	0 to $+125^{\circ}\text{C}$	Plastic DIP

SG1526, SG2526, SG3526

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	+40	Vdc
Collector Supply Voltage	V_C	+40	Vdc
Logic Inputs	—	-0.3 to +5.5	V
Analog Inputs	—	-0.3 to V_{CC}	V
Output Current, Source or Sink	I_O	± 200	mA
Reference Load Current ($V_{CC} = 40$ V, Note 2)	I_{ref}	50	mA
Logic Sink Current	—	15	mA
Power Dissipation (Plastic and Ceramic Package) (Note 3) $T_A = +25^\circ\text{C}$ (Note 4) $T_C = +25^\circ\text{C}$	P_D	1000 3000	mW
Thermal Resistance Junction to Air (Plastic and Ceramic Package)	$R_{\theta JA}$	100	$^\circ\text{C}/\text{W}$
Thermal Resistance Junction to Case (Plastic and Ceramic Package)	$R_{\theta JC}$	42	$^\circ\text{C}/\text{W}$
Operating Junction Temperature	T_J	+150	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Lead Temperature (Soldering, 10 Seconds)	T_{solder}	+300	$^\circ\text{C}$

Notes:

1. Values beyond which damage may occur
2. Maximum junction temperature must be observed
3. Derate at 10 mW/ $^\circ\text{C}$ for ambient temperatures above +50 $^\circ\text{C}$
4. Derate at 24 mW/ $^\circ\text{C}$ for case temperatures above +25 $^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	+8.0	+35	Vdc
Collector Supply Voltage	V_C	+4.5	+35	Vdc
Output Sink/Source Current (Each Output)	I_O	0	± 100	mA
Reference Load Current	I_{ref}	0	20	mA
Oscillator Frequency Range	f_{osc}	0.001	400	kHz
Oscillator Timing Resistor	R_T	2.0	150	k Ω
Oscillator Timing Capacitor	C_T	0.001	20	μF
Available Deadtime Range (40 kHz)		3.0	50	%
Operating Junction Temperature Range	T_J			$^\circ\text{C}$
SG1526		-55	+150	
SG2526		-40	+150	
SG3526		0	+125	

SG1526, SG2526, SG3526

ELECTRICAL CHARACTERISTICS $V_{CC} = +15 \text{ Vdc}$, $T_J = T_{\text{low}}$ to T_{high} [Note 5] unless otherwise specified)

Characteristic	Symbol	SG1526/2526			SG3526			Unit
		Min	Typ	Max	Min	Typ	Max	

REFERENCE SECTION (Note 6)

Reference Output Voltage ($T_J = +25^\circ\text{C}$)	V_{ref}	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation ($+8.0 \text{ V} \leq V_{CC} \leq +35 \text{ V}$)	Regline	—	10	20	—	10	30	mV
Load Regulation, $0 \text{ mA} \leq I_L \leq 20 \text{ mA}$	Regload	—	10	30	—	10	50	mV
Temperature Stability	$\Delta V_{\text{ref}}/\Delta T_J$	—	15	—	—	10	—	mV
Total Reference Output Voltage Variation ($+8.0 \text{ V} \leq V_{CC} \leq +35 \text{ V}$, $0 \text{ mA} \leq I_L \leq 20 \text{ mA}$)	ΔV_{ref}	4.90	5.00	5.10	4.85	5.00	5.15	V
Short Circuit Current ($V_{\text{ref}} = 0 \text{ V}$, Note 2)	I_{SC}	25	80	125	25	80	125	mA

UNDERVOLTAGE LOCKOUT

Reset Output Voltage ($V_{\text{ref}} = +3.8 \text{ V}$)	—	—	0.2	0.4	—	0.2	0.4	V
Reset Output Voltage ($V_{\text{ref}} = +4.8 \text{ V}$)	—	2.4	4.8	—	2.4	4.8	—	V

OSCILLATOR SECTION (Note 7)

Initial Accuracy ($T_J = +25^\circ\text{C}$)	—	—	± 3.0	± 8.0	—	± 3.0	± 8.0	%
Frequency Stability over Power Supply Range ($+8.0 \text{ V} \leq V_{CC} \leq +35 \text{ V}$)	$\frac{\Delta f_{\text{osc}}}{\Delta V_{CC}}$	—	0.5	1.0	—	0.5	1.0	%
Frequency Stability over Temperature ($\Delta T_J = T_{\text{low}}$ to T_{high})	$\frac{\Delta f_{\text{osc}}}{\Delta T_J}$	—	4.0	—	—	2.0	—	%
Minimum Frequency ($R_T = 150 \text{ k}\Omega$, $C_T = 20 \text{ }\mu\text{F}$)	f_{min}	—	0.5	—	—	0.5	—	Hz
Maximum Frequency ($R_T = 2.0 \text{ k}\Omega$, $C_T = 0.001 \text{ }\mu\text{F}$)	f_{max}	400	—	—	400	—	—	kHz
Sawtooth Peak Voltage ($V_{CC} = +35 \text{ V}$)	$V_{\text{osc(P)}}$	—	3.0	3.5	—	3.0	3.5	V
Sawtooth Valley Voltage ($V_{CC} = +8.0 \text{ V}$)	$V_{\text{osc(V)}}$	0.45	0.8	—	0.45	0.8	—	V

ERROR AMPLIFIER SECTION (Note 8)

Input Offset Voltage ($R_S \leq 2.0 \text{ k}\Omega$)	V_{IO}	—	2.0	5.0	—	2.0	10	mV
Input Bias Current	I_{IB}	—	—350	—1000	—	—350	—2000	nA
Input Offset Current	I_{IO}	—	35	100	—	35	200	nA
DC Open Loop Gain ($R_L \geq 10 \text{ M}\Omega$)	A_{Vol}	64	72	—	60	72	—	dB
High Output Voltage ($V_{\text{Pin 1}} - V_{\text{Pin 2}} \geq +150 \text{ mV}$, $I_{\text{source}} = 100 \text{ }\mu\text{A}$)	V_{OH}	3.6	4.2	—	3.6	4.2	—	V
Low Output Voltage ($V_{\text{Pin 2}} - V_{\text{Pin 1}} \geq +150 \text{ mV}$, $I_{\text{sink}} = 100 \text{ }\mu\text{A}$)	V_{OL}	—	0.2	0.4	—	0.2	0.4	V
Common Mode Rejection Ratio ($R_S \leq 2.0 \text{ k}\Omega$)	CMRR	70	94	—	70	94	—	dB
Power Supply Rejection Ratio ($+12 \text{ V} \leq V_{CC} \leq +18 \text{ V}$)	PSRR	66	80	—	66	80	—	dB

Notes:

5. $T_{\text{low}} = -55^\circ\text{C}$ for SG1526
 -40°C for SG2526
 0°C for SG3526

$T_{\text{high}} = +150^\circ\text{C}$ for SG1526/2526
 $+125^\circ\text{C}$ for SG3526

6. $I_L = 0 \text{ mA}$ unless otherwise noted.

7. $f_{\text{osc}} = 40 \text{ kHz}$ ($R_T = 4.12 \text{ k}\Omega \pm 1\%$).

$C_T = 0.01 \text{ }\mu\text{F} \pm 1\%$, $R_D = 0 \text{ }\Omega$

8. $0 \text{ V} \leq V_{\text{CM}} \leq +5.2 \text{ V}$

SG1526, SG2526, SG3526

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	SG1526/2526			SG3526			Unit
		Min	Typ	Max	Min	Typ	Max	
PWM COMPARATOR SECTION (Note 7)								
Minimum Duty Cycle ($V_{\text{compensation}} = +0.4 \text{ V}$)	DC _{min}	—	—	0	—	—	0	%
Maximum Duty Cycle ($V_{\text{compensation}} = +3.6 \text{ V}$)	DC _{max}	45	49	—	45	49	—	%

DIGITAL PORTS (SYNC, SHUTDOWN, RESET)

Output Voltage — High Logic Level ($I_{\text{source}} = 40 \mu\text{A}$)	V_{OH}	2.4	4.0	—	2.4	4.0	—	V
Output Voltage — Low Logic Level ($I_{\text{sink}} = 3.6 \text{ mA}$)	V_{OL}	—	0.2	0.4	—	0.2	0.4	V
Input Current — High Logic Level ($V_{\text{IH}} = +2.4 \text{ V}$)	I_{IH}	—	-125	-200	—	-125	-200	μA
Input Current — Low Logic Level ($V_{\text{IL}} = +0.4 \text{ V}$)	I_{IL}	—	-225	-360	—	-225	-360	μA

CURRENT LIMIT COMPARATOR SECTION (Note 9)

Sense Voltage ($R_S \leq 50 \Omega$)	V_{sense}	90	100	110	80	100	120	mV
Input Bias Current	I_{IB}	—	-3.0	-10	—	-3.0	-10	μA

SOFT-START SECTION

Error Clamp Voltage (Reset = +0.4 V)	—	—	0.1	0.4	—	0.1	0.4	V
CSoft-Start Charging Current (Reset = +2.4 V)	I_{CS}	50	100	150	50	100	150	μA

OUTPUT DRIVERS

(Each Output, $V_C = +15 \text{ Vdc}$ unless otherwise specified)

Output High Level $I_{\text{source}} = 20 \text{ mA}$ $I_{\text{source}} = 100 \text{ mA}$	V_{OH}	12.5 12	13.5 13	— —	12.5 12	13.5 13	— —	V
Output Low Level $I_{\text{sink}} = 20 \text{ mA}$ $I_{\text{sink}} = 100 \text{ mA}$	V_{OL}	— —	0.2 1.2	0.3 2.0	— —	0.2 1.2	0.3 2.0	V
Collector Leakage, $V_C = +40 \text{ V}$	$I_{\text{C(leak)}}$	—	50	150	—	50	150	μA
Rise Time ($C_L = 1000 \text{ pF}$)	t_r	—	0.3	0.6	—	0.3	0.6	μs
Fall Time ($C_L = 1000 \text{ pF}$)	t_f	—	0.1	0.2	—	0.1	0.2	μs
Supply Current (Shutdown = +0.4 V, $V_{\text{CC}} = +35 \text{ V}$, $R_T = 4.12 \text{ k}\Omega$)	I_{CC}	—	18	30	—	18	30	mA

7. $f_{\text{osc}} = 40 \text{ kHz}$ ($R_T = 4.12 \text{ k}\Omega \pm 1\%$,

$C_T = 0.01 \mu\text{F} \pm 1\%$, $R_D = 0 \Omega$)

8. $0 \text{ V} \leq V_{\text{CM}} \leq +5.2 \text{ V}$

9. $0 \text{ V} \leq V_{\text{CM}} \leq +12 \text{ V}$

TYPICAL CHARACTERISTICS

FIGURE 1 — SG1526 REFERENCE STABILITY OVER TEMPERATURE

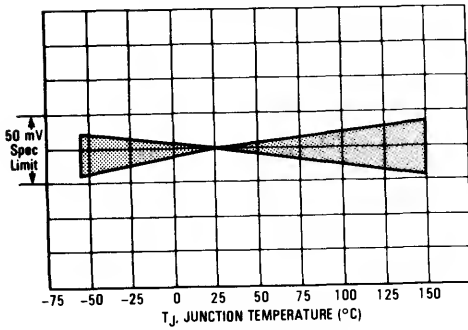


FIGURE 2 — REFERENCE VOLTAGE AS A FUNCTION SUPPLY VOLTAGE

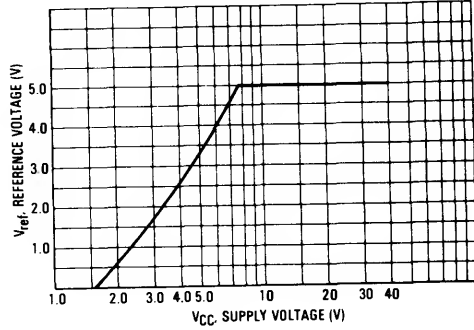


FIGURE 3 — ERROR AMPLIFIER OPEN LOOP FREQUENCY RESPONSE

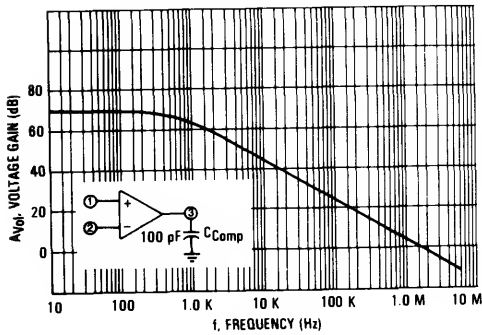


FIGURE 4 — CURRENT LIMIT COMPARATOR THRESHOLD

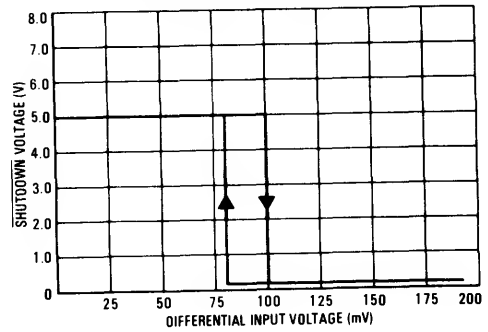


FIGURE 5 — UNDERVOLTAGE LOCKOUT CHARACTERISTIC

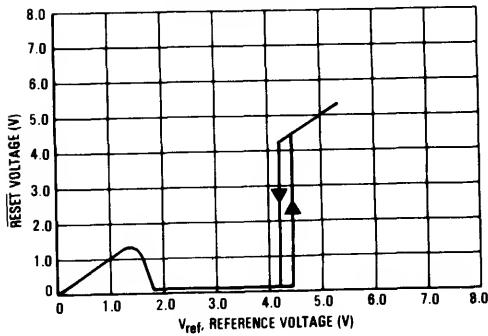


FIGURE 6 — OUTPUT DRIVER SATURATION VOLTAGE AS A FUNCTION OF SINK CURRENT

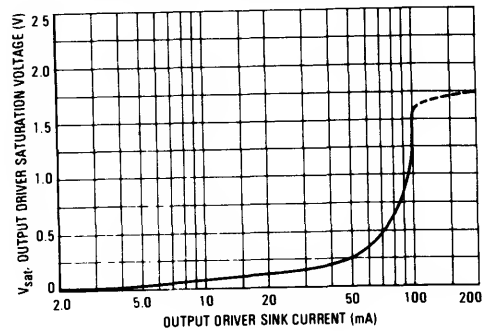


FIGURE 7 — V_C SATURATION VOLTAGE AS A FUNCTION OF SINK CURRENT

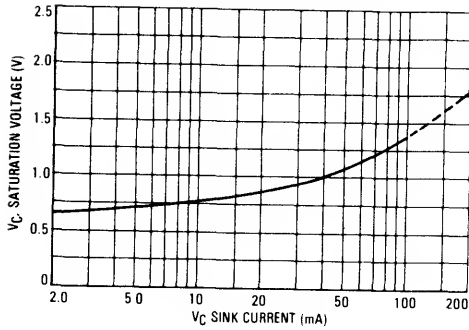


FIGURE 8 — SG1526 OSCILLATOR PERIOD

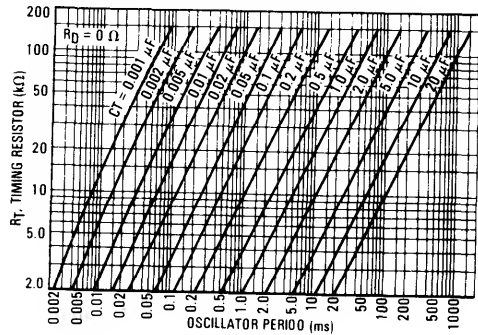


FIGURE 9 — SG1526 ERROR AMPLIFIER

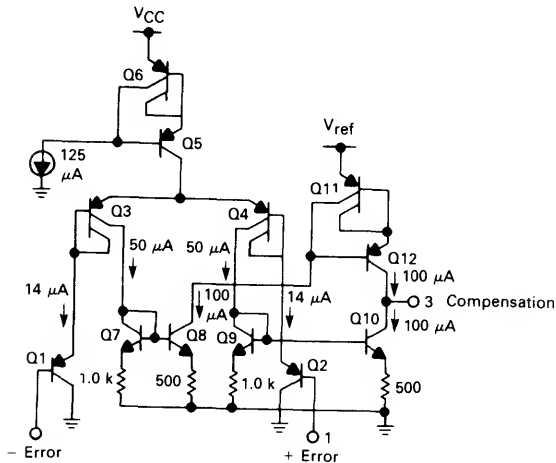


FIGURE 10 — SG1526 UNDERVOLTAGE LOCKOUT

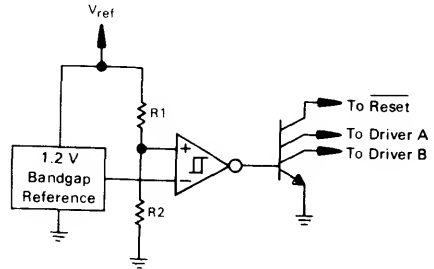
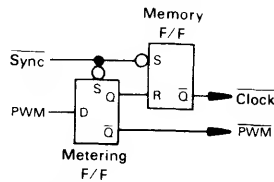


FIGURE 11 — SG1526 PULSE PROCESSING LOGIC



The metering FLIP-FLOP is an asynchronous data latch which suppresses high frequency oscillations by allowing only one PWM pulse per oscillator cycle

The memory FLIP-FLOP prevents double pulsing in a push-pull configuration by remembering which output produced the last pulse

APPLICATIONS INFORMATION

FIGURE 12 — EXTENDING REFERENCE OUTPUT CURRENT CAPABILITY

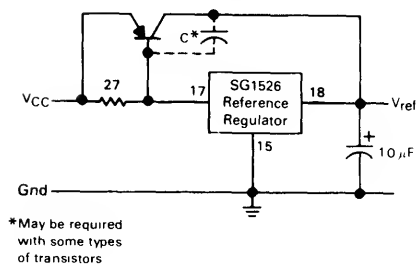


FIGURE 13 — ERROR AMPLIFIER CONNECTIONS

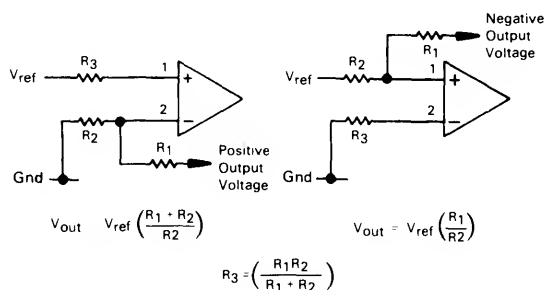


FIGURE 14 — OSCILLATOR CONNECTIONS

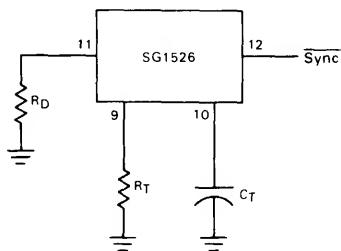


FIGURE 15 — FOLDBACK CURRENT LIMITING

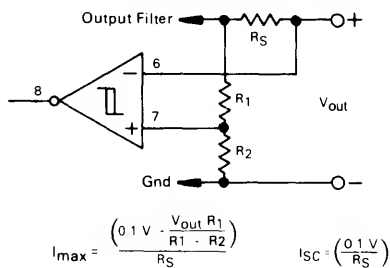


FIGURE 16 — SG1526 SOFT-START CIRCUITRY

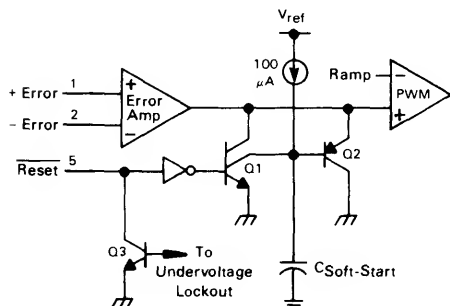
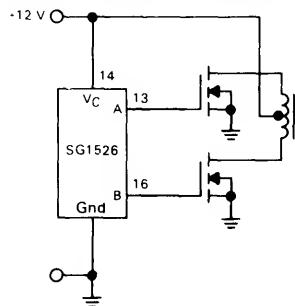


FIGURE 17 — DRIVING VMOS POWER FETS



The totem pole output drivers of the SG1526 are ideally suited for driving the input capacitance of power FETs at high speeds.

FIGURE 18 — HALF-BRIDGE CONFIGURATION

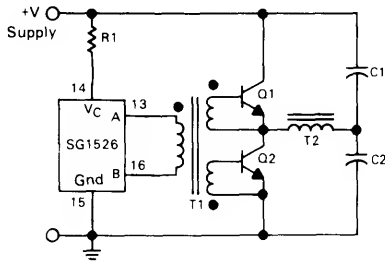
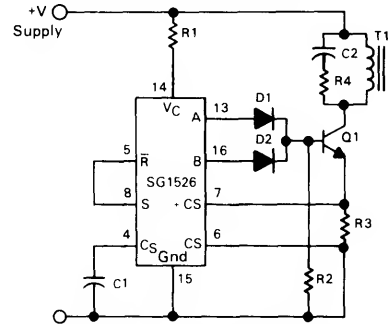


FIGURE 19 — FLYBACK CONVERTER WITH CURRENT LIMITING



In the above circuit, current limiting is accomplished by using the current limit comparator output to reset the soft-start capacitor

FIGURE 20 — SINGLE-ENDED CONFIGURATION

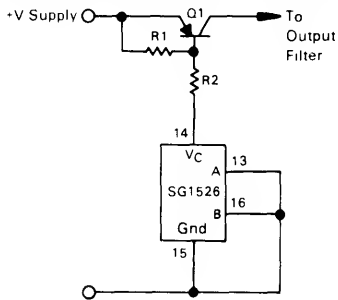
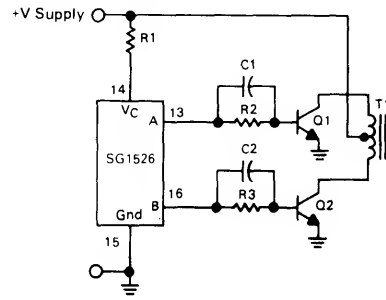


FIGURE 21 — PUSH-PULL CONFIGURATION



Advance Information

UNIVERSAL MICROPROCESSOR POWER SUPPLY/ CONTROLLER

The TCA5600 is a versatile power supply control circuit for microprocessor based systems and mainly intended for automotive applications and battery powered instruments. To cover a wide range of applications, the device offers high circuit flexibility with minimum of external components.

Functions included in this IC are a temperature compensated voltage reference, on chip dc/dc converter, programmable and remote controlled voltage regulator, fixed 5.0 V supply voltage regulator with external PNP power device, undervoltage detection circuit, power-on RESET delay and watchdog feature for safe and hazard free microprocessor operations.

- 6.0 to 30 V Operation Range
- 2.5 V Reference Voltage Accessible for Other Tasks
- Fixed 5.0 V \pm 4% Microprocessor Supply Regulator Including Current Limitation, Overvoltage Protection and Undervoltage Monitor
- Programmable 6.0 to 30 V Voltage Regulator Exhibiting High Peak Current (150 mA), Current Limiting and Thermal Protection
- Two Remote Inputs to Select the Regulator's Operation Mode: OFF, 5.0 V, 5.0 V Standby and Programmable Output Voltage
- Self Contained dc/dc Converter Fully Controlled By the Programmable Regulator to Guarantee Safe Operation Under All Working Conditions
- Programmable Power-On RESET Delay
- Watchdog Select Input
- Negative Edge Triggered Watchdog Input
- Low Current Consumption in the VCC1 Standby Mode
- All Digital Control Ports are TTL- and MOS-Compatible

APPLICATIONS INCLUDE

- Microprocessor Systems with E²PROMs
- High Voltage Crystal and Plasma Displays
- Decentralized Power Supplies in Computer and Telecommunication Systems

RECOMMENDED OPERATION CONDITIONS

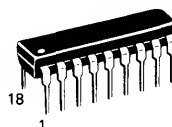
Characteristic	Symbol	Min	Max	Unit
Power Supply Voltage	VCC1	5.0	30	V
	VCC2	5.5	30	V
Collector Current	I _C	—	800	mA
Output Voltage	V _{out2}	6.0	30	V
Reference Source Current	I _{ref}	0	2.0	mA

This document contains information on a new product. Specifications and information herein are subject to change without notice.

TCA5600
TCF5600

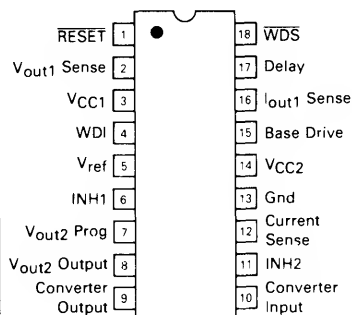
UNIVERSAL MICROPROCESSOR POWER SUPPLY CONTROLLER

SILICON MONOLITHIC
INTEGRATED CIRCUITS



PLASTIC PACKAGE
CASE 707

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Junction Temperature Range	Package
TCA5600	0 to +125°C	Plastic DIP
TCF5600	-40 to +150°C	Plastic DIP

TCA5600, TCF5600

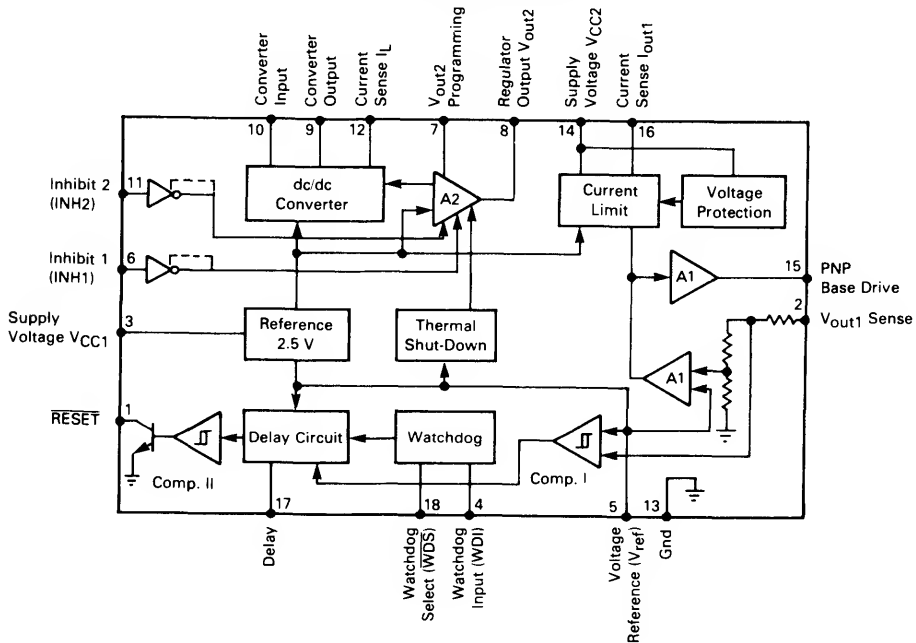
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted, Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 3, 14)	VCC1, VCC2	35	Vdc
Base Drive Current (Pin 15)	I _B	20	mA
Collector Current (Pin 10)	I _C	1.0	A
Forward Rectifier Current (Pin 10–Pin 9)	I _F	1.0	A
Logic Inputs INH1, INH2, $\overline{\text{WDS}}$ (Pin 6, 11, 18)	V _{INP}	–0.3 V to VCC1	Vdc
Logic Input Current WDI (Pin 4)	I _{WDI}	±0.5	mA
Output Sink Current RESET (Pin 1)	I _{RES}	10	mA
Analog Inputs (Pin 2) (Pin 7)	—	–0.3 to 10 –0.3 to 5.0	V
Reference Source Current (Pin 5)	I _{ref}	5.0	mA
Power Dissipation (Note 2) T _A = +75°C TCA5600 T _A = +85°C TCF5600	P _D	500 650	mW
Thermal Resistance (Junction to Air)	R _{θJA}	100	°C/W
Operating Temperature Range TCA5600 TCF5600	T _A	0 to +75 –40 to +85	°C
Operating Junction Temperature TCA5600 TCF5600	T _J	+125 +150	°C
Storage Temperature Range	T _{stg}	–65 to +150	°C

NOTES:

- Values beyond which damage may occur.
- Derate at 10 mW/°C for junction temperature above +75°C (TCA5600).
Derate at 10 mW/°C for junction temperature above +85°C (TCF5600).

FUNCTIONAL BLOCK DIAGRAM



TCA5600, TCF5600

ELECTRICAL CHARACTERISTICS ($V_{CC1} = V_{CC2} = 12\text{ V}$; $T_J = 25^\circ\text{C}$; $I_{ref} = 0$; $I_{out1} = 0$ (Note 3); $R_{SC} = 0.5\ \Omega$; $INH1 = \text{"High"}$; $INH2 = \text{"High"}$; $WDS = \text{"High"}$; $I_{out2} = 0$ (Note 4); if not otherwise specified)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION						
Nominal Reference Voltage	1	$V_{ref\ nom}$	2.42	2.5	2.58	V
Reference Voltage $I_{ref} = 0.5\text{ mA}$, $T_{low} \leq T_J \leq T_{high}$ (Note 5), $6.0\text{ V} \leq V_{CC1} \leq 18\text{ V}$		V_{ref}	2.4	—	2.6	V
Line Regulation ($6.0\text{ V} \leq V_{CC2} \leq 18\text{ V}$)		Reg_{line}	—	2.0	15	mV
Average Temperature Coefficient $T_{low} \leq T_J \leq T_{high}$ (Note 5)	2	$\frac{\Delta V_{ref}}{\Delta T_J}$	—	—	+/- 0.5	mV/°C
Ripple Rejection Ratio $f = 1.0\text{ kHz}$, $V_{sin} = 1.0\text{ V}_{pp}$	3	RR	60	70	—	dB
Output Impedance $0 \leq I_{ref} \leq 2.0\text{ mA}$		Z_O	—	1.0	—	Ohm
Standby Current Consumption $V_{CC2} = \text{Open}$	4	I_{CC1}	—	3.0	—	mA

NOTES:

- The external PNP power transistor satisfies the following minimum specifications:
 $h_{FE} \geq 60$ at $I_C = 500\text{ mA}$ and $V_{CE} = 5.0\text{ V}$; $V_{CE(sat)} \leq 300\text{ mV}$ at $I_B = 10\text{ mA}$ and $I_C = 300\text{ mA}$
- Regulator V_{out2} programmed for nominal 24 V output by means of R4, R5 (see Figure 1)
- $T_{low} = 0^\circ\text{C}$ for TCA5600; $T_{low} = -40^\circ\text{C}$ for TCF5600.
 $T_{high} = 125^\circ\text{C}$ for TCA5600; $T_{high} = 150^\circ\text{C}$ for TCF5600.

5.0 V MICROPROCESSOR VOLTAGE REGULATOR SECTION

Nominal Output Voltage		$V_{out1(nom)}$	4.8	5.0	5.2	V
Output Voltage $5.0\text{ mA} \leq I_{out1} \leq 300\text{ mA}$, $T_{low} \leq T_J \leq T_{high}$ (Note 5) $6.0\text{ V} \leq V_{CC2} \leq 18\text{ V}$	5 6	V_{out1}	4.75	—	5.25	V
Line Regulation ($6.0\text{ V} \leq V_{CC2} \leq 18\text{ V}$)		Reg_{line}	—	10	50	mV
Load Regulation ($5.0\text{ mA} \leq I_{out1} \leq 300\text{ mA}$)		Reg_{load}	—	20	100	mV
Base Current Drive ($V_{CC2} = 6.0\text{ V}$, $V_{I5} = 4.0\text{ V}$)		I_B	10	15	—	mA
Ripple Rejection Ratio $f = 1.0\text{ kHz}$, $V_{sin} = 1.0\text{ V}_{pp}$	3	RR	50	65	—	dB
Undervoltage Detection Level ($R_{SC} = 5.0\ \Omega$)	7	V_{low}	4.5	$0.93 \times V_{out1}$	—	V
Current Limitation Threshold ($R_{SC} = 5.0\ \Omega$)		V_{RSC}	210	250	290	mV
Average Temperature Coefficient $T_{low} \leq T_J \leq T_{high}$ (Note 5)		$\frac{\Delta V_{out1}}{\Delta T_J}$	—	—	± 1.0	mV/°C

3

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
PROGRAMMABLE VOLTAGE REGULATOR SECTION (Note 6)						
Nominal Output Voltage		$V_{out2(nom)}$	23	24	25	V
Output Voltage $1.0\text{ mA} \leq I_{out2} \leq 100\text{ mA}$, $T_{low} \leq T_J \leq T_{high}$ (Notes 5, 7)	8	V_{out2}	22.8	—	25.2	V
Load Regulation $1.0\text{ mA} \leq I_{out2} \leq 100\text{ mA}$ (Note 7)		Reg_{load}	—	40	200	mV
DC Output Current		I_{out2}	100	—	—	mA
Peak Output Current (Internally Limited)		$I_{out2\ p}$	150	200	—	mA
Ripple Rejection Ratio $f = 20\text{ kHz}$, $V = 0.4\text{ V}_{pp}$		RR	45	55	—	dB
Output Voltage (Fixed 5.0 V) $1.0\text{ mA} \leq I_{out2} \leq 20\text{ mA}$, $T_{low} \leq T_J \leq T_{high}$, INH1 = "High" (Note 5)		$V_{out2(5.0\text{ V})}$	4.75	—	5.25	V
OFF State Output Impedance (INH2 = "Low")		R_{out1}	—	10	—	k Ω
Average Temperature Coefficient $T_{low} \leq T_J \leq T_{high}$ (Note 5)		$\frac{\Delta V_{out2}}{\Delta T_J V_{out2}}$	—	—	± 0.25	mV/ $^{\circ}\text{C}$ V

NOTES:

6. $V_g = 28\text{ V}$, INH1 = "Low" for this Electrical Characteristic section unless otherwise specified.7. Pulse tested $t_p \leq 300\text{ }\mu\text{s}$ **DC/DC CONVERTER SECTION**

Collector Current Detection Level "High" $R_C = 10\text{ k}$ "Low"	9	$V_{12(H)}$ $V_{12(L)}$	350 —	400 50	450 —	mV
Collector Saturation Voltage $I_C = 600\text{ mA}$ (Note 7)	10	$V_{CE(sat)}$	—	—	1.6	V
Rectifier Forward Voltage Drop $I_F = 600\text{ mA}$ (Note 7)	11	V_F	—	—	1.4	V

WATCHDOG AND RESET CIRCUIT SECTION

Threshold Voltage "High" (static) "Low"		$V_{C5(H)}$ $V_{C5(L)}$	— —	2.5 1.0	— —	V
Current Source $T_{low} \leq T_J \leq T_{high}$ (Note 5) Power-Up RESET Watchdog Time Out Watchdog RESET		I_{C5}	— — —	— — —	— — —	μA
Watchdog Input Voltage Swing		V_{WDI}	—	—	± 5.5	V
Watchdog Input Impedance		r_i	12	15	—	k Ω
Watchdog Reset Pulse Width ($C8 = 1.0\text{ nF}$) (Note 9)		t_p	—	—	10	μs

DIGITAL PORTS: \overline{WDS} , INH 1, INH 2, RESET (Note 8)

Input Voltage Range		V_{INP}	—	—	—0.3 to V_{CC1}	V
Input HIGH Current $2.0\text{ V} \leq V_{IH} \leq 5.5\text{ V}$ $5.5\text{ V} \leq V_{IH} \leq V_{CC1}$		I_{IH}	— —	— —	100 150	μA
Input LOW Current $-0.3\text{ V} \leq V_{IL} \leq 0.8\text{ V}$ for INH1, INH2, $-0.3\text{ V} \leq V_{IL} \leq 0.4\text{ V}$ for \overline{WDS}		I_{IL}	—	—	—100	μA
Leakage Current Immunity (INH2, High "Z" State)	12	I_Z	± 20	—	—	μA
Output LOW Voltage RESET ($I_{OL} = 6.0\text{ mA}$)		V_{OL}	—	—	0.4	V
Output HIGH Current RESET ($V_{OH} = 5.5\text{ V}$)		V_{OH}	—	—	20	μA

NOTES:

8. Temperature range $T_{low} \leq T_J \leq T_{high}$ applies to this Electrical Characteristics section.9. For test purposes, a negative pulse is applied to Pin 4 ($-2.5\text{ V} \geq V_4 \geq -5.5\text{ V}$).

TYPICAL CHARACTERISTICS

FIGURE 1 — REFERENCE VOLTAGE versus SUPPLY VOLTAGE

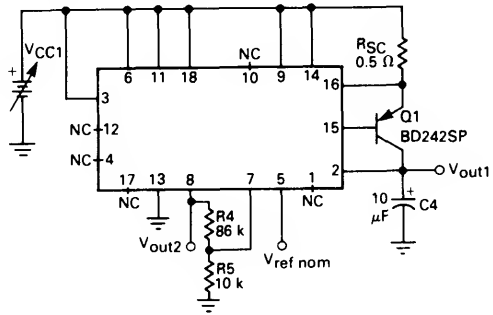
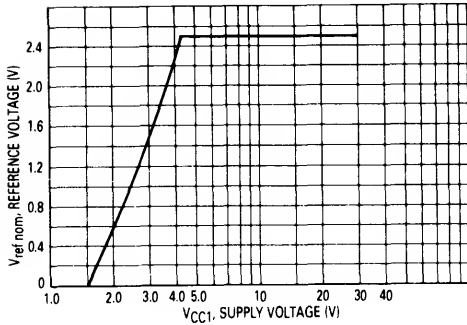


FIGURE 2 — REFERENCE STABILITY versus TEMPERATURE

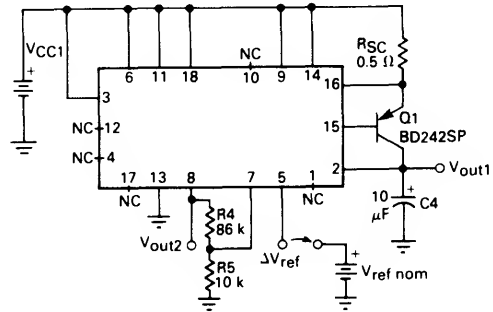
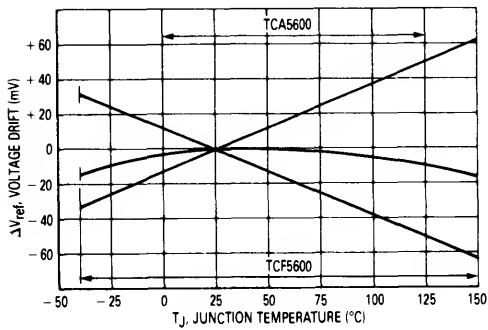
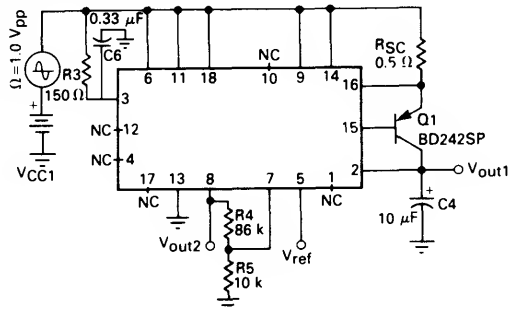
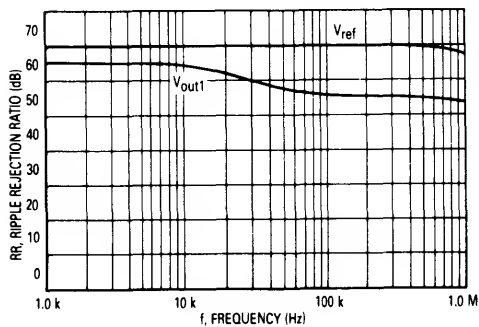


FIGURE 3 — RIPPLE REJECTION versus FREQUENCY



TCA5600, TCF5600

FIGURE 4 — STAND-BY CURRENT versus SUPPLY VOLTAGE

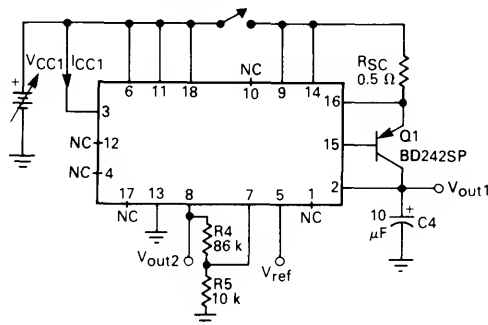
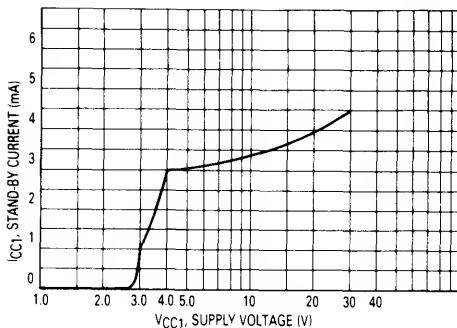


FIGURE 5 — POWER-UP BEHAVIOR OF THE 5.0 V REGULATOR

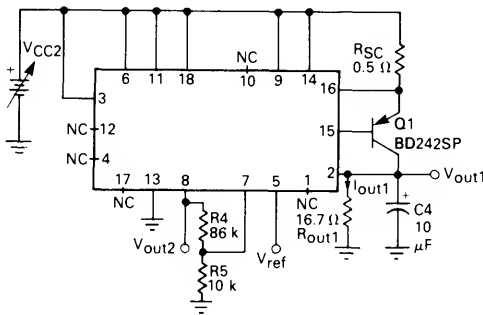
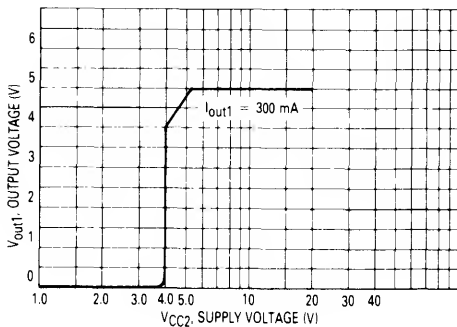
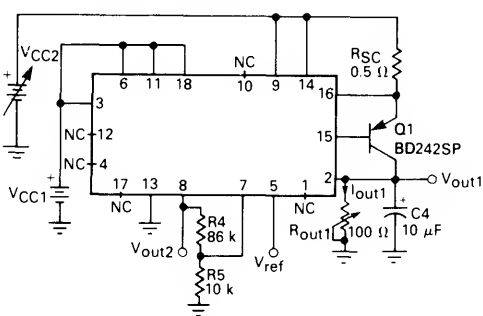
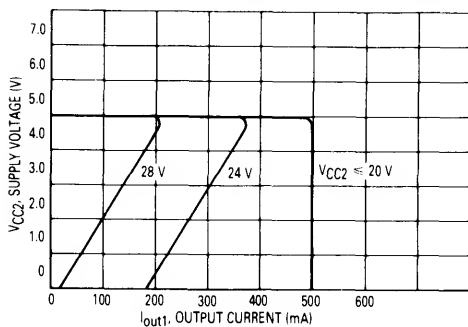


FIGURE 6 — FOLDBACK CHARACTERISTICS OF THE 5.0 V REGULATOR



TCA5600, TCF5600

FIGURE 7 — UNDERVOLTAGE LOCKOUT CHARACTERISTICS

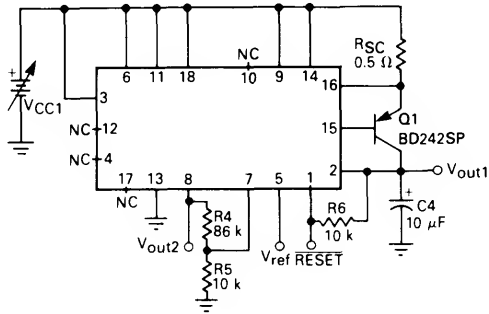
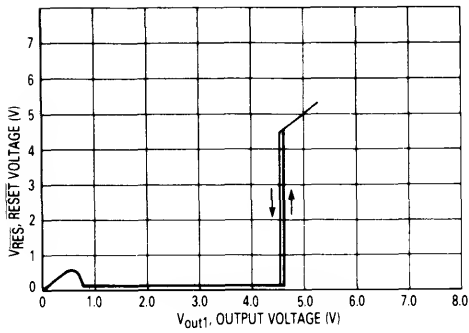


FIGURE 8 — OUTPUT CURRENT CAPABILITY OF THE PROGRAMMING REGULATOR

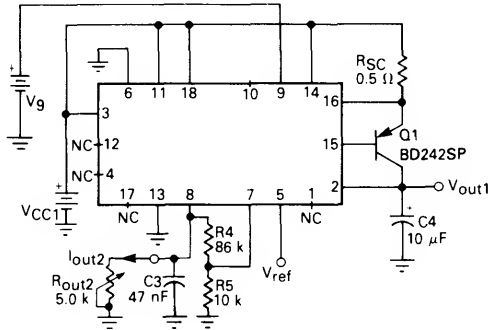
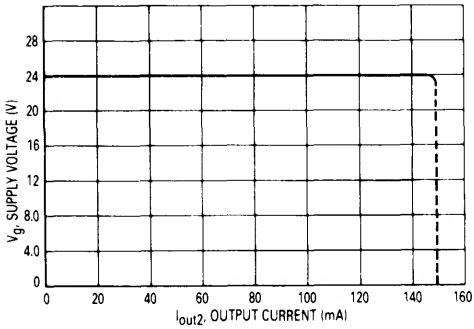
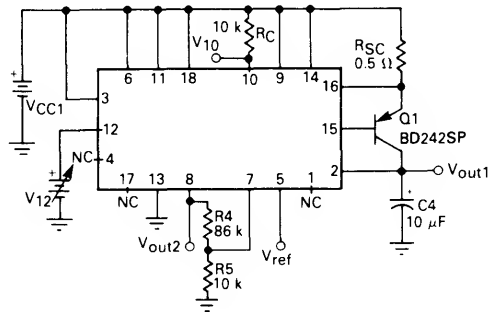
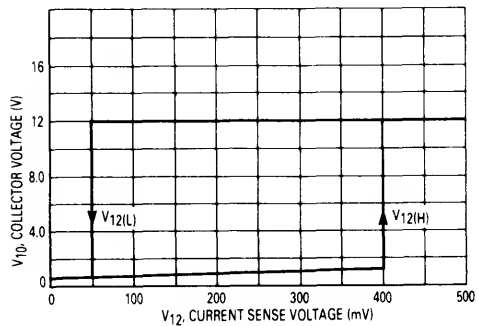


FIGURE 9 — COLLECTOR CURRENT DETECTION LEVEL



TCA5600, TCF5600

FIGURE 10 — POWER SWITCH CHARACTERISTICS

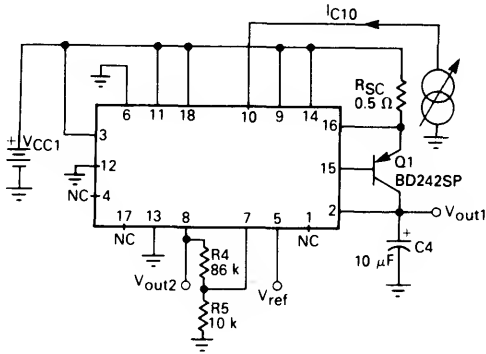
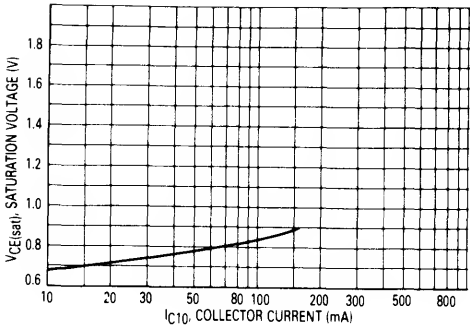


FIGURE 11 — RECTIFIER CHARACTERISTICS

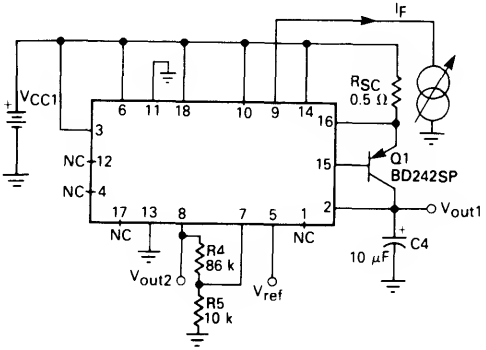
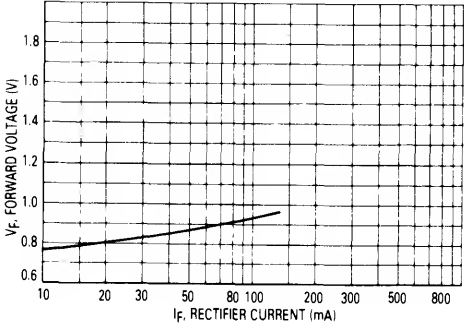
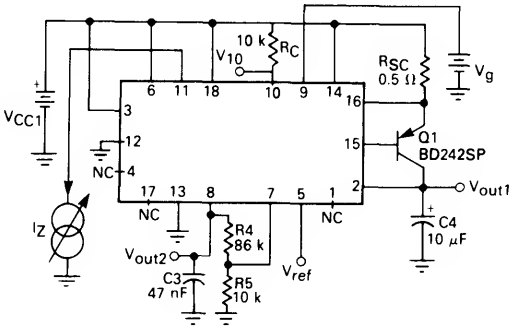
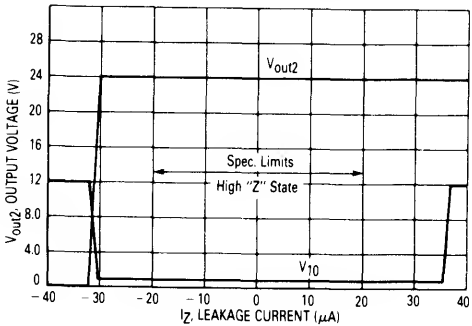


FIGURE 12 — INH 2 LEAKAGE CURRENT IMMUNITY



APPLICATIONS INFORMATION

(See Figure 18)

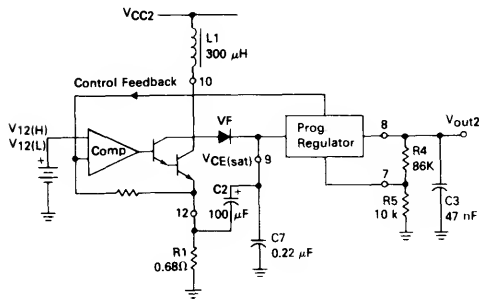
1. VOLTAGE REFERENCE V_{ref}

The voltage reference V_{ref} is based upon a highly stable bandgap voltage reference and is accessible on Pin 5 for additional tasks. This circuit part has its own supply connection on Pin 3 and is therefore able to operate in standby mode. The RC network R3, C6 improves the ripple rejection on both regulators.

2. DC/DC CONVERTER

The dc/dc converter performs according to the fly back principle and does not need a time base circuit. The maximum coil current is well defined by means of the current sensing resistor R1 under all working conditions (start-up phase, circuit overload, wide supply voltage range and extreme load current change). Figure 13 shows the simplified converter schematic:

FIGURE 13 — SIMPLIFIED CONVERTER SCHEMATIC



A simplified method on "how to calculate the coil inductance" is given below. The operation point at min. supply voltage (V_{CC2}) and max. output current (I_{out2}) for a fixed output voltage (V_{out2}) determines the coil data. Figure 14 shows the typical voltage and current wave forms on the coil L1 (coil losses neglected).

The equations (1) and (2) yield the respective coil voltage V_L - and V_L - (see Figure 14):

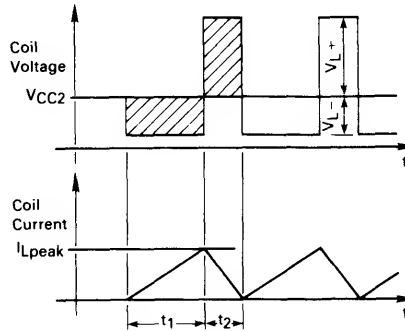
$$V_L + = V_{out2} + \Delta V(\text{Pin } 9 - \text{Pin } 8) + V_F - V_{CC2} \quad (1)$$

$$V_L - = V_{CC2} - V_{CE(sat)} - V_{12(H)} \quad (2)$$

($\Delta V(\text{Pin } 9 - \text{Pin } 8)$: input/output voltage drop of the regulator, 2.5 V typical)

($V_F, V_{CE(sat)}, V_{12(H)}$: see electrical characteristics)

FIGURE 14 — VOLTAGE AND CURRENT WAVEFORM ON THE COIL (not to scale)



The time ratio α for the charging time to dumping time is defined by equation (3):

$$\alpha = \frac{t_1}{t_2} = \frac{V_L +}{V_L -} \quad (3)$$

The coil charging time t_1 is found using equation (4):

$$t_1 = \frac{1}{(1 + \frac{1}{\alpha}) \cdot f} \quad (4)$$

(f : min. oscillation frequency which should be chosen above the audio frequency band (e.g. 20 kHz))

Knowing the dc output current I_{out2} of the programmable regulator, the peak coil current $I_{L(peak)}$ can now be calculated:

$$I_{L(peak)} = 2 \cdot I_{out2} \cdot (1 + \alpha) \quad (5)$$

The coil inductance L1 of the nonsaturated coil is given by equation (6):

$$L1 = \frac{t_1}{I_{L(peak)}} \cdot V_L - \quad (6)$$

The formula (6a) yields the current sensing resistor R1 for a defined peak coil current $I_{L(peak)}$:

$$R1 = \frac{V_{12(H)}}{I_{L(peak)}} \quad (6a)$$

In order to limit the by-pass current through capacitor C7 during the energy dumping phase the value $C2 \gg C7$ should be implemented.

For all other operation conditions, the feedback signal from the programmable voltage regulator controls the activity of the converter.

3. PROGRAMMABLE VOLTAGE REGULATOR

This series voltage regulator is programmable by the voltage divider R4, R5 for a nominal output voltage $6.0 \text{ V} \leq V_{\text{out}2} \leq 30 \text{ V}$.

$$R4 = \frac{(V_{\text{out}2} - V_{\text{ref nom}}) \cdot R5}{V_{\text{ref nom}}} \quad (7)$$

$$(R5 = 10 \text{ k}, V_{\text{ref nom}} = 2.5 \text{ V})$$

Current limitation and thermal shutdown capability are standard features of this regulator. The voltage drop $\Delta V(P_{\text{in}9} - P_{\text{in}8})$ across the series pass transistor generates the feedback signal to control the dc/dc converter (see Figure 13).

4. CONTROL INPUTS INH1, INH2

The dc/dc converter and/or the regulator $V_{\text{out}2}$ are remote controllable through the TTL, MOS compatible inhibit inputs INH1 and INH2 where the latter is a 3-level detector (Logic "0", high impedance "Z", Logic "1"). Both inputs are setup to provide the following truth table:

FIGURE 15 — INH1, INH2 TRUTH TABLE

Mode	INH1	INH2	$V_{\text{out}2}$	dc/dc
1	0	0	OFF	INT
2	0	High "Z"	$V_{\text{out}2}$	ON
3	0	1	$V_{\text{out}2}$	INT
4	1	0	OFF	INT
5	1	High "Z"	5.0 V	ON
6	1	1	5.0 V	INT

INT: Intermittent operation of the converter means that the converter operates only if $V_{\text{CC}2} < V_{\text{out}2}$.

ON: The converter loads the storage capacitor C2 to its full charge ($V_g = 33 \text{ V}$), allowing fast response time of the regulator $V_{\text{out}2}$ when addressed by the control software.

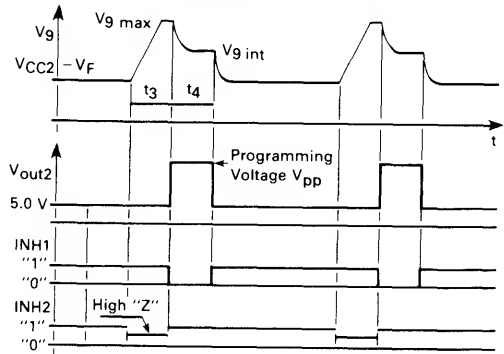
OFF: High impedance (internal resistor 10 k to ground)

Figure 16 represents a typical timing diagram for an E²PROM programming sequence in a microprocessor based system. The high "Z" state enables the dc/dc converter to ramp during t_3 to the voltage V_g at Pin 9 to a high level before the write cycle takes place in the memory.

5. MICROPROCESSOR SUPPLY REGULATOR

Together with an external PNP power transistor (Q1), a 5.0 V supply exhibiting low voltage drop is obtained to power microprocessor systems and auxiliary circuits. Using a power Darlington with adequate heat sink in the output stage boosts the output current $I_{\text{out}1}$ above 1 amp.

FIGURE 16 — TYPICAL E²PROM PROGRAMMING SEQUENCE (not to scale)



The current limitation circuit measures the emitter current of Q1 by means of the sensing resistor R_{SC} :

$$R_{\text{SC}} = \frac{V_{\text{RSC}}}{I_E} \quad (8)$$

(I_E : emitter current of Q1)

(V_{RSC} : threshold voltage (see electrical characteristics))

The voltage protection circuit performs a fold-back characteristic above a nominal operating voltage $V_{\text{CC}2} \geq 18 \text{ V}$.

6. DELAY AND WATCHDOG CIRCUIT

The under voltage monitor supervises the power supply $V_{\text{out}1}$ and releases the delay circuit RESET as soon as the regulator output reaches the microprocessor operating range (e.g. $V_{\text{LOW}} \geq 0.93 \cdot V_{\text{out}1(\text{nom})}$). The RESET output has an open-collector and may be connected in a "wired-OR" configuration.

The watchdog circuit consists of a retriggerable monostable with a negative edge sensitive control input WDI. The watchdog feature may be disabled by means of the watchdog select input WDS driven to a "1". Figure 17 displays the typical RESET timing diagram.

The commuted current source $I_{\text{C}5}$ on Pin 17, threshold voltage $V_{\text{C}5(\text{L})}$, $V_{\text{C}5(\text{H})}$ and an external capacitor C5 define the RESET delay and the watchdog timing. The relationship of the timing signals are indicated by the equations (9) to (11).

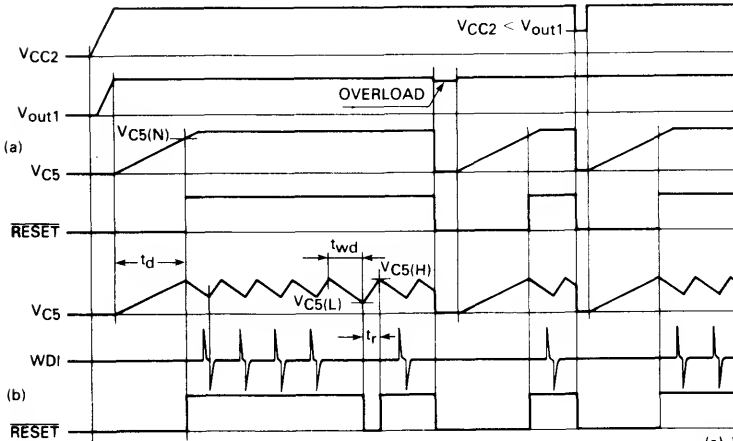
$$\text{RESET delay: } t_d = \frac{C5 \cdot V_{\text{C}5(\text{H})}}{I_{\text{C}5}} \quad (9)$$

$$\text{Watchdog time-out: } t_{\text{wd}} = \frac{C5 \cdot (V_{\text{C}5(\text{H})} - V_{\text{C}5(\text{L})})}{5 \cdot I_{\text{C}5}} \quad (10)$$

$$\text{Watchdog RESET: } t_r = \frac{C5 \cdot (V_{\text{C}5(\text{H})} - V_{\text{C}5(\text{L})})}{50 \cdot I_{\text{C}5}} \quad (11)$$

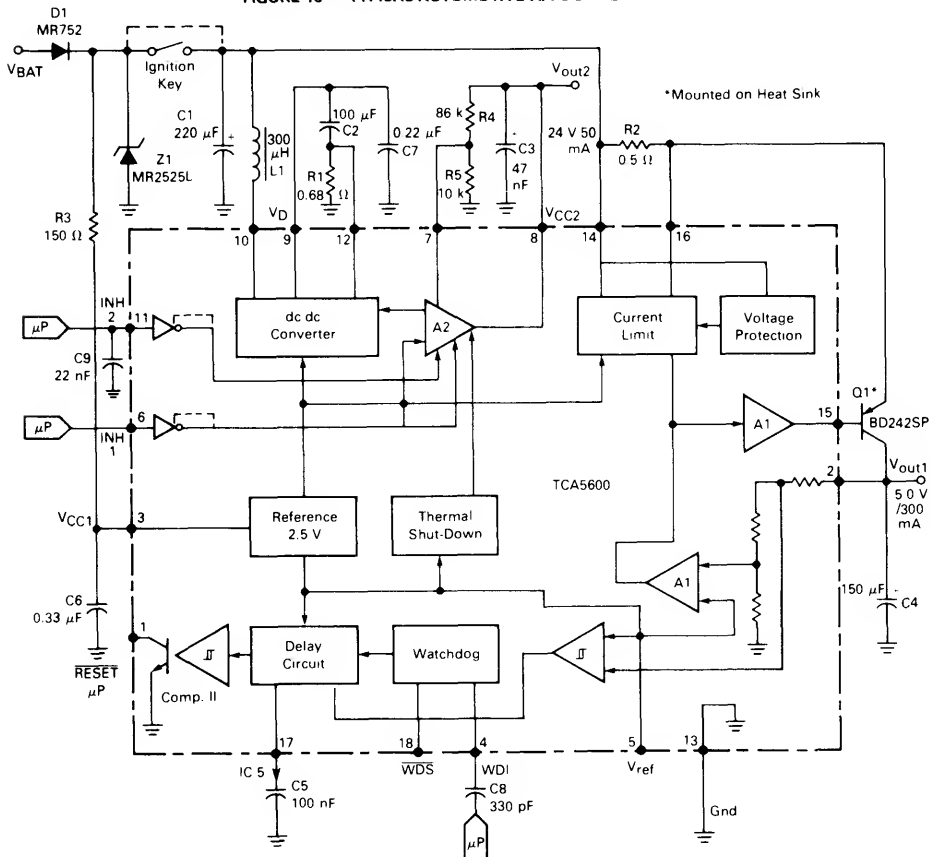
($I_{\text{C}5}$, $V_{\text{C}5(\text{H})}$, $V_{\text{C}5(\text{L})}$: see electrical characteristics.)

FIGURE 17 — TYPICAL RESET TIMING DIAGRAM
(not to scale)



(a) Watchdog inhibited, $\overline{WDS} = "1"$
(b) Watchdog operational, $\overline{WDS} = "0"$

FIGURE 18 — TYPICAL AUTOMOTIVE APPLICATION



Advance Information

CONTROL IC FOR LINE-ISOLATED FREE RUNNING FLYBACK CONVERTER

The bipolar integrated circuit TDA4601 drives, regulates and monitors the switching transistor in a power supply based on the ringing choke flyback principle.

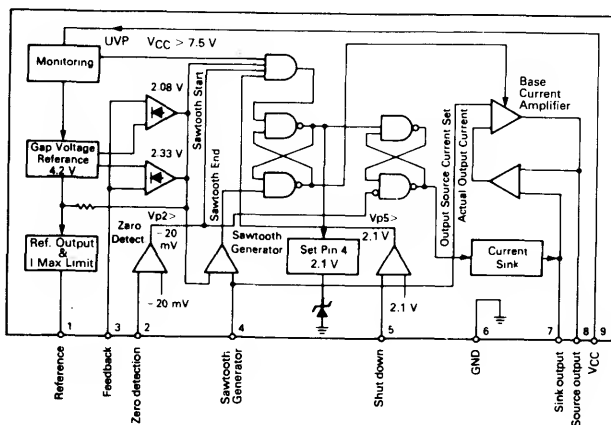
Due to the wide regulating range and the high voltage stability during large load changes, SMPS for Hi-Fi equipment and active loudspeakers can be realized as well as applications in TV receivers and video recorders.

The TDA4601 is available in a 9-pin plastic medium power SIP package. The operating temperature range is -15°C to $+85^{\circ}\text{C}$.

- Wide Operational Range
- High Voltage Stability Even at High Load Changes
- Direct Control of Switching Transistor
- Low Start-Up Current
- Linear Foldback of the Overload Characteristic
- Base Drive Proportional to the Current Through the Power Switching Transistor
- Standby Mode 3.5 W into the External Load
- Inhibit Capability (TTL Compatible)
- Undervoltage Lockout

For Application Details See ANE002

BLOCK DIAGRAM

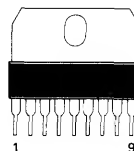


This document contains information on a new product. Specifications and information herein are subject to change without notice.

TDA4601

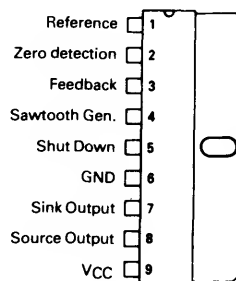
FLYBACK CONVERTER CONTROL CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT



PLASTIC
 MEDIUM POWER
 PACKAGE
 CASE 762

PIN ASSIGNMENTS



ORDERING INFORMATION

Device	Temperature Range	Package
TDA4601	-15°C to $+85^{\circ}\text{C}$	Plastic SIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V _g	20	V
Sink Output Voltage	V ₇ V ₇ -V ₈	0 to V _g ±6.0	V V
Reference Output	I ₁	-10 to +1.0	mA
Zero Crossing	I ₂	-3.0 to +3.0	mA
Control Amplifier	I ₃	-3.0 to 0	mA
Collector Current	I ₄	-2.0 to +5.0	mA
Trigger Input	I ₅	-2.0 to +3.0	mA
Sink Output	I ₇	-1.5	A
Junction Temperature	T _J	+150	°C
Storage Temperature	T _{stg}	-40 to +125	°C
Thermal Resistance (Junction to Air)	θ _{JA}	70	°C/W
Thermal Resistance (Junction to Case)	θ _{JC}	15	°C/W

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise stated)

Range of Operation	Symbol	Fig. No.	Min	Typ	Max	Unit
Supply Voltage	V _g		—	15	18	V
Ambient Temperature	T _A		-15	—	85	°C

START OPERATION T_A = 25°C

Current Consumption (V ₁ Not Yet Switched) V _g = 3.0 V V _g = 5.0 V V _g = 10 V	I _g	1	— — —	— 1.5 2.0	0.5 2.0 3.2	mA
Turn-On Point for V ₁	V _g	1	11.3	11.8	12.3	V
V ₄ Before Start-Up (V _g < 11.8 V)	V ₄	1	6.0	6.7	—	V

REGULATION MODE V_g = 15 V T_A = 25°C

Current Consumption V _{reg} = -10 V V _{reg} = 0	I _g	1	110 55	135 85	160 110	mA
Reference Voltage I ₁ < 0.1 mA I ₁ = 5.0 mA	V ₁	1	4.0 4.0	4.2 4.2	4.5 4.4	V
Reference Voltage Temperature Coefficient	TC ₁	1	—	100	—	ppm/°C
V _{Pin 4} Low Static Voltage	V ₄	1	1.8	2.08	2.5	V
V _{Pin 4} Regulation Peak Voltage I _{Pin 3} = 5.0 μA I _{Pin 3} = 1.3 mA	V ₄ peak	1	4.0 —	4.2 2.4	4.5 3.0	V
V _{Pin 3} Full Fold Back I _{Pin 3} = 1.3 mA Fold Back I _{Pin 3} = 0.5 mA Overload Decision I _{Pin 3} = 1.0 μA V _{Pin 3} Regulation I _{Pin 3} Regulation I _{Pin 3} Leakage at V _{Pin 3} = 1.5 V	V ₃	1	— — — —	3.7 2.5 2.4 2.11	4.0 3.0 2.9 —	V
	I ₃	1	— —	1.0 0.4	— —	μA
V _{Pin 7} Peak High V _R = 0 V (Full Fold Back) V _R = -10 V (Regulation) V _R = -15 V (Standby)	V ₇ peak	1	— — —	3.5 4.0 5.0	— — —	V
	V ₇ peak	1	— — —	1.4 1.45 1.57	— — —	V

TDA4601

ELECTRICAL CHARACTERISTICS (continued) ($T_A = 25^\circ\text{C}$ unless otherwise noted.)

Range of Operation	Symbol	Fig. No.	Min	Typ	Max	Unit
REGULATION MODE (continued) $V_g = 15\text{ V}$ $T_A = 25^\circ\text{C}$						
$I_{\text{Pin 7 Sink Peak}}$ $V_R = -15\text{ V}$	$I_7 \text{ peak}$	1	—	+0.7	—	A
$I_{\text{Pin 8 Source Peak}}$ $V_R = -15\text{ V}$	$I_8 \text{ peak}$	1	—	-0.8	—	A
$V_{\text{Pin 2}}$ $I_{\text{Pin 2}} = -3.0\text{ mA}$ $= -0.3\text{ mA}$ $+3.0\text{ mA}$ $+0.3\text{ mA}$	V_2	1	— — — —	-0.3 -0.2 +0.7 +0.8	— — — —	V
PROTECTIVE OPERATION $V_g = 15\text{ V}$ $T_A = 25^\circ\text{C}$						
Current Consumption ($V_5 < 1.8\text{ V}$)	I_g	1	14	20	26	mA
Turn-Off Voltage ($V_5 < 1.8\text{ V}$)	V_7 V_4	1 1	1.3 1.8	1.5 2.1	1.8 2.5	V
External Trigger Input Enable Voltage ($V_{\text{reg}} = 0\text{ V}$) Disabled Voltage ($V_{\text{reg}} = 0\text{ V}$)	V_5	1	— 2.0	2.2 2.2	2.4 —	V
Supply Voltage Disabling V_g and V_1	V_g	1	6.7	7.4	7.8	V
$V_{\text{Pin 5 Zener Voltage}}$ (Pin 5 Open)	V_5	1	6.5	7.3	7.8	V
$I_{\text{Pin 5}}$ $V_{\text{Pin 5}} = 3.0\text{ V}$ $V_{\text{Pin 5}} = 0\text{ V}$	I_5	1	— —	1.4 -11	— —	μA
Turn-On Time (Secondary Voltages)	t_{on}	2	—	350	450	ms
Voltage Change When $S_3 = \text{Closed}$ ($\Delta P_3 = 19\text{ W}$) When $S_2 = \text{Closed}$ ($\Delta P_2 = 15\text{ W}$)	ΔV_2	2	— —	100 500	500 1000	mV
Standby Operation (Minimum Secondary Power: 3.0 Watts) When $S_1 = \text{Open}$	ΔV_2	2	—	20	30	V
Switching Frequency During Standby Mode	f	2	70	75	—	kHz
Primary Power Consumption During Standby Mode The heatsink must be optimized, taking the maximum data (T_J, θ_{JC}, T_A) into consideration	P_{prim}	2	—	10	15	VA

CIRCUIT DESCRIPTION

The TDA4601 regulates, controls and protects the switching transistor in flyback converter power supplies at starting-up, normal, and overload operation.

A. Start-Up Sequence

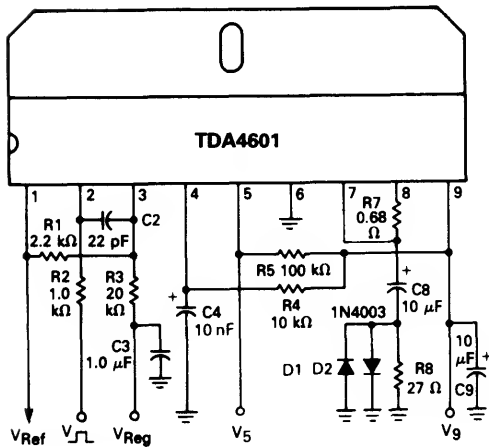
During start-up there are three consecutive operations:

1. An internal reference voltage is created. It supplies the voltage regulator and enables the supply to the coupling electrolytic capacitor and the switching transistor. For a supply voltage (V_g) of 12 V, the current is less than 3.2 mA.

2. Activation of the internal reference voltage $V_1 = 4.0\text{ V}$. This voltage is suddenly available when V_g reaches 12 V and enables all parts of the IC to be supplied from the control logic including thermal and overload protection.
3. Activation of the control logic. As soon as the reference voltage is available, the control is switched on through an additional stabilization circuit.

This start-up sequence is necessary for smoothly driving the switching transistor through the coupling electrolytic capacitor.

FIGURE 1 — TEST CONFIGURATION



B. Normal Operation

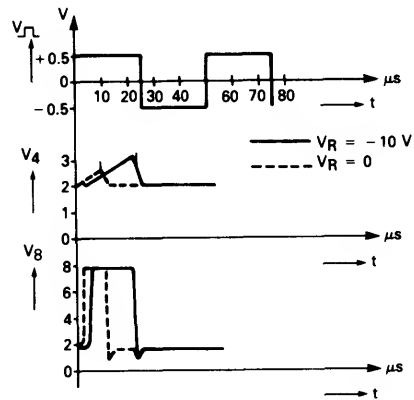
Zero crossing detection is sensed on Pin 2 and linked to the control logic.

The signal picked up on the feedback winding is applied, after filtering, to Pin 3 (used for input regulation and for overload protection). The regulating section works with an input voltage of about 2.0 V for normal regulation and a current of about 1.4 mA for foldback operation. Together with the collector current simulation Pin 4, the overload recognition defines the operating region of the regulating amplifier depending on the internal reference voltage. The simulation of the collector current is generated by an external RC network at Pin 4 and an internally set voltage level.

For a constant line voltage and for a given output power on the load (t on fixed) less than the maximum output power, a decrease of $C4$ produces an increase of the current sent to the base of the power switching transistor. So the foldback point is reached earlier. The regulation range starts from a 2.0 Vdc level which is the bottom of a sawtooth waveform; the maximum is limited at 4.0 V (reference voltage).

A secondary load of 19 W produces a switching frequency of about 50 kHz at an almost constant duty cycle (approximately 3). Furthermore, when the switchmode power supply delivers approximately 3.0 W, the switching frequency jumps to about 70 kHz at a duty cycle of approximately 11. At the same time, the collector peak current falls below 1.0 A.

FIGURE 2 — TEST DIAGRAM: NORMAL OPERATION



The comparison of the output level of the regulating amplifier, the overload detection and the collector current simulation drives the control logic. An additional steering control and blocking possibility is offered thru Pin 5. When the voltage applied on Pin 5 falls below 2.2 V then the source output (Pin 8) is blocked.

The control logic is set according to the start-up circuit, the zero crossing detection and the trigger enabling. This logic drives the base current amplifier and the base current shutdown. The base current amplifier drives the source output (Pin 8) proportionally to the sawtooth voltage (Pin 4). A current feedback is performed by an external shunt inserted between Pin 8 and the base of the switching power transistor. This resistor determines the maximum amplitude of the base current drive.

C. Protective Features

The base current shut-down, released by the control logic, clamps the sink output (Pin 7) at 1.6 V, turning off the switching transistor. This feature will be released if the voltage on Pin 9 is less than 7.4 V, or if the applied voltage on Pin 5 is less than 2.2 V. In case of a short circuit of the secondary windings, the TDA4601 continuously monitors the fault condition.

In standby operation the circuit is set to a high duty cycle. The total power consumption of the power supply is held below 6.0 to 10 W.

FIGURE 3 — FREQUENCY versus OUTPUT POWER

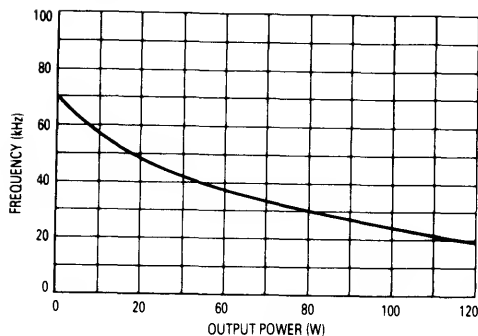
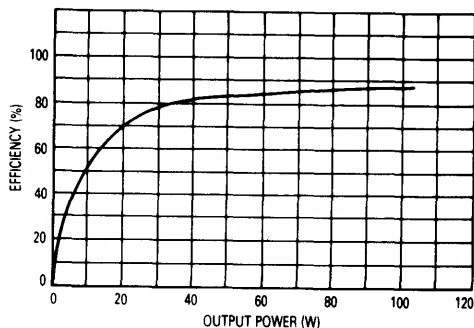
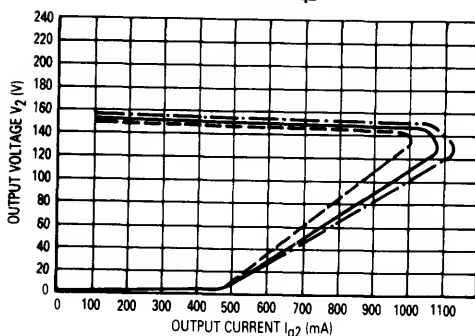
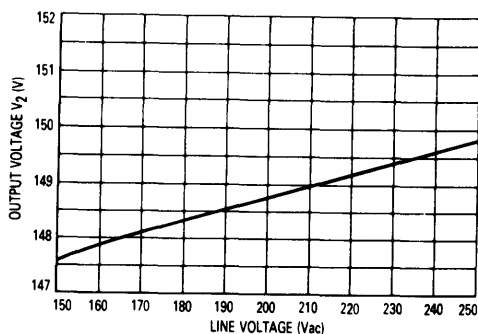


FIGURE 4 — EFFICIENCY versus OUTPUT POWER

FIGURE 5 — OUTPUT VOLTAGE (V_2) versus OUTPUT CURRENT (I_{Q2})FIGURE 6 — OUTPUT VOLTAGE (V_2) versus LINE VOLTAGE

TEST CIRCUIT AND TYPICAL APPLICATION (See Figure 7)

This application circuit shown in Figure 2 represents a blocking converter for color TV sets with 30 W to 120 W of output power and line voltages from 160 to 270 V.

In spite of regulation on the primary side, good voltage stability of the various secondary voltages is achieved even with large load changes.

For line voltage isolation and transformation to the desired secondary voltages, a transformer with ferrite core is used.

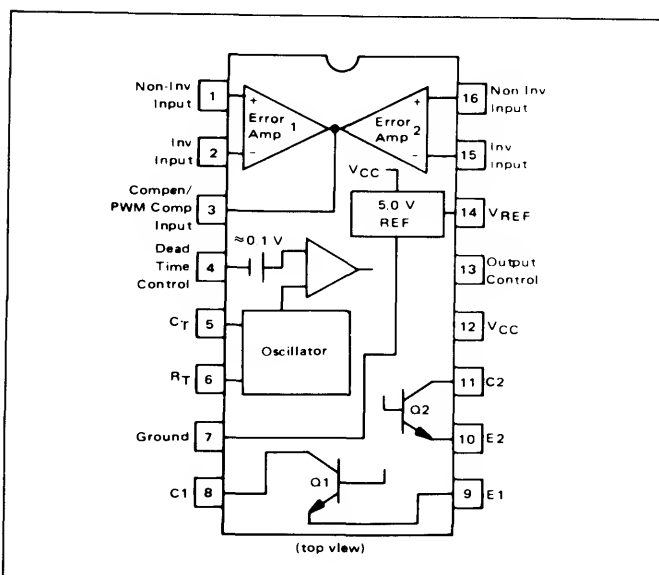
SPECIAL FEATURES OF THE FLYBACK CONVERTER POWER SUPPLY USING THE TDA4601

- Direct driving of the power switching transistor
- Low starting current, defined starting behavior also at slowly rising line voltage
- Short circuit proof and open-loop resistant circuit. In both cases a power of only 6.0 to 10 W is consumed. Linear foldback characteristic at overload.
- Automatic restart after elimination of the overload.
- Efficiency of more than 80% at an output power of 40 to 100 W.
- Frequency of oscillation between 20 kHz (100 W) and 70 kHz (without load).
- Simple RF1 suppression
- Good regulation of load current and line voltage variations. At a line voltage variation between 170 and 240 V the output voltage of 150 V will change approximately 2.0 V.

**SWITCHMODE
PULSE WIDTH MODULATION
CONTROL CIRCUITS**

The TL494 is a fixed frequency, pulse width modulation control circuit designed primarily for Switchmode power supply control. This device features:

- Complete Pulse Width Modulation Control Circuitry
- On-Chip Oscillator With Master Or Slave Operation
- On-Chip Error Amplifiers
- On-Chip 5 Volt Reference
- Adjustable Dead-Time Control
- Uncommitted Output Transistors Rated to 500 mA Source Or Sink
- Output Control For Push-Pull Or Single-Ended Operation
- Undervoltage Lockout



The TL494C is specified over the commercial operating range of 0°C to 70°C. The TL494I is specified over the industrial range of -25°C to 85°C. The TL494M is specified over the full military range of -55°C to 125°C.

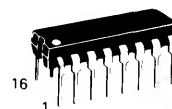
TL494

**SWITCHMODE
PULSE WIDTH MODULATION
CONTROL CIRCUITS**

**SILICON MONOLITHIC
INTEGRATED CIRCUITS**



J SUFFIX
CERAMIC PACKAGE
CASE 620



N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

Device	Temperature Range	Package
TL494CN	0° to +70°C	Plastic DIP
TL494CJ		Ceramic DIP
TL494IN	-25° to +85°C	Plastic DIP
TL494IJ		Ceramic DIP
TL494MJ	-55° to +125°C	Ceramic DIP

FIGURE 1 — BLOCK DIAGRAM

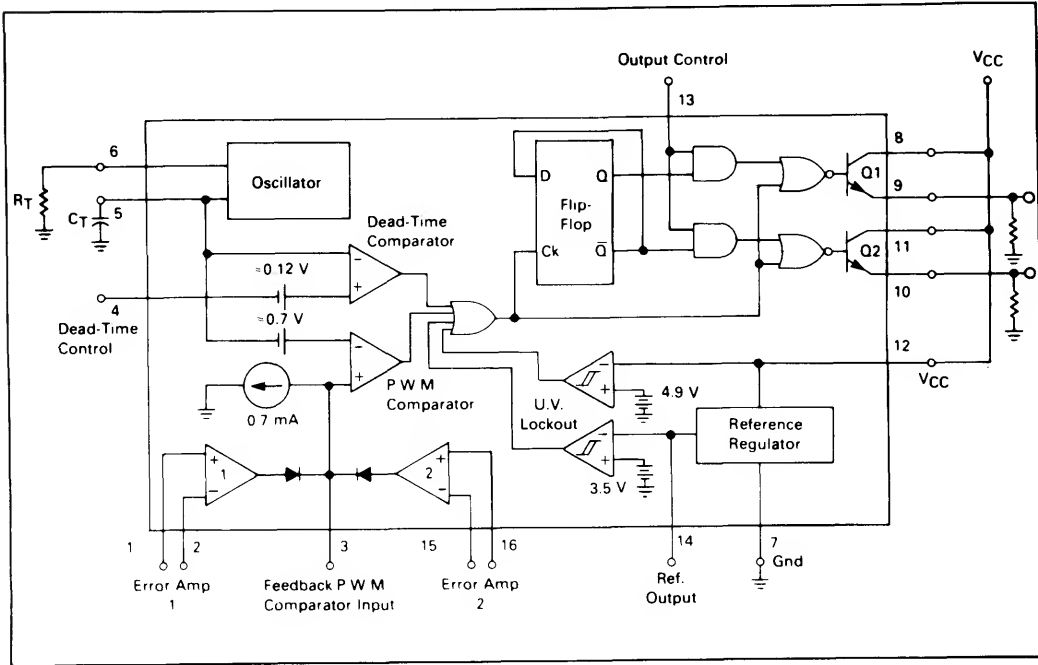
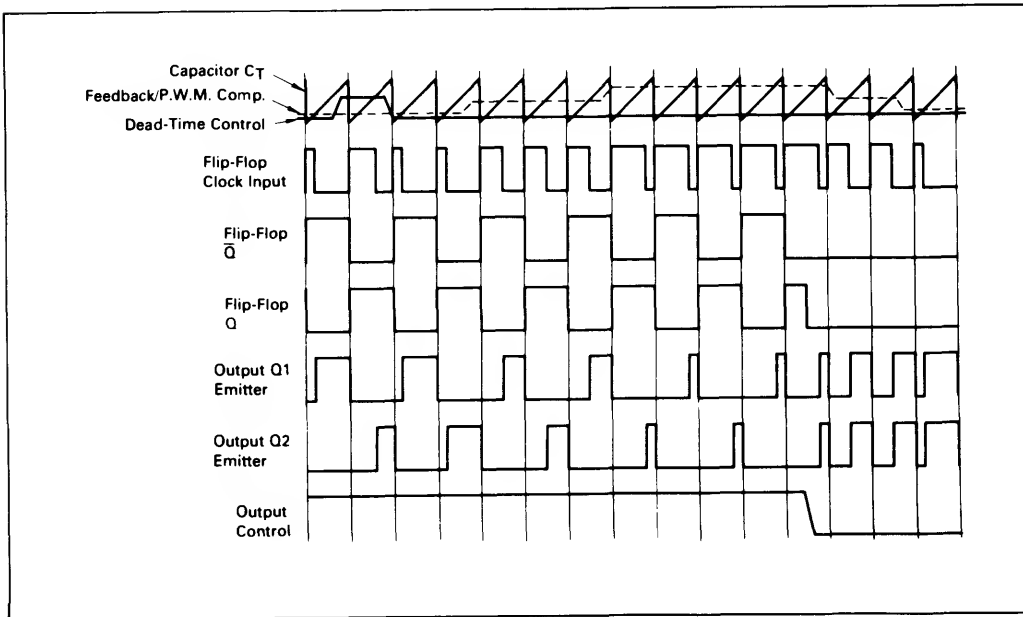


FIGURE 2 — TIMING DIAGRAM



Description

The TL494 is a fixed-frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply. (See Figure 1.) An internal-linear sawtooth oscillator is frequency-programmable by two external components, R_T and C_T . The approximate oscillator frequency is determined by:

$$f_{osc} \approx \frac{1.1}{R_T \bullet C_T}$$

For more information refer to Figure 4.

Output pulse width modulation is accomplished by comparison of the positive sawtooth waveform across capacitor C_T to either of two control signals. The NOR gates, which drive output transistors Q1 and Q2, are enabled only when the flip-flop clock-input line is in its low state. This happens only during that portion of time when the sawtooth voltage is greater than the control signals. Therefore, an increase in control-signal amplitude causes a corresponding linear decrease of output pulse width. (Refer to the timing diagram shown in Figure 2.)

The control signals are external inputs that can be fed into the dead-time control, the error amplifier inputs, or the feedback input. The dead-time control comparator has an effective 120 mV input offset which limits the minimum output dead time to approximately the first 4% of the sawtooth-cycle time. This would result in a maximum duty cycle on a given output of 96% with the output control grounded, and 48% with it connected to the reference line. Additional dead time may be imposed on the output by setting the dead time-control input to a fixed voltage, ranging between 0 to 3.3 V.

The pulse width modulator comparator provides a means for the error amplifiers to adjust the output pulse width from the maximum percent on-time, established by the dead time control input, down to zero, as the voltage at the feedback pin varies from 0.5 to 3.5 V. Both error amplifiers have a common-mode input range from -0.3 V to ($V_{CC} - 2$ V), and may be used to sense power-supply output voltage and current. The error-amplifier outputs are active high and are ORed together at the non-inverting input of the pulse-width modulator comparator. With this configuration, the amplifier that demands minimum output on time, dominates control of the loop.

When capacitor C_T is discharged, a positive pulse is generated on the output of the dead-time comparator, which clocks the pulse-steering flip-flop and inhibits the output transistors, Q1 and Q2. With the output-control connected to the reference line, the pulse-steering flip-flop directs the modulated pulses to each of the two output transistors alternately for push-pull operation. The output frequency is equal to half that of the oscillator. Output drive can also be taken from Q1 or Q2, when single-ended operation with a maximum on-time of less than 50% is required. This is desirable when the output transformer has a ringback winding with a catch diode used for snubbing. When higher output-drive currents are required for single-ended operation, Q1 and Q2 may be connected in parallel, and the output-mode pin must be tied to ground to disable the flip-flop. The output frequency will now be equal to that of the oscillator.

The TL494 has an internal 5 V reference capable of sourcing up to 10 mA of load current for external bias circuits. The reference has an internal accuracy of $\pm 5.0\%$ with a typical thermal drift of less than 50 mV over an operating temperature range of 0 to 70°C.

FIGURE 3 — FUNCTIONAL TABLE

Input	Output Function	$\frac{f_{out}}{f_{osc}} =$
Output Control		
Grounded	Single-ended P.W.M. at Q1 and Q2	1
At V_{ref}	Push-pull operation	0.5

TL494

3

MAXIMUM RATINGS (Full operating ambient temperature range applies unless otherwise noted)

Rating	Symbol	TL494C	TL494I	TL494M	Unit
Power Supply Voltage	V_{CC}	42	42	42	V
Collector Output Voltage	V_{C1}, V_{C2}	42	42	42	V
Collector Output Current (each transistor) (1)	I_{C1}, I_{C2}	500	500	500	mA
Amplifier Input Voltage Range	V_{IR}	-0.3 to 42	-0.3 to 42	-0.3 to 42	V
Power Dissipation (α $T_A \leq 45^\circ\text{C}$)	P_D	1000	1000	1000	mW
Operating Junction Temperature	T_J				$^\circ\text{C}$
Plastic Package		125	125	—	$^\circ\text{C}$
Ceramic Package		150	150	150	$^\circ\text{C}$
Operating Ambient Temperature Range	T_A	0 to 70	-25 to 85	-55 to 125	$^\circ\text{C}$
Storage Temperature Range	T_{stg}				$^\circ\text{C}$
Plastic Package		-55 to 125	-55 to 125	—	
Ceramic Package		-65 to 150	-65 to 150	-65 to 150	

NOTE 1: Maximum thermal limits must be observed.

THERMAL CHARACTERISTICS

Characteristics	Symbol	N Suffix Plastic Package	J Suffix Ceramic Package	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	80	100	$^\circ\text{C/W}$
Derating Ambient Temperature	T_A	45	50	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS

Condition/Value	Symbol	TL494			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	7.0	15	40	V
Collector Output Voltage	V_{C1}, V_{C2}	—	30	40	V
Collector Output Current (each transistor)	I_{C1}, I_{C2}	—	—	200	mA
Amplifier Input Voltage	V_{in}	-0.3	—	$V_{CC} - 2.0$	V
Current Into Feedback Terminal	I_{fb}	—	—	0.3	mA
Reference Output Current	I_{ref}	—	—	10	mA
Timing Resistor	R_T	1.8	30	500	k Ω
Timing Capacitor	C_T	0.0047	0.001	10	μF
Oscillator Frequency	f_{osc}	1.0	40	200	kHz

ELECTRICAL CHARACTERISTICS ($V_{CC} = 15\text{ V}$, $C_T = 0.01\text{ }\mu\text{F}$, $R_T = 12\text{ k}\Omega$ unless otherwise noted.)

For typical values $T_A = 25^\circ\text{C}$, for min max values T_A is the operating ambient temperature range that applies unless otherwise noted.

Characteristic	Symbol	TL494C,I			TL494M			Unit
		Min	Typ	Max	Min	Typ	Max	

REFERENCE SECTION

Reference Voltage ($I_O = 1.0\text{ mA}$)	V_{ref}	4.75	5.0	5.25	4.75	5.0	5.25	V
Line Regulation ($V_{CC} = 7.0\text{ V to }40\text{ V}$)	Reg_{line}	—	2.0	25	—	2.0	25	mV
Load Regulation ($I_O = 1.0\text{ mA to }10\text{ mA}$)	Reg_{load}	—	3.0	15	—	3.0	15	mV
Short-Circuit Output Current ($V_{ref} = 0\text{ V}$)	I_{SC}	15	35	75	15	35	75	mA

TL494

ELECTRICAL CHARACTERISTICS ($V_{CC} = 15\text{ V}$, $C_T = 0.01\text{ }\mu\text{F}$, $R_T = 12\text{ k}\Omega$ unless otherwise noted.)

For typical values $T_A = 25^\circ\text{C}$, for min/max values T_A is the operating ambient temperature range that applies unless otherwise noted.

Characteristic	Symbol	TL494C,I			TL494M			Unit
		Min	Typ	Max	Min	Typ	Max	

OUTPUT SECTION

Collector Off-State Current ($V_{CC} = 40\text{ V}$, $V_{CE} = 40\text{ V}$)	$I_{C(off)}$	—	2.0	100	—	2.0	100	μA
Emitter Off-State Current ($V_{CC} = 40\text{ V}$, $V_C = 40\text{ V}$, $V_E = 0\text{ V}$)	$I_{E(off)}$	—	—	-100	—	—	-150	μA
Collector-Emitter Saturation Voltage (2) Common-Emitter ($V_E = 0\text{ V}$, $I_C = 200\text{ mA}$) Emitter-Follower ($V_C = 15\text{ V}$, $I_E = -200\text{ mA}$)	$V_{SAT(C)}$	—	1.1	1.3	—	1.1	1.5	V
	$V_{SAT(E)}$	—	1.5	2.5	—	1.5	2.5	V
Output Control Pin Current Low State ($V_{OC} \leq 0.4\text{ V}$) High State ($V_{OC} = V_{ref}$)	I_{OCL}	—	10	—	—	10	—	μA
	I_{OCH}	—	0.2	3.5	—	0.2	3.5	mA
Output Voltage Rise Time Common-Emitter (See Figure 13) Emitter-Follower (See Figure 14)	t_r	—	100	200	—	100	200	ns
		—	100	200	—	100	200	ns
Output Voltage Fall Time Common-Emitter (See Figure 13) Emitter-Follower (See Figure 14)	t_f	—	25	100	—	25	100	ns
		—	40	100	—	40	100	ns

Characteristic	Symbol	TL494			Unit
		Min	Typ	Max	

ERROR AMPLIFIER SECTIONS

Input Offset Voltage (V_O (Pin 3) = 2.5 V)	V_{IO}	—	2.0	10	mV
Input Offset Current (V_O (Pin 3) = 2.5 V)	I_{IO}	—	5.0	250	nA
Input Bias Current (V_O (Pin 3) = 2.5 V)	I_{IB}	—	0.1	1.0	μA
Input Common-Mode Voltage Range ($V_{CC} = 40\text{ V}$, $T_A = 25^\circ\text{C}$)	V_{ICR}	-0.3 to $V_{CC} - 2.0$	—	—	V
Open-Loop Voltage Gain ($\Delta V_O = 3.0\text{ V}$, $V_O = 0.5\text{ to }3.5\text{ V}$, $R_L = 2.0\text{ k}\Omega$)	A_{VOL}	70	95	—	dB
Unity-Gain Crossover Frequency ($V_O = 0.5\text{ to }3.5\text{ V}$, $R_L = 2.0\text{ k}\Omega$)	f_C	—	350	—	kHz
Phase Margin at Unity-Gain ($V_O = 0.5\text{ to }3.5\text{ V}$, $R_L = 2.0\text{ k}\Omega$)	ϕ_m	—	65	—	deg
Common-Mode Rejection Ratio ($V_{CC} = 40\text{ V}$)	CMRR	65	90	—	dB
Power Supply Rejection Ratio ($\Delta V_{CC} = 33\text{ V}$, $V_O = 2.5\text{ V}$, $R_L = 2.0\text{ k}\Omega$)	PSRR	—	100	—	dB
Output Sink Current (V_O (Pin 3) = 0.7 V)	I_O	0.3	0.7	—	mA
Output Source Current (V_O (Pin 3) = 3.5 V)	I_O	2.0	4.0	—	mA

NOTE 2: Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperatures as possible.

TL494

ELECTRICAL CHARACTERISTICS ($V_{CC} = 15\text{ V}$, $C_T = 0.01\text{ }\mu\text{F}$, $R_T = 12\text{ k}\Omega$ unless otherwise noted.)

For typical values $T_A = 25^\circ\text{C}$, for min/max values T_A is the operating ambient temperature range that applies unless otherwise noted.

Characteristic	Symbol	TL494			Unit
		Min	Typ	Max	

PWM COMPARATOR SECTION (Test Circuit Figure 12)

Input Threshold Voltage (Zero duty cycle)	V_{TH}	—	3.5	4.5	V
Input Sink Current ($V_{Pin\ 3} = 0.7\text{ V}$)	I_{I-}	0.3	0.7	—	mA

DEAD-TIME CONTROL SECTION (Test Circuit Figure 12)

Input Bias Current (Pin 4) ($V_{Pin\ 4} = 0\text{ to }5.25\text{ V}$)	$I_{IB}\text{ (DT)}$	—	−2.0	−10	μA
Maximum Duty Cycle, Each Output, Push-Pull Mode ($V_{Pin\ 4} = 0\text{ V}$, $C_T = 0.01\text{ }\mu\text{F}$, $R_T = 12\text{ k}\Omega$) ($V_{Pin\ 4} = 0\text{ V}$, $C_T = 0.001\text{ }\mu\text{F}$, $R_T = 30\text{ k}\Omega$)	DC_{max}	45 —	48 45	50 50	%
Input Threshold Voltage (Pin 4) (Zero Duty Cycle) (Maximum Duty Cycle)	V_{TH}	— 0	2.8 —	3.3 —	V

OSCILLATOR SECTION

Frequency ($C_T = 0.001\text{ }\mu\text{F}$, $R_T = 30\text{ k}\Omega$)	f_{osc}	—	40	—	kHz
Standard Deviation of Frequency* ($C_T = 0.001\text{ }\mu\text{F}$, $R_T = 30\text{ k}\Omega$)	σf_{osc}	—	3.0	—	%
Frequency Change with Voltage ($V_{CC} = 7.0\text{ V to }40\text{ V}$, $T_A = 25^\circ\text{C}$)	$\Delta f_{osc}\text{ (}\Delta V\text{)}$	—	0.1	—	%
Frequency Change with Temperature ($\Delta T_A = T_{low}\text{ to }T_{high}$) ($C_T = 0.01\text{ }\mu\text{F}$, $R_T = 12\text{ k}\Omega$)	$\Delta f_{osc}\text{ (}\Delta T\text{)}$	—	—	12	%

UNDERVOLTAGE LOCKOUT SECTION

Turn-On Threshold (V_{CC} Increasing, $I_{ref} = 1.0\text{ mA}$)	V_{th}	5.5	6.43	7.0	V
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TOTAL DEVICE

Standby Supply Current (Pin 6 at V_{ref} , All Other Inputs and Outputs Open) ($V_{CC} = 15\text{ V}$) ($V_{CC} = 40\text{ V}$)	I_{CC}	— —	5.5 7.0	10 15	mA
Average Supply Current ($V_{Pin\ 4} = 2.0\text{ V}$) (See Figure 12) ($C_T = 0.01\text{ }\mu\text{F}$, $R_T = 12\text{ k}\Omega$, $V_{CC} = 15\text{ V}$)	—	—	7.0	—	mA

* Standard deviation is a measure of the statistical distribution about the mean as derived from the formula.

$$\sqrt{\frac{\sum_{n=1}^N (X_n - \bar{X})^2}{N - 1}}$$

FIGURE 4 — OSCILLATOR FREQUENCY
versus TIMING RESISTANCE

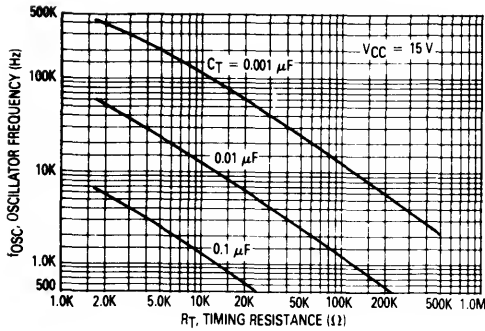


FIGURE 5 — OPEN-LOOP VOLTAGE GAIN AND PHASE
versus FREQUENCY

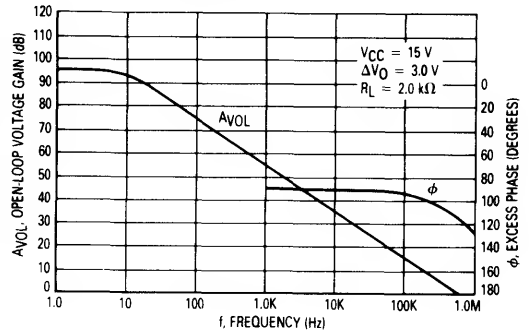


FIGURE 6 — PERCENT DEAD-TIME versus
OSCILLATOR FREQUENCY

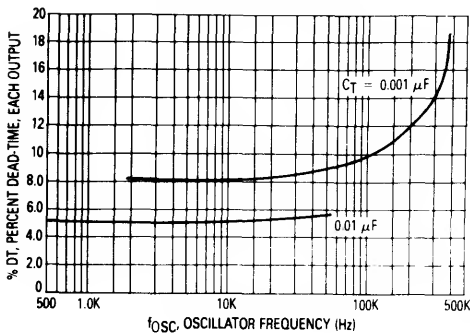


FIGURE 7 — PERCENT DUTY CYCLE versus
DEAD-TIME CONTROL VOLTAGE

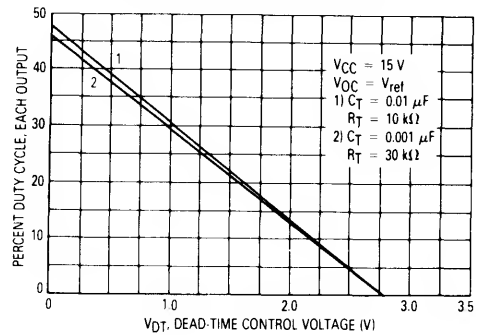


FIGURE 8 — EMITTER FOLLOWER CONFIGURATION
OUTPUT SATURATION VOLTAGE versus
EMITTER CURRENT

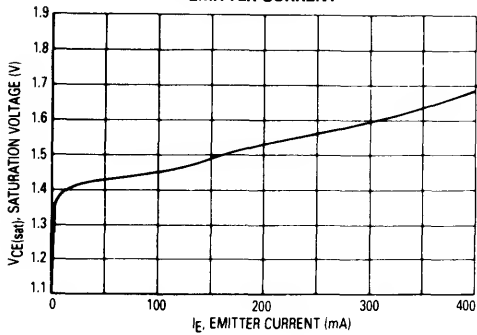


FIGURE 9 — COMMON EMITTER CONFIGURATION
OUTPUT SATURATION VOLTAGE versus
COLLECTOR CURRENT

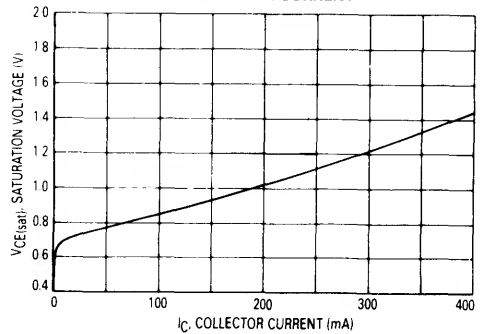


FIGURE 10 — STANDBY SUPPLY CURRENT
versus SUPPLY VOLTAGE

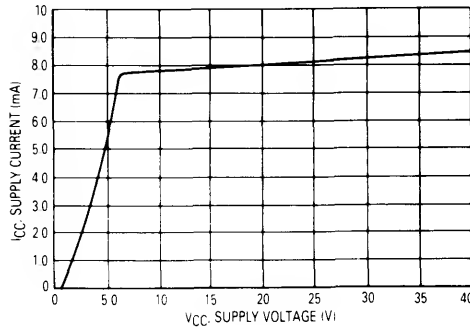


FIGURE 11 — ERROR AMPLIFIER CHARACTERISTICS

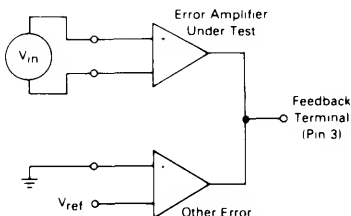


FIGURE 12 — DEAD-TIME AND FEEDBACK CONTROL
TEST CIRCUIT

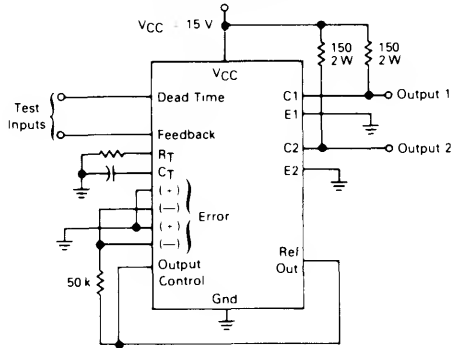


FIGURE 13 — COMMON-EMITTER CONFIGURATION
TEST CIRCUIT AND WAVEFORM

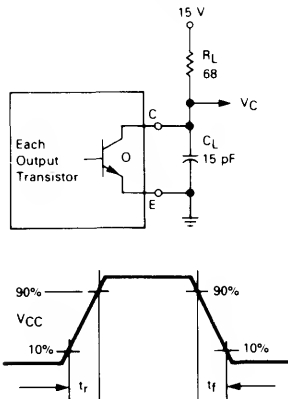


FIGURE 14 — EMITTER-FOLLOWER CONFIGURATION
TEST CIRCUIT AND WAVEFORM

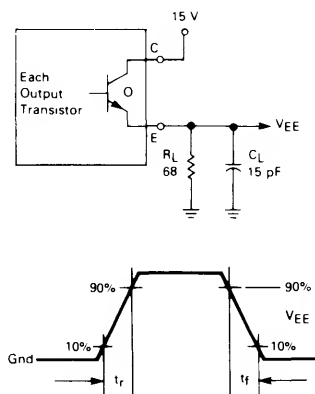


FIGURE 15 — ERROR-AMPLIFIER SENSING TECHNIQUES

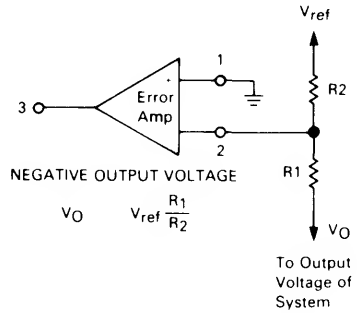
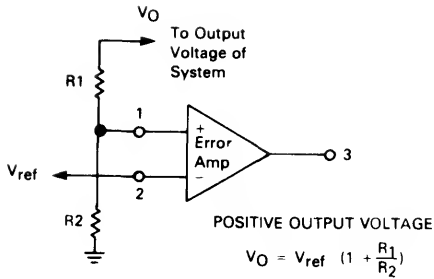
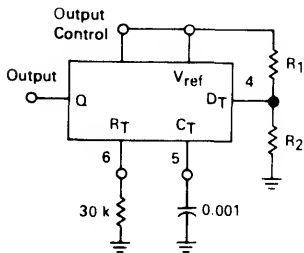


FIGURE 16 — DEAD-TIME CONTROL CIRCUIT



$$\text{Max \% on Time, Each Output} = 45 - \left(\frac{80}{1 + \frac{R_1}{R_2}} \right)$$

FIGURE 17 — SOFT-START CIRCUIT

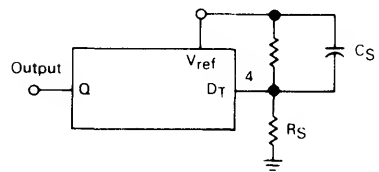
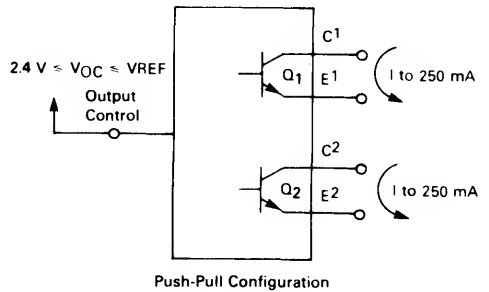
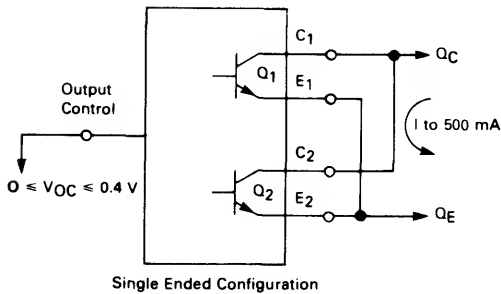


FIGURE 18 — OUTPUT CONNECTIONS FOR SINGLE-ENDED AND PUSH-PULL CONFIGURATIONS



TL494

FIGURE 19 — SLAVING TWO OR MORE CONTROL CIRCUITS

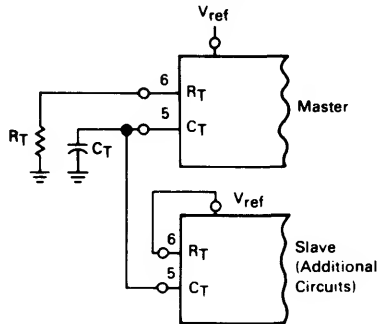


FIGURE 20 — OPERATION WITH $V_{IN} > 40$ V USING EXTERNAL ZENER

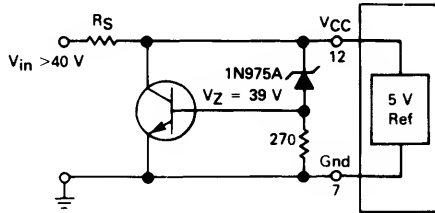
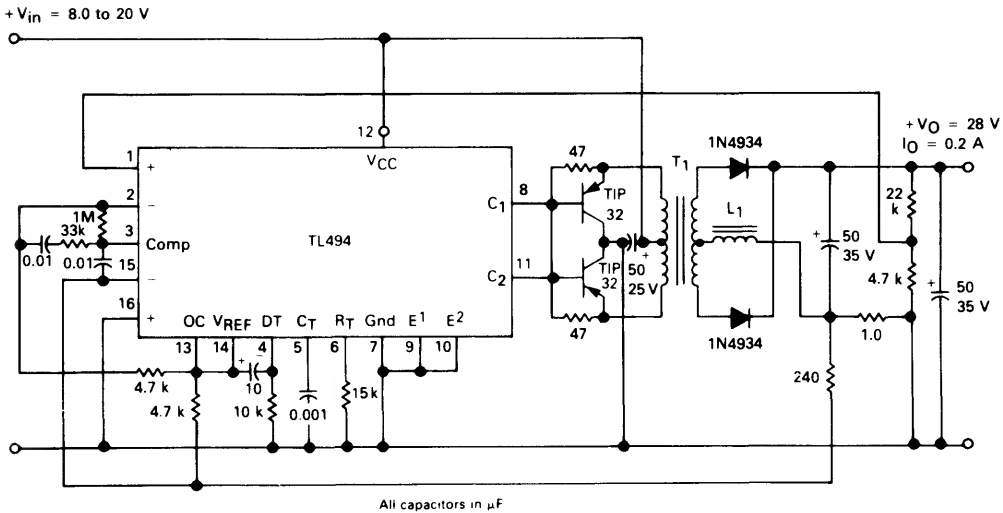


FIGURE 21 — PULSE-WIDTH MODULATED PUSH-PULL CONVERTER



All capacitors in μ F

L1 — 3.5 mH @ 0.3 A

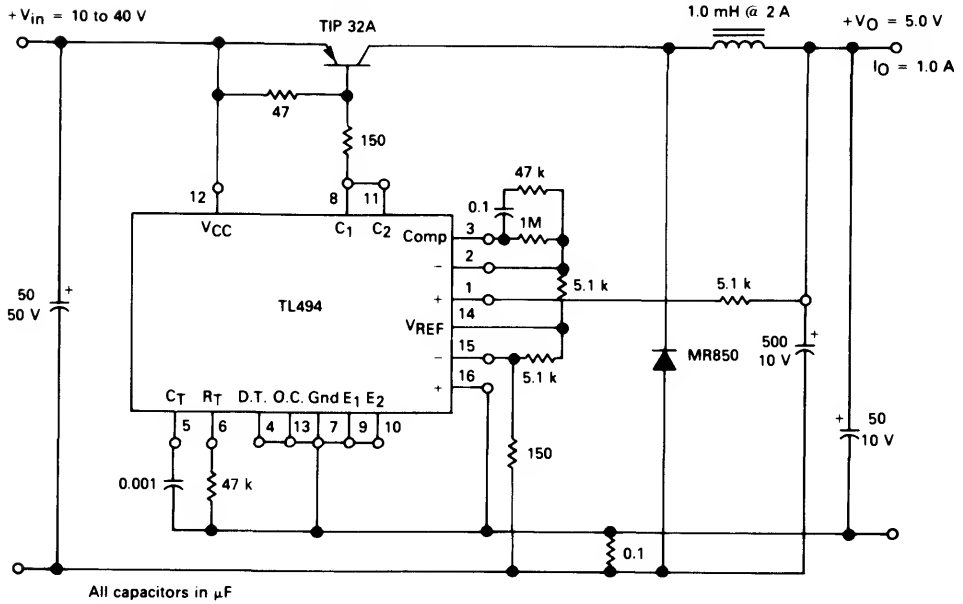
T1 — Primary: 20T C.T. #28 AWG

Secondary: 120T C.T. #36 AWG

Core: Ferroxcube 1408P-L00-3C8

TEST	CONDITIONS	RESULTS
Line Regulation	$V_{in} = 10$ V to 40 V	14 mV 0.28%
Load Regulation	$V_{in} = 28$ V, $I_O = 1$ mA to 1 A	3.0 mV 0.06%
Output Ripple	$V_{in} = 28$ V, $I_O = 1.0$ A	65 mV P-P P.A.R.D.
Short Circuit Current	$V_{in} = 28$ V, $R_L = 0.1 \Omega$	1.6 amps
Efficiency	$V_{in} = 28$ V, $I_O = 1$ A	71%

FIGURE 22 — PULSE-WIDTH MODULATED STEP-DOWN CONVERTER

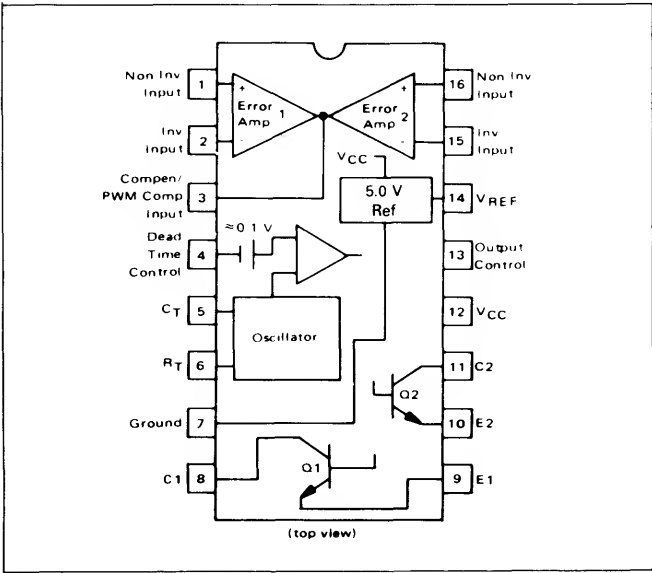


TEST	CONDITIONS	RESULTS
Line Regulation	$V_{in} = 8.0 \text{ to } 40 \text{ V}$	3.0 mV 0.01%
Load Regulation	$V_{in} = 12.6 \text{ V}, I_O = 0.2 \text{ to } 200 \text{ mA}$	5.0 mV 0.02%
Output Ripple	$V_{in} = 12.6 \text{ V}, I_O = 200 \text{ mA}$	40 mV p-P P.A.R.D.
Short Circuit Current	$V_{in} = 12.6 \text{ V}, R_L = 0.1 \Omega$	250 mA
Efficiency	$V_{in} = 12.6 \text{ V}, I_O = 200 \text{ mA}$	72%

PRECISION SWITCHMODE
PULSE WIDTH MODULATION
CONTROL CIRCUIT

The TL594 is a fixed frequency, pulse width modulation control circuit designed primarily for Switchmode power supply control. This device features:

- Complete Pulse Width Modulation Control Circuitry
- On-Chip Oscillator With Master Or Slave Operation
- On-Chip Error Amplifiers
- On-Chip 5 Volt Reference, 1.5% Accuracy
- Adjustable Dead-Time Control
- Uncommitted Output Transistors Rated to 500 mA Source Or Sink
- Output Control For Push-Pull Or Single-Ended Operation
- Undervoltage Lockout

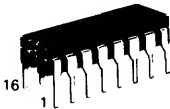


The TL594C is specified over the commercial operating range of 0°C to 70°C. The TL594I is specified over the industrial range of -25°C to 85°C. The TL594M is specified over the full military range of -55°C to 125°C.

TL594

PRECISION SWITCHMODE
PULSE WIDTH MODULATION
CONTROL CIRCUIT

SILICON MONOLITHIC
INTEGRATED CIRCUITS



J SUFFIX
CERAMIC PACKAGE
CASE 620



N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

Device	Temperature Range	Package
TL594CN	0° to +70°C	Plastic DIP
TL594IN	-25° to +85°C	Plastic DIP
TL594MJ	-55° to +125°C	Ceramic DIP

FIGURE 1 — BLOCK DIAGRAM

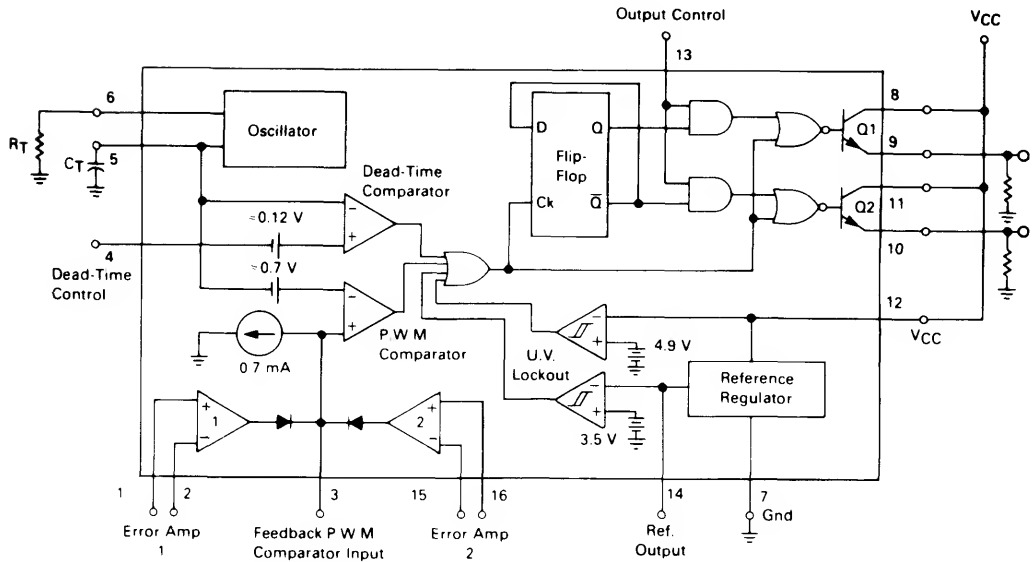
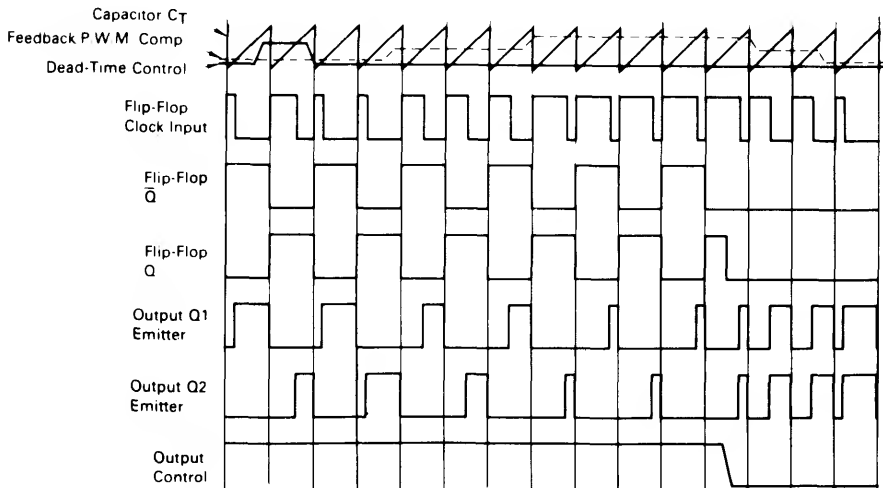


FIGURE 2 — TIMING DIAGRAM



Description

The TL594 is a fixed-frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply. (See Figure 1.) An internal-linear sawtooth oscillator is frequency-programmable by two external components, R_T and C_T . The approximate oscillator frequency is determined by:

$$f_{osc} \approx \frac{1.2}{R_T \bullet C_T}$$

For more information refer to Figure 4.

Output pulse width modulation is accomplished by comparison of the positive sawtooth waveform across capacitor C_T to either of two control signals. The NOR gates, which drive output transistors Q1 and Q2, are enabled only when the flip-flop clock-input line is in its low state. This happens only during that portion of time when the sawtooth voltage is greater than the control signals. Therefore, an increase in control-signal amplitude causes a corresponding linear decrease of output pulse width. (Refer to the timing diagram shown in Figure 2.)

The control signals are external inputs that can be fed into the dead-time control, the error amplifier inputs, or the feedback input. The dead-time control comparator has an effective 120 mV input offset which limits the minimum output dead time to approximately the first 4% of the sawtooth-cycle time. This would result in a maximum duty cycle on a given output of 96% with the output control grounded, and 48% with it connected to the reference line. Additional dead time may be imposed on the output by setting the dead time-control input to a fixed voltage, ranging between 0 to 3.3 V.

The pulse width modulator comparator provides a means for the error amplifiers to adjust the output pulse width from the maximum percent on-time, established by the dead time control input, down to zero, as the voltage at the feedback pin varies from 0.5 to 3.5 V. Both error amplifiers have a common-mode input range from -0.3 V to $(V_{CC} - 2$ V), and may be used to sense power-supply output voltage and current. The error-amplifier outputs are active high and are ORed together at the non-inverting input of the pulse-width modulator comparator. With this configuration, the amplifier that demands minimum output on time, dominates control of the loop.

When capacitor C_T is discharged, a positive pulse is generated on the output of the dead-time comparator, which clocks the pulse-steering flip-flop and inhibits the output transistors, Q1 and Q2. With the output-control connected to the reference line, the pulse-steering flip-flop directs the modulated pulses to each of the two output transistors alternately for push-pull operation. The output frequency is equal to half that of the oscillator. Output drive can also be taken from Q1 or Q2, when single-ended operation with a maximum on-time of less than 50% is required. This is desirable when the output transformer has a ringback winding with a catch diode used for snubbing. When higher output-drive currents are required for single-ended operation, Q1 and Q2 may be connected in parallel, and the output-mode pin must be tied to ground to disable the flip-flop. The output frequency will now be equal to that of the oscillator.

The TL594 has an internal 5.0 V reference capable of sourcing up to 10 mA of load current for external bias circuits. The reference has an internal accuracy of $\pm 1.5\%$ with a typical thermal drift of less than 50 mV over an operating temperature range of 0 to 70°C.

FIGURE 3 — FUNCTIONAL TABLE

Input	Output Function	$\frac{f_{out}}{f_{osc}} =$
Output Control		
Grounded	Single-ended P.W.M. at Q1 and Q2	1
At V_{ref}	Push-pull operation	0.5

TL594

MAXIMUM RATINGS (Full operating ambient temperature range applies unless otherwise noted)

Rating	Symbol	TL594C	TL594I	TL594M	Unit
Power Supply Voltage	V_{CC}	42	42	42	V
Collector Output Voltage	V_{C1}, V_{C2}	42	42	42	V
Collector Output Current (each transistor) (Note 1)	I_{C1}, I_{C2}	500	500	500	mA
Amplifier Input Voltage Range	V_{IR}	-0.3 to 42	-0.3 to 42	-0.3 to 42	V
Power Dissipation (a $T_A \leq 45^\circ\text{C}$)	P_D	1000	1000	1000	mW
Operating Junction Temperature Plastic Package Ceramic Package	T_J	125 —	125 —	— 150	$^\circ\text{C}$
Operating Ambient Temperature Range	T_A	0 to 70	-25 to 85	-55 to 125	$^\circ\text{C}$
Storage Temperature Range Plastic Package Ceramic Package	T_{stg}	-55 to 125 —	-55 to 125 —	— -65 to 150	$^\circ\text{C}$

NOTE 1: Maximum thermal limits must be observed

THERMAL CHARACTERISTICS

Characteristics	Symbol	N Suffix Plastic Package	J Suffix Ceramic Package	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	80	100	$^\circ\text{C/W}$
Derating Ambient Temperature	T_A	45	50	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS

Condition/Value	Symbol	TL594			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	7.0	15	40	V
Collector Output Voltage	V_{C1}, V_{C2}	—	30	40	V
Collector Output Current (each transistor)	I_{C1}, I_{C2}	—	—	200	mA
Amplifier Input Voltage	V_{in}	0.3	—	$V_{CC} - 2.0$	V
Current Into Feedback Terminal	I_{fb}	—	—	0.3	mA
Reference Output Current	I_{ref}	—	—	10	mA
Timing Resistor	R_T	1.8	30	500	k Ω
Timing Capacitor	C_T	0.0047	0.001	10	μF
Oscillator Frequency	f_{osc}	1.0	40	200	kHz
PWM Input Voltage (Pins 3, 4 & 13)	—	0.3	—	5.3	V

ELECTRICAL CHARACTERISTICS ($V_{CC} = 15\text{ V}$, $C_T = 0.01\text{ }\mu\text{F}$, $R_T = 12\text{ k}\Omega$ unless otherwise noted.)

For typical values $T_A = 25^\circ\text{C}$, for min max values T_A is the operating ambient temperature range that applies unless otherwise noted.

Characteristic	Symbol	TL594C,I			TL594M			Unit
		Min	Typ	Max	Min	Typ	Max	

REFERENCE SECTION

Reference Voltage ($I_O = 1.0\text{ mA}$, $T_A = 25^\circ\text{C}$) ($I_O = 1.0\text{ mA}$)	V_{ref}	4.925 4.9	5.0 —	5.075 5.1	4.925 4.9	5.0 —	5.075 5.1	V
Line Regulation ($V_{CC} = 7.0\text{ V}$ to 40 V)	Reg_{line}	—	2.0	25	—	2.0	25	mV
Load Regulation ($I_O = 1.0\text{ mA}$ to 10 mA)	Reg_{load}	—	2.0	15	—	2.0	15	mV
Short-Circuit Output Current ($V_{ref} = 0\text{ V}$)	I_{SC}	15	40	75	15	40	75	mA

TL594

ELECTRICAL CHARACTERISTICS ($V_{CC} = 15\text{ V}$, $C_T = 0.01\text{ }\mu\text{F}$, $R_T = 12\text{ k}\Omega$) unless otherwise noted.)

For typical values $T_A = 25^\circ\text{C}$, for min/max values T_A is the operating ambient temperature range that applies unless otherwise noted.

Characteristic	Symbol	TL594C,I			TL594M			Unit
		Min	Typ	Max	Min	Typ	Max	

OUTPUT SECTION

Collector Off-State Current ($V_{CC} = 40\text{ V}$, $V_{CE} = 40\text{ V}$)	$I_{C(off)}$	—	2.0	100	—	2.0	100	μA
Emitter Off-State Current ($V_{CC} = 40\text{ V}$, $V_C = 40\text{ V}$, $V_E = 0\text{ V}$)	$I_{E(off)}$	—	—	—100	—	—	—100	μA
Collector-Emitter Saturation Voltage (Note 2) Common-Emitter ($V_E = 0\text{ V}$, $I_C = 200\text{ mA}$) Emitter-Follower ($V_C = 15\text{ V}$, $I_E = -200\text{ mA}$)	$V_{SAT(C)}$	—	1.1	1.3	—	1.1	1.5	V
	$V_{SAT(E)}$	—	1.5	2.5	—	1.5	2.5	V
Output Control Pin Current Low State ($V_{OC} \approx 0.4\text{ V}$) High State ($V_{OC} = V_{ref}$)	I_{OCL}	—	0.1	—	—	0.1	—	μA
	I_{OCH}	—	2.0	20	—	2.0	20	μA
Output Voltage Rise Time Common-Emitter (See Figure 14) Emitter-Follower (See Figure 15)	t_r	—	100	200	—	100	200	ns
		—	100	200	—	100	200	ns
Output Voltage Fall Time Common-Emitter (See Figure 14) Emitter-Follower (See Figure 15)	t_f	—	40	100	—	40	100	ns
		—	40	100	—	40	100	ns

Characteristic	Symbol	TL594			Unit
		Min	Typ	Max	

ERROR AMPLIFIER SECTIONS

Input Offset Voltage (V_O (Pin 3) = 2.5 V)	V_{IO}	—	2.0	10	mV
Input Offset Current (V_O (Pin 3) = 2.5 V)	I_{IO}	—	5.0	250	nA
Input Bias Current (V_O (Pin 3) = 2.5 V)	I_{IB}	—	—0.1	—1.0	μA
Input Common-Mode Voltage Range ($V_{CC} = 40\text{ V}$, $T_A = 25^\circ\text{C}$)	V_{ICR}	0 to $V_{CC} - 2.0$	—	—	V
Inverting Input Voltage Range	$V_{IR(INV)}$	—0.3 to $V_{CC} - 2.0$	—	—	V
Open-Loop Voltage Gain ($\Delta V_O = 6.0\text{ V}$, $V_O = 0.5$ to 3.5 V , $R_L = 2.0\text{ k}\Omega$)	A_{VOL}	70	95	—	dB
Unity-Gain Crossover Frequency ($V_O = 0.5$ to 3.5 V , $R_L = 2.0\text{ k}\Omega$)	f_C	—	700	—	kHz
Phase Margin at Unity-Gain ($V_O = 0.5$ to 3.5 V , $R_L = 2.0\text{ k}\Omega$)	θ_m	—	65	—	deg.
Common-Mode Rejection Ratio ($V_{CC} = 40\text{ V}$)	CMRR	65	90	—	dB
Power Supply Rejection Ratio ($\Delta V_{CC} = 33\text{ V}$, $V_O = 2.5\text{ V}$, $R_L = 2.0\text{ k}\Omega$)	PSRR	—	100	—	dB
Output Sink Current (V_O (Pin 3) = 0.7 V)	I_{O-}	0.3	0.7	—	mA
Output Source Current (V_O (Pin 3) = 3.5 V)	I_{O+}	—2.0	—4.0	—	mA

NOTE 2: Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

ELECTRICAL CHARACTERISTICS ($V_{CC} = 15\text{ V}$, $C_T = 0.01\text{ }\mu\text{F}$, $R_T = 12\text{ k}\Omega$ unless otherwise noted.)

For typical values $T_A = 25^\circ\text{C}$, for min/max values T_A is the operating ambient temperature range that applies unless otherwise noted.

Characteristic	Symbol	TL594			Unit
		Min	Typ	Max	

PWM COMPARATOR SECTION (Test Circuit Figure 12)

Input Threshold Voltage (Zero Duty Cycle)	V_{TH}	—	3.6	4.5	V
Input Sink Current ($V_{Pin\ 3} = 0.7\text{ V}$)	I_{I-}	0.3	0.7	—	mA

DEAD-TIME CONTROL SECTION (Test Circuit Figure 12)

Input Bias Current (Pin 4) ($V_{Pin\ 4} = 0\text{ to }5.25\text{ V}$)	$I_{IB}\text{ (DT)}$	—	2.0	— 10	μA
Maximum Duty Cycle, Each Output, Push-Pull Mode ($V_{Pin\ 4} = 0\text{ V}$, $C_T = 0.01\text{ }\mu\text{F}$, $R_T = 12\text{ k}\Omega$) ($V_{Pin\ 4} = 0\text{ V}$, $C_T = 0.001\text{ }\mu\text{F}$, $R_T = 30\text{ k}\Omega$)	DC_{max}	45 —	48 45	50 —	%
Input Threshold Voltage (Pin 4) (Zero Duty Cycle) (Maximum Duty Cycle)	V_{TH}	— 0	2.8 —	3.3 —	V

OSCILLATOR SECTION

Frequency ($C_T = 0.001\text{ }\mu\text{F}$, $R_T = 30\text{ k}\Omega$) ($C_T = 0.01\text{ }\mu\text{F}$, $R_T = 12\text{ k}\Omega$, $T_A = 25^\circ\text{C}$) ($C_T = 0.01\text{ }\mu\text{F}$, $R_T = 12\text{ k}\Omega$, $T_A = T_{low}\text{ to }T_{high}$)	f_{osc}	— 9.2 9.0	40 10 —	— 10.8 12	kHz
Standard Deviation of Frequency* ($C_T = 0.001\text{ }\mu\text{F}$, $R_T = 30\text{ k}\Omega$)	σf_{osc}	—	1.5	—	%
Frequency Change with Voltage ($V_{CC} = 7.0\text{ V to }40\text{ V}$, $T_A = 25^\circ\text{C}$)	$\Delta f_{osc}\text{ }(\Delta V)$	—	0.2	1.0	%
Frequency Change with Temperature ($\Delta T_A = T_{low}\text{ to }T_{high}$, $C_T = 0.01\text{ }\mu\text{F}$, $R_T = 12\text{ k}\Omega$)	$\Delta f_{osc}\text{ }(\Delta T)$	—	4.0	—	%

UNDERVOLTAGE LOCKOUT SECTION

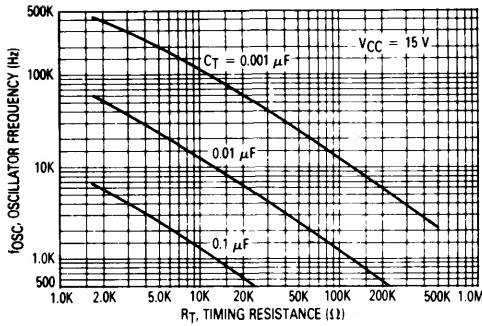
Turn-On Threshold (V_{CC} Increasing, $I_{ref} = 1.0\text{ mA}$) $T_A = 25^\circ\text{C}$ $T_A = T_{low}\text{ to }T_{high}$	V_{th}	4.0 3.5	5.2 —	6.0 6.5	V
Hysteresis TL594C,I TL594M	V_H	100 50	150 150	300 300	mV

TOTAL DEVICE

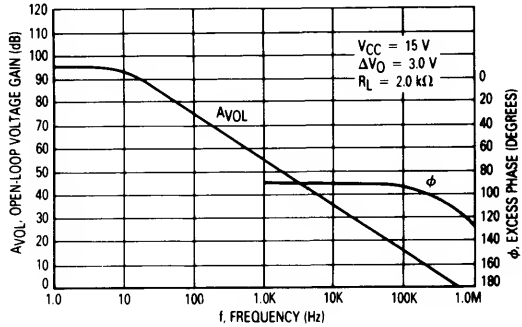
Standby Supply Current (Pin 6 at V_{ref} , All Other Inputs and Outputs Open) ($V_{CC} = 15\text{ V}$) ($V_{CC} = 40\text{ V}$)	I_{CC}	— —	8.0 8.5	15 18	mA
Average Supply Current ($V_{Pin\ 4} = 2.0\text{ V}$, $C_T = 0.01\text{ }\mu\text{F}$, $R_T = 12\text{ k}\Omega$, $V_{CC} = 15\text{ V}$, See Figure 12)	—	—	11	—	mA

*Standard deviation is a measure of the statistical distribution about the mean as derived from the formula, $\sigma = \sqrt{\frac{\sum_{n=1}^N (x_n - \bar{x})^2}{N - 1}}$

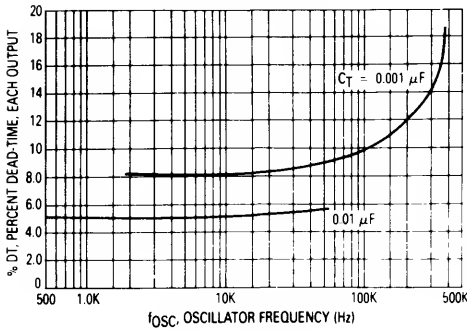
**FIGURE 4 — OSCILLATOR FREQUENCY
versus TIMING RESISTANCE**



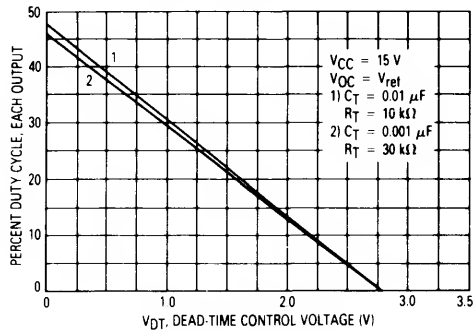
**FIGURE 5 — OPEN-LOOP VOLTAGE GAIN AND PHASE
versus FREQUENCY**



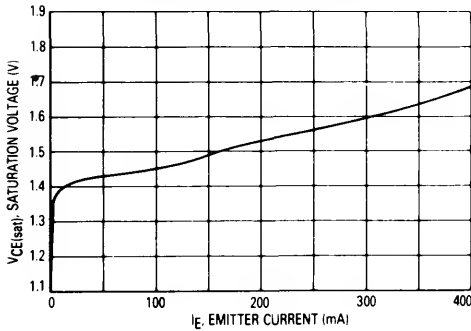
**FIGURE 6 — PERCENT DEAD-TIME versus
OSCILLATOR FREQUENCY**



**FIGURE 7 — PERCENT DUTY CYCLE versus
DEAD-TIME CONTROL VOLTAGE**



**FIGURE 8 — EMITTER FOLLOWER CONFIGURATION
OUTPUT SATURATION VOLTAGE versus
EMITTER CURRENT**



**FIGURE 9 — COMMON EMITTER CONFIGURATION
OUTPUT SATURATION VOLTAGE versus
COLLECTOR CURRENT**

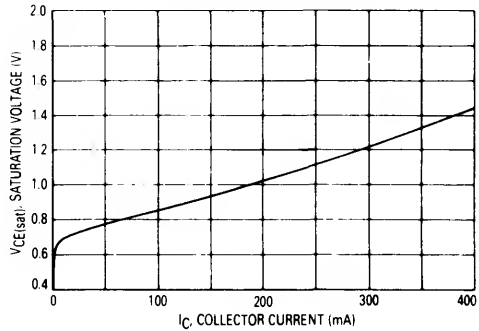


FIGURE 10 — STANDBY SUPPLY CURRENT
versus SUPPLY VOLTAGE

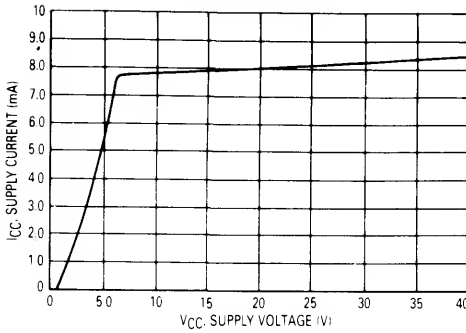


FIGURE 11 — UNDERVOLTAGE LOCKOUT THRESHOLDS
versus REFERENCE LOAD CURRENT

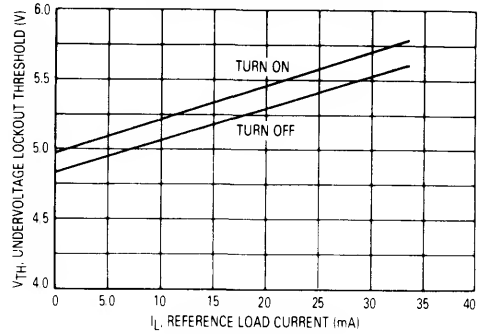


FIGURE 12 — ERROR AMPLIFIER CHARACTERISTICS

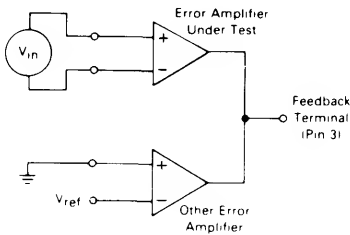


FIGURE 13 — DEAD-TIME AND FEEDBACK CONTROL
TEST CIRCUIT

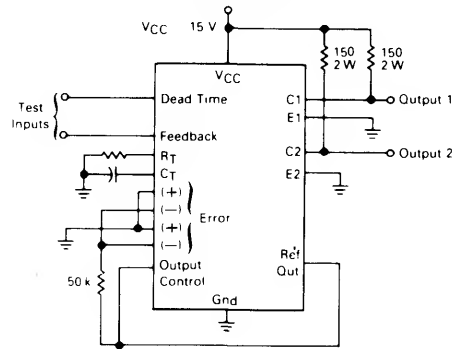


FIGURE 14 — COMMON-EMITTER CONFIGURATION
TEST CIRCUIT AND WAVEFORM

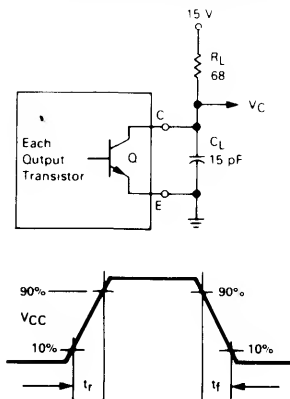


FIGURE 15 — EMITTER-FOLLOWER CONFIGURATION
TEST CIRCUIT AND WAVEFORM

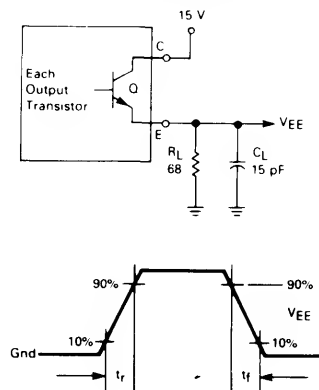


FIGURE 16 — ERROR-AMPLIFIER SENSING TECHNIQUES

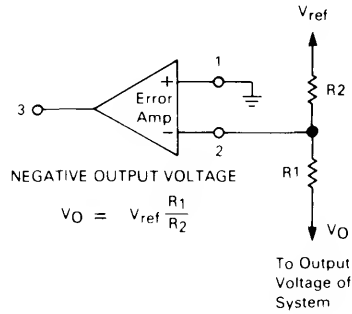
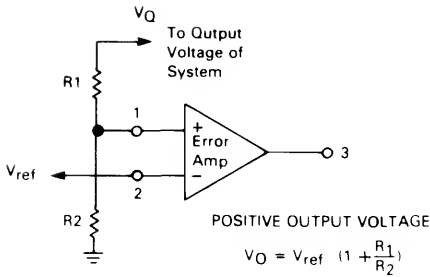


FIGURE 17 — DEAD-TIME CONTROL CIRCUIT

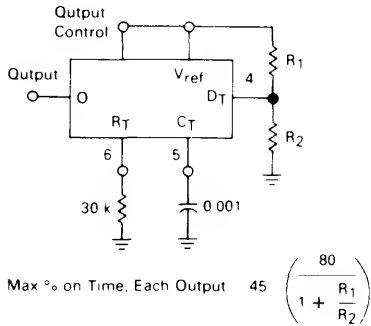


FIGURE 18 — SOFT-START CIRCUIT

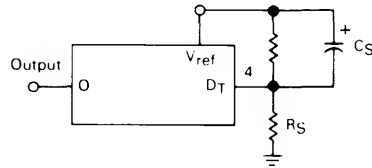
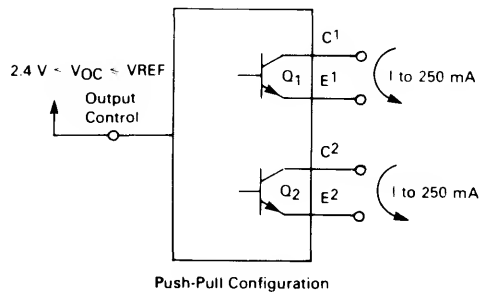
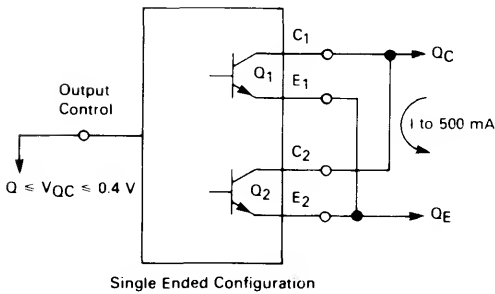


FIGURE 19 — OUTPUT CONNECTIONS FOR SINGLE-ENDED AND PUSH-PULL CONFIGURATIONS



3

The circuit diagram shows a precision current source using a TL594 IC. The input is $-V_{in}$ (8.0 to 20 V) and the output is V_O (28 V, 0.2 A). The TL594 IC is configured with a feedback loop containing a transformer T_1 and two TIP transistors. The output is regulated by two 1N4934 diodes and a 240 Ω resistor. The circuit includes various passive components such as resistors (1M, 33k, 4.7k, 10k, 15k, 22k, 4.7k, 1k) and capacitors (0.01, 0.001, 50 μ F, 35 μ F). The output is V_O (28 V, 0.2 A).

All capacitors in μ F

T1 — Primary: 20T C.T. #28 AWG
Secondary: 120T C.T. #36 AWG
Core: Ferroxcube 1408P-L00-3C8

MOTOROLA LINEAR/INTERFACE DEVICES

3

3

3

THREE-TERMINAL POSITIVE VOLTAGE REGULATORS

This family of precision fixed voltage regulators are monolithic integrated circuits capable of driving loads in excess of 1.5 amperes. Innovative design concepts, coupled with advanced thermal layout techniques has resulted in improved accuracy and excellent load, line and thermal regulation characteristics. Internal current limiting, thermal shutdown and safe-area compensation are employed, making these devices extremely rugged and virtually immune to overload.

- $\pm 1\%$ Output Voltage Tolerance ($\alpha 25^\circ\text{C}$)
- $\pm 2\%$ Output Voltage Tolerance Over Full Operating Temperature Range
- Internal Short-Circuit Current Limiting
- Internal Thermal Overload Protection
- Output Transistor Safe-Area Compensation
- No External Components Required
- Pinout Compatible with MC7800 Series

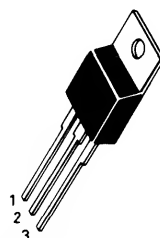
TL780 Series

THREE-TERMINAL POSITIVE FIXED VOLTAGE REGULATORS

SILICON MONOLITHIC INTEGRATED CIRCUITS

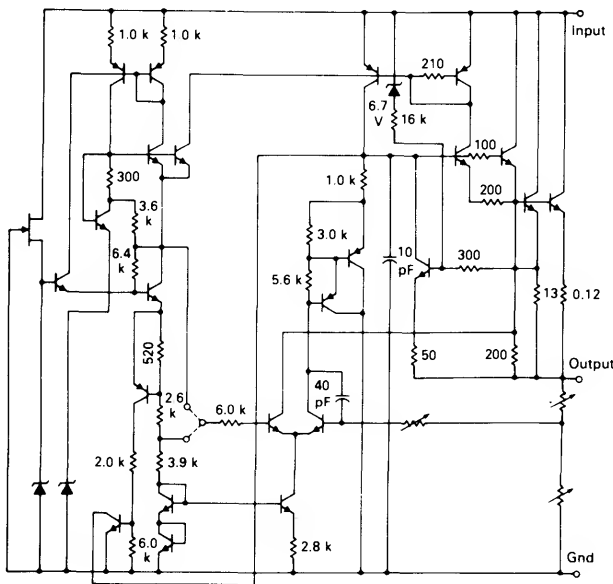
KC SUFFIX
 PLASTIC PACKAGE
 CASE 221A

Pin 1. Input
 2. Ground
 3. Output

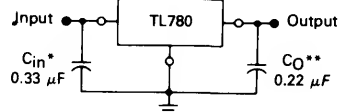


(Heatsink surface connected to Pin 2.)

EQUIVALENT SCHEMATIC DIAGRAM



STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O is not needed for stability; however, it does improve transient response.

ORDERING INFORMATION

Nominal Output Voltage	Device
5.0 V	TL780-05CKC
12 V	TL780-12CKC
15 V	TL780-15CKC

TL780 Series

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	V_{in}	35	Vdc
Power Dissipation and Thermal Characteristics			
$T_A = +25^\circ\text{C}$	P_D	2.0	Watts
Derate above $T_A = +25^\circ\text{C}$	$1 \theta_{JA}$	16	mW $^\circ\text{C}$
Thermal Resistance, Junction to Air	θ_{JA}	62.5	$^\circ\text{C/W}$
$T_C = +25^\circ\text{C}$	P_D	15	Watts
Derate above $T_C = +75^\circ\text{C}$ (See Figure 1)	$1 \theta_{JC}$	200	mW $^\circ\text{C}$
Thermal Resistance, Junction to Case	θ_{JC}	5.0	$^\circ\text{C/W}$
Operating Junction Temperature Range	T_J	0 to +150	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to -150	$^\circ\text{C}$

TL780-05C

ELECTRICAL CHARACTERISTICS ($V_{in} = 10\text{ V}$, $I_O = 500\text{ mA}$, $0^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$ unless otherwise noted [Note 1])

Characteristic	Symbol	TL780-05C			Unit
		Min	Typ	Max	
Output Voltage $5.0\text{ mA} \leq I_O \leq 1.0\text{ A}$, $P \leq 15\text{ W}$ $7.0\text{ V} \leq V_{in} \leq 20\text{ V}$ $T_J = +25^\circ\text{C}$ $0^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$	V_O	4.95 4.90	5.0 —	5.05 5.10	V
Line Regulation ($T_J = -25^\circ\text{C}$) $7.0\text{ V} \leq V_{in} \leq 25\text{ V}$ $8.0\text{ V} \leq V_{in} \leq 12\text{ V}$	Regline	— —	0.5 0.5	5.0 5.0	mV
Load Regulation ($T_J = -25^\circ\text{C}$) $5.0\text{ mA} \leq I_O \leq 1.5\text{ A}$ $250\text{ mA} \leq I_O \leq 750\text{ mA}$	Regload	— —	4.0 1.5	25 15	mV
Ripple Rejection $8.0\text{ V} \leq V_{in} \leq 18\text{ V}$, $f = 120\text{ Hz}$	RR	70	80	—	dB
Output Resistance ($f = 1.0\text{ kHz}$)	r_O	—	0.0035	—	Ω
Average Temperature Coefficient of Output Voltage $I_O = 5.0\text{ mA}$	TCV_O	—	0.06	—	mV $^\circ\text{C}$
Output Noise Voltage ($T_J = +25^\circ\text{C}$) $10\text{ Hz} \leq f \leq 100\text{ kHz}$	V_n	—	75	—	μV
Dropout Voltage ($T_J = -25^\circ\text{C}$) $I_O = 1.0\text{ A}$	V_{in-V_O}	—	2.0	—	V
Bias Current ($T_J = +25^\circ\text{C}$)	I_B	—	3.5	8.0	mA
Bias Current Change $7.0\text{ V} \leq V_{in} \leq 25\text{ V}$, $I_O = 500\text{ mA}$ $5.0\text{ mA} \leq I_O \leq 1.0\text{ A}$, $V_{in} = 10\text{ V}$	ΔI_B	— —	0.7 0.03	1.3 0.5	mA
Short-Circuit Output Current ($T_J = -25^\circ\text{C}$) $V_{in} = 35\text{ V}$	I_{sc}	—	200	—	mA
Peak Output Current ($T_J = +25^\circ\text{C}$)	I_P	—	2.2	—	A

Note 1: Line and load regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

TL780-12C

ELECTRICAL CHARACTERISTICS ($V_{in} = 19\text{ V}$, $I_O = 500\text{ mA}$, $0^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$ unless otherwise noted [Note 1])

Characteristic	Symbol	TL780-12C			Unit
		Min	Typ	Max	
Output Voltage $5.0\text{ mA} \leq I_O \leq 1.0\text{ A}$, $P \leq 15\text{ W}$ $14.5\text{ V} \leq V_{in} \leq 27\text{ V}$ $T_J = +25^\circ\text{C}$ $0^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$	V_O	11.88 11.76	12 —	12.12 12.24	V
Line Regulation ($T_J = +25^\circ\text{C}$) $14.5\text{ V} \leq V_{in} \leq 30$ $16\text{ V} \leq V_{in} \leq 22$	Regline	— —	1.2 1.2	12 12	mV

TL780 Series

TL780-12C (continued)

ELECTRICAL CHARACTERISTICS ($V_{in} = 19\text{ V}$, $I_O = 500\text{ mA}$, $0^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$ unless otherwise noted [Note 1])

Characteristic	Symbol	TL780-12C			Unit
		Min	Typ	Max	
Load Regulation ($T_J = +25^\circ\text{C}$) $5.0\text{ mA} \leq I_O \leq 1.5\text{ A}$ $250\text{ mA} \leq I_O \leq 750\text{ mA}$	Reg_{load}	— —	6.5 2.5	60 36	mV
Ripple Rejection $15\text{ V} \leq V_{in} \leq 25\text{ V}$, $f = 120\text{ Hz}$	RR	65	77	—	dB
Output Resistance ($f = 1.0\text{ kHz}$)	r_O	—	0.0035	—	Ω
Average Temperature Coefficient of Output Voltage $I_O = 5.0\text{ mA}$	TCV_O	—	0.15	—	$\text{mV}/^\circ\text{C}$
Output Noise Voltage ($T_J = +25^\circ\text{C}$) $10\text{ Hz} \leq f \leq 100\text{ kHz}$	V_n	—	180	—	μV
Dropout Voltage ($T_J = +25^\circ\text{C}$) $I_O = 1.0\text{ A}$	$V_{in}-V_O$	—	2.0	—	V
Bias Current ($T_J = +25^\circ\text{C}$)	I_B	—	3.5	8.0	mA
Bias Current Change $14.5\text{ V} \leq V_{in} \leq 30\text{ V}$, $I_O = 500\text{ mA}$ $5.0\text{ mA} \leq I_O \leq 1.0\text{ A}$, $V_{in} = 19\text{ V}$	ΔI_B	— —	0.4 0.03	1.3 0.5	mA
Short-Circuit Output Current ($T_J = +25^\circ\text{C}$) $V_{in} = 35\text{ V}$	I_{sc}	—	200	—	mA
Peak Output Current ($T_J = +25^\circ\text{C}$)	I_P	—	2.2	—	A

Note 1: Line and load regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

TL780-15C

ELECTRICAL CHARACTERISTICS ($V_{in} = 23\text{ V}$, $I_O = 500\text{ mA}$, $0^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$ unless otherwise noted [Note 1])

Characteristic	Symbol	TL780-15C			Unit
		Min	Typ	Max	
Output Voltage $5.0\text{ mA} \leq I_O \leq 1.0\text{ A}$, $P \leq 15\text{ W}$ $17.5\text{ V} \leq V_{in} \leq 30\text{ V}$ $T_J = +25^\circ\text{C}$ $0^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$	V_O	14.85 14.70	15 —	15.15 15.30	V
Line Regulation ($T_J = +25^\circ\text{C}$) $17.5\text{ V} \leq V_{in} \leq 30\text{ V}$ $20\text{ V} \leq V_{in} \leq 26\text{ V}$	Reg_{line}	— —	1.5 1.5	15 15	mV
Load Regulation ($T_J = +25^\circ\text{C}$) $5.0\text{ mA} \leq I_O \leq 1.5\text{ A}$ $250\text{ mA} \leq I_O \leq 750\text{ mA}$	Reg_{load}	— —	7.0 2.5	75 45	mV
Ripple Rejection $18.5\text{ V} \leq V_{in} \leq 28.5\text{ V}$, $f = 120\text{ Hz}$	RR	60	75	—	dB
Output Resistance ($f = 1.0\text{ kHz}$)	r_O	—	0.0035	—	Ω
Average Temperature Coefficient of Output Voltage $I_O = 5.0\text{ mA}$	TCV_O	—	0.18	—	$\text{mV}/^\circ\text{C}$
Output Noise Voltage ($T_J = +25^\circ\text{C}$) $10\text{ Hz} \leq f \leq 100\text{ kHz}$	V_n	—	225	—	μV
Dropout Voltage ($T_J = +25^\circ\text{C}$) $I_O = 1.0\text{ A}$	$V_{in}-V_O$	—	2.0	—	V
Bias Current ($T_J = +25^\circ\text{C}$)	I_B	—	3.6	8.0	mA
Bias Current Change $17.5\text{ V} \leq V_{in} \leq 30\text{ V}$, $I_O = 500\text{ mA}$ $5.0\text{ mA} \leq I_O \leq 1.0\text{ A}$, $V_{in} = 23\text{ V}$	ΔI_B	— —	0.4 0.02	1.3 0.5	mA
Short-Circuit Output Current ($T_J = +25^\circ\text{C}$) $V_{in} = 35\text{ V}$	I_{sc}	—	200	—	mA
Peak Output Current ($T_J = +25^\circ\text{C}$)	I_P	—	2.2	—	A

Note 1: Line and load regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

TYPICAL PERFORMANCE CHARACTERISTICS

VOLTAGE REGULATOR PERFORMANCE

The performance of a voltage regulator is specified by its immunity to changes in load, input voltage, power dissipation, and temperature. Line and load regulation are tested with a pulse of short duration ($< 100 \mu\text{s}$) and are strictly a function of electrical gain. However, pulse widths of longer duration ($> 1.0 \text{ ms}$) are sufficient to affect temperature gradients across the die. These temperature gradients can cause a change in the output voltage, in addition to changes caused by line and load regulation. Longer pulse widths and thermal gradients make it desirable to specify thermal regulation.

Thermal regulation is defined as the change in output voltage caused by a change in dissipated power for a specified time, and is expressed as a percentage output voltage change

per watt. The change in dissipated power can be caused by a change in either the input voltage or the load current. Thermal regulation is a function of I.C. layout and die attach techniques, and usually occurs within 10 ms of a change in power dissipation. After 10 ms, additional changes in the output voltage are due to the temperature coefficient of the device.

Figure 1 shows the line and thermal regulation response of a typical TL780-05C to a 10 watt input pulse. The variation of the output voltage due to line regulation is labeled ① and the thermal regulation component is labeled ②. Figure 2 shows the load and thermal regulation response of a typical TL780-05C to a 15 watt load pulse. The output voltage variation due to load regulation is labeled ① and the thermal regulation component is labeled ②.

FIGURE 1 — LINE AND THERMAL REGULATION

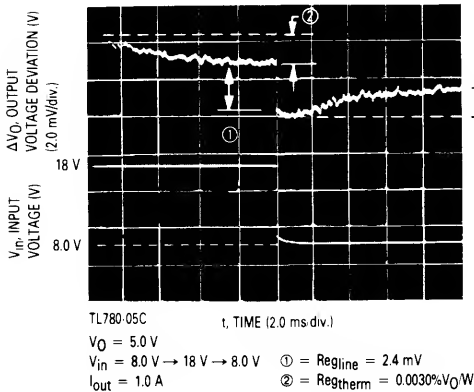


FIGURE 2 — LOAD AND THERMAL REGULATION

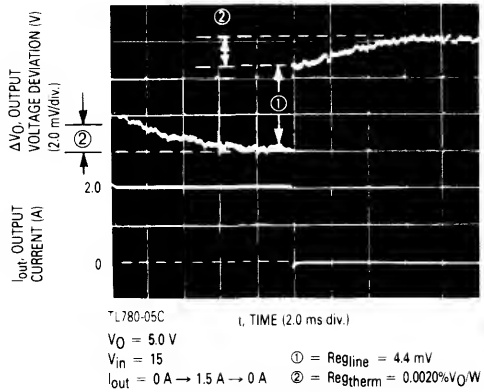


FIGURE 3 — TEMPERATURE STABILITY

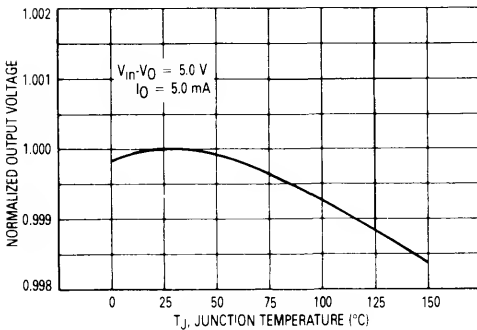


FIGURE 4 — OUTPUT IMPEDANCE

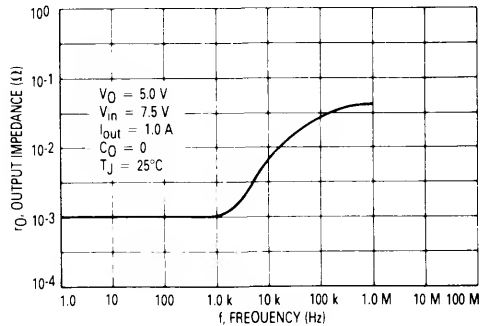


FIGURE 5 — RIPPLE REJECTION versus FREQUENCY

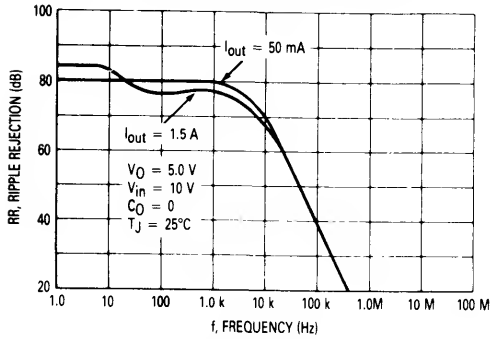


FIGURE 6 — RIPPLE REJECTION versus OUTPUT CURRENT

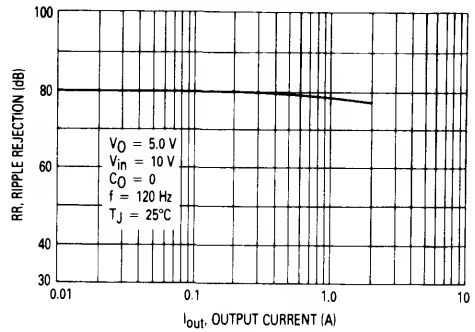


FIGURE 7 — BIAS CURRENT versus INPUT VOLTAGE

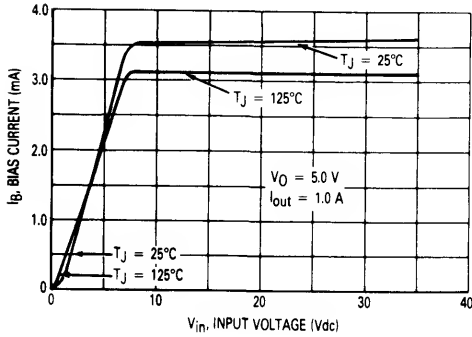


FIGURE 8 — BIAS CURRENT versus OUTPUT CURRENT

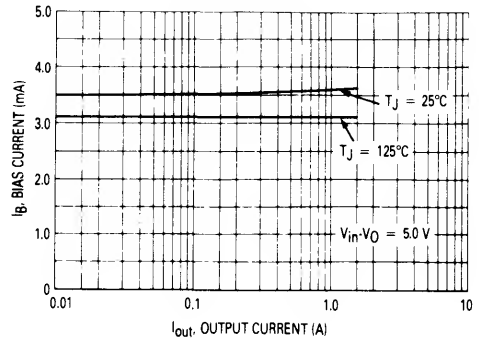


FIGURE 9 — DROPOUT VOLTAGE

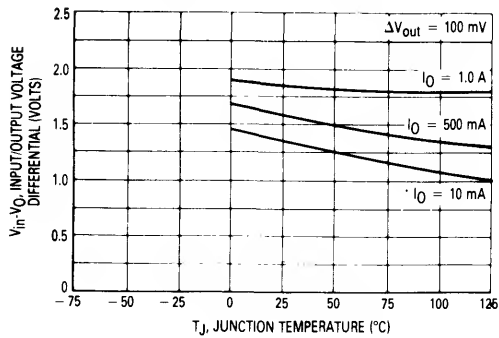
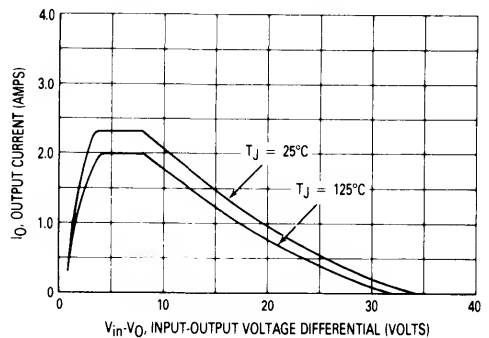


FIGURE 10 — PEAK OUTPUT CURRENT



TL780 Series

FIGURE 11 — LINE TRANSIENT RESPONSE

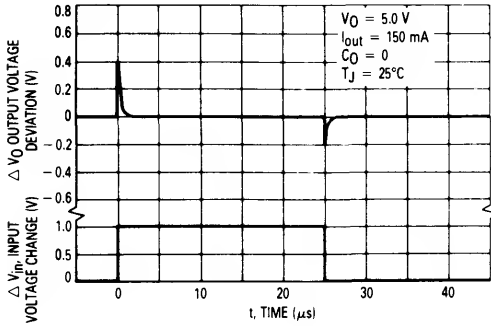
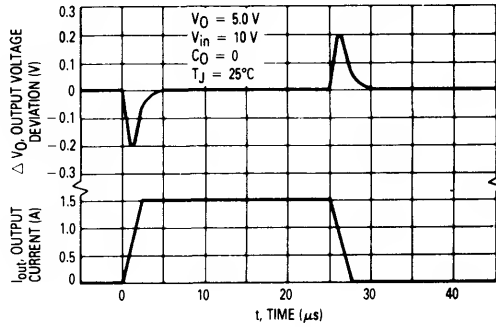
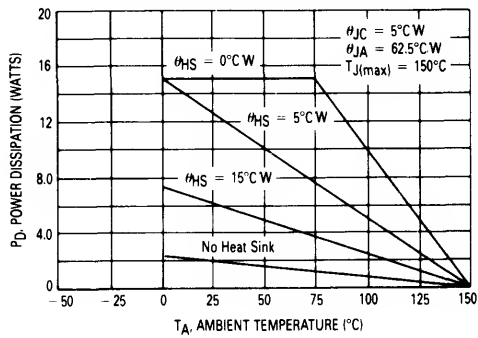


FIGURE 12 — LOAD TRANSIENT RESPONSE



**FIGURE 13 — WORST CASE POWER DISSIPATION
versus AMBIENT TEMPERATURE**



Advance Information

HIGH PERFORMANCE CURRENT MODE CONTROLLER

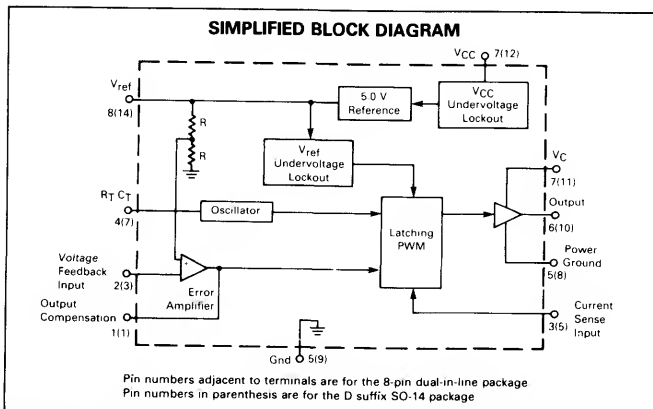
The UC3842A, UC3843A series are high performance fixed frequency current mode controllers. They are specifically designed for Off-Line and DC-to-DC converter applications offering the designer a cost effective solution with minimal external components. These integrated circuits feature a trimmed oscillator for precise duty cycle control, a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totem pole output ideally suited for driving a power MOSFET.

Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle-by-cycle current limiting, programmable output deadtime, and a latch for single pulse metering.

These devices are available in 8-pin dual-in-line ceramic and plastic packages as well as the 14-pin plastic surface mount (SO-14). The SO-14 package has separate power and ground pins for the totem pole output stage.

The UCX842A has UVLO thresholds of 16 V (on) and 10 V (off), ideally suited for off-line converters. The UCX843A is tailored for lower voltage applications having UVLO thresholds of 8.5 V (on) and 7.6 V (off).

- Trimmed Oscillator Discharge Current for Precise Duty Cycle Control
- Current Mode Operation to 500 kHz
- Automatic Feed Forward Compensation
- Latching PWM for Cycle-By-Cycle Current Limiting
- Internally Trimmed Reference with Undervoltage Lockout
- High Current Totem Pole Output
- Undervoltage Lockout with Hysteresis
- Low Start-Up and Operating Current
- Direct Interface with Motorola SENSEFET Products



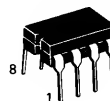
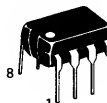
This document contains information on a new product. Specifications and information herein are subject to change without notice.

UC3842A, 43A UC2842A, 43A

HIGH PERFORMANCE CURRENT MODE CONTROLLER

SILICON MONOLITHIC INTEGRATED CIRCUIT

N SUFFIX
PLASTIC PACKAGE
CASE 626

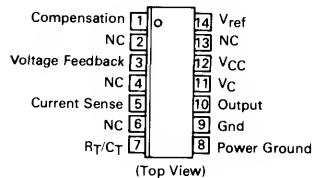
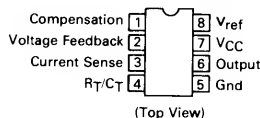


J SUFFIX
CERAMIC PACKAGE
CASE 693

D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)



PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
UC3842AD	0 to +70°C	SO-14 Plastic DIP
UC3843AD		SO-14 Plastic DIP
UC3842AN		Plastic DIP
UC3843AN		Plastic DIP
UC2842AD	-25 to +85°C	SO-14 Plastic DIP
UC2843AD		SO-14 Plastic DIP
UC2842AJ		Ceramic DIP
UC2843AJ		Ceramic DIP
UC2842AN		Plastic DIP
UC2843AN		Plastic DIP

UC3842A, UC3843A, UC2842A, UC2843A

MAXIMUM RATING

Rating	Symbol	Value	Unit
Total Power Supply and Zener Current	$(I_{CC} + I_Z)$	30	mA
Output Current, Source or Sink (Note 1)	I_O	1.0	A
Output Energy (Capacitive Load per Cycle)	W	5.0	μJ
Current Sense and Voltage Feedback Inputs	V_{in}	-0.3 to +5.5	V
Error Amp Output Sink Current	I_O	10	mA
Power Dissipation and Thermal Characteristics			
D Suffix, Plastic Package			
Maximum Power Dissipation @ $T_A = 25^\circ C$	P_D	862	mW
Thermal Resistance Junction to Air	$R_{\theta JA}$	145	$^\circ C/W$
N Suffix, Plastic Package and			
J Suffix, Ceramic Package			
Maximum Power Dissipation @ $T_A = 25^\circ C$	P_D	1.25	W
Thermal Resistance Junction to Air	$R_{\theta JA}$	100	$^\circ C/W$
Operating Junction Temperature	T_J	+150	$^\circ C$
Operating Ambient Temperature	T_A		$^\circ C$
UC3842A, UC3843A		0 to +70	
UC2842A, UC2843A		-25 to +85	
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ C$

ELECTRICAL CHARACTERISTICS ($V_{CC} = 15 V$ [Note 2], $R_T = 10 k$, $C_T = 3.3 nF$, $T_A = T_{low}$ to T_{high} [Note 3] unless otherwise noted)

Characteristic	Symbol	UC284XA			UC384XA			Unit
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION								
Reference Output Voltage ($I_O = 1.0\text{ mA}$, $T_J = 25^\circ\text{C}$)	V_{ref}	4.95	5.0	5.05	4.9	5.0	5.1	V
Line Regulation ($V_{CC} = 12\text{ V to } 25\text{ V}$)	Reg_{line}	—	2.0	20	—	2.0	20	mV
Load Regulation ($I_O = 1.0\text{ mA to } 20\text{ mA}$)	Reg_{load}	—	3.0	25	—	3.0	25	mV
Temperature Stability	T_S	—	0.2	—	—	0.2	—	mV/°C
Total Output Variation over Line, Load, and Temperature	V_{ref}	4.9	—	5.1	4.82	—	5.18	V
Output Noise Voltage ($f = 10\text{ Hz to } 10\text{ kHz}$, $T_J = 25^\circ\text{C}$)	V_n	—	50	—	—	50	—	μV
Long Term Stability ($T_A = 125^\circ\text{C}$ for 1000 Hours)	S	—	5.0	—	—	5.0	—	mV
Output Short Circuit Current	I_{SC}	−30	−85	−180	−30	−85	−180	mA

OSCILLATOR SECTION

Frequency $T_J = 25^\circ C$ $T_A = T_{low}$ to T_{high}	f_{OSC}	47 46	52 —	57 60	47 46	52 —	57 60	kHz
Frequency Change with Voltage ($V_{CC} = 12 V$ to $25 V$)	$\Delta f_{OSC}/\Delta V$	—	0.2	1.0	—	0.2	1.0	%
Frequency Change with Temperature $T_A = T_{low}$ to T_{high}	$\Delta f_{OSC}/\Delta T$	—	5.0	—	—	5.0	—	%
Oscillator Voltage Swing (Peak-to-Peak)	V_{OSC}	—	1.6	—	—	1.6	—	V
Discharge Current ($V_{OSC} = 2.0 V$) $T_J = 25^\circ C$ $T_A = T_{low}$ to T_{high}	I_{dischg}	7.5 7.2	8.4 —	9.3 9.5	7.5 7.2	8.4 —	9.3 9.5	mA

- Notes: 1. Maximum Package power dissipation limits must be observed.
2. Adjust V_{CC} above the Start-Up threshold before setting to 15 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
 $T_{low} = 0^\circ C$ for UC3842A, UC3843A $T_{high} = +70^\circ C$ for UC3842A, UC3843A
 $= -25^\circ C$ for UC2842A, UC2843A $= +85^\circ C$ for UC2842A, UC2843A
4. This parameter is measured at the latch trip point with $V_{FB} = 0 V$.
 $A_V = \frac{\Delta V \text{ Output/Compensation}}{\Delta V \text{ Current Sense Input}}$
5. Comparator gain is defined as:

UC3842A, UC3843A, UC2842A, UC2843A

ELECTRICAL CHARACTERISTICS ($V_{CC} = 15\text{ V}$ [Note 2], $R_T = 10\text{ k}$, $C_T = 3.3\text{ nF}$, $T_A = T_{\text{low}}$ to T_{high} [Note 3] unless otherwise noted)

Characteristic	Symbol	UC284XA			UC384XA			Unit
		Min	Typ	Max	Min	Typ	Max	
ERROR AMPLIFIER SECTION								
Voltage Feedback Input ($V_O = 2.5\text{ V}$)	V_{FB}	2.45	2.5	2.55	2.42	2.5	2.58	V
Input Bias Current ($V_{FB} = 2.7\text{ V}$)	I_{IB}	—	−0.1	−1.0	—	−0.1	−2.0	μA
Open-Loop Voltage Gain ($V_O = 2.0\text{ V}$ to 4.0 V)	A_{VOL}	65	90	—	65	90	—	dB
Unity Gain Bandwidth ($T_J = 25^\circ\text{C}$)	BW	0.7	1.0	—	0.7	1.0	—	MHz
Power Supply Rejection Ratio ($V_{CC} = 12\text{ V}$ to 25 V)	PSRR	60	70	—	60	70	—	dB
Output Current Sink ($V_O = 1.1\text{ V}$, $V_{FB} = 2.7\text{ V}$) Source ($V_O = 5.0\text{ V}$, $V_{FB} = 2.3\text{ V}$)	I_{Sink} I_{Source}	2.0 −0.5	12 −1.0	—	2.0 −0.5	12 −1.0	—	mA
Output Voltage Swing High State ($R_L = 15\text{ k}$ to ground, $V_{FB} = 2.3\text{ V}$) Low State ($R_L = 15\text{ k}$ to V_{ref} , $V_{FB} = 2.7\text{ V}$)	V_{OH} V_{OL}	5.0 —	6.2 0.8	— 1.1	5.0 —	6.2 0.8	— 1.1	V
CURRENT SENSE SECTION								
Current Sense Input Voltage Gain (Notes 4 & 5)	A_V	2.85	3.0	3.15	2.85	3.0	3.15	V/V
Maximum Current Sense Input Threshold (Note 4)	V_{th}	0.9	1.0	1.1	0.9	1.0	1.1	V
Power Supply Rejection Ratio $V_{CC} = 12\text{ V}$ to 25 V , Note 4	PSRR	—	70	—	—	70	—	dB
Input Bias Current	I_{IB}	—	−2.0	−10	—	−2.0	−10	μA
Propagation Delay (Current Sense Input to Output)	$t_{PLH(IN/OUT)}$	—	150	300	—	150	300	ns
OUTPUT SECTION								
Output Voltage Low State ($I_{Sink} = 20\text{ mA}$) ($I_{Sink} = 200\text{ mA}$) High State ($I_{Source} = 20\text{ mA}$) ($I_{Source} = 200\text{ mA}$)	V_{OL} V_{OH}	— 13 12	0.1 1.6 13.5 13.4	0.4 2.2 — —	— — 13 12	0.1 1.6 13.5 13.4	0.4 2.2 — —	V
Output Voltage with UVLO Activated $V_{CC} = 6.0\text{ V}$, $I_{Sink} = 1.0\text{ mA}$	$V_{OL(UVLO)}$	—	0.1	1.1	—	0.1	1.1	V
Output Voltage Rise Time ($C_L = 1.0\text{ nF}$, $T_J = 25^\circ\text{C}$)	t_r	—	50	150	—	50	150	ns
Output Voltage Fall Time ($C_L = 1.0\text{ nF}$, $T_J = 25^\circ\text{C}$)	t_f	—	50	150	—	50	150	ns
UNDERVOLTAGE LOCKOUT SECTION								
Start-Up Threshold UCX842A UCX843A	V_{th}	15 7.8	16 8.4	17 9.0	14.5 7.8	16 8.4	17.5 9.0	V
Minimum Operating Voltage After Turn-On UCX842A UCX843A	$V_{CC(min)}$	9.0 7.0	10 7.6	11 8.2	8.5 7.0	10 7.6	11.5 8.2	V
PWM SECTION								
Duty Cycle Maximum Minimum	DC_{max} DC_{min}	94 —	96 —	— 0	94 —	96 —	— 0	%
TOTAL DEVICE								
Power Supply Current Start-Up ($V_{CC} = 6.5\text{ V}$ for UCX843A, 14 V for UCX842A) Operating (Note 2)	I_{CC}	— —	0.5 12	1.0 17	— —	0.5 12	1.0 17	mA
Power Supply Zener Voltage ($I_{CC} = 25\text{ mA}$)	V_Z	30	36	—	30	36	—	V

FIGURE 1 — TIMING RESISTOR versus OSCILLATOR FREQUENCY

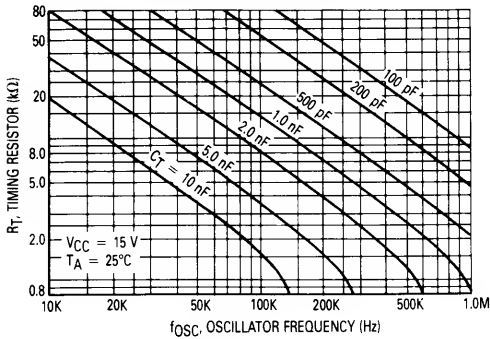


FIGURE 3 — OSCILLATOR DISCHARGE CURRENT versus TEMPERATURE

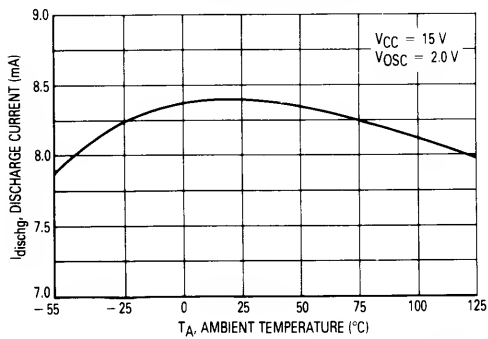


FIGURE 5 — ERROR AMP SMALL SIGNAL TRANSIENT RESPONSE

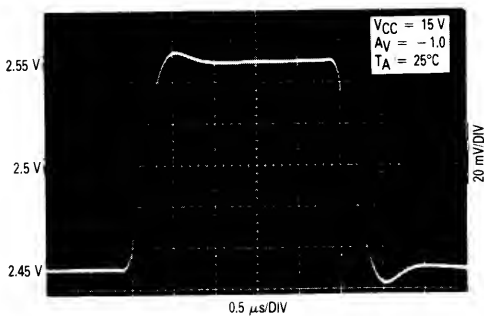


FIGURE 2 — OUTPUT DEAD TIME versus OSCILLATOR FREQUENCY

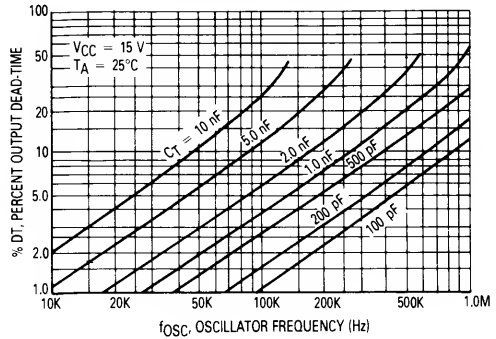


FIGURE 4 — MAXIMUM OUTPUT DUTY CYCLE versus TIMING RESISTOR

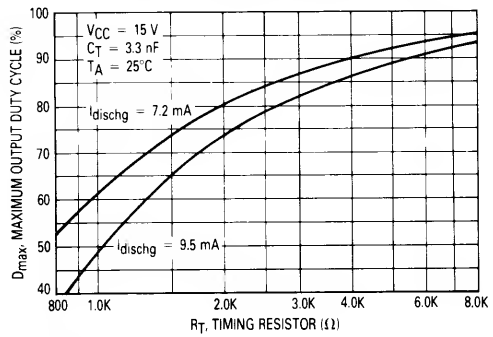


FIGURE 6 — ERROR AMP LARGE SIGNAL TRANSIENT RESPONSE

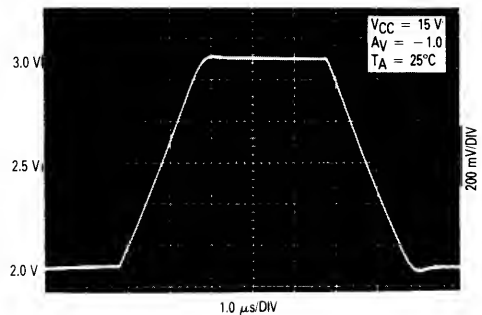


FIGURE 7 — ERROR AMP OPEN-LOOP GAIN AND PHASE versus FREQUENCY

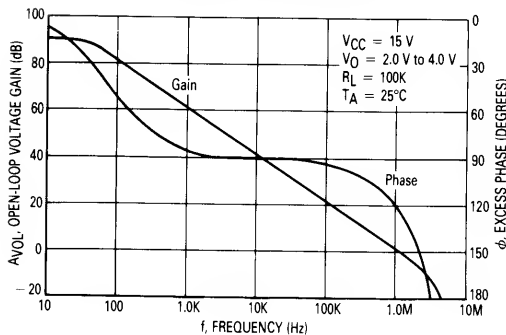


FIGURE 8 — CURRENT SENSE INPUT THRESHOLD versus ERROR AMP OUTPUT VOLTAGE

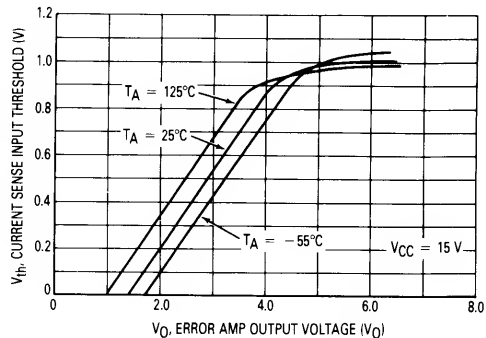


FIGURE 9 — REFERENCE VOLTAGE CHANGE versus SOURCE CURRENT

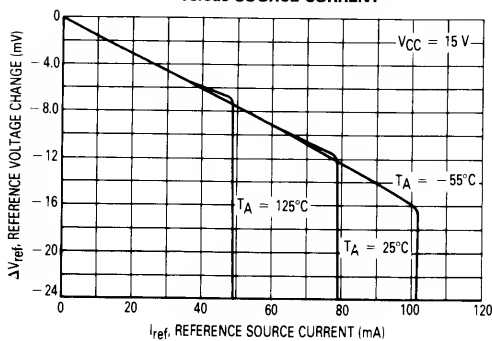


FIGURE 10 — REFERENCE SHORT CIRCUIT CURRENT versus TEMPERATURE

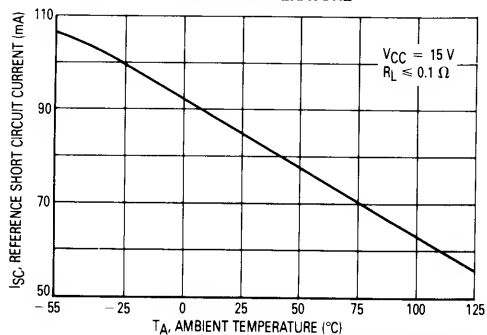


FIGURE 11 — REFERENCE LOAD REGULATION

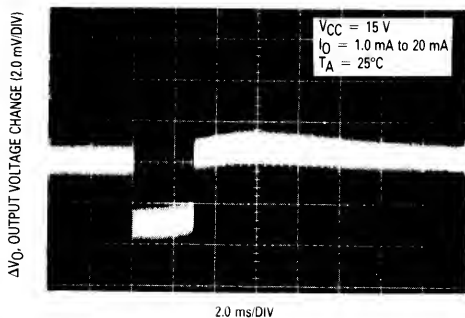
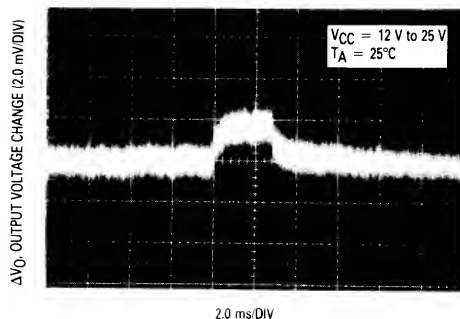


FIGURE 12 — REFERENCE LINE REGULATION



UC3842A, UC3843A, UC2842A, UC2843A

**FIGURE 13 — OUTPUT SATURATION VOLTAGE
versus LOAD CURRENT**

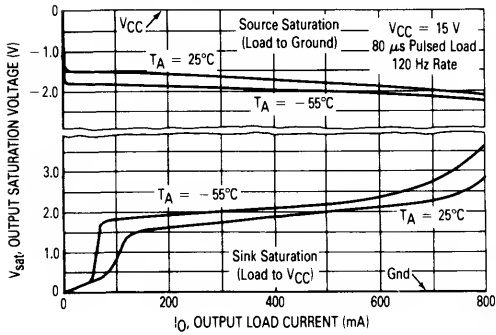


FIGURE 14 — OUTPUT WAVEFORM

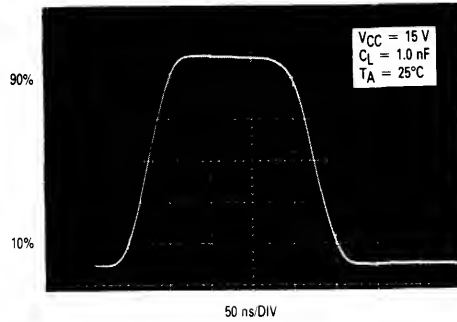


FIGURE 15 — OUTPUT CROSS CONDUCTION

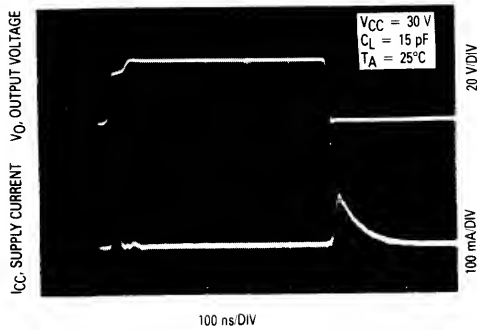
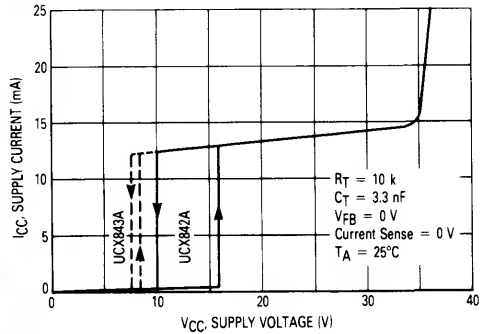


FIGURE 16 — SUPPLY CURRENT versus SUPPLY VOLTAGE



UC3842A, UC3843A, UC2842A, UC2843A

FIGURE 17 — REPRESENTATIVE BLOCK DIAGRAM

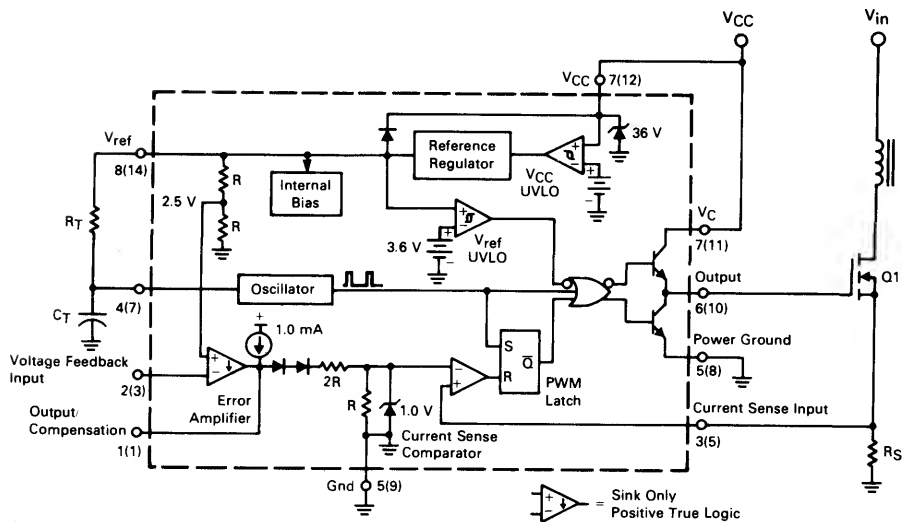
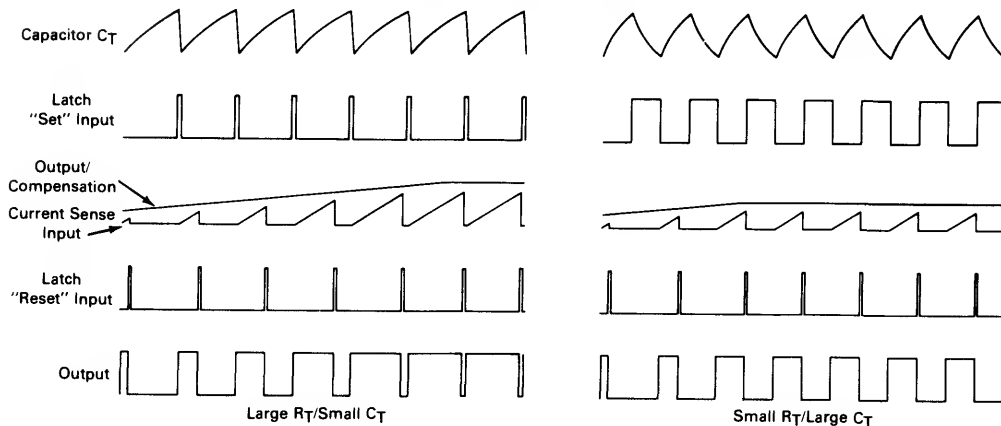


FIGURE 18 — TIMING DIAGRAM



Undervoltage Lockout

Two undervoltage lockout comparators have been incorporated to guarantee that the IC is fully functional before the output stage is enabled. The positive power supply terminal (V_{CC}) and the reference output (V_{ref}) are each monitored by separate comparators. Each has built-in hysteresis to prevent erratic output behavior as

their respective thresholds are crossed. The V_{CC} comparator upper and lower thresholds are 16 V/10 V for the UCX842A, and 8.4 V/7.6 V for the UCX843A. The V_{ref} comparator upper and lower thresholds are 3.6 V/3.4 V. The large hysteresis and low start-up current of the UCX842A makes it ideally suited in off-line converter applications where efficient bootstrap start-up tech-

niques are required (Figure 33). The UCX843A is intended for lower voltage DC to DC converter applications. A 36 V zener is connected as a shunt regulator from V_{CC} to ground. Its purpose is to protect the IC from excessive voltage that can occur during system start-up. The minimum operating voltage for the UCX842A is 11 V and 8.2 V for the UCX843A.

Output

These devices contain a single totem pole output stage that was specifically designed for direct drive of power MOSFET's. It is capable of up to ± 1.0 A peak drive current and has a typical rise and fall time of 50 ns with a 1.0 nF load. Additional internal circuitry has been added to keep the Output in a sinking mode whenever an undervoltage lockout is active. This characteristic eliminates the need for an external pull-down resistor.

The SO-14 surface mount package provides separate pins for V_C (output supply) and Power Ground. Proper implementation will significantly reduce the level of switching transient noise imposed on the control circuitry. This becomes particularly useful when reducing the $I_{pk(max)}$ clamp level. The separate V_C supply input allows the designer added flexibility in tailoring the drive voltage independent of V_{CC} . A zener clamp is typically connected to this input when driving power MOSFETs in systems where V_{CC} is greater than 20 V. Figure 25 shows proper power and control ground connections in a current sensing power MOSFET application.

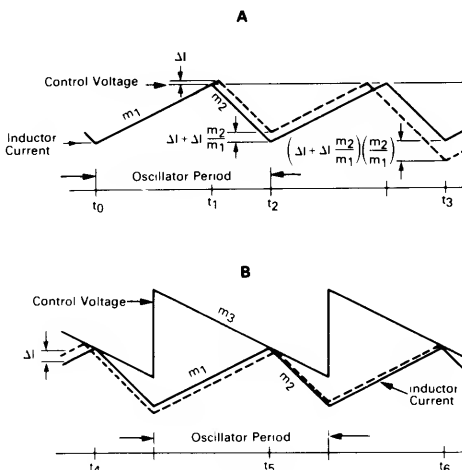
Reference

The 5.0 V bandgap reference is trimmed to $\pm 1.0\%$ tolerance at $T_J = 25^\circ\text{C}$ on the UC284XA, and $\pm 2.0\%$ on the UC384XA. Its primary purpose is to supply charging current to the oscillator timing capacitor. The reference has short circuit protection and is capable of providing in excess of 20 mA for powering additional control system circuitry.

Design Considerations

Do not attempt to construct the converter on wire-wrap or plug-in prototype boards. High frequency circuit layout techniques are imperative to prevent pulse-width jitter. This is usually caused by excessive noise pick-up imposed on the Current Sense or Voltage Feedback inputs. Noise immunity can be improved by lowering circuit impedances at these points. The printed circuit layout should contain a ground plane with low-current signal and high-current switch and output grounds returning on separate paths back to the input filter capacitor. Ceramic bypass capacitors (0.1 μF) connected directly to V_{CC} , V_C , and V_{ref} may be required depending upon circuit layout. This provides a low impedance path for filtering the high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI. The Error Amp compensation circuitry and the converter output voltage divider should be located close to the IC and as far as possible from the power switch and other noise generating components.

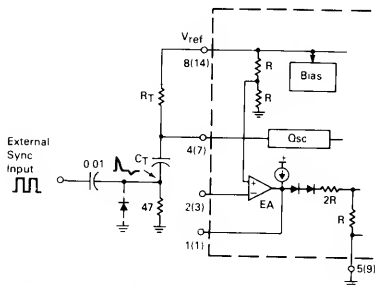
FIGURE 19 — CONTINUOUS CURRENT WAVEFORMS



Current mode converters can exhibit subharmonic oscillations when operating at a duty cycle greater than 50% with continuous inductor current. This instability is independent of the regulators closed loop characteristics and is caused by the simultaneous operating conditions of fixed frequency and peak current detecting. Figure 19A shows the phenomenon graphically. At t_0 , switch conduction begins, causing the inductor current to rise at a slope of m_1 . This slope is a function of the input voltage divided by the inductance. At t_1 , the Current Sense Input reaches the threshold established by the control voltage. This causes the switch to turn off and the current to decay at a slope of m_2 , until the next oscillator cycle. The unstable condition can be shown if a perturbation is added to the control voltage, resulting in a small ΔI (dashed line). With a fixed oscillator period, the current decay time is reduced, and the minimum current at switch turn-on (t_2) is increased by $\Delta I + \Delta I m_2/m_1$. The minimum current at the next cycle (t_3) decreases to $(\Delta I + \Delta I m_2/m_1)(m_2/m_1)$. This perturbation is multiplied by m_2/m_1 on each succeeding cycle, alternately increasing and decreasing the inductor current at switch turn-on. Several oscillator cycles may be required before the inductor current reaches zero causing the process to commence again. If m_2/m_1 is greater than 1, the converter will be unstable. Figure 19B shows that by adding an artificial ramp that is synchronized with the PWM clock to the control voltage, the ΔI perturbation will decrease to zero on succeeding cycles. This compensating ramp (m_3) must have a slope equal to or slightly greater than $m_2/2$ for stability. With $m_2/2$ slope compensation, the average inductor current follows the control voltage yielding true current mode operation. The compensating ramp can be derived from the oscillator and added to either the Voltage Feedback or Current Sense inputs (Figure 32).

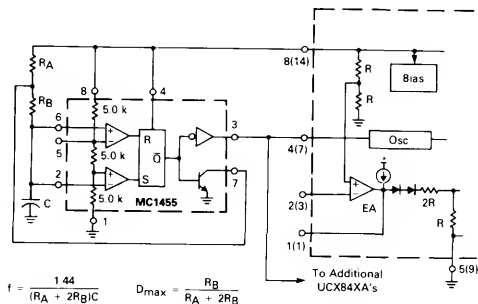
UC3842A, UC3843A, UC2842A, UC2843A

FIGURE 20 — EXTERNAL CLOCK SYNCHRONIZATION



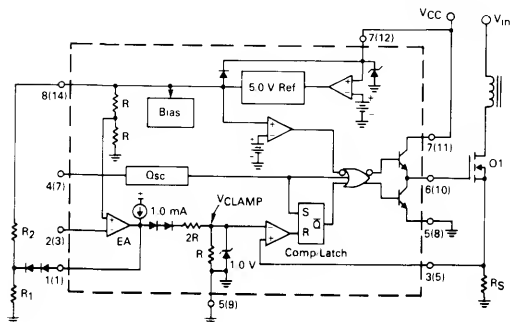
The diode clamp is required if the Sync amplitude is large enough to cause the bottom side of C_T to go more than 300 mV below ground

FIGURE 21 — EXTERNAL DUTY CYCLE CLAMP AND MULTI UNIT SYNCHRONIZATION



$$f = \frac{1.44}{(R_A + 2R_{BI})C} \quad D_{max} = \frac{R_B}{R_A + 2R_B}$$

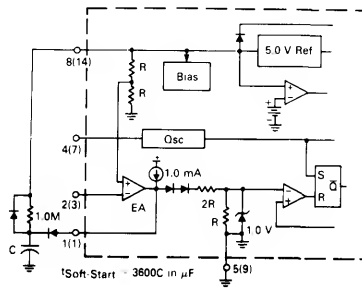
FIGURE 22 — ADJUSTABLE REDUCTION OF CLAMP LEVEL



$$V_{CLAMP} = \frac{1.67}{\left(\frac{R_2}{R_1} + 1\right)} \cdot 0.33 \times 10^{-3} \left(\frac{R_1 R_2}{R_1 + R_2}\right)$$

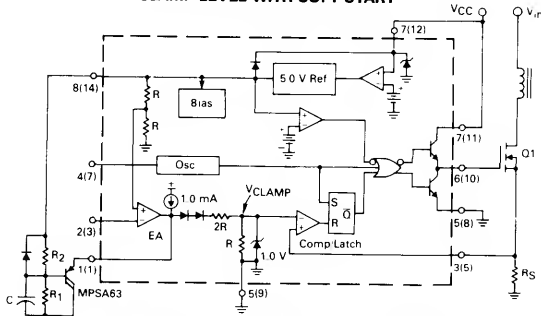
$$I_{pk(max)} = \frac{V_{CLAMP}}{R_S} \quad \text{Where } 0 < V_{CLAMP} < 1.0 \text{ V}$$

FIGURE 23 — SOFT-START CIRCUIT



$$t_{Soft\ Start} = 3600C \text{ in } \mu F$$

FIGURE 24 — ADJUSTABLE BUFFERED REDUCTION OF CLAMP LEVEL WITH SOFT-START

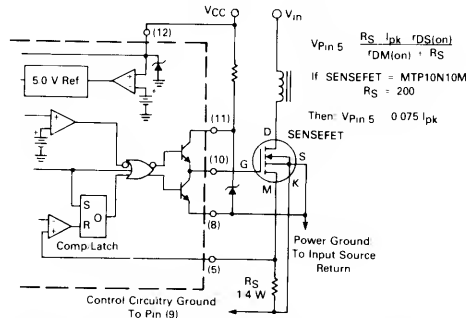


$$V_{CLAMP} = \frac{1.67}{\left(\frac{R_2}{R_1} + 1\right)}$$

$$I_{pk(max)} = \frac{V_{CLAMP}}{R_S} \quad \text{Where } 0 < V_{CLAMP} < 1.0 \text{ V}$$

$$t_{SOFTSTART} = \ln \left[1 + \frac{V_C}{3 V_{CLAMP}} \right] C \frac{R_1 R_2}{R_1 + R_2}$$

FIGURE 25 — CURRENT SENSING POWER MOSFET



$$V_{Pin\ 5} = \frac{R_S \cdot I_{pk} \cdot (DS(on) + DM(on))}{R_S}$$

$$\text{If SENSEFET} = \text{MTP10N10M}$$

$$R_S = 200$$

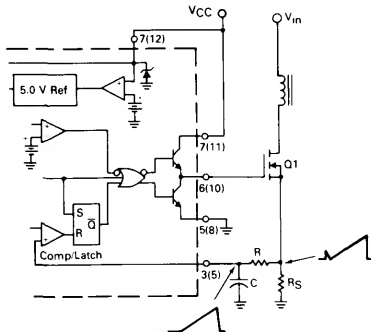
$$\text{Then } V_{Pin\ 5} = 0.075 I_{pk}$$

Virtually lossless current sensing can be achieved with the implementation of a SENSEFET power switch. For proper operation during over current conditions, a reduction of the $I_{pk(max)}$ clamp level must be implemented. Refer to Figures 22 and 24

UC3842A, UC3843A, UC2842A, UC2843A

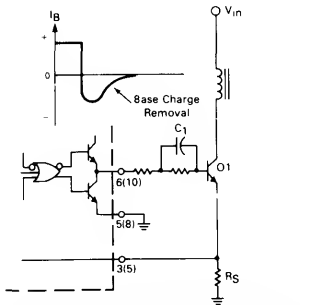
3

FIGURE 26 — CURRENT WAVEFORM SPIKE SUPPRESSION



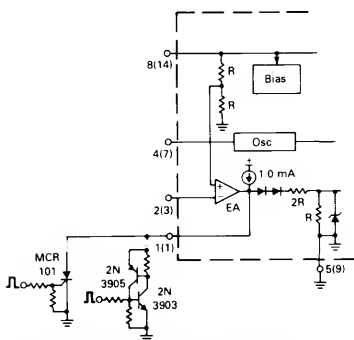
The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform.

FIGURE 28 — BIPOLAR TRANSISTOR DRIVE



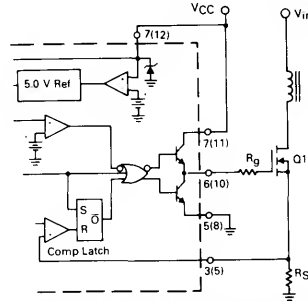
The totem-pole output can furnish negative base current for enhanced transistor turn-off, with the addition of capacitor C1.

FIGURE 30 — LATCHED SHUTDOWN



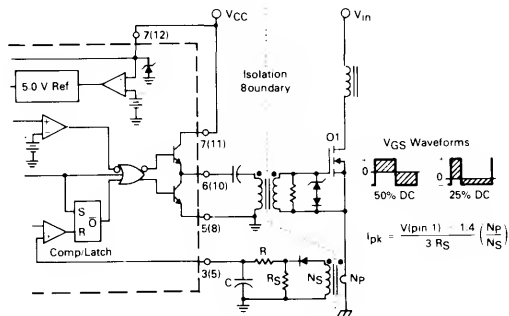
The MCR101 SCR must be selected for a holding of less than 0.5 mA at TA(min). The simple two transistor circuit can be used in place of the SCR as shown. All resistors are 10 k.

FIGURE 27 — MOSFET PARASITIC OSCILLATIONS



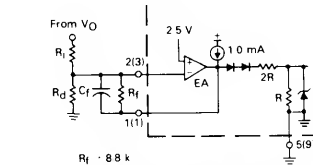
Series gate resistor Rg will damp any high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate-source circuit.

FIGURE 29 — ISOLATED MOSFET DRIVE

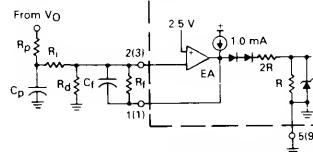


$$I_{pk} = \frac{V_{ipin 1}}{3 R_S} \left(\frac{N_p}{N_S} \right)$$

FIGURE 31 — ERROR AMPLIFIER COMPENSATION



Error Amp compensation circuit for stabilizing any current-mode topology except for boost and flyback converters operating with continuous inductor current.

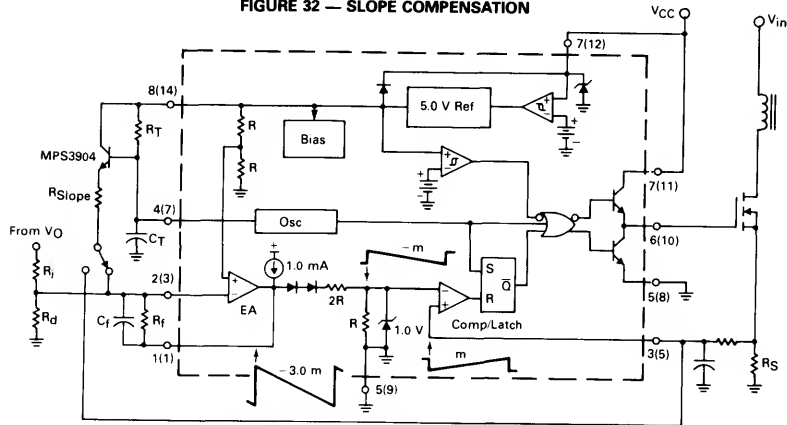


Error Amp compensation circuit for stabilizing current-mode boost and flyback topologies operating with continuous inductor current.

UC3842A, UC3843A, UC2842A, UC2843A

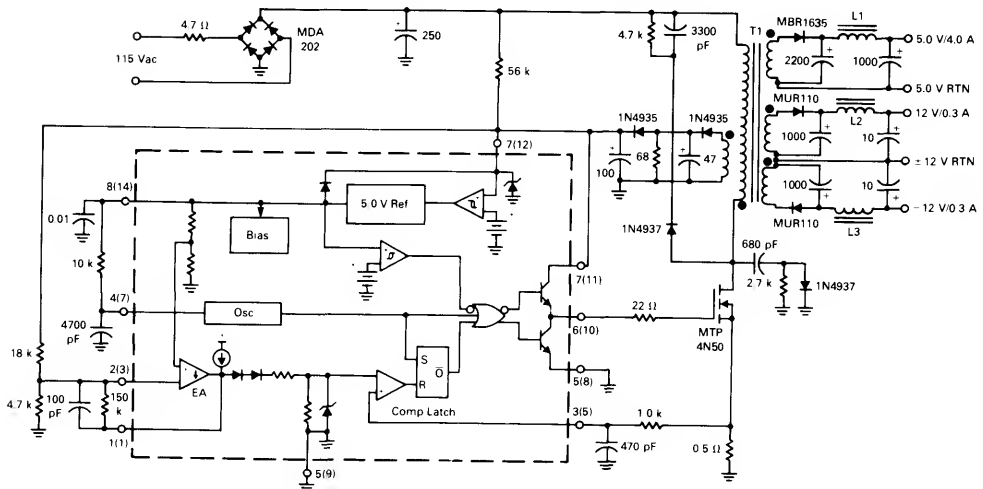
3

FIGURE 32 — SLOPE COMPENSATION



The buffered oscillator ramp can be resistively summed with either the voltage feedback or current sense inputs to provide slope compensation.

FIGURE 33 — 27 WATT OFF-LINE FLYBACK REGULATOR



T1 — Primary: 45 Turns #26 AWG
Secondary ± 12 V: 9 Turns #30 AWG (2 strands) Bifilar Wound
Secondary 5.0 V: 4 Turns (six strands) #26 Hexfililar Wound
Secondary Feedback: 10 Turns #30 AWG (2 strands) Bifilar Wound
Core: Ferroxcube EC35-3C8
Bobbin: Ferroxcube EC35PCB1
Gap = 0.01" for a primary inductance of 1.0 mH

L1 — 15 μ H at 5.0 A, Coilcraft Z7156.
L2, L3 — 25 μ H at 1.0 A, Coilcraft Z7157.

Line Regulation: 5.0 V ± 12 V	$V_{in} = 95$ to 130 Vac	$\Delta = 50$ mV or $\pm 0.5\%$ $\Delta = 24$ mV or $\pm 0.1\%$
Load Regulation: 5.0 V ± 12 V	$V_{in} = 115$ Vac, $I_{out} = 1.0$ A to 4.0 A $V_{in} = 115$ Vac, $I_{out} = 100$ mA to 300 mA	$\Delta = 300$ mV or $\pm 3.0\%$ $\Delta = 60$ mV or $\pm 0.25\%$
Output Ripple: 5.0 V ± 12 V	$V_{in} = 115$ Vac	40 mV _{p-p} 80 mV _{p-p}
Efficiency	$V_{in} = 115$ Vac	70%

All outputs are at nominal load currents unless otherwise noted.

UC3842A, UC3843A, UC2842A, UC2843A

PIN FUNCTION DESCRIPTION

Pin No.		Function	Description
8-Pin	14-Pin		
1	1	Compensation	This pin is the Error Amplifier output and is made available for loop compensation.
2	3	Voltage Feedback	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	5	Current Sense	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	7	R_T/C_T	The Oscillator frequency and maximum Output duty cycle are programmed by connecting resistor R_T to V_{ref} and capacitor C_T to ground. Operation to 500 kHz is possible.
5	—	Gnd	This pin is the combined control circuitry and power ground (8-pin package only).
6	10	Output	This output directly drives the gate of a power MOSFET. Peak currents up to 1.0 A are sourced and sunk by this pin.
7	12	V_{CC}	This pin is the positive supply of the control IC.
8	14	V_{ref}	This is the reference output. It provides charging current for capacitor C_T through resistor R_T .
—	8	Power Ground	This pin is a separate power ground return (14-pin package only) that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
—	11	V_C	The Output high state (V_{OH}) is set by the voltage applied to this pin (14-pin package only). With a separate power source connection, it can reduce the effects of switching transient noise on the control circuitry.
—	9	Gnd	This pin is the control circuitry ground return (14-pin package only) and is connected back to the power source ground.
—	2,4,6,13	NC	No connection (14-pin package only). These pins are not internally connected.

OPERATING DESCRIPTION

The UC3842A, UC3843A series are high performance, fixed frequency, current mode controllers. They are specifically designed for Off-Line and DC-to-DC converter applications offering the designer a cost effective solution with minimal external components. A representative block diagram is shown in Figure 17.

Oscillator

The oscillator frequency is programmed by the values selected for the timing components R_T and C_T . Capacitor C_T is charged from the 5.0 V reference through resistor R_T to approximately 2.8 V and discharged to 1.2 V by an internal current sink. During the discharge of C_T , the oscillator generates an internal blanking pulse that holds the center input of the NOR gate high. This causes the Output to be in a low state, thus producing a controlled amount of output deadtime. Figure 1 shows R_T versus Oscillator Frequency and Figure 2, Output Deadtime versus Frequency, both for given values of C_T . Note that many values of R_T and C_T will give the same oscillator frequency but only one combination will yield a specific output deadtime at a given frequency. The oscillator thresholds are temperature compensated, and the discharge current is trimmed and guaranteed to within $\pm 10\%$ at $T_J = 25^\circ\text{C}$. These internal circuit refinements minimize variations of oscillator frequency and maximum output duty cycle. The results are shown in Figures 3 and 4.

In many noise sensitive applications it may be desirable to frequency-lock the converter to an external system clock. This can be accomplished by applying a clock signal to the circuit shown in Figure 20. For reliable locking, the free-running oscillator frequency should be set about 10% less than the clock frequency. A method for multi unit synchronization is shown in Figure 21. By tailoring the clock waveform, accurate Output duty cycle clamping can be achieved.

Error Amplifier

A fully compensated Error Amplifier with access to the inverting input and output is provided. It features a typical DC voltage gain of 90 dB, and a unity gain bandwidth of 1.0 MHz with 57 degrees of phase margin (Figure 7). The non-inverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input. The maximum input bias current is $-2.0 \mu\text{A}$ which can cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp Output (Pin 1) is provided for external loop compensation (Figure 31). The output voltage is offset by two diode drops ($\approx 1.4 \text{ V}$) and divided by three before it connects to the inverting input of the Current Sense Comparator. This guarantees that no drive pulses appear at the Output (Pin 6) when pin 1 is at its lowest

state (V_{OL}). This occurs when the power supply is operating and the load is removed, or at the beginning of a soft-start interval (Figures 23, 24). The Error Amp minimum feedback resistance is limited by the amplifier's source current (0.5 mA) and the required output voltage (V_{OH}) to reach the comparator's 1.0 V clamp level:

$$R_f(\text{MIN}) \approx \frac{3.0 (1.0 \text{ V}) + 1.4 \text{ V}}{0.5 \text{ mA}} = 8800 \Omega$$

Current Sense Comparator and PWM Latch

The UC3842A, UC3843A operate as a current mode controller, whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier Output/Compensation (Pin 1). Thus the error signal controls the peak inductor current on a cycle-by-cycle basis. The Current Sense Comparator PWM Latch configuration used ensures that only a single pulse appears at the Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting the ground referenced sense resistor R_S in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input (Pin 3) and compared a level derived from the Error Amp Output. The peak inductor current under normal operating conditions is controlled by the voltage at pin 1 where:

$$I_{pk} = \frac{V(\text{Pin } 1) - 1.4 \text{ V}}{3 R_S}$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the Current Sense Comparator threshold will be internally clamped to 1.0 V. Therefore the maximum peak switch current is:

$$I_{pk}(\text{max}) = \frac{1.0 \text{ V}}{R_S}$$

When designing a high power switching regulator it becomes desirable to reduce the internal clamp voltage in order to keep the power dissipation of R_S to a reasonable level. A simple method to adjust this voltage is shown in Figure 22. The two external diodes are used to compensate the internal diodes yielding a constant clamp voltage over temperature. Erratic operation due to noise pickup can result if there is an excessive reduction of the $I_{pk}(\text{max})$ clamp voltage.

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Current Sense Input with a time constant that approximates the spike duration will usually eliminate the instability; refer to Figure 26.

Advance Information

HIGH PERFORMANCE CURRENT MODE CONTROLLER

The UC3844, UC3845 series are high performance fixed frequency current mode controllers. They are specifically designed for Off-Line and DC-to-DC converter applications offering the designer a cost effective solution with minimal external components. These integrated circuits feature an oscillator, a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totem pole output ideally suited for driving a power MOSFET.

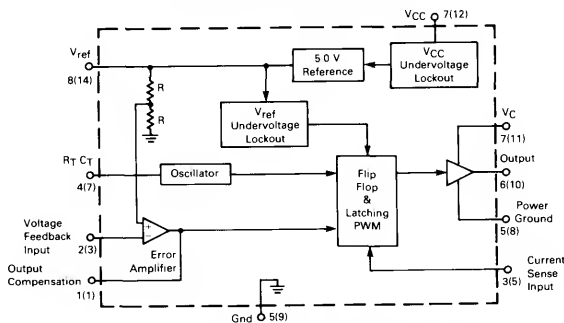
Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle-by-cycle current limiting, a latch for single pulse metering, and a flip-flop which blanks the output off every other oscillator cycle, allowing output deadtimes to be programmed from 50% to 70%.

These devices are available in 8-pin dual-in-line ceramic and plastic packages as well as the 14-pin plastic surface mount (SO-14). The SO-14 package has separate power and ground pins for the totem pole output stage.

The UC3844 has UVLO thresholds of 16 V (on) and 10 V (off), ideally suited for off-line converters. The UC3845 is tailored for lower voltage applications having UVLO thresholds of 8.5 V (on) and 7.6 V (off).

- Current Mode Operation to 500 kHz Output Switching Frequency
- Output Deadtime Adjustable from 50% to 70%
- Automatic Feed Forward Compensation
- Latching PWM for Cycle-By-Cycle Current Limiting
- Internally Trimmed Reference with Undervoltage Lockout
- High Current Totem Pole Output
- Input Undervoltage Lockout with Hysteresis
- Low Start-Up and Operating Current
- Direct Interface with Motorola SENSEFET Products

SIMPLIFIED BLOCK DIAGRAM



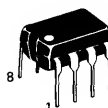
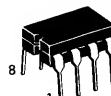
Pin numbers adjacent to terminals are for the 8 pin dual-in-line package.
 Pin numbers in parenthesis are for the D suffix SO-14 package.

UC3844, 45
UC2844, 45

HIGH PERFORMANCE CURRENT MODE CONTROLLER

SILICON MONOLITHIC
INTEGRATED CIRCUIT

N SUFFIX
PLASTIC PACKAGE
CASE 626

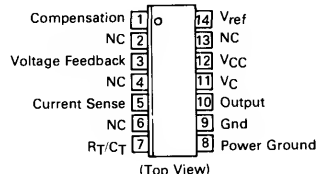
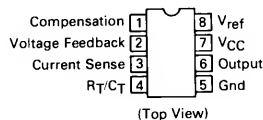


J SUFFIX
CERAMIC PACKAGE
CASE 693

D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)



PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
UC3844D	0 to +70°C	SO-14 Plastic DIP
UC3845D		SO-14 Plastic DIP
UC3844N		Plastic DIP
UC3845N		Plastic DIP
UC2844D	-25 to +85°C	SO-14 Plastic DIP
UC2845D		SO-14 Plastic DIP
UC2844J		Ceramic DIP
UC2845J		Ceramic DIP
UC2844N		Plastic DIP
UC2845N		Plastic DIP

This document contains information on a new product. Specifications and information herein are subject to change without notice.
 SENSEFET is a trademark of Motorola Inc.

MAXIMUM RATING

Rating	Symbol	Value	Unit
Total Power Supply and Zener Current	$(I_{CC} + I_Z)$	30	mA
Output Current, Source or Sink (Note 1)	I_O	1.0	A
Output Energy (Capacitive Load per Cycle)	W	5.0	μJ
Current Sense and Voltage Feedback Inputs	V_{in}	-0.3 to +5.5	V
Error Amp Output Sink Current	I_O	10	mA
Power Dissipation and Thermal Characteristics D Suffix, Plastic Package Maximum Power Dissipation @ $T_A = 25^\circ C$ Thermal Resistance Junction to Air N Suffix, Plastic Package and J Suffix, Ceramic Package Maximum Power Dissipation @ $T_A = 25^\circ C$ Thermal Resistance Junction to Air	P_D $R_{\theta JA}$	862 145	mW $^\circ C/W$
Operating Junction Temperature	T_J	+150	$^\circ C$
Operating Ambient Temperature UC3844, UC3845 UC2844, UC2845	T_A	0 to +70 -25 to +85	$^\circ C$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ C$

ELECTRICAL CHARACTERISTICS ($V_{CC} = 15 V$ [Note 2], $R_T = 10 k$, $C_T = 3.3 nF$, $T_A = T_{low}$ to T_{high} [Note 3] unless otherwise noted)

Characteristic	Symbol	UC284X			UC384X			Unit
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION								
Reference Output Voltage ($I_O = 1.0\text{ mA}$, $T_J = 25^\circ\text{C}$)	V_{ref}	4.95	5.0	5.05	4.9	5.0	5.1	V
Line Regulation ($V_{CC} = 12\text{ V}$ to 25 V)	Reg_{line}	—	2.0	20	—	2.0	20	mV
Load Regulation ($I_O = 1.0\text{ mA}$ to 20 mA)	Reg_{load}	—	3.0	25	—	3.0	25	mV
Temperature Stability	T_S	—	0.2	—	—	0.2	—	mV/°C
Total Output Variation over Line, Load, and Temperature	V_{ref}	4.9	—	5.1	4.82	—	5.18	V
Output Noise Voltage ($f = 10\text{ Hz}$ to 10 kHz , $T_J = 25^\circ\text{C}$)	V_n	—	50	—	—	50	—	μV
Long Term Stability ($T_A = 125^\circ\text{C}$ for 1000 Hours)	S	—	5.0	—	—	5.0	—	mV
Output Short Circuit Current	I_{SC}	−30	−85	−180	−30	−85	−180	mA

OSCILLATOR SECTION

Frequency $T_J = 25^\circ C$ $T_A = T_{low}$ to T_{high}	f_{OSC}	47 46	52 —	57 60	47 46	52 —	57 60	kHz
Frequency Change with Voltage ($V_{CC} = 12 V$ to $25 V$)	$\Delta f_{OSC}/\Delta V$	—	0.2	1.0	—	0.2	1.0	%
Frequency Change with Temperature $T_A = T_{low}$ to T_{high}	$\Delta f_{OSC}/\Delta T$	—	5.0	—	—	5.0	—	%
Oscillator Voltage Swing (Peak-to-Peak)	V_{OSC}	—	1.6	—	—	1.6	—	V
Discharge Current ($V_{OSC} = 2.0 V$, $T_J = 25^\circ C$)	I_{dischg}	—	10.8	—	—	10.8	—	mA

- Notes: 1. Maximum Package power dissipation limits must be observed.
2. Adjust V_{CC} above the Start-Up threshold before setting to 15 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
 $T_{low} = 0^\circ C$ for UC3844, UC3845
 $T_{low} = -25^\circ C$ for UC2844, UC2845
 $T_{high} = +70^\circ C$ for UC3844, UC3845
 $T_{high} = +85^\circ C$ for UC2844, UC2845

UC3844, UC2844, UC3845, UC2845

ELECTRICAL CHARACTERISTICS ($V_{CC} = 15\text{ V}$ [Note 2], $R_T = 10\text{ k}$, $C_T = 3.3\text{ nF}$, $T_A = T_{\text{low}}$ to T_{high} [Note 3] unless otherwise noted)

Characteristic	Symbol	UC284X			UC384X			Unit
		Min	Typ	Max	Min	Typ	Max	

ERROR AMPLIFIER SECTION

Voltage Feedback Input ($V_O = 2.5\text{ V}$)	V_{FB}	2.45	2.5	2.55	2.42	2.5	2.58	V
Input Bias Current ($V_{FB} = 2.7\text{ V}$)	I_{IB}	—	−0.1	−1.0	—	−0.1	−2.0	μA
Open-Loop Voltage Gain ($V_O = 2.0\text{ V}$ to 4.0 V)	A_{VOL}	65	90	—	65	90	—	dB
Unity Gain Bandwidth ($T_J = 25^\circ\text{C}$)	BW	0.7	1.0	—	0.7	1.0	—	MHz
Power Supply Rejection Ratio ($V_{CC} = 12\text{ V}$ to 25 V)	PSRR	60	70	—	60	70	—	dB
Output Current Sink ($V_O = 1.1\text{ V}$, $V_{FB} = 2.7\text{ V}$) Source ($V_O = 5.0\text{ V}$, $V_{FB} = 2.3\text{ V}$)	I_{Sink} I_{Source}	2.0 −0.5	12 −1.0	—	2.0 −0.5	12 −1.0	—	mA
Output Voltage Swing High State ($R_L = 15\text{ k}$ to ground, $V_{FB} = 2.3\text{ V}$) Low State ($R_L = 15\text{ k}$ to V_{ref} , $V_{FB} = 2.7\text{ V}$)	V_{OH} V_{OL}	5.0 —	6.2 0.8	— 1.1	5.0 —	6.2 0.8	— 1.1	V

CURRENT SENSE SECTION

Current Sense Input Voltage Gain (Notes 4 & 5)	A_V	2.85	3.0	3.15	2.85	3.0	3.15	V/V
Maximum Current Sense Input Threshold (Note 4)	V_{th}	0.9	1.0	1.1	0.9	1.0	1.1	V
Power Supply Rejection Ratio $V_{CC} = 12\text{ V}$ to 25 V (Note 4)	PSRR	—	70	—	—	70	—	dB
Input Bias Current	I_{IB}	—	−2.0	−10	—	−2.0	−10	μA
Propagation Delay (Current Sense Input to Output)	$t_{PLH(IN/OUT)}$	—	150	300	—	150	300	ns

OUTPUT SECTION

Output Voltage Low State ($I_{\text{Sink}} = 20\text{ mA}$) ($I_{\text{Sink}} = 200\text{ mA}$) High State ($I_{\text{Source}} = 20\text{ mA}$) ($I_{\text{Source}} = 200\text{ mA}$)	V_{OL} V_{OH}	— — 13 12	0.1 1.6 13.5 13.4	0.4 2.2 — —	— — 13 12	0.1 1.6 13.5 13.4	0.4 2.2 — —	V
Output Voltage with UVLO Activated $V_{CC} = 6.0\text{ V}$, $I_{\text{Sink}} = 1.0\text{ mA}$	$V_{OL(UVLO)}$	—	0.1	1.1	—	0.1	1.1	V
Output Voltage Rise Time ($C_L = 1.0\text{ nF}$, $T_J = 25^\circ\text{C}$)	t_r	—	50	150	—	50	150	ns
Output Voltage Fall Time ($C_L = 1.0\text{ nF}$, $T_J = 25^\circ\text{C}$)	t_f	—	50	150	—	50	150	ns

UNDERVOLTAGE LOCKOUT SECTION

Start-Up Threshold UCX844 UCX845	V_{th}	15 7.8	16 8.4	17 9.0	14.5 7.8	16 8.4	17.5 9.0	V
Minimum Operating Voltage After Turn-On UCX844 UCX845	$V_{CC(\text{min})}$	9.0 7.0	10 7.6	11 8.2	8.5 7.0	10 7.6	11.5 8.2	V

PWM SECTION

Duty Cycle Maximum Minimum	DC_{max} DC_{min}	46 —	48 —	50 0	47 —	48 —	50 0	%
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TOTAL DEVICE

Power Supply Current Start-Up ($V_{CC} = 6.5\text{ V}$ for UCX845, 14 V for UCX844) Operating (Note 2)	I_{CC}	— —	0.5 12	1.0 17	— —	0.5 12	1.0 17	mA
Power Supply Zener Voltage ($I_{CC} = 25\text{ mA}$)	V_Z	30	36	—	30	36	—	V

Notes: 4. This parameter is measured at the latch trip point with $V_{FB} = 0\text{ V}$.

5. Comparator gain is defined as: $A_V = \frac{\Delta V_{\text{Output/Compensation}}}{\Delta V_{\text{Current Sense Input}}}$

3

FIGURE 1 — TIMING RESISTOR versus OSCILLATOR FREQUENCY

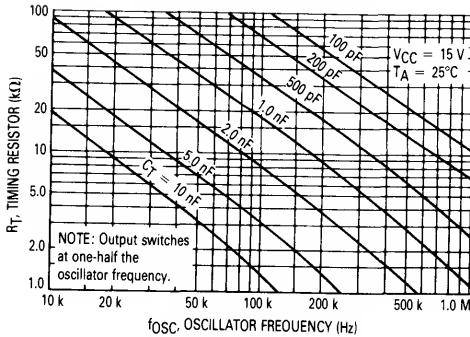


FIGURE 2 — OUTPUT DEAD TIME versus OSCILLATOR FREQUENCY

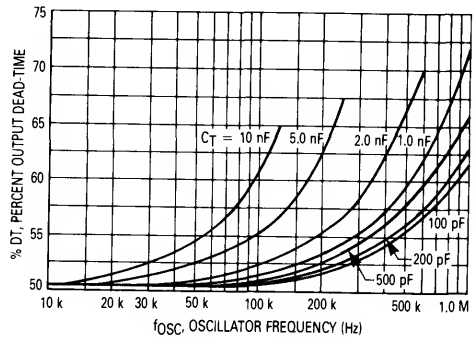


FIGURE 3 — ERROR AMP SMALL SIGNAL TRANSIENT RESPONSE

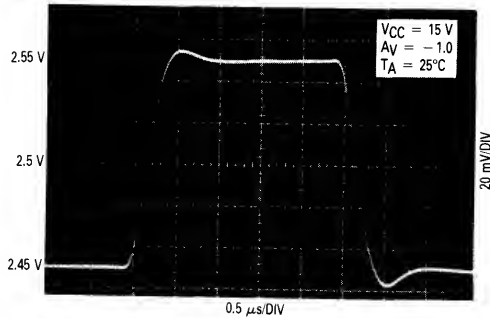


FIGURE 4 — ERROR AMP LARGE SIGNAL TRANSIENT RESPONSE

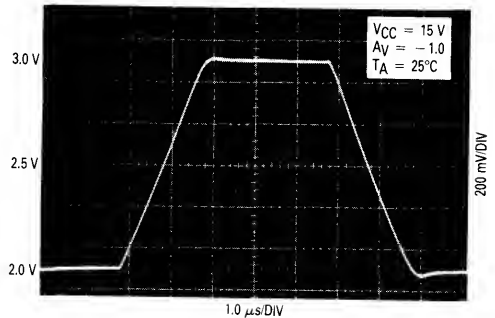


FIGURE 5 — ERROR AMP OPEN-LOOP GAIN AND PHASE versus FREQUENCY

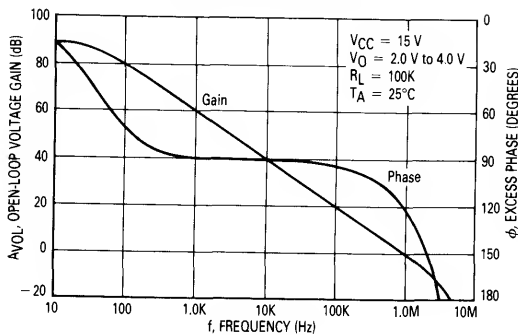
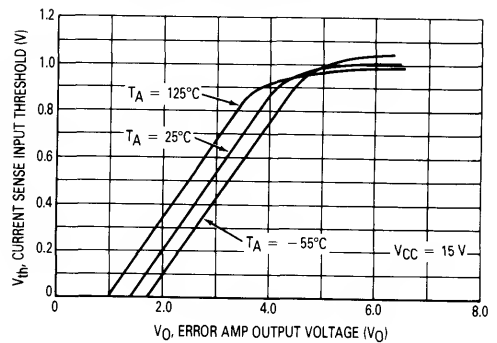
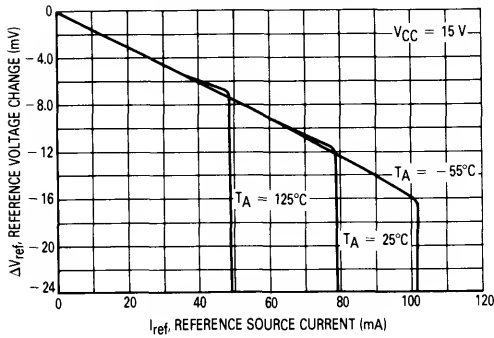


FIGURE 6 — CURRENT SENSE INPUT THRESHOLD versus ERROR AMP OUTPUT VOLTAGE



UC3844, UC2844, UC3845, UC2845

**FIGURE 7 — REFERENCE VOLTAGE CHANGE
versus SOURCE CURRENT**



**FIGURE 8 — REFERENCE SHORT CIRCUIT CURRENT
versus TEMPERATURE**

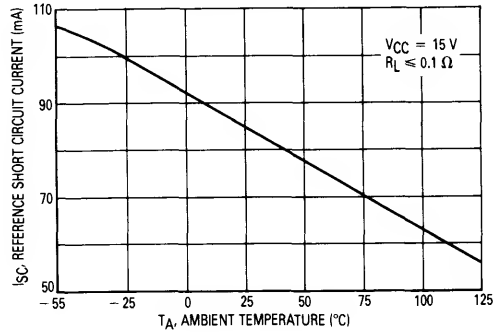


FIGURE 9 — REFERENCE LOAD REGULATION

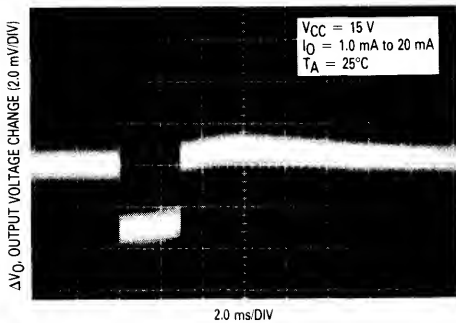
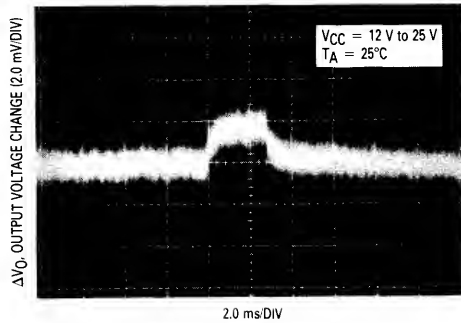


FIGURE 10 — REFERENCE LINE REGULATION



**FIGURE 11 — OUTPUT SATURATION VOLTAGE
versus LOAD CURRENT**

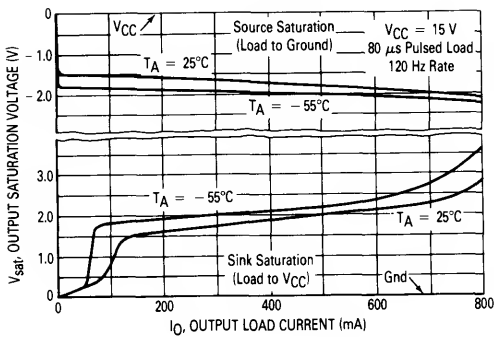
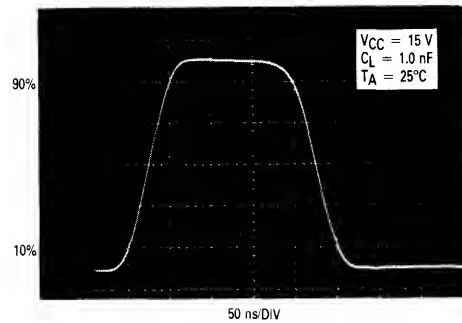


FIGURE 12 — OUTPUT WAVEFORM



UC3844, UC2844, UC3845, UC2845

FIGURE 13 — OUTPUT CROSS CONDUCTION

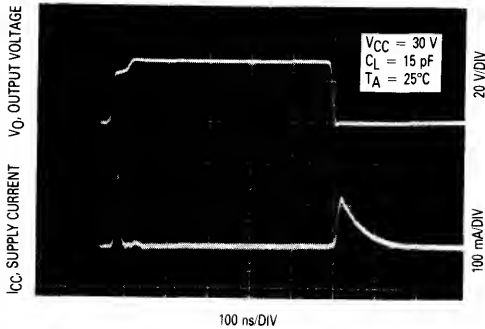
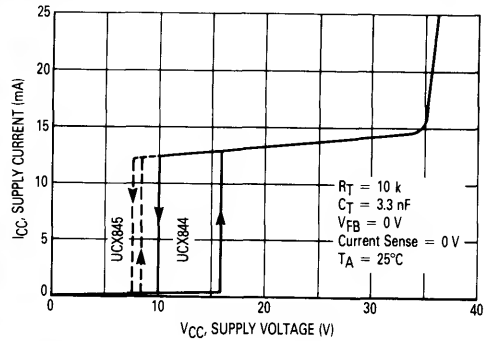


FIGURE 14 — SUPPLY CURRENT versus SUPPLY VOLTAGE



PIN FUNCTION DESCRIPTION

Pin No.		Function	Description
8-Pin	14-Pin		
1	1	Compensation	This pin is the Error Amplifier output and is made available for loop compensation.
2	3	Voltage Feedback	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	5	Current Sense	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	7	R_T/C_T	The Oscillator frequency and maximum Output duty cycle are programmed by connecting resistor R_T to V_{ref} and capacitor C_T to ground. Oscillator operation to 1.0 MHz is possible.
5	—	Gnd	This pin is the combined control circuitry and power ground (8-pin package only).
6	10	Output	This output directly drives the gate of a power MOSFET. Peak currents up to 1.0 A are sourced and sunk by this pin. The output switches at one-half the oscillator frequency.
7	12	V_{CC}	This pin is the positive supply of the control IC.
8	14	V_{ref}	This is the reference output. It provides charging current for capacitor C_T through resistor R_T .
—	8	Power Ground	This pin is a separate power ground return (14-pin package only) that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
—	11	V_C	The Output high state (V_{OH}) is set by the voltage applied to this pin (14-pin package only). With a separate power source connection, it can reduce the effects of switching transient noise on the control circuitry.
—	9	Gnd	This pin is the control circuitry ground return (14-pin package only) and is connected back to the power source ground.
—	2,4,6,13	NC	No connection (14-pin package only). These pins are not internally connected.

OPERATING DESCRIPTION

The UC3844, UC3845 series are high performance, fixed frequency, current mode controllers. They are specifically designed for Off-Line and DC-to-DC converter applications offering the designer a cost effective solution with minimal external components. A representative block diagram is shown in Figure 15.

Oscillator

The oscillator frequency is programmed by the values selected for the timing components R_T and C_T . Capacitor C_T is charged from the 5.0 V reference through resistor R_T to approximately 2.8 V and discharged to 1.2 V by an internal current sink. During the discharge of C_T , the oscillator generates an internal blanking pulse that holds the center input of the NOR gate high. This causes the Output to be in a low state, thus producing a controlled amount of output deadtime. An internal flip-flop has been incorporated in the UC3844/5 which blanks the output off every other clock cycle by holding one of the inputs of the NOR gate high. This in combination with the C_T discharge period yields output deadtimes programmable from 50% to 70%. Figure 1 shows R_T versus Oscillator Frequency and Figure 2, Output Deadtime versus Frequency, both for given values of C_T . Note that many values of R_T and C_T will give the same oscillator frequency but only one combination will yield a specific output deadtime at a given frequency.

In many noise sensitive applications it may be desirable to frequency-lock the converter to an external system clock. This can be accomplished by applying a clock signal to the circuit shown in Figure 17. For reliable locking, the free-running oscillator frequency should be set about 10% less than the clock frequency. A method for multi unit synchronization is shown in Figure 18. By tailoring the clock waveform, accurate Output duty cycle clamping can be achieved to realize output deadtimes of greater than 70%.

Error Amplifier

A fully compensated Error Amplifier with access to the inverting input and output is provided. It features a typical DC voltage gain of 90 dB, and a unity gain bandwidth of 1.0 MHz with 57 degrees of phase margin (Figure 5). The non-inverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input. The maximum input bias current is $-2.0 \mu\text{A}$ which can cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp Output (Pin 1) is provided for external loop compensation (Figure 28). The output voltage is offset by two diode drops ($\approx 1.4 \text{ V}$) and divided by three before it connects to the inverting input of the Current Sense Comparator. This guarantees that no drive pulses appear at the Output (Pin 6) when Pin 1 is at its lowest

state (V_{OL}). This occurs when the power supply is operating and the load is removed, or at the beginning of a soft-start interval (Figures 20, 21). The Error Amp minimum feedback resistance is limited by the amplifier's source current (0.5 mA) and the required output voltage (V_{OH}) to reach the comparator's 1.0 V clamp level:

$$R_f(\text{MIN}) \approx \frac{3.0 (1.0 \text{ V}) + 1.4 \text{ V}}{0.5 \text{ mA}} = 8800 \Omega$$

Current Sense Comparator and PWM Latch

The UC3844, UC3845 operate as a current mode controller, whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier Output/Compensation (Pin 1). Thus the error signal controls the peak inductor current on a cycle-by-cycle basis. The Current Sense Comparator PWM Latch configuration used ensures that only a single pulse appears at the Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting the ground referenced sense resistor R_S in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input (Pin 3) and compared to a level derived from the Error Amp Output. The peak inductor current under normal operating conditions is controlled by the voltage at pin 1 where:

$$I_{pk} = \frac{V(\text{Pin } 1) - 1.4 \text{ V}}{3 R_S}$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the Current Sense Comparator threshold will be internally clamped to 1.0 V. Therefore the maximum peak switch current is:


$$I_{pk(\text{max})} = \frac{1.0 \text{ V}}{R_S}$$

When designing a high power switching regulator it becomes desirable to reduce the internal clamp voltage in order to keep the power dissipation of R_S to a reasonable level. A simple method to adjust this voltage is shown in Figure 19. The two external diodes are used to compensate the internal diodes yielding a constant clamp voltage over temperature. Erratic operation due to noise pickup can result if there is an excessive reduction of the $I_{pk(\text{max})}$ clamp voltage.

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Current Sense Input with a time constant that approximates the spike duration will usually eliminate the instability; refer to Figure 23.

FIGURE 15 — REPRESENTATIVE BLOCK DIAGRAM

Legend: $\left(\begin{array}{c} + \\ - \end{array} \right) = \text{Sink Only Positive True Logic}$

 = Sink Only
Positive True Logic

The figure displays two sets of timing diagrams for a current-mode DAC, comparing the behavior for **Large R_T /Small C_T** (left) and **Small R_T /Large C_T** (right).

The signals shown are:

- Capacitor C_T** : Shows the voltage across the capacitor. In the left case, it has a high-frequency sawtooth pattern. In the right case, it has a lower-frequency sawtooth pattern.
- Latch "Set" Input**: A series of narrow pulses that trigger the DAC output.
- Output/Compensation**: A signal that ramps up during the "Set" phase and then levels off.
- Current Sense Input**: A signal that ramps up during the "Set" phase and then levels off.
- Latch "Reset" Input**: A series of narrow pulses that trigger the DAC output.
- Output**: The final DAC output signal, which is a square wave.

Undervoltage Lockout

Two undervoltage lockout comparators have been incorporated to guarantee that the IC is fully functional before the output stage is enabled. The positive power supply terminal (V_{CC}) and the reference output (V_{ref}) are each monitored by separate comparators. Each has built-in hysteresis to prevent erratic output behavior as their respective thresholds are crossed. The V_{CC} comparator upper and lower thresholds are 16 V/10 V for the UCX844, and 8.4 V/7.6 V for the UCX845. The V_{ref} comparator upper and lower thresholds are 3.6 V/3.4 V. The large hysteresis and low start-up current of the UCX844 makes it ideally suited in off-line converter applications where efficient bootstrap start-up techniques are required (Figure 29). The UCX845 is intended for lower voltage DC-to-DC converter applications. A 36 V zener is connected as a shunt regulator from V_{CC} to ground. Its purpose is to protect the IC from excessive voltage that can occur during system start-up. The minimum operating voltage for the UCX844 is 11 V and 8.2 V for the UCX845.

Output

These devices contain a single totem pole output stage that was specifically designed for direct drive of power MOSFET's. It is capable of up to ± 1.0 A peak drive current and has a typical rise and fall time of 50 ns with a 1.0 nF load. Additional internal circuitry has been added to keep the Output in a sinking mode whenever an undervoltage lockout is active. This characteristic eliminates the need for an external pull-down resistor.

The SO-14 surface mount package provides separate pins for V_C (output supply) and Power Ground. Proper implementation will significantly reduce the level of switching transient noise imposed on the control circuitry. This becomes particularly useful when reducing the $I_{pk(max)}$ clamp level. The separate V_C supply input allows the designer added flexibility in tailoring the

drive voltage independent of V_{CC} . A zener clamp is typically connected to this input when driving power MOSFETs in systems where V_{CC} is greater than 20 V. Figure 22 shows proper power and control ground connections in a current sensing power MOSFET application.

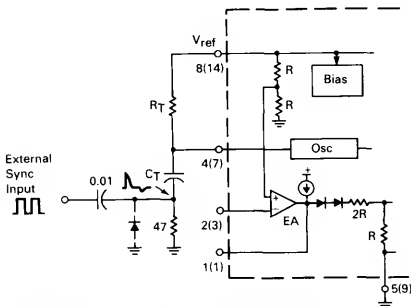
Reference

The 5.0 V bandgap reference is trimmed to $\pm 1.0\%$ tolerance at $T_J = 25^\circ\text{C}$ on the UC284X, and $\pm 2.0\%$ on the UC384X. Its primary purpose is to supply charging current to the oscillator timing capacitor. The reference has short circuit protection and is capable of providing in excess of 20 mA for powering additional control system circuitry.

Design Considerations

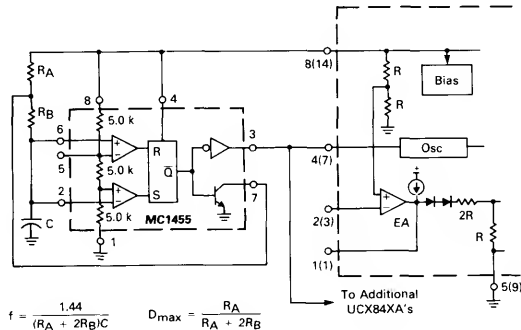
Do not attempt to construct the converter on wire-wrap or plug-in prototype boards. High frequency circuit layout techniques are imperative to prevent pulse-width jitter. This is usually caused by excessive noise pick-up imposed on the Current Sense or Voltage Feedback inputs. Noise immunity can be improved by lowering circuit impedances at these points. The printed circuit layout should contain a ground plane with low-current signal and high-current switch and output grounds returning on separate paths back to the input filter capacitor. Ceramic bypass capacitors (0.1 μF) connected directly to V_{CC} , V_C , and V_{ref} may be required depending upon circuit layout. This provides a low impedance path for filtering the high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI. The Error Amp compensation circuitry and the converter output voltage divider should be located close to the IC and as far as possible from the power switch and other noise generating components.

FIGURE 17 — EXTERNAL CLOCK SYNCHRONIZATION



The diode clamp is required if the Sync amplitude is large enough to cause the bottom side of C_T to go more than 300 mV below ground.

FIGURE 18 — EXTERNAL DUTY CYCLE CLAMP AND MULTI UNIT SYNCHRONIZATION



$$f = \frac{1.44}{(R_A + 2R_B)C} \quad D_{max} = \frac{R_A}{R_A + 2R_B}$$

FIGURE 19 — ADJUSTABLE REDUCTION OF CLAMP LEVEL

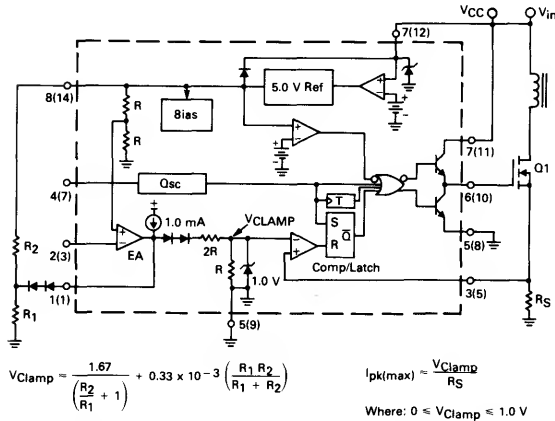


FIGURE 20 — SOFT-START CIRCUIT

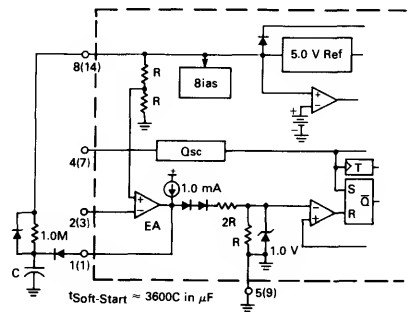


FIGURE 21 — ADJUSTABLE BUFFERED REDUCTION OF CLAMP LEVEL WITH SOFT-START

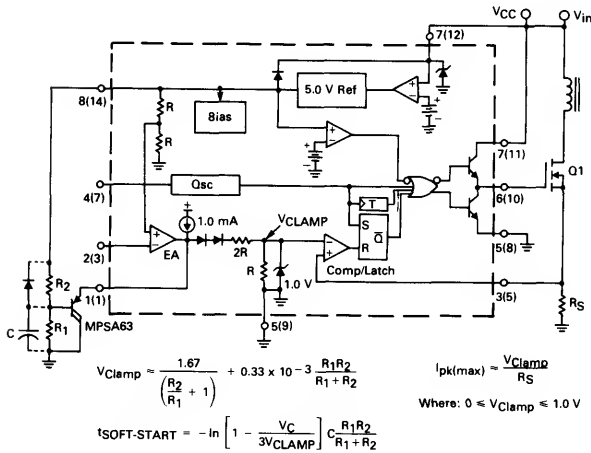
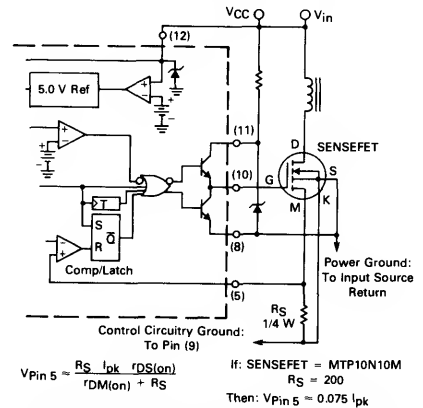
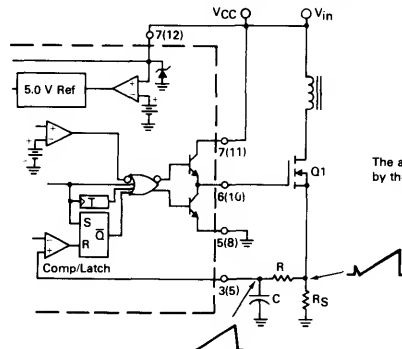


FIGURE 22 — CURRENT SENSING POWER MOSFET



Virtually lossless current sensing can be achieved with the implementation of a SENSEFET power switch. For proper operation during over current conditions, a reduction of the $I_{\text{pk(max)}}$ clamp level must be implemented. Refer to Figures 19 and 21.

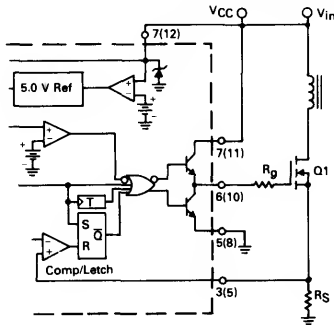
FIGURE 23 — CURRENT WAVEFORM SPIKE SUPPRESSION



The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform.

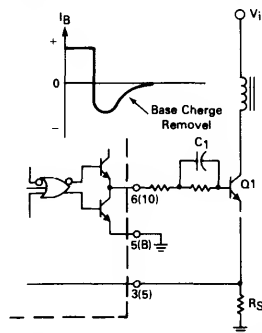
UC3844, UC2844, UC3845, UC2845

FIGURE 24 — MOSFET PARASITIC OSCILLATIONS



Series gate resistor R_g will damp any high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate-source circuit.

FIGURE 25 — BIPOLAR TRANSISTOR DRIVE



The totem-pole output can furnish negative base current for enhanced transistor turn-off, with the addition of capacitor C_1 .

FIGURE 26 — ISOLATED MOSFET DRIVE

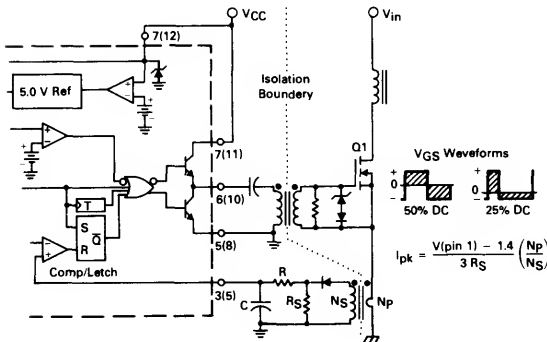
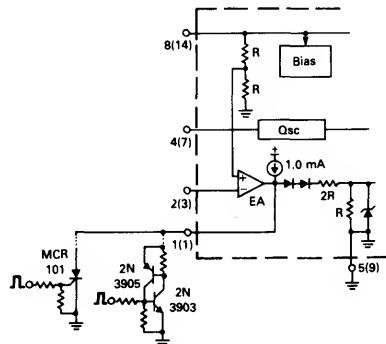
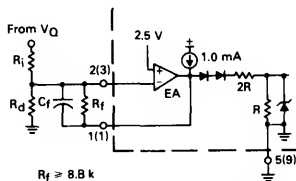


FIGURE 27 — LATCHED SHUTDOWN

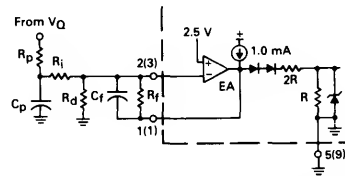


The MCR101 SCR must be selected for a holding of less than 0.5 mA at $T_A(\min)$. The simple two transistor circuit can be used in place of the SCR as shown. All resistors are 10 k.

FIGURE 28 — ERROR AMPLIFIER COMPENSATION



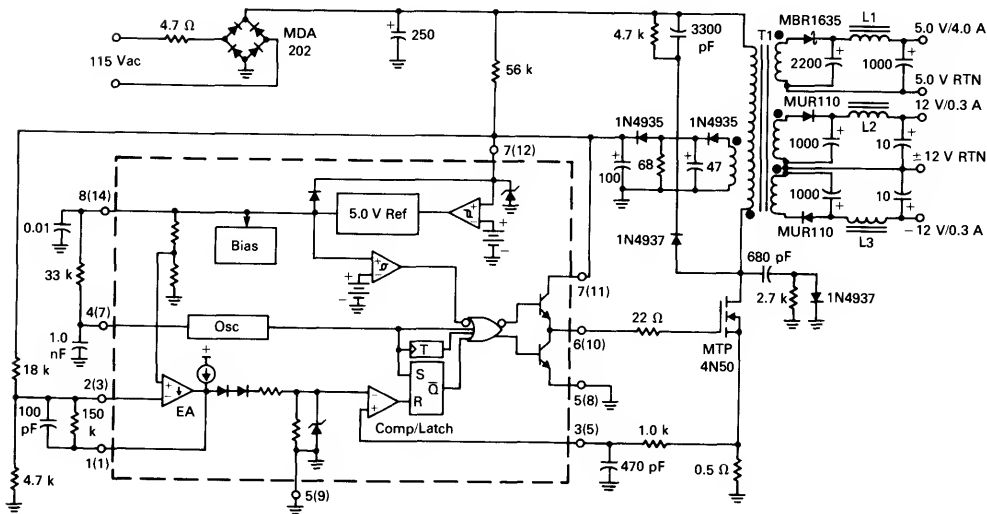
Error Amp compensation circuit for stabilizing any current-mode topology except for boost and flyback converters operating with continuous inductor current.



Error Amp compensation circuit for stabilizing current-mode boost and flyback topologies operating with continuous inductor current.

UC3844, UC2844, UC3845, UC2845

FIGURE 29 — 27 WATT OFF-LINE FLYBACK REGULATOR



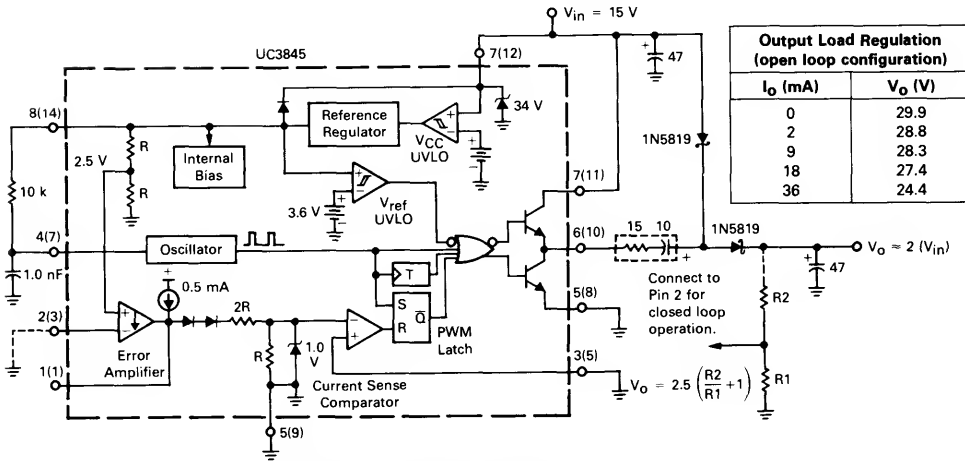
T1 — Primary: 45 Turns #26 AWG
 Secondary ± 12 V: 9 Turns #30 AWG (2 strands) Bifilar Wound
 Secondary 5.0 V: 4 Turns (six strands) #26 Hexfilar Wound
 Secondary Feedback: 10 Turns #30 AWG (2 strands) Bifilar Wound
 Core: Ferroxcube EC35-3C8
 Bobbin: Ferroxcube EC35PCB1
 Gap: = 0.10" for a primary inductance of 1.0 mH

L1 — 15 μ H at 5.0 A, Coilcraft Z7156.
 L2, L3 — 25 μ H at 1.0 A, Coilcraft Z7157.

Line Regulation: 5.0 V ± 12 V	$V_{in} = 95$ to 130 Vac	$\Delta = 50$ mV or $\pm 0.5\%$ $\Delta = 24$ mV or $\pm 0.1\%$
Load Regulation: 5.0 V ± 12 V	$V_{in} = 115$ Vac, $I_{out} = 1.0$ A to 4.0 A $V_{in} = 115$ Vac, $I_{out} = 100$ mA to 300 mA	$\Delta = 300$ mV or $\pm 3.0\%$ $\Delta = 60$ mV or $\pm 0.25\%$
Output Ripple: 5.0 V ± 12 V	$V_{in} = 115$ Vac	40 mV _{p-p} 80 mV _{p-p}
Efficiency	$V_{in} = 115$ Vac	70%

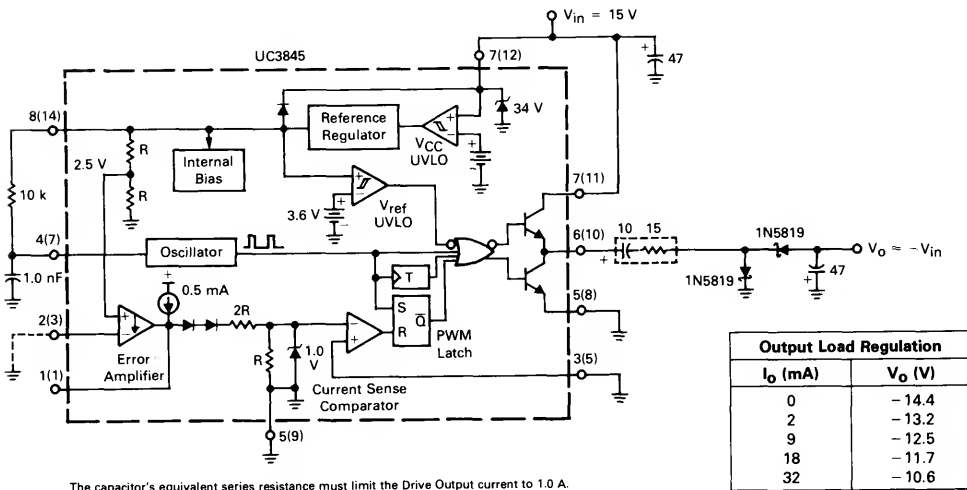
All outputs are at nominal load currents unless otherwise noted.

FIGURE 30 — STEP-UP CHARGE PUMP CONVERTER



The capacitor's equivalent series resistance must limit the Drive Output current to 1.0 A. An additional series resistor may be required when using tantalum or other low ESR capacitors. The converter's output can provide excellent line and load regulation by connecting the R2/R1 resistor divider as shown.

FIGURE 31 — VOLTAGE-INVERTING CHARGE PUMP CONVERTER



The capacitor's equivalent series resistance must limit the Drive Output current to 1.0 A. An additional series resistor may be required when using tantalum or other low ESR capacitors.

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

3

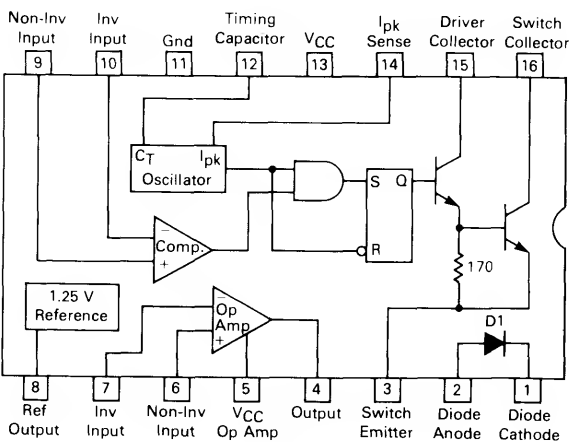
UNIVERSAL SWITCHING REGULATOR SUBSYSTEM

The $\mu A78S40$ is a monolithic-switching regulator subsystem, providing all active functions necessary for a switching regulator system. The device consists of a temperature compensated voltage reference, controlled-duty cycle oscillator with an active current limit circuit, comparator, high-current and high-voltage output switch, capable of 1.5 A and 40 V, pinned-out power diode and an uncommitted operational amplifier, which can be powered up or down independent of the IC supply. The switching output can drive external NPN or PNP transistors when voltages greater than 40 V, or currents in excess of 1.5 A, are required. Some of the features are wide-supply voltage range, low standby current, high efficiency and low drift. The $\mu A78S40$ is available in commercial (0°C to +70°C), automotive (-40°C to +85°C), and military (-55°C to +125°C) temperature ranges.

Some of the applications include use in step-up, step-down, and inverting regulators, with extremely good results obtained in battery-operated systems.

- Output Adjustable from 1.25 V to 40 V
- Peak Output Current of 1.5 A Without External Transistor
- 80 dB Line and Load Regulation
- Operation from 2.5 V to 40 V Supply
- Low Standby Current Drain
- High Gain, High Output Current, Uncommitted Op Amp

BLOCK DIAGRAM

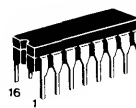


(Bottom View)

$\mu A78S40$

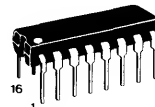
UNIVERSAL SWITCHING REGULATOR SUBSYSTEM

SILICON MONOLITHIC INTEGRATED CIRCUIT

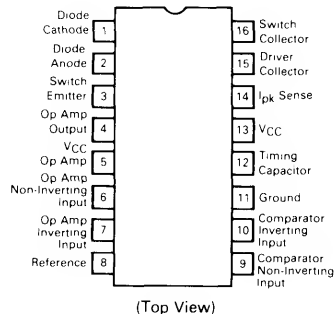


D SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
$\mu A78S40PC$	0°C to +70°C	Plastic DIP
$\mu A78S40PV$	-40°C to +85°C	Plastic DIP
$\mu A78S40DC$	0°C to +70°C	Ceramic DIP
$\mu A78S40DM$	-55°C to +125°C	Ceramic DIP

μ A78S40

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	V
Op Amp Power Supply Voltage	V_{CC} (Op Amp)	40	V
Common Mode Input Range (Comparator and Op Amp)	V_{ICR}	-0.3 to V_{CC}	V
Differential Input Voltage (Note 2)	V_{ID}	± 30	V
Output Short-Circuit Duration (Op Amp)	—	Continuous	—
Reference Output Current	I_{ref}	10	mA
Voltage from Switch Collectors to Gnd	—	40	V
Voltage from Switch Emitters to Gnd	—	40	V
Voltage from Switch Collectors to Emitter	—	40	V
Voltage from Power Diode to Gnd	—	40	V
Reverse-Power Diode Voltage	V_{DR}	40	V
Current through Power Switch	I_{SW}	1.5	A
Current through Power Diode	I_D	1.5	A
Power Dissipation and Thermal Characteristics			
Plastic Package — $T_A = +25^\circ\text{C}$	P_D	1500	mW
Derate above $+25^\circ\text{C}$ (Note 1)	1 $R_{\theta JA}$	14	mW/°C
Ceramic Package — $T_A = +25^\circ\text{C}$	P_D	1000	mW
Derate above $+25^\circ\text{C}$ (Note 1)	1 $R_{\theta JA}$	8.0	mW/°C
Storage Temperature Range	T_{stg}	-65 to $+150$	°C
Operating Temperature Range	T_A		°C
$\mu\text{A78S40M}$		-55 to $+125$	
$\mu\text{A78S40V}$		-40 to $+85$	
$\mu\text{A78S40C}$		0 to $+70$	

Notes:

- $T_{low} = -55^\circ\text{C}$ for $\mu\text{A78S40DM}$
 $= -40^\circ\text{C}$ for $\mu\text{A78S40PV}$
 $= 0^\circ\text{C}$ for $\mu\text{A78S40DC}$ and $\mu\text{A78S40PC}$
 - $T_{high} = +125^\circ\text{C}$ for $\mu\text{A78S40DM}$
 $= +85^\circ\text{C}$ for $\mu\text{A78S40PV}$
 $= +70^\circ\text{C}$ for $\mu\text{A78S40DC}$ and $\mu\text{A78S40PC}$
2. For supply voltages less than 30 V the maximum differential input voltage (Error Amp and Op Amp) is equal to the supply voltage.

ELECTRICAL CHARACTERISTICS ($V_{CC} = V_{CC}$ (Op Amp) 5.0 V, T_A T_{low} to T_{high} unless otherwise noted.)

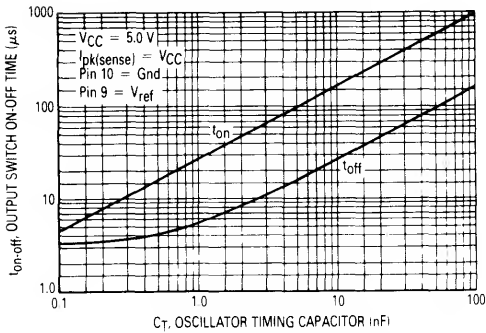
Characteristic	Symbol	Min	Typ	Max	Unit
GENERAL					
Supply Voltage	V_{CC}	2.5	—	40	V
Supply Current (Op Amp V_{CC} Disconnected) ($V_{CC} = 5.0$ V) ($V_{CC} = 40$ V)	I_{CC}	— —	1.8 2.3	3.5 5.0	mA
Supply Current (Op Amp V_{CC} Connected) ($V_{CC} = 5.0$ V) ($V_{CC} = 40$ V)	I_{CC}	— —	— —	4.0 5.5	mA
REFERENCE					
Reference Voltage ($I_{ref} = 1.0$ mA)	V_{ref}	1.180	1.245	1.310	V
Reference Voltage Line Regulation (3.0 V $\leq V_{CC} \leq 40$ V, $I_{ref} = 1.0$ mA, $T_A = 25^\circ\text{C}$)	Reg_{line}	—	0.04	0.2	mV/V
Reference Voltage Load Regulation (1.0 mA $\leq I_{ref} \leq 10$ mA, $T_A = 25^\circ\text{C}$)	Reg_{load}	—	0.2	0.5	mV/mA

μA78S40

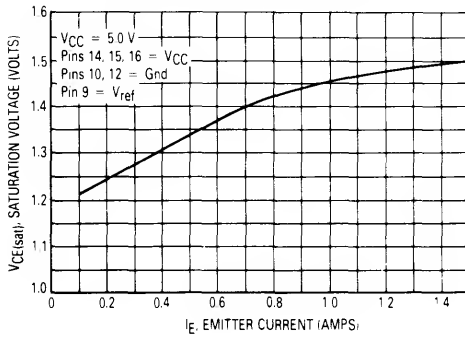
ELECTRICAL CHARACTERISTICS (Continued) ($V_{CC} = V_{CC} \text{ [Op Amp]} = 5.0 \text{ V}$, $T_A = T_{\text{low}}$ to T_{high} unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Charging Current ($T_A = 25^\circ\text{C}$) ($V_{CC} = 5.0 \text{ V}$) ($V_{CC} = 40 \text{ V}$)	I_{chg}	20 20	— —	50 70	μA
Discharge Current ($T_A = 25^\circ\text{C}$) ($V_{CC} = 5.0 \text{ V}$) ($V_{CC} = 40 \text{ V}$)	I_{dis}	150 150	— —	250 350	μA
Oscillator Voltage Swing ($T_A = 25^\circ\text{C}$) ($V_{CC} = 5.0 \text{ V}$)	V_{osc}	—	0.5	—	V
Ratio of Charge/Discharge Time	$t_{\text{chg}}/t_{\text{dis}}$	—	6.0	—	—
CURRENT LIMIT					
Current-Limit Sense Voltage ($T_A = 25^\circ\text{C}$) ($V_{CC} = V_{\text{IpK}}$ Sense)	V_{CLS}	250	—	350	mV
OUTPUT SWITCH					
Output Saturation Voltage 1 ($I_{\text{SW}} = 1.0 \text{ A}$, Pin 15 tied to Pin 16)	V_{sat1}	—	0.93	1.3	V
Output Saturation Voltage 2 ($I_{\text{SW}} = 1.0 \text{ A}$, $I_{15} = 50 \text{ mA}$)	V_{sat2}	—	0.5	0.7	V
Output Transistor Current Gain ($T_A = 25^\circ\text{C}$) ($I_C = 1.0 \text{ A}$, $V_{CE} = 5.0 \text{ V}$)	h_{FE}	—	70	—	—
Output Leakage Current ($T_A = 25^\circ\text{C}$) ($V_{CE} = 40 \text{ V}$)	$I_{C(\text{off})}$	—	10	—	nA
POWER DIODE					
Forward Voltage Drop ($I_D = 1.0 \text{ A}$)	V_D	—	1.25	1.5	V
Diode Leakage Current ($T_A = 25^\circ\text{C}$) ($V_{DR} = 40 \text{ V}$)	I_{DR}	—	10	—	nA
COMPARATOR					
Input Offset Voltage ($V_{CM} = V_{\text{Ref}}$)	V_{IO}	—	1.5	15	mV
Input Bias Current ($V_{CM} = V_{\text{Ref}}$)	I_{IB}	—	35	200	nA
Input Offset Current ($V_{CM} = V_{\text{Ref}}$)	I_{IO}	—	5.0	75	nA
Common-Mode Voltage Range ($T_A = 25^\circ\text{C}$)	V_{ICR}	0	—	$V_{CC} - 2.0$	V
Power-Supply Rejection Ratio ($T_A = 25^\circ\text{C}$) ($3.0 \leq V_{CC} \leq 40 \text{ V}$)	PSRR	70	96	—	dB
OUTPUT OPERATIONAL AMPLIFIER					
Input Offset Voltage ($V_{CM} = 2.5 \text{ V}$)	V_{IO}	—	4.0	15	mV
Input Bias Current ($V_{CM} = 2.5 \text{ V}$)	I_{IB}	—	30	200	nA
Input Offset Current ($V_{CM} = 2.5 \text{ V}$)	I_{IO}	—	5.0	75	nA
Voltage Gain + ($T_A = 25^\circ\text{C}$) ($R_L = 2.0 \text{ k}\Omega$ to Gnd, $1.0 \text{ V} \leq V_O \leq 2.5 \text{ V}$)	A_{VOL+}	25	250	—	V/mV
Voltage Gain - ($T_A = 25^\circ\text{C}$) ($R_L = 2.0 \text{ k}\Omega$ to V_{CC} (Op Amp), $1.0 \text{ V} \leq V_O \leq 2.5 \text{ V}$)	A_{VOL-}	25	250	—	V/mV
Common-Mode Voltage Range ($T_A = 25^\circ\text{C}$)	V_{ICR}	0	—	$V_{CC} - 2.0$	V
Common-Mode Rejection Ratio ($T_A = 25^\circ\text{C}$) ($V_{CM} = 0$ to 3.0 V)	CMRR	76	100	—	dB
Power-Supply Rejection Ratio ($T_A = 25^\circ\text{C}$) ($3.0 \text{ V} \leq V_{CC}$ (Op Amp) $\leq 40 \text{ V}$)	PSRR	76	100	—	dB
Output Source Current ($T_A = 25^\circ\text{C}$)	I_{Source}	75	150	—	mA
Output Sink Current ($T_A = 25^\circ\text{C}$)	I_{Sink}	10	35	—	mA
Slew Rate ($T_A = 25^\circ\text{C}$)	SR	—	0.6	—	V/μs
Output Low Voltage ($T_A = 25^\circ\text{C}$, $I_L = -5.0 \text{ mA}$)	V_{OL}	—	—	1.0	V
Output High Voltage ($T_A = 25^\circ\text{C}$, $I_L = 50 \text{ mA}$)	V_{OH}	V_{CC} (Op Amp) - 3.0	—	—	V

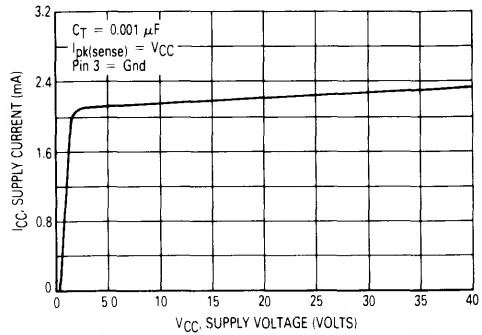
**FIGURE 1 — OUTPUT SWITCH ON/OFF TIME
versus OSCILLATOR TIMING
CAPACITOR**



**FIGURE 3 — EMITTER-FOLLOWER CONFIGURATION
OUTPUT SWITCH SATURATION VOLTAGE
versus EMITTER CURRENT**



**FIGURE 2 — STANDBY SUPPLY CURRENT
versus SUPPLY VOLTAGE**



**FIGURE 4 — COMMON-EMITTER CONFIGURATION
OUTPUT SWITCH SATURATION VOLTAGE
versus COLLECTOR CURRENT**

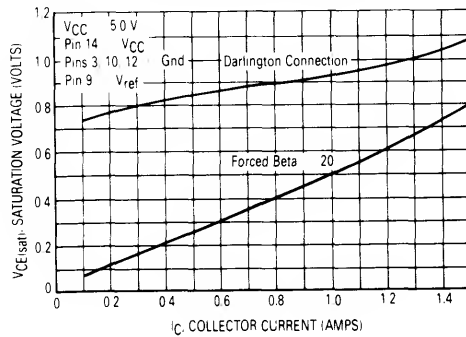


FIGURE 5 — STEP-DOWN CONVERTER

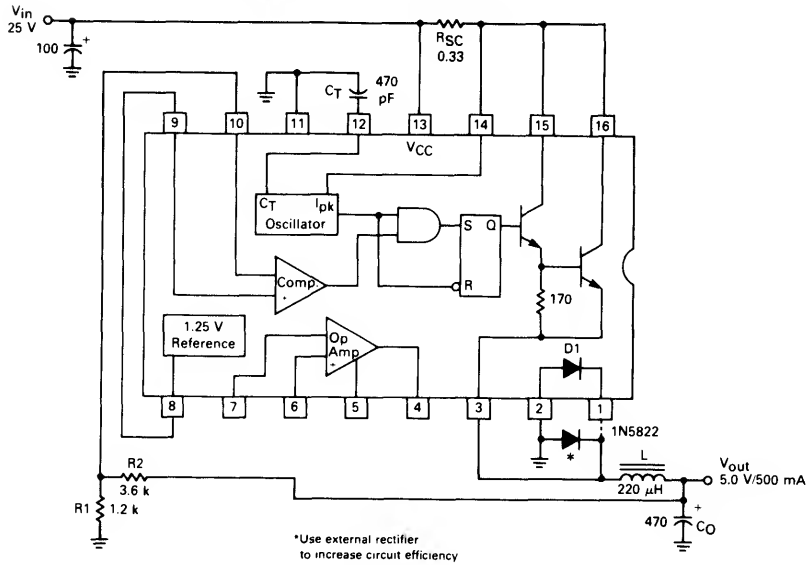


FIGURE 6 — STEP-UP CONVERTER

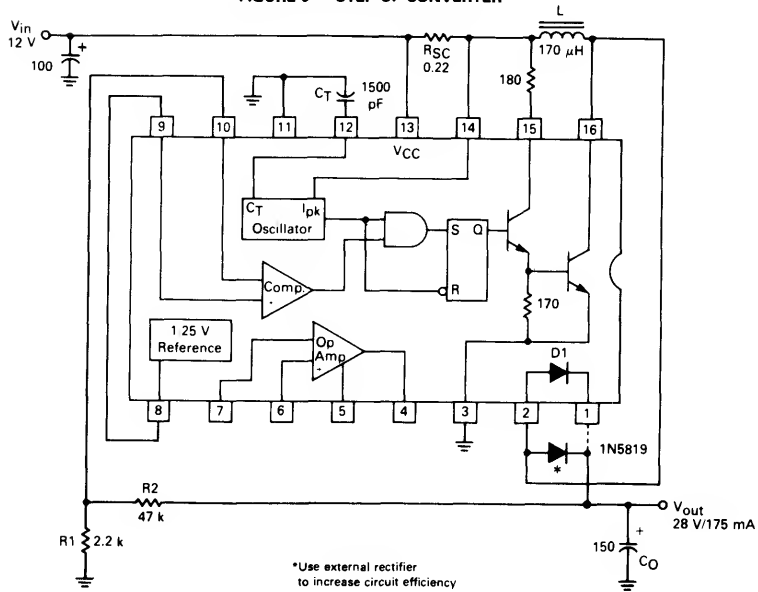


FIGURE 7 — INVERTING CONVERTER

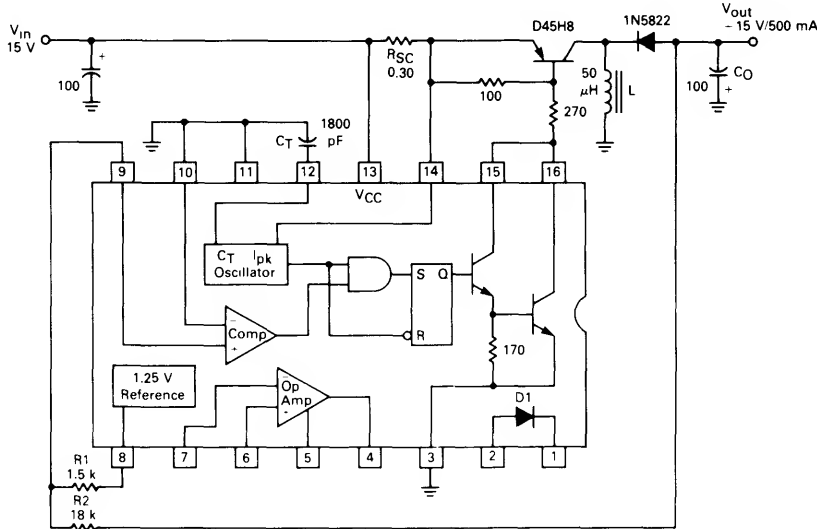


FIGURE 8 — DESIGN FORMULA TABLE

Calculation	Step-Down	Step-Up	Inverting
$\frac{t_{on}}{t_{off}}$	$\frac{V_{out} + V_F}{V_{in(min)} - V_{sat} - V_{out}}$	$\frac{V_{out} - V_F}{V_{in(min)} - V_{sat}}$	$\frac{V_{out} - V_F}{V_{in(min)} - V_{sat}}$
$(t_{on} + t_{off})_{max}$	$\frac{1}{f_{min}}$	$\frac{1}{f_{min}}$	$\frac{1}{f_{min}}$
C_T	$4 \times 10^{-5} t_{on}$	$4 \times 10^{-5} t_{on}$	$4 \times 10^{-5} t_{on}$
$I_{pk(switch)}$	$2 I_{out(max)}$	$2 I_{out(max)} \left(\frac{t_{on} + t_{off}}{t_{off}} \right)$	$2 I_{out(max)} \left(\frac{t_{on} + t_{off}}{t_{off}} \right)$
R_{SC}	$\frac{0.33}{I_{pk(switch)}}$	$\frac{0.33}{I_{pk(switch)}}$	$\frac{0.33}{I_{pk(switch)}}$
$L_{(min)}$	$\left(\frac{V_{in(min)} - V_{sat} - V_{out}}{I_{pk(switch)}} \right) t_{on(max)}$	$\left(\frac{V_{in(min)} - V_{sat}}{I_{pk(switch)}} \right) t_{on(max)}$	$\left(\frac{V_{in(min)} - V_{sat}}{I_{pk(switch)}} \right) t_{on(max)}$
C_O	$\frac{I_{pk(switch)}(t_{on} + t_{off})}{8 \text{ Ripple}(p-p)}$	$\frac{I_{out} t_{on}}{\text{ripple}}$	$\frac{I_{out} t_{on}}{\text{ripple}}$

V_{sat} = Saturation voltage of the output switch V_F = Forward voltage drop of the ringback rectifier

The following power supply characteristics must be chosen:

V_{in} — Nominal input voltage. If this voltage is not constant, then use $V_{in(max)}$ for step-down and $V_{in(min)}$ for step-up and inverting converter.

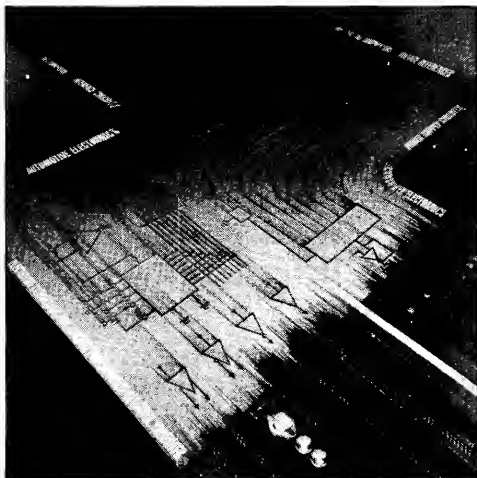
V_{out} — Desired output voltage, $V_{out} = 1.25 \left(1 + \frac{R_2}{R_1} \right)$ for step-down and step-up; $V_{out} = \frac{1.25 R_2}{R_1}$ for Inverting.

I_{out} — Desired output current.

f_{min} — Minimum desired output switching frequency at the selected values for V_{in} and I_O .

$V_{ripple(p-p)}$ — Desired peak-to-peak output ripple voltage. In practice, the calculated value will need to be increased due to the capacitor's equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly effect the line and load regulation.

See Application Note AN920R2 for further information.



In Brief . . .

With the expansion of electronics into more and more mechanical systems there comes an ever increasing demand for simple but intelligent circuits that can blend these two technologies together. In past years, the task of power/motor control was once the domain of discrete devices. But today, increasingly, this task is being performed by bipolar IC technology because of cost, size, and reliability constraints. Motorola offers integrated circuits designed to anticipate the requirements for both simple and sophisticated control systems, while providing cost effective solutions to meet the application.

Power/Motor Control Circuits

Selector Guide

Power Controllers	4-2
Motor Controllers	4-4

Alphanumeric Listing	4-8
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Data Sheets	4-9
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Power/Motor Control Circuits

Power Controllers

An assortment of battery and ac line-operated control ICs for specific applications is shown. They are designed to enhance system performance and reduce complexity in a wide variety of control applications.

Zero Voltage Switches

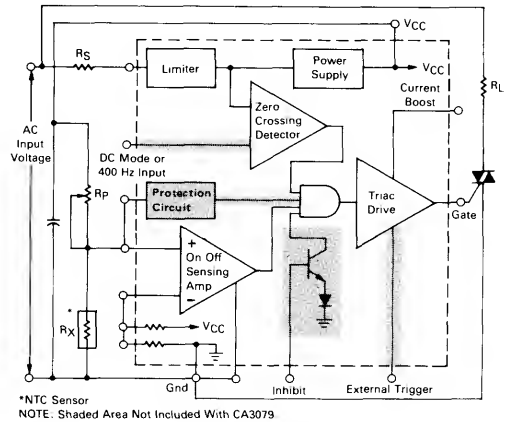
CA3079P/CA3059P

$T_A = -40^\circ$ to $+85^\circ\text{C}$, Case 646

This series is designed for thyristor control in a variety of ac power switching applications for ac input voltages of 24 V, 120 V, 208/230 V, and 227 V @ 50/60 Hz. Features include:

- **Limiters-Power Supply** — Allows operation directly from an ac line.
- **Differential On/Off Sensing Amplifier** — Tests for condition of external sensors or input command signals. Proportional control capability or hysteresis may be implemented.
- **Zero-Crossing Detector** — Synchronizes the output pulses to the zero voltage point of the ac cycle. Eliminates RFI when used with resistive loads.
- **Triac Drive** — Supplies high-current pulses to the external power controlling thyristor.
- **Protection Circuit (CA3059 only)** — A built-in circuit may be actuated, if the sensor opens or shorts, to remove the drive circuit from the external triac.
- **Inhibit Capability (CA3059 only)** — Thyristor firing may be inhibited by the action of an internal diode gate.
- **High Power DC Comparator Operation (CA3059 only)** — Operation in this mode is accomplished by connecting Pin 7 to Pin 12 (thus overriding the action of the zero-crossing detector).

CA3079

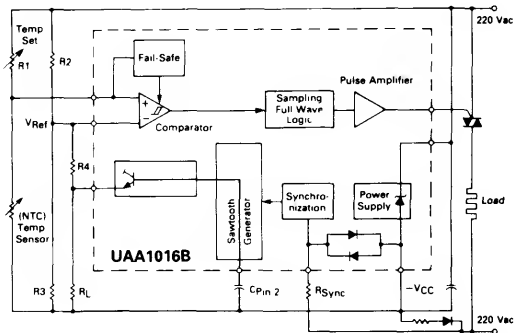


Zero Voltage Controller

UAA1016B — $T_A = -20^\circ$ to $+100^\circ\text{C}$, Case 626

This device is designed to drive triacs with the Zero Voltage technique which allows RFI free power regulation of resistive loads. They provide the following features:

- Proportional Temperature Control Over an Adjustable Band
- Adjustable Burst Frequency (to Comply with Standards)
- Sensor Fail-Safe
- No dc Current Component Through the Main Line (to Comply with Standards)
- Negative Output Current Pulses (Triacs Quadrants 2 and 3)
- Direct ac Line Operation
- Low External Components Count

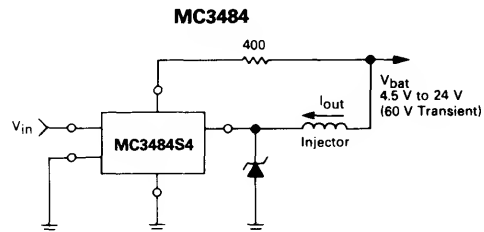


4

Integrated Solenoid Driver

MC3484S2,S4 — $T_J = -40^\circ$ to $+125^\circ\text{C}$, Case 314D

The MC3484 is an integrated monolithic solenoid driver. Its typical function is to apply full battery voltage to fuel injector(s) for rapid current rise, in order to produce positive injector opening. When load current reaches a preset level (4.0 A in MC3484S4 or 2.4 A in MC3484S2) the injector driver reduces the load current by a 4-to-1 ratio and operates as a constant current supply. This condition holds the injector open and reduces system dissipation.

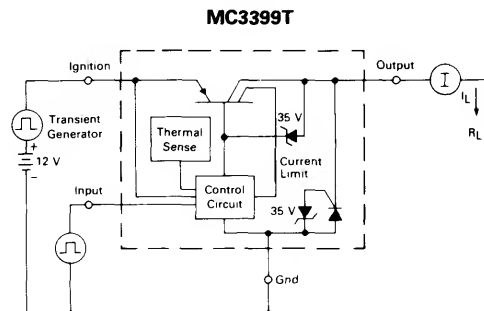


High-Side Driver Switch

MC3399T — $T_J = -40^\circ$ to $+150^\circ\text{C}$, Case 314D

The MC3399T is a High-Side Driver Switch that is designed to drive loads from the positive side of the power supply. The output is controlled by a TTL compatible Enable pin. In the ON state, the device exhibits very low saturation voltages for load currents in excess of 750 mA. The device also protects the load from positive- or negative-going high voltage transients by becoming an open circuit and isolating the transient for its duration from the load.

The MC3399T is fabricated on a power BIMOS process which combines the best features of Bipolar and MOS technologies. The mixed technology provides higher gain PNP output devices and results in Power Integrated Circuits with reduced quiescent current.



Power/Motor Control Circuits

Motor Controllers

This section contains integrated circuits designed for cost effective control of specific motor-families. Included

are controllers for brushless, dc servo, stepper, and universal type motors.

Brushless DC Motor Controllers

Advances in magnetic materials technology and integrated circuits have contributed to the unprecedented rise in popularity of brushless DC motors. Linear control ICs are making the many features and advantages of brushless motors available at a much more economical price. Motorola offers a family of monolithic integrated

brushless DC motor controllers. These ICs provide a choice of control functions which allow many system features to be easily implemented at a fraction of the cost of discrete solutions. The following table summarizes and compares the features of Motorola's brushless motor controllers.

Features Summary For Motorola Brushless DC Motor Controllers

Device	Operating Voltage Range (Volts)		Undervoltage Lockout	Internal Thermal Shutdown	Fwd/Rev Control	Sensor Electrical Phasing	Output Enable	Output Drivers		6.25 V Reference Output	Current Sense Comparator Input(s)	Error Amplifier	FAULT Output	Separate Drive Ground	Separate Drive Vc	Brake Input	Package (Case)
	Vcc	Vc						Totem Pole (Bottom)	Open Collector (Top)								
MC33033P	10–30		X	X	X	60°/300° and 120°/240°	X	X	X	X	Noninv. Only	X					20 Pin Plastic (738)
MC33034P60	10–40	10–40	X	X	X	60°/300°	X	X	X	X	Noninv. Only	X	X	X	X	X	24 Pin Plastic (724)
MC33034P120	10–40	10–40	X	X	X	120°/240°	X	X	X	X	Noninv. Only	X	X	X	X	X	24 Pin Plastic (724)
MC33035P	10–40	10–30	X	X	X	60°/300° and 120°/240°	X	X	X	X	Noninv. and Inv.	X	X		X	X	24 Pin Plastic (724)

MC33034P60,P120 — $T_A = -40^\circ$ to $+85^\circ\text{C}$, Case 724
MC33034DW60,DW120 — $T_A = -40^\circ$ to $+85^\circ\text{C}$,
 Case 751E

The MC33034 Series is a first-generation high performance brushless motor controller containing all of the active functions required to implement a full featured open-loop three or four phase motor control system. These devices consist of a rotor position decoder for proper commutation sequencing, a temperature compensated 6.25 V reference capable of supplying sensor power, frequency programmable sawtooth oscillator, a fully accessible error amplifier, pulse width modulator comparator, three open collector top drivers, and three high current totem pole bottom drivers ideally suited for driving power MOSFETs. Inputs are provided for speed control, forward/reverse, run enable, and dynamic braking functions. Cycle-by-cycle current limiting, undervoltage lockout, and internal thermal shutdown protection are also provided.

MC33035P — $T_A = -40^\circ$ to $+85^\circ\text{C}$, Case 724
MC33035DW — $T_A = -40^\circ$ to $+85^\circ\text{C}$, Case 751E

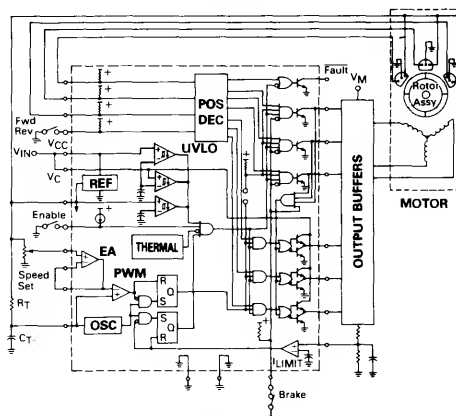
The MC33035 is a second-generation high performance brushless DC motor controller which contains all of the active functions required to implement a full featured open-loop motor control system. While being pin-compatible with its MC33034 predecessor, the MC33035 offers additional features at a lower price. The two additional features provided by the MC33035 are a pin which allows the user to select $60^\circ/300^\circ$ or $120^\circ/240^\circ$ sensor electrical phasings, and access to both inverting and non-inverting inputs of the current sense comparator. The earlier devices had two part numbers which were needed to support the different sensor phasings, and the inverting input to the current sense comparator was internally grounded. All of the control and protection features of the MC33034 are also provided in the newer MC33035.

MC33033P — $T_A = -40^\circ$ to $+85^\circ\text{C}$, Case 738
MC33033DW — $T_A = -40^\circ$ to $+85^\circ\text{C}$, Case 751D

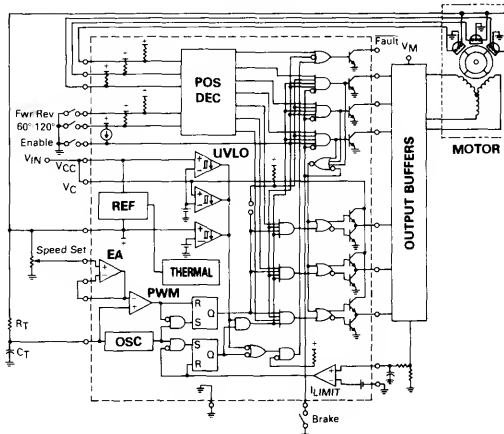
The MC33033 is a lower cost second-generation brushless DC motor controller which has evolved from the full featured MC33034 and MC33035 controllers. The MC33033 contains all of the active functions needed to implement a low cost open-loop motor control system. This IC has all of the key control and protection functions of the two full featured devices with the following secondary features deleted: separate drive-circuit supply and ground pins, the brake input, and the fault output signal. Like its MC33035 predecessor, the MC33033 has a control pin which allows the user to select $60^\circ/300^\circ$ or $120^\circ/240^\circ$ sensor electrical phasings.

Because of its low cost, the MC33033 can efficiently be used to control brush DC motors as well as brushless. A brush DC motor can be driven using two of the three drive output phases provided in the MC33033, while the Hall sensor input pins are selectively tied to V_{REF} or ground. Other features such as forward/reverse, output enable, speed control, current limiting, undervoltage lockout and internal thermal shutdown remain functional in this operating mode.

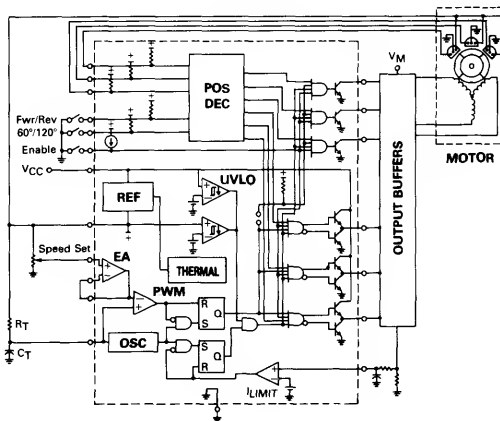
MC33034



MC33035



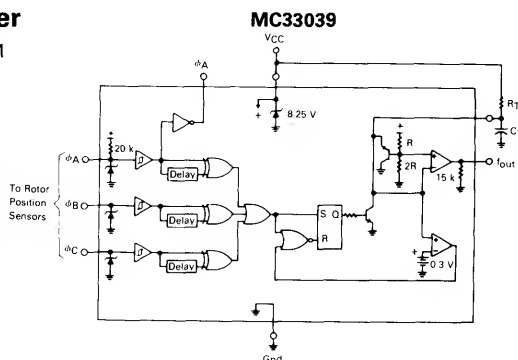
MC33033



Closed-Loop Brushless Motor Adapter

MC33039P,D — $T_A = -40^\circ$ to $+85^\circ\text{C}$, Case 626, 751

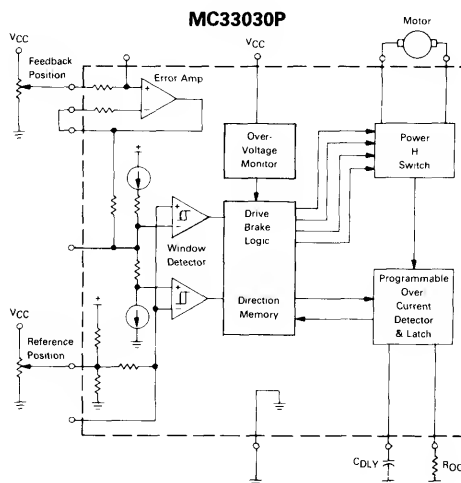
The MC33039P,D is a high performance closed-loop speed control adapter specifically designed for use in brushless dc motor control systems. Implementation will allow precise speed regulation without the need for a magnetic or optical tachometer. These devices contain three input buffers each with hysteresis for noise immunity, three digital edge detectors, a programmable monostable, and an internal shunt regulator. Also included is an inverter output for use in systems that require conversion of sensor phasing. Although this device is primarily intended for use with the MC33033/34/35 brushless motor controllers, it can be used cost effectively in many other closed-loop speed control applications.



DC Servo Motor Controller/Driver

MC33030P — $T_A = -40^\circ$ to $+85^\circ\text{C}$, Case 648C

A monolithic dc servo motor controller providing all active functions necessary for a complete closed loop system. This device consists of an on-chip op amp and window comparator with wide input common-mode range, drive and brake logic with direction memory, power H switch driver capable of 1.0 A, independently programmable over-current monitor and shutdown delay, and over-voltage monitor. This part is ideally suited for almost any servo positioning application that requires sensing of temperature, pressure, light, magnetic flux, or any other means that can be converted to a voltage.

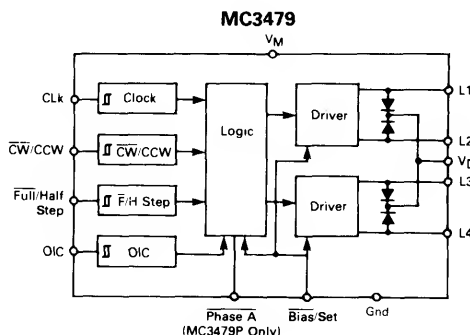


Stepper Motor Drivers

MC3479P — $T_A = 0^\circ$ to $+70^\circ\text{C}$, Case 648C

SAA1042,A — $T_A = 0^\circ$ to $+70^\circ\text{C}$, Case 721

Stepper Motor Drivers provide up to 500 mA of drive per coil for two phase 6.0 V to 24 V stepper motors. Control logic is provided to accept commands for clockwise, counter clockwise and half or full step operation. The MC3479P has an added Output Impedance Control (OIC) and a Phase A drive state indicator (not available on SAA1042 devices).



Universal Motor Speed Controllers

TDA1085A $T_A = 0^\circ \text{ to } +70^\circ\text{C}$, Case 648

This device contains all the necessary functions for the speed control of universal (ac/dc) motors in an open or closed loop configuration. Facility for defining the initial speed/time characteristic. The circuits provide a phase angle varied trigger pulse to the motor control triac.

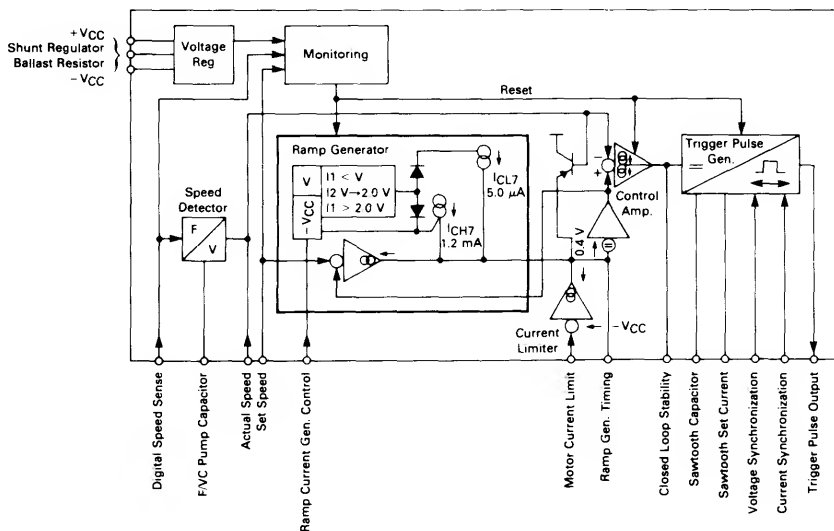
- Guaranteed Full Wave Triac Drive
- Soft Start from Power-up
- On-Chip Frequency/Voltage Converter and Ramp Generator
- Current Limiting Incorporated
- Direct Drive from ac Line

TDA1085C $T_A = -10^\circ \text{ to } +120^\circ\text{C}$, Case 648

Similar to TDA1085A, but designed for commercial washing machine service.

4

TDA1085A



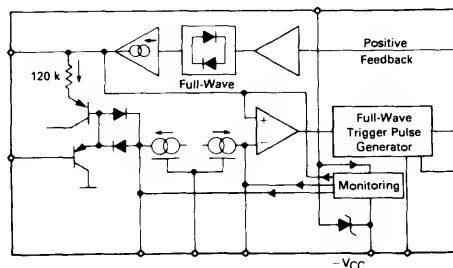
Triac Phase Angle Controller

TDA1185A $T_A = 0^\circ \text{ to } +70^\circ\text{C}$, Case 646

This device generates controlled triac triggering pulses and allows tacholeless speed stabilization of universal motors by an integrated positive feedback function.

- Low Cost External Components Count
- Optimum Triac Firing (2nd and 3rd Quadrants)
- Repetitive Trigger Pulses When Triac Current is Interrupted by Motor Brush Bounce
- Triac Current Sensed to Allow Inductive Loads
- Soft Start
- Power Failure Detection and General Circuit Reset
- Low Power Consumption: 1.0 mA

TDA1185A



POWER CONTROLLERS

Device	Function	Page
CA3059	Zero Voltage Switch	4-9
CA3079	Zero Voltage Switch	4-9
MC3399T	High Side Driver Switch	See Chapter 10
MC3484S2,S4	Integrated Solenoid Driver	See Chapter 10
UAA1016B	Zero Voltage Controller	4-134
UAA2016	Zero Voltage Switch Power Controller	4-140

MOTOR CONTROLLERS

Device	Function	Page
MC33030	DC Servo Motor Controller/Driver	4-22
MC33033	Brushless DC Motor Controller	4-35
MC33034	DC Brushless Motor Controller	4-56
MC33035	Brushless DC Motor Controller	4-76
MC33039	Closed Loop Brushless Motor Adapter	4-98
MC3479P	Stepper Motor Driver	4-14
SAA1042,A	Stepper Motor Driver	4-103
TDA1085A	Universal Motor Speed Controller	4-108
TDA1085C	Universal Motor Speed Controller	4-115
TDA1185A	TRIAC Phase Angle Controller	4-125

CA3059
CA3079

ZERO VOLTAGE SWITCHES

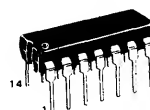
This series is designed for thyristor control in a variety of ac power switching applications for ac input voltages of 24 V, 120 V, 208/230 V, and 277 V @ 50/60 Hz.

Applications:

- Relay Control
- Valve Control
- Synchronous Switching of Flashing Lights
- On-Off Motor Switching
- Differential Comparator With Self-Contained Power Supply for Industrial Applications
- Photosensitive Control
- Heater Control
- Lamp Control
- Power One-Shot Control

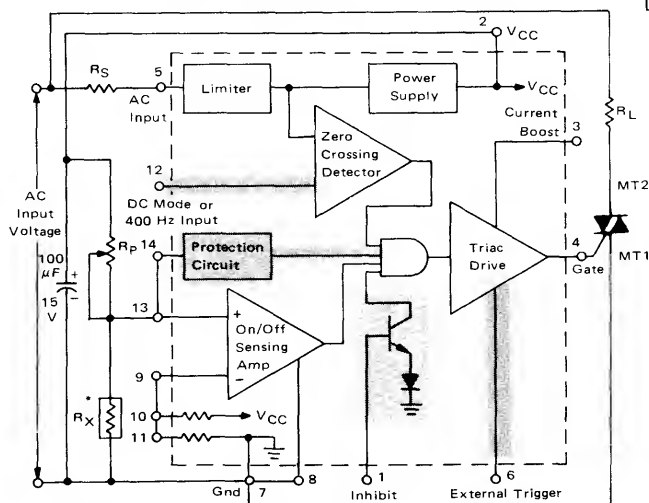
ZERO VOLTAGE SWITCHES

**SILICON MONOLITHIC
INTEGRATED CIRCUITS**



PLASTIC PACKAGE
CASE 646

FIGURE 1 — FUNCTIONAL BLOCK DIAGRAM



*NTC Sensor

NOTE: Shaded Area Not Included With CA3079.

**FUNCTIONAL BLOCK
DESCRIPTION**

1. **Limiter-Power Supply** — Allows operation of the CA3059/79 directly from an ac line. Suggested dropping resistor (R_S) values are given in the table below.
2. **Differential On/Off Sensing Amplifier** — Tests for condition of external sensors or input command signals. Proportional control capability or hysteresis may be implemented using this block.
3. **Zero-Crossing Detector** — Synchronizes the output pulses to the zero voltage point of the ac cycle. This synchronization eliminates RFI when used with resistive loads.
4. **Triac Drive** — Supplies high-current pulses to the external power controlling thyristor.
5. **Protection Circuit (CA3059 only)** — A built-in circuit may be actuated, if the sensor opens or shorts, to remove the drive current from the external triac.
6. **Inhibit Capability (CA3059 only)** — Thyristor firing may be inhibited by the action of an internal diode gate at Pin 1.
7. **High Power DC Comparator Operation (CA3059 only)** — Operation in this mode is accomplished by connecting Pin 7 to Pin 12 (thus overriding the action of the zero-crossing detector). When Pin 13 is positive with respect to Pin 9, current to the thyristor is continuous.

AC Input Voltage (50/60 Hz)	Input Series Resistor (R_S)	Dissipation Rating for R_S
vac	k Ω	W
24	2.0	0.5
120	10	2.0
208/230	20	4.0
277	25	5.0

CA3059, CA3079

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage (Between Pins 2 and 7) CA3059 CA3079	V _{CC}	12 10	Vdc
DC Supply Voltage (Between Pins 2 and 8) CA3059 CA3079	V _{CC}	12 10	Vdc
Peak Supply Current (Pins 5 and 7)	I _{S,7}	± 50	mA
Fail-Safe Input Current (Pin 14)	I _{I4}	2.0	mA
Output Pulse Current (Pin 4) (Note 1)	I _{out}	150	mA
Junction Temperature	T _J	150	°C
Operating Temperature Range	T _A	−40 to +85	°C
Storage Temperature Range	T _{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (Operation @ 120 Vrms, 50–60 Hz, T_A = 25°C, [Note 2])

Characteristic	Test Circuits	Symbol	Min	Typ	Max	Unit
DC Supply Voltage Inhibit Mode R _S = 10 k, I _L = 0 R _S = 5.0 k, I _L = 2.0 mA Pulse Mode R _S = 10 k, I _L = 0 R _S = 5.0 k, R _L = 2.0 mA	Fig. 2	V _S	6.1 —	6.5 6.1	7.0 —	Vdc
Gate Trigger Current (V _{GT} = 1.0 V, Pins 3 and 2 connected)	Fig. 3	I _{GT}	—	160	—	mA
Peak Output Current, Pulsed With Internal Power Supply, V _{GT} = 0 Pin 3 Open Pins 3 and 2 Connected With External Power Supply, V _{CC} = 12 V, V _{GT} = 0 Pin 3 Open Pins 3 and 2 Connected	Fig. 3 Fig. 4	I _{OM}	50 90 — —	125 190 230 300	— — — —	mA
Inhibit Input Ratio (Ratio of Voltage @ Pin 9 to Pin 2)	Fig. 5	V _g /V ₂	0.465	0.485	0.520	—
Total Gate Pulse Duration (C _{Ext} = 0) Positive dv/dt Negative dv/dt	Fig. 6	t _p t _n	70 70	100 100	140 140	μs
Pulse Duration After Zero Crossing (C _{Ext} = 0, R _{Ext} = ∞) Positive dv/dt Negative dv/dt	Fig. 6	t _{p1} t _{n1}	— —	50 60	— —	μs
Output Leakage Current Inhibit Mode (Note 3)	Fig. 3	I _l	—	0.001	10	μA
Input Bias Current CA3059 CA3079	Fig. 7	I _{IB}	— —	0.15 0.15	1.0 2.0	μA
Common Mode Input Voltage Range (Pins 9 and 13 Connected)	—	V _{CMR}	—	1.4 to 5.0	—	Vdc
Inhibit Input Voltage CA3059 only	Fig. 8	V _I	—	1.4	1.6	Vdc
External Trigger Voltage CA3059 only	—	V ₆ –V ₄	—	1.4	—	Vdc

- NOTES:**
- Care must be taken, especially when using an external power supply, that total package dissipation is not exceeded.
 - The values given in the Electrical Characteristics Chart at 120 V also apply for operation at input voltages of 24 V, 208/230 V, and 277 V, except for Pulse Duration test. However, the series resistor (R_S) must have the indicated value, shown in Table A for the specified input voltage.
 - I_l out of Pin 4, 2.0 V on Pin 1, S1 position 2.

TEST CIRCUITS

(All resistor values are in ohms)

FIGURE 2 – DC SUPPLY VOLTAGE

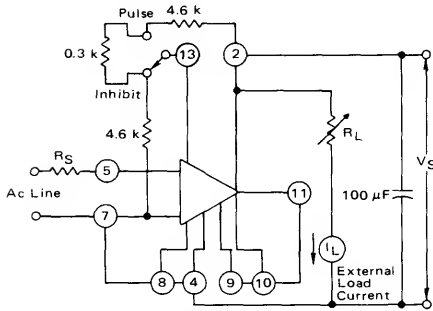


FIGURE 4 – PEAK OUTPUT CURRENT (PULSED) WITH EXTERNAL POWER SUPPLY

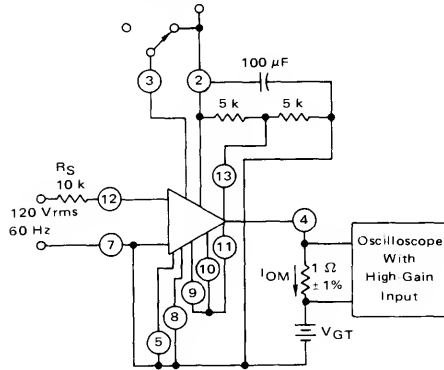


FIGURE 6 – GATE PULSE DURATION TEST CIRCUIT WITH ASSOCIATED WAVEFORM

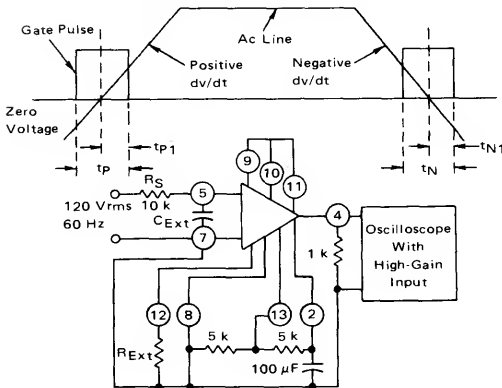


FIGURE 3 – PEAK OUTPUT (PULSED) AND GATE TRIGGER CURRENT WITH INTERNAL POWER SUPPLY

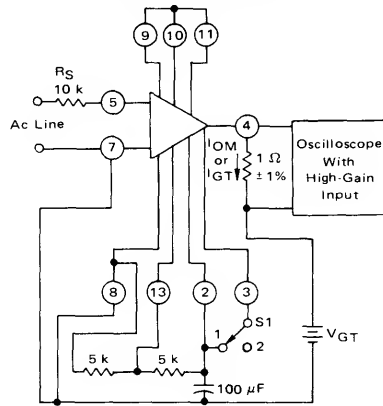


FIGURE 5 – INPUT INHIBIT RATIO

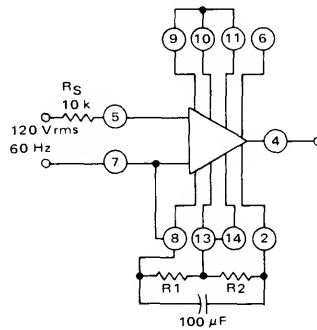
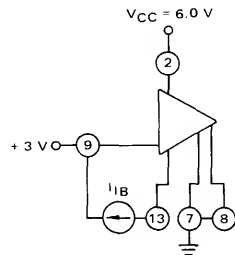
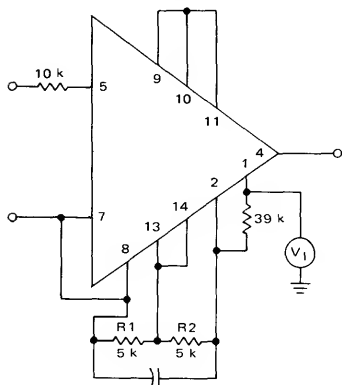
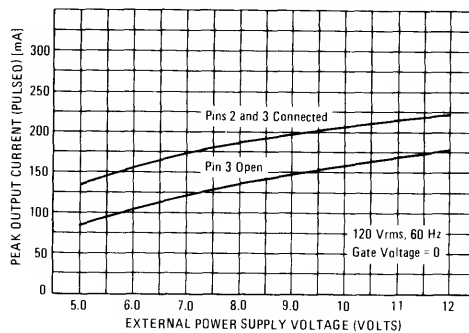
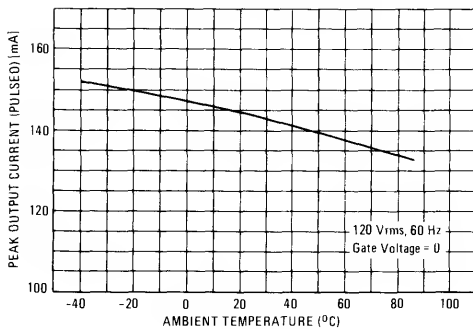
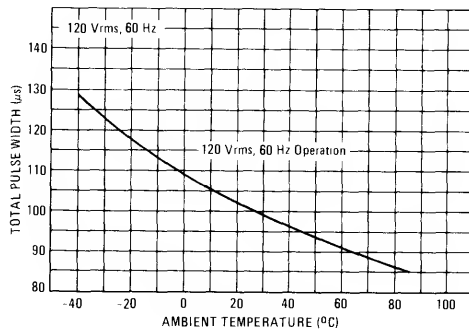
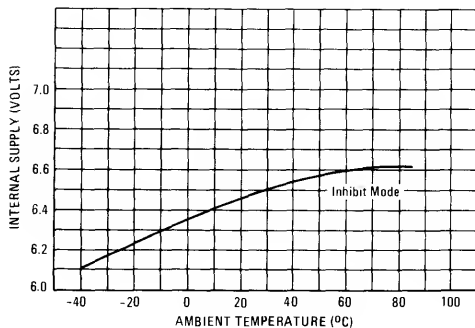
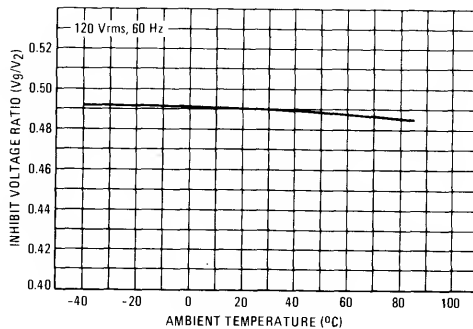


FIGURE 7 – INPUT BIAS CURRENT TEST CIRCUIT



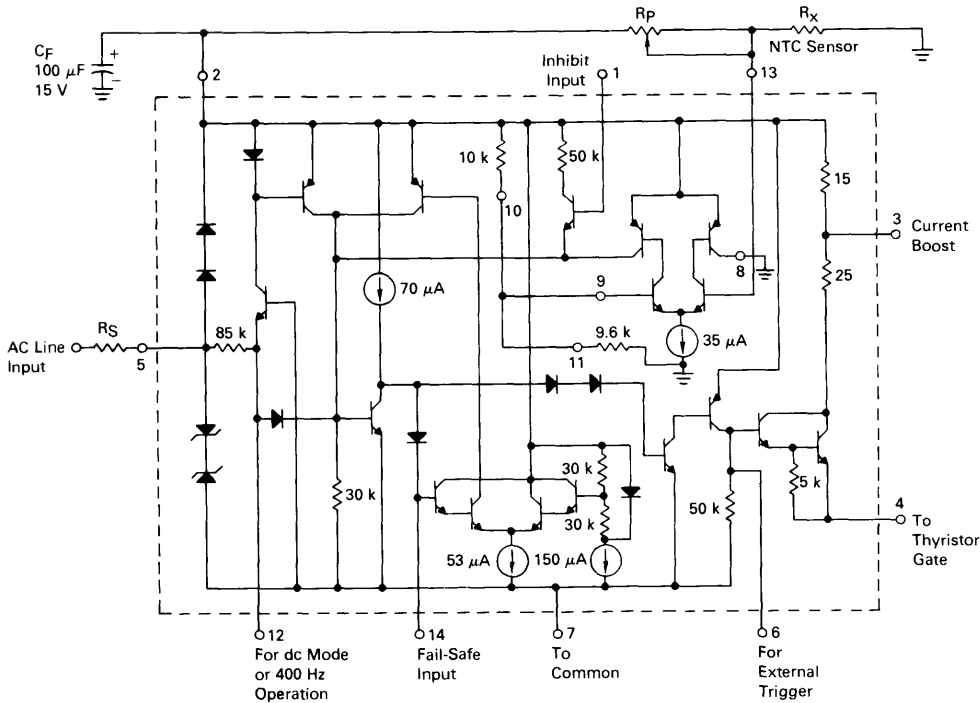
TYPICAL CHARACTERISTICS

FIGURE 8 — INHIBIT INPUT VOLTAGE TEST

FIGURE 9 — PEAK OUTPUT CURRENT (PULSED)
versus EXTERNAL POWER SUPPLY VOLTAGEFIGURE 10 — PEAK OUTPUT CURRENT (PULSED)
versus AMBIENT TEMPERATUREFIGURE 11 — TOTAL PULSE WIDTH versus
AMBIENT TEMPERATUREFIGURE 12 — INTERNAL SUPPLY versus
AMBIENT TEMPERATUREFIGURE 13 — INHIBIT VOLTAGE RATIO
versus AMBIENT TEMPERATURE

CA3059, CA3079

FIGURE 14 — CIRCUIT SCHEMATIC



NOTE: Current sources are established by an internal reference.

Pins 1, 6, 12, and 14 are not used with CA3079.

APPLICATION INFORMATION

Power Supply

The CA3059 and CA3079 are self-powered circuits, powered from the ac line through an appropriate dropping resistor (see Table A). The internal supply is designed to power the auxiliary power circuits.

In applications where more output current from the internal supply is required, an external power supply of higher voltage should be used. To use an external power supply, connect pin 5 and pin 7 together and apply the synchronizing voltage to pin 12 and the dc supply voltage to pin 2 as shown in Figure 4.

Operation of Protection Circuit (CA3059 Only)

The protection circuit, when connected, will remove current drive from the triac if an open or shorted sensor is detected. This circuit is activated by connecting pin 13 to pin 14 (see Figure 1).

The following conditions should be observed when the protection circuit is utilized:

- The internal supply should be used and the external load current must be limited to 2 mA with a 5 k Ω dropping resistor.

- Sensor Resistance (R_X) and R_p values should be between 2 k Ω and 100 k Ω .

- The relationship $0.33 < R_X/R_p < 3$ must be met over the anticipated temperature range to prevent undesired activation of the circuit. A shunt or series resistor may have to be added.

External Inhibit Function (CA3059 Only)

A priority inhibit command applied to pin 1 will remove current drive from the thyristor. A command of at least +1.2 V @ 10 μ A is required. A DTL or T²L logic 1 applied to pin 1 will activate the inhibit function.

DC Gate Current Mode (CA3059 Only)

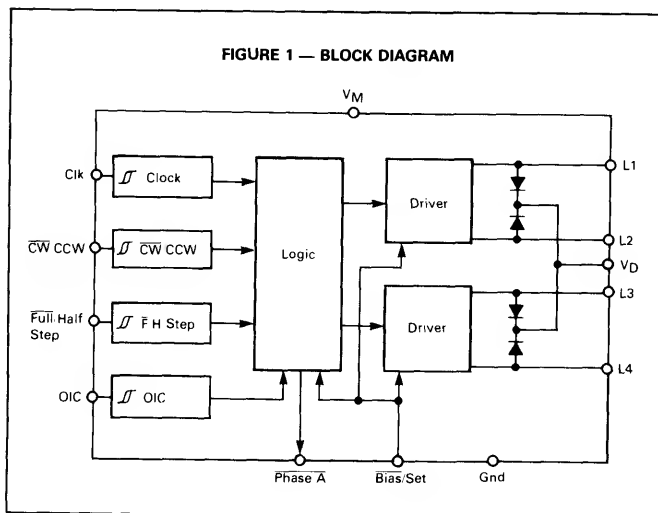
When comparator operation is desired or inductive loads are being switched, pins 7 and 12 should be connected. This connection disables the zero-crossing detector to permit the flow of gate current from the differential sensing amplifier on demand. Care should be exercised to avoid possible overloading of the internal power supply when operating the device in this mode. A resistor should be inserted between pin 4 and the thyristor gate in order to limit the current.

STEPPER MOTOR DRIVER

The MC3479 is designed to drive a two-phase stepper motor in the bipolar mode. The circuit consists of four input sections, a logic decoding/sequencing section, two driver-stages for the motor coils, and an output to indicate the Phase A drive state.

- Single Supply Operation — +7.2 to +16.5 Volts
- 350 mA/Coil Drive Capability
- Clamp Diodes Provided for Back-EMF Suppression
- Selectable CW/CCW and Full/Half Step Operation
- Selectable High/Low Output Impedance (Half Step Mode)
- TTL/CMOS Compatible Inputs
- Input Hysteresis — 400 mV Minimum
- Phase Logic Can Be Initialized to Phase A
- Phase A Output Drive State Indication (Open-Collector)
- Available in Standard DIP and Surface Mount

FIGURE 1 — BLOCK DIAGRAM



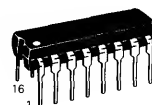
ORDERING INFORMATION

Device	Operating Junction Temperature Range	Package
MC3479P	-65° to +150°C	Plastic
MC3479FN		Plastic

MC3479

STEPPER MOTOR DRIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT

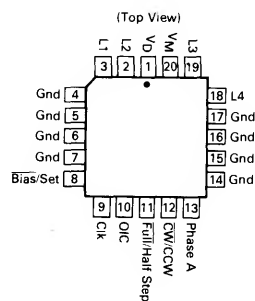
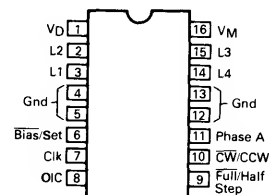


P SUFFIX
PLASTIC PACKAGE
CASE 648C



FN SUFFIX
PLASTIC PACKAGE
CASE 775
(PLCC 20)

PIN ASSIGNMENTS



INPUT TRUTH TABLE

	Input Low	Input High
CW/CCW	CW	CCW
Full/Half Step	Full Step	Half Step
OIC	Hi Z	Low Z
Clk	Positive Edge Triggered	

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_M	+18	Vdc
Clamp Diode Cathode Voltage (Pin 1)	V_D	$V_M + 5.0$	Vdc
Driver Output Voltage	V_{OD}	$V_M + 6.0$	Vdc
Drive Output Current/Coil	I_{OD}	± 500	mA
Input Voltage (Logic Controls)	V_{in}	-0.5 to +7.0	Vdc
Bias/Set Current	I_{BS}	-10	mA
Phase A Output Voltage	V_{OA}	+18	Vdc
Phase A Sink Current	I_{OA}	20	mA
Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Max	Unit
Supply Voltage	V_M	+7.2	+16.5	Vdc
Clamp Diode Cathode Voltage	V_D	V_M	$V_M + 4.5$	Vdc
Driver Output Current (Per Coil) (Note 5)	I_{OD}	—	350	mA
Input Voltage (Logic Controls)	V_{in}	0	+5.5	Vdc
Bias/Set Current (Outputs Active)	I_{BS}	-300	-75	μA
Phase A Output Voltage	V_{OA}	—	V_M	Vdc
Phase A Sink Current	I_{OA}	0	8.0	mA
Operating Ambient Temperature	T_A	0	+70	°C

NOTE:

5. See section on Power Dissipation in Application Information.

DC ELECTRICAL CHARACTERISTICS *(Pin numbers refer to the DIP Package)

(Specifications apply over the recommended supply voltage and temperature ranges unless otherwise noted.) (See Notes 1, 2)

Characteristic	*Pins	Symbol	Min	Typ	Max	Unit
INPUT LOGIC LEVELS						
Threshold Voltage (Low-to-High)	7, 8, 9, 10	V_{TLH}	—	—	2.0	Vdc
Threshold Voltage (High-to-Low)		V_{THL}	0.8	—	—	Vdc
Hysteresis		V_{HYS}	0.4	—	—	Vdc
Current ($V_I = 0.4$ V) ($V_I = 5.5$ V) ($V_I = 2.7$ V)		I_{IL} I_{IH1} I_{IH2}	-100 — —	— — —	— +100 +20	μA

DRIVER OUTPUT LEVELS

Output High Voltage ($I_{BS} = -300 \mu A$) ($I_{OD} = -350$ mA) ($I_{OD} = -0.1$ mA)	2, 3, 14, 15	V_{OHD}	$V_M - 2.0$ $V_M - 1.2$	— —	— —	Vdc
Output Low Voltage ($I_{BS} = -300 \mu A$, $I_{OD} = 350$ mA)		V_{OLD}	—	—	0.8	Vdc
Differential Mode Output Voltage Difference (Note 3) ($I_{BS} = -300 \mu A$, $I_{OD} = 350$ mA)		DV_{OD}	—	—	0.15	Vdc
Common Mode Output Voltage Difference (Note 4) ($I_{BS} = -300 \mu A$, $I_{OD} = -0.1$ mA)		CV_{OD}	—	—	0.15	Vdc
Output Leakage — Hi Z State ($0 \leq V_{OD} \leq V_M$, $I_{BS} = -5.0 \mu A$) ($0 \leq V_{OD} \leq V_M$, $I_{BS} = -300 \mu A$, F/H = 2.0 V, OIC = 0.8 V)		I_{OZ1} I_{OZ2}	-100 -100	— —	+100 +100	μA

NOTES:

- Algebraic convention rather than absolute values is used to designate limit values.
- Current into a pin is designated as positive. Current out of a pin is designated as negative.
- $DV_{OD} = |V_{OD1,2} - V_{OD3,4}|$ where: $V_{OD1,2} = (V_{OHD1} - V_{OLD2})$ or $(V_{OHD2} - V_{OLD1})$, and $V_{OD3,4} = (V_{OHD3} - V_{OLD4})$ or $(V_{OHD4} - V_{OLD3})$.
- $CV_{OD} = |V_{OHD1} - V_{OHD2}|$ or $|V_{OHD3} - V_{OHD4}|$.

DC ELECTRICAL CHARACTERISTICS (continued) *(Pin numbers refer to the DIP Package)

(Specifications apply over the recommended supply voltage and temperature ranges unless otherwise noted.) (See Notes 1, 2)

Characteristic	*Pins	Symbol	Min	Typ	Max	Unit
CLAMP DIODES						
Forward Voltage ($I_D = 350 \text{ mA}$)	1, 2, 3, 14, 15	V_{DF}	—	2.5	3.0	Vdc
Leakage Current (Per Diode) (Pin 1 = 21 V; Outputs = 0 V; $I_{BS} = 0 \mu\text{A}$)		I_{DR}	—	—	100	μA

PHASE A OUTPUT

Output Low Voltage ($I_{OA} = 8.0 \text{ mA}$)	11	V_{OLA}	—	—	0.4	Vdc
Off State Leakage Current ($V_{OHA} = 16.5 \text{ V}$)		I_{OHA}	—	—	100	μA

POWER SUPPLY

Power Supply Current ($I_{OD} = 0 \mu\text{A}$, $I_{BS} = -300 \mu\text{A}$) ($L1 = V_{OHD}$, $L2 = V_{OLD}$, $L3 = V_{OHD}$, $L4 = V_{OLD}$) ($L1 = V_{OHD}$, $L2 = V_{OLD}$, $L3 = Hi Z$, $L4 = Hi Z$) ($L1 = V_{OHD}$, $L2 = V_{OLD}$, $L3 = V_{OHD}$, $L4 = V_{OHD}$)	16	I_{MW} I_{MZ} I_{MN}	— — —	— — —	70 40 75	mA
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BIAS/SET CURRENT

To Set Phase A	6	I_{BS}	-5.0	—	—	μA
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PACKAGE THERMAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Thermal Resistance, Junction to Ambient — No Heatsink	$R_{\theta JA}$	—	45	—	$^{\circ}\text{C/W}$

AC SWITCHING CHARACTERISTICS ($T_A = +25^{\circ}\text{C}$, $V_M = 12 \text{ V}$) (See Figures 2, 3, 4)

Characteristic	*Pins	Symbol	Min	Typ	Max	Unit
Clock Frequency	7	f_{CK}	0	—	50	kHz
Clock Pulse Width — High	7	PW_{CKH}	10	—	—	μs
Clock Pulse Width — Low	7	PW_{CKL}	10	—	—	μs
Bias/Set Pulse Width	6	PW_{BS}	10	—	—	μs
Setup Time — CW/CCW and F/HS	10-7 9-7	t_{su}	5.0	—	—	μs
Hold Time — CW/CCW and F/HS	10-7 9-7	t_h	10	—	—	μs
Propagation Delay — Clk-to-Driver Output		t_{PCD}	—	8.0	—	μs
Propagation Delay — Bias/Set-to-Driver Output		t_{PBSD}	—	1.0	—	μs
Propagation Delay — Clk-to-Phase A Low	7-11	t_{PLA}	—	12	—	μs
Propagation Delay — Clk-to-Phase A High	7-11	t_{PLHA}	—	5.0	—	μs

NOTES:

- Algebraic convention rather than absolute values is used to designate limit values.
- Current into a pin is designated as positive. Current out of a pin is designated as negative.

MC3479

FIGURE 2 — AC TEST CIRCUIT

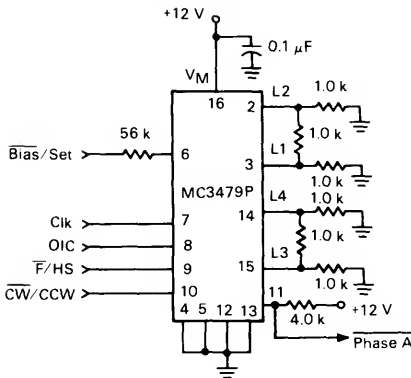
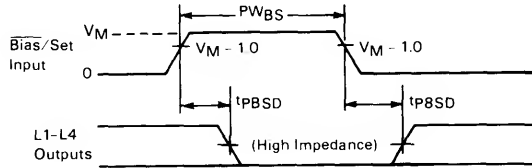


FIGURE 3 — $\overline{\text{BIAS}}/\text{SET}$ TIMING (Refer to Figure 2)



Note: t_r , t_f (10% - 90%) for input signals are ≤ 25 ns

PIN DESCRIPTION

Name	Symbol	Pin #		Description
		FN	DIP	
Power Supply	V_M	20	16	Power supply pin for both the logic circuit and the motor coil current. Voltage range is +7.2 to +16.5 volts.
Ground	Gnd	4, 5, 6, 7, 14, 15, 16, 17	4, 5, 12, 13	Ground pins for the logic circuit and the motor coil current. The physical configuration of the pins aids in dissipating heat from within the IC package.
Clamp Diode Voltage	V_D	1	1	This pin is used to protect the outputs where large voltage spikes may occur as the motor coils are switched. Typically a diode is connected between this pin and Pin 16. See Figure 11.
Driver Outputs	L1, L2 L3, L4	2, 3, 18, 19	2, 3, 14, 15	High current outputs for the motor coils. L1 and L2 are connected to one coil, and L3 and L4 to the other coil.
Bias/Set	\overline{B}/S	8	6	This pin is typically 0.7 volts below V_M . The current out of this pin (through a resistor to ground) determines the maximum output sink current. If the pin is opened ($I_{BS} < 5.0 \mu A$) the outputs assume a high impedance condition, while the internal logic presets to a Phase A condition.
Clock	Clk	9	7	The positive edge of the clock input switches the outputs to the next position. This input has no effect if Pin 6 is open.
Full/Half Step	\overline{F}/HS	11	9	When low (Logic "0"), each clock pulse will cause the motor to rotate one full step. When high, each clock pulse will cause the motor to rotate one-half step. See Figure 7 for sequence.
Clockwise/ Counterclockwise	\overline{CW}/CCW	12	10	This input allows reversing the rotation of the motor. See Figure 7 for sequence.
Output Impedance Control	OIC	10	8	This input is relevant only in the half step mode (Pin 9 > 2.0 V). When low (Logic "0") the two driver outputs of the non-energized coil will be in a high impedance condition. When high the same driver outputs will be at a low impedance referenced to V_M . See Figure 7.
Phase A	Ph A	13	11	This open-collector output indicates (when low) that the driver outputs are in the Phase A condition ($L1 = L3 = VOHD$, $L2 = L4 = VOLD$).

APPLICATION INFORMATION

GENERAL

The MC3479 integrated circuit is designed to drive a stepper positioning motor in applications such as disk drives and robotics. The outputs can provide up to 350 mA to each of two coils of a two-phase motor. The outputs change state with each low-to-high transition of the clock input, with the new output state depending on the previous state, as well as the input conditions at the logic controls.

OUTPUTS

The outputs (L1-L4) are high current outputs (see Figure 5), which when connected to a two-phase motor, provide two full-bridge configurations (L3 and L4 are not shown in Figure 5). The polarities applied to the motor coils depend on which transistor (Q_H or Q_L) of each output is on, which in turn depends on the inputs and the decoding circuitry.

MC3479

FIGURE 4 — CLOCK TIMING (Refer to Figure 2)

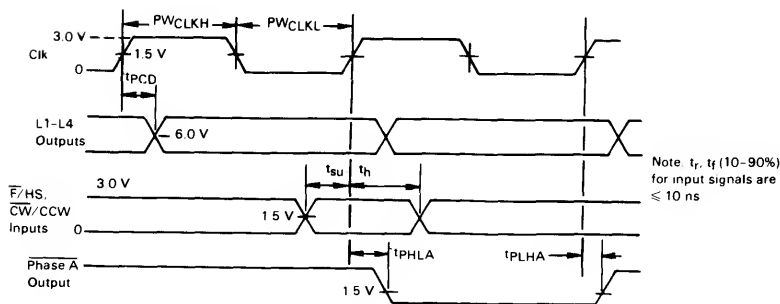
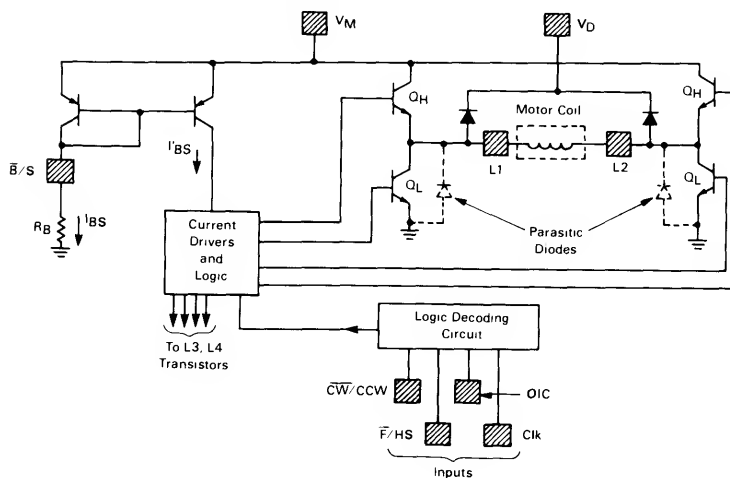


FIGURE 5 — OUTPUT STAGES

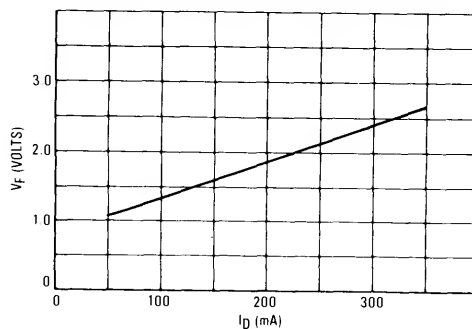


The maximum sink current available at the outputs is a function of the resistor connected between Pin 6 and ground (see section on Bias/Set operation). Whenever the outputs are to be in a high impedance state, both transistors (Q_H and Q_L of Figure 5) of each output are off.

V_D

This pin allows for provision of a current path for the motor coil current during switching, in order to suppress back-EMF voltage spikes. V_D is normally connected to V_M (Pin 16) through a diode (zener or regular), a resistor, or directly. The peaks instantaneous voltage at the outputs must not exceed V_M by more than 6.0 volts. The voltage drop across the internal clamping diodes must be included in this portion of the design (see Figure 6). Note the parasitic diodes (Figure 5) across each Q_L of each output provide for a complete circuit path for the switched current.

FIGURE 6 — CLAMP DIODE CHARACTERISTICS



FULL/HALF STEP

When this input is at a Logic "0" (<0.8 volts), the outputs change a full step with each clock cycle, with the sequence direction depending on the CW/CCW input. There are four steps (Phase A, B, C, D) for each complete cycle of the sequencing logic. Current flows through both motor coils during each step, as shown in Figure 7.

When taken to a Logic "1" (>2.0 volts), the outputs change a half step with each clock cycle, with the sequence direction depending on the CW/CCW input. Eight steps (Phase A-H) result for each complete cycle of the sequencing logic. Phase A, C, E and G correspond (in polarity) to Phase A, B, C, and D, respectively, of the full step sequence. Phase B, D, F and H provide current to one motor coil, while de-energizing the other coil. The condition of the outputs of the de-energized coil depends on the OIC input. See Figure 7 for timing diagram.

OIC

The output impedance control input determines the output impedance to the de-energized coil when operating in the half-step mode. When the outputs are in

Phase B, D, F or H (Figure 7) and this input is at a Logic "0" (<0.8 V), the two outputs to the de-energized coil are in a high impedance condition — Q_L and Q_H of both outputs (Figure 5) are off. When this input is at a Logic "1" (>2.0 V), a low impedance output is provided to the de-energized coil as both outputs have Q_H on (Q_L off). To complete the low impedance path requires connecting V_D to V_M as described elsewhere in this data sheet.

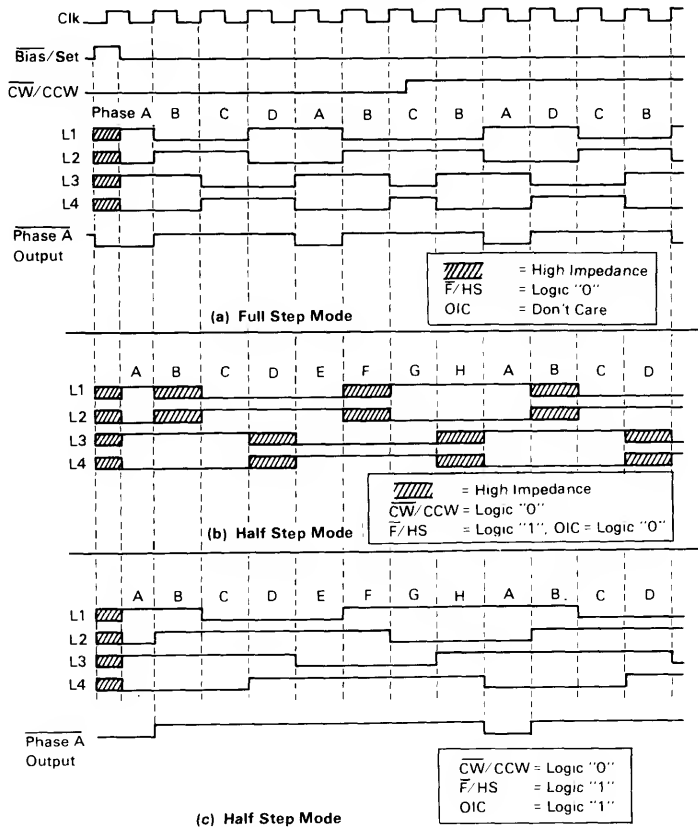
BIAS/SET

This pin can be used for three functions:
a) determining the maximum output sink current;
b) setting the internal logic to a known state; and
c) reducing power consumption.

a) The maximum output sink current is determined by the base drive current supplied to the lower transistors (Q_L s of Figure 5) of each output, which in turn, is a function of I_{BS} . The appropriate value of I_{BS} is determined by:

$$I_{BS} = I_{OD} \times 0.86$$

where I_{BS} is in microamps, and I_{OD} is the motor current/coil in milliamps.

FIGURE 7 — OUTPUT SEQUENCE

The value of R_B (between this pin and ground) is then determined by:

$$R_B = \frac{V_M - 0.7 \text{ V}}{I_{BS}}$$

b) When this pin is opened (raised to V_M) such that I_{BS} is $< 5.0 \mu\text{A}$, the internal logic is set to the Phase A condition, and the four driver outputs are put into a high impedance state. The Phase A output (Pin 11) goes active (low), and input signals at the controls are ignored during this time. Upon re-establishing I_{BS} , the driver outputs become active, and will be in the Phase A position ($L1 = L3 = V_{OHD}$, $L2 = L4 = V_{OLD}$). The circuit will then respond to the inputs at the controls.

The Set function (opening this pin) can be used as a power-up reset while supply voltages are settling. A CMOS logic gate (powered by V_M) can be used to control this pin as shown in Figure 11.

c) Whenever the motor is not being stepped, power dissipation in the IC and in the motor may be lowered by reducing I_{BS} , so as to reduce the output (motor) current. Setting I_{BS} to $75 \mu\text{A}$ will reduce the motor current, but will not reset the internal logic as described above. See Figure 12 for a suggested circuit.

POWER DISSIPATION

The power dissipated by the MC3479 must be such that the junction temperature (T_J) does not exceed 150°C . The power dissipated can be expressed as:

$$P = (V_M \times I_M) + (2 \times I_{OD}) (V_M - V_{OHD}) + V_{OLD}$$

where V_M = Supply voltage;

I_M = Supply current other than I_{OD} ;

I_{OD} = Output current to each motor coil;

V_{OHD} = Driver output high voltage;

V_{OLD} = Driver output low voltage.

The power supply current (I_M) is obtained from Figure 8. After the power dissipation is calculated, the junction temperature can be calculated using:

$$T_J = (P \times R_{\theta JA}) + T_A$$

where $R_{\theta JA}$ = Junction to ambient thermal resistance; (52°C/W for the DIP, 72°C/W for the FN Package)

T_A = Ambient Temperature.

For example, assume an application where $V_M = 12 \text{ V}$, the motor requires 200 mA/coil , operating at room

temperature with no heatsink on the IC. I_{BS} is calculated:

$$I_{BS} = 200 \times 0.86$$

$$I_{BS} = 172 \mu\text{A}$$

R_B is calculated:

$$R_B = (12 - 0.7) \text{ V} / 172 \mu\text{A}$$

$$R_B = 65.7 \text{ k}\Omega$$

From Figure 8, I_M (max) is determined to be 40 mA .

From Figure 9, V_{OLD} is 0.46 volts , and from Figure 10, $(V_M - V_{OHD})$ is 1.4 volts .

$$P = (12 \times 0.040) + (2 \times 0.2) (1.4 + 0.46)$$

$$P = 1.22 \text{ W}$$

$$T_J = (1.22 \text{ W} \times 52^\circ\text{C/W}) + 25^\circ\text{C}$$

$$T_J = 88^\circ\text{C}$$

This temperature is well below the maximum limit. If the calculated T_J had been higher than 150°C , a heatsink such as the Staver Co. V-7 Series, Aavid #5802, or Thermalloy #6012 could be used to reduce $R_{\theta JA}$. In extreme cases forced air cooling should be considered.

The above calculation, and $R_{\theta JA}$, assumes that a ground plane is provided under the MC3479 (either on both sides of the PC board) to aid in the heat dissipation. Single nominal width traces leading from the four ground pins should be avoided as this will increase T_J , as well as provide potentially disruptive ground noise and I_Q drops when switching the motor current.

FIGURE 9 — MAXIMUM SATURATION VOLTAGE — DRIVER OUTPUT LOW

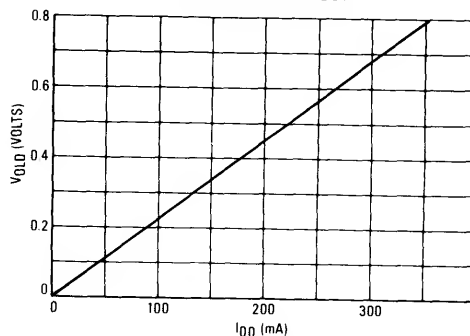


FIGURE 10 — MAXIMUM SATURATION VOLTAGE — DRIVER OUTPUT HIGH

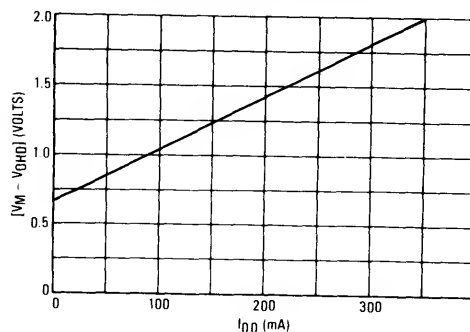
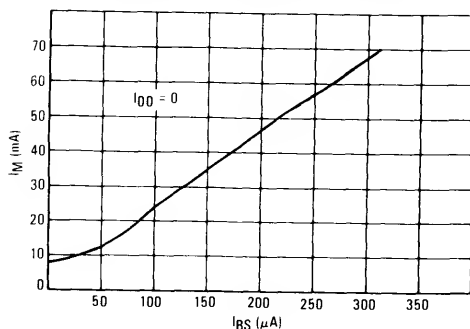


FIGURE 8 — POWER SUPPLY CURRENT



MC3479

FIGURE 11 — TYPICAL APPLICATIONS CIRCUIT

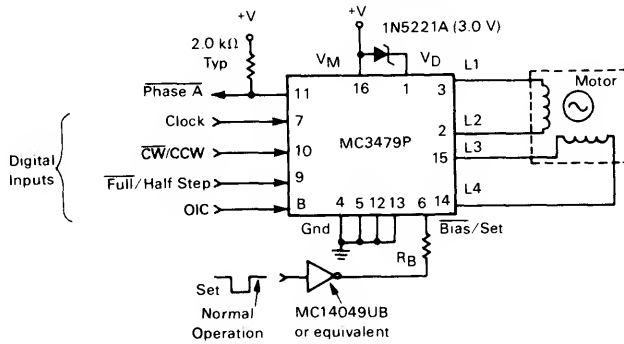
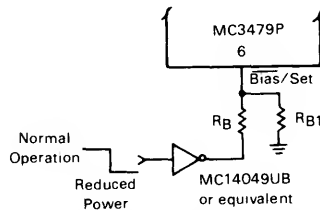


FIGURE 12 — POWER REDUCTION



- Suggested value for R_{B1} ($V_M = 12\text{ V}$) is $150\text{ k}\Omega$
- R_B calculation (see text) must take into account the current through R_{B1}

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

4

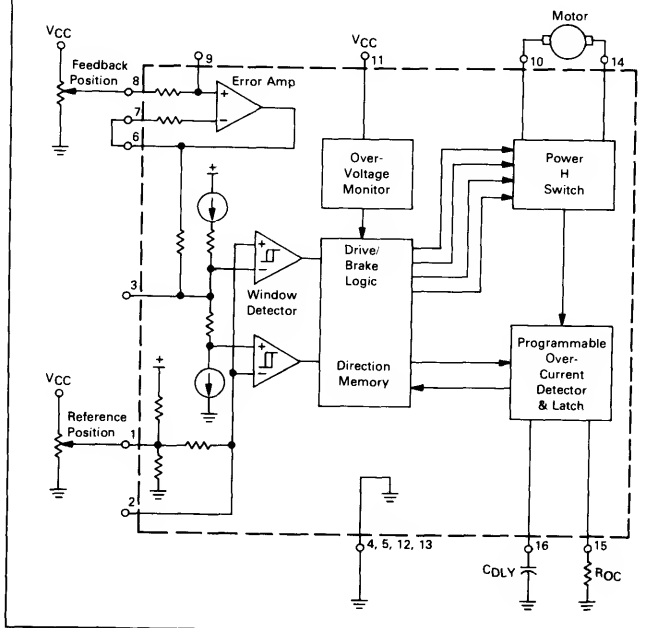
DC SERVO MOTOR CONTROLLER/DRIVER

The MC33030 is a monolithic dc servo motor controller providing all active functions necessary for a complete closed loop system. This device consists of an on-chip op amp and window comparator with wide input common-mode range, drive and brake logic with direction memory, power H switch driver capable of 1.0 A, independently programmable over-current monitor and shutdown delay, and over-voltage monitor. This part is ideally suited for almost any servo positioning application that requires sensing of temperature, pressure, light, magnetic flux, or any other means that can be converted to a voltage.

Although this device is primarily intended for servo applications, it can be used as a switchmode motor controller.

- On-Chip Error Amp for Feedback Monitoring
- Window Detector with Deadband and Self Centering Reference Input
- Drive/Brake Logic with Direction Memory
- 1.0 A Power H Switch
- Programmable Over-Current Detector
- Programmable Over-Current Shutdown Delay
- Over-Voltage Shutdown

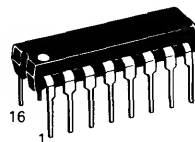
SIMPLIFIED BLOCK DIAGRAM



MC33030

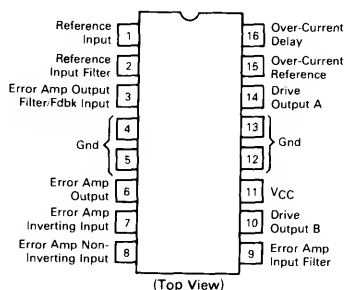
DC SERVO MOTOR CONTROLLER/DRIVER

SILICON MONOLITHIC
INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 648C

PIN CONNECTIONS



Pins 4, 5, 12 and 13 are electrical ground and heat sink pins for IC

ORDERING INFORMATION

Device	Temperature Range	Package
MC33030P	-40°C to +85°C	Plastic DIP

MC33030

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	36	V
Input Voltage Range Op Amp, Comparator, Current Limit. Pins 1, 2, 3, 6, 7, 8, 9, 15.	V_{IR}	-0.3 to V_{CC}	V
Input Differential Voltage Range Op Amp, Comparator. Pins 1, 2, 3, 6, 7, 8, 9.	V_{IDR}	-0.3 to V_{CC}	V
Delay Pin Sink Current (Pin 16)	$I_{DL}(sink)$	20	mA
Output Source Current (Op Amp)	I_{source}	10	mA
Drive Output Voltage Range (Note 1)	V_{DRV}	-0.3 to ($V_{CC} + V_F$)	V
Drive Output Source Current (Note 2)	$I_{DRV}(source)$	1.0	A
Drive Output Sink Current (Note 2)	$I_{DRV}(sink)$	1.0	A
Brake Diode Forward Current (Note 2)	I_F	1.0	A
Power Dissipation and Thermal Characteristics Maximum Power Dissipation (θ $T_A = 70^\circ\text{C}$ Thermal Resistance Junction to Air Thermal Resistance Junction to Case. Pins 4, 5, 12, 13.	P_D $R_{\theta JA}$ $R_{\theta JC}$	1000 80 15	mW $^\circ\text{C/W}$ $^\circ\text{C/W}$
Operating Junction Temperature	T_J	+150	$^\circ\text{C}$
Operating Ambient Temperature Range	T_A	-40 to +85	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

NOTES:

1. The upper voltage level is clamped by the forward drop, V_F , of the brake diode.
2. These values are for continuous dc current. Maximum package power dissipation limits must be observed.

ELECTRICAL CHARACTERISTICS ($V_{CC} = 14\text{ V}$, $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ERROR AMP					
Input Offset Voltage ($-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$) $V_{Pin\ 6} = 7.0\text{ V}$, $R_L = 100\text{ k}$	V_{IO}	—	1.5	10	mV
Input Offset Current $V_{Pin\ 6} = 1.0\text{ V}$, $R_L = 100\text{ k}$	I_{IO}	—	0.7	—	nA
Input Bias Current $V_{Pin\ 6} = 7.0\text{ V}$, $R_L = 100\text{ k}$	I_{IB}	—	7.0	—	nA
Input Common-Mode Voltage Range $\Delta V_{IO} = 20\text{ mV}$, $R_L = 100\text{ k}$	V_{ICR}	—	0 to ($V_{CC} - 1.2$)	—	V
Slew Rate, Open Loop ($V_{ID} = 0.5\text{ V}$, $C_L = 15\text{ pF}$)	SR	—	0.40	—	V/ μs
Unity-Gain Crossover Frequency	f_c	—	550	—	kHz
Unity-Gain Phase Margin	ϕ_m	—	63	—	deg.
Common-Mode Rejection Ratio $V_{Pin\ 6} = 7.0\text{ V}$, $R_L = 100\text{ k}$	CMRR	50	82	—	dB
Power Supply Rejection Ratio $V_{CC} = 9.0\text{ to }16\text{ V}$, $V_{Pin\ 6} = 7.0\text{ V}$, $R_L = 100\text{ k}$	PSRR	—	89	—	dB
Output Source Current ($V_{Pin\ 6} = 12\text{ V}$)	I_{O+}	—	1.8	—	mA
Output Sink Current ($V_{Pin\ 6} = 1.0\text{ V}$)	I_{O-}	—	250	—	μA
Output Voltage Swing ($R_L = 17\text{ k}$ to Ground)	V_{OH} V_{OL}	12.5 —	13.1 0.02	— —	V V

(Continued)

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Min	Typ	Max	Unit
WINDOW DETECTOR					
Input Hysteresis Voltage ($V_1 - V_4$, $V_2 - V_3$, Figure 17)	V_H	25	35	45	mV
Input Dead Zone Range ($V_2 - V_4$, Figure 17)	V_{IDZ}	166	210	254	mV
Input Offset Voltage ($ (V_2 - V_{Pin 2}) - (V_{Pin 2} - V_4) $, Figure 17)	V_{IO}	—	25	—	mV
Input Functional Common-Mode Range (Note 3)					V
Upper Threshold	V_{IH}	—	($V_{CC} - 1.05$)	—	
Lower Threshold	V_{IL}	—	0.24	—	
Reference Input Self Centering Voltage Pins 1 and 2 Open	V_{RSC}	—	($1/2 V_{CC}$)	—	V
Window Detector Propagation Delay Comparator Input, Pin 3, to Drive Outputs $V_{ID} = 0.5$ V, $R_{L(DRV)} = 390$ Ω	$t_{p(IN/DRV)}$	—	2.0	—	μ s

OVER-CURRENT MONITOR

Over-Current Reference Resistor Voltage (Pin 15)	R_{OC}	3.9	4.3	4.7	V
Delay Pin Source Current $V_{DLY} = 0$ V, $R_{OC} = 27$ k, $I_{DRV} = 0$ mA	$I_{DLY(source)}$	—	5.5	6.9	μ A
Delay Pin Sink Current ($R_{OC} = 27$ k, $I_{DRV} = 0$ mA)	$I_{DLY(sink)}$				mA
$V_{DLY} = 5.0$ V		—	0.1	—	
$V_{DLY} = 8.3$ V		—	0.7	—	
$V_{DLY} = 14$ V		—	16.5	—	
Delay Pin Voltage, Low State ($I_{DLY} = 0$ mA)	$V_{OL(DLY)}$	—	0.3	0.4	V
Over-Current Shutdown Threshold	$V_{th(OC)}$				V
$V_{CC} = 14$ V		6.8	7.5	8.2	
$V_{CC} = 8.0$ V		5.5	6.0	6.5	
Over-Current Shutdown Propagation Delay Delay Capacitor Input, Pin 16, to Drive Outputs $V_{ID} = 0.5$ V	$t_{p(DLY/DRV)}$	—	1.8	—	μ s

POWER H-SWITCH

Drive-Output Saturation ($-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$, Note 4)					V
High State ($I_{source} = 100$ mA)	$V_{OH(DRV)}$	($V_{CC} - 2$)	($V_{CC} - 0.85$)	—	
Low State ($I_{sink} = 100$ mA)	$V_{OL(DRV)}$	—	0.12	1.0	
Drive-Output Voltage Switching Time ($C_L = 15$ pF)					ns
Rise Time	t_r	—	200	—	
Fall Time	t_f	—	200	—	
Brake Diode Forward Voltage Drop ($I_F = 200$ mA, Note 4)	V_F	—	1.04	2.5	V

TOTAL DEVICE

Standby Supply Current	I_{CC}	—	14	25	mA
Over-Voltage Shutdown Threshold ($-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$)	$V_{th(OV)}$	16.5	18	20.5	V
Over-Voltage Shutdown Hysteresis (Device off to on)	$V_{H(OV)}$	0.3	0.6	1.0	V
Operating Voltage Lower Threshold ($-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$)	V_{CC}	—	7.5	8.0	V

NOTES:

- The upper or lower hysteresis will be lost when operating the Input, Pin 3, close to the respective rail. Refer to Figure 4.
- Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

FIGURE 1 — ERROR AMP INPUT COMMON-MODE VOLTAGE RANGE versus TEMPERATURE

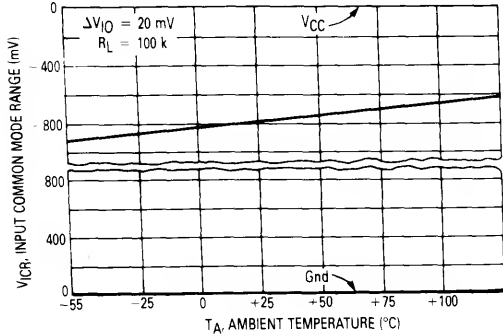


FIGURE 2 — ERROR AMP OUTPUT SATURATION versus LOAD CURRENT

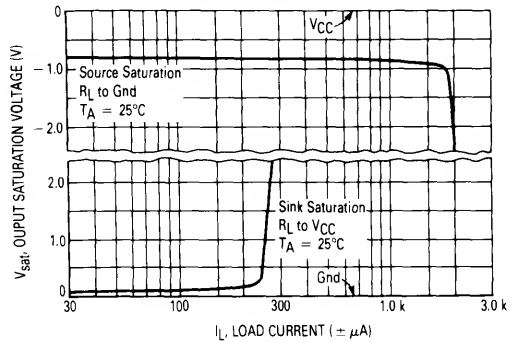


FIGURE 3 — OPEN-LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY

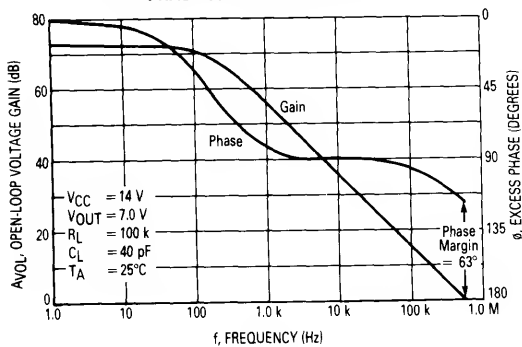


FIGURE 4 — WINDOW DETECTOR REFERENCE-INPUT COMMON-MODE VOLTAGE RANGE versus TEMPERATURE

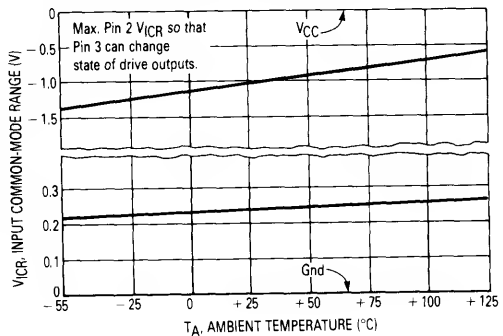


FIGURE 5 — WINDOW DETECTOR FEEDBACK-INPUT THRESHOLDS versus TEMPERATURE

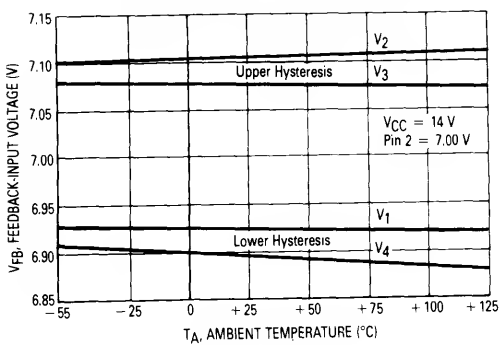
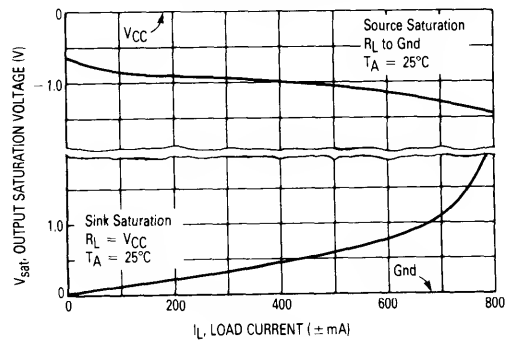
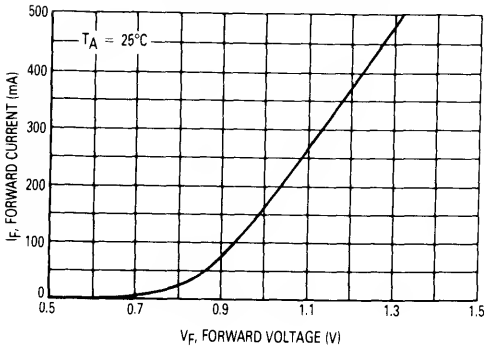


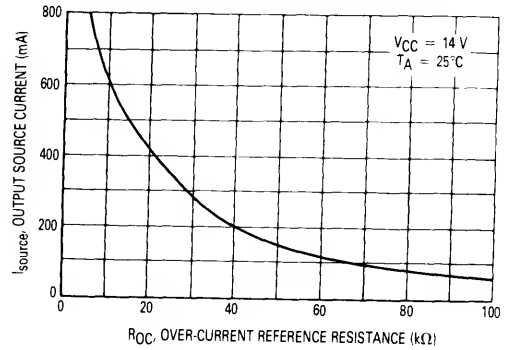
FIGURE 6 — OUTPUT DRIVE SATURATION versus LOAD CURRENT



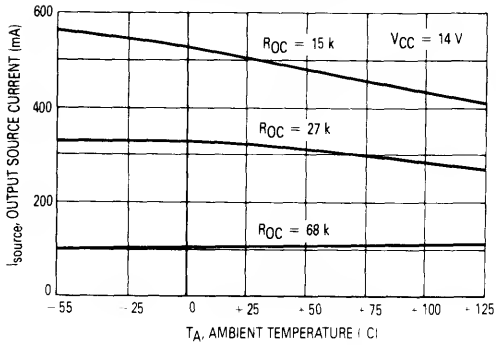
**FIGURE 7 — BRAKE DIODE FORWARD CURRENT
versus FORWARD VOLTAGE**



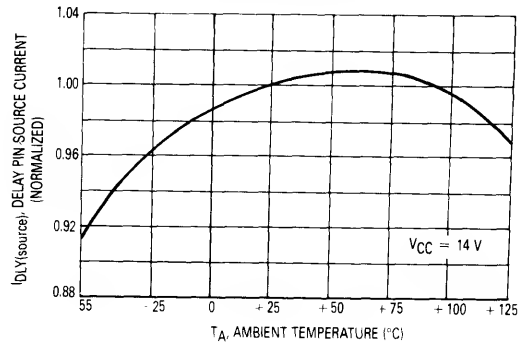
**FIGURE 8 — OUTPUT SOURCE CURRENT-LIMIT
versus OVER-CURRENT REFERENCE RESISTANCE**



**FIGURE 9 — OUTPUT SOURCE CURRENT-LIMIT
versus TEMPERATURE**



**FIGURE 10 — NORMALIZED DELAY PIN SOURCE CURRENT
versus TEMPERATURE**



**FIGURE 11 — NORMALIZED OVER-CURRENT DELAY
THRESHOLD VOLTAGE versus TEMPERATURE**

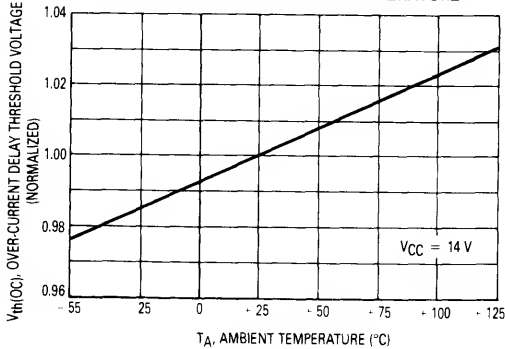


FIGURE 12 — SUPPLY CURRENT versus SUPPLY VOLTAGE

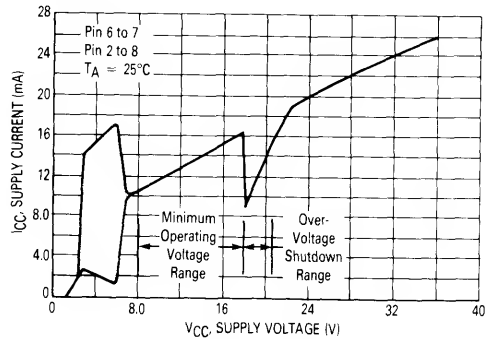


FIGURE 13 — NORMALIZED OVER-VOLTAGE SHUTDOWN THRESHOLD versus TEMPERATURE

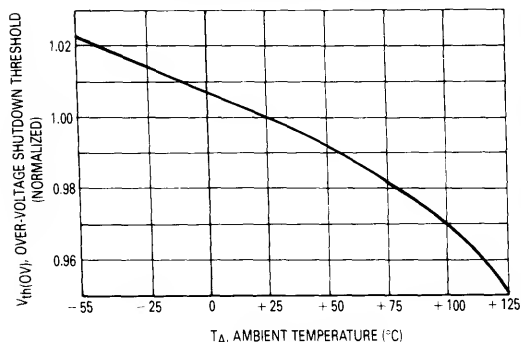


FIGURE 14 — NORMALIZED OVER-VOLTAGE SHUTDOWN HYSTERESIS versus TEMPERATURE

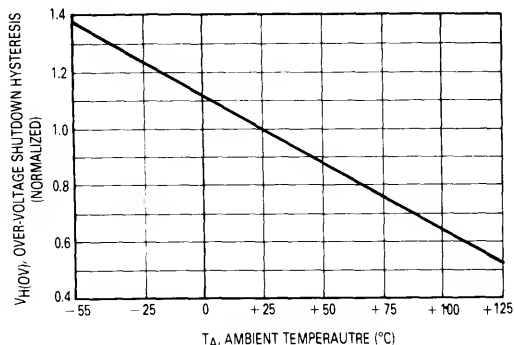
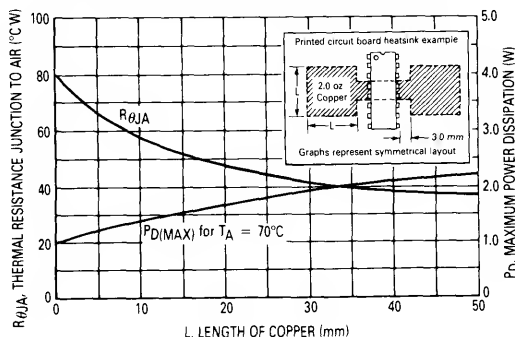


FIGURE 15 — THERMAL RESISTANCE AND MAXIMUM POWER DISSIPATION versus P.C.B. COPPER LENGTH



OPERATING DESCRIPTION

The MC33030 was designed to drive fractional horsepower dc motors and sense actuator position by voltage feedback. A typical servo application and representative internal block diagram are shown in Figure 16. The system operates by setting a voltage on the reference input of the Window Detector (Pin 1) which appears on (Pin 2). A dc motor then drives a position sensor, usually a potentiometer driven by a gear box, in a corrective fashion so that a voltage proportional to position is present at Pin 3. The servo motor will continue to run until the voltage at Pin 3 falls within the dead zone, which is centered about the reference voltage.

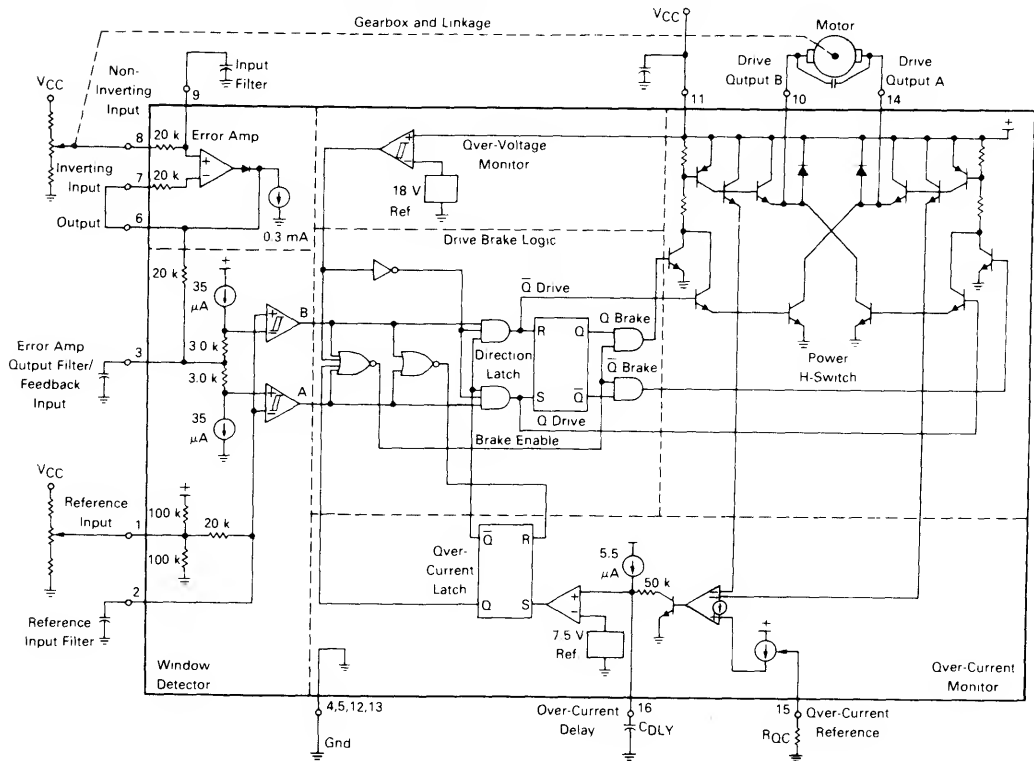
The Window Detector is composed of two comparators, A and B, each containing hysteresis. The reference input, common to both comparators, is pre-biased at $1/2 V_{CC}$ for simple two position servo systems and can easily be overridden by an external voltage divider. The feedback voltage present at Pin 3 is connected to the center of two resistors that are driven by an equal magnitude current source and sink. This generates an offset voltage at the input of each comparator which is

centered about Pin 3 that can float virtually from V_{CC} to ground. The sum of the upper and lower offset voltages is defined as the window detector input dead zone range.

To increase system flexibility, an on-chip Error Amp is provided. It can be used to buffer and/or gain-up the actuator position voltage which has the effect of narrowing the dead zone range. A PNP differential input stage is provided so that the input common-mode voltage range will include ground. The main design goal of the error amp output stage was to be able to drive the window detector input. It typically can source 1.8 mA and sink 250 μA . Special design considerations must be made if it is to be used for other applications.

The Power H-Switch provides a direct means for motor drive and braking with a maximum source, sink, and brake current of 1.0 A continuous. Maximum package power dissipation limits must be observed. Refer to Figure 15 for thermal information. For greater drive current requirements, a method for buffering that maintains all the system features is shown in Figure 29.

FIGURE 16 — REPRESENTATIVE BLOCK DIAGRAM AND TYPICAL SERVO APPLICATION



The Over-Current Monitor is designed to distinguish between motor start-up or locked rotor conditions that can occur when the actuator has reached its travel limit. A fraction of the Power H-Switch source current is internally fed into one of the two inverting inputs of the current comparator, while the non-inverting input is driven by a programmable current reference. This reference level is controlled by the resistance value selected for R_{OC} , and must be greater than the required motor run-current with its mechanical load over temperature; refer to Figure 8. During an over-current condition, the comparator will turn off and allow the current source to charge the delay capacitor, C_{DLY} . When C_{DLY} charges to a level of 7.5 V, the set input of the over-current latch will go high, disabling the drive and brake functions of the Power H-Switch. The programmable time delay is determined by the capacitance value selected for C_{DLY} .

$$t_{DLY} = \frac{V_{ref} C_{DLY}}{I_{DLY}(\text{source})} = \frac{7.5 C_{DLY}}{5.5 \mu A} = 1.36 C_{DLY} \text{ in } \mu F$$

This system allows the Power H-Switch to supply motor start-up current for a predetermined amount of time. If the rotor is locked, the system will time-out and shut-down. This feature eliminates the need for servo end-of-travel or limit switches. Care must be taken so as not to select too large of a capacitance value for C_{DLY} . An over-current condition for an excessively long time-out period can cause the integrated circuit to overheat and eventually fail. Again, the maximum package power dissipation limits must be observed. The over-current latch is reset upon power-up or by readjusting $V_{pin 2}$ as to cause $V_{pin 3}$ to enter or pass through the dead zone. This can be achieved by requesting the motor to reverse direction.

An Over-Voltage Monitor circuit provides protection for the integrated circuit and motor by disabling the Power H-Switch functions if V_{CC} should exceed 18 V. Resumption of normal operation will commence when V_{CC} falls below 17.4 V.

A timing diagram that depicts the operation of the Drive/Brake Logic section is shown in Figure 17. The waveforms grouped in [1] show a reference voltage that was preset, appearing on Pin 2, which corresponds to the desired actuator position. The true actuator position is represented by the voltage on Pin 3. The points V_1 through V_4 represent the input voltage thresholds of comparators A and B that cause a change in their respective output state. They are defined as follows:

V_1 = Comparator B turn-off threshold

V_2 = Comparator A turn-on threshold

V_3 = Comparator A turn-off threshold

V_4 = Comparator B turn-on threshold

V_1 - V_4 = Comparator B input hysteresis voltage

V_2 - V_3 = Comparator A input hysteresis voltage

V_2 - V_4 = Window detector input dead zone range

$|(V_2 - V_{pin2}) - (V_{pin2} - V_4)|$ = Window detector input offset voltage

It must be remembered that points V_1 through V_4 always try to follow and center about the reference voltage setting if it is within the input common-mode voltage range of Pin 3; Figures 4 and 5. Initially consider that the feedback input voltage level is somewhere on the dashed line between V_2 and V_4 in [1]. This is within the dead zone range as defined above and the motor will be off. Now if the reference voltage is raised so that V_{pin3} is less than V_4 , comparator B will turn-on [3] enabling \bar{Q} Drive, causing Drive Output A to sink and B to source motor current [8]. The actuator will move in Direction B until V_{pin3} becomes greater than V_1 . Comparator B will turn-off, activating the brake enable [4] and \bar{Q} Brake [6] causing Drive Output A to go high and B to go into a high impedance state. The inertia of the mechanical system will drive the motor as a generator creating a positive voltage on Pin 10 with respect to Pin 14. The servo system can be stopped quickly, so as not to over-shoot through the dead zone range, by braking. This is accomplished by shorting the motor/generator terminals together. Brake current will flow into the diode at Drive Output B, through the internal V_{CC} rail, and out the emitter of the sourcing transistor at Drive Output A. The end of the solid line and beginning of the dashed for V_{pin3} [1] indicates the possible resting position of the actuator after braking.

If V_{pin3} should continue to rise and become greater than V_2 , the actuator will have over shot the dead zone range and cause the motor to run in Direction A until V_{pin3} is equal to V_3 . The Drive/Brake behavior for Direction A is identical to that of B. Overshooting the dead zone range in both directions can cause the servo system to continuously hunt or oscillate. Notice that the

last motor run-direction is stored in the direction latch. This information is needed to determine whether Q or \bar{Q} Brake is to be enabled when V_{pin3} enters the dead zone range. The dashed lines in [8,9] indicate the resulting waveforms of an over-current condition that has exceeded the programmed time delay. Notice that both Drive Outputs go into a high impedance state until V_{pin2} is readjusted so that V_{pin3} enters or crosses through the dead zone [7,4].

The inputs of the Error Amp and Window Detector can be susceptible to the noise created by the brushes of the dc motor and cause the servo to hunt. Therefore, each of these inputs are provided with an internal series resistor and are pinned out for an external bypass capacitor. It has been found that placing a capacitor with short leads directly across the brushes will significantly reduce noise problems. Good quality RF bypass capacitors in the range of 0.001 to 0.1 μ F may be required. Many of the more economical motors will generate significant levels of RF energy over a spectrum that extends from dc to beyond 200 MHz. The capacitance value and method of noise filtering must be determined on a system by system basis.

Thus far, the operating description has been limited to servo systems in which the motor mechanically drives a potentiometer for position sensing. Figures 18, 19, 26, and 30 show examples that use light, magnetic flux, temperature, and pressure as a means to drive the feedback element. Figures 20, 21 and 22 are examples of two position, open-loop servo systems. In these systems, the motor runs the actuator to each end of its travel limit where the Over-Current Monitor detects a locked rotor condition and shuts down the drive. Figures 31 and 32 show two possible methods of using the MC33030 as a switching motor controller. In each example a fixed reference voltage is applied to Pin 2. This causes V_{pin3} to be less than V_4 and Drive Output A, Pin 14, to be in a low state saturating the TIP42 transistor. In Figure 31, the motor drives a tachometer that generates an ac voltage proportional to RPM. This voltage is rectified, filtered, divided down by the speed set potentiometer, and applied to Pin 8. The motor will accelerate until V_{pin3} is equal to V_1 at which time Pin 14 will go to a high state and terminate the motor drive. The motor will now coast until V_{pin3} is less than V_4 where upon drive is then reapplied. The system operation of Figure 32 identical to that of 31 except the signal at Pin 3 is an amplified average of the motors drive and back EMF voltages. Both systems exhibit excellent control of RPM with variations of V_{CC} ; however, Figure 31 has somewhat better torque characteristics at low RPM.

FIGURE 17 — TIMING DIAGRAM

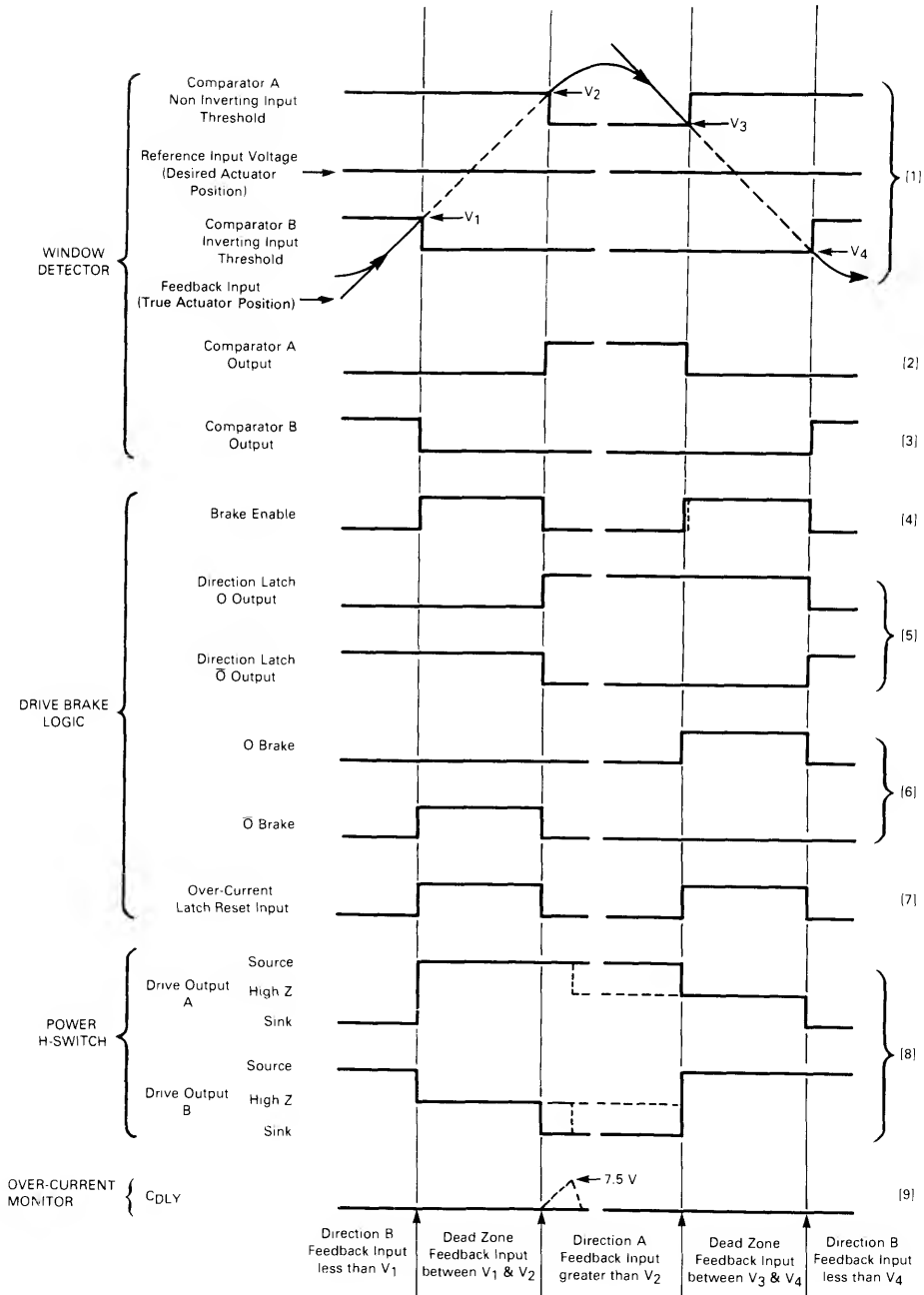


FIGURE 18 — SOLAR TRACKING SERVO SYSTEM

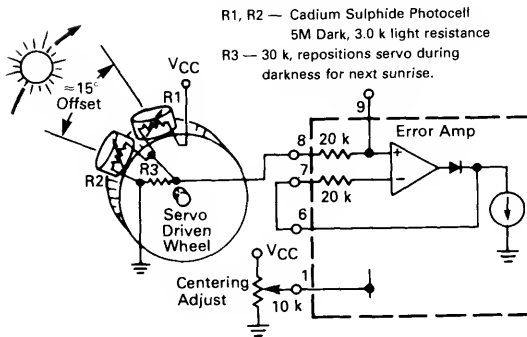
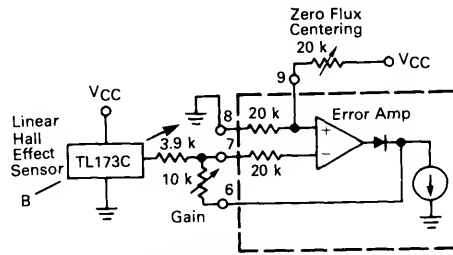
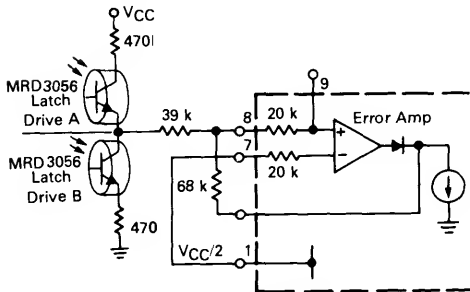


FIGURE 19 — MAGNETIC SENSING SERVO SYSTEM



Typical sensitivity with gain set at 3.9 k is 1.5 mV/gauss. Servo motor controls magnetic field about sensor.

FIGURE 20 — INFRARED LATCHED TWO POSITION SERVO SYSTEM



Over-current monitor (not shown) shuts down servo when end stop is reached.

FIGURE 22 — 0.25 Hz SQUARE-WAVE SERVO AGITATOR

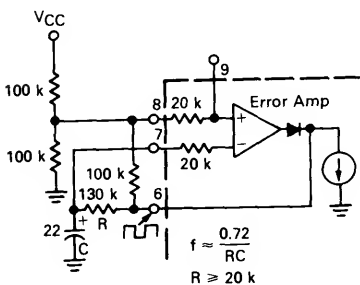
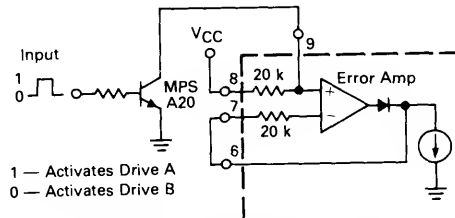


FIGURE 21 — DIGITAL TWO POSITION SERVO SYSTEM



Over-Current monitor (not shown) shuts down servo when end stop is reached.

FIGURE 23 — SECOND ORDER LOW-PASS ACTIVE FILTER

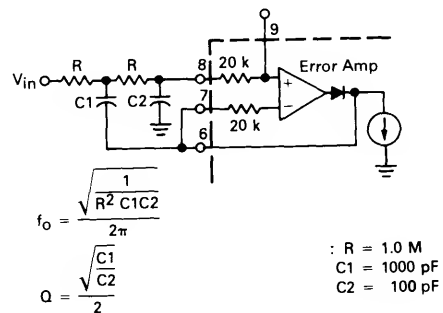


FIGURE 24 — NOTCH FILTER

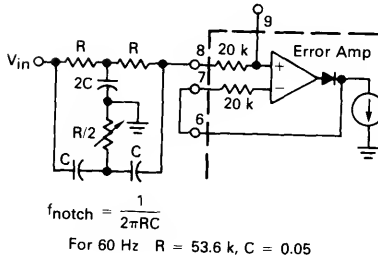


FIGURE 25 — DIFFERENTIAL INPUT AMPLIFIER

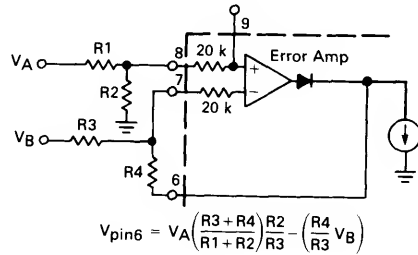


FIGURE 26 — TEMPERATURE SENSING SERVO SYSTEM

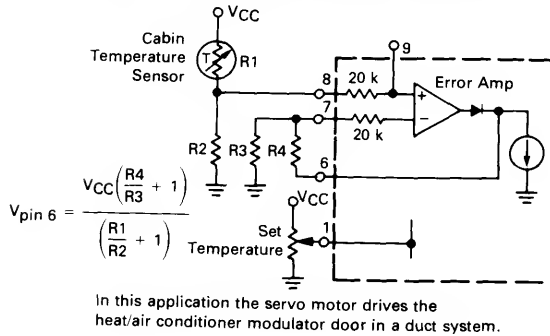


FIGURE 27 — BRIDGE AMPLIFIER

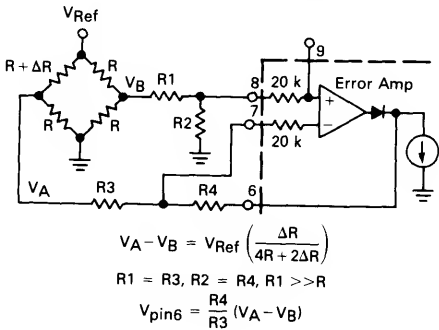


FIGURE 28 — REMOTE LATCHED SHUTDOWN

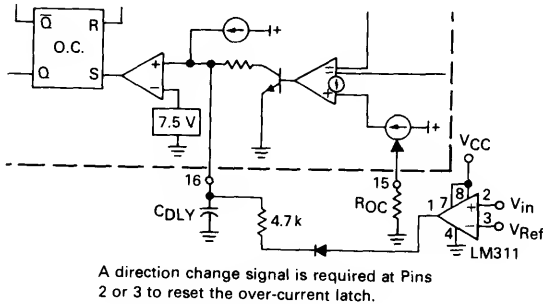
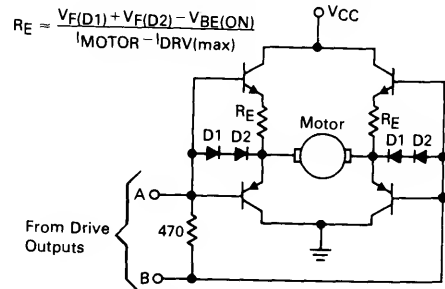


FIGURE 29 — POWER H-SWITCH BUFFER



This circuit maintains the brake and over-current features of the MC33030. Set R_{OC} to 15 k for $I_{\text{DRV(max)}} \approx 0.5 \text{ A}$.

FIGURE 30 — ADJUSTABLE PRESSURE DIFFERENTIAL REGULATOR

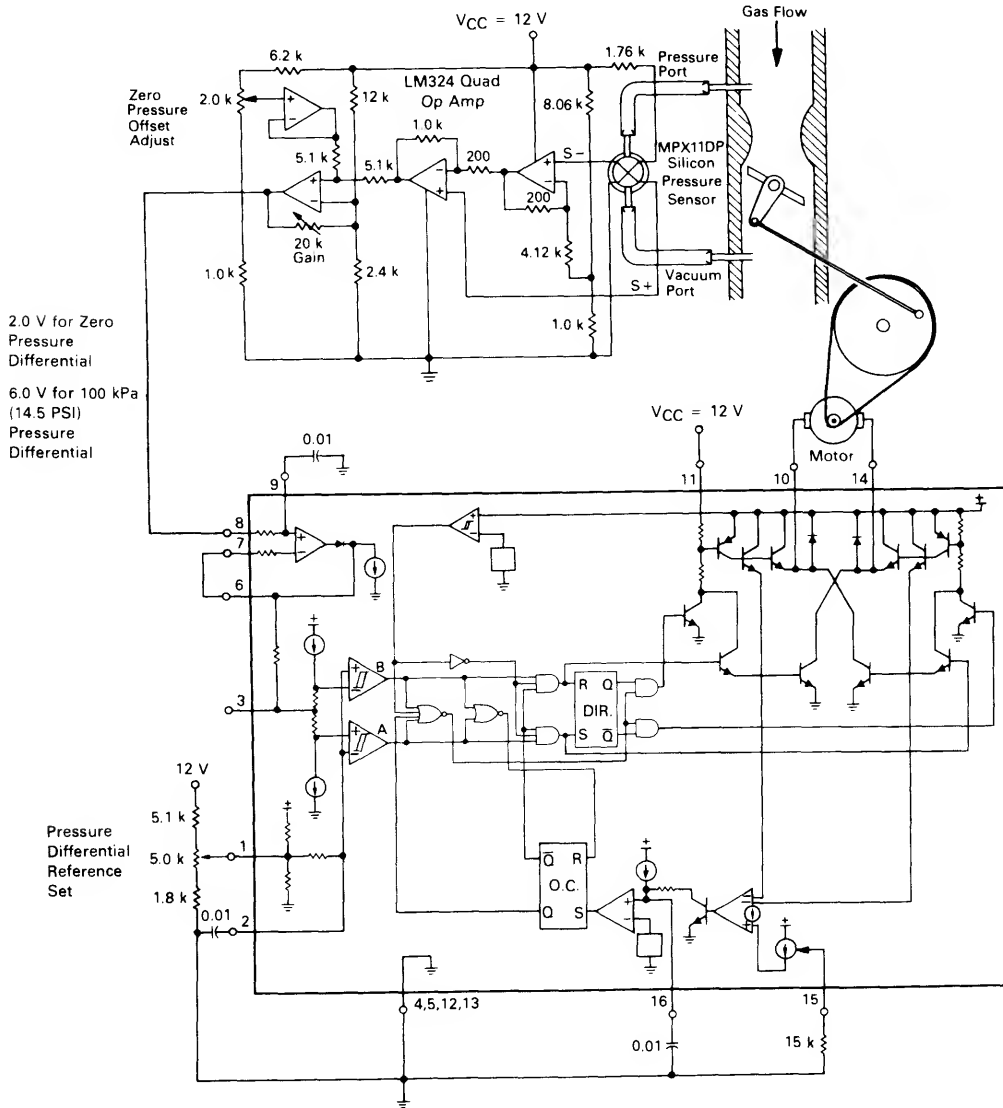


FIGURE 31 — SWITCHING MOTOR CONTROLLER WITH BUFFERED OUTPUT AND TACH FEEDBACK

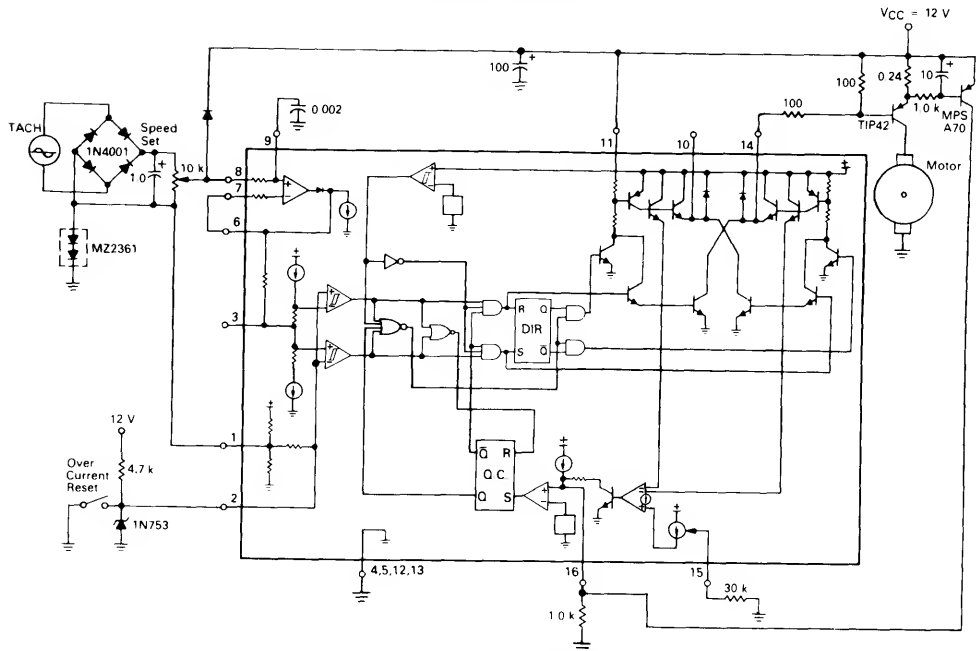
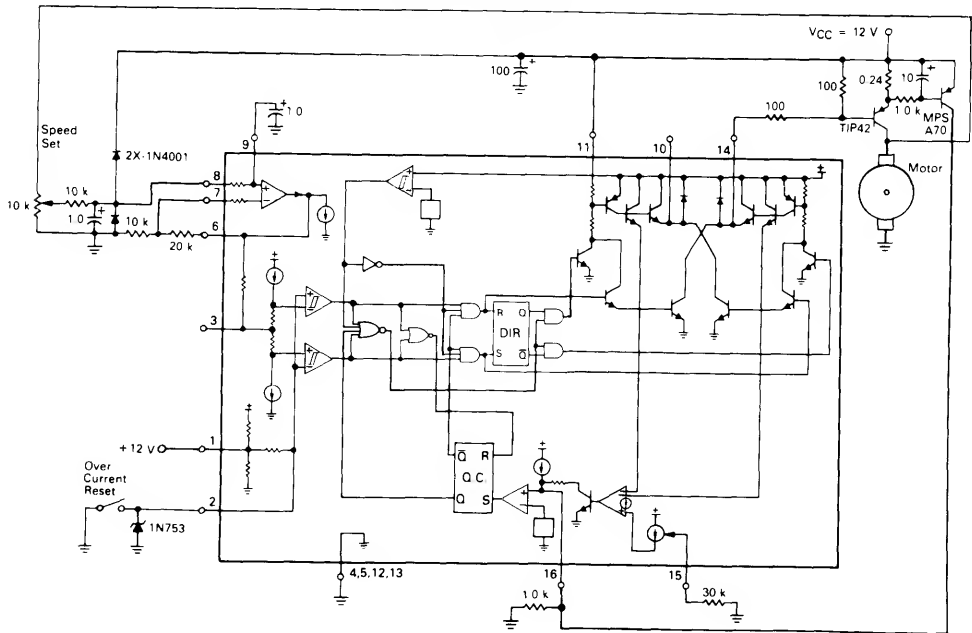


FIGURE 32 — SWITCHING MOTOR CONTROLLER WITH BUFFERED OUTPUT AND BACK EMF SENSING



Advance Information

BRUSHLESS DC MOTOR CONTROLLER

The MC33033 is a high performance second generation, limited feature, monolithic brushless DC motor controller which has evolved from Motorola's full featured MC33034 and MC33035 controllers. It contains all of the active functions required for the implementation of open-loop, three or four phase motor control. The device consists of a rotor position decoder for proper commutation sequencing, temperature compensated reference capable of supplying sensor power, frequency programmable sawtooth oscillator, fully accessible error amplifier, pulse width modulator comparator, three open collector top drivers, and three high current totem pole bottom drivers ideally suited for driving power MOSFETs. Unlike its predecessors, it does not feature separate drive circuit supply and ground pins, brake input, or fault output signal.

Included in the MC33033 are protective features consisting of under-voltage lockout, cycle-by-cycle current limiting with a selectable time delayed latched shutdown mode, and internal thermal shutdown.

Typical motor control functions include open-loop speed, forward or reverse direction, and run enable. The MC33033 is designed to operate brushless motors with electrical sensor phasings of 60°/300° or 120°/240°, and can also efficiently control brush DC motors.

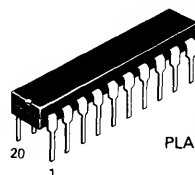
- 10 V to 30 V Operation
- Undervoltage Lockout
- 6.25 V Reference Capable of Supplying Sensor Power
- Fully Accessible Error Amplifier for Closed-Loop Servo Applications
- High Current Drivers can Control MPM3003 MOSFET 3-Phase Bridge
- Cycle-By-Cycle Current Limiting
- Internal Thermal Shutdown
- Selectable 60°/300° or 120°/240° Sensor Phasings
- Also Efficiently Controls Brush DC Motors with MPM3002 MOSFET H-Bridge

MC33033

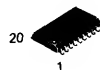
BRUSHLESS DC MOTOR CONTROLLER

SILICON MONOLITHIC INTEGRATED CIRCUIT

4

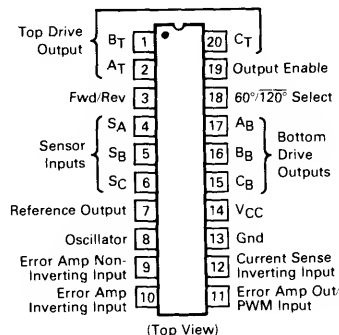


P SUFFIX
PLASTIC PACKAGE
CASE 738



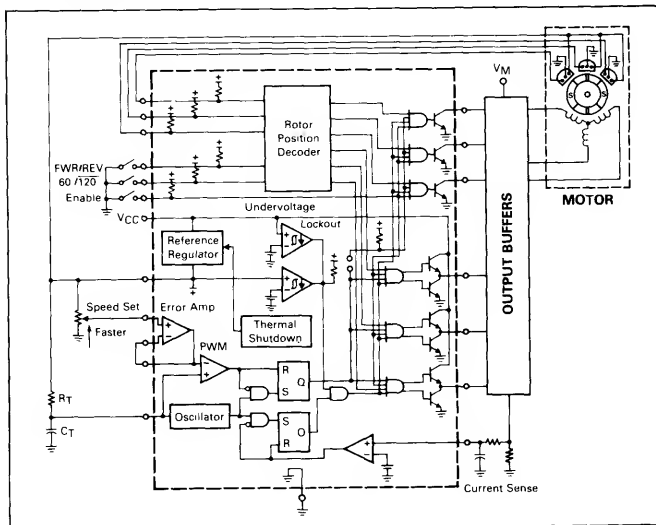
DW SUFFIX
PLASTIC PACKAGE
CASE 751D
(SO-20L)

PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Ambient Temperature Range	Package
MC33033P	-40°C to +85°C	Plastic DIP
MC33033DW	-40°C to +85°C	SO-20L



This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	30	V
Digital Inputs (Pins 3, 4, 5, 6, 18, 19)	—	V_{ref}	V
Oscillator Input Current (Source or Sink)	I_{OSC}	30	mA
Error Amp Input Voltage Range (Pins 9, 10, Note 1)	V_{IR}	-3.0 to V_{ref}	V
Error Amp Output Current (Source or Sink, Note 2)	I_{Out}	10	mA
Current Sense Input Voltage Range	V_{Sense}	-0.3 to 5.0	V
Top Drive Voltage (Pins 1, 2, 20)	$V_{CE(top)}$	40	V
Top Drive Sink Current (Pins 1, 2, 20)	$I_{Sink(top)}$	50	mA
Bottom Drive Output Current (Source or Sink, Pins 15, 16, 17)	I_{DRV}	100	mA
Power Dissipation and Thermal Characteristics Maximum Power Dissipation (α $T_A = 85^\circ\text{C}$ Thermal Resistance, Junction to Air	P_D $R_{\theta JA}$	867 75	mW $^\circ\text{C/W}$
Operating Junction Temperature	T_J	150	$^\circ\text{C}$
Operating Ambient Temperature Range	T_A	-40 to +85	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($V_{CC} = 20\text{ V}$, $R_T = 4.7\text{ k}$, $C_T = 10\text{ nF}$, $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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REFERENCE SECTION

Reference Output Voltage ($I_{ref} = 1.0\text{ mA}$) $T_A = 25^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	V_{ref}	5.9 5.82	6.24 —	6.5 6.57	V
Line Regulation ($V_{CC} = 10\text{ V}$ to 30 V , $I_{ref} = 1.0\text{ mA}$)	Reg_{line}	—	1.5	30	mV
Load Regulation ($I_{ref} = 1.0\text{ mA}$ to 20 mA)	Reg_{load}	—	16	30	mV
Output Short-Circuit Current (Note 3)	I_{SC}	40	75	—	mA
Reference Under Voltage Lockout Threshold	V_{th}	4.0	4.5	5.0	V

ERROR AMPLIFIER

Input Offset Voltage ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)	V_{IO}	—	0.4	10	mV
Input Offset Current ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)	I_{IO}	—	8.0	500	nA
Input Bias Current ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)	I_{IB}	—	-46	-1000	nA
Input Common Mode Voltage Range	V_{ICR}	(0 V to V_{ref})			V
Open-Loop Voltage Gain ($V_O = 3.0\text{ V}$, $R_L = 15\text{ k}$)	AV_{OL}	70	80	—	dB
Input Common Mode Rejection Ratio	$CMRR$	55	86	—	dB
Power Supply Rejection Ratio ($V_{CC} = 10\text{ V}$ to 30 V)	$PSRR$	65	105	—	dB
Output Voltage Swing High State ($R_L = 15\text{ k}$ to Ground) Low State ($R_L = 15\text{ k}$ to V_{ref})	V_{OH} V_{OL}	4.6 —	5.3 0.5	— 1.0	V

NOTES:

1. The input common mode voltage or input signal voltage should not be allowed to go negative by more than 0.3 V.
2. The compliance voltage must not exceed the range of -0.3 to V_{ref} .
3. Maximum package power dissipation limits must be observed.

ELECTRICAL CHARACTERISTICS (continued) ($V_{CC} = 20\text{ V}$, $R_T = 4.7\text{ k}$, $C_T = 10\text{ nF}$, $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR SECTION					
Oscillator Frequency	f_{OSC}	22	25	28	kHz
Frequency Change with Voltage ($V_{CC} = 10\text{ V}$ to 30 V)	$\Delta f_{OSC}/\Delta V$	—	0.01	5.0	%
Sawtooth Peak Voltage	$V_{OSC(P)}$	—	4.1	4.5	V
Sawtooth Valley Voltage	$V_{OSC(V)}$	1.2	1.5	—	V

LOGIC INPUTS

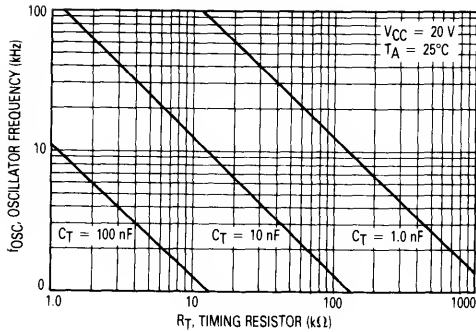
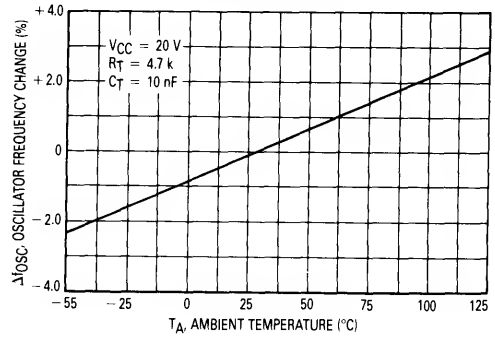
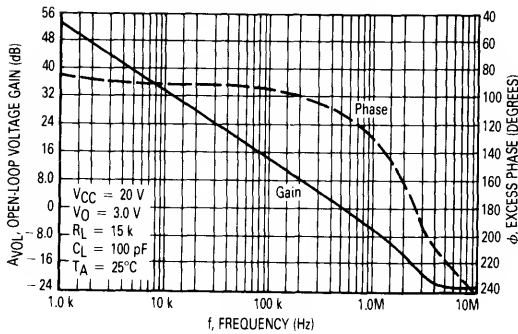
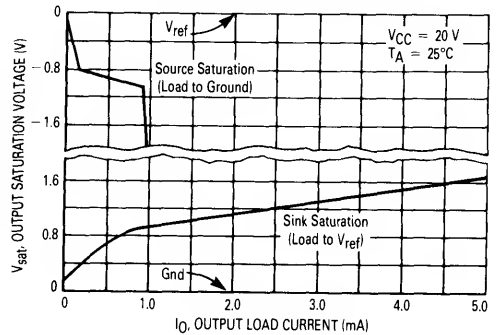
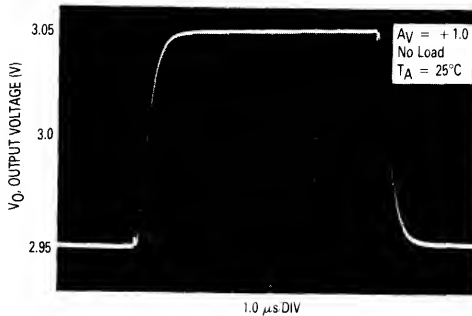
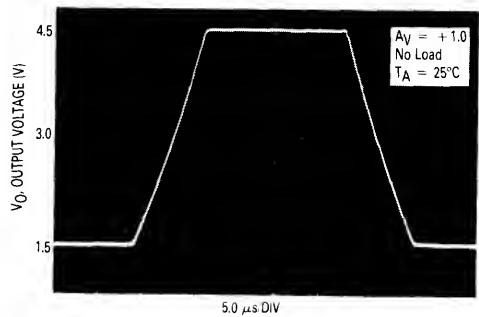
Input Threshold Voltage (Pins 3, 4, 5, 6, 18, 19)					V
High State	V_{IH}	3.0	2.2	—	
Low State	V_{IL}	—	1.7	0.8	
Sensor Inputs (Pins 4, 5, 6)					μA
High State Input Current ($V_{IH} = 5.0\text{ V}$)	I_{IH}	-150	-70	-20	
Low State Input Current ($V_{IL} = 0\text{ V}$)	I_{IL}	-600	-337	-150	
Forward/Reverse, 60°/120° Select and Output Enable (Pins 3, 18, 19)					μA
High State Input Current ($V_{IH} = 5.0\text{ V}$)	I_{IH}	-75	-36	-10	
Low State Input Current ($V_{IL} = 0\text{ V}$)	I_{IL}	-300	-175	-75	

CURRENT-LIMIT COMPARATOR

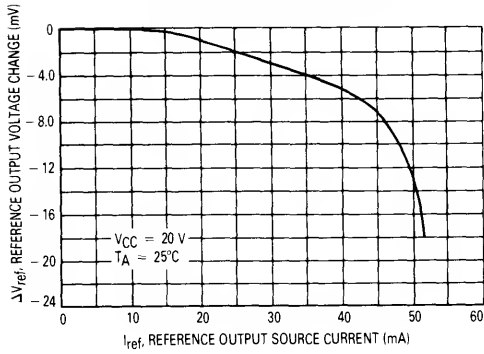
Threshold Voltage	V_{th}	85	101	115	mV
Input Common Mode Voltage Range	V_{ICR}	—	3.0	—	V
Input Bias Current	I_{IB}	—	-0.9	-5.0	μA

OUTPUTS AND POWER SECTIONS

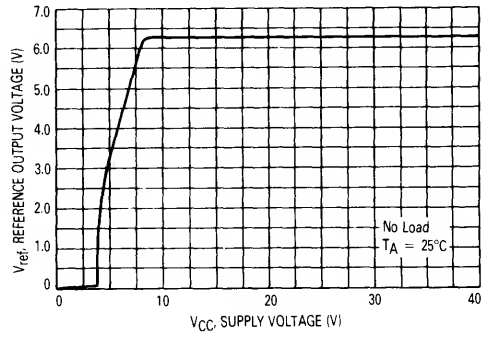
To Drive Output Sink Saturation ($I_{sink} = 25\text{ mA}$)	$V_{CE(sat)}$	—	0.5	1.5	V
Top Drive Output Off-State Leakage ($V_{CE} = 30\text{ V}$)	$I_{DRV(leak)}$	—	0.06	100	μA
Top Drive Output Switching Time ($C_L = 47\text{ pF}$, $R_L = 1.0\text{ k}$)					ns
Rise Time	t_r	—	107	300	
Fall Time	t_f	—	26	300	
Bottom Drive Output Voltage					V
High State ($V_{CC} = 30\text{ V}$, $I_{source} = 50\text{ mA}$)	V_{OH}	($V_{CC} - 2.0$)	($V_{CC} - 1.1$)	—	
Low State ($V_{CC} = 30\text{ V}$, $I_{sink} = 50\text{ mA}$)	V_{OL}	—	1.5	2.0	
Bottom Drive Output Switching Time ($C_L = 1000\text{ pF}$)					ns
Rise Time	t_r	—	38	200	
Fall Time	t_f	—	30	200	
Under Voltage Lockout					V
Drive Output Enabled (V_{CC} Increasing)	$V_{th(on)}$	8.2	8.9	10	
Hysteresis	V_H	0.1	0.2	0.3	
Power Supply Current	I_{CC}	—	15	22	mA

FIGURE 1 — OSCILLATOR FREQUENCY versus TIMING RESISTOR

FIGURE 2 — OSCILLATOR FREQUENCY CHANGE versus TEMPERATURE

FIGURE 3 — ERROR AMP OPEN-LOOP GAIN AND PHASE versus FREQUENCY

FIGURE 4 — ERROR AMP OUTPUT SATURATION VOLTAGE versus LOAD CURRENT

FIGURE 5 — ERROR AMP SMALL-SIGNAL TRANSIENT RESPONSE

FIGURE 6 — ERROR AMP LARGE-SIGNAL TRANSIENT RESPONSE


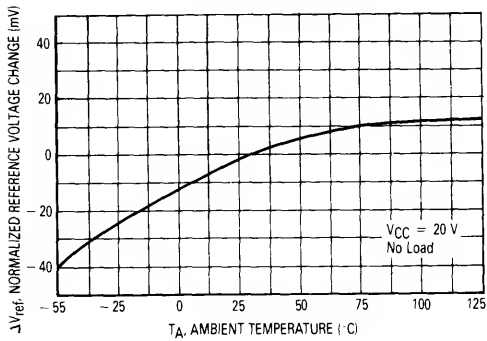
**FIGURE 7 — REFERENCE OUTPUT VOLTAGE CHANGE
versus OUTPUT SOURCE CURRENT**



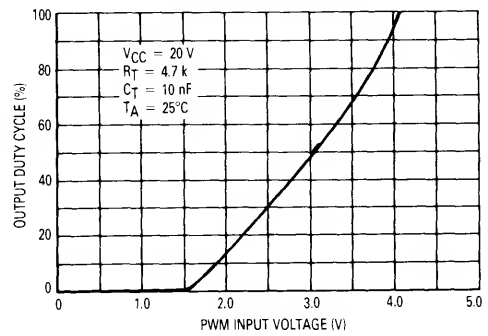
**FIGURE 8 — REFERENCE OUTPUT VOLTAGE
versus SUPPLY VOLTAGE**



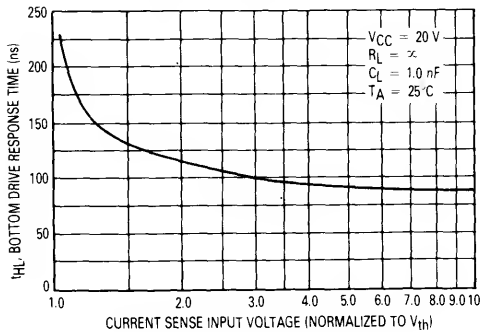
**FIGURE 9 — REFERENCE OUTPUT VOLTAGE
versus TEMPERATURE**



**FIGURE 10 — OUTPUT DUTY CYCLE versus
PWM INPUT VOLTAGE**



**FIGURE 11 — BOTTOM DRIVE RESPONSE TIME versus
CURRENT SENSE INPUT VOLTAGE**



**FIGURE 12 — TOP DRIVE OUTPUT SATURATION
VOLTAGE versus SINK CURRENT**

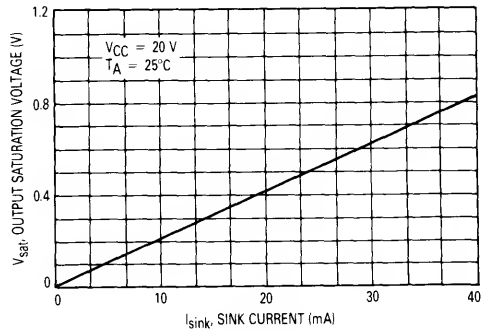


FIGURE 13 — TOP DRIVE OUTPUT WAVEFORM

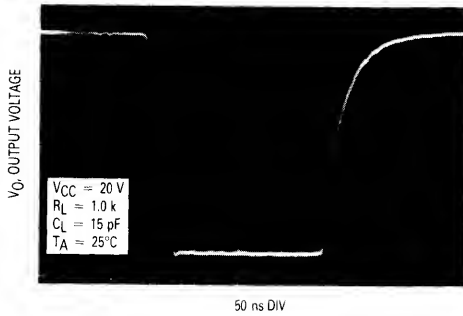


FIGURE 14 — BOTTOM DRIVE OUTPUT WAVEFORM

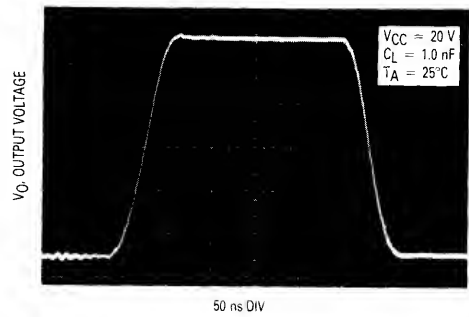


FIGURE 15 — BOTTOM DRIVE OUTPUT WAVEFORM

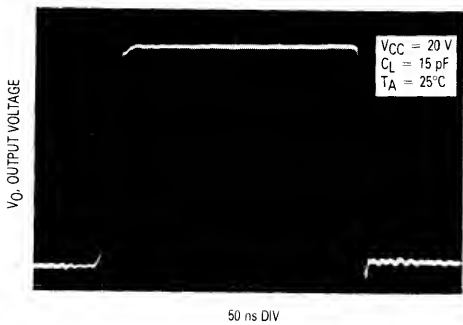


FIGURE 16 — BOTTOM DRIVE OUTPUT SATURATION VOLTAGE versus LOAD CURRENT

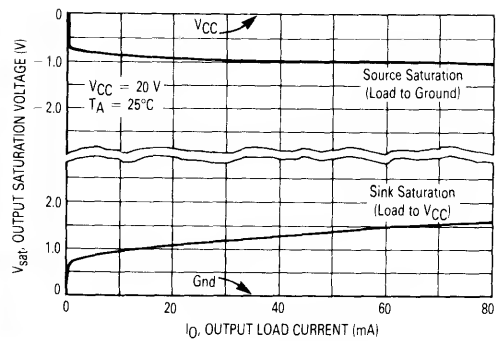
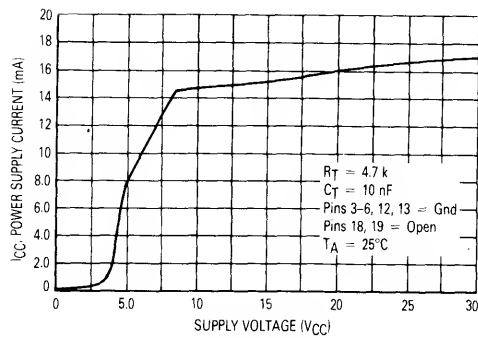


FIGURE 17 — SUPPLY CURRENT versus VOLTAGE



PIN FUNCTION DESCRIPTION

Pin No.	Function	Description
1, 2, 20	B _T , A _T , C _T	These three open collector Top Drive Outputs are designed to drive the external upper power switch transistors.
3	FWD/REV	The Forward/Reverse Input is used to change the direction of motor rotation.
4, 5, 6	S _A , S _B , S _C	These three Sensor Inputs control the commutation sequence.
7	Reference Output	This output provides charging current for the oscillator timing capacitor C _T and a reference for the error amplifier. It may also serve to furnish sensor power.
8	Oscillator	The Oscillator frequency is programmed by the values selected for the timing components, R _T and C _T .
9	Error Amp (Noninverting Input)	This input is normally connected to the speed set potentiometer.
10	Error Amp (Inverting Input)	This input is normally connected to the Error Amp Output in open-loop applications.
11	Error Amp Output/PWM Input	This pin is available for compensation in closed-loop applications.
12	Current Sense (Noninverting Input)	A 100 mV signal, with respect to Pin 13, at this input terminates output switch conduction during a given oscillator cycle. This pin normally connects to the top side of the current sense resistor.
13	Ground	This pin supplies a separate ground return for the control circuit and should be referenced back to the power source ground.
14	V _{CC}	This pin is the positive supply of the control IC. The controller is functional over a V _{CC} range of 10 V to 30 V.
15, 16, 17	C _B , B _B , A _B	These three totem pole Bottom Drive Outputs are designed for direct drive of the external bottom power switch transistors.
18	60°/120° Select	The electrical state of this pin configures the control circuit operation for either 60° (high state) or 120° (low state) sensor electrical phasing inputs.
19	Output Enable	A logic high at this input causes the motor to run, while a low causes it to coast.

INTRODUCTION

The MC33033 is one of a series of high performance monolithic DC brushless motor controllers produced by Motorola. It contains all of the functions required to implement a limited-feature, open-loop, three or four phase motor control system. Constructed with Bipolar Analog technology, it offers a high degree of performance and ruggedness in hostile industrial environments. The MC33033 contains a rotor position decoder for proper commutation sequencing, a temperature compensated reference capable of supplying sensor power, a frequency programmable sawtooth oscillator, a fully accessible error amplifier, a pulse width modulator comparator, three open collector top drive outputs, and three high current totem pole bottom driver outputs ideally suited for driving power MOSFETs.

Included in the MC33033 are protective features consisting of undervoltage lockout, cycle by cycle current limiting with a latched shutdown mode, and internal thermal shutdown.

Typical motor control functions include open-loop speed control, forward or reverse rotation, and run enable. In addition, the MC33033 has a 60°/120° select pin which configures the rotor position decoder for either 60° or 120° sensor electrical phasing inputs.

FUNCTIONAL DESCRIPTION

A representative internal block diagram is shown in Figure 18, with various applications shown in Figures 34, 36, 37, 41, 43, and 44. A discussion of the features and function of each of the internal blocks given below and referenced to Figures 18 and 36.

Rotor Position Decoder

An internal rotor position decoder monitors the three sensor inputs (Pins 4, 5, 6) to provide the proper sequencing of the top and bottom drive outputs. The sensor inputs are designed to interface directly with open collector type Hall Effect switches or opto slotted couplers. Internal pull-up resistors are included to minimize the required number of external components. The inputs are TTL compatible, with their thresholds typically at 2.2 volts. The MC33033 series is designed to control three phase motors and operate with four of the most common conventions of sensor phasing. A 60°/120° select (Pin 18) is conveniently provided which affords the MC33033 to configure itself to control motors having either 60°, 120°, 240° or 300° electrical sensor phasing. With three sensor inputs there are eight possible input code combinations, six of which are valid rotor positions. The remaining two codes are invalid and are usually caused by an open or shorted sensor line. With six valid input codes, the decoder can resolve the motor rotor position to within a window of 60 electrical degrees.

The forward/reverse input (Pin 3) is used to change the direction of motor rotation by reversing the voltage across the stator winding. When the input changes state, from high to low with a given sensor input code (for example 100), the enabled top and bottom drive outputs with the same alpha designation are exchanged

(A_T to A_B, B_T to B_B, C_T to C_B). In effect the commutation sequence is reversed and the motor changes directional rotation.

Motor on/off control is accomplished by the output enable (Pin 19). When left disconnected, an internal pull-up resistor to a positive source, enables sequencing of the top and bottom drive outputs. When grounded, the top drive outputs turn off and the bottom drives are forced low, causing the motor to coast.

The commutation logic truth table is shown in Figure 19. In half wave motor drive applications, the top drive outputs are not required and are typically left disconnected.

Error Amplifier

A high performance, fully compensated error amplifier with access to both inputs and output (Pins 9, 10, 11) is provided to facilitate the implementation of closed-loop motor speed control. The amplifier features a typical DC voltage gain of 80 dB, 0.6 MHz gain bandwidth, and a wide input common mode voltage range that extends from ground to V_{ref}. In most open-loop speed control applications, the amplifier is configured as a unity gain voltage follower with the non-inverting input connected to the speed set voltage source. Additional configurations are shown in Figures 29 through 33.

Oscillator

The frequency of the internal ramp oscillator is programmed by the values selected for timing components R_T and C_T. Capacitor C_T is charged from the reference output (Pin 7) through resistor R_T and discharged by an internal discharge transistor. The ramp peak and valley voltages are typically 4.1 V and 1.5 V respectively. To provide a good compromise between audible noise and output switching efficiency, an oscillator frequency in the range of 20 kHz to 30 kHz is recommended. Refer to Figure 1 for component selection.

Pulse Width Modulator

The use of pulse width modulation provides an energy efficient method of controlling the motor speed by varying the average voltage applied to each stator winding during the commutation sequence. As C_T discharges, the oscillator sets both latches, allowing conduction of the top and bottom drive outputs. The PWM comparator resets the upper latch, terminating the bottom drive output conduction when the positive-going ramp of C_T becomes greater than the error amplifier output. The pulse width modulator timing diagram is shown in Figure 20. Pulse width modulation for speed control appears only at the bottom drive outputs.

Current Limit

Continuous operation of a motor that is severely overloaded results in overheating and eventual failure. This destructive condition can best be prevented with the use of cycle-by-cycle current limiting. That is, each on-cycle is treated as a separate event. Cycle-by-cycle current limiting is accomplished by monitoring the stator

4

Inputs (Note 2)									Outputs (Note 3)							
Sensor Electrical Phasing (Note 4)									Top Drives			Bottom Drives				
S _A	60° S _B	S _C	S _A	120° S _B	S _C				F/R	Enable	Current Sense	A _T	B _T	C _T		A _B
1	0	0	1	0	0	1	1	0	0	1	1	0	0	0	1	(Note 5) F/R = 1
1	1	0	1	1	0	1	1	0	1	0	1	0	0	0	1	
1	1	1	0	1	0	1	1	0	1	0	1	1	0	0	0	
0	1	1	0	1	1	1	1	0	1	1	0	1	0	0	0	
0	0	1	0	0	1	1	1	0	1	1	0	0	1	0	0	
0	0	0	1	0	0	1	1	0	0	1	1	0	1	1	0	
0	0	0	1	0	1	1	1	0	0	1	1	0	1	1	0	
1	0	0	1	0	0	0	1	0	1	1	0	1	0	0	0	(Note 5) F/R = 0
1	1	0	1	1	0	0	1	0	1	1	0	0	1	0	0	
1	1	1	0	1	0	0	1	0	0	1	1	0	1	0	0	
0	1	1	0	1	1	0	1	0	0	1	1	0	0	0	1	
0	0	1	0	0	1	0	1	0	1	0	1	0	0	0	1	
0	0	0	1	0	0	0	1	0	1	0	1	0	0	1	0	
0	0	0	1	0	1	0	1	0	1	0	1	1	0	0	0	
1	0	1	1	1	1	X	X	X	1	1	1	0	0	0	0	(Note 6)
0	1	0	0	0	0	X	X	X	1	1	1	0	0	0	0	
V	V	V	V	V	V	X	0	X	1	1	1	0	0	0	0	(Note 7)
V	V	V	V	V	V	X	1	1	1	1	1	0	0	0	0	(Note 8)

1. V = Any one of six valid sensor or drive combinations.
X = Don't care.
2. The digital inputs (Pins 3, 4, 5, 6, 18, 19) are all TTL compatible. The current sense input (Pin 12) has a 100 mV threshold with respect to Pin 13.
A logic 0 for this input is defined as < 85 mV, and a logic 1 is > 115 mV.
3. The top drive outputs are open collector design and active in the low (0) state.
4. With 60°/120° select (Pin 18) in the high (1) state, configuration is for 60° sensor electrical phasing inputs. With Pin 18 in the low (0) state, configuration is for 120° sensor electrical phasing inputs.
5. Valid 60° or 120° sensor combinations for corresponding valid top and bottom drive outputs.
6. Invalid sensor inputs; All top and bottom drives are off.
7. Valid sensor inputs with enable = 0; All top and bottom drives are off.
8. Valid sensor inputs with enable and current sense = 1; All top and bottom drives are off.

current build-up each time an output switch conducts, and upon sensing an over current condition, immediately turning off the switch and holding it off for the remaining duration of the oscillator ramp-up period. The stator current is converted to a voltage by inserting a ground-referenced sense resistor R_S (Figure 34) in series with the three bottom switch transistors (Q4, Q5, Q6). The voltage developed across the sense resistor is monitored by the current sense input (Pin 12), and compared to the internal 100 mV reference. If the current sense threshold is exceeded, the comparator resets the lower latch and terminates output switch conduction. The value for the sense resistor is:

$$R_S = \frac{0.1}{I_{\text{stator(max)}}$$

The dual-latch PWM configuration ensures that only one single output conduction pulse occurs during any given oscillator cycle, whether terminated by the output of the error amp or the current limit comparator.

Reference

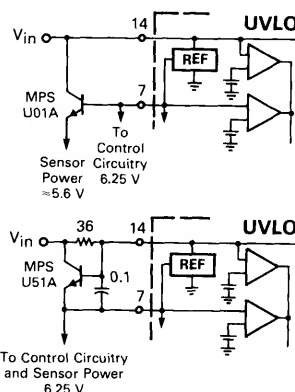
The on-chip 6.25 V regulator (Pin 7) provides charging current for the oscillator timing capacitor, a reference for the error amplifier, and can supply 20 mA of current suitable for directly powering sensors in low voltage applications. In higher voltage applications it may become necessary to transfer the power dissipated by the regulator off the IC. This is easily accomplished with the addition of an external pass transistor as shown in Figure 21. A 6.25 V reference level was chosen to allow implementation of the simpler NPN circuit, where $V_{\text{ref}} - V_{\text{BE}}$ exceeds the minimum voltage required by Hall Effect sensors over temperature. With proper transistor selection, and adequate heatsinking, up to one amp of load current can be obtained.

Undervoltage Lockout

A dual Undervoltage Lockout has been incorporated to prevent damage to the IC and the external power switch transistors. Under low power supply conditions,

it guarantees that the IC and sensors are fully functional, and that there is sufficient bottom drive output voltage. The positive power supply to the IC (V_{CC}) is monitored to a threshold of 8.9 V. This level ensures sufficient gate drive necessary to attain low $r_{\text{DS(on)}}$ when interfacing with standard power MOSFET devices. When directly powering the Hall sensors from the reference, improper sensor operation can result if the reference output voltage should fall below 4.5 V. If one or both of the comparators detects an undervoltage condition, the top drives are turned off and the bottom drive outputs are held in a low state. Each of the comparators contain hysteresis to prevent oscillations when crossing their respective thresholds.

FIGURE 21 — REFERENCE OUTPUT BUFFERS



The NPN circuit is recommended for powering Hall or opto sensors, where the output voltage temperature coefficient is not critical. The PNP circuit is slightly more complex, but also more accurate. Neither circuit has current limiting.

FIGURE 20 — PWM TIMING DIAGRAM

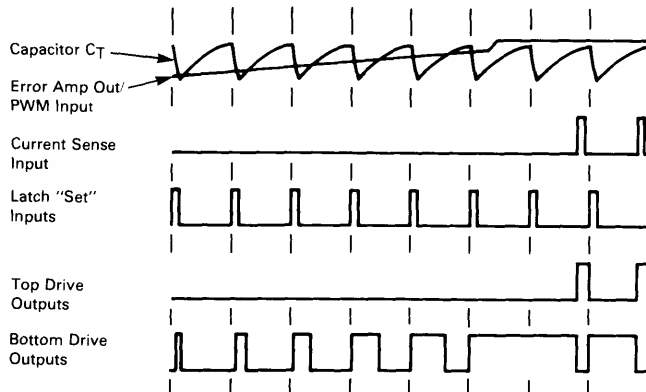
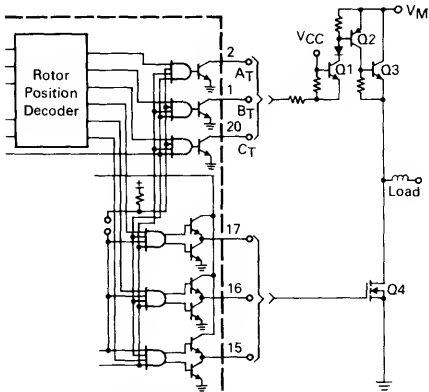
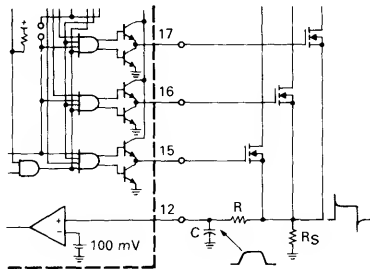


FIGURE 22 — HIGH VOLTAGE INTERFACE WITH NPN POWER TRANSISTORS



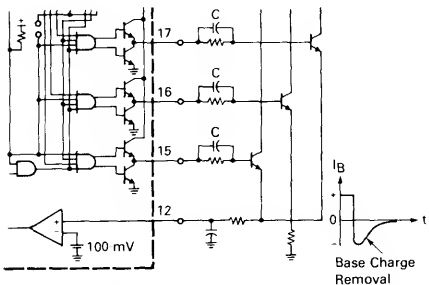
Transistor Q1 is a common base stage used to level shift from V_{CC} to the high motor voltage, V_M . The collector diode is required if V_{CC} is present while V_M is low.

FIGURE 24 — CURRENT WAVEFORM SPIKE SUPPRESSION



The addition of the RC filter will eliminate current-limit instability caused by the leading edge spike on the current waveform. Resistor R_S should be a low inductance type.

FIGURE 26 — BIPOLAR TRANSISTOR DRIVE



The totem pole output can furnish negative base current for enhanced transistor turn-off, with the addition of capacitor C.

FIGURE 23 — HIGH VOLTAGE INTERFACE WITH 'N' CHANNEL POWER MOSFETS

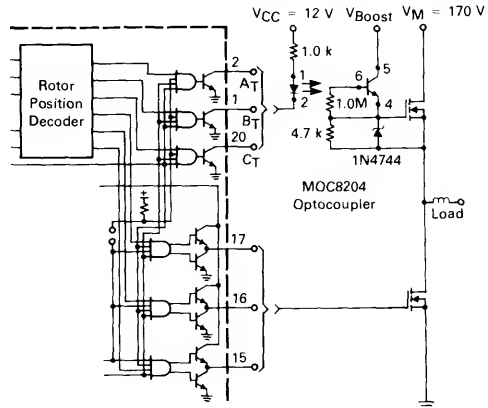
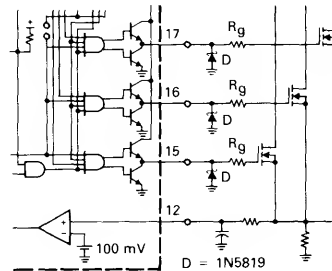
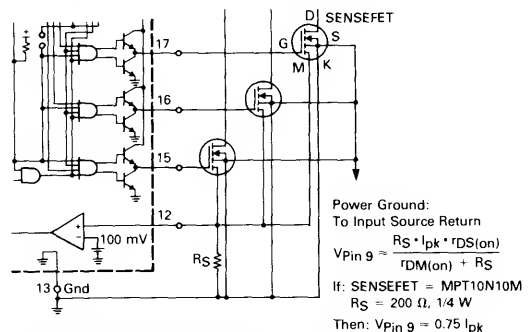


FIGURE 25 — MOSFET DRIVE PRECAUTIONS



Series gate resistor R_g will damp any high frequency oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate-source circuit. Diode D is required if the negative current into the Bottom Drive Outputs exceeds 50 mA.

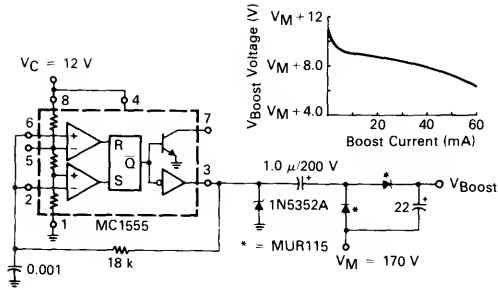
FIGURE 27 — CURRENT SENSING POWER MOSFETS



Power Ground:
To Input Source Return
 $V_{pin9} \approx \frac{R_S \cdot I_{pk} \cdot f_{DS(on)}}{f_{DM(on)} + R_S}$
If: SENSEFET = MPT10N10M
 $R_S = 200 \Omega, 1/4 W$
Then: $V_{pin9} = 0.75 I_{pk}$

Virtually lossless current sensing can be achieved with the implementation of SENSEFET power switches.

FIGURE 28 — HIGH VOLTAGE BOOST SUPPLY



This circuit generates V_{Boost} for Figure 23.

FIGURE 29 — DIFFERENTIAL INPUT SPEED CONTROLLER

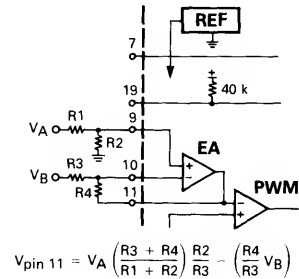
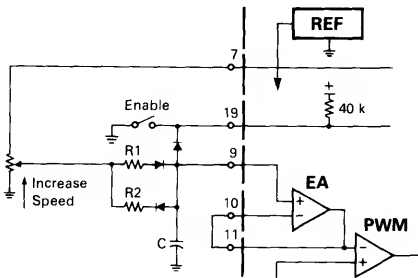
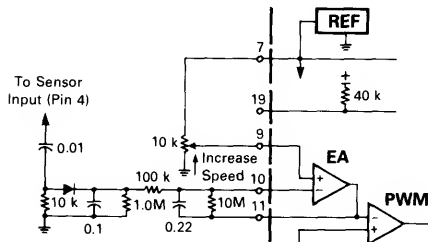


FIGURE 30 — CONTROLLED ACCELERATION/DECELERATION



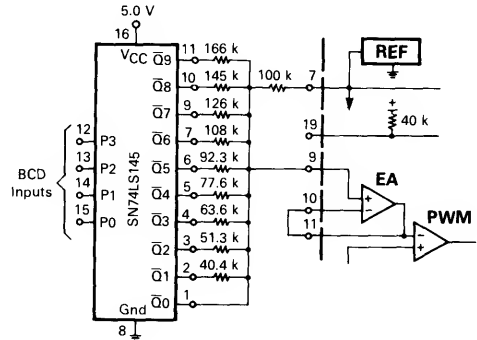
Resistor R1 with capacitor C sets the acceleration time constant while R2 controls the deceleration. The values of R1 and R2 should be at least ten times greater than the speed set potentiometer to minimize time constant variations with different speed settings.

FIGURE 32 — CLOSED LOOP SPEED CONTROL



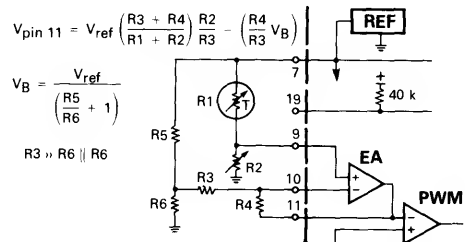
The rotor position sensors can be used as a tachometer. By differentiating the positive-going edges and then integrating them over time, a voltage proportional to speed can be generated. The error amp compares this voltage to that of the speed set to control the PWM.

FIGURE 31 — DIGITAL SPEED CONTROLLER



The SN74LS145 is an open collector BCD to One of Ten decoder. When connected as shown, input codes 0000 through 1001 steps the PWM in increments of approximately 10% from 0 to 90% on-time. Input codes 1010 through 1111 will produce 100% on-time or full motor speed.

FIGURE 33 — CLOSED LOOP TEMPERATURE CONTROL



This circuit can control the speed of a cooling fan proportional to the difference between the sensor and set temperatures. The control loop is closed as the forced air cools the NTC thermistor. For controlled heating applications, exchange the positions of R1 and R2.

Drive Outputs

The three top drive outputs (Pins 1, 2, 20) are open collector NPN transistors capable of sinking 50 mA with a minimum breakdown of 30 volts. Interfacing into higher voltage applications is easily accomplished with the circuits shown in Figures 22 and 23.

The three totem pole bottom drive outputs (Pins 15, 16, 17) are particularly suited for direct drive of 'N' channel MOSFETs or NPN bipolar transistors (Figures 24, 25, 26 and 27). Each output is capable of sourcing and sinking up to 100 mA.

Thermal Shutdown

Internal thermal shutdown circuitry is provided to protect the IC in the event the maximum junction temperature is exceeded. When activated, typically at 170°C, the IC acts as though the regulator was disabled, in turn shutting down the IC.

SYSTEM APPLICATIONS

Three Phase Motor Commutation

The three phase application shown in Figure 34 is an open-loop motor controller with full wave, six step drive. The upper power switch transistors are Darling-

ton PNP's while the lower switches are 'N' channel power MOSFETs. Each of these devices contains an internal parasitic catch diode that is used to return the stator inductive energy back to the power supply. The outputs are capable of driving a delta or wye connected stator, and a grounded neutral wye if split supplies are used. At any given rotor position, only one top and one bottom power switch (of different totem poles) is enabled. This configuration switches both ends of the stator winding from supply to ground which causes the current flow to be bidirectional or full wave. A leading edge spike is usually present on the current waveform and can cause a current-limit error. The spike can be eliminated by adding an RC filter in series with the current sense input. Using a low inductance type resistor for R_S will also aid in spike reduction. Figure 35 shows the commutation waveforms over two electrical cycles. The first cycle (0° to 360°) depicts motor operation at full speed while the second cycle (360° to 720°) shows a reduced speed with about 50 percent pulse width modulation. The current waveforms reflect a constant torque load and are shown synchronous to the commutation frequency for clarity.

FIGURE 34 — THREE PHASE, SIX STEP, FULL WAVE MOTOR CONTROLLER

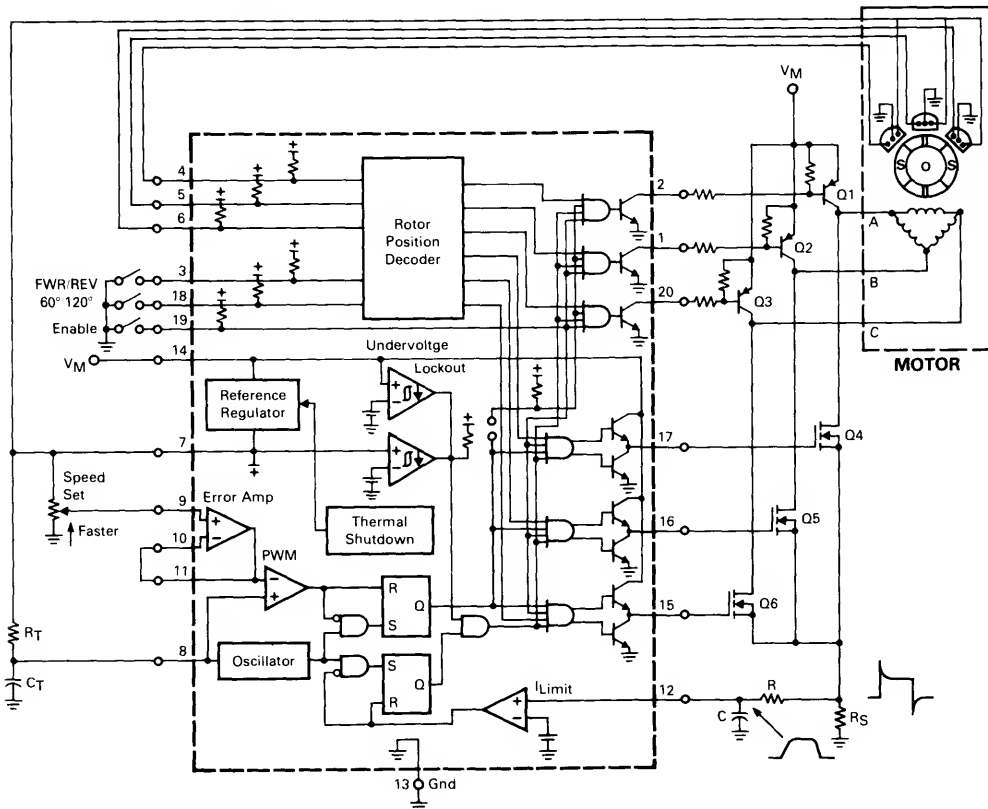


FIGURE 35 — THREE PHASE, SIX STEP, FULL WAVE COMMUTATION WAVEFORMS

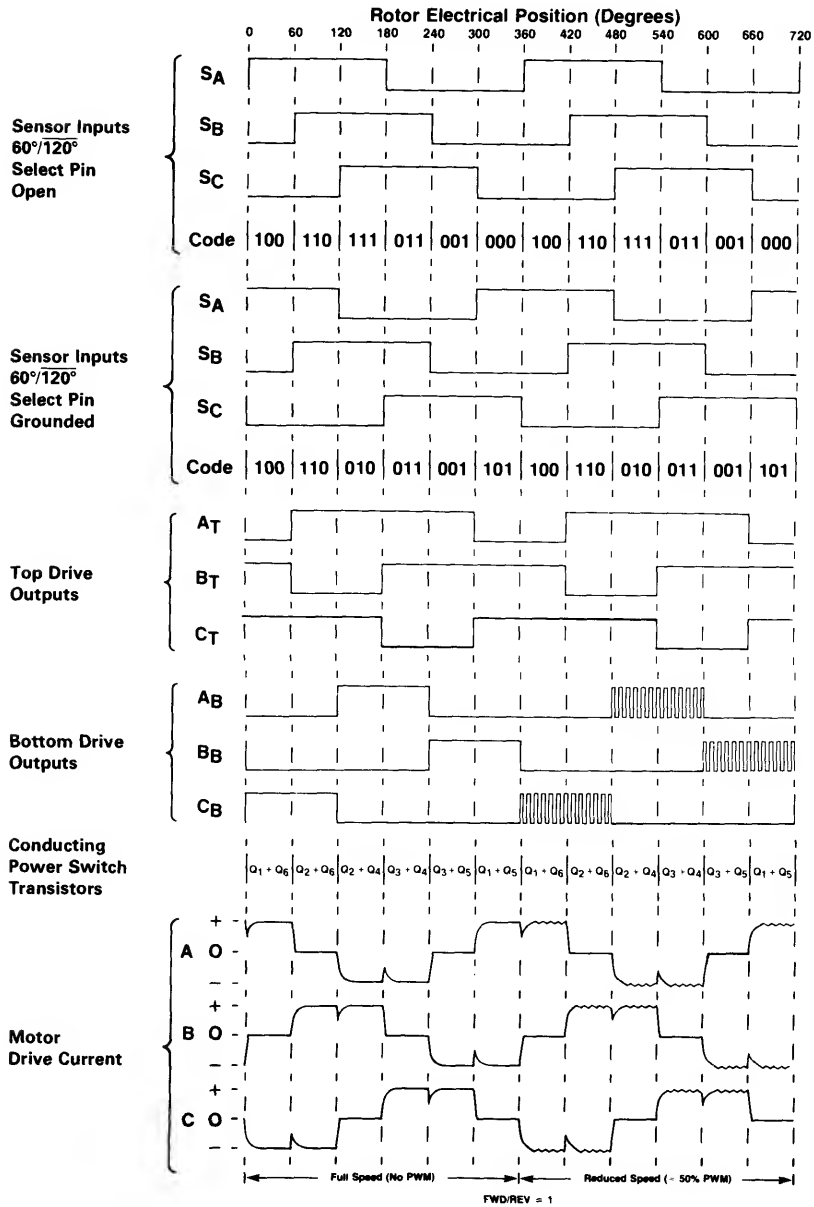
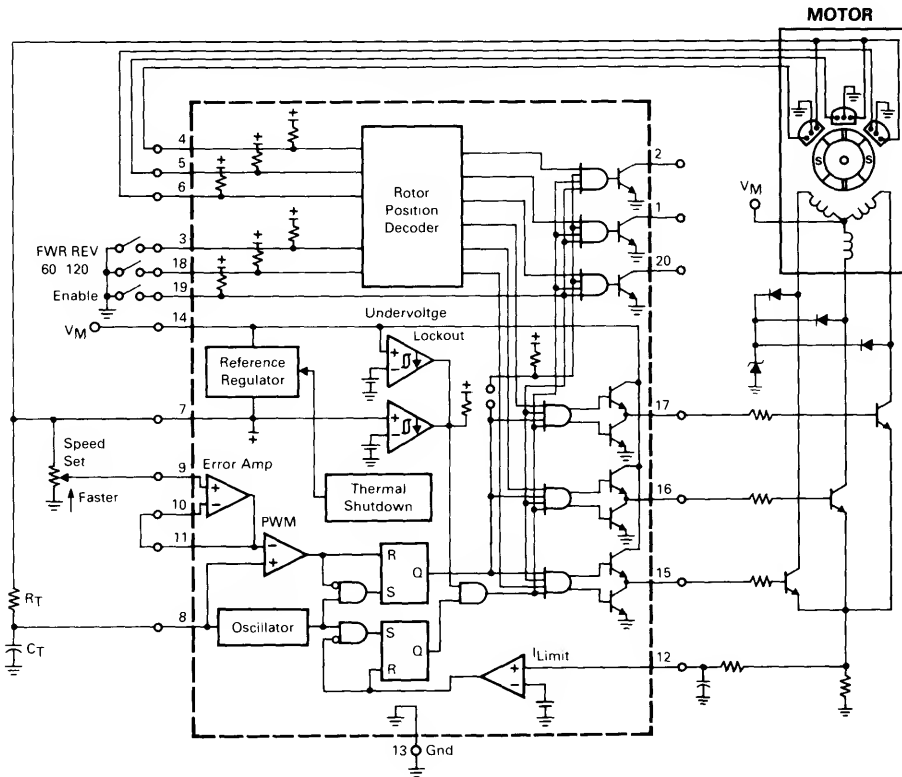


Figure 36 shows a three phase, three step, half wave motor controller. This configuration is ideally suited for automobile and other low voltage applications since there is only one power switch voltage drop in series

with a given stator winding. Current flow is unidirectional or half wave because only one end of each winding is switched. The stator flyback voltage is clamped by a single zener and three diodes.

FIGURE 36 — THREE PHASE, THREE STEP, HALF WAVE MOTOR CONTROLLER



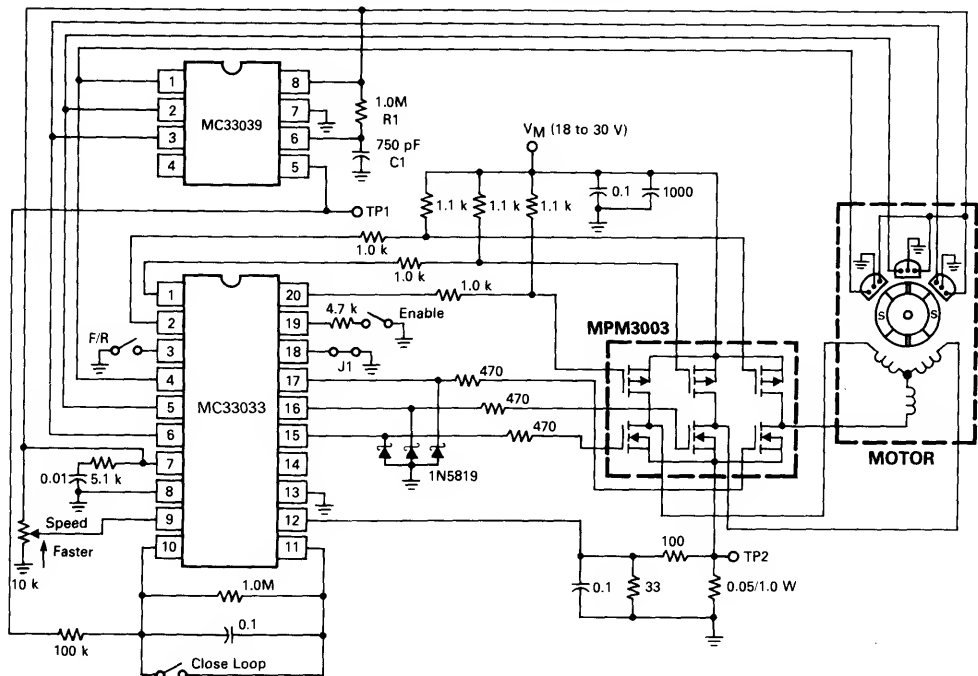
Three Phase Closed Loop Controller

The MC33033, by itself, is capable of open loop motor speed control. For closed loop speed control, the MC33033 requires an input voltage proportional to the motor speed. Traditionally this has been accomplished by means of a tachometer to generate the motor speed feedback voltage. Figure 37 shows an application whereby an MC33039, powered from the 6.25 volt reference (Pin 7) of the MC33033, is used to generate the required feedback voltage without the need of a costly tachometer. The same Hall sensor signals used by the MC33033 for rotor position decoding are utilized by the MC33039. Every positive or negative going transition of the Hall sensor signals on any of the sensor lines causes the MC33039 to produce an output pulse of defined amplitude and time duration, as determined by the external resistor R1 and capacitor C1. The resulting out-

put train of pulses present at Pin 5 of the MC33039 are integrated by the error amplifier of the MC33033 configured as an integrator, to produce a DC voltage level which is proportional to the motor speed. This speed proportional voltage establishes the PWM reference level at Pin 11 of the MC33033 motor controller and completes or closes the feedback loop. The MC33033 outputs drive an MPM3003 T MOS power MOSFET 3-phase bridge circuit which is capable of delivering up to 25 Amperes of surge current. High current can be expected during conditions of start-up and when changing direction of the motor.

The system shown in Figure 37 is designed for a motor having 120/240 degrees Hall sensor electrical phasing. The system can easily be modified to accommodate 60/300 degree Hall sensor electrical phasing by removing the jumper (J1) at Pin 18 of the MC33033.

FIGURE 37 — CLOSED LOOP BRUSHLESS DC MOTOR CONTROL WITH THE MC33033 USING THE MC33039 AND MC33033



Sensor Phasing Comparison

There are four conventions used to establish the relative phasing of the sensor signals in three phase motors. With six step drive, an input signal change must occur every 60 electrical degrees, however, the relative signal phasing is dependent upon the mechanical sensor placement. A comparison of the conventions in electrical degrees is shown in Figure 38. From the sensor phasing table (Figure 39), note that the order of input codes for 60° phasing is the reverse of 300°. This means the MC33033, when the 60°/120° select (Pin 18) and the FWD/REV (Pin 3) both in the high state (open), is configured to operate a 60° sensor phasing motor in the forward direction. Under the same conditions a 300° sensor phasing motor would operate equally well but in the reverse direction. One would simply have to reverse the FWD/REV switch (FWD/REV closed) in order to cause the 300° motor to also operate in the same direction. The same difference exists between the 120° and 240° conventions.

FIGURE 38 — SENSOR PHASING COMPARISON

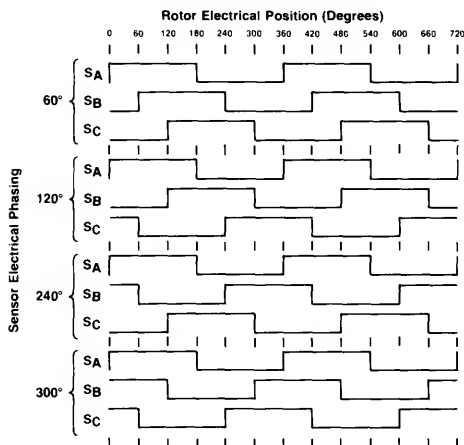


FIGURE 39 — SENSOR PHASING TABLE

Sensor Electrical Phasing (Degrees)											
60°			120°			240°			300°		
SA	SB	SC	SA	SB	SC	SA	SB	SC	SA	SB	SC
1	0	0	1	0	1	1	1	0	1	1	1
1	1	0	1	0	0	1	0	0	1	1	0
1	1	1	1	1	0	1	0	1	1	0	0
0	1	1	0	1	0	0	0	1	0	0	0
0	0	1	0	1	1	0	1	1	0	0	1
0	0	0	0	0	1	0	1	0	0	1	1

In this data sheet, the rotor position has always been given in electrical degrees since the mechanical position is a function of the number of rotating magnetic poles. The relationship between the electrical and mechanical position is:

$$\text{Electrical Degrees} = \text{Mechanical Degrees} \left(\frac{\text{\#Rotor Poles}}{2} \right)$$

An increase in the number of magnetic poles causes more electrical revolutions for a given mechanical revolution. General purpose three phase motors typically contain a four pole rotor which yields two electrical revolutions for one mechanical.

Two and Four Phase Motor Commutation

The MC33033 configured for 60° sensor inputs is capable of providing a four step output that can be used to drive two or four phase motors. The truth table in Figure 40 shows that by connecting sensor inputs SB and SC together, it is possible to truncate the number of drive output states from six to four. The output power switches are connected to BT, CT, BB, and CB. Figure 41 shows a four phase, four step, full wave motor control application. Power switch transistors Q1 through Q8 are Darlington type, each with an internal parasitic catch diode. With four step drive, only two rotor position sensors spaced at 90 electrical degrees are required. The commutation waveforms are shown in Figure 42.

Figure 43 shows a four phase, four step, half wave motor controller. It has the same features as the circuit in Figure 36, except for the deletion of speed adjust.

FIGURE 40 — TWO AND FOUR PHASE, FOUR STEP, COMMUTATION TRUTH TABLE

MC33033 (60°/120° Select Pin Open)						
Inputs			Outputs			
Sensor Electrical Spacing* = 90°	SA	SB	F/R	Top Drives	Bottom Drives	
				BT	CT	BB CB
1	0	1	1	1	1	0 1
1	1	1	0	1	0	0 0
0	1	1	1	1	0	0 0
0	0	1	1	1	1	1 0
1	0	0	0	1	0	0 0
1	1	0	1	1	1	1 0
0	1	0	1	1	0	0 1
0	0	0	0	0	1	0 0

*With MC33033 sensor input SB connected to SC

FIGURE 41 — FOUR PHASE, FOUR STEP, FULL WAVE CONTROLLER

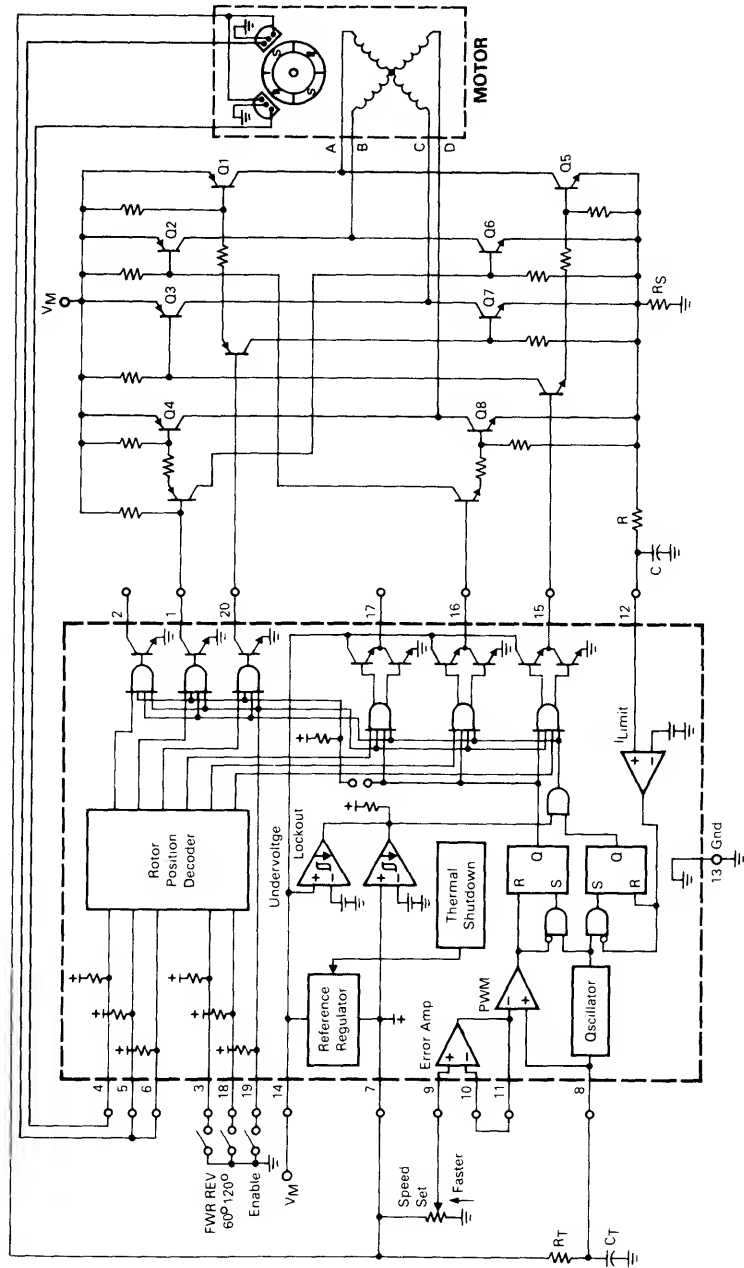


FIGURE 42 — FOUR PHASE, FOUR STEP, FULL WAVE COMMUTATION WAVEFORMS

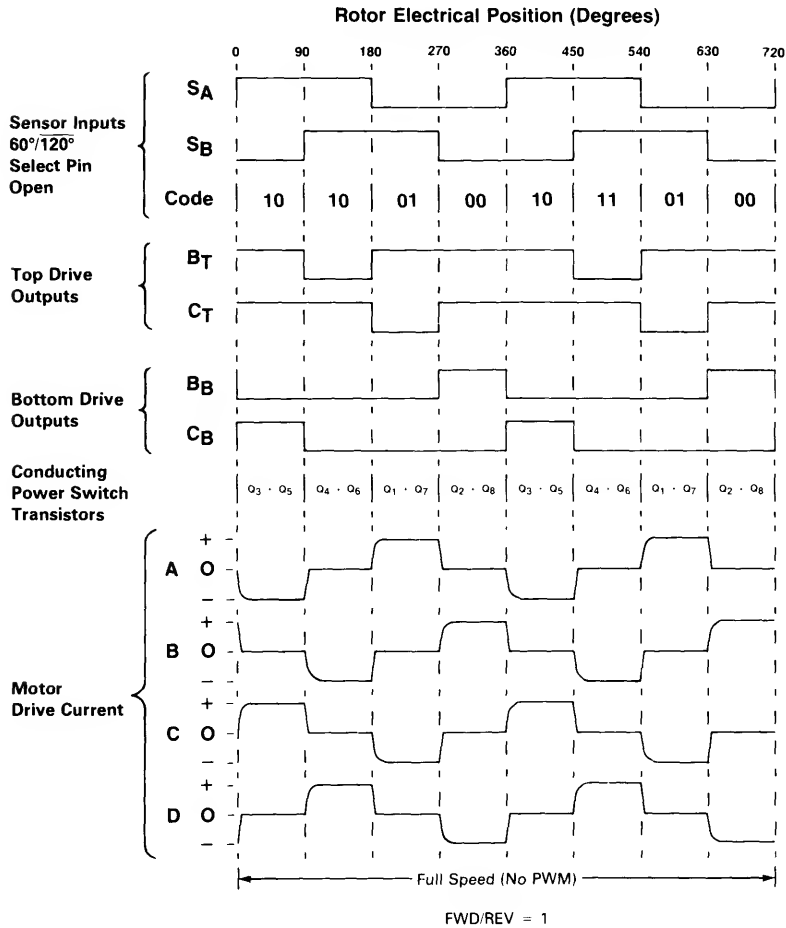
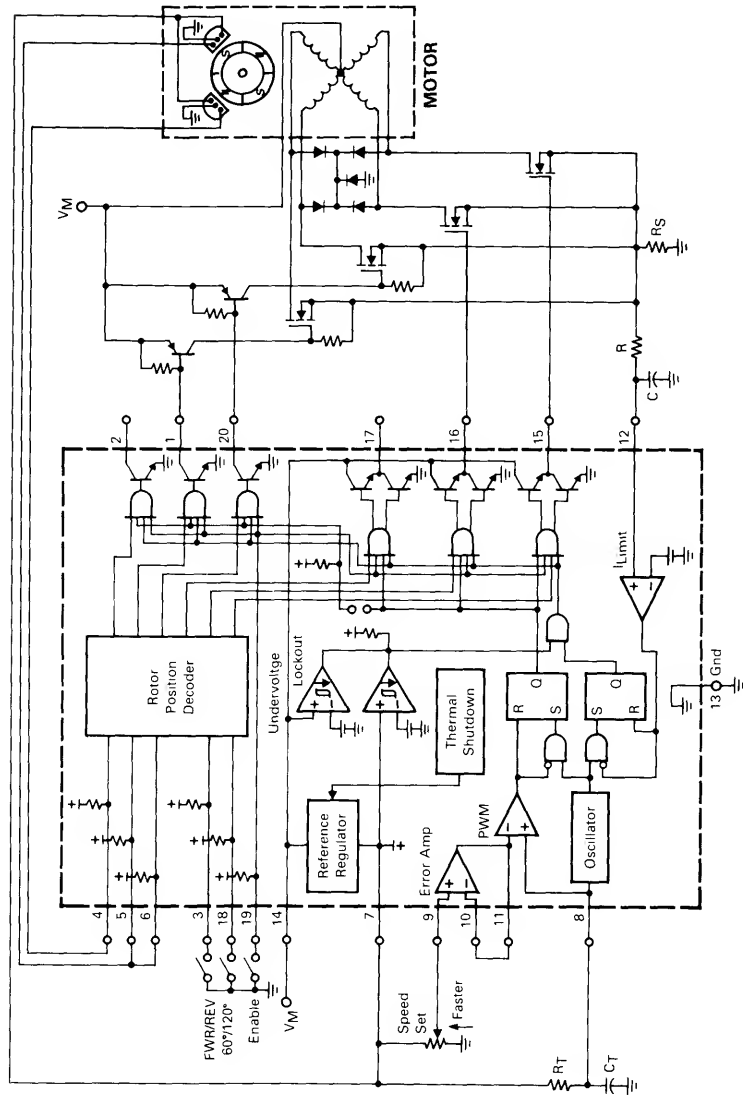


FIGURE 43 — FOUR PHASE, FOUR STEP, HALF WAVE MOTOR CONTROLLER

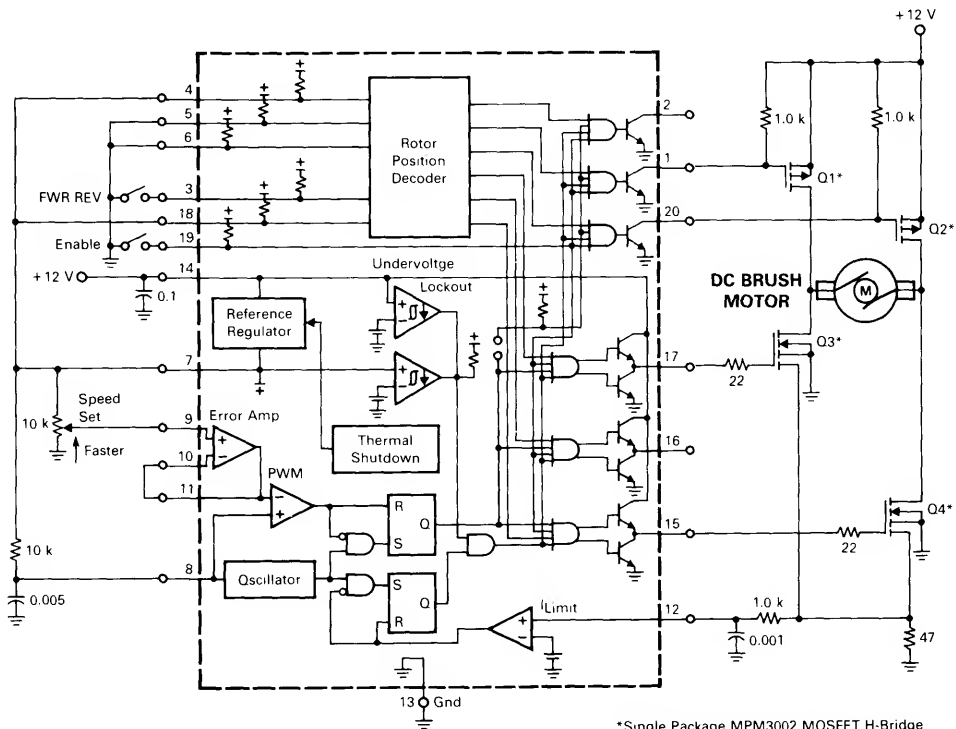


Brush Motor Control

Though the MC33033 was designed to control brushless DC motors, it may also be used to control DC brush-type motors. Figure 44 shows an application of the MC33033 driving a Motorola MPM3002 H-bridge affording minimal parts count to operate a one-tenth horsepower brush-type motor. Key to the operation is the input sensor code [100] which produces a top-left (Q1) and a bottom-right (Q4) drive when the controller's forward/reverse pin is at logic [1]; top-right (Q2), bottom-left (Q3) drive is realized when the forward/reverse pin is at logic [0]. This code supports the requirements necessary for H-bridge drive accomplishing both direction and speed control.

The controller functions in a normal manner with a pulse-width-modulated frequency of approximately 25 kHz. Motor speed is controlled by adjusting the voltage presented to the non-inverting input of the error amplifier establishing the PWM's slice or reference level. Cycle-by-cycle current limiting of 3.0 amperes motor current is accomplished by sensing the voltage (100 mV threshold) across the 47 Ohm resistor to ground of the H-bridge motor current. The over current sense circuit makes it possible to reverse the direction of the motor, on the fly, using the normal forward/reverse switch, and not have to completely stop before reversing.

FIGURE 44 — H-BRIDGE BRUSH-TYPE CONTROLLER



*Single Package MPM3002 MOSFET H-Bridge
M = 1/10th horsepower DC brush-type motor

LAYOUT CONSIDERATIONS

Do not attempt to construct any of the motor control circuits on wire-wrap or plug-in prototype boards. High frequency printed circuit layout techniques are imperative to prevent pulse jitter. This is usually caused by excessive noise pick-up imposed on the current sense or error amp inputs. The printed circuit layout should contain a ground plane with low current signal and high drive and output buffer grounds returning on separate

paths back to the power supply input filter capacitor V_M . Ceramic bypass capacitors (0.01 μF) connected close to the integrated circuit at V_{CC} , V_{ref} and error amplifier non-inverting input may be required depending upon circuit layout. This provides a low impedance path for filtering any high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI.

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

4

BRUSHLESS DC MOTOR CONTROLLER

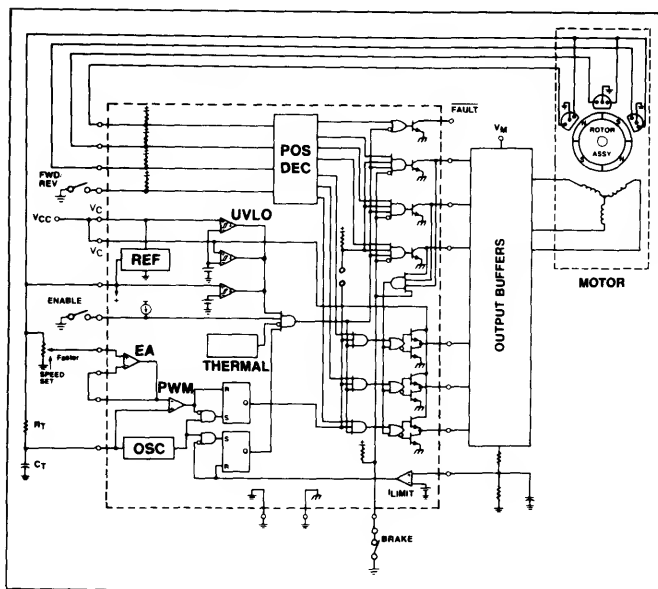
The MC33034 series is a high performance monolithic brushless motor controller containing all of the active functions required to implement a full featured open-loop three or four phase motor control system. These devices consist of a rotor position decoder for proper commutation sequencing, temperature compensated reference capable of supplying sensor power, frequency programmable sawtooth oscillator, fully accessible error amplifier, pulse width modulator comparator, three open collector top drivers, and three high current totem pole bottom drivers ideally suited for driving power MOSFETs.

Also included are protective features consisting of undervoltage lockout, cycle-by-cycle current limiting with a selectable time delayed latched shutdown mode, internal thermal shutdown, and a unique fault output that can be interfaced into microprocessor controlled systems.

Typical motor control functions include open-loop speed, forward or reverse direction, run enable, and dynamic braking.

The MC33034P60 and MC33034P120 are designed to operate with an electrical sensor phasing of 60°/300° and 120°/240° respectively.

- 10 V to 40 V Operation
- Undervoltage Lockout
- 6.25 V Reference Capable of Supplying Sensor Power
- Fully Accessible Error Amplifier for Servo Applications
- High Current Totem Pole Bottom Drivers
- Cycle-By-Cycle Current Limiting
- Internal Thermal Shutdown

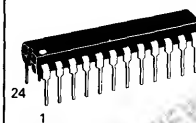


SENSEFET is a trademark of Motorola.

MC33034

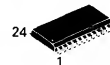
BRUSHLESS DC MOTOR CONTROLLER

SILICON MONOLITHIC
INTEGRATED CIRCUIT

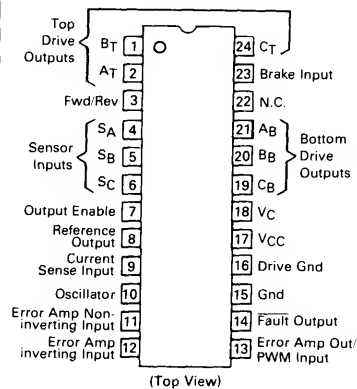


P SUFFIX
PLASTIC PACKAGE
CASE 724

DW SUFFIX
PLASTIC PACKAGE
CASE 751E
(SO-24L)



PIN CONNECTIONS



ORDERING INFORMATION

Package	Sensor Electrical Phasing	Device
MC33034DW60	60°/300°	SO-24L
MC33034DW120	120°/240°	SO-24L
MC33034P60	60°/300°	Plastic DIP
MC33034P120	120°/240°	Plastic DIP

Ambient Temperature Range
= -40°C to +85°C

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	V
Digital Inputs (Pins 3, 4, 5, 6, 7, 23)	—	V_{ref}	V
Oscillator Input Current (Source or Sink)	I_{OSC}	30	mA
Error Amp Input Voltage Range (Pins 11, 12, Note 1)	V_{IR}	-0.3 to 40	V
Error Amp Output Current, Source or Sink (Note 2)	I_{Out}	10	mA
Current Sense Input Voltage	V_{Sense}	5.0	V
Fault Output Voltage	$V_{CE(Fault)}$	20	V
Fault Output Sink Current	$I_{Sink(Fault)}$	20	mA
Top Drive Voltage (Pins 1, 2, 24)	$V_{CE(top)}$	45	V
Top Drive Sink Current (Pins 1, 2, 24)	$I_{Sink(top)}$	50	mA
Bottom Drive Supply Voltage (Pin 18)	V_C	40	V
Bottom Drive Output Current, Source or Sink (Pins 19, 20, 21)	I_{DRV}	100	mA
Power Dissipation and Thermal Characteristics			
Maximum Power Dissipation ($\theta_A = 85^\circ\text{C}$)	P_D	867	mW
Thermal Resistance Junction to Air	$R_{\theta JA}$	75	$^\circ\text{C/W}$
Operating Junction Temperature	T_J	+150	$^\circ\text{C}$
Operating Ambient Temperature Range	T_A	-40 to +85	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS (V_{CC} and $V_C = 20\text{ V}$, $R_T = 4.7\text{ k}$, $C_T = 10\text{ nF}$, $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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REFERENCE SECTION

Reference Output Voltage ($I_{Ref} = 1.0\text{ mA}$) $T_A = 25^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	V_{ref}	5.9 5.82	6.25 —	6.5 6.57	V
Line Regulation ($V_{CC} = 10\text{ V}$ to 40 V , $I_{ref} = 1.0\text{ mA}$)	Reg_{line}	—	12	30	mV
Load Regulation ($I_{ref} = 1.0\text{ mA}$ to 20 mA)	Reg_{load}	—	5.0	30	mV
Output Short Circuit Current (Note 3)	I_{SC}	40	60	—	mA
Reference Under Voltage Lockout Threshold	V_{th}	4.0	4.5	5.0	V

ERROR AMPLIFIER

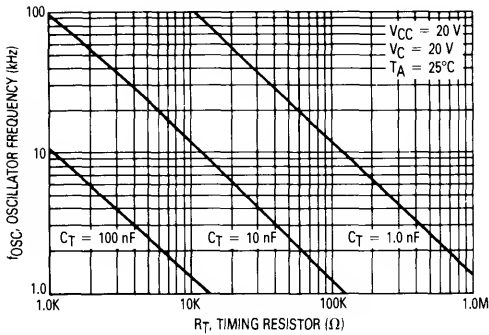
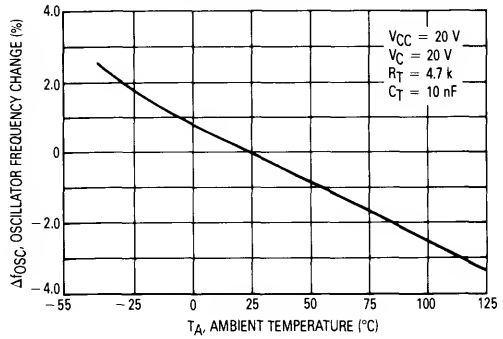
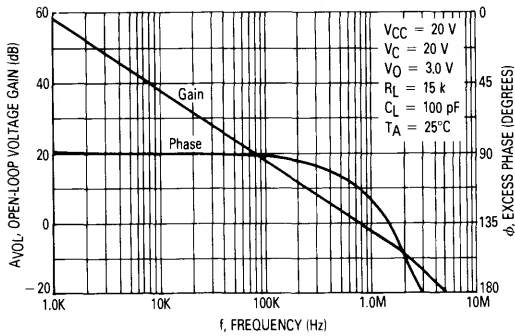
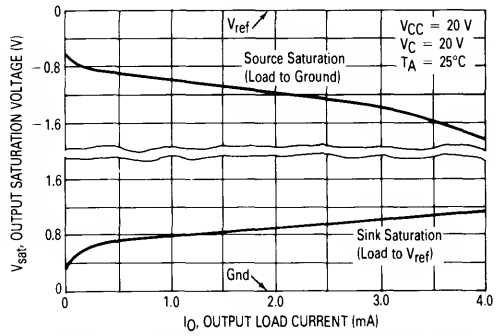
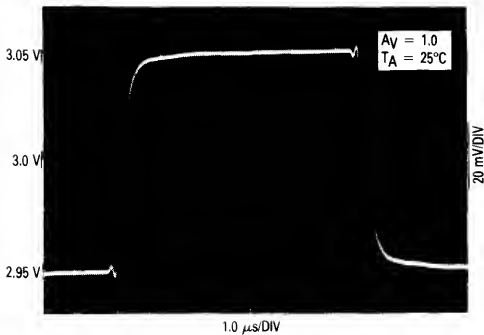
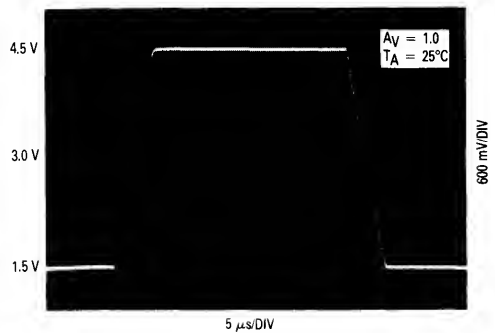
Input Offset Voltage ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)	V_{IO}	—	2.0	10	mV
Input Offset Current ($T_A = -40$ to $+85^\circ\text{C}$)	I_{IO}	—	10	500	nA
Input Bias Current ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)	I_{IB}	—	-25	-1000	nA
Input Common Mode Voltage Range	V_{ICR}	(0 V to $V_{CC} - 2.0\text{ V}$)			V
Open-Loop Voltage Gain ($V_O = 3.0\text{ V}$, $R_L = 15\text{ k}$)	A_{VOL}	75	95	—	dB
Input Common Mode Rejection Ratio	$CMRR$	55	80	—	dB
Power Supply Rejection Ratio (V_{CC} and $V_C = 10\text{ V}$ to 40 V)	$PSRR$	65	95	—	dB
Output Voltage Swing					V
High State ($R_L = 15\text{ k}$ to Gnd)	V_{OH}	4.6	5.4	—	
Low State ($R_L = 15\text{ k}$ to V_{ref})	V_{OL}	—	0.7	1.0	

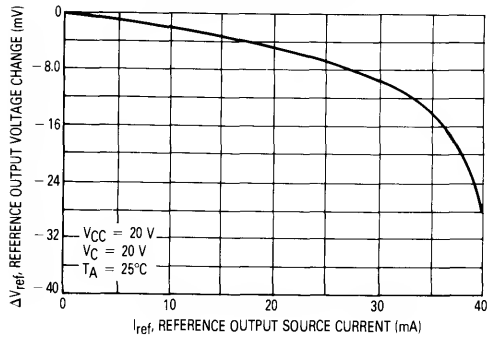
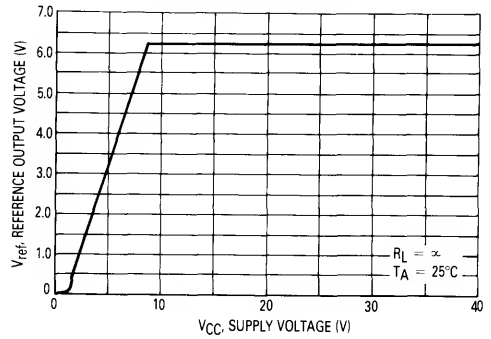
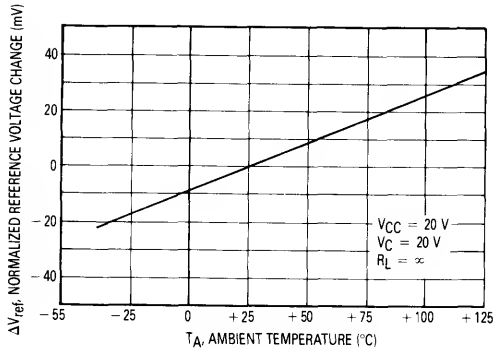
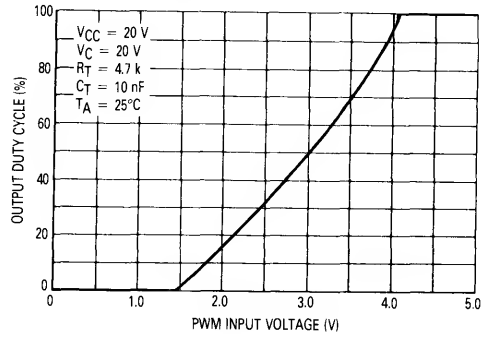
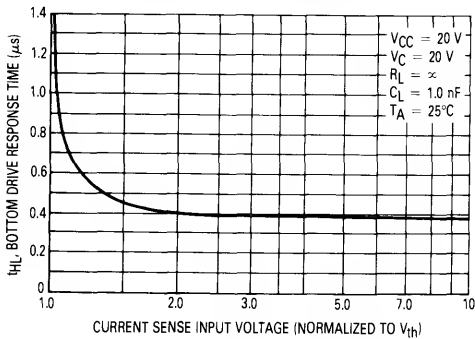
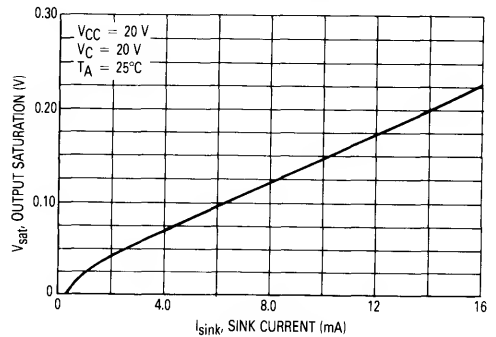
Notes:

1. The input common mode voltage or input signal voltage should not be allowed to go negative by more than 0.3 V. The upper functional limit of the common mode voltage range is typically $V_{CC} - 2.0\text{ V}$, but either or both inputs can go to 40 V, independent of V_{CC} without device destruction.
2. The compliance voltage must not exceed the range of -0.3 V to V_{ref} .
3. Maximum package power dissipation limits must be observed.

ELECTRICAL CHARACTERISTICS (V_{CC} and $V_C = 20\text{ V}$, $R_T = 4.7\text{ k}$, $C_T = 10\text{ nF}$, $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR SECTION					
Oscillator Frequency	f_{OSC}	21	23.5	26	kHz
Frequency Change with Voltage ($V_{CC} = 10\text{ V}$ to 40 V)	$\Delta f_{OSC}/\Delta V$	—	0.1	5.0	%
Sawtooth Peak Voltage	$V_{OSC(P)}$	—	4.0	4.2	V
Sawtooth Valley Voltage	$V_{OSC(V)}$	1.2	1.5	—	V
LOGIC INPUTS					
Input Threshold Voltage (Pins 3, 4, 5, 6, 7, 23)					
High State	V_{IH}	2.0	1.4	—	V
Low State	V_{IL}	—	1.4	0.8	
Sensor Inputs (Pins 4, 5, 6)					
High State Input Current ($V_{IH} = 5.0\text{ V}$)	I_{IH}	−250	−150	−40	μA
Low State Input Current ($V_{IL} = 0\text{ V}$)	I_{IL}	−900	−600	−300	
Forward/Reverse and Brake Inputs (Pins 3, 23)					
High State Input Current ($V_{IH} = 5.0\text{ V}$)	I_{IH}	−150	−88	−25	μA
Low State Input Current ($V_{IL} = 0\text{ V}$)	I_{IL}	−600	−325	−150	
Output Enable					
High State Input Current ($V_{IH} = 5.0\text{ V}$)	I_{IH}	−70	−40	−10	μA
Low State Input Current ($V_{IL} = 0\text{ V}$)	I_{IL}	−80	−40	−20	
CURRENT-LIMIT COMPARATOR					
Threshold Voltage	V_{th}	75	100	125	mV
Input Bias Current ($V_{in} = 0\text{ V}$ to 5.0 V)	I_{IB}	—	−1.0	−2.0	μA
OUTPUTS AND POWER SECTIONS					
Top Drive Output Sink Saturation ($I_{sink} = 25\text{ mA}$)	$V_{CE(sat)}$	—	0.95	1.5	V
Top Drive Output Off-State Leakage ($V_{CE} = 40\text{ V}$)	$I_{DRV(Leak)}$	—	2.0	100	μA
Top Drive Output Switching Time ($C_L = 47\text{ pF}$, $R_L = 1.0\text{ k}$)					
Rise Time	t_r	—	100	300	ns
Fall Time	t_f	—	35	300	
Bottom Drive Output Voltage					
High State ($I_{source} = 50\text{ mA}$)	V_{OH}	($V_C - 3.0$)	($V_C - 2.4$)	—	V
Low State ($I_{sink} = 50\text{ mA}$)	V_{OL}	—	1.5	2.0	
Bottom Drive Output Switching Time ($C_L = 1000\text{ pF}$)					
Rise Time	t_r	—	75	200	ns
Fall Time	t_f	—	65	200	
Fault Output Sink Saturation ($I_{sink} = 16\text{ mA}$)	$V_{CE(sat)}$	—	225	500	mV
Fault Output Off-State Leakage ($V_{CE} = 20\text{ V}$)	$I_{FLT(Leak)}$	—	1.0	100	μA
Under Voltage Lockout					
Drive Outputs Enabled (V_{CC} or V_C Increasing)	$V_{th(on)}$	8.2	9.1	10	V
Hysteresis	V_H	0.1	0.2	0.3	
Power Supply Current					
V_{CC} and $V_C = 20\text{ V}$					
V_{CC} Current (Pin 17)	I_{CC}	—	16	22	mA
V_C Current (Pin 18)	I_C	—	3.0	7.0	

FIGURE 1 — OSCILLATOR FREQUENCY versus TIMING RESISTOR

FIGURE 2 — OSCILLATOR FREQUENCY CHANGE versus TEMPERATURE

FIGURE 3 — ERROR AMP OPEN-LOOP GAIN AND PHASE versus FREQUENCY

FIGURE 4 — ERROR AMP OUTPUT SATURATION versus LOAD CURRENT

FIGURE 5 — ERROR AMP SMALL-SIGNAL TRANSIENT RESPONSE

FIGURE 6 — ERROR AMP LARGE-SIGNAL TRANSIENT RESPONSE


**FIGURE 7 — REFERENCE OUTPUT VOLTAGE CHANGE
versus SOURCE CURRENT****FIGURE 8 — REFERENCE OUTPUT VOLTAGE
versus SUPPLY VOLTAGE****FIGURE 9 — REFERENCE OUTPUT VOLTAGE
versus TEMPERATURE****FIGURE 10 — OUTPUT DUTY CYCLE versus
PWM INPUT VOLTAGE****FIGURE 11 — BOTTOM DRIVE RESPONSE TIME versus
CURRENT SENSE INPUT VOLTAGE****FIGURE 12 — FAULT OUTPUT SATURATION
versus SINK CURRENT**

**FIGURE 13 — TOP DRIVE OUTPUT SATURATION
versus SINK CURRENT**

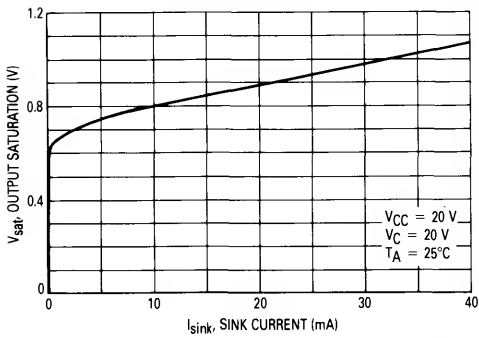


FIGURE 14 — TOP DRIVE OUTPUT WAVEFORM

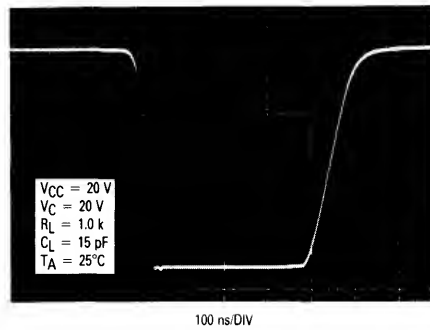


FIGURE 15 — BOTTOM DRIVE OUTPUT WAVEFORM

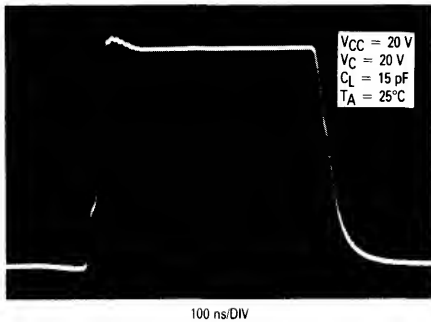
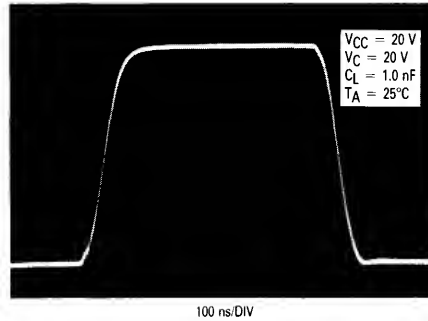
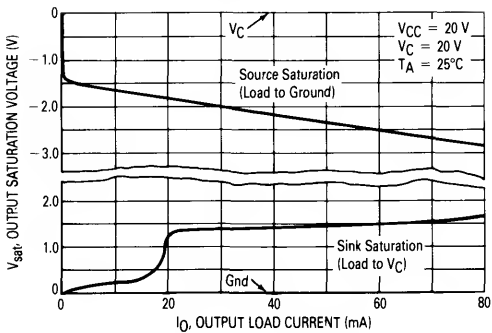


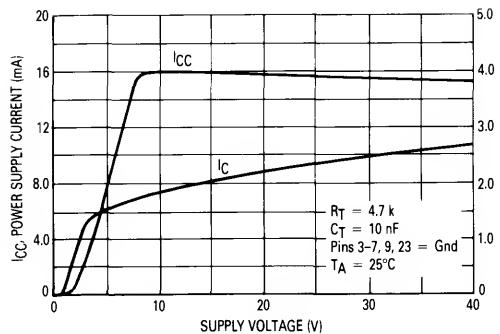
FIGURE 16 — BOTTOM DRIVE OUTPUT WAVEFORM



**FIGURE 17 — BOTTOM DRIVE OUTPUT SATURATION
versus LOAD CURRENT**



**FIGURE 18 — POWER AND BOTTOM DRIVE SUPPLY
CURRENT versus SUPPLY VOLTAGE**



MC33034

PIN FUNCTION DESCRIPTION

Pin No.	Function	Description
1, 2, 24	B _T , A _T , C _T	These three open collector Top Drive Outputs are designed to drive the external upper power switch transistors.
3	FWD/REV	The Forward/Reverse input is used to change the direction of motor rotation.
4, 5, 6	S _A , S _B , S _C	These three Sensor Inputs control the commutation sequence.
7	Output Enable	A logic high at this input causes the motor to run, while a low causes it to coast.
8	Reference Output	This output provides charging current for the oscillator timing capacitor C _T and a reference for the error amplifier. It can also furnish sensor power.
9	Current Sense Input	A 100 mV signal at this input terminates output switch conduction during a given oscillator cycle.
10	Oscillator	The Oscillator frequency is programmed by the values selected for timing components R _T and C _T .
11	Error Amp Noninverting Input	This input is normally connected to the speed set potentiometer.
12	Error Amp Inverting Input	This input is normally connected to the Error Amp Output in open-loop applications.
13	Error Amp Output/PWM Input	This pin is available for compensation in closed-loop applications.
14	Fault Output	This open collector output is active low during one or more of the following conditions: Invalid Sensor Input code, Enable Input at logic 0, Current Sense Input > 100 mV, Undervoltage Lockout activation, and Thermal Shutdown.
15	Ground	This pin is the control circuitry ground return and is connected back to the source ground.
16	Drive Ground	This pin is a separate power ground return that is connected back to the power source. It reduces the effects of switching transient noise on the control circuitry.
17	V _{CC}	This pin is the positive supply of the control IC. The controller is functional over a minimum V _{CC} range of 10 V to 40 V.
18	V _C	The high state (V _{OH}) of the Bottom Drive Outputs are set by the voltage applied to this pin. The controller is operational over a minimum V _C range of 10 V to 40 V.
19, 20, 21	C _B , B _B , A _B	These three totem pole Bottom Drive Outputs are designed for direct drive of the external bottom power switch transistors.
22	N.C.	No connection. This pin is not internally connected.
23	Brake Input	A logic low at this input causes the motor to run, while a high causes rapid deceleration.

MC33034

FIGURE 19 — REPRESENTATIVE BLOCK DIAGRAM

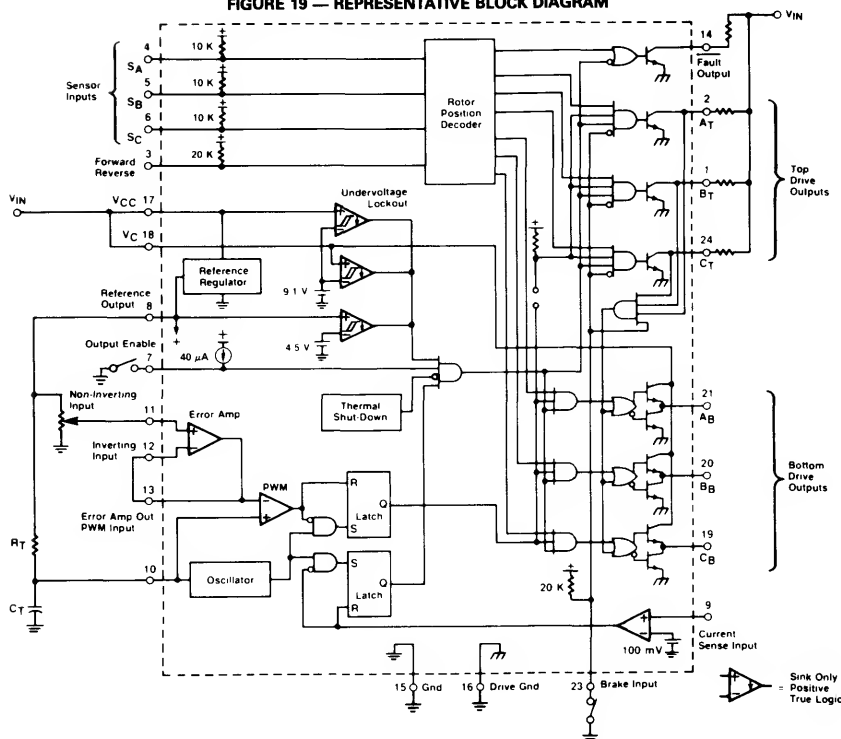


FIGURE 20 — THREE PHASE, SIX STEP COMMUTATION TRUTH TABLE

Inputs (Note 1)										Outputs (Note 2)						
Sensor Electrical Phasing										Top Drives			Bottom Drives			Fault
MC33034P60 60°			MC33034P120 120°							Current Sense			A _T	B _T	C _T	
S _A	S _B	S _C	S _A	S _B	S _C	F/R	Enable	Brake	Sense	A _T	B _T	C _T	A _B	B _B	C _B	Fault
1	0	0	1	0	0	1	1	0	0	0	1	1	0	0	1	1
1	1	0	1	1	0	1	1	0	0	1	0	1	0	0	1	1
1	1	1	0	1	0	1	1	0	0	1	0	1	1	0	0	1
0	1	1	0	1	1	1	1	0	0	1	1	0	1	0	0	1
0	0	1	0	0	1	1	1	0	0	1	1	0	0	1	0	1
0	0	0	1	0	1	1	1	0	0	0	1	1	0	1	0	1
1	0	0	1	0	0	0	1	0	0	1	1	0	1	0	0	1
1	1	0	1	1	0	0	1	0	0	1	1	0	0	1	0	1
1	1	1	0	1	0	0	1	0	0	0	1	1	0	1	0	1
0	1	1	0	1	1	0	1	0	0	0	1	1	0	0	1	1
0	0	1	0	0	1	0	1	0	0	1	0	1	0	0	1	1
0	0	0	1	0	1	0	1	0	0	1	0	1	1	0	0	1
1	0	1	0	0	0	X	X	0	X	1	1	1	0	0	0	0
0	1	0	1	1	1	X	X	0	X	1	1	1	0	0	0	0
X	X	X	X	X	X	X	0	0	X	1	1	1	0	0	0	0
V	V	V	V	V	V	X	1	1	0	1	1	1	1	1	1	1
X	X	X	X	X	X	X	X	1	1	1	1	1	1	1	1	0
X	X	X	X	X	X	X	X	0	1	1	1	1	0	0	0	0

Notes:

- The digital inputs (Pins 3, 4, 5, 6, 7, 23) are all TTL compatible. The current sense input (Pin 9) has a 100 mV threshold. A logic 0 for this input is defined as < 80 mV, and a logic 1 is > 120 mV.
- The Fault and top drive outputs are open collectors and are active in the low (0) state.
- V = any one of the six valid sensor combinations.
X = Don't care.

INTRODUCTION

The Motorola MC33034 is a high performance monolithic brushless motor controller containing all of the active functions required to implement a full featured, open-loop, three or four phase motor control system. These integrated circuits are constructed with Bipolar Analog technology which offers a high degree of performance and ruggedness in hostile industrial environments. The MC33034 consists of a rotor position decoder for proper commutation sequencing, temperature compensated reference capable of supplying sensor power, frequency programmable sawtooth oscillator, fully accessible error amplifier, pulse width modulator comparator, three open collector top drivers, and three high current totem pole bottom drivers ideally suited for driving power MOSFETs.

Also included are protective features consisting of undervoltage lockout, cycle by cycle current limiting with a selectable time delayed latched shutdown mode, internal thermal shutdown, and a unique Fault output that can be interfaced into microprocessor controlled systems.

Typical motor control functions include open-loop speed control, forward or reverse direction, run enable, and dynamic braking.

FUNCTIONAL DESCRIPTION

A representative internal block diagram and a typical system application are shown in Figures 19 and 36. A discussion of the features and function of each of the internal blocks is given below.

Rotor Position Decoder

An internal rotor position decoder monitors the three sensor inputs (Pins 4, 5, 6) to provide the proper sequencing of the top and bottom drive outputs. The sensor inputs are designed to interface directly with open collector type Hall Effect switches or opto slotted couplers. Internal pull-up resistors are included to minimize the required number of external components. The inputs are TTL compatible, with the thresholds typically at 1.4 volts. The MC33034 series consists of two device types, each is designed to control three phase motors and operate with two of the four most common conventions of sensor phasing. The MC33034P60 is intended to operate with an electrical sensor phasing of 60° or 300° and the MC33034P120 with 120° or 240°. With three sensor inputs there are eight possible input code combinations, six of these are valid rotor positions. The remaining two codes are invalid and are usually caused by an open or shorted sensor line. When an invalid input condition exists, the Fault output is activated and the drive outputs are disabled. With six valid input codes, the decoder can resolve the rotor position to within a window of 60 electrical degrees.

The forward/reverse input (Pin 3) is used to change the direction of motor rotation by reversing the voltage across the stator winding. When this input changes state, from high to low with a given sensor input code (for example 100), the enabled top and bottom drive

outputs with the same alpha designation are exchanged (A_T to A_B , C_B to C_T). In effect the commutation sequence is reversed.

Motor on/off control is accomplished by the output enable (Pin 7). When left disconnected, an internal 40 μA current source enables sequencing of the top and bottom drive outputs. When grounded, the top drive outputs turn off and the bottom drives are forced low, causing the motor to coast and activating the Fault output.

Dynamic motor braking allows an additional margin of safety to be designed into the final product. Braking is accomplished by placing the brake input (Pin 23) in a high state. This causes the top drive outputs to turn off and the bottom drives to turn on, shorting the motor-generated back EMF. The brake input has unconditional priority over all other inputs. The internal 20 k Ω pull-up resistor simplifies interfacing with the system safety-switch by ensuring brake activation if opened or disconnected. The commutation truth table is shown in Figure 20. A four input AND gate is used to monitor the brake input and the three top drive outputs. Its purpose is to disable braking until the top drive outputs attain a high state. This helps to avoid simultaneous conduction of the top and bottom power switches. In half wave motor drive applications, the top drive outputs are not required and are typically left disconnected. Under these conditions braking will be disabled by the AND gate. If required, it can be enabled by connecting a single pull-up resistor from V_{CC} to the three open collector outputs. Figure 38 shows a pull-up method utilizing the enable input current source.

Error Amplifier

A high performance, fully compensated error amplifier with access to both inputs and output (Pins 11, 12, 13) is provided to facilitate the implementation of closed-loop motor speed control. The amplifier features a typical DC voltage gain of 95 dB, 800 kHz gain bandwidth, and a wide input common mode voltage range that extends from ground to $V_{CC} - 2.0 V$. In most open-loop speed control applications, the amplifier is configured as a unity gain voltage follower with the non-inverting input connected to the speed set voltage source. Additional configurations are shown in Figures 31 through 35.

Oscillator

The frequency of the internal ramp oscillator is programmed by the values selected for timing components R_T and C_T . Capacitor C_T is charged from the reference output (Pin 8) through resistor R_T and discharged by an internal transistor. The ramp peak and valley voltages are typically 4.0 V and 1.5 V respectively. To provide a good compromise between audible noise and output switching efficiency, an oscillator frequency in the range of 20 kHz to 30 kHz is recommended. Refer to Figure 1 for component selection.

Pulse Width Modulator

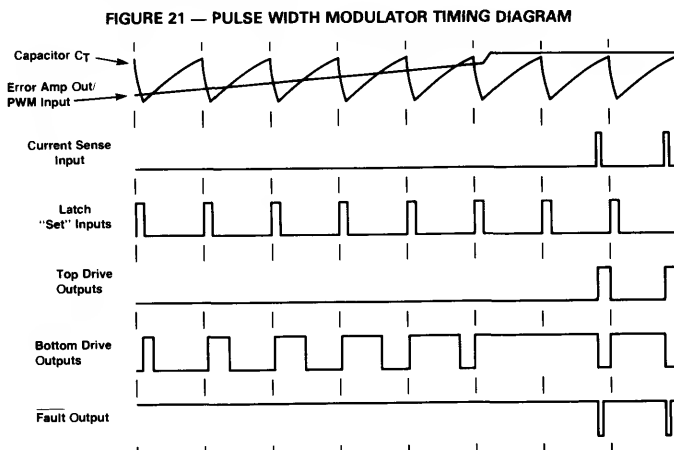
The use of pulse width modulation provides an energy efficient method of controlling the motor speed by varying the average voltage applied to each stator winding during the commutation sequence. As C_T discharges, the oscillator sets both latches, allowing conduction of the top and bottom drive outputs. The PWM comparator resets the upper latch, terminating bottom drive output conduction when the positive-going ramp on C_T becomes greater than the error amplifier output. The pulse width modulator timing diagram is shown in Figure 21. Pulse width modulation for speed control appears only at the bottom drive outputs.

Current Limit

Continuous operation of a motor that is severely overloaded results in overheating and eventual failure. This destructive condition can best be prevented with the use of cycle-by-cycle current limiting. That is, each on-cycle is treated as a separate problem. This is implemented by monitoring the stator current build-up each time the output switch conducts, and upon sensing an over current condition, immediately turns off the switch and holds it off for the duration of the oscillator ramp-up period. The stator current is converted to a voltage by inserting a ground-referenced sense resistor R_S (Figure 36) in series with the three bottom switch transistors (Q4, Q5, Q6). This voltage is monitored by the current sense input (Pin 9), and compared to an internal 100 mV reference. If exceeded, the comparator resets the lower latch and terminates output switch conduction. The value for the sense resistor is:

$$R_S = \frac{0.1}{I_{\text{stator(max)}}$$

The $\overline{\text{Fault}}$ output is activated during the over current condition. The dual-latch PWM configuration ensures that only a single output conduction pulse will occur

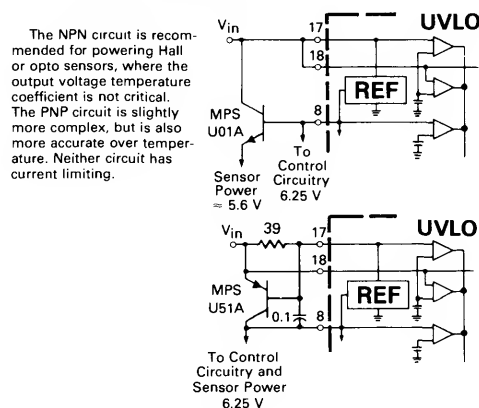


during any given oscillator cycle, whether terminated by the output of the error amp or current limit comparator.

Reference

The on chip 6.25 V regulator (Pin 8) provides charging current for the oscillator timing capacitor, a reference for the error amplifier, and has a current capability of 40 mA for direct power of the sensors in low voltage applications. In higher voltage applications it may become necessary to transfer the power dissipated by the regulator off the I.C. This is easily accomplished with the addition of an external pass transistor as shown in Figure 22. A 6.25 V reference level was chosen to allow implementation of the simpler NPN circuit, where $V_{\text{ref}} - V_{\text{BE}}$ exceeds the minimum voltage required by Hall Effect sensors over temperature. With proper transistor selection, and adequate heatsinking, up to 1.0 amp of load current can be obtained.

FIGURE 22 — REFERENCE OUTPUT BUFFERS



Undervoltage Lockout

A triple Undervoltage Lockout has been incorporated to prevent damage to the control IC and the external power switch transistors. Under low power supply conditions, it guarantees that the IC and sensors are fully functional, and that there is sufficient bottom drive output voltage. The positive power supplies to the IC (V_{CC}) and the bottom drives (V_C) are each monitored by separate comparators that have their thresholds at 9.1 V. This level ensures sufficient gate drive for low $r_{DS(on)}$ when interfacing with standard power MOSFETs. When directly powering the Hall sensors from the reference, improper sensor operation can result if the output voltage should fall below 4.5 V. A third comparator is used to detect this condition. If one or more of the comparators detects an undervoltage condition, the Fault output is activated, the top drives are turned off and the bottom drive outputs are held in a low state. Each of the comparators contain hysteresis to prevent oscillations when crossing their respective thresholds.

Fault Output

The open collector $\overline{\text{Fault}}$ output (Pin 14) was designed to provide diagnostic information in the event of a system malfunction. It has a sink current capability of 16 mA and can directly drive a light emitting diode for visual indication. Additionally, it is easily interfaced with TTL/CMOS logic for use in a microprocessor controlled system. The Fault output is active low when one or more of the following conditions occur:

- 1) Invalid Sensor Input code.
- 2) Enable Input at Logic "0."
- 3) Current Sense Input > 100 mV.
- 4) Undervoltage Lockout, activation of one or more of the comparators.
- 5) Thermal Shutdown, maximum junction temperature has been exceeded.

This unique output can also be used to distinguish between motor start-up or sustained operation in an overloaded condition. With the addition of an R/C network between the $\overline{\text{Fault}}$ output and the enable input, it is possible to create a time-delayed latched shutdown for overcurrent. The added circuitry shown in Figure 23, makes easy starting of motor systems which have high inertial loads by providing additional starting torque, while still preserving overcurrent protection. This task is accomplished by setting the current limit to a higher than nominal value for a predetermined time. During an excessively long overcurrent condition, capacitor C_{DLY} will charge causing the enable input to cross its threshold to a low state. A latch will now be formed by a positive feedback loop from the Fault output to the enable input. Once set by the current sense input, it can only be reset by shorting C_{DLY} or cycling the power supply.

Drive Outputs

The three top drive outputs (Pins 1, 2, 24) are open collector NPN transistors capable of sinking 50 milliamps with a minimum breakdown of 45 volts. Interfacing into higher voltage applications is easily accomplished with the circuits shown in Figures 24 and 25.

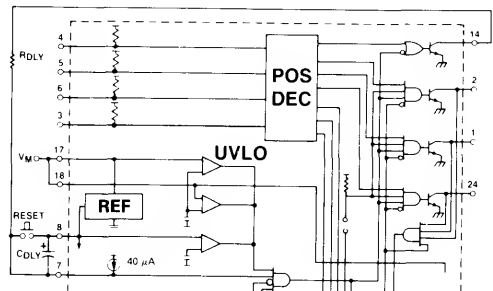
The three totem pole bottom drive outputs (Pins 19, 20, 21) are particularly suited for direct drive of 'N' channel MOSFETs or NPN bipolar transistors (Figures 26, 27 and 28). Each output is capable of sourcing and sinking up to 100 mA. Power for the bottom drives is supplied from V_C (Pin 18). This separate supply input allows the designer added flexibility in tailoring the drive voltage, independent of V_{CC} . A zener clamp is typically connected to this input when driving power MOSFETs in systems where V_{CC} is greater than 20 V.

A separate drive ground (Pin 16) is included to reduce the effects of switching transient noise imposed on the current sense input. This feature becomes particularly useful when driving current sensing power MOSFETs (Figure 29).

Thermal Shutdown

Internal thermal shutdown circuitry is provided to protect the IC in the event that the maximum junction temperature is exceeded. When activated, typically at 170°C, the IC acts as though the enable input was grounded.

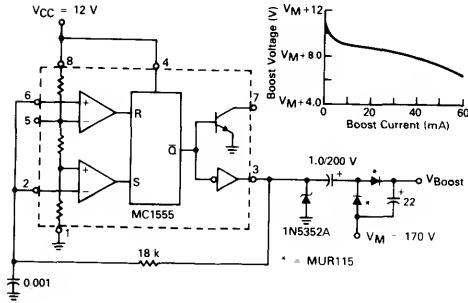
FIGURE 23 — TIMED DELAYED LATCHED OVER-CURRENT SHUTDOWN



$$t_{DLY} \approx RDLY \cdot CDLY \ln \left(\frac{V_{ref} - (I_{IL \text{ enable}} RDLY)}{V_{th \text{ enable}} - (I_{IL \text{ enable}} RDLY)} \right)$$

$$\approx RDLY \cdot CDLY \ln \left(\frac{6.25 - (40 \times 10^{-6} RDLY)}{1.4 - (40 \times 10^{-6} RDLY)} \right)$$

FIGURE 30 — HIGH VOLTAGE BOOST SUPPLY



This circuit generates V_{Boost} for Figure 25.

FIGURE 31 — DIFFERENTIAL INPUT SPEED CONTROLLER

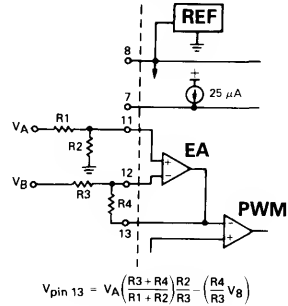
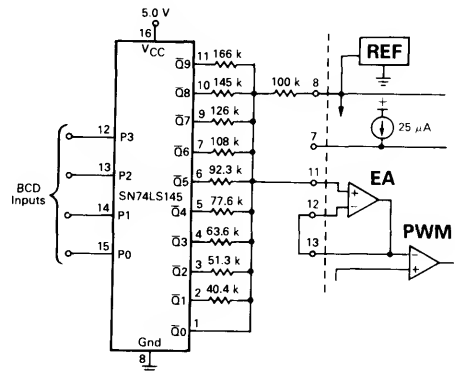
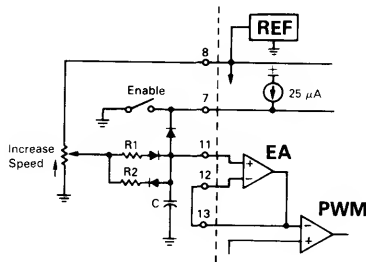


FIGURE 33 — DIGITAL SPEED CONTROLLER



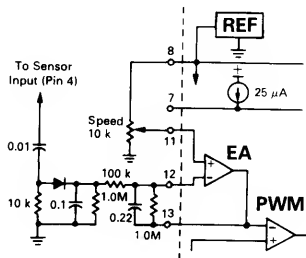
The SN74LS175 is an open collector BCD to One of Ten decoder. When connected as shown, input codes 0000 through 1001 steps the PWM in increments of approximately 10% from 0 to 90% on-time. Input codes 1010 through 1111 will produce 100% on-time or full motor speed.

FIGURE 32 — CONTROLLED ACCELERATION/DECELERATION



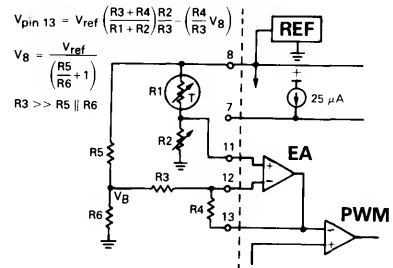
Resistors R1 with capacitor C sets the acceleration time constant while R2 controls the deceleration. The values of R1 and R2 should be at least ten times greater than that of the speed set potentiometer to minimize time constant variations with different speed settings.

FIGURE 34 — CLOSED-LOOP SPEED CONTROL



The rotor position sensors can be used as a tachometer. By differentiating the positive-going edges and then integrating them over time, a voltage proportional to speed can be generated. The error amp compares this voltage to that of the speed set to control the PWM.

FIGURE 35 — CLOSED-LOOP TEMPERATURE CONTROL



This circuit can control the speed of a cooling fan proportional to the difference between the sensor and set temperatures. The control loop is closed as the forced air cools the NTC thermistor. For controlled heating applications, exchange the positions of R1 and R2.

SYSTEM APPLICATIONS

Three Phase Motor Commutation

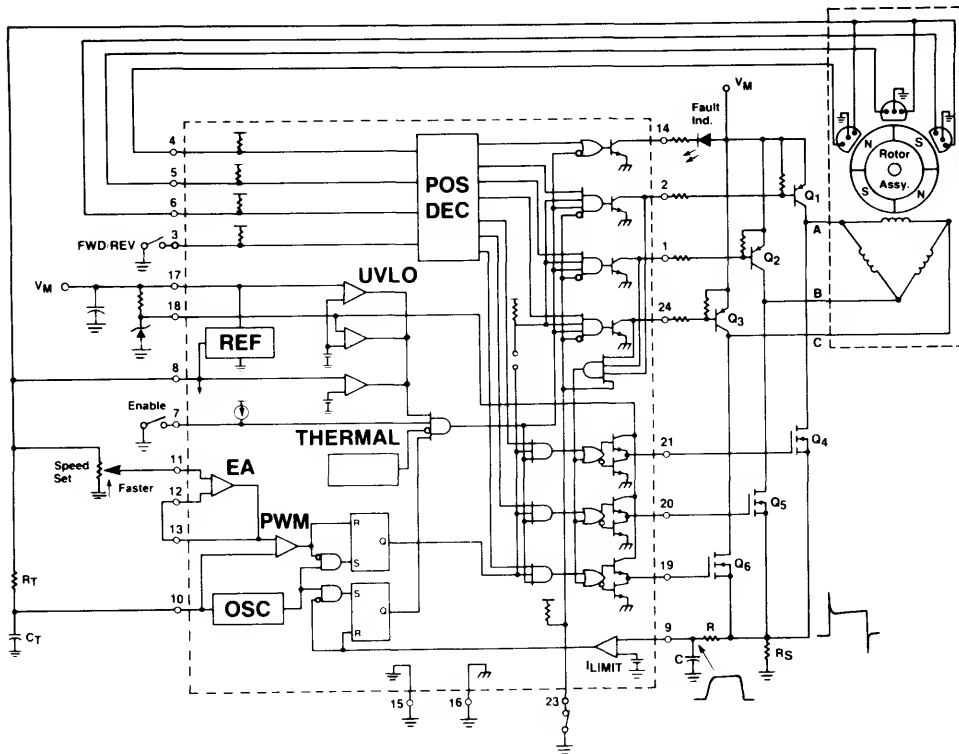
The three phase application shown in Figure 36 is a full-featured open-loop motor controller with full wave, six step drive. The upper power switch transistors are Darlingtons while the lower devices are power MOSFETs. Each of these devices contains an internal parasitic catch diode that is used to return the stator inductive energy back to the power supply. The outputs are capable of driving a delta or wye connected stator, and a grounded neutral wye if split supplies are used. At any given rotor position, only one top and one bottom power switch (of different totem poles) is enabled. This configuration switches both ends of the stator winding from supply to ground which causes the current flow to be bidirectional or full wave. A leading edge spike is usually present on the current waveform and can cause a current-limit instability. The spike can be eliminated by adding an RC filter in series with the current sense input. Using a low inductance type resistor for R_S will

also aid in spike reduction. Care must be taken in the selection of the bottom power switch transistors so that the current during braking does not exceed the device rating. During braking, the peak current generated is limited only by the series resistance of the conducting bottom switch and winding.

$$I_{\text{peak}} = \frac{V_M + \text{EMF}}{R_{\text{switch}} + R_{\text{winding}}}$$

If the motor is running at maximum speed with no load, the generated back EMF can be as high as the supply voltage, and at the onset of braking the peak current may approach twice the motor stall current. Figure 37 shows the commutation waveforms over two electrical cycles. The first cycle (0° to 360°) depicts motor operation at full speed while the second cycle (360° to 720°) shows a reduced speed with about 50 percent pulse width modulation. The current waveforms reflect a constant torque load and are shown synchronous to the commutation frequency for clarity.

FIGURE 36 — THREE PHASE, SIX STEP, FULL WAVE MOTOR CONTROLLER



MC33034

FIGURE 37 — THREE PHASE, SIX STEP, FULL WAVE COMMUTATION WAVEFORMS

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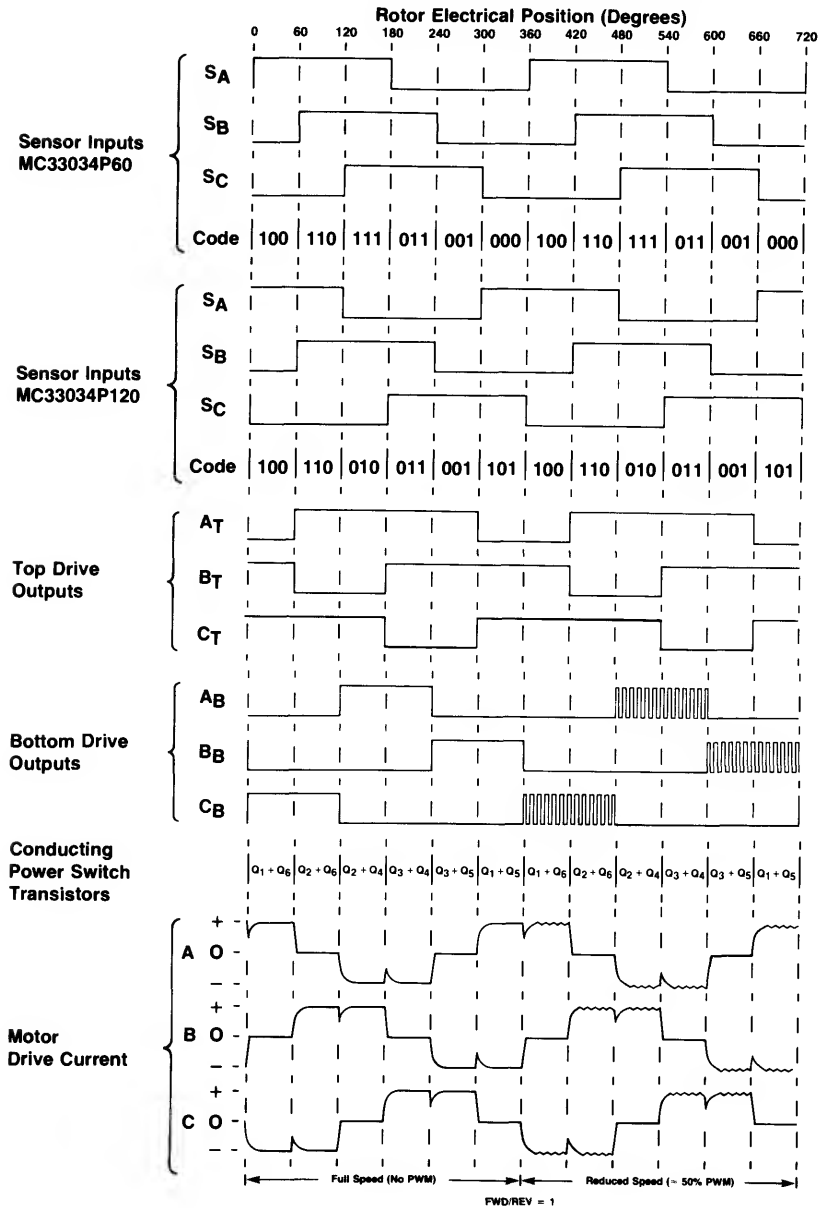
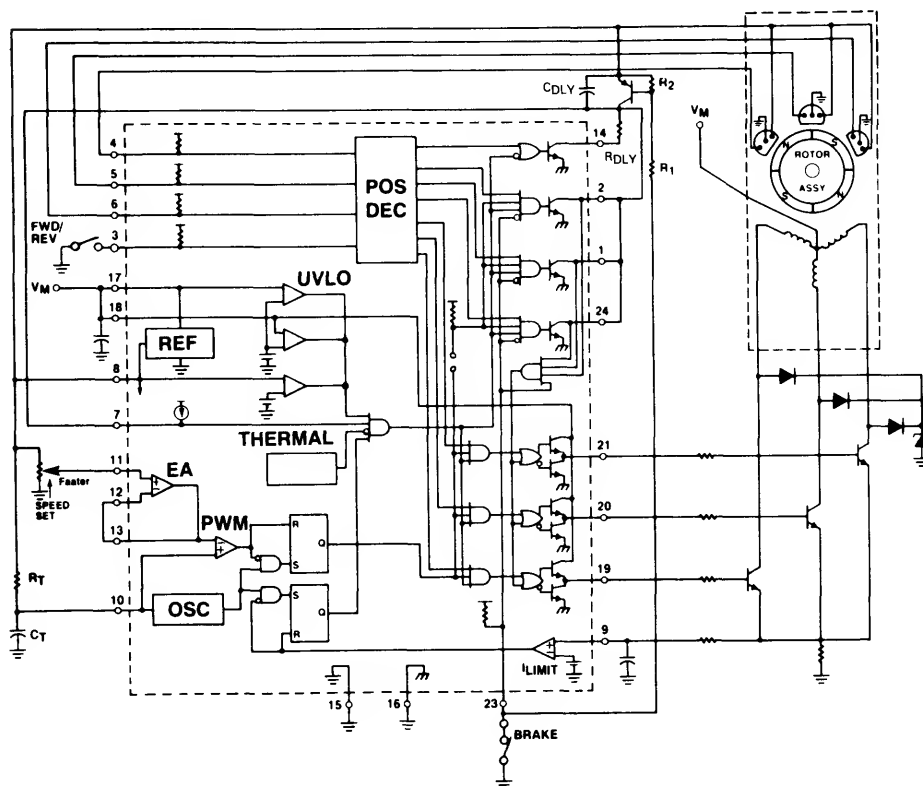


FIGURE 38 — THREE PHASE, THREE STEP, HALF WAVE MOTOR CONTROLLER



4

Figure 38 shows a three phase, three step, half wave motor controller. This configuration is ideally suited for automotive and other low voltage applications since there is only one power switch voltage drop in series with a given stator winding. Current flow is unidirectional or half wave because only one end of each winding is switched. Continuous braking with the typical half wave arrangement presents a motor overheating problem since stator current is limited only by the winding resistance. This is due to the lack of upper power switch transistors, as in the full wave circuit, used to disconnect the windings from the supply voltage V_M . A unique

solution is to provide braking until the motor stops and then turn off the bottom drives. This can be accomplished by using the fault output in conjunction with the enable input as an over current timer. Components $RDLY$ and $CDLY$ are selected to give the motor sufficient time to stop before latching the enable input and the top drive AND gate low. To enabling the motor, the PNP transistor along with resistors $R1$ and $R3$ are used to reset the latch by discharging $CDLY$ upon brake switch closure. The stator flyback voltage is clamped by a single zener and three diodes.

Sensor Phasing Comparison

There are four conventions used to establish the relative phasing of the sensor signals in three phase motors. With six step drive, an input signal change must occur every 60 electrical degrees, however, the relative signal phasing is dependent upon the mechanical sensor placement. A comparison of the conventions in electrical degrees is shown in Figure 39(a). From the sensor phasing table, Figure 39(b), note that the order of input codes for 60° phasing is the reverse of 300°. This means that a P60 suffix part will operate with either convention with a resulting change in rotor direction. The same is true for the P120 part operating between 120° and 240° conventions. Further examination of the 60° and 120° columns reveal that either suffix part will operate with any of the sensor conventions with the addition of an

inverter and the interchanging of S_B and S_C inputs as shown in Figure 40.

In this data sheet, the rotor position has always been given in electrical degrees, since the mechanical position is a function of the number of rotating magnetic poles. The relationship between the electrical and mechanical position is:

$$\text{Electrical Degrees} = \text{Mechanical Degrees} \left(\frac{\# \text{Rotor Poles}}{2} \right)$$

An increase in the number of magnetic poles causes more electrical revolutions for a given mechanical revolution. General purpose three phase motors typically contain a four pole rotor which yields two electrical revolutions for one mechanical.

FIGURE 39(a) — SENSOR PHASING COMPARISON

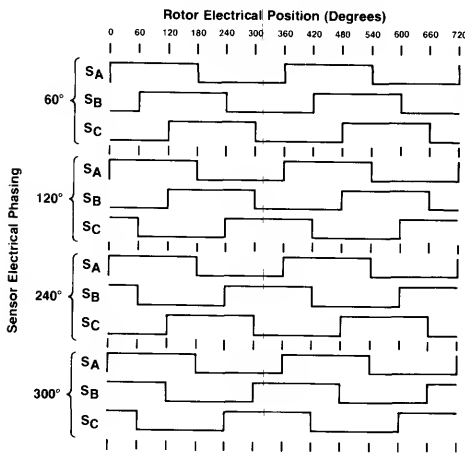
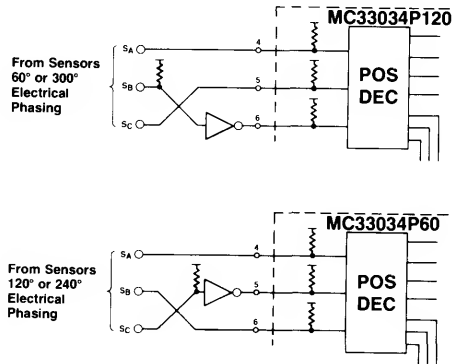


FIGURE 39(b) — SENSOR PHASING TABLE

Sensor Electrical Phasing (Degrees)											
60°			120°			240°			300°		
S_A	S_B	S_C	S_A	S_B	S_C	S_A	S_B	S_C	S_A	S_B	S_C
1	0	0	1	0	1	1	1	0	1	1	1
1	1	0	1	0	0	1	0	0	1	1	0
1	1	1	1	1	0	1	0	1	1	0	0
0	1	1	0	1	0	0	0	1	0	0	0
0	0	1	0	1	1	0	1	1	0	0	1
0	0	0	0	0	1	0	1	0	0	1	1

FIGURE 40 — SENSOR PHASING CONVERSION



MC33034

Two and Four Phase Motor Commutation

The MC33034P60 is also capable of providing a four step output that can be used to drive two or four phase motors. The truth table in Figure 41 shows that by connecting sensor inputs S_B and S_C together, it is possible to truncate the number of drive output states from six to four. The output power switches are connected to B_T , C_T , B_B , and C_B . Figure 42 shows a four phase, four step, full wave motor control application. Power switch transistors Q1 through Q8 are Darlington type, each

with an internal parasitic catch diode. With four step drive, only two rotor position sensors spaced at 90 electrical degrees are required. The commutation waveforms are shown in Figure 43. Note that speed control cannot be accomplished with this circuit, since pulse width modulation does not appear at the top drive outputs.

Figure 44 shows a four phase, four step, half wave motor controller. It has the same features as the circuit in Figure 38, except for the deletion of braking.

FIGURE 41 — TWO AND FOUR PHASE, FOUR STEP, COMMUTATION TRUTH TABLE

MC33034P60						
Inputs			Outputs			
Sensor Electrical Spacing = 90°			Top Drives		Bottom Drives	
S_A	S_B	F/R	B_T	C_T	B_B	C_B
1	0	1	1	1	0	1
1	1	1	0	1	0	0
0	1	1	1	0	0	0
0	0	1	1	1	1	0
1	0	0	1	0	0	0
1	1	0	1	1	1	0
0	1	0	1	1	0	1
0	0	0	0	1	0	0

S_B connected to S_C

FIGURE 42 — FOUR PHASE, FOUR STEP, FULL WAVE MOTOR CONTROLLER

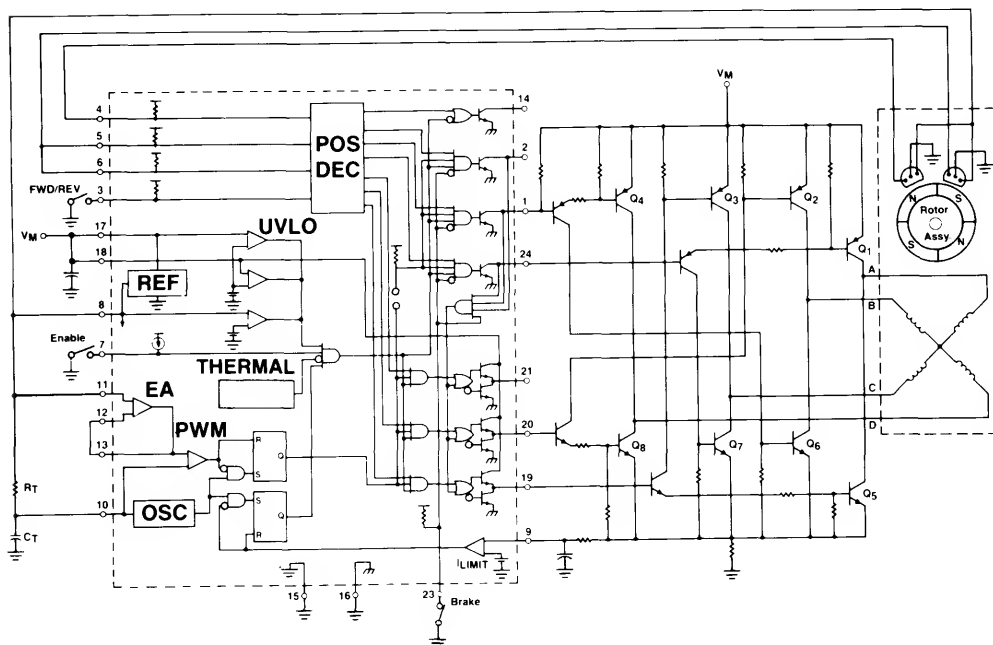
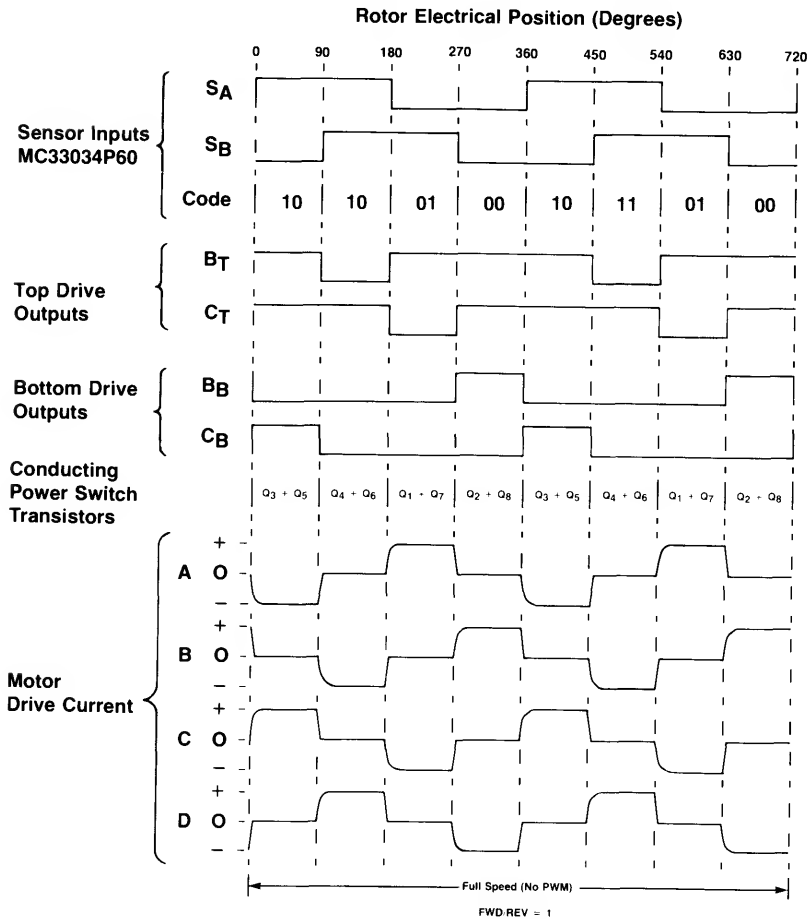


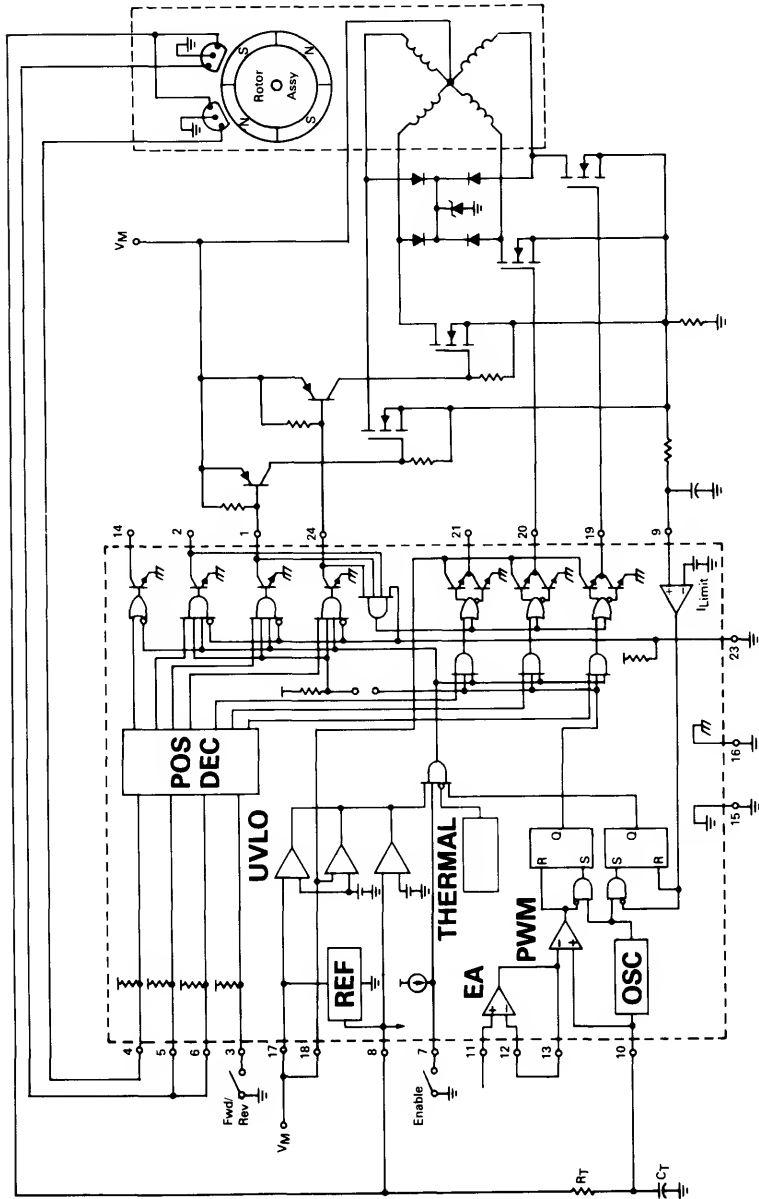
FIGURE 43 — FOUR PHASE, FOUR STEP, FULL WAVE COMMUTATION WAVEFORMS

**LAYOUT CONSIDERATIONS**

Do not attempt to construct any of the brushless motor control circuits on wire-wrap or plug-in prototype boards. High frequency printed circuit layout techniques are imperative to prevent pulse jitter. This is usually caused by excessive noise pick-up imposed on the current sense or error amp inputs. The printed circuit layout should contain a ground plane with low current signal and high current drive and output buffer grounds

returning on separate paths back to the power supply input filter capacitor V_M . Ceramic bypass capacitors ($0.1 \mu F$) connected close to the integrated circuit at V_{CC} , V_C , V_{ref} and the error amp non-inverting input may be required depending upon circuit layout. This provides a low impedance path for filtering any high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI.

FIGURE 44 — FOUR PHASE, FOUR STEP, HALF WAVE MOTOR CONTROLLER



Advance Information

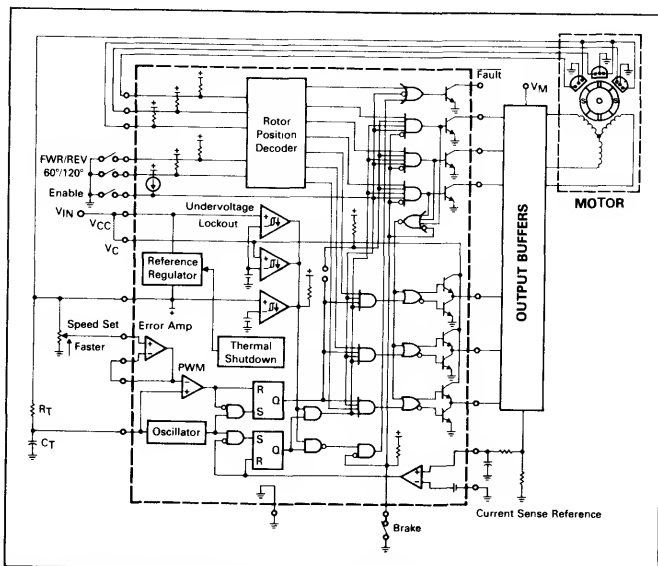
BRUSHLESS DC MOTOR CONTROLLER

The MC33035 is a high performance second generation monolithic brushless DC motor controller containing all of the active functions required to implement a full featured open-loop, three or four phase motor control system. This device consists of a rotor position decoder for proper commutation sequencing, temperature compensated reference capable of supplying sensor power, frequency programmable sawtooth oscillator, fully accessible error amplifier, pulse width modulator comparator, three open collector top drivers, and three high current totem pole bottom drivers ideally suited for driving power MOSFETs.

Also included are protective features consisting of undervoltage lock-out, cycle-by-cycle current limiting with a selectable time delayed latched shutdown mode, internal thermal shutdown, and a unique fault output that can be interfaced into microprocessor controlled systems.

Typical motor control functions include open-loop speed, forward or reverse direction, run enable, and dynamic braking. The MC33035 is designed to operate with electrical sensor phasings of 60°/300° or 120°/240°, and can also efficiently control brush DC motors.

- 10 V to 30 V Operation
- Undervoltage Lockout
- 6.25 V Reference Capable of Supplying Sensor Power
- Fully Accessible Error Amplifier for Closed-Loop Servo Applications
- High Current Drivers can Control MPM3003 MOSFET 3-Phase Bridge
- Cycle-By-Cycle Current Limiting
- Pinned-Out Current Sense Reference
- Internal Thermal Shutdown
- Selectable 60°/300° or 120°/240° Sensor Phasings
- Can Efficiently Control Brush DC Motors with MPM3002 MOSFET H-Bridge

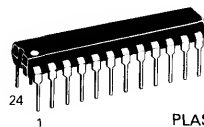


This document contains information on a new product. Specifications and information herein are subject to change without notice.

MC33035

BRUSHLESS DC MOTOR CONTROLLER

SILICON MONOLITHIC INTEGRATED CIRCUIT

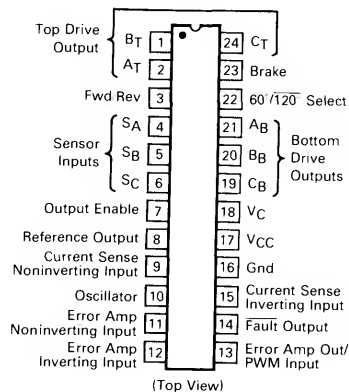


P SUFFIX
 PLASTIC PACKAGE
 CASE 724



DW SUFFIX
 PLASTIC PACKAGE
 CASE 751E
 (SO-24L)

PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Ambient Temperature Range	Package
MC33035P	-40°C to +85°C	Plastic DIP
MC33035DW	-40°C to +85°C	SO-24L

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	V
Digital Inputs (Pins 3, 4, 5, 6, 22, 23)	—	V_{ref}	V
Oscillator Input Current (Source or Sink)	I_{OSC}	30	mA
Error Amp Input Voltage Range (Pins 11, 12, Note 1)	V_{IR}	−3.0 to V	V
Error Amp Output Current (Source or Sink, Note 2)	I_{Out}	10	mA
Current Sense Input Voltage Range (Pins 9, 15)	V_{Sense}	−0.3 to 5.0	V
Fault Output Voltage	$V_{CE(Fault)}$	20	V
Fault Output Sink Current	$I_{Sink(Fault)}$	20	mA
Top Drive Voltage (Pins 1, 2, 24)	$V_{CE(top)}$	40	V
Top Drive Sink Current (Pins 1, 2, 24)	$I_{Sink(Top)}$	50	mA
Bottom Drive Supply Voltage (Pin 18)	V_C	30	V
Bottom Drive Output Current (Source or Sink, Pins 19, 20, 21)	I_{DRV}	100	mA
Power Dissipation and Thermal Characteristics Maximum Power Dissipation @ $T_A = 85^\circ\text{C}$	P_D	867	mW
Thermal Resistance, Junction to Air	$R_{\theta JA}$	75	$^\circ\text{C/W}$
Operating Junction Temperature	T_J	150	$^\circ\text{C}$
Operating Ambient Temperature Range	T_A	−40 to +85	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	−65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($V_{CC} = V_C = 20\text{ V}$, $R_T = 4.7\text{ k}$, $C_T = 10\text{ nF}$, $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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REFERENCE SECTION

Reference Output Voltage ($I_{ref} = 1.0\text{ mA}$) $T_A = 25^\circ\text{C}$ $T_A = -40^\circ\text{C to } +85^\circ\text{C}$	V_{ref}	5.9 5.82	6.24 —	6.5 6.57	V
Line Regulation ($V_{CC} = 10\text{ V to } 30\text{ V}$, $I_{ref} = 1.0\text{ mA}$)	Reg_{line}	—	1.5	30	mV
Load Regulation ($I_{ref} = 1.0\text{ mA to } 20\text{ mA}$)	Reg_{load}	—	16	30	mV
Output Short Circuit Current (Note 3)	I_{SC}	40	75	—	mA
Reference Under Voltage Lockout Threshold	V_{th}	4.0	4.5	5.0	V

ERROR AMPLIFIER

Input Offset Voltage ($T_A = -40^\circ\text{C to } +85^\circ\text{C}$)	V_{IO}	—	0.4	10	mV
Input Offset Current ($T_A = -40^\circ\text{C to } +85^\circ\text{C}$)	I_{IO}	—	8.0	500	nA
Input Bias Current ($T_A = -40^\circ\text{C to } +85^\circ\text{C}$)	I_{IB}	—	−46	−1000	nA
Input Common Mode Voltage Range	V_{ICR}	(0 V to V_{ref})			V
Open-Loop Voltage Gain ($V_O = 3.0\text{ V}$, $R_L = 15\text{ k}$)	A_{VOL}	70	80	—	dB
Input Common Mode Rejection Ratio	$CMRR$	55	86	—	dB
Power Supply Rejection Ratio ($V_{CC} = V_C = 10\text{ V to } 30\text{ V}$)	$PSRR$	65	105	—	dB
Output Voltage Swing High State ($R_L = 15\text{ k to Ground}$) Low State ($R_L = 15\text{ k to } V_{ref}$)	V_{OH} V_{OL}	4.6 —	5.3 0.5	— 1.0	V

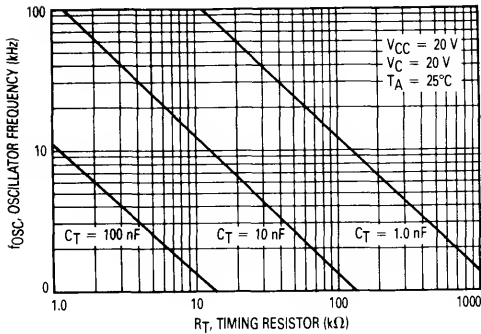
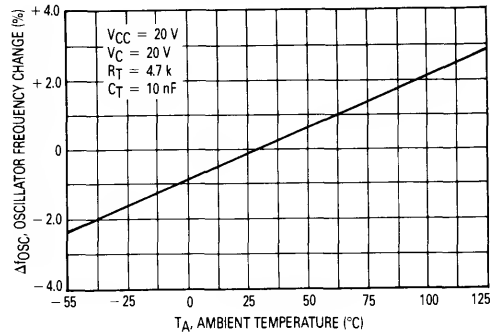
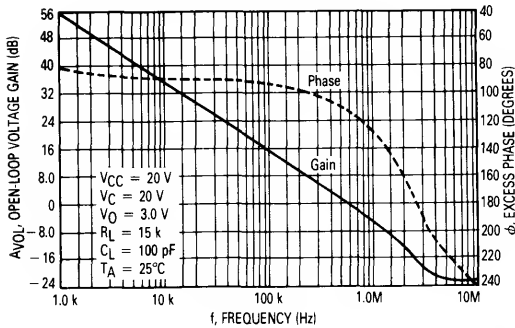
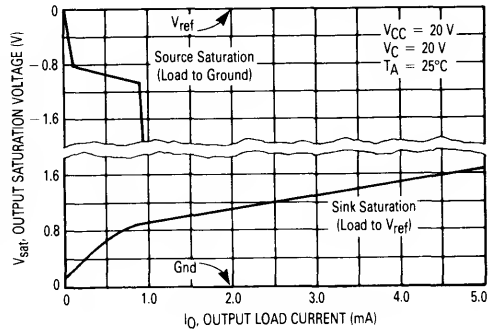
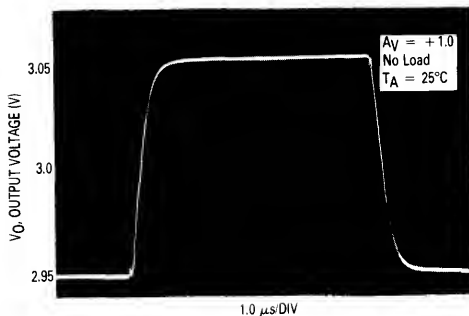
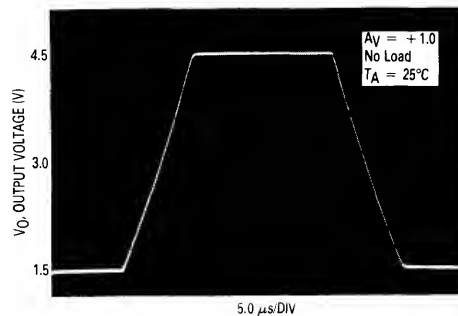
NOTES:

1. The input common mode voltage or input signal voltage should not be allowed to go negative by more than 0.3 V.
2. The compliance voltage must not exceed the range of −0.3 to V_{ref} .
3. Maximum package power dissipation limits must be observed.

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ELECTRICAL CHARACTERISTICS (continued) ($V_{CC} = V_C = 20\text{ V}$, $R_T = 4.7\text{ k}$, $C_T = 10\text{ nF}$, $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR SECTION					
Oscillator Frequency	f_{OSC}	22	25	28	kHz
Frequency Change with Voltage ($V_{CC} = 10\text{ V}$ to 30 V)	$\Delta f_{OSC}/\Delta V$	—	0.01	5.0	%
Sawtooth Peak Voltage	$V_{OSC(P)}$	—	4.1	4.5	V
Sawtooth Valley Voltage	$V_{OSC(V)}$	1.2	1.5	—	V
LOGIC INPUTS					
Input Threshold Voltage (Pins 3, 4, 5, 6, 7, 22, 23) High State Low State	V_{IH} V_{IL}	3.0 —	2.2 1.7	— 0.8	V
Sensor Inputs (Pins 4, 5, 6) High State Input Current ($V_{IH} = 5.0\text{ V}$) Low State Input Current ($V_{IL} = 0\text{ V}$)	I_{IH} I_{IL}	−150 −600	−70 −337	−20 −150	μA
Forward/Reverse and $60^\circ/120^\circ$ Select (Pins 3, 22, 23) High State Input Current ($V_{IH} = 5.0\text{ V}$) Low State Input Current ($V_{IL} = 0\text{ V}$)	I_{IH} I_{IL}	−75 −300	−36 −175	−10 −75	μA
Output Enable High State Input Current ($V_{IH} = 5.0\text{ V}$) Low State Input Current ($V_{IL} = 0\text{ V}$)	I_{IH} I_{IL}	−60 −60	−29 −29	−10 −10	μA
CURRENT-LIMIT COMPARATOR					
Threshold Voltage	V_{th}	85	101	115	mV
Input Common Mode Voltage Range	V_{ICR}	—	3.0	—	V
Input Bias Current	I_{IB}	—	−0.9	−5.0	μA
OUTPUTS AND POWER SECTIONS					
To Drive Output Sink Saturation ($I_{sink} = 25\text{ mA}$)	$V_{CE(sat)}$	—	0.5	1.5	V
Top Drive Output Off-State Leakage ($V_{CE} = 30\text{ V}$)	$I_{DRV(Leak)}$	—	0.06	100	μA
Top Drive Output Switching Time ($C_L = 47\text{ pF}$, $R_L = 1.0\text{ k}$) Rise Time Fall Time	t_r t_f	— —	107 26	300 300	ns
Bottom Drive Output Voltage High State ($V_{CC} = 20\text{ V}$, $V_C = 30\text{ V}$, $I_{source} = 50\text{ mA}$) Low State ($V_{CC} = 20\text{ V}$, $V_C = 30\text{ V}$, $I_{sink} = 50\text{ mA}$)	V_{OH} V_{OL}	($V_{CC} - 2.0$) —	($V_{CC} - 1.1$) 1.5	— 2.0	V
Bottom Drive Output Switching Time ($C_L = 1000\text{ pF}$) Rise Time Fall Time	t_r t_f	— —	38 30	200 200	ns
Fault Output Sink Saturation ($I_{sink} = 16\text{ mA}$)	$V_{CE(sat)}$	—	225	500	mV
Fault Output Off-State Leakage ($V_{CE} = 20\text{ V}$)	$I_{FLT(Leak)}$	—	1.0	100	μA
Under Voltage Lockout Drive Output Enabled (V_{CC} or V_C Increasing) Hysteresis	$V_{th(on)}$ V_H	8.2 0.1	8.9 0.2	10 0.3	V
Power Supply Current Pin 17 ($V_{CC} = V_C = 20\text{ V}$) Pin 17 ($V_{CC} = 20\text{ V}$, $V_C = 30\text{ V}$) Pin 18 ($V_{CC} = V_C = 20\text{ V}$) Pin 18 ($V_{CC} = 20\text{ V}$, $V_C = 30\text{ V}$)	I_{CC} I_C	— — —	12 14 3.5 5.0	16 20 6.0 10	mA

FIGURE 1 — OSCILLATOR FREQUENCY versus TIMING RESISTOR

FIGURE 2 — OSCILLATOR FREQUENCY CHANGE versus TEMPERATURE

FIGURE 3 — ERROR AMP OPEN LOOP GAIN AND PHASE versus FREQUENCY

FIGURE 4 — ERROR AMP OUTPUT SATURATION VOLTAGE versus LOAD CURRENT

FIGURE 5 — ERROR AMP SMALL-SIGNAL TRANSIENT RESPONSE

FIGURE 6 — ERROR AMP LARGE-SIGNAL TRANSIENT RESPONSE


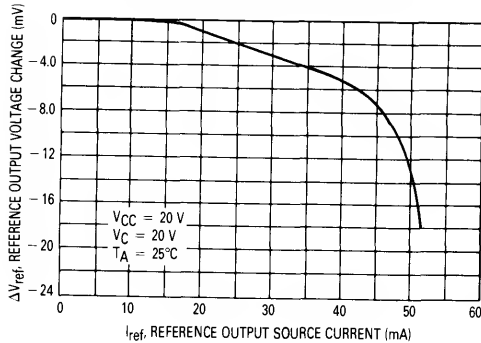
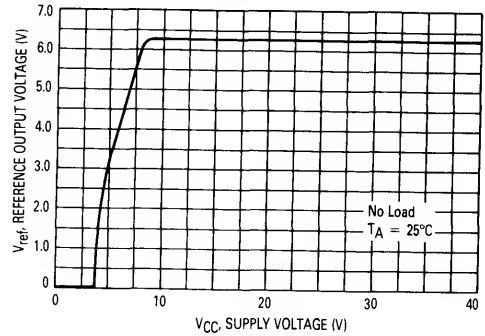
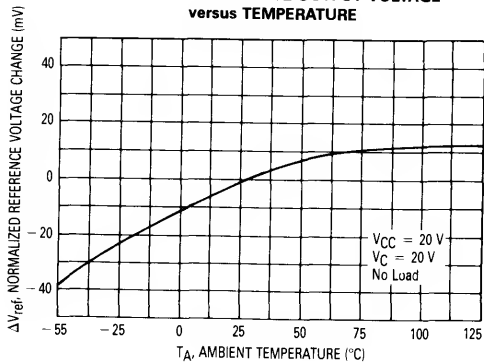
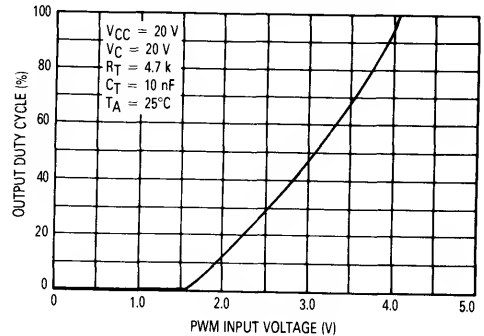
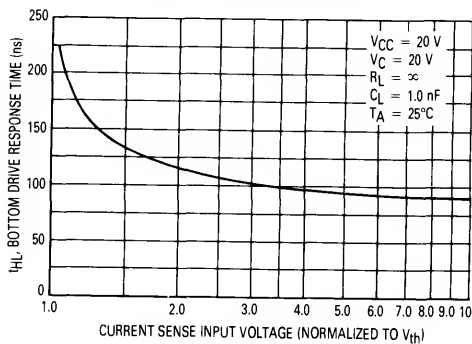
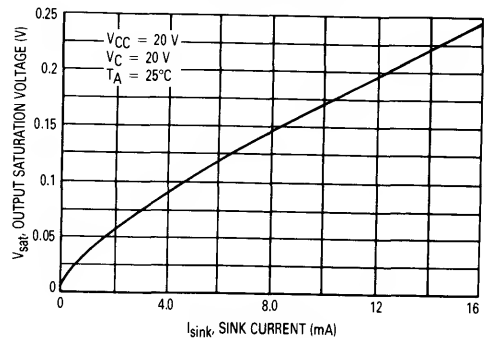
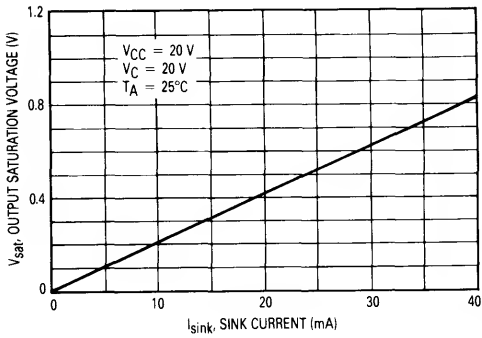
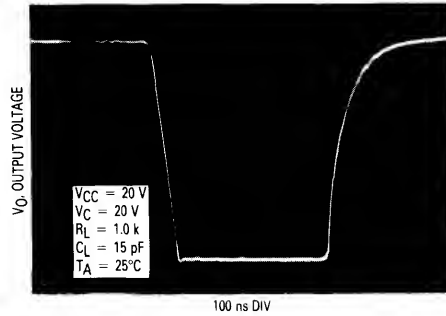
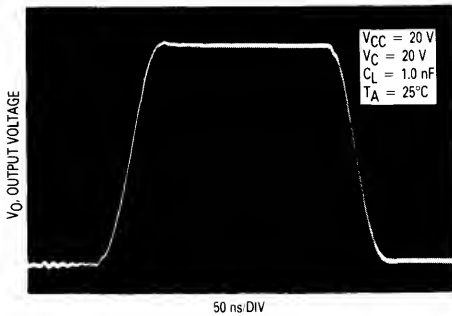
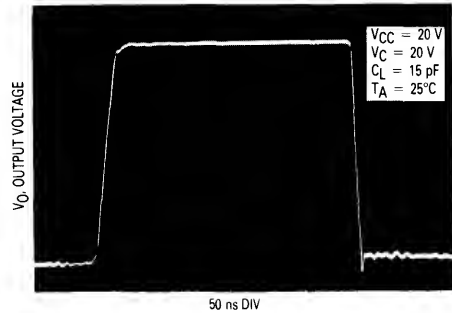
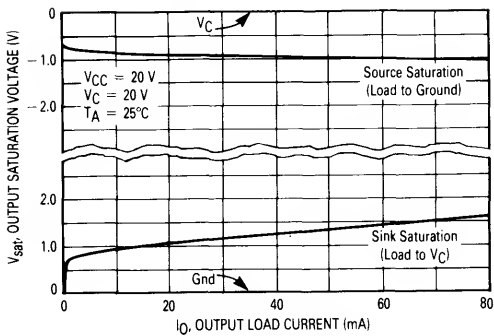
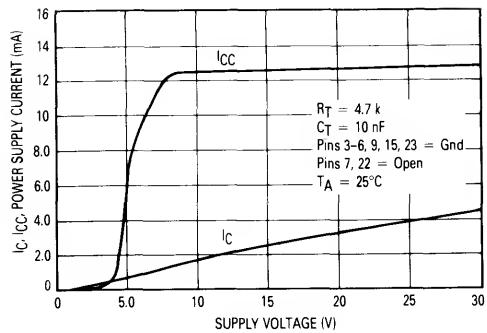
**FIGURE 7 — REFERENCE OUTPUT VOLTAGE CHANGE
versus OUTPUT SOURCE CURRENT**

**FIGURE 8 — REFERENCE OUTPUT VOLTAGE
versus SUPPLY VOLTAGE**

**FIGURE 9 — REFERENCE OUTPUT VOLTAGE
versus TEMPERATURE**

**FIGURE 10 — OUTPUT DUTY CYCLE versus
PWM INPUT VOLTAGE**

**FIGURE 11 — BOTTOM DRIVE RESPONSE TIME versus
CURRENT SENSE INPUT VOLTAGE**

**FIGURE 12 — FAULT OUTPUT SATURATION
versus SINK CURRENT**


FIGURE 13 — TOP DRIVE OUTPUT SATURATION VOLTAGE versus SINK CURRENT

FIGURE 14 — TOP DRIVE OUTPUT WAVEFORM

FIGURE 15 — BOTTOM DRIVE OUTPUT WAVEFORM

FIGURE 16 — BOTTOM DRIVE OUTPUT WAVEFORM

FIGURE 17 — BOTTOM DRIVE OUTPUT SATURATION VOLTAGE versus LOAD CURRENT

FIGURE 18 — POWER AND BOTTOM DRIVE SUPPLY CURRENT versus SUPPLY VOLTAGE


PIN FUNCTION DESCRIPTION

Pin No.	Function	Description
1, 2, 24	B _T , A _T , C _T	These three open collector Top Drive Outputs are designed to drive the external upper power switch transistors.
3	FWD/REV	The Forward/Reverse Input is used to change the direction of motor rotation.
4, 5, 6	S _A , S _B , S _C	These three Sensor Inputs control the commutation sequence.
7	Output Enable	A logic high at this input causes the motor to run, while a low causes it to coast.
8	Reference Output	This output provides charging current for the oscillator timing capacitor C _T and a reference for the error amplifier. It may also serve to furnish sensor power.
9	Current Sense (Noninverting Input)	A 100 mV signal, with respect to pin 15, at this input terminates output switch conduction during a given oscillator cycle. This pin normally connects to the top side of the current sense resistor.
10	Oscillator	The Oscillator frequency is programmed by the values selected for the timing components, R _T and C _T .
11	Error Amp (Noninverting Input)	This input is normally connected to the speed set potentiometer.
12	Error Amp (Inverting Input)	This input is normally connected to the Error Amp Output in open-loop applications.
13	Error Amp Output/PWM Input	This pin is available for compensation in closed-loop applications.
14	Fault Output	This open collector output is active low during one or more of the following conditions: Invalid Sensor Input code, Enable Input at logic 0, Current Sense Input greater than 100 mV (pin 9 with respect to pin 15), Undervoltage Lockout activation, and Thermal Shutdown.
15	Current Sense (Inverting Input)	Reference pin for internal 100 mV threshold. This pin is normally connected to the bottom side of the current sense resistor.
16	Ground	This pin supplies a ground for the control circuit and should be referenced back to the power source ground.
17	V _{CC}	This pin is the positive supply of the control IC. The controller is functional over a minimum V _{CC} range of 10 V to 30 V.
18	V _C	The high state (V _{OH}) of the Bottom Drive Outputs is set by the voltage applied to this pin. The controller is operational over a minimum V _C range of 10 V to 30 V.
19, 20, 21	C _B , B _B , A _B	These three totem pole Bottom Drive Outputs are designed for direct drive of the external bottom power switch transistors.
22	60°/120° Select	The electrical state of this pin configures the control circuit operation for either 60° (high state) or 120° (low state) sensor electrical phasing inputs.
23	Brake Input	A logic low state at this input allows the motor to run, while a high state does not allow motor operation and if operating causes rapid deceleration.

INTRODUCTION

The MC33035 is one of a series of high performance monolithic DC brushless motor controllers produced by Motorola. It contains all of the functions required to implement a full-featured, open-loop, three or four phase motor control system. In addition, the controller can be made to operate DC brush motors. Constructed with Bipolar Analog technology, it offers a high degree of performance and ruggedness in hostile industrial environments. The MC33035 contains a rotor position decoder for proper commutation sequencing, a temperature compensated reference capable of supplying a sensor power, a frequency programmable sawtooth oscillator, a fully accessible error amplifier, a pulse width modulator comparator, three open collector top drive outputs, and three high current totem pole bottom driver outputs ideally suited for driving power MOSFETs.

Included in the MC33035 are protective features consisting of undervoltage lockout, cycle by cycle current limiting with a selectable time delayed latched shutdown mode, internal thermal shutdown, and a unique fault output that can easily be interfaced to a microprocessor controller.

Typical motor control functions include open-loop speed control, forward or reverse rotation, run enable, and dynamic braking. In addition, the MC33035 has a 60°/120° select pin which configures the rotor position decoder for either 60° or 120° sensor electrical phasing inputs.

FUNCTIONAL DESCRIPTION

A representative internal block diagram is shown in Figure 19 with various applications shown in Figures 36, 38, 42, 44, 45, and 46. A discussion of the features and function of each of the internal blocks given below is referenced to Figures 19 and 36.

Rotor Position Decoder

An internal rotor position decoder monitors the three sensor inputs (Pins 4, 5, 6) to provide the proper sequencing of the top and bottom drive outputs. The sensor inputs are designed to interface directly with open collector type Hall Effect switches or opto slotted couplers. Internal pull-up resistors are included to minimize the required number of external components. The inputs are TTL compatible, with their thresholds typically at 2.2 volts. The MC33035 series is designed to control three phase motors and operate with four of the most common conventions of sensor phasing. A 60°/120° select (Pin 22) is conveniently provided which affords the MC33035 to configure itself to control motors having either 60°, 120°, 240° or 300° electrical sensor phasing. With three sensor inputs there are eight possible input code combinations, six of which are valid rotor positions. The remaining two codes are invalid and are usually caused by an open or shorted sensor line. When an invalid input condition exists, the $\overline{\text{Fault}}$ output is activated and the drive outputs are disabled. With six valid input codes, the decoder can resolve the motor rotor position to within a window of 60 electrical degrees.

The forward/reverse input (Pin 3) is used to change the direction of motor rotation by reversing the voltage across the stator winding. When the input changes state, from high to low with a given sensor input code (for example 100), the enabled top and bottom drive outputs with the same alpha designation are exchanged (A_T to A_B , B_T to B_B , C_T to C_B). In effect the commutation sequence is reversed and the motor changes directional rotation.

Motor on/off control is accomplished by the output enable (Pin 7). When left disconnected, an internal 25 μA current source enables sequencing of the top and bottom drive outputs. When grounded, the top drive outputs turn off and the bottom drives are forced low, causing the motor to coast and the Fault output to activate.

Dynamic motor braking allows an additional margin of safety to be designed into the final product. Braking is accomplished by placing the brake input (Pin 23) in a high state. This causes the top drive outputs to turn off and the bottom drives to turn on, shorting the motor-generated back EMF. The brake input has unconditional priority over all other inputs. The internal 40 k Ω pull-up resistor simplifies interfacing with the system safety-switch by insuring brake activation if opened or disconnected. The commutation logic truth table is shown in Figure 20. A four input NOR gate is used to monitor the brake input and the inputs to the three top drive output transistors. Its purpose is to disable braking until the top drive outputs attain a high state. This helps to prevent simultaneous conduction of the top and bottom power switches. In half wave motor drive applications, the top drive outputs are not required and are normally left disconnected. Under these conditions braking will still be accomplished since the NOR gate senses the base voltage to the top drive output transistors.

Error Amplifier

A high performance, fully compensated error amplifier with access to both inputs and output (Pins 11, 12, 13) is provided to facilitate the implementation of closed-loop motor speed control. The amplifier features a typical DC voltage gain of 80 dB, 0.6 MHz gain bandwidth, and a wide input common mode voltage range that extends from ground to V_{ref} . In most open-loop speed control applications, the amplifier is configured as a unity gain voltage follower with the non-inverting input connected to the speed set voltage source. Additional configurations are shown in Figures 31 through 35.

Oscillator

The frequency of the internal ramp oscillator is programmed by the values selected for timing components R_T and C_T . Capacitor C_T is charged from the reference output (Pin 8) through resistor R_T and discharged by an internal discharge transistor. The ramp peak and valley voltages are typically 4.1 V and 1.5 V respectively. To provide a good compromise between audible noise and output switching efficiency, an oscillator frequency in the range of 20 kHz to 30 kHz is recommended. Refer to Figure 1 for component selection.

MC33035

FIGURE 19 — REPRESENTATIVE BLOCK DIAGRAM

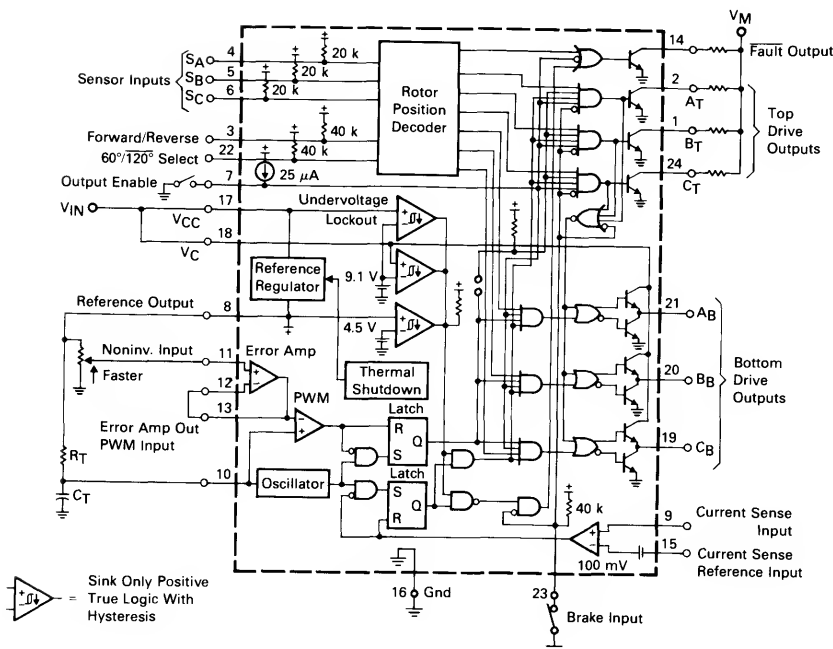


FIGURE 20 — THREE PHASE, SIX STEP COMMUTATION TRUTH TABLE (Note 1)

Inputs (Note 2)										Outputs (Note 3)						
Sensor Electrical Phasing (Note 4)										Top Drives			Bottom Drives			Fault
SA	SB	SC	SA	SB	SC	F/R	Enable	Brake	Current Sense	AT	BT	CT	AB	BB	CB	
1	0	0	1	0	0	1	1	0	0	0	1	1	0	0	1	1
1	1	0	1	1	0	1	1	0	0	1	1	0	0	0	1	(Note 5)
1	1	1	0	1	0	1	1	0	0	1	0	1	1	0	0	F/R = 1
0	1	1	0	1	1	1	1	0	0	1	1	0	1	0	0	1
0	0	1	0	0	1	1	1	0	0	1	1	0	0	1	0	1
0	0	0	1	0	1	1	1	0	0	0	1	1	0	1	0	1
1	0	0	1	0	0	0	1	0	0	1	1	0	1	0	0	1
1	1	0	1	1	0	0	1	0	0	1	1	0	0	1	0	(Note 5)
1	1	1	0	1	0	0	1	0	0	0	1	1	0	1	0	F/R = 0
0	1	1	0	1	1	0	1	0	0	0	1	1	0	0	1	1
0	0	1	0	0	1	0	1	0	0	1	0	1	0	0	1	1
0	0	0	1	0	1	0	1	0	0	1	0	1	1	0	0	1
1	0	1	1	1	1	X	X	0	X	1	1	1	0	0	0	(Note 6)
0	1	0	1	0	0	X	X	0	X	1	1	1	0	0	0	Brake = 0
1	0	1	1	1	1	X	X	1	X	1	1	1	1	1	1	(Note 7)
0	1	0	1	0	0	X	X	1	X	1	1	1	1	1	1	Brake = 1
V	V	V	V	V	V	X	1	1	X	1	1	1	1	1	1	(Note 8)
V	V	V	V	V	V	X	0	1	X	1	1	1	1	1	1	(Note 9)
V	V	V	V	V	V	X	0	0	X	1	1	1	0	0	0	(Note 10)
V	V	V	V	V	V	X	1	0	1	1	1	1	0	0	0	(Note 11)

NOTES:

- V = Any one of six valid sensor or drive combinations.
- X = Don't care.
- The digital inputs (Pins 3, 4, 5, 6, 7, 22, 23) are all TTL compatible. The current sense input (Pin 9) has a 100 mV threshold with respect to Pin 15. A logic 0 for this input is defined as < 85 mV, and a logic 1 is > 115 mV.
- The fault and top drive outputs are open collector design and active in the low (0) state.
- With 60°/120° select (Pin 22) in the high (1) state, configuration is for 60° sensor electrical phasing inputs. With Pin 22 in low (0) state, configuration is for 120° sensor electrical phasing inputs.
- Valid 60° or 120° sensor combinations for corresponding valid top and bottom drive outputs.
- Invalid sensor inputs with brake = 0; All top and bottom drives off, Fault low.
- Invalid sensor inputs with brake = 1; All top drives off, all bottom drives on, Fault low.
- Valid 60° or 120° sensor inputs with brake = 1; All top drives off, all bottom drives on, Fault high.
- Valid sensor inputs with brake = 1 and enable = 0; All top drives off, all bottom drives on, Fault low.
- Valid sensor inputs with brake = 0 and enable = 0; All top and bottom drives off, Fault low.
- All bottom drives off, Fault low.

Pulse Width Modulator

The use of pulse width modulation provides an energy efficient method of controlling the motor speed by varying the average voltage applied to each stator winding during the commutation sequence. As C_T discharges, the oscillator sets both latches, allowing conduction of the top and bottom drive outputs. The PWM comparator resets the upper latch, terminating the bottom drive output conduction when the positive-going ramp of C_T becomes greater than the error amplifier output. The pulse width modulator timing diagram is shown in Figure 21. Pulse width modulation for speed control appears only at the bottom drive outputs.

Current Limit

Continuous operation of a motor that is severely overloaded results in overheating and eventual failure. This destructive condition can best be prevented with the use of cycle-by-cycle current limiting. That is, each on-cycle is treated as a separate event. Cycle-by-cycle current limiting is accomplished by monitoring the stator current build-up each time an output switch conducts, and upon sensing an over current condition, immediately turning off the switch and holding it off for the remaining duration of the oscillator ramp-up period. The stator current is converted to a voltage by inserting a ground-referenced sense resistor R_S (Figure 36) in series with the three bottom switch transistors (Q_4 , Q_5 , Q_6). The voltage across the sense resistor is directly monitored by the current sense comparator inputs (Pins 9 and 15) and compared to the internal 100 mV reference. The current sense comparator inputs have an input common mode input range of approximately 3.0 volts. If the 100 mV current sense threshold is exceeded, the comparator resets the lower sense latch and terminates output switch conduction. The value for the current sense resistor is:

$$R_S = \frac{0.1}{I_{\text{stator(max)}}$$

The Fault output activates during an over current condition. The dual-latch PWM configuration ensures that

only one single output conduction pulse occurs during any given oscillator cycle, whether terminated by the output of the error amp or the current limit comparator.

Reference

The on-chip 6.25 V regulator (Pin 8) provides charging current for the oscillator timing capacitor, a reference for the error amplifier, and can supply 20 mA of current suitable for directly powering sensors in low voltage applications. In higher voltage applications it may become necessary to transfer the power dissipated by the regulator off the IC. This is easily accomplished with the addition of an external pass transistor as shown in Figure 22. A 6.25 V reference level was chosen to allow implementation of the simpler NPN circuit, where $V_{\text{ref}} - V_{\text{BE}}$ exceeds the minimum voltage required by Hall Effect sensors over temperature. With proper transistor selection, and adequate heatsinking, up to one amp of load current can be obtained.

FIGURE 22 — REFERENCE OUTPUT BUFFERS

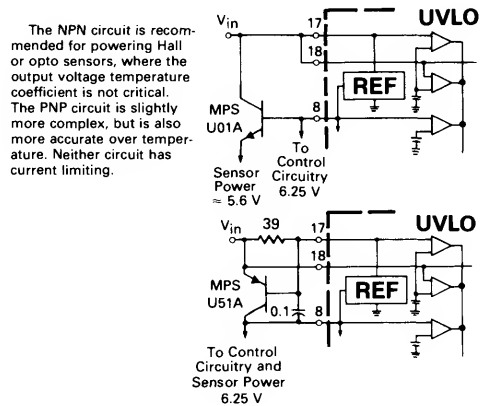
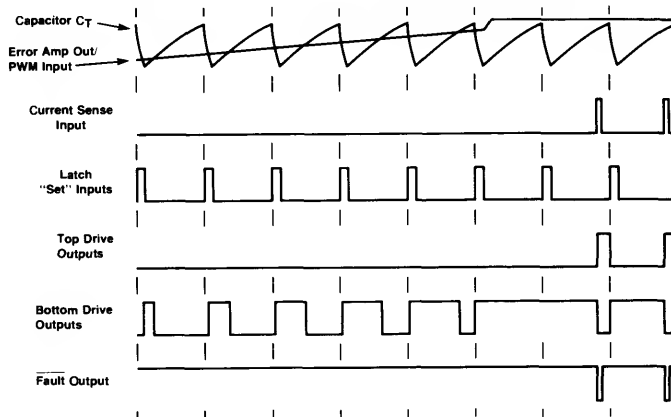


FIGURE 21 — PULSE WIDTH MODULATOR TIMING DIAGRAM



Undervoltage Lockout

A triple Undervoltage Lockout has been incorporated to prevent damage to the IC and the external power switch transistors. Under low power supply conditions, it guarantees that the IC and sensors are fully functional, and that there is sufficient bottom drive output voltage. The positive power supplies to the IC (V_{CC}) and the bottom drives (V_C) are each monitored by separate comparators that have their thresholds at 9.1 V. This level ensures sufficient gate drive necessary to attain low $r_{DS(on)}$ when driving standard power MOSFET devices. When directly powering the Hall sensors from the reference, improper sensor operation can result, if the reference output voltage falls below 4.5 V. A third comparator is used to detect this condition. If one or more of the comparators detects an undervoltage condition, the Fault output is activated, the top drives are turned off and the bottom drive outputs are held in a low state. Each of the comparators contain hysteresis to prevent oscillations when crossing their respective thresholds.

Fault Output

The open collector Fault output (Pin 14) was designed to provide diagnostic information in the event of a system malfunction. It has a sink current capability of 16 mA and can directly drive a light emitting diode for visual indication. Additionally, it is easily interfaced with TTL/CMOS logic for use in a microprocessor controlled system. The Fault output is active low when one or more of the following conditions occur:

- 1) Invalid Sensor Input code.
- 2) Enable Input at logic [0].
- 3) Current Sense Input greater than 100 mV.
- 4) Undervoltage Lockout, activation of one or more of the comparators.
- 5) Thermal Shutdown, maximum junction temperature being exceeded.

This unique output can also be used to distinguish between motor start-up or sustained operation in an overloaded condition. With the addition of an R/C network between the Fault output and the enable input, it is possible to create a time-delayed latched shutdown for overcurrent. The added circuitry shown in Figure 23, makes easy starting of motor systems which have high inertial loads by providing additional starting torque, while still preserving overcurrent protection. This task is accomplished by setting the current limit to a higher than nominal value for a predetermined time. During an excessively long overcurrent condition, capacitor C_{DLY} will charge causing the enable input to cross its threshold to a low state. A latch is then formed by the positive feedback loop from the Fault output to the enable input. Once set, by the current sense input, it can only be reset by shorting C_{DLY} or cycling the power supplies.

Drive Outputs

The three top drive outputs (Pins 1, 2, 24) are open collector NPN transistors capable of sinking 50 mA with a minimum breakdown of 30 volts. Interfacing into higher voltage applications is easily accomplished with the circuits shown in Figures 24 and 25.

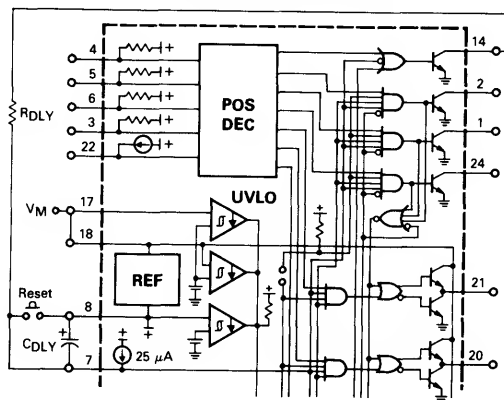
The three totem pole bottom drive outputs (Pins 19, 20, 21) are particularly suited for direct drive of 'N' channel MOSFETs or NPN bipolar transistors (Figures 26, 27, 28 and 29). Each output is capable of sourcing and sinking up to 100 mA. Power for the bottom drives is supplied from V_C (Pin 18). This separate supply input allows the designer added flexibility in tailoring the drive voltage, independent of V_{CC} . A zener clamp should be connected to this input when driving power MOSFETs in systems where V_{CC} is greater than 20 V so as to prevent rupture of the MOSFET gates.

The control circuitry ground (Pin 16) and current sense inverting input (Pin 15) must return on separate paths to the central input source ground.

Thermal Shutdown

Internal thermal shutdown circuitry is provided to protect the IC in the event the maximum junction temperature is exceeded. When activated, typically at 170°C, the IC acts as though the enable input was grounded.

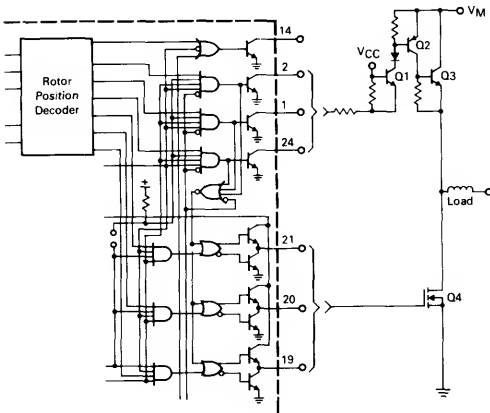
FIGURE 23 — TIMED DELAYED LATCHED OVER CURRENT SHUTDOWN



$$t_{DLY} \approx R_{DLY} C_{DLY} \ln \left(\frac{V_{ref} - (I_{IL} \text{ enable } R_{DLY})}{V_{th} \text{ enable} - (I_{IL} \text{ enable } R_{DLY})} \right)$$

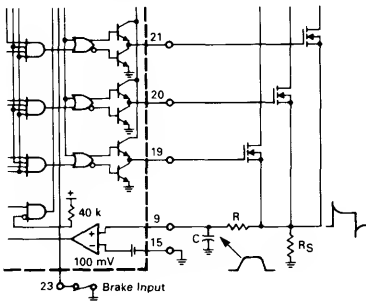
$$\approx R_{DLY} C_{DLY} \ln \left(\frac{6.25 - (20 \times 10^{-6} R_{DLY})}{1.4 - (20 \times 10^{-6} R_{DLY})} \right)$$

FIGURE 24 — HIGH VOLTAGE INTERFACE WITH NPN POWER TRANSISTORS



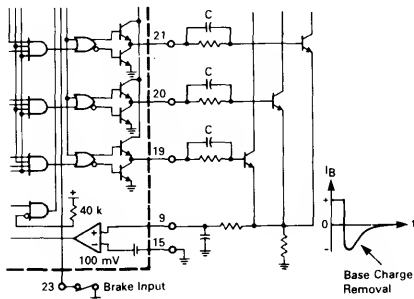
Transistor Q1 is a common base stage used to level shift from V_{CC} to the high motor voltage, V_M . The collector diode is required if V_{CC} is present while V_M is low.

FIGURE 26 — CURRENT WAVEFORM SPIKE SUPPRESSION



The addition of the RC filter will eliminate current-limit instability caused by the leading edge spike on the current waveform. Resistor R_S should be a low inductance type.

FIGURE 28 — BIPOLAR TRANSISTOR DRIVE



The totem-pole output can furnish negative base current for enhanced transistor turn-off, with the addition of capacitor C.

FIGURE 25 — HIGH VOLTAGE INTERFACE WITH 'N' CHANNEL POWER MOSFETs

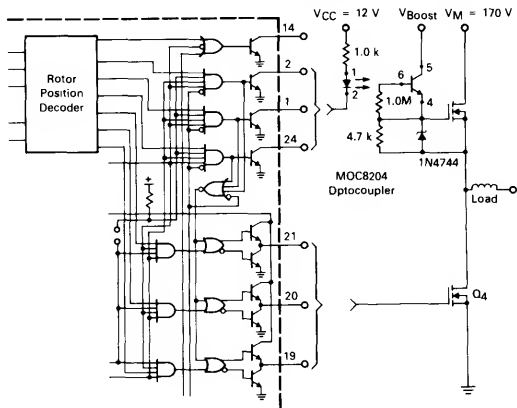
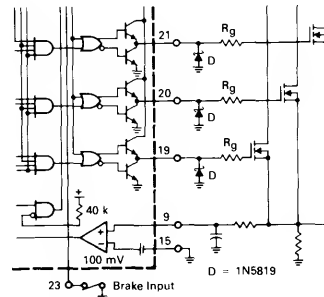
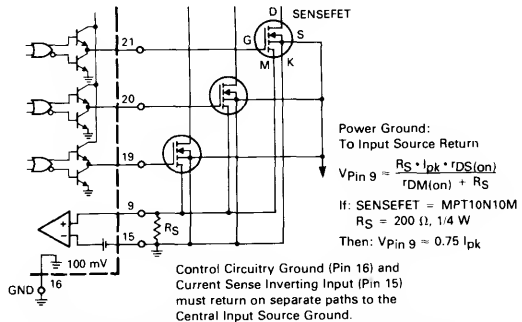


FIGURE 27 — MOSFET DRIVE PRECAUTIONS



Series gate resistor R_g will damp any high frequency oscillations caused by the MOSFET input capacitance and any series wiring induction in the gate-source circuit. Diode D is required if the negative current into the Bottom Drive Outputs exceeds 50 mA.

FIGURE 29 — CURRENT SENSING POWER MOSFETs

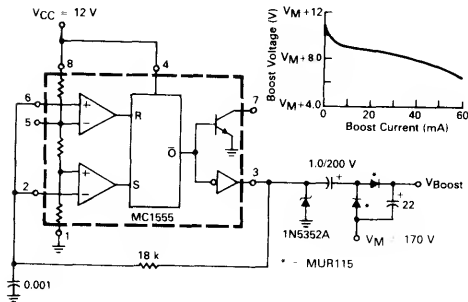


Power Ground:
To Input Source Return
 $V_{Pin 9} = \frac{R_S \cdot I_{pk} \cdot r_{DS(on)}}{r_{DM(on)} + R_S}$
If: SENSEFET = MPT10N10M
 $R_S = 200 \Omega$, 1/4 W
Then: $V_{Pin 9} = 0.75 I_{pk}$

Control Circuitry Ground (Pin 16) and Current Sense Inverting Input (Pin 15) must return on separate paths to the Central Input Source Ground.

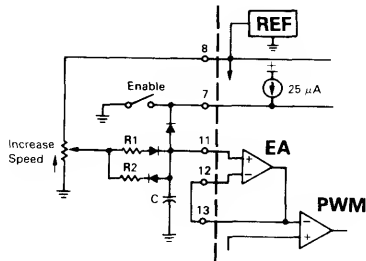
Virtually lossless current sensing can be achieved with the implementation of SENSEFET power switches.

FIGURE 30 — HIGH VOLTAGE BOOST SUPPLY



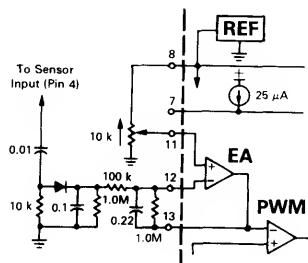
This circuit generates V_{Boost} for Figure 25.

FIGURE 32 — CONTROLLED ACCELERATION/DECELERATION



Resistor R1 with capacitor C sets the acceleration time constant while R2 controls the deceleration. The values of R1 and R2 should be at least ten times greater than the speed set potentiometer to minimize time constant variations with different speed settings.

FIGURE 34 — CLOSED LOOP SPEED CONTROL



The rotor position sensors can be used as a tachometer. By differentiating the positive-going edges and then integrating them over time, a voltage proportional to speed can be generated. The error amp compares this voltage to that of the speed set to control the PWM.

FIGURE 31 — DIFFERENTIAL INPUT SPEED CONTROLLER

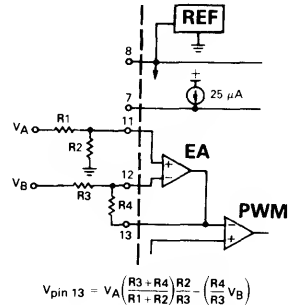
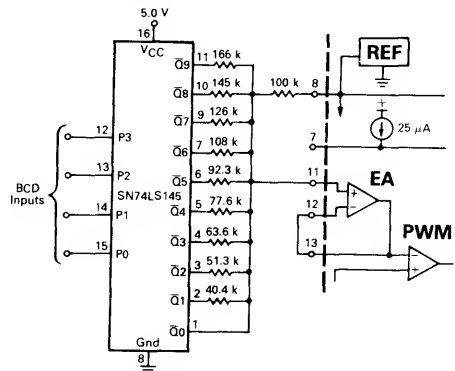
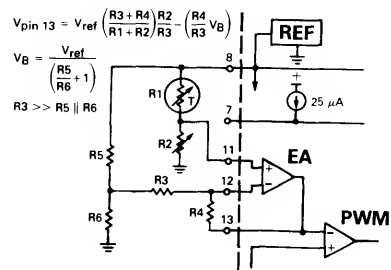


FIGURE 33 — DIGITAL SPEED CONTROLLER



The SN74LS145 is an open collector BCD to One of Ten decoder. When connected as shown, input codes 0000 through 1001 steps the PWM in increments of approximately 10% from 0 to 90% on-time. Input codes 1010 through 1111 will produce 100% on-time or full motor speed.

FIGURE 35 — CLOSED LOOP TEMPERATURE CONTROL



This circuit can control the speed of a cooling fan proportional to the difference between the sensor and set temperatures. The control loop is closed as the forced air cools the NTC thermistor. For controlled heating applications, exchange the positions of R1 and R2.

SYSTEM APPLICATIONS

Three Phase Motor Commutation

The three phase application shown in Figure 36 is a full-featured open-loop motor controller with full wave, six step drive. The upper power switch transistors are Darlington's while the lower devices are power MOSFETs. Each of these devices contains an internal parasitic catch diode that is used to return the stator inductive energy back to the power supply. The outputs are capable of driving a delta or wye connected stator, and a grounded neutral wye if split supplies are used. At any given rotor position, only one top and one bottom power switch (of different totem poles) is enabled. This configuration switches both ends of the stator winding from supply to ground which causes the current flow to be bidirectional or full wave. A leading edge spike is usually present on the current waveform and can cause a current-limit instability. The spike can be eliminated by adding an RC filter in series with the current sense input. Using a low inductance type resistor for R_S will also aid in spike reduction. Care must be

taken in the selection of the bottom power switch transistors so that the current during braking does not exceed the device rating. During braking, the peak current generated is limited only by the series resistance of the conducting bottom switch and winding.

$$I_{\text{peak}} = \frac{V_M + \text{EMF}}{R_{\text{switch}} + R_{\text{winding}}}$$

If the motor is running at maximum speed with no load, the generated back EMF can be as high as the supply voltage, and at the onset of braking the peak current may approach twice the motor stall current. Figure 37 shows the commutation waveforms over two electrical cycles. The first cycle (0° to 360°) depicts motor operation at full speed while the second cycle (360° to 720°) shows a reduced speed with about 50 percent pulse width modulation. The current waveforms reflect a constant torque load and are shown synchronous to the commutation frequency for clarity.

FIGURE 36 — THREE PHASE, SIX STEP, FULL WAVE MOTOR CONTROLLER

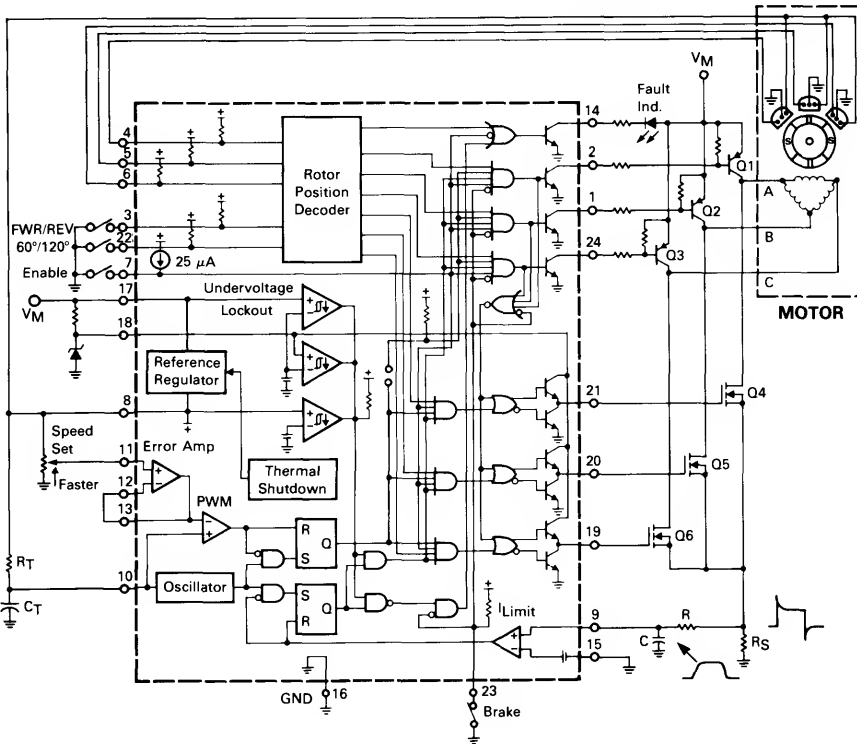


FIGURE 37 — THREE PHASE, SIX STEP, FULL WAVE COMMUTATION WAVEFORMS

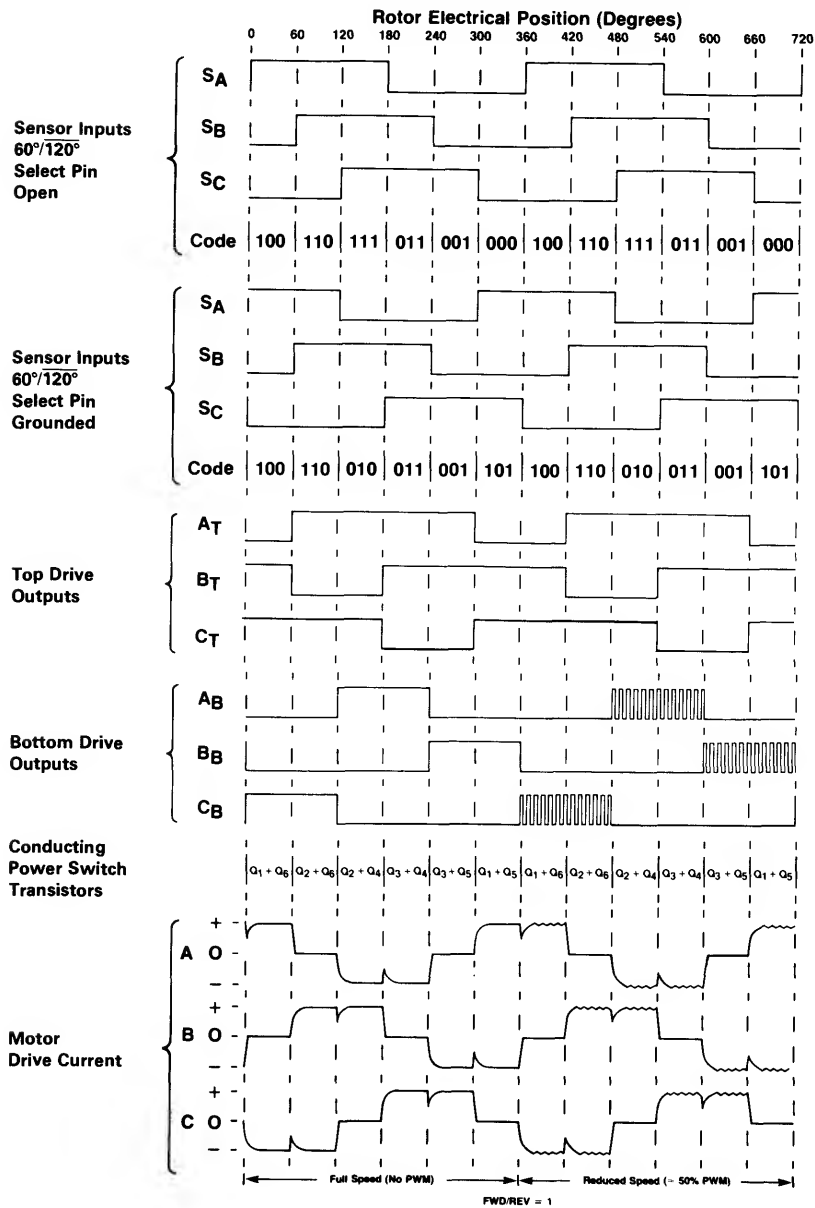
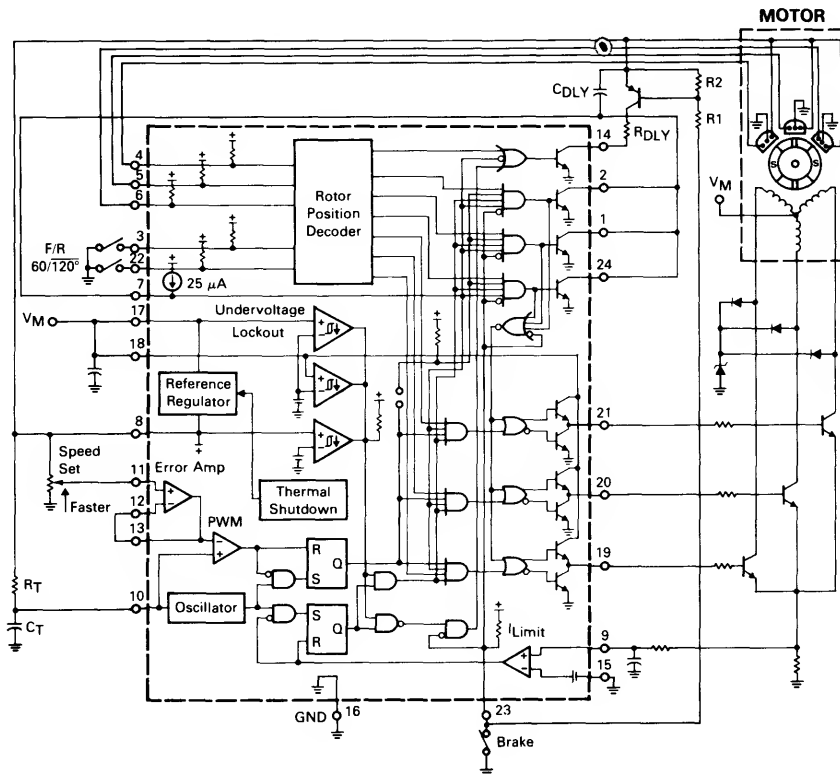


Figure 38 shows a three phase, three step, half wave motor controller. This configuration is ideally suited for automotive and other low voltage applications since there is only one power switch voltage drop in series with a given stator winding. Current flow is unidirectional or half wave because only one end of each winding is switched. Continuous braking with the typical half wave arrangement presents a motor overheating problem since stator current is limited only by the winding resistance. This is due to the lack of upper power switch transistors, as in the full wave circuit, used to disconnect the windings from the supply voltage V_M . A unique

solution is to provide braking until the motor stops and then turn off the bottom drives. This can be accomplished by using the Fault output in conjunction with the Enable input as an over current timer. Components R_{DLY} and C_{DLY} are selected to give the motor sufficient time to stop before latching the Enable input and the top drive AND gates low. When enabling the motor, the brake switch is closed and the PNP transistor along with resistors R_1 and R_{DLY} are used to reset the latch by discharging C_{DLY} . The stator flyback voltage is clamped by a single zener and three diodes.

FIGURE 38 — THREE PHASE, THREE STEP, HALF WAVE MOTOR CONTROLLER



The MC33035, by itself, is only capable of open loop motor speed control. For closed loop motor speed control, the MC33035 requires an input voltage proportional to the motor speed. Traditionally this has been accomplished by means of a tachometer to generate the motor speed feedback voltage. Figure 39 shows an application whereby an MC33039, powered from the 6.25 volt reference (Pin 8) of the MC33035, is used to generate the required feedback voltage without the need of a costly tachometer. The same Hall sensor signals used by the MC33035 for rotor position decoding are utilized by the MC33039. Every positive or negative going transition of the Hall sensor signals on any of the sensor lines causes the MC33039 to produce an output pulse of defined amplitude and time duration, as determined by the external resistor R1 and capacitor C1. The output train

The system shown in Figure 39 is designed for a motor having 120/240 degrees Hall sensor electrical phasing. The system can easily be modified to accommodate 60/300 degree Hall sensor electrical phasing by removing the jumper (J2) at Pin 22 of the MC33035.

[illegible]

Sensor Phasing Comparison

There are four conventions used to establish the relative phasing of the sensor signals in three phase motors. With six step drive, an input signal change must occur every 60 electrical degrees, however, the relative signal phasing is dependent upon the mechanical sensor placement. A comparison of the conventions in electrical degrees is shown in Figure 40. From the sensor phasing table, Figure 41, note that the order of input codes for 60° phasing is the reverse of 300°. This means the MC33035, when configured for 60° sensor electrical phasing, will equally operate a motor with either 60° or 300° sensor electrical phasing, but resulting in opposite directions of rotation. The same is true for the part when it is configured for 120° sensor electrical phasing; the motor will equally operate, but will result in opposite directions of rotation for 120° for 240° conventions.

FIGURE 40 — SENSOR PHASING COMPARISON

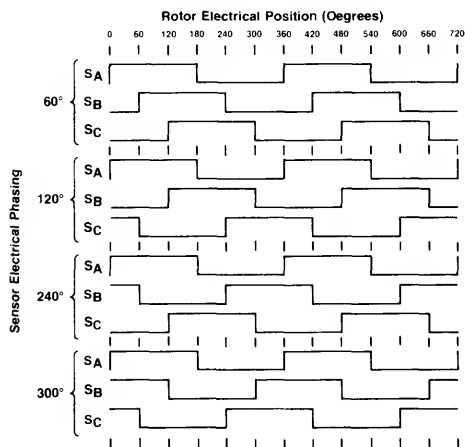


FIGURE 41 — SENSOR PHASING TABLE

Sensor Electrical Phasing (Degrees)											
60°			120°			240°			300°		
SA	SB	SC	SA	SB	SC	SA	SB	SC	SA	SB	SC
1	0	0	1	0	1	1	1	0	1	1	1
1	1	0	1	0	0	1	0	0	1	1	0
1	1	1	1	1	0	1	0	1	1	0	0
0	1	1	0	1	0	0	0	1	0	0	0
0	0	1	0	1	1	0	1	1	0	0	1
0	0	0	0	0	1	0	1	0	0	1	1

In this data sheet, the rotor position is always given in electrical degrees since the mechanical position is a function of the number of rotating magnetic poles. The relationship between the electrical and mechanical position is:

$$\text{Electrical Degrees} = \text{Mechanical Degrees} \left(\frac{\# \text{Rotor Poles}}{2} \right)$$

An increase in the number of magnetic poles causes more electrical revolutions for a given mechanical revolution. General purpose three phase motors typically contain a four pole rotor which yields two electrical revolutions for one mechanical.

Two and Four Phase Motor Commutation

The MC33035 is also capable of providing a four step output that can be used to drive two or four phase motors. The truth table in Figure 42 shows that by connecting sensor inputs SB and SC together, it is possible to truncate the number of drive output states from six to four. The output power switches are connected to BT, CT, BB, and CB. Figure 43 shows a four phase, four step, full wave motor control application. Power switch transistors Q1 through Q8 are Darlington type, each with an internal parasitic catch diode. With four step drive, only two rotor position sensors spaced at 90 electrical degrees are required. The commutation waveforms are shown in Figure 44.

Figure 45 shows a four phase, four step, half wave motor controller. It has the same features as the circuit in Figure 38, except for the deletion of speed control and braking.

FIGURE 42 — TWO AND FOUR PHASE, FOUR STEP, COMMUTATION TRUTH TABLE

MC33035 (60°/120° Select Pin Open)					
Inputs			Outputs		
Sensor Electrical Spacing* = 90°		F/R	Top Drives		Bottom Drives
SA	SB		BT	CT	BB CB
1	0	1	1	1	0 1
1	1	1	0	1	0 0
0	1	1	1	0	0 0
0	0	1	1	1	1 0
1	0	0	1	0	0 0
1	1	0	1	1	1 0
0	1	0	1	1	0 1
0	0	0	0	1	0 0

*With MC33035 sensor input SB connected to SC

FIGURE 43 — FOUR PHASE, FOUR STEP, FULL WAVE CONTROLLER

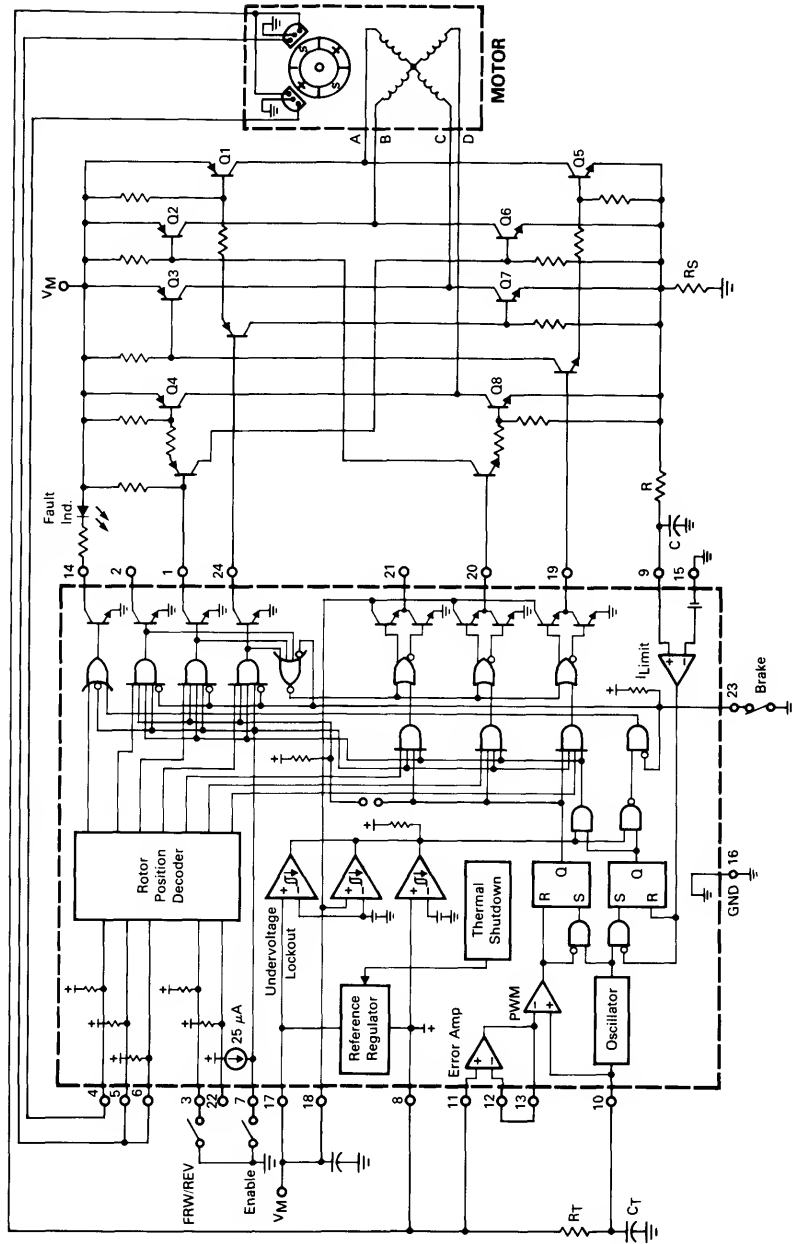


FIGURE 44 — FOUR PHASE, FOUR STEP, FULL WAVE MOTOR CONTROLLER

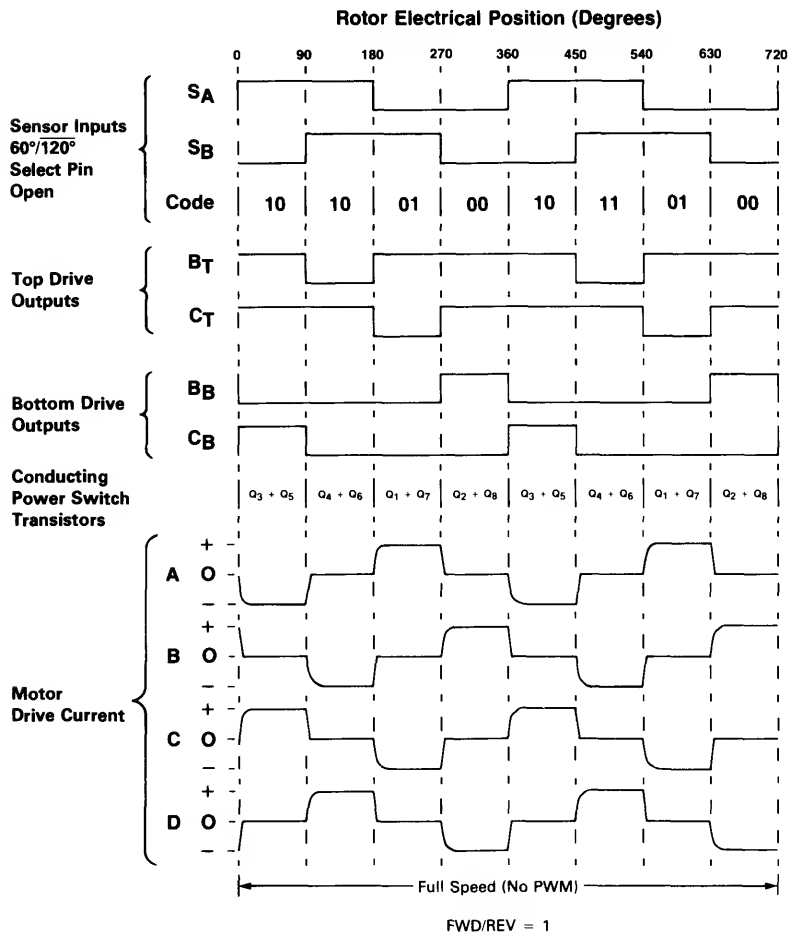
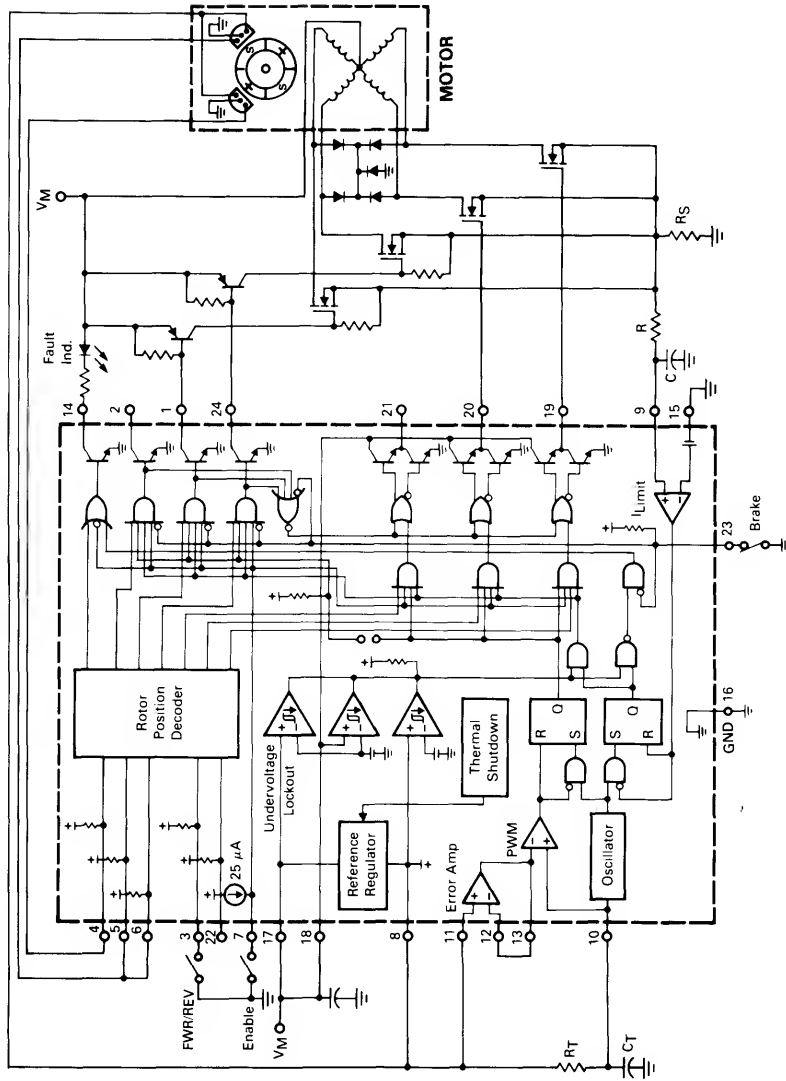


FIGURE 45 — FOUR PHASE, FOUR STEP, HALF WAVE MOTOR CONTROLLER

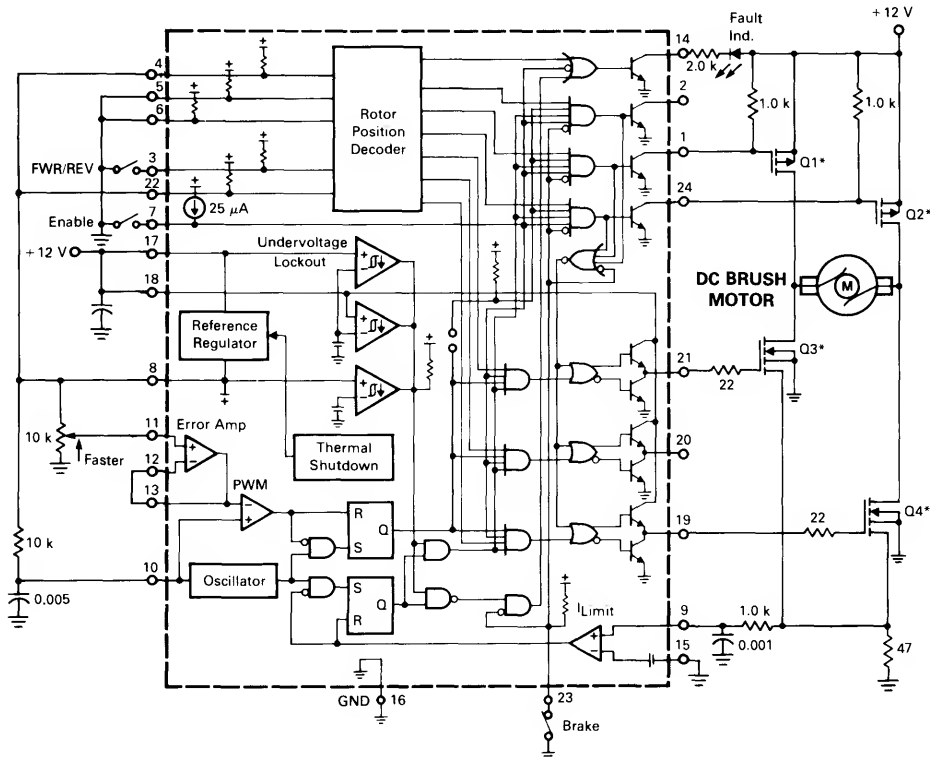


Brush Motor Control

Though the MC33035 was designed to control brushless DC motors, it may also be used to control DC brush-type motors. Figure 46 shows an application of the MC33035 driving a Motorola MPM3002 MOSFET H-bridge affording minimal parts count to operate a one-tenth horsepower brush-type motor. Key to the operation is the input sensor code [100] which produces a top-left (Q1) and a bottom-right (Q4) drive when the controller's forward/reverse pin is at logic [1]; top-right (Q2), bottom-left (Q3) drive is realized when the forward/reverse pin is at logic [0]. This code supports the requirements necessary for H-bridge drive accomplishing both direction and speed control.

The controller functions in a normal manner with a pulse width modulated-frequency of approximately 25 kHz. Motor speed is controlled by adjusting the voltage presented to the noninverting input of the error amplifier establishing the PWM's slice or reference level. Cycle-by-cycle current limiting of 3.0 amperes motor current is accomplished by sensing the voltage (100 mV) across the 47 Ohm resistor to ground of the H-bridge motor current. The over current sense circuit makes it possible to reverse the direction of the motor, using the normal forward/reverse switch, on the fly and not have to completely stop before reversing.

FIGURE 46 — H-BRIDGE BRUSH-TYPE CONTROLLER



*Single Package MPM3002 MOSFET H-Bridge
M = 1/10th horsepower DC brush-type motor

LAYOUT CONSIDERATIONS

Do not attempt to construct any of the brushless motor control circuits on wire-wrap or plug-in prototype boards. High frequency printed circuit layout techniques are imperative to prevent pulse jitter. This is usually caused by excessive noise pick-up imposed on the current sense or error amp inputs. The printed circuit layout should contain a ground plane with low current signal and high drive and output buffer grounds return-

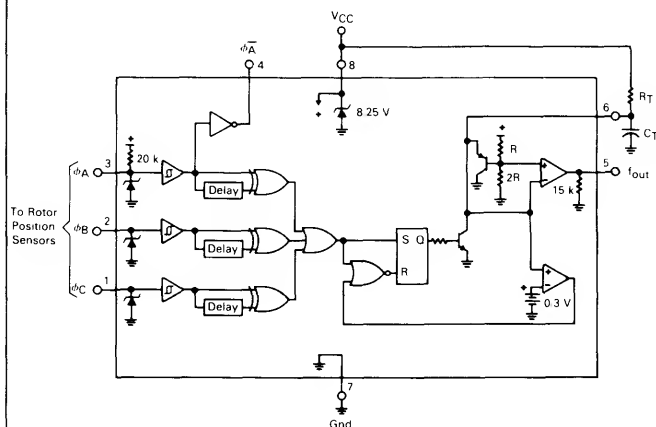
ing on separate paths back to the power supply input filter capacitor V_M . Ceramic bypass capacitors ($0.1 \mu\text{F}$) connected close to the integrated circuit at V_{CC} , V_C , V_{ref} and the error amp noninverting input may be required depending upon circuit layout. This provides a low impedance path for filtering any high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI.

CLOSED-LOOP BRUSHLESS MOTOR ADAPTER

The MC33039 is a high performance closed-loop speed control adapter specifically designed for use in brushless dc motor control systems. Implementation will allow precise speed regulation without the need for a magnetic or optical tachometer. This device contains three input buffers each with hysteresis for noise immunity, three digital edge detectors, a programmable monostable, and an internal shunt regulator. Also included is an inverter output for use in systems that require conversion of sensor phasing. Although this device is primarily intended for use with the MC33034 brushless motor controller, it can be used cost effectively in many other closed-loop speed control applications.

- Digital Detection of Each Input Transition for Improved Low Speed Motor Operation
- TTL Compatible Inputs With Hysteresis
- Operation Down to 5.5 V for Direct Powering from MC33034 Reference
- Internal Shunt Regulator Allows Operation from a Non-Regulated Voltage Source
- Inverter Output for Easy Conversion Between 60°/300° and 120°/240° Sensor Phasing Conventions

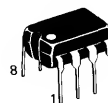
REPRESENTATIVE BLOCK DIAGRAM



MC33039

CLOSED-LOOP BRUSHLESS MOTOR ADAPTER

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**

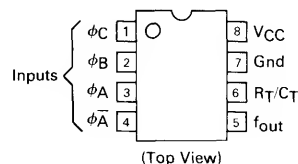


P SUFFIX
PLASTIC PACKAGE
CASE 626



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
MC33039D	- 40°C to + 85°C	SO-8
MC33039P		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
V _{CC} Zener Current	I _{Z(VCC)}	30	mA
Logic Input Current (Pins 1, 2, 3)	I _{IH}	5.0	mA
Output Current (Pin 4, 5), Sink or Source	I _{DRV}	20	mA
Power Dissipation and Thermal Characteristics			
Maximum Power Dissipation (at T _A = +85°C)	P _D	650	mW
Thermal Resistance Junction to Air	R _{θJA}	100	°C/W
Operating Junction Temperature	T _J	+150	°C
Operating Ambient Temperature Range	T _A	-40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 6.25 V, R_T = 10 k, C_T = 22 nF, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
LOGIC INPUTS					
Input Threshold Voltage					V
High State	V _{IH}	2.4	2.1	—	
Low State	V _{IL}	—	1.4	1.0	
Hysteresis	V _H	0.4	0.7	0.9	
Input Current					μA
High State (V _{IH} = 5.0 V)	I _{IH}	-40	-60	-80	
φ _A		—	-0.3	-5.0	
φ _B , φ _C					
Low State (V _{IL} = 0 V)	I _{IL}	-190	-300	-380	
φ _A		—	-0.3	-5.0	
φ _B , φ _C					

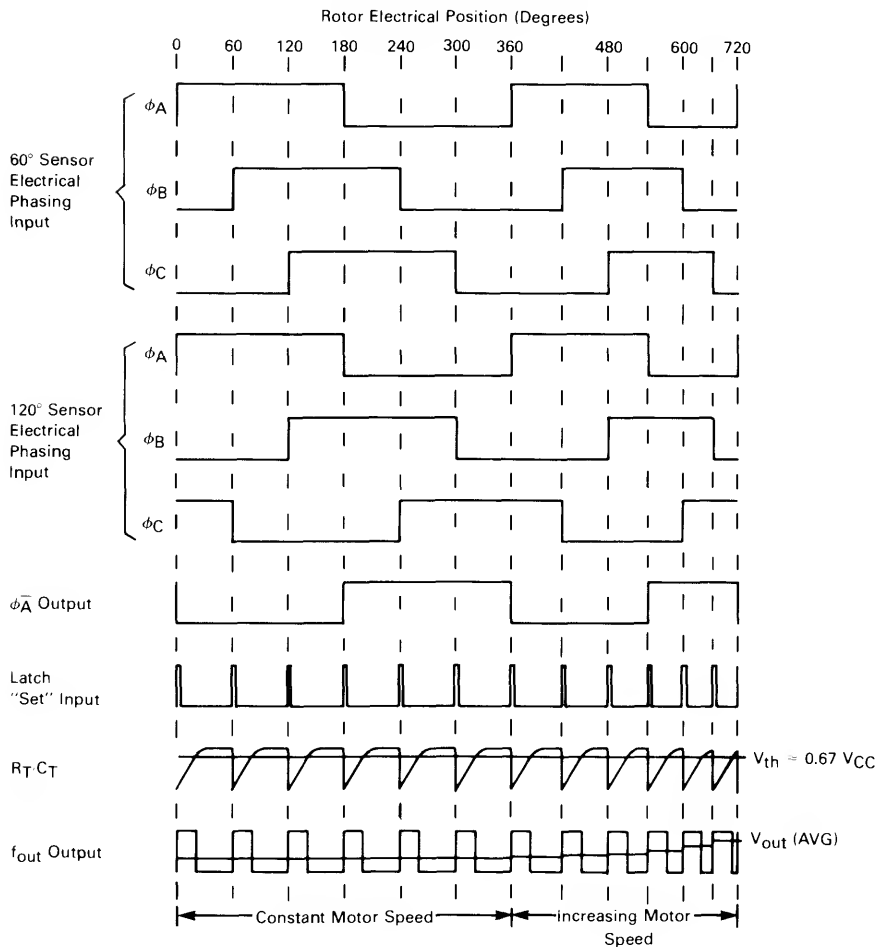
MONOSTABLE AND OUTPUT SECTIONS

Output Voltage					V
High State	V _{OH}	3.60	3.95	4.20	
f _{out} (I _{source} = 5.0 mA)		4.20	4.75	—	
φ _A (I _{source} = 2.0 mA)					
Low State	V _{OL}	—	0.25	0.50	
f _{out} (I _{sink} = 10 mA)		—	0.25	0.50	
φ _A (I _{sink} = 10 mA)					
Capacitor C _T Discharge Current	I _{dischg}	20	35	60	mA
Output Pulse Width (Pin 5)	tp _W	205	225	245	μs

POWER SUPPLY SECTION

Power Supply Operating Voltage Range (T _A = -40°C to +85°C)	V _{CC}	5.5	—	V _Z	V
Power Supply Current	I _{CC}	1.8	3.9	5.0	mA
Zener Voltage (I _Z = 10 mA)	V _Z	7.5	8.25	9.0	V
Zener Dynamic Impedance (ΔI _Z = 10 mA to 20 mA, f ≤ 1.0 kHz)	Z _{ka}	—	2.0	5.0	Ω

FIGURE 1 — TYPICAL THREE PHASE, SIX STEP MOTOR APPLICATION



OPERATING DESCRIPTION

The MC33039 provides an economical method of implementing closed-loop speed control of brushless dc motors by eliminating the need for a magnetic or optical tachometer. Shown in the timing diagram of Figure 1, the three inputs (Pins 1, 2, 3) monitor the brushless motor rotor position sensors. Each sensor signal transition is digitally detected, OR'ed at the Latch 'Set' Input, and causes C_T to discharge. A corresponding output pulse is generated at f_{out} (Pin 5) of a defined amplitude, and programmable width determined by the values selected for R_T and C_T (Pin 6). The average voltage of the output pulse train increases with motor speed. When fed through a low pass filter or integrator, a dc voltage proportional to speed is generated. Figure 2 shows the proper connections for a typical closed loop

application using the MC33034 brushless motor controller. Constant speed operation down to 100 RPM is possible with economical three phase four pole motors.

The ϕ_A inverter output (Pin 4) is used in systems where the controller and motor sensor phasing conventions are not compatible. A method of converting from either convention to the other is shown in Figure 3. For a more detailed explanation of this subject, refer to the text above Figure 39 on the MC33034 data sheet.

The output pulse amplitude V_{OH} is constant with temperature and controlled by the supply voltage on V_{CC} (Pin 8). Operation down to 5.5 V is guaranteed over temperature. For systems without a regulated power supply, an internal 8.25 V shunt regulator is provided.

MC33039

FIGURE 2 — TYPICAL CLOSED-LOOP SPEED CONTROL APPLICATION

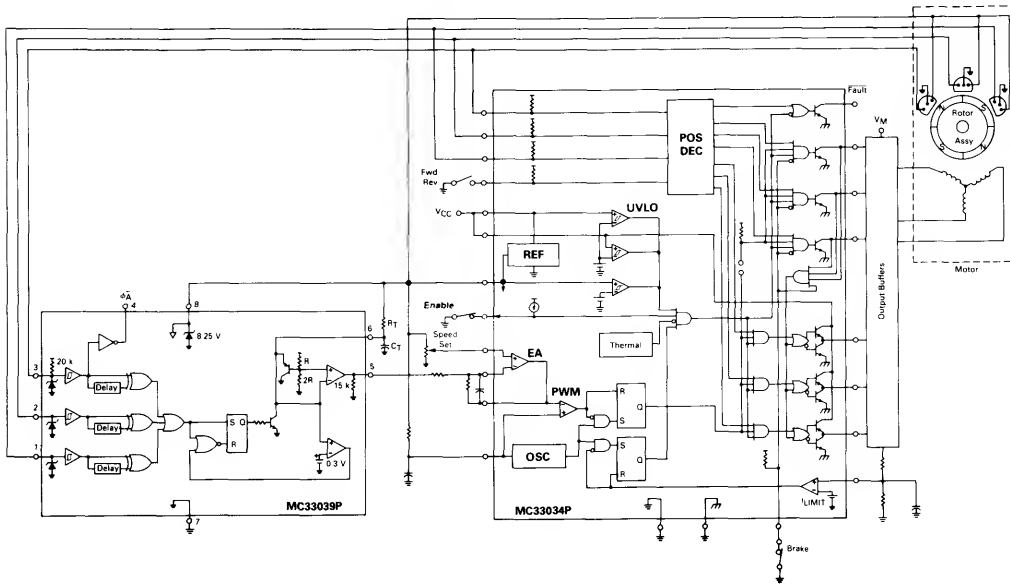


FIGURE 3 — CONVERSION BETWEEN SENSOR PHASING CONVENTIONS

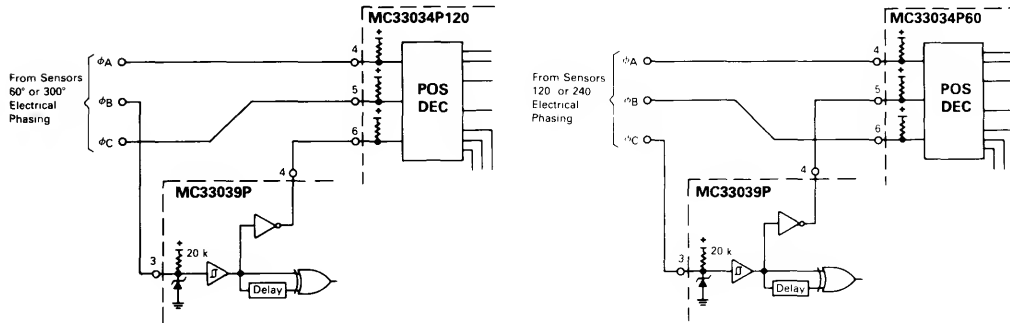


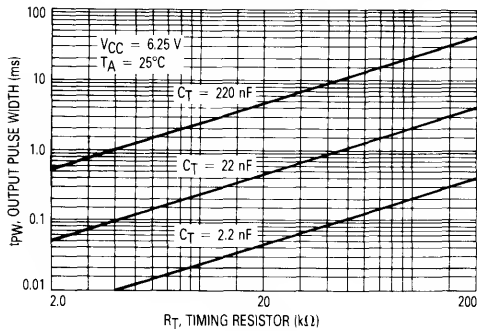
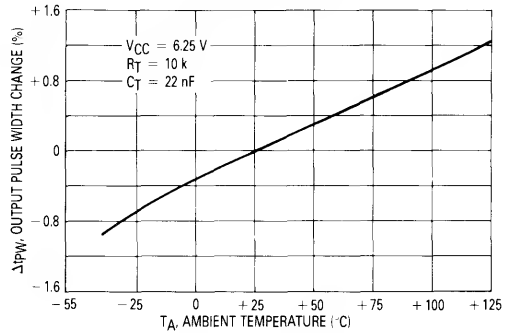
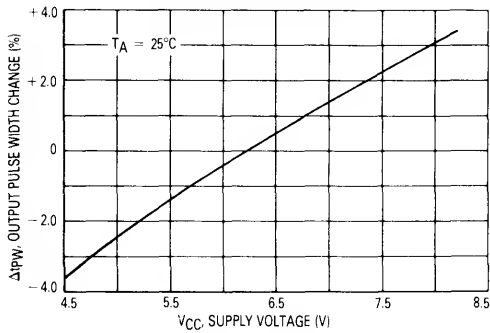
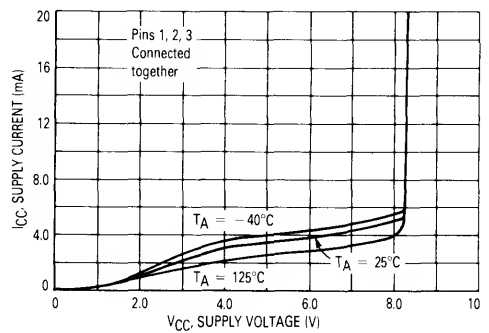
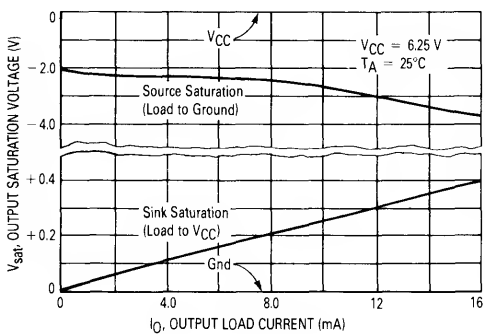
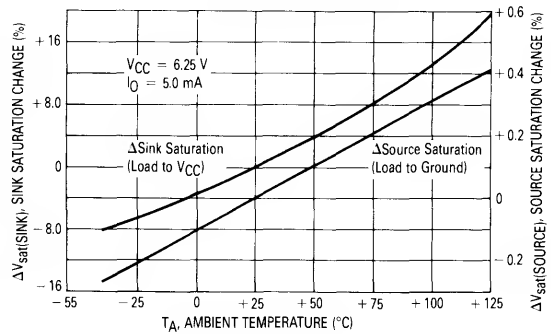
FIGURE 4 — f_{out} PULSE WIDTH versus TIMING RESISTORFIGURE 5 — f_{out} PULSE WIDTH CHANGE versus TEMPERATUREFIGURE 6 — f_{out} PULSE WIDTH CHANGE versus SUPPLY VOLTAGE

FIGURE 7 — SUPPLY CURRENT versus SUPPLY VOLTAGE

FIGURE 8 — f_{out} SATURATION versus LOAD CURRENTFIGURE 9 — f_{out} SATURATION CHANGE versus TEMPERATURE

SAA1042
SAA1042A

STEPPER MOTOR DRIVER

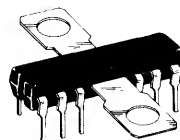
The SAA1042 drives a two-phase stepper motor in the bipolar mode. The device contains: three input stages, a logic section and two output stages.

- Drive Stages Designed for Motors: 6.0 V and 12 V: SAA1042
24 V: SAA1042A
- 500 mA/Coil Drive Capability
- Built-In Clamp Diodes for Overvoltage Suppression
- Wide Logic Supply Voltage Range
- Accepts Commands for CW/CCW and Half/Full Step Operation
- Inputs Compatible with Popular Logic Families: MOS, TTL, DTL
- Set Input Defined Output State
- Drive Stage Bias Adaptable to Motor Power Dissipation for Optimum Efficiency

STEPPER MOTOR DRIVER

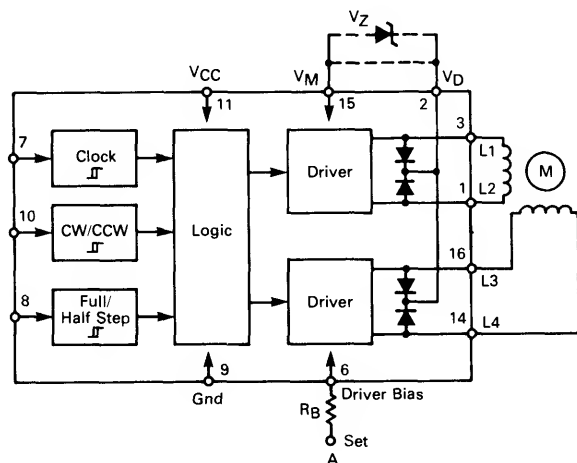
SILICON MONOLITHIC
INTEGRATED CIRCUIT

4

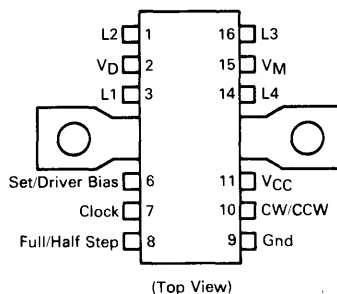


PLASTIC PACKAGE
CASE 721

FIGURE 1 — SAA1042 BLOCK DIAGRAM



PIN ASSIGNMENT



Note: Case heatsink is electrically connected to ground (Pin 9) through the die substrate.

SAA1042, SAA1042A

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	SAA1042	SAA1042A	Unit
Clamping Voltage (Pins 1, 3, 14 & 16)	V _{clamp}	20	30	V
Over Voltage (V _{OV} = V _{clamp} - V _M)	V _{OV}	6.0		V
Supply Voltage	V _{CC}	20	30	V
Switching or Motor Current/Coil	I _M	500		mA
Input Voltage (Pins 7, 8 & 10)	V _{in} clock V _{in} Full/Half V _{in} CW/CCW	V _{CC}		V
Power Dissipation (Note 1) Derate above T _A = 25°C	P _D	2.0		W
Thermal Resistance, Junction to Air	1/θ _{JA}	20		mW/°C
Thermal Resistance, Junction to Case	θ _{JA}	50		°C/W
	θ _{JC}	8.0		°C/W
Operating Junction Temperature Range	T _J	-30 to +125		°C
Storage Temperature Range	T _{stg}	-65 to +150		°C

NOTE: 1. The power dissipation, P_D, of the circuit is given by the supply voltage, V_M and V_{CC}, and the motor current, I_M, and can be determined from Figures 3 and 5. P_D = P_{drive} + P_{logic}.

ELECTRICAL CHARACTERISTICS (T_A = +25°C)

Characteristic	Pin	Symbol	V _{CC}	Min	Typ	Max	Unit
Supply Current	11	I _{CC}	5.0 V 20 V	— —	— —	3.5 8.5	mA
Motor Supply Current (I Pin 6 = -400 μA, Pins 1, 3, 14, 16 Open) V _M = 6.0 V V _M = 12 V V _M = 24 V	15	I _M	5.0 V 5.0 V 5.0 V	— — —	25 30 40	— — —	mA
Input Voltage — High State	7, 8, 10	V _{IH}	5.0 V 10 V 15 V 20 V	2.0 7.0 10 14	— — — —	— — — —	V
Input Voltage — Low State	7, 8, 10	V _{IL}	5.0 V 10 V 15 V 20 V	— — — —	— — — —	0.8 1.5 2.5 3.5	V
Input Reverse Current — High State (V _{in} = V _{CC})	7, 8, 10	I _{IR}	5.0 V 10 V 15 V 20 V	— — — —	— — — —	2.0 2.0 3.0 5.0	μA
Input Forward Current — Low State (V _{in} = Gnd)	7, 8, 10	I _{IF}	5.0 V 10 V 15 V 20 V	-10 -25 -40 -55	— — — —	— — — —	μA
Output Voltage — High State (V _M = 12 V) I _{out} = -500 mA I _{out} = -50 mA	1, 3, 14, 16	V _{OH}	5.0 to 20 V	— —	V _M - 2.0 V _M - 1.2	— —	V
Output Voltage — Low State I _{out} = 500 mA I _{out} = 50 mA	1, 3, 14, 16	V _{OL}	5.0 to 20 V	— —	0.7 0.2	— —	V
Output Leakage Current (V _M = V _D = V _{clamp} max.) Pin 6: Open	1, 3, 14, 16	I _{DR}	5.0 to 20 V	-100	—	—	μA
Clamp Diode Forward Voltage (Drop at I _M = 500 mA)	2	V _F	—	—	2.5	3.5	V
Clock Frequency	7	f _c	5.0 to 20 V	0	—	50	kHz
Clock Pulse Width	7	t _w	5.0 to 20 V	10	—	—	μs
Set Pulse Width	6	t _s	—	10	—	—	μs
Set Control Voltage — High State Low State	6	—	—	V _M —	— —	— 0.5	V

INPUT/OUTPUT FUNCTIONS

Clock — (Pin 7) This input is active on the positive edge of the clock pulse and accepts Logic '1' input levels dependant on the supply voltage and includes hysteresis for noise immunity.

CW/CCW — (Pin 10) This input determines the motor's rotational direction. When the input is held low, (OV, see the electrical characteristics) the motor's direction is nominally clockwise (CW). When the input is in the high state, Logic '1,' the motor direction will be nominally counter clockwise (CCW), depending on the motor connections.

Full/Half Step — (Pin 8) This input determines the angular rotation of the motor for each clock pulse. In the low state the motor will make a full step for each applied clock pulse, while in the high state, the motor will make half a step.

V_D — (Pin 2) This pin is used to protect the outputs (1, 3, 14, 16) where large positive spikes occur due to switching the motor coils. The maximum allowable voltage on these pins is the clamp voltage (V_{clamp}). Motor performance is improved if a zener diode is connected between Pin 2 and Pin 15 as shown in Figure 1.

The following conditions have to be considered when selecting the zener diode:

$$V_{\text{clamp}} = V_M + 6.0 \text{ V}$$

$$V_Z = V_{\text{clamp}} - V_M - V_F^*$$

where: V_F = clamp diodes forward voltage drop (see Figure 4)

$$V_{\text{clamp}}: \\ \leq 20 \text{ V for SAA1042} \\ \leq 30 \text{ V for SAA1042A}$$

Pins 2 and 15 can be linked, in this case V_Z = 0 V.

Set/Bias Input — (Pin 6) This input has two functions:

The resistor R_B adapts the drivers to the motor current.

A pulse via the resistor R_B sets the outputs (1, 3, 14, 16) to a defined state.

The resistor R_B can be determined from the graph of Figure 2 according to the motor current and voltage. Smaller values of R_B will increase the power dissipation of the circuit and larger values of R_B may increase the saturation voltage of the driver transistors.

When the "set" function is not used, terminal A of the resistor R_B must be grounded. When the set function is used, terminal A has to be connected to an open-collector (buffer) circuit. Figure 7 shows this configuration. The buffer circuit (off-state) has to sustain the motor voltage V_M. When a pulse is applied via the buffer and the bias resistor R_B:

During the pulse duration, the motor driver transis-

tors are turned off.

After elapsing the pulse, the outputs will have defined states.

Figure 6 shows the timing diagram.

Figure 7 illustrates a typical application in which the SAA1042 drives a 12 V stepper motor with a current consumption of 200 mA/coil.

A bias resistor (R_B) of 56 kΩ is chosen according to Figure 2.

The maximum voltage permitted at the output pin is V_M + 6.0 V (see the Maximum Ratings), in this application V_M = 12 V, therefore the maximum voltage is 18 V. The outputs are protected by the internal diodes and an external zener connected between Pins 2 and 15.

From Figure 4, it can be seen that the voltage drop across the internal diodes is about 1.7 V at 200 mA. This results in a zener voltage between Pins 2 and 15 of:

$$V_Z = 6.0 \text{ V} - 1.7 \text{ V} = 4.3 \text{ V.}$$

To allow for production tolerances and a safety margin, a 3.9 V zener has been chosen for this example.

The clock is derived from the line frequency which is phase locked by the MC14046B and the MC14024.

The voltage on the clock input, is normally low (Logic '0'). The motor steps on the positive going transition of the clock pulse.

A Logic '0' applied to the Full/Half input, Pin 8, operates the motor in the Full Step mode. A Logic '1' at this input will result in the Half Step mode. The logic level state on the CW/CCW input, Pin 10, and the connection of the motor coils to the outputs determines the rotational direction of the motor.

These two inputs should be biased to a Logic '0' or '1' and not left floating. In the event of non-use, they should be tied to ground or the logic supply line, V_{CC}.

The output drivers can be set to a fixed operating point by use of the Set input and a bias resistor R_B. A positive pulse to this input turns the drivers off and sets the logic state of the outputs.

After the negative going transition of the Set pulse, and until the first positive going transition of the clock, the outputs will be:

L1 = L3 = high and L2 = L4 = low.
(See Figure 6, the timing diagram).

The Set input can be driven by a MC14007B or a transistor whose collector resistor is R_B. If the input is not used, the 'bottom' of R_B must be grounded.

The total power dissipation of the circuit can be determined from Figures 3 and 5.

$$P_D = 0.9 \text{ W} + 0.08 \text{ W} = 0.98 \text{ W.}$$

This results in a junction to ambient temperature, without a heatsink of:

T_J - T_A = 50°C/W × 0.98 W = 49°C.
or a maximum ambient temperature of 76°C. For operation at elevated temperatures a heatsink is required.

FIGURE 2 — BIAS RESISTOR R_B versus MOTOR CURRENT

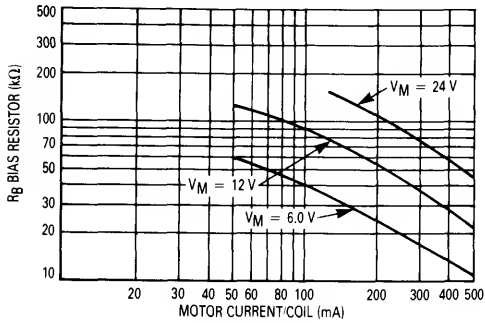


FIGURE 3 — DRIVE STAGE POWER DISSIPATION

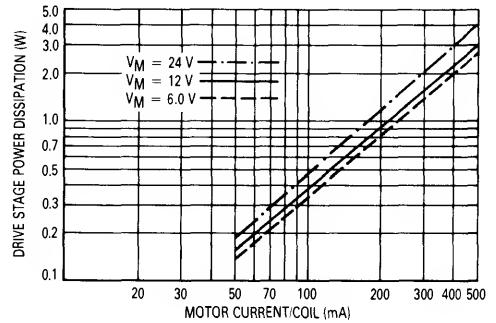


FIGURE 4 — CLAMP DIODE FORWARD CURRENT versus FORWARD VOLTAGE

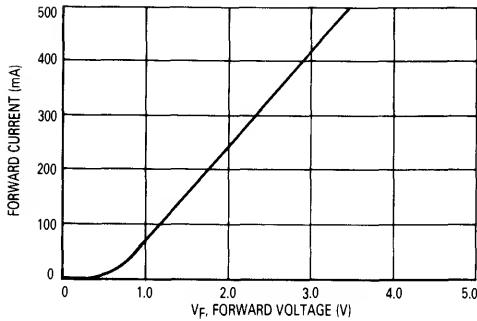


FIGURE 5 — POWER DISSIPATION versus LOGIC SUPPLY VOLTAGE

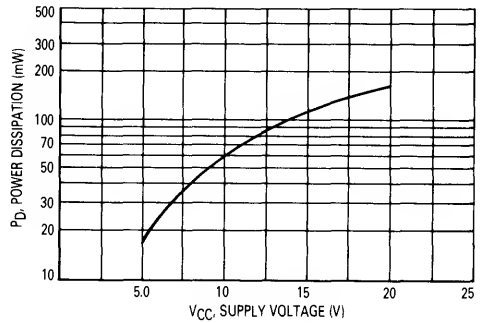
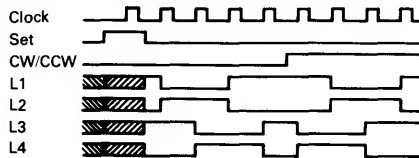


FIGURE 6 — TIMING DIAGRAM

Full Step Motor Drive Mode. Full/Half Step Input = 0



Don't Care

High Output Impedance

Half Step Motor Drive Mode. Full/Half Step Input = 1

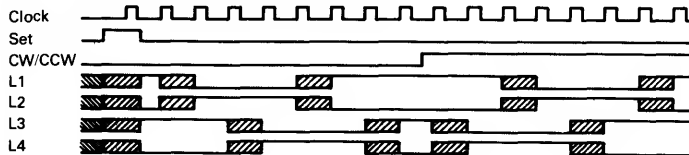
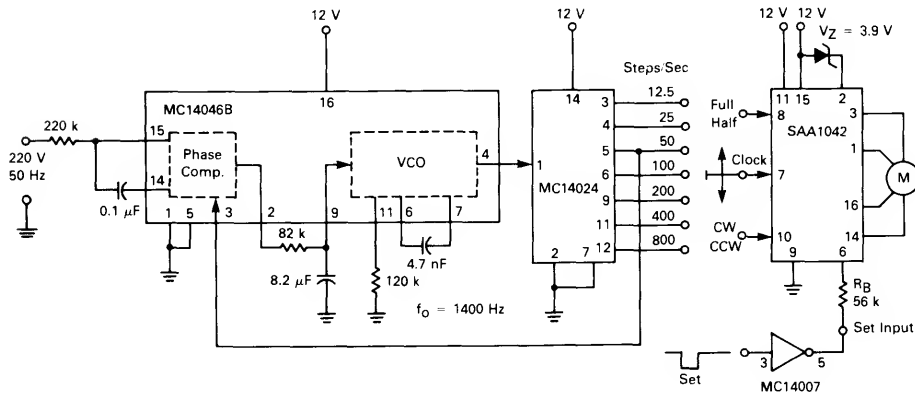


FIGURE 7 — TYPICAL APPLICATION
SELECTABLE STEP RATES WITH THE TIME BASE DERIVED FROM THE LINE FREQUENCY



TDA1085A

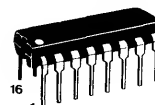
UNIVERSAL MOTOR SPEED CONTROLLER

The TDA1085A has all the necessary functions for the speed control of universal (ac/dc) motors in an open or closed loop configuration. Additionally it has the facility for defining the initial speed/time characteristic. The circuit provides a phase angle varied trigger pulse to the motor control triac.

- Guaranteed Full Wave Triac Drive
- Soft Start from Powerup
- On-Chip Frequency/Voltage Convertor and Ramp Generator
- Current Limiting Incorporated
- Direct Drive from ac Line

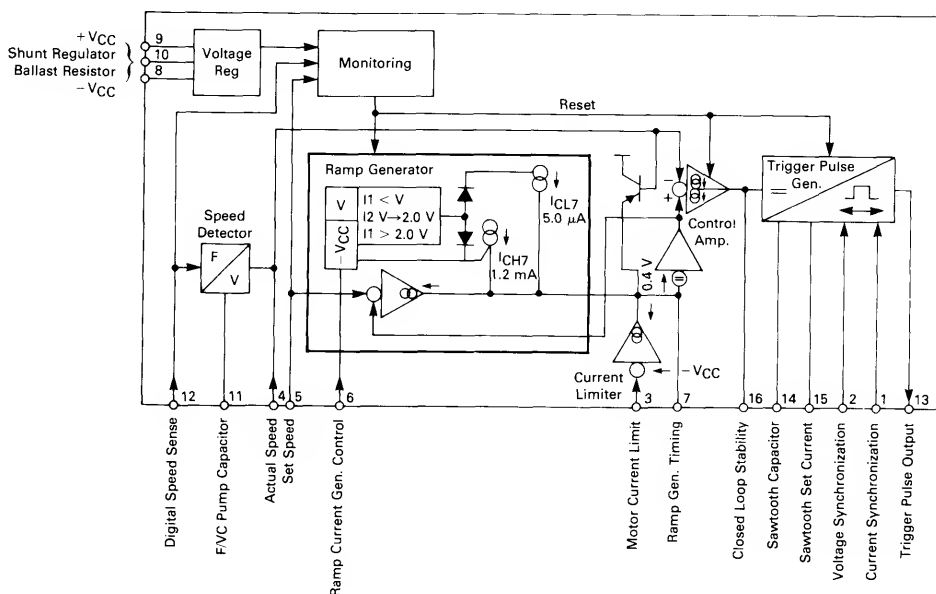
UNIVERSAL MOTOR SPEED CONTROLLER

SILICON MONOLITHIC INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 648

FIGURE 1 — BLOCK DIAGRAM AND PIN ASSIGNMENT



TDA1085A

4

MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Power Supply Voltage	$V_{Pin\ 9-8}$	17	V
Power Supply Current (Pin 10 Open)	$I_{Pin\ 9}$	15	mA
Peak Power Supply Regulation Current	$I_{Pin\ 9} + I_{Pin\ 10}$	35	mA
Peak ac Synchronization Input Current	$I_{Pin\ 1}$ $I_{Pin\ 2}$	± 1.0	mA
Peak Output Triggering Current (Pulse Width 300 μ s; Duty Cycle $\leq 3\%$)	$I_{Pin\ 13}$	200	mA
Current Drain per Listed Pin	I_{15} I_3 I_{12}	1.0 - 5.0 - 3.0, + 0.1	mA
Power Dissipation ($T_A = 25^\circ\text{C}$) Derate above 25°C	P_D $1/R_{\theta JA}$	625 6.8	mW mW/ $^\circ\text{C}$
Operating Temperature Range	T_A	0 to + 70	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	- 55 to + 125	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_A = + 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
VOLTAGE REGULATOR					
Regulated Voltage* ($I_g + I_{10} = 10\text{ mA}$)	V_{CC}	—	15.5	—	V
Monitoring Enable Level*	V_{ME}	—	15.1	—	V
Monitoring Disable Level*	V_{MD}	—	14.5	—	V
Internal Current Consumption (Note 1)	$I_{Pin\ 9}$	—	4.2	—	mA
RAMP GENERATOR					
Reference Input Voltage Range (Note 2)	$V_{Pin\ 5-8}$	0.08	—	13.5	V
Reference Input Bias Current	$I_{Pin\ 5}$	—	—	- 20	μA
Distribute Low Level Voltage Range	$V_{Pin\ 6}$	0	—	2.0	V
Distribute — Low Level (Figure 2)	V_{DL}	—	$V_{Pin\ 6}$	—	V
Distribute — Upper Level* (Figure 2) ($V_{Pin\ 6} = 950\text{ mV}$)	V_{DU}	$1.9 V_6$	$2.0 V_6$	$2.1 V_6$	V
Low-High Acceleration Range (Figure 2)	ΔV_{DA}	—	400	—	mV
High Acceleration Charging Current	I_{CH7}	—	1.2	—	mA
Low Charging Current (Note 3)	I_{CL7}	—	5.0	—	μA

NOTES:

1. Pins 1, 2, 11, 12, 14 and 15 not connected; Pins 4, 5, 6 and 7 grounded to Pin 8: $V_{CC} = 15.5\text{ V}$.
2. When $V_{Pin\ 5}$ is $\approx 80\text{ mV}$, the internal monitoring circuit interprets it as a true zero, thus minimizing the effects of control amplifier offsets.
3. This value should be accounted for when externally setting the distribute acceleration charging current.

* These figures apply for the application shown in Figure 4.

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Min	Typ	Max	Unit
CURRENT LIMITER					
Stage Current Gain	I_{DL7} ΔI_3	—	170	—	—
Output Discharge Current Swing	I_{DL7}	—	35	—	mA
CONTROL AMPLIFIER					
Actual Speed Voltage Range	$V_{Pin\ 4-8}$	0	—	13.5	V
Actual Speed Input Bias Current	$I_{Pin\ 4}$	—	—	–350	nA
Total Input Offset Voltage (Note 4)	V_{off}	–60	—	20	mV
Transconductance $\left(\frac{\Delta I_{Pin\ 16}}{V_{Pin\ 4} - V_{Pin\ 7}} \right)$	g_m	—	300	—	$\mu A/V$
Output Current Swing	$I_{Pin\ 16}$	—	± 100	—	μA
FREQUENCY/VOLTAGE CONVERTER					
Input Signal Low Voltage (Note 5)	V_{L12}	–0.1	—	—	V
Input Signal High Voltage	V_{H12}	0.1	—	5.0	V
Polarization Current	$I_{Pin\ 12}$	—	–25	—	μA
Conversion Rate* (Note 6)	K_C	—	15	—	mV/Hz
Linearity* (Figure 3)	K_L	—	± 4.0	—	%
TRIGGER PULSE GENERATOR					
Voltage Synchronization Levels	$I_{Pin\ 2}$	—	± 50	—	μA
Current Synchronization Levels	$I_{Pin\ 1}$	—	± 50	—	μA
Input Voltage Swing (for full angle swing)	V	—	11.7	—	V
Trigger Pulse Width (Note 7)	t_p	—	55	—	μs
Trigger Pulse Repetition Period	t	—	215	—	μs
Trigger Pulse High Level ($I_{Pin\ 13} = 150\text{ mA}$)	$V_{Pin\ 13}$	$V_{CC} - 4$	—	—	V
Output Leakage Current ($V_{Pin\ 13} = 0\text{ V}$)	$I_{oPin\ 13}$	—	—	30	μA

4. V_{off} is defined as being the voltage difference between Pin 5 and 4 with no current flow on Pin 16.

5. The negative swing is clamped to –0.3 V.

6. $V_{Pin\ 4} = k \cdot C_{Pin\ 11} \cdot (V_{CC} - V_a) \cdot R_{Pin\ 4} \cdot \left(1 + \frac{180 \times 10^3}{R_{Pin\ 11}} \right) - 1 \cdot \text{freq in.}$

Where: $9 < k < 13$ & $V_a = 1.3\text{ V}$.

7. The timing given is when $C_{Pin\ 14} = 47\text{ nF}$.

* These figures apply for the application shown in Figure 4.

INPUT/OUTPUT FUNCTIONS

VOLTAGE REGULATOR — (Pins 8, 9, 10). This is a parallel type voltage regulator able to sink a large amount of current while offering good regulation characteristics.

A resistor between Pins 9 and 10 reduces the internal power dissipation. Under minimal current sink conditions (min. current from the unregulated supply, min. consumption by the circuitry), at least 1.0 mA should flow through this resistor. Under max. sink conditions (max. current from the unregulated supply, min. consumption by the circuitry), the maximum resistor value is chosen so that the voltage at Pin 10 falls towards 3.0 V, but not lower. The above, fixed dynamic range of the regulator must not be exceeded within one line cycle.

A power supply failure causes shutdown.

For operation from an externally regulated voltage, Pin 10 is not connected.

SPEED SENSING — (Pins 4, 11, 12). Speed sensing can be achieved either digitally (tachogenerator frequency) or analogously (tachogenerator amplitude).

For digital sensing, a bipolar signal with respect to ground is applied to Pin 12. During positive excursions

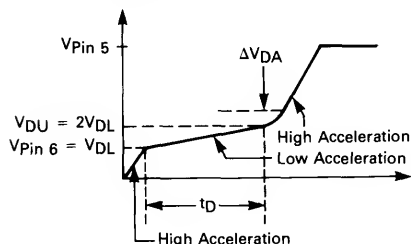
$C_{Pin\ 11}$ is charged. An internal mirror delivers ten times the charge on $C_{Pin\ 11}$ via Pin 4. However, due to internal circuitry, the charge on Pin 4 can vary in the region of 9 to 13 times the charge on $C_{Pin\ 11}$. For that reason it is necessary to calibrate the Frequency/Voltage Converter (F/V/C) with a variable resistor on Pin 4. Thus the relationship between speed and $V_{Pin\ 4}$ is defined by $R_{Pin\ 4}$ and $C_{Pin\ 11}$.

To maintain linearity in the high speed ranges it is important that $C_{Pin\ 11}$ is fully charged across an equivalent resistor of about 180 k Ω . It should be borne in mind that the impedance on Pin 11 should be kept as low as possible as $C_{Pin\ 11}$ has a large influence on the temperature coefficient of the FV/C. The time constant on Pin 4 should also be kept as low as possible.

Pin 12 is also an impedance monitoring input; at high impedances $V_{Pin\ 12}$ increases. Should $V_{Pin\ 12}$ exceed 5.0 V the triac trigger pulses are inhibited and the circuit resets.

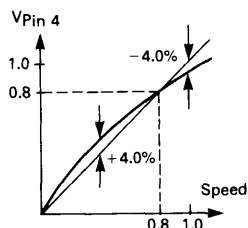
A 470 k Ω resistor from Pin 11 to $+V_{CC}$ significantly reduces the leakage current and reduces the device temperature coefficient to almost zero.

FIGURE 2 — RAMP GENERATOR
TRANSFER CHARACTERISTIC



The shape of the curve is determined by $CR_{Pin\ 7}$; where $C_{Pin\ 7}$ defines the high acceleration slope and $R_{Pin\ 7}$ defines that of the low acceleration.

FIGURE 3 — FREQUENCY/VOLTAGE CONVERTER
OUTPUT CHARACTERISTIC



INPUT/OUTPUT FUNCTIONS (continued)

For analog sensing input 12 should be grounded and a positive signal, with respect to ground, Pin 8, applied to Pin 4.

RAMP GENERATOR — (Pins 5, 6, 7) (refer to Figure 2). A preset voltage applied to Pin 5 will initiate the generation of a ramp whose final value is determined by the voltage applied to Pin 5. The voltage applied to Pin 6 will determine how much of the full ramp, shown in Figure 2, is used. The charging current passing through Pin 7 to the ramp generator timing capacitor determines the ramp slope.

When Pin 6 is held at $-V_{CC}$ a charging current of 1.2 mA is delivered to Pin 7, regardless of the voltage of Pin 5. This represents the high acceleration period shown in Figure 2.

If the preset voltage applied to Pin 5 is equal to or less than the voltage on Pin 6 the charging current will be 1.2 mA, or high acceleration.

If the preset voltage applied to Pin 5 is between $V_{Pin 6}$ and $2 V_{Pin 6}$ the charging current is 1.2 mA (high acceleration) until the voltage at the reference input of the control amplifier equals $V_{Pin 6}$. At this point the charging current will switch to 5.0 μA ; i.e. low acceleration.

If the preset voltage applied to Pin 5 is greater than $2 V_{Pin 6}$ the charging current will be 1.2 mA (high acceleration) until the control amplifier's reference input reaches $V_{Pin 6}$ when it will switch to 5.0 μA (low acceleration) until $2 V_{Pin 6}$ is reached. At this point the charging current will revert to 1.2 mA, high acceleration, until the final value of $V_{Pin 5}$ is reached.

Should the preset voltage at Pin 5 fall below 80 mV, the triac trigger pulses are inhibited and the circuit resets. This fact should be borne in mind when switching from one preset value to another.

As long as the voltages applied at Pins 5 and 6 are derived from the internal voltage regulator, they and the voltage on Pin 4 are ratioed and thus independent of the voltage regulator spread and temperature coefficient.

CURRENT LIMITER — (Pin 3). Safe operation of the motor and triac under all conditions is ensured by reducing the motor speed if a preset current limit is exceeded.

This is achieved as follows: The motor current will set up an alternating current, consisting of positive and negative peaks through the shunt resistor (0.05 Ω in Figure 4).

The negative peaks of this current are fed through a resistor to Pin 3 where they are compared with a preset current defined by a resistor between Pin 3 and $+V_{CC}$. An excessive shunt current will try to pull Pin 3 below $-V_{CC}$, but the current limiter becomes active at this point and reduces the charge on $C_{Pin 7}$, consequently reducing the motor speed.

Thus the value of the shunt and the ratio of the two resistors to Pin 3 fix the level at which the limiter becomes active, while the parallel equivalent of the two resistors determines the magnitude of the discharge current and thus how rapidly the circuit responds to an overcurrent condition.

CONTROL AMPLIFIER — (Pin 16). Connected to this pin is a network which compensates electrically for the mechanical characteristics of the motor and its load to give the circuit optimum closed loop stability and transient response.

The component values are best determined empirically by connecting R and C substitution boxes and looking for the best results.

TRIGGER PULSE GENERATOR — (Pins 1, 2, 13, 14, 15). This circuit performs four functions:

1. The conversion of the control amplifier's dc output level to a proportional firing angle positioned to within half a line cycle.
2. The calibration of the pulse width.
3. The repetition of the firing pulse if the triac fails to latch, or if the current is interrupted by brush bounce.
4. To delay the firing pulse until the current crosses zero at wide firing angles.

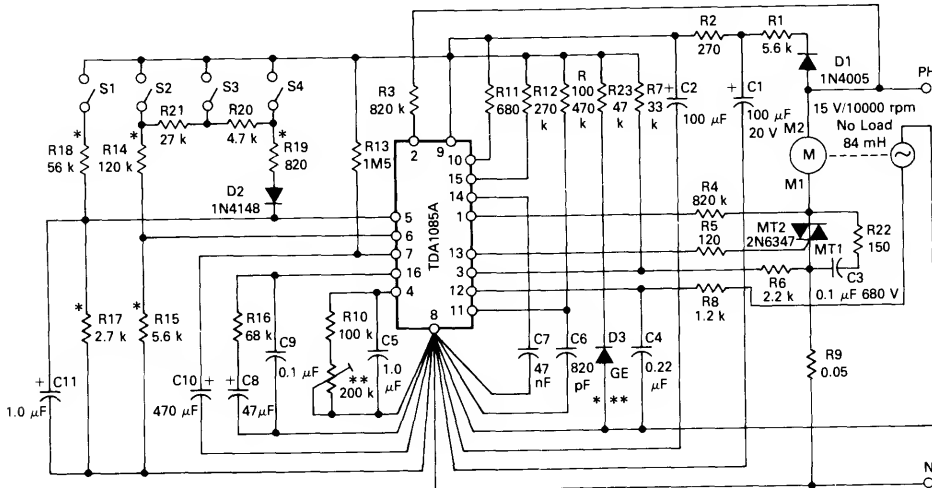
$R_{Pin 15}$ and $C_{Pin 14}$ fix the sawtooth while $C_{Pin 14}$ also determines the pulse width.

Pin 13 is the trigger pulse output. A current limiting resistor is essential on this pin. This configuration will drive two thyristors controlling a bridge if the supply for the speed controller is isolated.

TDA1085A

TYPICAL APPLICATIONS

FIGURE 4 — CLOSED LOOP, FULLY PROGRAMMED, MULTI-SPEED SYSTEM WITH CURRENT LIMITING



- * Chosen to suit the speeds required
- ** Adjust for the highest speed
- *** Required only with 'A' suffix device

Speed Control Resistor Network Equations

R17	=	given
R18	=	$R17 \left(\frac{15.5 \text{ V}}{V_W} - 1 \right)$
R19	=	$R17 \left(\frac{14.8 \text{ V}}{V_{\text{spin 2}}} - 1 \right)$
R20	=	$R17 \left(\frac{14.8 \text{ V}}{V_{\text{spin 1}}} - 1 \right) - R19$
R21	=	$R17 \left(\frac{14.8 \text{ V}}{K \cdot V_W} - 1 \right) - R19 - R20$
R15	=	$R21 \left(\frac{K \cdot V_W}{15.5 \text{ V} (2 \cdot K)} \right)$
R14	=	$R15 \left(\frac{15.5 \text{ V}}{V_W} - 1 \right)$

The ratio distribute speed to wash speed can be chosen as:

$$\frac{V_{\text{DIST}}}{V_{\text{WASH}}} \leq 2 \approx K$$

	S1	S2	S3	S4	V _{Pin 5}	V _{Pin 6}
Wash	sc	oc	oc	oc	V _W	0
Distribute	oc	sc	oc	oc	KV _W	V _W
Spin 1	oc	oc	sc	oc	>KV _W	$\frac{K}{2} V_W$
Spin 2	oc	oc	oc	sc	>>KV _W	$\frac{K}{2} V_W$

sc = switch closed
oc = switch open

Note:

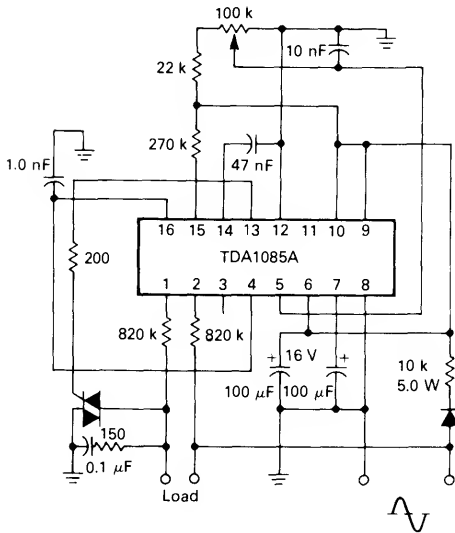
When changing from one speed to another V_{Pin 5} must not be allowed to fall below 80 mV — otherwise the circuit will reset and restart from zero.

The component values given in Figure 4 correspond to:

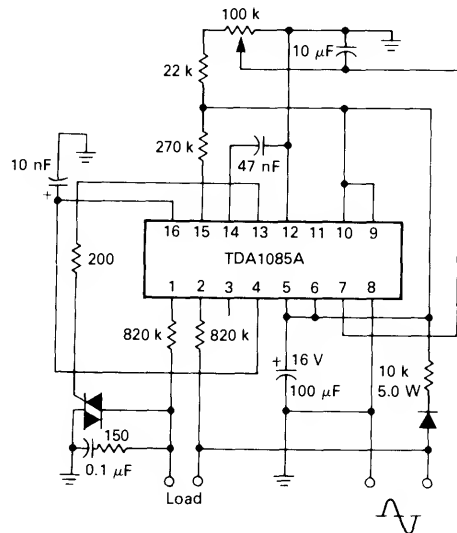
V _W	=	0.7 V
V _D	=	1.13 V
V _{spin 1}	=	5.0 V
V _{spin 2}	=	11 V
K	=	1.6

TDA1085A

**FIGURE 5 — OPEN LOOP, SOFT START — WITH
PROGRAMMED TIME TO MAX. SPEED**
($t = C_{pin} 7.65 \times 10^5$)



**FIGURE 6 — OPEN LOOP,
SOFT-START/SOFT-STOP,
LIGHTING/INDUCTIVE LOAD CONTROLLER**



TDA1085C

UNIVERSAL MOTOR SPEED CONTROLLER

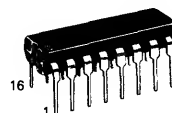
The TDA1085C is a phase angle triac controller having all the necessary functions for universal motor speed control in washing machines. It operates in closed loop configuration and provides two ramps possibilities.

- On-Chip Frequency to Voltage Converter
- On-Chip Ramps Generator
- Soft Start
- Load Current Limitation
- Tachogenerator Circuit Sensing
- Direct Supply from AC Line
- Security Functions Performed by Monitor

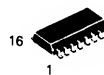
UNIVERSAL MOTOR SPEED CONTROLLER

LINEAR INTEGRATED CIRCUIT

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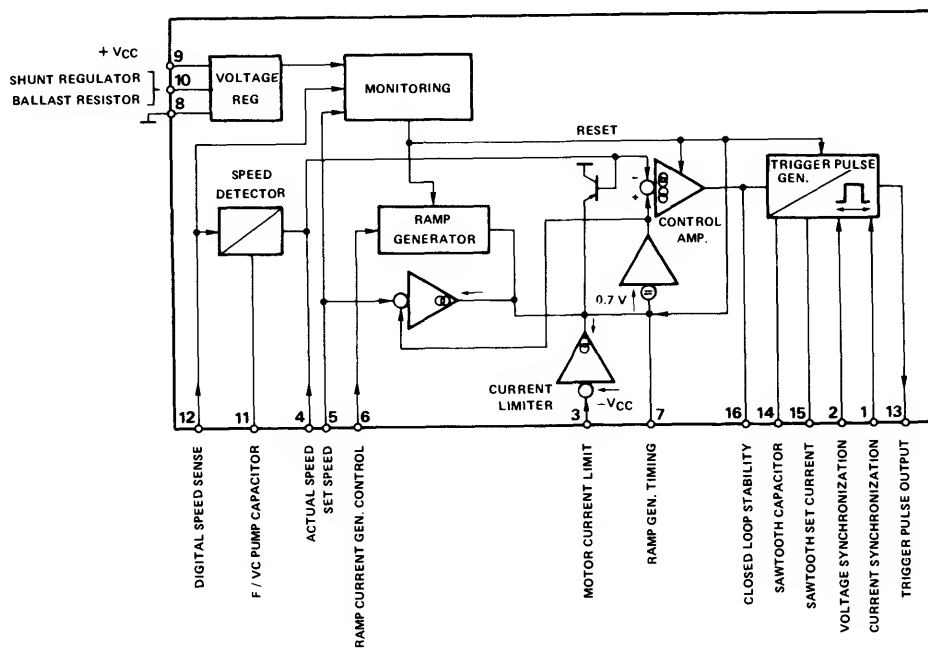


PLASTIC PACKAGE
CASE 648



D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO-16)

FIGURE 1 — BLOCK DIAGRAM AND PIN ASSIGNMENT



TDA1085C

MAXIMUM RATINGS (T_A = 25°C, Voltages are referred to pin 8, Ground)

Rating	Symbol	Value	Unit
Power Supply, when externally regulated, V _{Pin9}	V _{CC}	15	V
Maximum Voltage per listed pin Pin 3 Pin 4-5-6-7-13-14-16 Pin 10	V _{pin}	+5.0 0 to +V _{CC} 0 to +17	V
Maximum Current per listed pin Pin 1 and 2 Pin 3 Pin 9 (V _{CC}) Pin 10 shunt regulator Pin 12 Pin 13	I _{pin}	-3.0 to +3.0 -1.0 to +0 15 35 -1.0 to +1.0 -200	mA
Maximum Power Dissipation	P _D	1.0	W
Junction to Air Thermal Resistance	R _{θJA}	65	°C/W
Operating Junction Temperature	T _A	-10 to +120	°C
Storage Temperature Range	T _{stg}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
VOLTAGE REGULATOR					
Internally Regulated Voltage (V _{Pin9}) (I _{Pin7} = 0, I _{Pin9} + I _{Pin10} = 15 mA, I _{Pin13} = 0)	V _{CC}	15	15.3	15.6	V
V _{CC} Temperature Factor	TF	—	-100	—	ppm/°C
Current Consumption (I _{Pin9}) (V _g = 15 V, V ₁₂ = V _g = 0, I ₁ = I ₂ = 100 μA, all other pins not connected)	I _{CC}	—	4.5	6.0	mA
V _{CC} Monitoring Enabling Level Disable Level	V _{CC} EN V _{CC} DIS	— —	V _{CC} - 0.4 V _{CC} - 1.0	— —	V
RAMP GENERATOR					
Reference Speed Input Voltage Range	V _{Pin5}	0.08	—	13.5	V
Reference Input Bias Current	-I _{Pin5}	0	0.8	1.0	μA
Ramp Selection Input Bias Current	-I _{Pin6}	0	—	1.0	μA
Distribution Starting Level Range (V _{DS})	V _{Pin6}	0	—	2.0	V
Distribution Final Level (V _{DP}) V _{Pin6} = 0.75 V	V _{DS} /V _{Pin6}	2.0	2.09	2.2	
High Acceleration Charging Current V _{Pin7} = 0 V V _{Pin7} = 10 V	-I _{Pin7}	1.0 1.0	— 1.2	1.7 1.4	mA
Distribution Charging Current V _{Pin7} = 2.0 Volts	-I _{Pin7}	4.0	5.0	6.0	μA

TDA1085C

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
CURRENT LIMITER					
Limiter Current Gain — I_{Pin7}/I_{Pin3} ($I_{Pin3} = -300 \mu A$)	C_g	130	180	250	
Detection Threshold Voltage $I_{Pin3} = -10 \mu A$	$V_{Pin3 TH}$	50	65	80	mV
FREQUENCY TO VOLTAGE CONVERTER					
Input Signal "Low Voltage"	$V_{12 L}$	-100	—	—	mV
Input Signal "High Voltage"	$V_{12 H}$	+100	—	—	mV
Monitoring Reset Voltage	$V_{12 R}$	5.0	—	—	V
Negative Clamping Voltage $I_{Pin12} = -200 \mu A$	$-V_{12 CL}$	—	0.6	—	V
Input Bias Current	$-I_{Pin12}$	—	25	—	μA
Internal Current Source Gain $G = \frac{I_{Pin4}}{I_{Pin11}}$, $V_{Pin4} = V_{Pin11} = 0$	G.0	10	10.3	10.5	
Gain Linearity versus Voltage on Pin 4 ($G_{8.6} = \text{Gain for } V_{Pin4} = 8.6 \text{ Volts}$) $V_4 = 0 \text{ V}$ $V_4 = 4.3 \text{ V}$ $V_4 = 12 \text{ V}$	G/ $G_{8.6}$	1.04 1.015 0.965	1.05 1.025 0.975	1.06 1.035 0.985	
Gain Temperature Effect ($V_{Pin4} = 0$)	TF	—	350	—	ppm/ $^{\circ}C$
Output Leakage Current ($I_{Pin11} = 0$)	$-I_{Pin4}$	0	—	100	nA
CONTROL AMPLIFIER					
Actual Speed Input Voltage Range	V_{Pin4}	0	—	13.5	V
Input Offset Voltage $V_{Pin5} - V_{Pin4}$ ($I_{Pin16} = 0$, $V_{Pin16} = 3.0$ and 8.0 Volts)	V_{off}	0	—	50	mV
Amplifier Transconductance ($I_{Pin16}/\Delta(V_5 - V_4)$) ($I_{Pin16} = +$ and $-50 \mu A$, $V_{Pin16} = 3.0 \text{ Volts}$)	T	270	340	400	$\mu A/V$
Output Current Swing Capability Source Sink	I_{Pin16}	-200 50	-100 100	-50 200	μA
Output Saturation Voltage	$V_{16 sat}$	—	—	0.8	V
TRIGGER PULSE GENERATOR					
Synchronization Level Currents Voltage Line Sensing Triac Sensing	I_{Pin2} I_{Pin1}	— —	± 50 ± 50	± 100 ± 100	μA
Trigger Pulse Duration ($C_{Pin14} = 47 \text{ nF}$, $R_{Pin15} = 270 \text{ k}\Omega$)	T_p	—	55	—	μs
Trigger Pulse Repetition Period, conditions as a.m.	T_R	—	220	—	μs
Output Pulse Current $V_{Pin13} = V_{CC} - 4.0 \text{ Volts}$	$-I_{Pin13}$	180	192	—	mA
Output Leakage Current $V_{Pin13} = -3.0 \text{ Volts}$	$I_{13 L}$	—	—	30	μA
Full Angle Conduction Input Voltage	V_{14}	—	11.7	—	V
Saw Tooth "High" Level Voltage	$V_{14 H}$	12	—	12.7	V
Saw Tooth Discharge Current, $I_{Pin15} = 100 \mu A$	I_{Pin14}	95	—	105	μA

GENERAL DESCRIPTION

The TDA 1085C triggers a triac accordingly to the speed regulation requirements. Motor speed is digitally sensed by a tachogenerator and then converted into an analog voltage.

The speed set is externally fixed and is applied to the internal linear regulation input after having been submitted to programmable acceleration ramps. The overall result consists in a full motor speed range with two acceleration ramps which allow efficient washing machine control (Distribute function).

Additionally, the TDA 1085C protects the whole system against AC line stop or variations, overcurrent in the motor and tachogenerator failure.

INPUT/OUTPUT FUNCTIONS

(Referred to Figures 1 and 8)

VOLTAGE REGULATOR — (pins 9 and 10) This is a parallel type regulator able to sink a large amount of current and offering good characteristics. Current flow is provided from AC line by external dropping resistors R1, R2, and rectifier: This half wave current is used to feed a smoothing capacitor, the voltage of which is checked by the IC.

When V_{CC} is reached, the excess of current is derived by another dropping resistor R10 and by pin 10. These three resistors must be determined in order:

- to let 1mA flow through pin 10 when AC line is minimum and V_{CC} consumption is maximum (fast ramps and pulses present).
- to let V_{I0} reach 3V when AC line provides maximum current and V_{CC} consumption is minimum (no ramps and no pulses).
- all along the main line cycle, the pin 10 dynamic range must not be exceeded unless loss of regulation.

An AC line supply failure would cause shut down.

The double capacitive filter built with R1 and R2 gives an efficient V_{CC} smoothing and helps to remove noise from set speeds.

SPEED SENSING — (pins 4-11-12) The IC is compatible with an external analog speed sensing: its output must be applied to pin 4, and pin 12 connected to pin 8.

In most of the applications it is more convenient to use a digital speed sensing with an unexpensive tachogenerator which doesn't need any tuning. During every positive cycle at pin 12, the capacitor $C_{pin 11}$ is charged to almost V_{CC} and during this time, pin 4 delivers a current which is 10 times the one charging $C_{pin 11}$. The current source gain is called G and is tightly specified, but nevertheless requires an adjustment on Rpin 4. The current into this resistor is proportional to $C_{pin 11}$ and to the motor speed; being filtered by a capacitor, $V_{pin 4}$ becomes smoothed and represents the "true actual motor speed".

To maintain linearity into the high speed range, it is important to verify that $C_{pin 11}$ is fully charged: the internal source on pin 11 has 100 K Ω impedance. Nevertheless $C_{pin 11}$ has to be as high as possible as it has a large influence on FV/C temperature factor. A 470 K Ω resistor between pins 11 and 9 reduces leakage currents and temperature factor as well, down to neglectable effects.

Pin 12 has also a monitoring function: when its voltage is above 5V, the trigger pulses are inhibited and the IC is reset. It also senses the tachogenerator continuity and in case of any circuit aperture, it inhibits pulse, avoiding the motor to run out of control. In the TDA 1085C, pin 12 is negatively clamped by an internal diode which removes the necessity of the external one used in the former circuit.

RAMP GENERATOR — (pins 5-6-7) The true Set Speed value taken in consideration by the regulation is the output of the ramp generator (pin 7). With a given value of speed set input (pin 5), the ramp generator charges an external capacitor $C_{pin 7}$ up to the moment $V_{pin 5}$ (set speed) equals $V_{pin 4}$ (true speed), see fig. 2. The IC has an internal charging current source of 1.2mA and delivers it from 0 to 12 V at pin 7. It is the high acceleration ramp (5 seconds typ.) which allows rapid motor speed changes without excessive strains on the mechanics. The TDA 1085C offers in addition the possibility to break this high acceleration with the introduction of a low acceleration ramp (called Distribution) by reducing the pin 7 source current down to 5 μ A under pin 6 full control, as shown by following conditions:

- Presence of high acceleration ramp $V_{pin 5} > V_{pin 4}$
- Distribution occurs in the $V_{pin 4}$ range (true motor speed) defined by $V_{pin 6} \leq V_{pin 4} \leq 2V_{pin 6}$

For two fixed values of $V_{pin 5}$ and $V_{pin 6}$, the motor speed will have high acceleration, excluding the time for $V_{pin 4}$ to go from $V_{pin 6}$ to two times this value, high acceleration again, up to the moment the motor has reached the set speed value, at which it will stay, see fig. 3.

Should a reset happen (whatever the cause would be), the above mentioned successive ramps will be fully reproduced from 0 to the max. speed. If $V_{pin 6} = 0$, only the high acceleration ramp occurs.

To get a real zero speed position, pin 5 has been designed in such a way that its voltage from 0 to 80 mV is interpreted as a true zero. As a consequence, when changing the speed set position, the designer must be sure that any transient zero would not occur: if any, the entire circuit will be reset.

As the voltages applied by pins 5 and 6, are derived from the internal voltage regulator supply and pin 4 voltage is also derived from the same source, motor speed, which is determined by the ratios between above mentioned voltages, is totally independent from V_{CC} variations and temperature factor.

CONTROL AMPLIFIER — (pin 16) It amplifies the difference between true speed (pin 4) and set speed (pin 5), through the ramp generator. Its output available at pin 16 is a double sense current source with a max. capability of $\pm 100 \mu$ A and a specified transconductance (340 μ A/V typ.). Pin 16 drives directly the trigger pulse generator, and must be loaded by an electrical network which compensates the mechanical characteristics of the motor and its load, in order to provide stability in any condition and shortest transient response, see fig. 4.

This network must be adjusted experimentally.

In case of a periodic torque variations, pin 16 provides directly the phase angle oscillations.

TRIGGER PULSE GENERATOR — (pins 5 1-2-13-14-15)

This circuit performs four functions:

- The conversion of the control amplifier DC output level to a proportionnal firing angle at every main line half cycle.
- The calibration of pulse duration.
- The repetition of the pulse if the triac fails to latch on if the current has been interrupted by brush bounce.
- The delay of firing pulse until the current crosses zero at wide firing angles and inductive loads.

R_{pin 15} programs the pin 14 discharging current. Saw-tooth signal is then fully determined by R₁₅ and C₁₄ (usually 47 nF). Firing pulse duration and repetition period are in inverse ratio to the saw-tooth slope.

Pin 13 is the pulse output and an external limiting resistor is mandatory. Max current capability is 200 mA.

CURRENT LIMITER — (pin 3) Safe operation of the motor and triac under all conditions is ensured by limiting the peak current. The motor current develops an alternative voltage in the shunt resistor (0.05 ohm in fig. 4). The negative half waves are transferred to pin 3 which is positively preset at a voltage determined by resistors R₃ and R₄. As motor current increases, the dynamical voltage range of pin 3 increases and when pin 3 becomes slightly negative in respect of pin 8 a current starts to circulate in it. This current, amplified typically 180 times, is then used to discharge pin 7 capacitor and, as a result, reduces firing angle down to a value where an equilibrium is reached. The choice of resistors R₃, R₄ and shunt determines the magnitude of the discharge current signals on C_{pin 7}.

Notice that the current limiter acts only on peak Triac current.

APPLICATION NOTES (Referred to Figure 4)

PRINTED CIRCUIT LAYOUT RULES

In the common applications, where TDA1085C is used, there is on the same board, presence of high voltage, high currents as well as low voltage signals where millivolts count. It is of first magnitude importance to separate them each other and to respect following rules:

- Capacitors decoupling pins which are the inputs of the same comparator, must be physically close to the IC, close to each other and grounded in the same point.
- Ground connexion for tachogenerator must be directly connected to pin 8 and should ground only the tach. In effect the latter is a first magnitude noise generator due to its proximity of the motor which induces high dφ/dt signals.
- The ground pattern must be in the "star style", in order to fully eliminate power currents flowing in the ground network devoted to capacitors decoupling sensitive pins: (4-5-7-11-12-14-16).

As an example, fig. 5 presents a PC board pattern which concerns the group of sensitive pins and their associated capacitors into which the a.m. rules have been implemented. Notice the full separation of "Signal World" from "Power" one by line AB and their communication by a unique strip.

These rules will lead to much satisfactory volume production

in the sense that speed adjustment will stay valid in the entire speed range.

POWER SUPPLY

As dropping resistor dissipates noticeable power, it is necessary to reduce the I_{CC} needs down to a minimum. Triggering pulses, if a certain number of repetition is in reserve to cope with motor brush wearing at end of its life, are the largest I_{CC} user. Classical worst case configuration have to be considered to select dropping resistor. In addition the parallel regulator must be always into its dynamic range, i.e. I_{pin 10} over 1 mA and V_{pin 10} over 3 volt in any extreme configuraton. The double filtering cell is mandatory.

TACHOGENERATOR CIRCUIT

The tach signal voltage is proportional to the motor speed. Stability considerations, in addition, require a RC filter the pole of which must be looked at. The combination of both elements yield a constant amplitude signal on pin 12 in most of the speed range. It is recommended to verify this maximum amplitude to be within 1 volt peak in order to have the largest signal/noise ratio without resetting the integrated circuit (which occurs if V_{pin 12} reaches 5.5 V). It must be also verified that the pin 12 signal is approximately balanced between "High" (over 300 mV) and "Low". A 8 poles tach. is a minimum for low speed stability and a 16 poles is even better.

The RC pole of the tach circuit should be chosen within 30 Hz in order to be as far as possible from the 150 Hz which corresponds to the AC line 3rd harmonic generated by the motor during starting procedure. In addition, a high value resistor coming from V_{CC} introduces a positive offset at pin 12, removes noise to be interpreted as a tach signal. This offset should be designed in order to let pin 12 to reach at least -200 mV (negative voltage) at the lowest motor speed. We remember the necessity of an individual tach. ground connection.

FREQUENCY TO VOLTAGE CONVERTER — F V/C

C_{pin 11} has a recommended value of 820 pF for 8 poles tachos and max. motor rpm of 15000, and R_{pin 11} must be always 470 K.

R_{pin 4} should be chosen to deliver within 12 volts at maximum motor speed in order to maximize signal/noise ratio. As the FV/C ratio as well as the C_{pin 11} value are dispersed, R_{pin 4} must be adjustable and should be made of a fixed resistor in serie with a trimmer representing 25% of the total. Adjustment would become easier.

Once adjusted, for instance at maximum motor speed, the F V/C presents a residual non linearity; the conversion factor (mV per R.P.M.) increases by within 7.7% as speed tends to zero. The guaranteed dispersion of the latter being very narrow, a maximum 1% speed error is guaranteed if during pin 5 network design the small set values are modified, once for ever, according this increase.

The following formulae gives V_{pin 4}:

$$V_{pin4} = 140 \cdot C_{pin11} \cdot R_4 \cdot f \cdot \frac{1}{(1 + \frac{180k}{R_{pin11}})} \text{ in volt per Hertz.}$$

SPEED SET — (pin 5) Upon designer choice, a set of external resistors apply a serie of various voltages corresponding to the various motor speeds. When switching external resistors, verify that a voltage below 80 mV in never applied to pin 5, if no, a full circuit reset will occur.

RAMPS GENERATOR — (pin 6) If only a high acceleration ramp is needed, connect pin 6 to ground.

When a Distribute ramp should occur, pre-set a voltage on pin 6 to which corresponds the motor speed starting ramp point. Distribution (or low ramp) will continue up to the moment the motor speed would have reached twice the starting value.

The ratio of two is imposed by the IC. Nevertheless it could be externally changed downwards (fig. 6) or upwards (fig. 7).

The distribution ramp can be shortened by an external resistor from V_{CC} charging Cpin 7, adding its current to the internal 5 μA generator.

POWER CIRCUITS

Triac Triggering pulse amplitude must be determined by Pin 13 resistor according to the needs in Quadrant IV. Trigger pulses duration can be disturbed by noise signals, generated by the triac itself, which interfere within pins 14 and 16, precisely those which determine it. While easily visible this effect is harmless.

Triac must be protected from high AC line dV/dt during external disturbances by 100 nF \times 100 Ω network.

Shunt resistor must be as non selfic as possible. It can be made locally by Constantan alloy wiring.

When the load is a DC fed universal motor through a rectifier

bridge, the triac must be protected from commutating dV/dt by a 1 to 2 mH coil in serie with MT₂.

Synchronisation functions are performed by resistors sensing AC line and triac conduction. 820 K values are usual but could be reduced down to 330 K in order to detect the Zeros with accuracy and to reduce the residual DC line component below 20 mA.

CURRENT LIMITATION

The current limiter starts to discharge pin 7 capacitor (reference speed) as Motor current reaches the designed threshold level. The loop gain is determined by the resistor connecting pin 3 to the serie shunt. Experience has shown that its optimal value for a 10 A rms limitation is within 2 K Ω . Pin 3 input has a sensitivity in current which is limited to reasonable values and should not react to spikes.

If not used, pin 3 must be connected to a max. positive voltage of 5 V rather to be left open.

LOOP STABILITY

The pin 16 network is predominant and must be adjusted experimentally during module development. The values indicated in fig. 4 are typical for washing machines applications but accept large modifications from one model to another. R16, it is the sole restriction, should not be below 33 k otherwise slow rate limitation will cause large transient errors for load steps.

FIGURE 2 — ACCELERATION RAMP

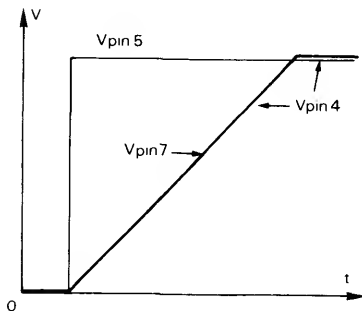


FIGURE 3 — PROGRAMMABLE DOUBLE ACCELERATION RAMP

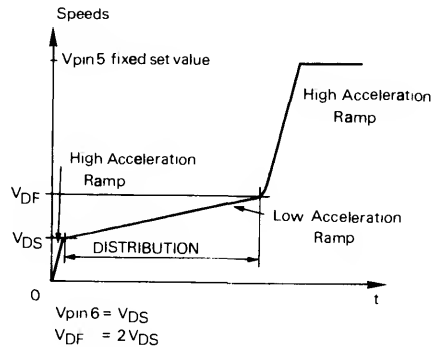
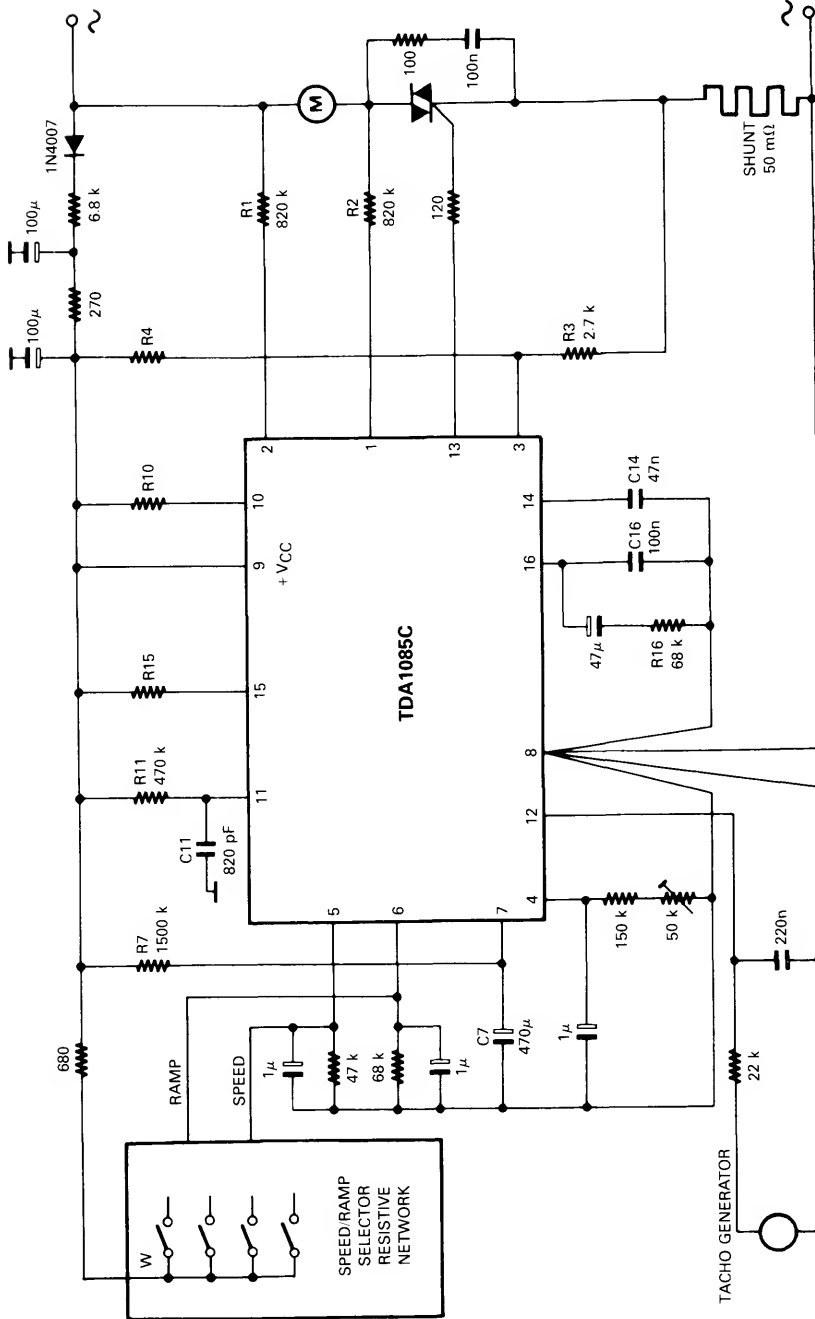


FIGURE 4 — BASIC APPLICATION CIRCUIT

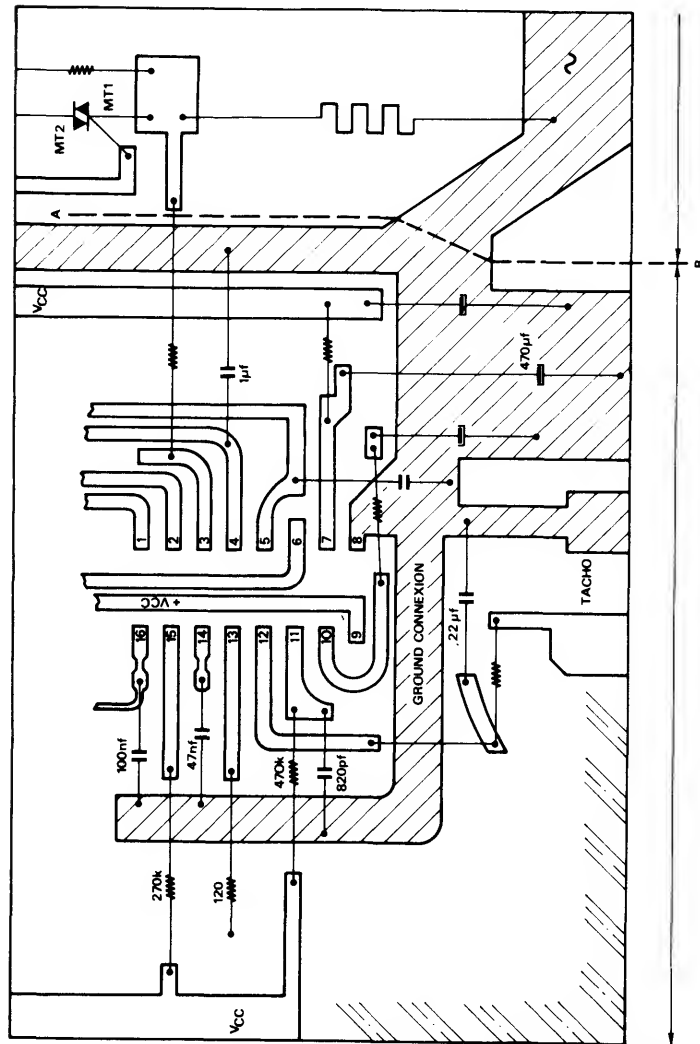


Current limitation: 10 A adjusted by R_4 experimentally
 Ramps High acceleration: 3200 rpm per second
 Distribution ramp: 10 s from 850 to 1300 rpm

Pin 5 voltage Set:
 Wash 800 rpm 609 mV Including nonlinearity corrections
 Distribution 1300 996 mV Including nonlinearity corrections
 Spin 1: 7500 5.912 V Including nonlinearity corrections
 Spin 2: 15,000 12,000 V Adjustment point

Motor Speed Range: 0 to 15,000 rpm
 Tachogenerator 8 poles
 delivering 30 V peak to peak at 6000 rpm, in open circuit
 FVC Factor: 8 mV per rpm (12 V full speed) $C_{pin11} = 680 \text{ pF}$ $V_{CC} = 15.3 \text{ V}$
 TRIAC MAC15A-8 15 A 600 V
 lgt min = 90 mA to cover Quad IV at -10°C

FIGURE 5 — PC BOARD LAYOUT



TDA1085C

FIGURE 6 – DISTRIBUTION SPEED $k < 2$

For $k = 1.6$, $R_3 = 0.6 (R_1 + R_2)$,
 $R_3 C$ within 4 seconds

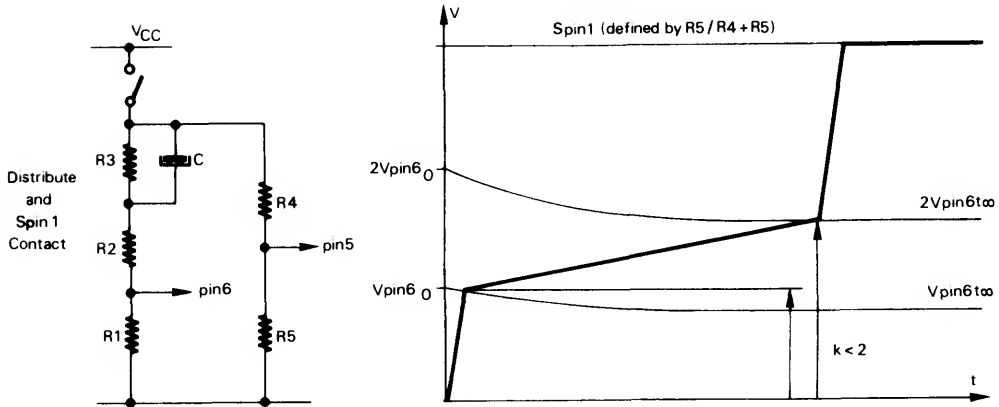


FIGURE 7 – DISTRIBUTION SPEED $k > 2$

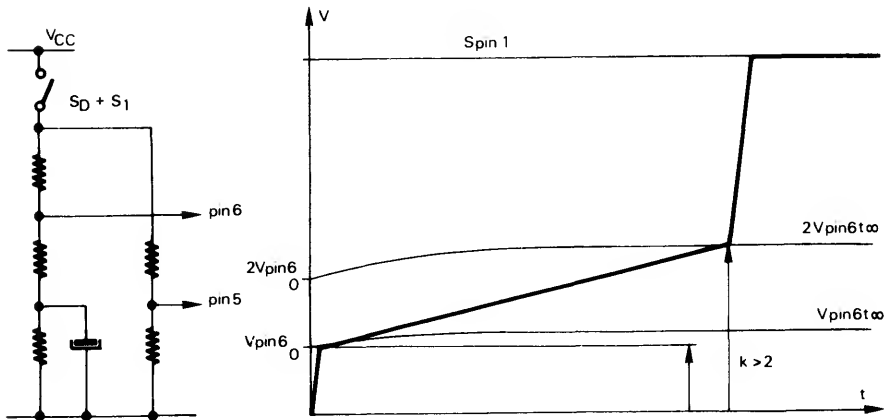
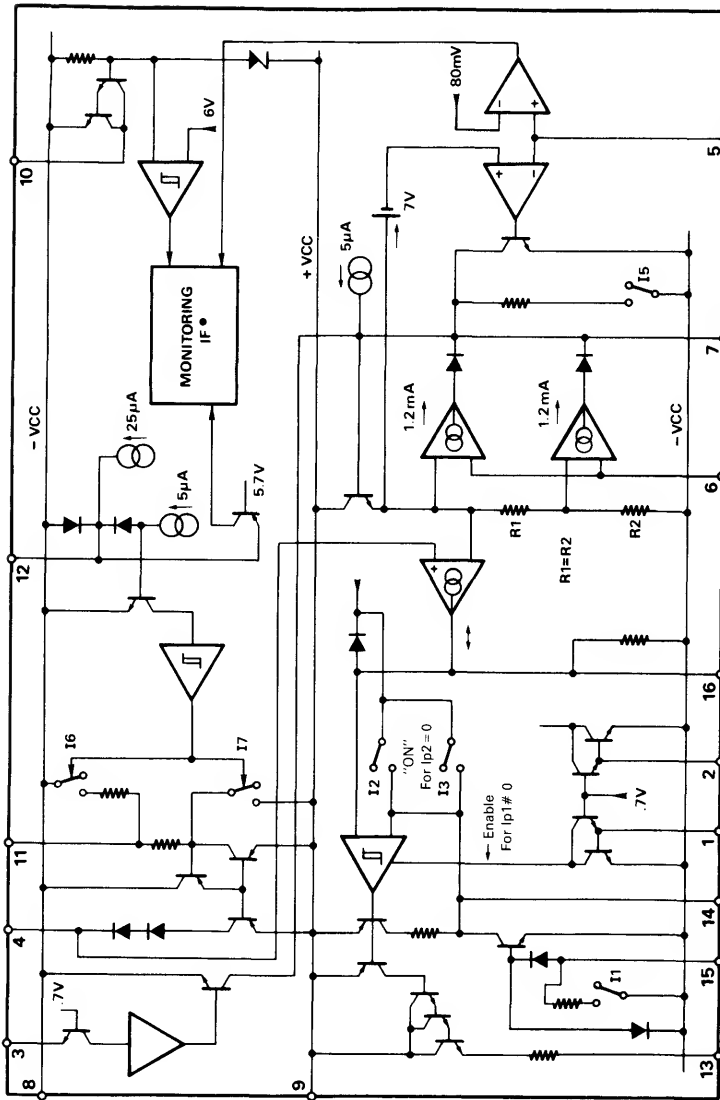


FIGURE 8 — SIMPLIFIED SCHEMATIC



* (P12 connected) AND (VCC OK) AND (VP5 > 80mV)
 THEN
 (I1 OFF), (I2 OFF), (I4 OFF) AND (I5 OFF)

TDA1185A

TRIAC PHASE ANGLE CONTROLLER

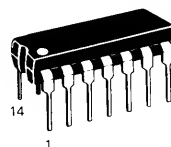
The TDA1185A generates controlled TRIAC triggering pulses and allows tachless speed stabilization of universal motors by an integrated positive feedback function. Typical applications are power hand tools, vacuum cleaners, mixers, light dimmer and other small appliances.

- Supply Power Obtained From AC Line
- Can Be Used with 220 V/50 Hz or 110 V 60 Hz
- Low Count/Cost External Components
- Optimum TRIAC Firing (2nd and 3rd Quadrants)
- Repetitive Trigger Pulses When TRIAC Current is Interrupted by Motor Brush Bounce
- TRIAC Current Sensing to Allow Inductive Loads
- Programmable Soft-Start
- Power Failure Detection and General Circuit Reset
- Low Power Consumption: 6.0 mA

TRIAC PHASE ANGLE CONTROLLER

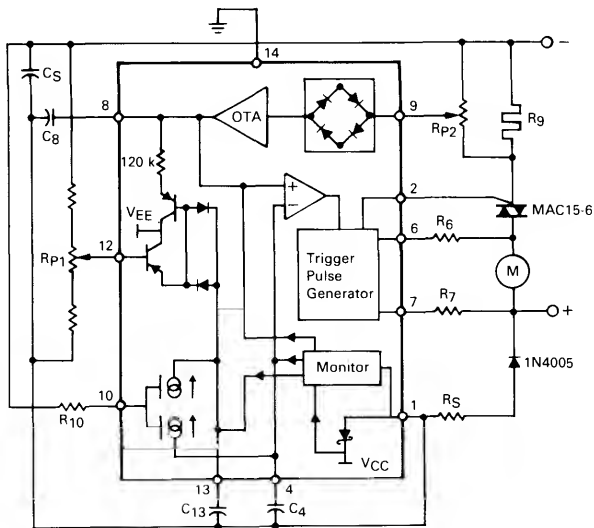
SILICON MONOLITHIC INTEGRATED CIRCUIT

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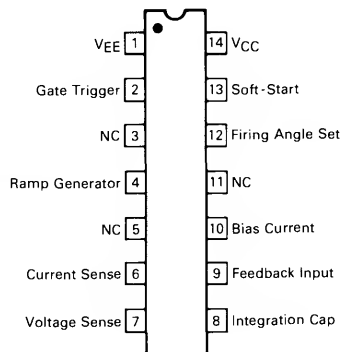


PLASTIC PACKAGE
CASE 646

FIGURE 1 — TYPICAL SYSTEM CONFIGURATION



PIN CONNECTIONS



TDA1185A

MAXIMUM RATINGS (Voltages are referenced to Pin 14 (ground) unless otherwise noted)

Rating	Symbol	Value	Unit
Maximum Voltage Range per Listed Pin Pins 3-5-11 (not connected) Pins 4-8-13 Pin 2	V _{Pin}	-20 to +20 -V _{CC} to 0 -3.0 to +3.0	V
Maximum Positive Voltage (No minimum value allowed; see current ratings)	V _{Pin 12} V _{Pin 1}	0 0.5	
Maximum Current per Listed Pin Pin 1 Pins 6 and 7 Pin 9 Pin 10 Pin 12	I _{Pin}	±20 ±2.0 ±0.5 ±300 -500	mA mA mA μA μA
Maximum Power Dissipation (<i>at</i> T _A = 25°C)	P _D	250	mW
Maximum Junction to Ambient Thermal Resistance	R _{θJA}	100	°C/W
Operating Ambient Temperature Range	T _A	0 to +70	°C
Storage Temperature Range	T _{stg}	-55 to +125	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, voltages are referenced to Pin 14 (ground), unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Power Supply					
Zener Regulated Voltage, (V _{Pin 1}) I _{Pin 1} = 2.0 mA	-V _{CC}	-9.6	-8.6	-7.6	V
Circuit Current Consumption, I _{Pin 1} V _{Pin 1} = -6.0 V, I _{Pin 2} = 0 A	-I _{CC}	-2.0	-1.0	—	mA
Monitoring Enable Supply Voltage (V _{EN})	V _{Pin 1EN}	V _{CC} + 0.2	—	V _{CC} + 0.5	V
Monitoring Disable Supply Voltage (V _{DIS})	V _{Pin 1DIS}	V _{EN} + 0.12	—	V _{EN} + 0.3	V
Phase Set					
Control Voltage Static Offset V _{Pin 8} - V _{Pin 12}	V _{off}	1.2	—	1.8	V
Pin 12 Input Bias Current	I _{Pin 12}	-200	—	0	nA
V _{Pin 4} - V _{Pin 12} Residual Offset		—	180	—	mV
Soft-Start					
Capacitor Charging Current R _{Pin 10} = 100 kΩ, V _{Pin 13} from -V _{CC} to -3.0 V	I _{Pin 13}	-17	-14	-11	μA
Sawtooth Generator					
Sawtooth Capacitor Discharge Current R ₁₀ = 100 kΩ V _{Pin 4} from -2.0 to -6.0 V	I _{Pin 4}	67	70	73	μA
Capacitor Charging Current	I _{Pin 4}	-10	—	-1.5	mA
Sawtooth "High" Voltage (V _{Pin 4})	V _H TH	-2.5	-1.6	-1.0	V
Sawtooth Minimum "Low" Voltage (V _{Pin 4})	V _L TH	—	-7.1	—	V
Positive Feedback					
Pin 9 Input Bias Current, V _{Pin 9} = 0	I _{Pin 9}	—	2 × I _{Pin 10}	—	
Programming Pin Voltage Related to Pin 1	V _{Pin 10}	1.0	1.25	1.5	V
Transfer Function Gain ΔV _{Pin 8} /ΔV _{Pin 9} R ₁₀ = 100 kΩ, ΔV _{Pin 9} = 50 mV	A	—	75	—	
R ₁₀ = 270 kΩ, ΔV _{Pin 9} = 50 mV	A	—	36	—	
Pin 8 Output Internal Impedance	Z _{Pin 8}	—	120	—	kΩ
Trigger Pulse Generator					
Output Current (Sink) V _{Pin 2} = 0 V	I _{Pin 2}	60	—	80	mA
Output Leakage Current V _{Pin 2} = +2.0 V		—	—	4.0	μA
Output Pulse Width C ₄ = 47 nF R ₁₀ = 270 kΩ	t _p	—	55	—	μs
Output Pulse Repetition Period C ₄ = 47 nF R ₁₀ = 270 kΩ	t	—	420	—	μs
Current Synchronization Threshold Levels I _{Pin 6} · I _{Pin 7}	I _{SYNC}	-40	—	+40	μA

PIN FUNCTION DESCRIPTION

Pin No.	Function	Description
1	V _{EE}	This pin is the negative supply for the chip and is clamped at -8.6 V by an internal zener.
2	Gate Trigger Pulse	This pin supplies -1.0 V TRIAC trigger pulse at twice the line frequency.
3	NC	Not connected
4	Ramp Generator	The value of the capacitor at this pin determines the slope of the ramp.
5	NC	Not connected
6	Current Sense	This pin senses if the TRIAC is on, and if so, will disable the gate trigger pulse.
7	Voltage Sense	The internal timing of the chip is set by the frequency of the voltage at this pin.
8	Integration Capacitor	This pin is the output of the feedback and the variation in voltage is averaged out by the capacitor.
9	Feedback Input	The change in load current is detected by the change in voltage across R ₉ .
10	Current Program	The bias current for the circuit is determined by the resistor value at this pin.
11	NC	Not connected
12	Phase Angle Set	The voltage at this pin sets the no-load firing angle.
13	Soft-Start	The firing angle is slowly increased from 180° to the set value of Pin 12.
14	V _{CC}	Ground

INTRODUCTION

The Motorola TDA1185A generates trigger pulses (Pin 2) for TRIAC control of power into an AC load. The TRIAC trigger pulse is determined by generating a ramp voltage (Pin 4) synchronized to twice the AC line frequency and compared to an external set voltage (Pin 12) representing the conduction angle. Gate pulses are negative (sink current) and thus the TRIAC is driven into its most effective quadrants (Q2-Q3).

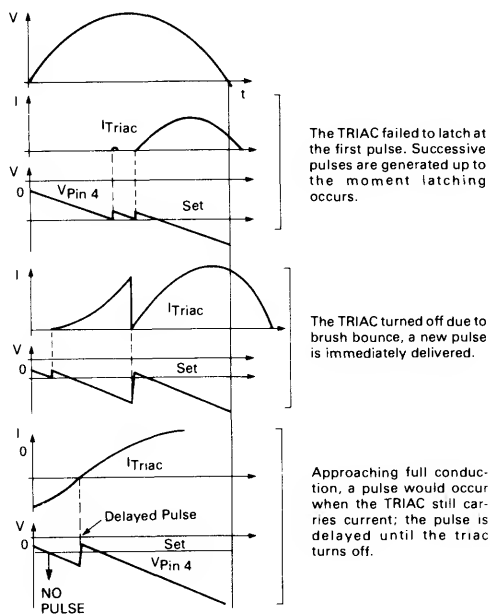
If the load is a Universal motor (the speed of which decreases as torque increases), the TDA1185A allows to increase the conduction angle proportionally to the motor current, sensed (Pin 9) by a low value resistor in series with the load.

FUNCTIONAL DESCRIPTION

DC POWER SUPPLY — DC power is directly derived from the AC line through a 2.0 watt resistor, half-wave rectifier and filtering capacitor circuit. The V_{EE} voltage is internally regulated by an integrated zener. Referenced to ground (Pin 14), the power supply voltage is -8.6 V. The TDA1185A internal consumption is 6.0 mA.

TRIGGER PULSE GENERATOR — It delivers a 60 mA minimum sink current pulse (Pin 2) through an internally short circuit protected output. Pulse width is roughly proportional to $R_{10} \times C_4$ and is repeated every 420 μ s if TRIAC fails to latch or is switched off by brush bounce. With inductive loads, the current lags in respect to the voltage. Pin 6 delays the triggering pulse up to the moment the TRIAC is off, in order to prevent erratic power control (see Figure 2).

FIGURE 2 — MULTIPULSE GENERATION DELAYED PULSE



RAMP GENERATOR — A constant current sink discharges capacitor C_4 producing a negative voltage ramp synchronized with the main line. Pin 4 voltage is reset to -1.6 volts at every AC line zero crossing (see Figure 3) and ramps down to -7.1 volts. The constant current sink is externally programmable by R_{10} using the equation below.

$$I_4 = I_{10} \pm 5\%$$

$$I_{10} = \frac{|V_{EE} + 1.25|}{R_{10}}$$

MAIN COMPARATOR — Its role is to determine the trigger pulse which occurs when the ramp voltage equals the phase angle set voltage at Pin 12. Fixed phase angle set voltage values lead to a constant TRIAC conduction angle unless positive current feedback (Pin 9) is connected or the Soft-Start capacitor (Pin 13) is not charged.

SOFT-START — The TDA1185A allows the user to avoid any abrupt inrush of current into the load. This provides protection for fragile loads, light bulbs or tubes. Another advantage is that the AC line disturbance is minimized.

The conduction angle is established from zero to the set value at Pin 12 according to a voltage ramp generated by a constant current delivered to C_{13} . The value of current I_{13} can be expressed by the following equation:

$$I_{13} = 0.2 \times I_{10} \pm 10\%$$

The voltage ramp lasts as long as V_{13} is lower than the set voltage V_{12} . Upon reset, V_{13} is forced to V_{EE} as shown in Figure 4. If the load is a universal motor, it will not turn until a minimum conduction angle is achieved to overcome friction. The time the voltage ramp requires to reach its threshold value is considered "dead" time, and can be eliminated by an appropriate series resistor at Pin 13. The voltage drop developed by I_{13} thru the resistor causes the conduction angle to immediately reach the threshold value and have the Soft-Start function without dead time (see Figure 5).

FIGURE 3 — TRIGGERING PULSE TIMING

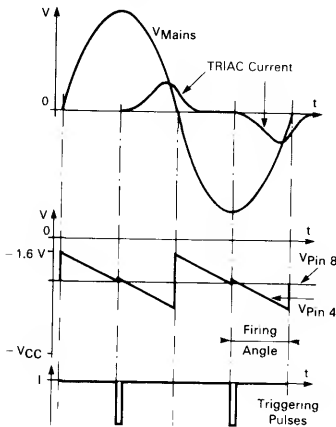


FIGURE 4 — SOFT START

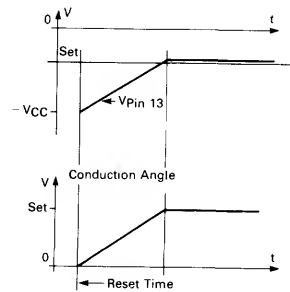


FIGURE 5 — SOFT-START WITHOUT DEAD TIME

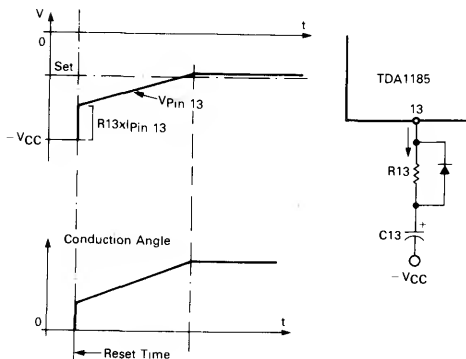
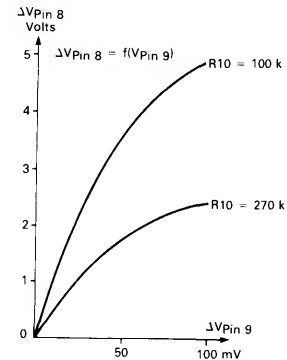


FIGURE 6 — TRANSFER FUNCTION



POSITIVE CURRENT FEEDBACK — The Universal motor speed drops as load increases. To maintain the speed, the TRIAC conduction angle must be increased. For this purpose, Pin 9 senses the motor current as a **voltage** developed in a low value resistor, R_g , amplifies, rectifies and adds it internally to the set voltage at Pin 12. Any voltage variation at the output of the feedback, Pin 8, is smoothed out by capacitor C_g . The transfer function, $\Delta V_8 = f(\Delta V_g)$, is shown in Figure 6.

The gain in the linear region is dependent on R_{10} . The voltage transferred to Pin 8 is proportional to the current RMS value, as motor current is not far from a sine wave. This averaging effect is shown in Figure 7.

With large amplitude signals at Pin 9, the change in voltage at Pin 8 reaches a maximum value. This saturation effect limits the maximum conduction angle increase. This effect is illustrated in Figure 8 where the total Pin 8 voltage can be written as follows:

$$V_8 = V_{12} + f(|V_g|, R_{10}) + 1.25$$

The effect of the feedback is illustrated in Figure 9.

MONITORING — A central logic block performs the ENABLE/DISABLE function of the IC with respect to power supply voltage. Under DISABLE conditions, Pin 4, 8, 12 and 13 are forced to appropriate voltages to prepare for the next reset. Refer to the block diagram in Figure 10.

APPLICATION CONSIDERATIONS

COMPONENT SELECTION — To regulate the speed of a universal motor it is necessary to determine how much gain in the feedback is needed. A change in motor current (due to load increase) causes the conduction angle to change by the appropriate amount to keep the speed constant. This entails, through trial and error, choosing an appropriate resistor value for R_{10} , since the gain of the feedback is determined by value of R_{10} as shown in Figure 8.

FIGURE 7 — AVERAGING EFFECT OF TRANSFER FUNCTION

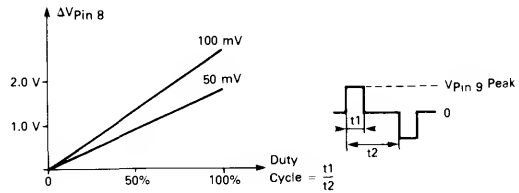
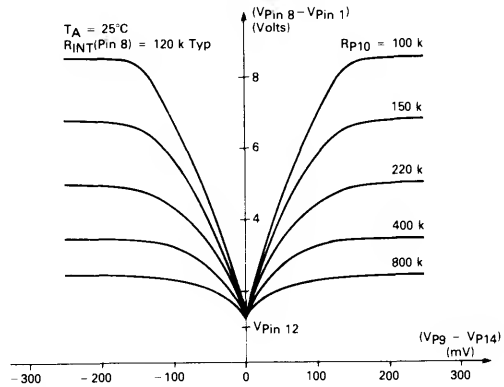


FIGURE 8 — TRANSFER FUNCTION (Pin 8/Pin 9)



Once R_{10} is picked, C_4 can be calculated from the following equation:

$$C_4 \approx \frac{.672}{f_{line} \times R_{10}}$$

where f_{line} is the line frequency.

FIGURE 9 — POSITIVE FEEDBACK EFFECT
(Offset voltages have been neglected)

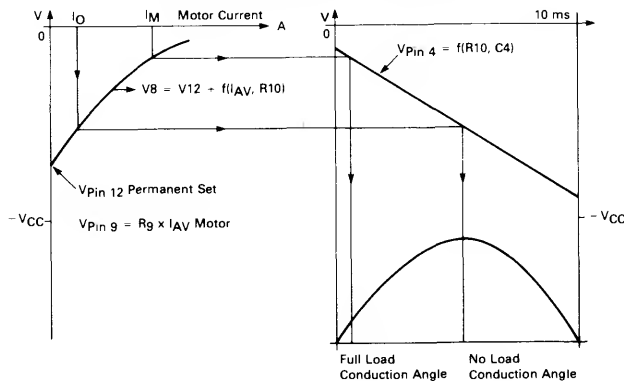
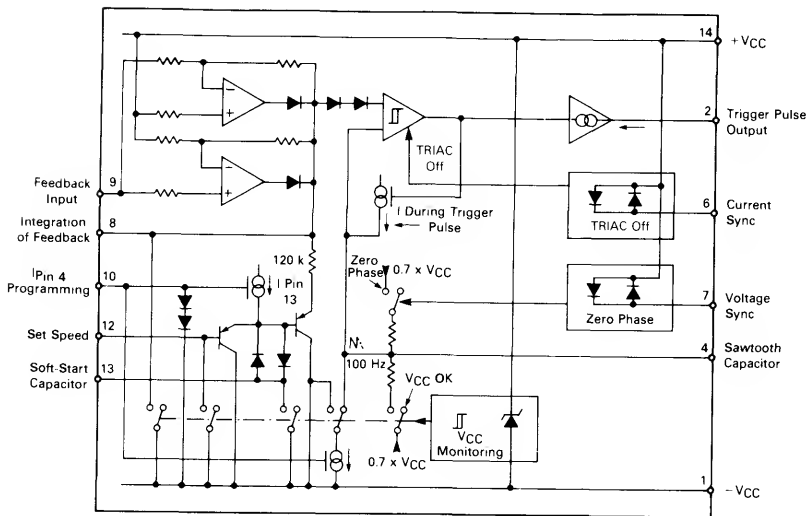


FIGURE 10 — INTERNAL BLOCK DIAGRAM



Capacitor C₈ is an integration cap used to smooth out the voltage at Pin 8. The value should be large enough to accomplish this task yet not too large to slow the response of the system.

Capacitor C₁₃ determines how fast the conduction angle reaches the set value programmed at Pin 12. To achieve a desired delay, the value for C₁₃ can be calculated by the following equation:

$$C_{13} \approx \frac{8 \times t_d}{8.6 - V_{12} \times R_{10}}$$

The remaining component values have experimentally been determined and are constant, regardless of application. The following table lists typical values for 110 volt application.

Component	Value	Units
R ₅	10/2.0 W	kΩ
R _{P1}	100	kΩ
R _{P2}	100	Ω
R ₆	330/0.5 W	kΩ
R ₇	330/0.5 W	kΩ
R ₉	0.05/5.0 W	Ω
R ₁₀	100	kΩ
C ₄	0.1	μF
C ₈	0.22	μF
C ₁₃	10	μF

Using an oscilloscope, it should be verified that the ramp generator is ramping down from -1.6 to -7.1 volts. The slope of the ramp can be changed by C₄ and the DC level of the waveform can be adjusted by R₇.

Pin 9 has a low internal impedance and requires R_{P2} to adjust the feedback level. Pin 8 must always be connected to V_{EE} through a filtering capacitor. For values of R₁₀ less than 100 kΩ, the circuit becomes sensitive and could become unstable. Figures 11 and 12 show typical waveforms. As shown, the increase in motor current has resulted in the firing angle to decrease. This translates to an increase in the average power delivered to the load.

FIGURE 11 — NO LOAD APPLIED

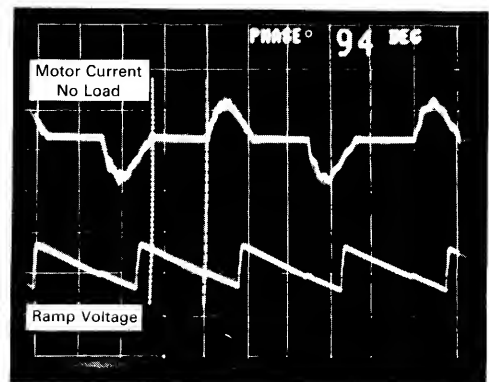
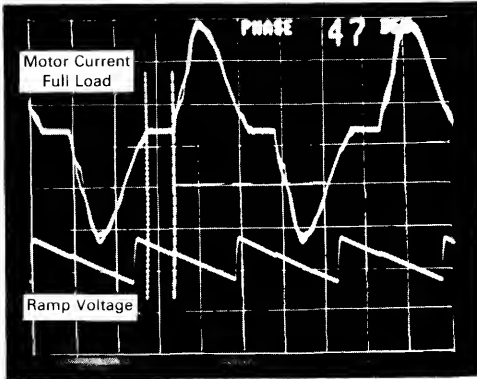


FIGURE 12 — LOAD APPLIED



TEMPERATURE EFFECTS — The TDA1185A has a very efficient internal temperature compensation. If the current feedback is not connected, the RMS power delivered to the load is stabilized within $\pm 0.2\%$ over a temperature range of $+20$ to $+70^\circ\text{C}$. The feedback introduces, in the same temperature range, a drift of 250 mV on the voltage of Pin 8; this slight increase in conduction angle may be successfully used to compensate a motor ohmic resistance increase with temperature.

MAIN LINE VOLTAGE COMPENSATION — As the conduction angle is independent of main line voltage, any change in the latter induces a power variation to the load. A resistor connected to the rectifier anode and to Pin 12 with a capacitor to V_{EE} will introduce a decrease in voltage at Pin 12 as the line voltage is increasing. The values of the RC network can experimentally be determined.

FIRING ANGLE DYNAMICS — With purely resistive loads, the effective RMS applied voltage to the load is directly proportional to the firing angle (Figure 13). With inductive loads, since the current lags with respect to voltage, 100% power corresponds to a firing angle which is less than 180° .

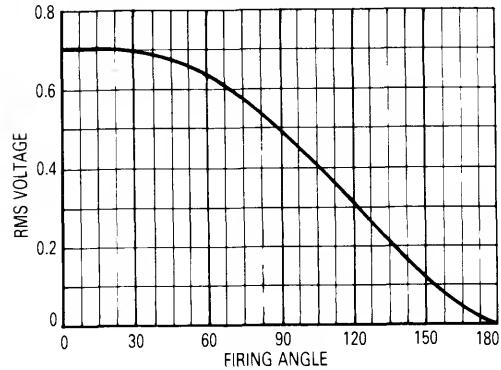
APPLICATION IDEAS

SOFT-START — The Soft-Start feature of the TDA1185A in itself opens the door to a lot of interesting applications. For example, the TDA1185A can be used to bring up fragile loads slowly. Expensive and sensitive tubes can be turned on slowly thus eliminating the inrush of current that could lead to burn out. In this application R_{P1} is replaced with a resistor divider such that the voltage at Pin 12 results in a conduction angle of 180° . Pin 9 should be grounded, since the feedback portion of the TDA1185A is not necessary (see Figure 14). The time to achieve full conduction is found by the equation below:

$$\Delta t \approx 8.71 \times R_{10} \times C_{13}$$

LIGHT DIMMER — With practically no modification the TDA1185A can be used in a light dimmer application. All that is required is to ground the input to the feedback. Pin 9. By grounding Pin 9 we have disconnected the feedback loop and the conduction angle is controlled solely by R_{P1} . Further, since the feedback is disconnected, R_9 and R_{P2} are no longer necessary. The Soft-Start feature can still be used to protect the bulb from an inrush of current. This setup can be used in any application that requires manual control of the power delivered to the load (see Figure 15).

FIGURE 13 — RMS VOLTAGE versus FIRING ANGLE

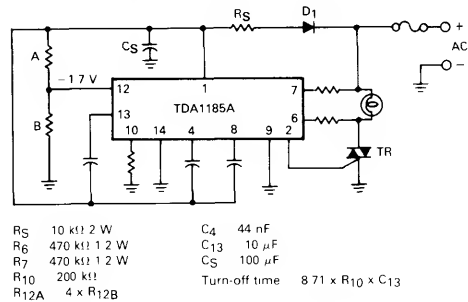


SOFT SHUT-OFF — Once again with little modification, the TDA1185A can be used to turnoff the load slowly. An example of this is in automatic garage lighting. Typically, lights that are on a timer go off without a warning, usually in the most inopportune time (like when you're about to step over the dog). With a soft shut-off, the light dims out slowly, alerting you that it is about to go off. As in the previous case, the feedback is disconnected and R_{P1} is replaced with capacitor C_{12} and a switch (see Figure 16). The turn-off time can be calculated by the following equation.

$$\Delta t \approx R_{12} \times C_{12}$$

R_{12} is the sum of the two resistors on both sides of C_{12} .

FIGURE 14 — SOFT-START CIRCUIT



PC BOARD — The printed circuit board in Figure 17 is included for the designers convenience to evaluate the TDA1185A. The size of the board is intentionally small to show the compactness that can be achieved. Figure 18 shows the component layout for the PC board. Rp1 has one of the outer leads connected to

VEE and the other to R12. The center lead of Rp1 is connected to Pin 12.

WARNING SHOCK HAZARD: IT IS HIGHLY RECOMMENDED THAT AN ISOLATION TRANSFORMER BE USED. REMOVE THE CHASSIS GROUND FOR ALL TEST EQUIPMENT.

FIGURE 15 — LIGHT DIMMER CIRCUIT

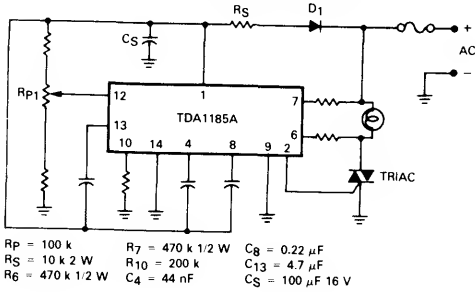


FIGURE 16 — SOFT SHUT-OFF CIRCUIT

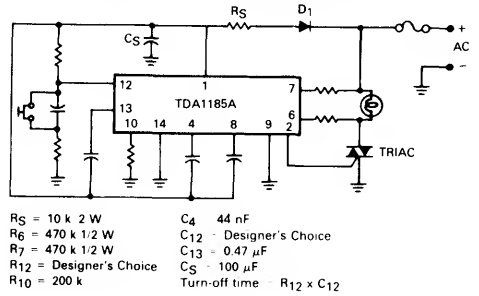
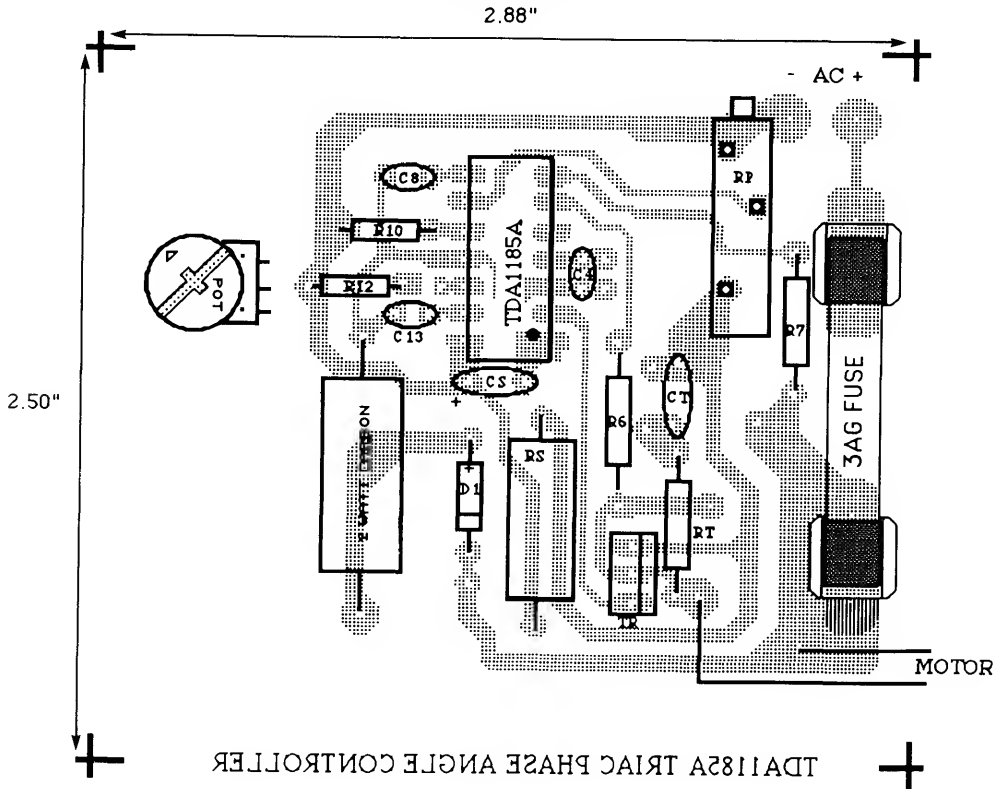
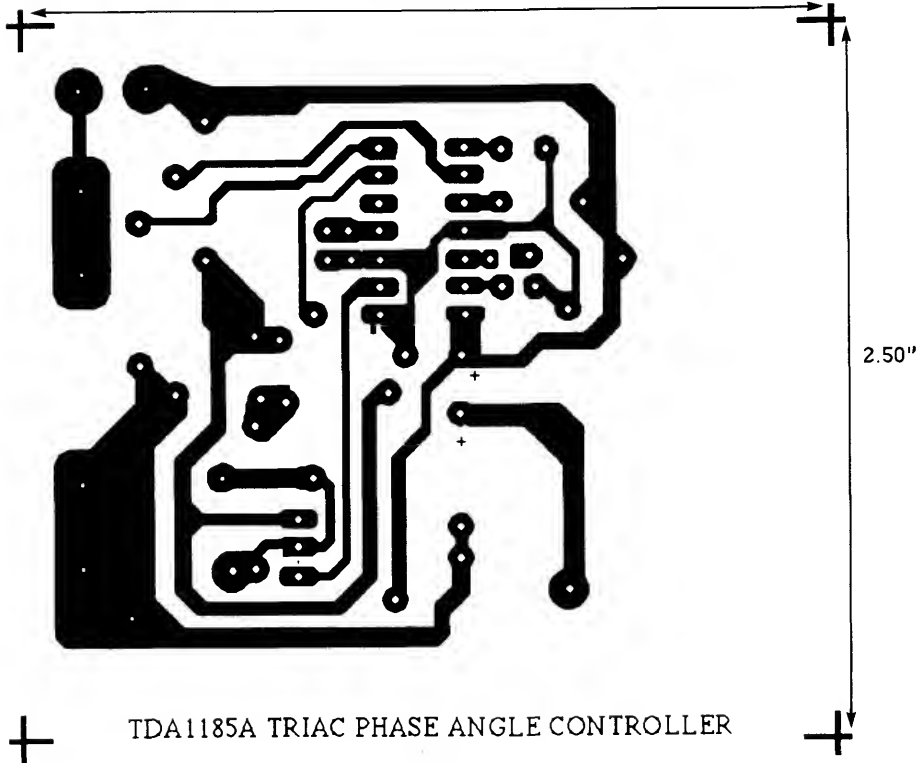


FIGURE 17 — TDA1185A EVALUATION BOARD
COMPONENT SIDE



TDA1185A

FIGURE 18 — TDA1185A EVALUATION BOARD COPPER SIDE
2.88"



4

UAA1016B

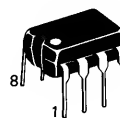
ZERO VOLTAGE CONTROLLER

The UAA1016B is designed to drive triacs with the Zero Voltage technique which allows RFI free power regulation of resistive loads. It provides the following features:

- Proportional Temperature Control Over an Adjustable Band
- Adjustable Burst Frequency (to Comply with Standards)
- Sensor Fail-Safe
- No dc Current Component Through the Main Line (to Comply with Standards)
- Negative Output Current Pulses (TRIAC Quadrants 2 and 3)
- Direct ac Line Operation
- Low External Components Count

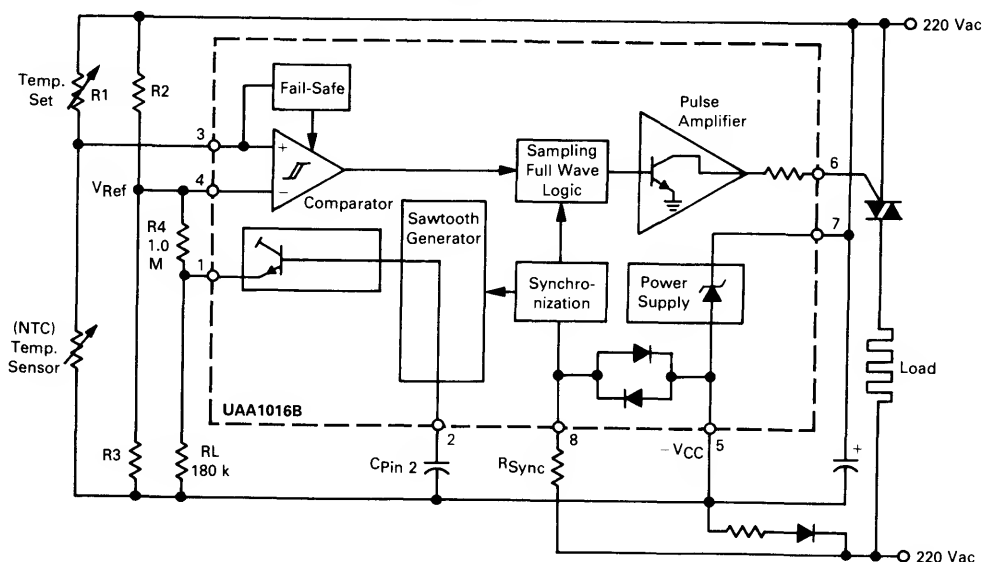
ZERO VOLTAGE SWITCH PROPORTIONAL BAND TEMPERATURE CONTROLLER

**SILICON MONOLITHIC
 INTEGRATED CIRCUITS**



PLASTIC PACKAGE
 CASE 626

FIGURE 1 — BLOCK DIAGRAM AND PIN ASSIGNMENT



- Design Notes:
1. Let $R4 \geq 5RL$
 2. Select $\frac{R2}{R3}$ Ratio for a symmetrical reference deviation centered about Pin 1 output swing, $R2$ will be slightly greater than $R3$.
 3. Select $R2$ and $R3$ values for the desired reference deviation where $\Delta V_{REF} = \frac{\Delta V_{Pin 1}}{\frac{R4}{R2 || R3} + 1}$

MAXIMUM RATINGS (Voltages referred to Pin 7)

Parameter	Symbol	Max. Rating	Unit
Supply Current ($I_{Pin\ 5}$)	I_{CC}	15	mA
Nonrepetitive Supply Current ($I_{Pin\ 5}$)	I_{CCP}	200	mA
AC Synchronization Current (Pin 8)	I_{syn}	3.0	mA (RMS)
Maximum Pin Voltages	$V_{Pin\ 1}$ $V_{Pin\ 2}$ $V_{Pin\ 3}$ $V_{Pin\ 4}$ $V_{Pin\ 6}$	0; $-V_{CC}$ 0; $-V_{CC}$ 0; $-V_{CC}$ 0; $-V_{CC}$ +2.0; $-V_{CC}$	Volt
Maximum Current Drain	$I_{Pin\ 1}$	1.0	mA
Power Dissipation $T_A = 25^\circ\text{C}$	P_D	625	mW
Maximum Thermal Resistance	$R_{\theta JA}$	100	$^\circ\text{C/W}$
Operating Temperature Range	T_A	-20 to +100	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, Voltages referred to Pin 7 unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
Current Consumption (Pins 6 and 8 not connected)	I_{CC}	—	0.8	1.5	mA
Stabilized Supply Voltage ($V_{Pin\ 5}$) $I_{CC} = 2.0\text{ mA max}$	$-V_{CC}$	-9.6	-8.6	-7.6	V
Output Pulse Current ($V_{Pin\ 6}$ from -1.0 to +1.0 Volt)	I_{out}	60	90	120	mA
Output Pulse Width $R_{Pin\ 8} = 220\text{ k}\Omega$, $V_{mains} = 220\text{ Vac}/50\text{ Hz}$, (Figures 4 and 5)	t_{p1} t_{p2}	58 160	60 220	120 320	μs
Comparator Input Offset Voltage ($V_{Pin\ 3} - V_{Pin\ 4}$)	V_{off}	-10	—	+10	mV
Comparator Common Mode Voltage Range	V_{CM}	$-V_{CC} + 1$	—	-1.5	V
Input Bias Current (Pins 3 and 4)	I_B	—	—	1.0	μA
Output Leakage Current ($I_{Pin\ 6}$) $V_{Pin\ 6} = +2.0\text{ V}$	I_{outL}	—	—	10	μA
Fail-safe Threshold Voltage ($V_{Pin\ 3}$)	V_{FSTH}	—	-0.7	—	V
Capacitor Charging Current (Source)	$I_{Pin\ 2}$	-20	-16	-12	μA
Capacitor Discharge Current (Sink)	$I'_{Pin\ 2}$	—	6.4	—	mA
Sawtooth Pulse Length ($C_{Pin\ 2} = 1.0\text{ }\mu\text{F}$)	t_{saw}	—	0.85	—	S
Output Threshold Sawtooth Levels ($V_{Pin\ 2}$)	V_{TH1} V_{TH2}	— —	-1.0 $-V_{CC} + 1.25$	— —	V
Output Voltage Pin 1	$V_{Pin\ 1}$	—	$V_{Pin\ 2} - 0.75$	—	V

CIRCUIT DESCRIPTION

The circuit delivers current pulses to the triac at zero crossings of the main line sensed by Pin 8 through R_{sync} . An internal full wave logic allows the triac to latch during full wave periods in order to avoid any dc component in the main line, in compliance with European regulations. Trigger pulses are generated when the comparator detects $V_{Pin\ 3}$ is above $V_{Pin\ 4}$ (or $V_{reference}$) as sensed temperature through the NTC is then lower than the set value (V_{REF} corresponding to the external Wheatstone bridge equilibrium).

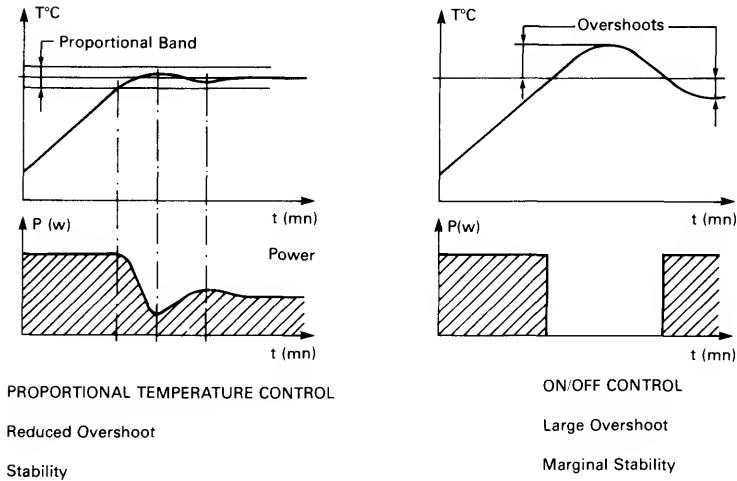
In order to comply with norms limiting the frequency at which a kW sized load, or above, may be connected to the main line (fluorescent tubes "flickering"), the UAA1016B has an internal time base providing (power

is delivered by bursts to the load) a proportional temperature band control. In fact, most of the heating regulation systems require low temperature overshoot for more precision and stability which cannot be accomplished by direct on/off regulation (see Figure 2). An internal low frequency sawtooth generator whose output is available at Pin 1, allows the designer to introduce a periodic linear change of V_{REF} . This deviation defines the temperature band allowing proportional power control (see Figure 3).

A fail-safe circuit inhibits output pulses when the sensor circuit has a fault (open or short circuit).

The IC is directly powered from the mains by a dropping resistor, a diode and a filter capacitor.

FIGURE 2 — PROPORTIONAL TEMPERATURE CONTROL versus ON/OFF CONTROL



KEY CIRCUIT FUNCTIONS DESCRIPTION

POWER SUPPLY — The rectified supply current is Zener regulated to 8.6 V. Current consumption of the UAA1016B is typically less than 1.0 mA. The major part of the current fed by the dropping resistor is used for the sensor bridge and triac gate pulses. Any excess of supply current is excess power dissipation into the integrated Zener. Current consumption of the triac pulses may be derived from Figure 4 and 5 (lgt max. and pulse duration). Usually an 18 k Ω , 2.0 W dropping resistor is convenient to feed the UAA1016.

COMPARATOR — When $V_{Pin\ 3}$ is higher than $V_{Pin\ 4}$ (V_{Ref}), the comparator allows the triggering logic to deliver pulses to the triac (Figure 3). The offset hysteresis input voltage has been designed to be as low as possible (± 10 mV max) in order to minimize the uncontrollable temperature band (proportional to the hysteresis) as per Figure 6. Noise rejection is performed by a synchronous sampling of the comparator output during very short times (typ. less than 100 ns).

SAWTOOTH GENERATOR — A sawtooth voltage signal is generated by a constant current source (typ. 7.5 μ A), charging an external capacitor $C_{Pin\ 2}$ between two threshold levels, V_{TH1} and V_{TH2} , which are respectively:

$$V_{TH1} = -1.0\text{ V}$$

$$V_{TH2} = -V_{CC} + 1.25\text{ V.}$$

Charging and discharging currents occur only with negative halfcycles of the line.

In the UAA1016B, the sawtooth signal is available at Pin 1 as a voltage source $V_{Pin\ 1} = V_{Pin\ 2} - 0.75\text{ V}$.

Maximum source current is 1.0 mA, but to keep good linearity of sawtooth signal, a source current of 40 μ A is recommended (see Figure 7).

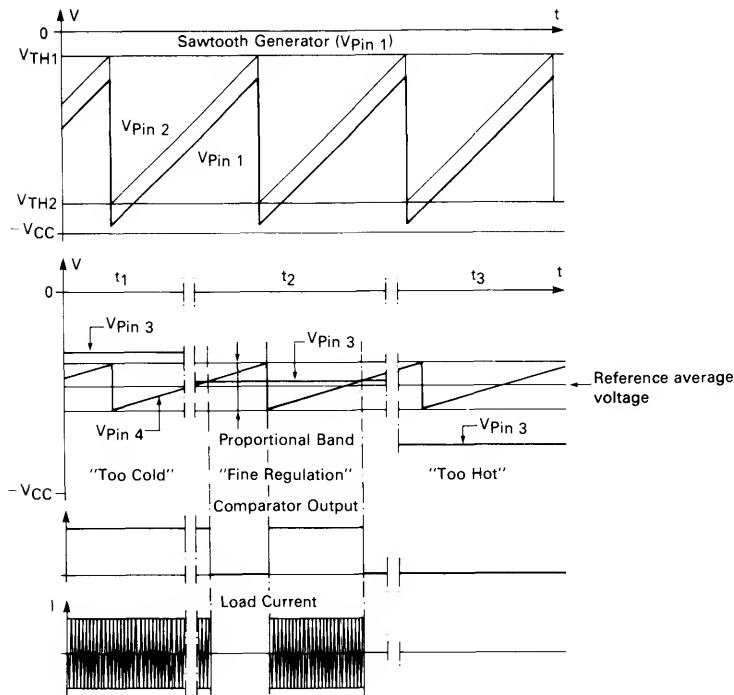
FAIL-SAFE — Output pulses are inhibited by the "fail-safe" circuit if the comparator input voltage exceeds the specified threshold voltage. This would occur if the temperature sensor circuit had a fault.

SAMPLING FULL WAVE LOGIC — Two consecutive zero-crossing trigger pulses are generated at every positive mains half-cycle of the line to minimize generation of noise (as per Figure 8). Within every zero-crossing the pulses are positioned as per Figure 4. Pulse length is also adjustable by R_{sync} on Pin 8 to allow positive triggering of the triac at this critical moment (firing with low voltage between main terminals requires long pulses).

PULSE AMPLIFIER — The pulse amplifier circuit delivers minimum current pulses of 60 mA (sink). The triac is triggered in quadrants II and III.

SYNCHRONIZATION CIRCUIT — This circuit detects mains zero-crossings through R_{sync} and the value selected determines the trigger pulse length. A zero crossing current detector is employed with typical thresholds of $\pm 27\text{ }\mu$ A to $\pm 98\text{ }\mu$ A (see Figures 4 and 5).

FIGURE 3 — SAWTOOTH GENERATOR AND PROPORTIONAL BAND



COMMENTS TO FIGURE 3

Referring to Figure 1, the average value of V_{Ref} is set by R_2 and R_3 . R_4 defines the amplitude of the sawtooth signal superimposed on V_{Ref} , defining the Proportional Band.

Figure 3 shows three conditions:

- 1) During time t_1 we always have $V_{Pin 3} > V_{Ref}$, and as a result, the comparator is always "on" and the triac fired (100% max. power)
- 2) During time t_2 , $V_{Pin 3}$ is in the proportional band, and the average power delivered to the load is a fraction of maximum power.
- 3) During time t_3 , $V_{Pin 3} < V_{Ref}$, and the triac is always "off."

When the sensor temperature is above the set value and is slowly decreasing as no heating occurs, $V_{Pin 3} - V_{Pin 4}$ must exceed half the hysteresis value before power is applied again (1). A similar effect occurs in the opposite direction when temperature sensor is below

the set value and can remain stable as position (2). This defines the "uncontrollable temperature band" which will be very small if hysteresis is also very small.

SUGGESTIONS FOR USE

The temperature sensor circuit is a Wheatstone bridge including the sensor element. Comparator inputs may be free from power line noise only if the sensor element is purely resistive (NTC resistor). Usage of any P-N junction sensor would drastically reduce noise rejection.

Fixed phase sensing of the internal comparator output eliminates parasitic signals.

Some loads, even designed to be resistive, have in fact a slight inductive component. A phase shift at Pin 8 can be achieved with external capacitor C_3 connected to Pin 8 network (see Figure 9).

Suggested maximum source current at Pin 1 is 40 μA , in order to have acceptable sawtooth signal linearity.

FIGURE 4 — OUTPUT PULSE WIDTH DEFINITIONS

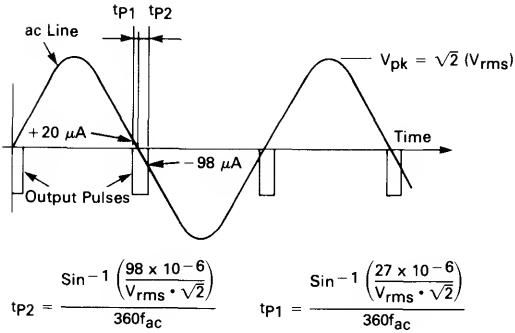


FIGURE 5 — TYPICAL OUTPUT PULSE LENGTH versus SYNCHRONIZATION RESISTOR

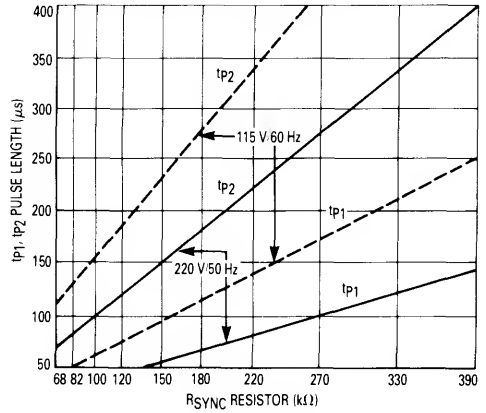


FIGURE 6 — EFFECTS OF INPUTS COMPARATOR HYSTERESIS

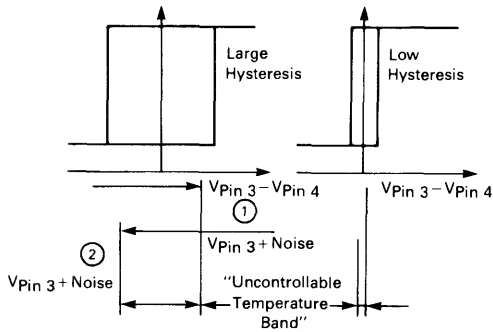


FIGURE 7 — PIN 1 INTERNAL NETWORK

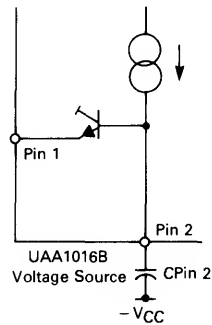
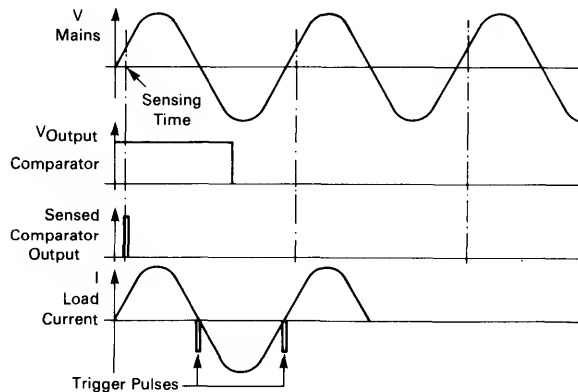


FIGURE 8 — TRIGGER PULSE GENERATION



UAA1016B

APPLICATION CIRCUITS

Figure 9 shows a very simple application of the UAA1016B as an electronic rheostat having 100% efficiency. C_3 is required only if load has an inductive com-

ponent. Figure 10 shows a typical application as a panel heater thermostat with a proportional temperature band of 1°C at 25°C .

FIGURE 9 — APPLICATION CIRCUIT — ELECTRONIC RHEOSTAT

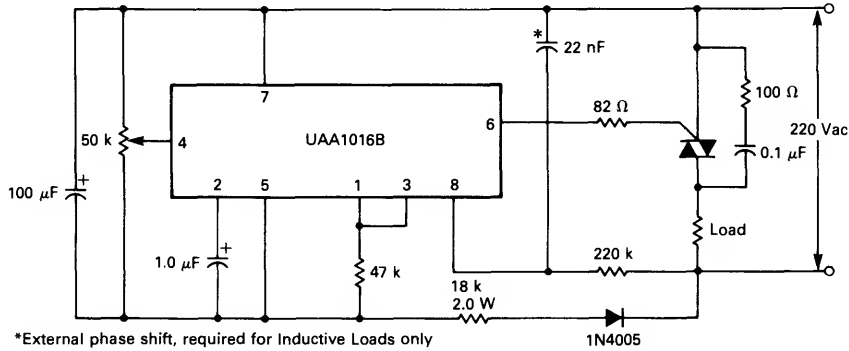
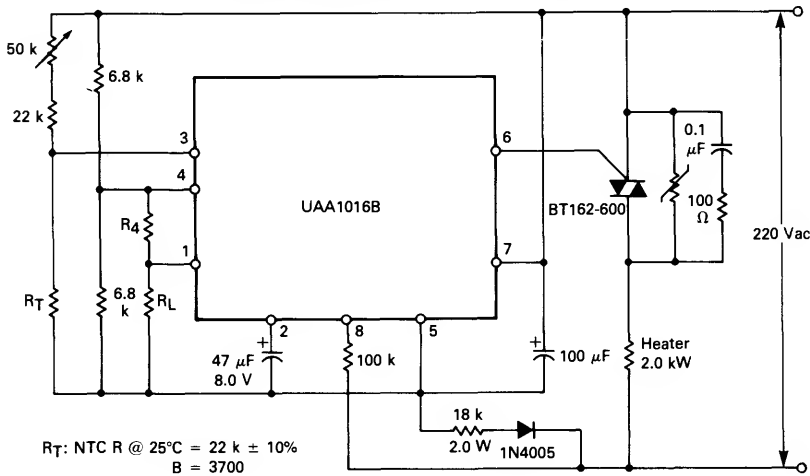


FIGURE 10 — APPLICATION CIRCUIT — ELECTRIC RADIATOR WITH PROPORTIONAL BAND THERMOSTAT, PROPORTIONAL BAND 1°C AT 25°C



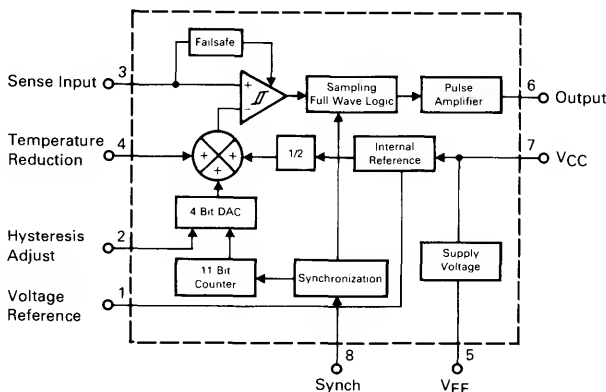
Product Preview

ZERO VOLTAGE SWITCH POWER CONTROLLER

The UAA2016 is designed to drive triacs with the Zero Voltage technique which allows RFI-free power regulation of resistive loads. Operating directly from the AC power line, its main application is the precision regulation of electrical heating systems (panel heaters, irons, etc. . .). A built-in digital sawtooth signal permits proportional temperature regulation about the set point. For energy savings, there is a programmable temperature reduction function, and for security, a sensor failsafe that inhibits output pulses when the sensor connection is broken. A preset temperature (i.e. defrost) application is also possible. In applications where high hysteresis is needed, its value can be adjusted around the set point. All of these features can be implemented with very few external components.

- Zero Voltage Switch for Triacs, Up to 2.0 kW (MAC212A8)
- Direct AC Line Operation
- Proportional Regulation of Temperature
- Programmable Temperature Reduction
- Preset Temperature (i.e. Defrost)
- Sensor Failsafe
- Adjustable Hysteresis
- Low External Component Count

REPRESENTATIVE BLOCK DIAGRAM

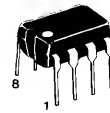


This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

UAA2016

ZERO VOLTAGE SWITCH POWER CONTROLLER

SILICON MONOLITHIC INTEGRATED CIRCUIT

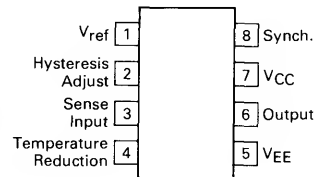


P SUFFIX
PLASTIC PACKAGE
CASE 626



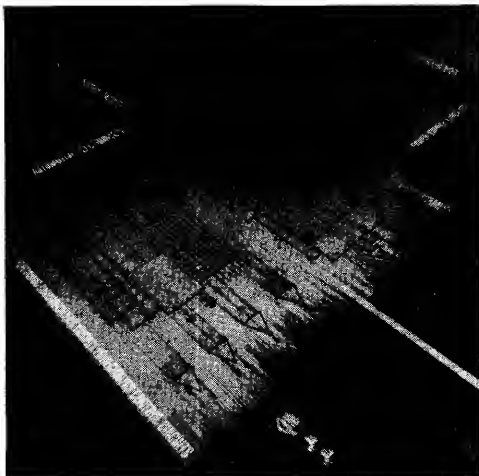
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
UAA2016D	- 20 to +85°C	SO-8
UAA2016P		Plastic DIP



In Brief . . .

Motorola's line of precision voltage references is designed for applications requiring high initial accuracy, low temperature drift, and long term stability. Initial accuracies of $\pm 1.0\%$, and $\pm 2.0\%$ mean production line adjustments can be eliminated. Temperature coefficients of 25 ppm/ $^{\circ}\text{C}$ max (typically 10 ppm/ $^{\circ}\text{C}$) provide excellent stability. Uses for the references include D/A converters, A/D converters, precision power supplies, voltmeter systems, temperature monitors, and others.

Voltage References

5

Selector Guide

Precision Low Voltage References	5-2
Alphanumeric Listing	5-3
Data Sheets	5-4

Voltage References

Precision Low Voltage References

A family of precision low voltage bandgap reference devices designed for applications requiring low temperature drift.

V _{out} Volts Typ	I _O mA Max	V _{out} /T ppm/°C Max	Device		Regline mV Max	Regload mV Max	Case				
			0 to +70°C	−55 to +125°C −40 to +85°C							
1.235 ± 12 mV 1.235 ± 25 mV	20	20 Typ	LM385BZ-1.2 LM385Z-1.2	LM285Z-1.2 (−40 to +85°C)	(Note 1)	1.0 (Note 2)	29				
2.5 ± 38 mV 2.5 ± 75 mV			LM385BZ-2.5 LM385Z-2.5	LM285Z-2.5 (−40 to +85°C)		2.0 (Note 3)					
2.5 ± 25 mV			10	25 40 55		MC1403A MC1403		MC1503	3.0/4.5 (Note 4)	10 (Note 6)	693, 751
5.0 ± 50 mV	10	25 40 55	MC1404AU5 MC1404U5		6.0 (Note 5)		693				
6.25 ± 60 mV		25 40 55	MC1404AU6 MC1404U6								
		25 40 55	MC1404AU10 MC1404U10								
		25 40 55		MC1504U5 MC1504U6 MC1504U10							
2.5 to 37		100	50 Typ	TL431C,AC				TL431I, Al (−40 to +85°C) TL431M	Shunt Reference Dynamic Impedance z ≤ 0.5 ohm		29,626 693
											693

Notes: 1. Micropower Reference Diode Dynamic Impedance (z) ≤ 1.0 Ω at I_R = 100 μA
2. 10 μA ≤ I_R ≤ 1.0 mA

3. 20 μA ≤ I_R ≤ 1.0 mA
4. 4.5 V ≤ V_{in} ≤ 15 V/15 V ≤ V_{in} ≤ 40 V

5. (V_{out} + 2.5 V) ≤ V_{in} ≤ 40 V
6. 0 mA ≤ I_L ≤ 10 mA

VOLTAGE REFERENCES

Device	Function	Page
LM285	Micropower Voltage Reference Diode	5-4
LM385	Micropower Voltage Reference Diode	5-4
MC1403,A	Precision Low Voltage Reference	5-8
MC1404,A	Precision Low Drift Voltage Reference	5-12
MC1503,A	Precision Low Voltage Reference	5-8
MC1504	Precision Low Drift Voltage Reference	5-12
TL431,A	Programmable Precision References	5-17

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

5

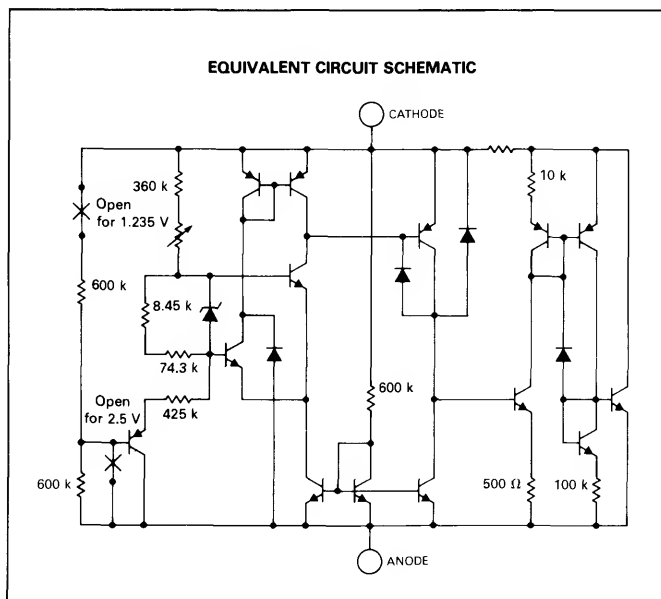
MICROPOWER VOLTAGE REFERENCE DIODES

The LM285/LM385 series are micropower two-terminal band-gap voltage regulator diodes. Designed to operate over a wide current range of 10 μ A to 20 mA, these devices feature exceptionally low dynamic impedance, low noise and stable operation over time and temperature. Tight voltage tolerances are achieved by on-chip trimming. The large dynamic operating range enables these devices to be used in applications with widely varying supplies with excellent regulation. Extremely low operating current make these devices ideal for micropower circuitry like portable instrumentation, regulators and other analog circuitry where extended battery life is required.

The LM285/LM385 series are packaged in a low cost TO-226AA plastic case and are available in two voltage versions of 1.235 and 2.500 volts as denoted by the device suffix (see ordering information table). The LM285 is specified over a -40°C to $+85^{\circ}\text{C}$ temperature range while the LM385 is rated from 0°C to $+70^{\circ}\text{C}$. The LM385 is also available in a surface mount plastic package in voltages of 1.235 and 2.500 volts.

- Operating Current from 10 μ A to 20 mA
- 1.0%, 1.5%, 2.0% and 3.0% Initial Tolerance Grades
- Low Temperature Coefficient
- 1.0 Ω Dynamic Impedance
- Surface Mount Package Available

EQUIVALENT CIRCUIT SCHEMATIC



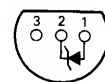
LM285 LM385

MICROPOWER VOLTAGE REFERENCE DIODES

SILICON MONOLITHIC INTEGRATED CIRCUIT

Z SUFFIX PLASTIC PACKAGE CASE 29

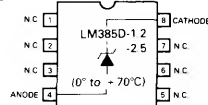
(Bottom View)



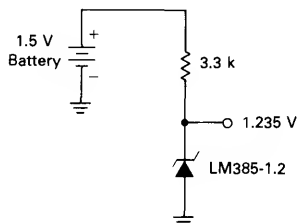
N.C. 3
CATHODE 2
ANODE 1



D SUFFIX PLASTIC PACKAGE CASE 751 (SO-8)



STANDARD APPLICATION



ORDERING INFORMATION

Device	Temp. Range	Reverse Break-down Voltage	Tolerance
LM285D-1.2	-40°C to $+85^{\circ}\text{C}$	1.235 Volts	$\pm 1.0\%$
LM285Z-1.2		1.235 Volts	$\pm 1.0\%$
LM285D-2.5	-40°C to $+85^{\circ}\text{C}$	2,500 Volts	$\pm 1.5\%$
LM285Z-2.5		2,500 Volts	$\pm 1.5\%$
LM385BD-1.2	0°C to $+70^{\circ}\text{C}$	1.235 Volts	$\pm 1.0\%$
LM385BZ-1.2		1.235 Volts	$\pm 1.0\%$
LM385D-1.2		1.235 Volts	$\pm 2.0\%$
LM385Z-1.2		1.235 Volts	$\pm 2.0\%$
LM385BD-2.5		2,500 Volts	$\pm 1.5\%$
LM385BZ-2.5		2,500 Volts	$\pm 1.5\%$
LM385D-2.5		2,500 Volts	$\pm 3.0\%$
LM385Z-2.5		2,500 Volts	$\pm 3.0\%$

LM285, LM385

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Reverse Current	I_R	30	mA
Forward Current	I_F	10	mA
Operating Ambient Temperature Range LM285 LM385	T_A	-40 to +85 0 to +70	$^\circ\text{C}$
Operating Junction Temperature	T_J	+150	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	LM285-1.2			LM385-1.2/LM385B-1.2			Unit
		Min	Typ	Max	Min	Typ	Max	
Reverse Breakdown Voltage $I_{Rmin} \leq I_R \leq 20 \text{ mA}$ LM285-1.2/LM385B-1.2 $T_A = T_{low} \text{ to } T_{high}$ (Note 1) LM385-1.2 $T_A = T_{low} \text{ to } T_{high}$ (Note 1)	$V_{(BR)R}$	1.223 1.200 — —	1.235 — — —	1.247 1.270 — —	1.223 1.210 1.205 1.192	1.235 — 1.235 —	1.247 1.260 1.260 1.273	V
Minimum Operating Current $T_A = 25^\circ\text{C}$ $T_A = T_{low} \text{ to } T_{high}$ (Note 1)	I_{Rmin}	— —	8.0 —	10 20	— —	8.0 —	15 20	μA
Reverse Breakdown Voltage Change with Current $I_{Rmin} \leq I_R \leq 1.0 \text{ mA}$, $T_A = +25^\circ\text{C}$ $T_A = T_{low} \text{ to } T_{high}$ (Note 1) $1.0 \text{ mA} \leq I_R \leq 20 \text{ mA}$, $T_A = +25^\circ\text{C}$ $T_A = T_{low} \text{ to } T_{high}$ (Note 1)	$\Delta V_{(BR)R}$	— — — —	— — — —	1.0 1.5 10 20	— — — —	— — — —	1.0 1.5 20 25	mV
Reverse Dynamic Impedance $I_R = 100 \mu\text{A}$, $T_A = +25^\circ\text{C}$	Z	—	0.6	—	—	0.6	—	Ω
Average Temperature Coefficient $10 \mu\text{A} \leq I_R \leq 20 \text{ mA}$, $T_A = T_{low} \text{ to } T_{high}$ (Note 1)	$\Delta V_{(BR)}/\Delta T$	—	80	—	—	80	—	ppm/ $^\circ\text{C}$
Wideband Noise (RMS) $I_R = 100 \mu\text{A}$, $10 \text{ Hz} \leq f \leq 10 \text{ kHz}$	n	—	60	—	—	60	—	μV
Long Term Stability $I_R = 100 \mu\text{A}$, $T_A = +25^\circ\text{C} \pm 0.1^\circ\text{C}$	S	—	20	—	—	20	—	ppm/ kHR

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	LM285-2.5			LM385-2.5/LM385B-2.5			Unit
		Min	Typ	Max	Min	Typ	Max	
Reverse Breakdown Voltage $I_{Rmin} \leq I_R \leq 20 \text{ mA}$ LM285-2.5/LM385B-2.5 $T_A = T_{low} \text{ to } T_{high}$ (Note 1) LM385-2.5 $T_A = T_{low} \text{ to } T_{high}$ (Note 1)	$V_{(BR)R}$	2.462 2.415 — —	2.5 — — —	2.538 2.585 — —	2.462 2.436 2.425 2.400	2.5 — 2.5 —	2.538 2.564 2.575 2.600	V
Minimum Operating Current $T_A = 25^\circ\text{C}$ $T_A = T_{low} \text{ to } T_{high}$ (Note 1)	I_{Rmin}	— —	13 —	20 30	— —	13 —	20 30	μA
Reverse Breakdown Voltage Change with Current $I_{Rmin} \leq I_R \leq 1.0 \text{ mA}$, $T_A = +25^\circ\text{C}$ $T_A = T_{low} \text{ to } T_{high}$ (Note 1) $1.0 \text{ mA} \leq I_R \leq 20 \text{ mA}$, $T_A = +25^\circ\text{C}$ $T_A = T_{low} \text{ to } T_{high}$ (Note 1)	$\Delta V_{(BR)R}$	— — — —	— — — —	1.0 1.5 10 20	— — — —	— — — —	2.0 2.5 20 25	mV
Reverse Dynamic Impedance $I_R = 100 \mu\text{A}$, $T_A = +25^\circ\text{C}$	Z	—	0.6	—	—	0.6	—	Ω
Average Temperature Coefficient $20 \mu\text{A} \leq I_R \leq 20 \text{ mA}$, $T_A = T_{low} \text{ to } T_{high}$ (Note 1)	$\Delta V_{(BR)}/\Delta T$	—	80	—	—	80	—	ppm/ $^\circ\text{C}$
Wideband Noise (RMS) $I_R = 100 \mu\text{A}$, $10 \text{ Hz} \leq f \leq 10 \text{ kHz}$	n	—	120	—	—	120	—	μV
Long Term Stability $I_R = 100 \mu\text{A}$, $T_A = +25^\circ\text{C} \pm 0.1^\circ\text{C}$	S	—	20	—	—	20	—	ppm/ kHR

Note: 1. $T_{low} = -40^\circ\text{C}$ for LM285-1.2, LM285-2.5

= 0°C for LM385-1.2, LM385B-1.2, LM385-2.5, LM385B-2.5

$T_{high} = +85^\circ\text{C}$ for LM285-1.2, LM285-2.5

= $+70^\circ\text{C}$ for LM385-1.2, LM385B-1.2, LM385-2.5, LM385B-2.5

LM285, LM385

TYPICAL PERFORMANCE CURVES FOR LM285-1.2/385-1.2/385B-1.2

FIGURE 1 — REVERSE CHARACTERISTICS

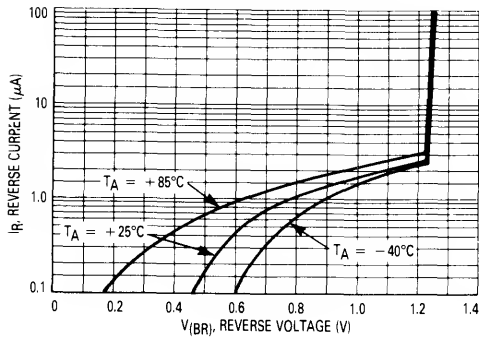


FIGURE 2 — REVERSE CHARACTERISTICS

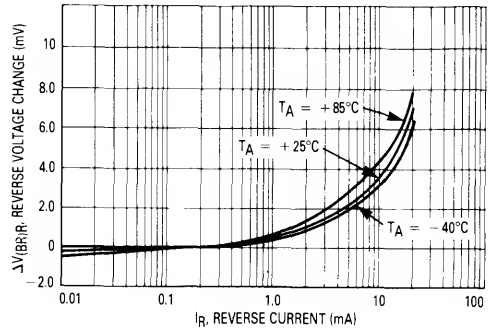


FIGURE 3 — FORWARD CHARACTERISTICS

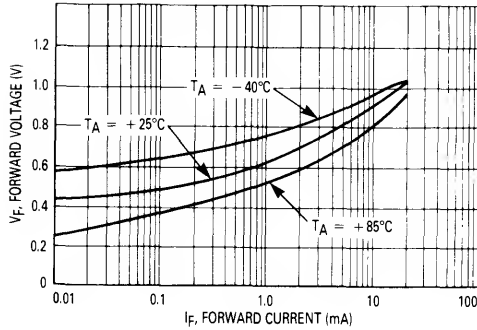


FIGURE 4 — TEMPERATURE DRIFT

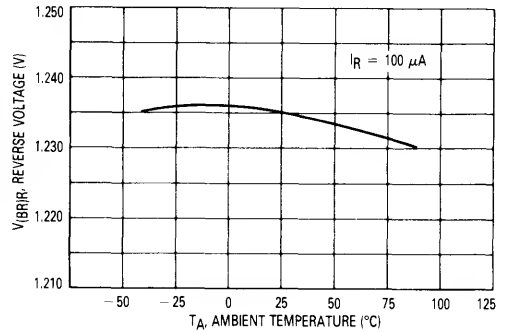


FIGURE 5 — NOISE VOLTAGE

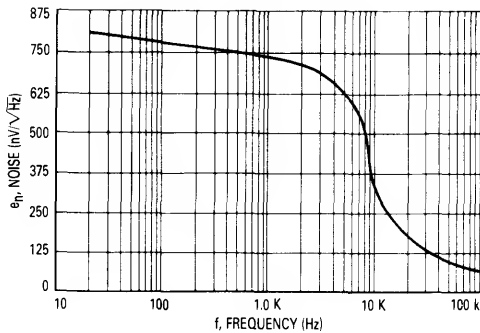
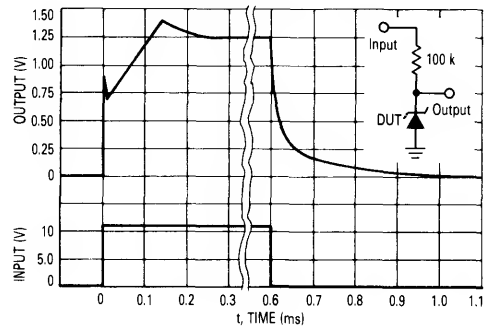


FIGURE 6 — RESPONSE TIME



LM285, LM385

TYPICAL PERFORMANCE CURVES FOR LM285-2.5/385-2.5/385B-2.5

FIGURE 7 — REVERSE CHARACTERISTICS

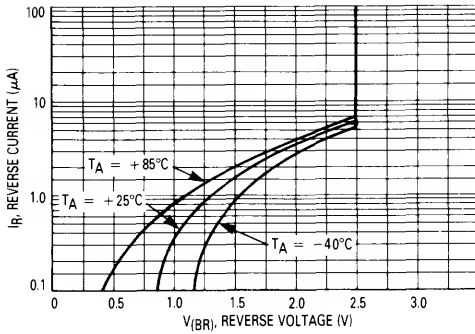


FIGURE 8 — REVERSE CHARACTERISTICS

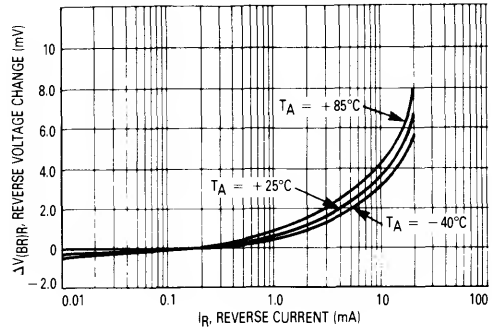


FIGURE 9 — FORWARD CHARACTERISTICS

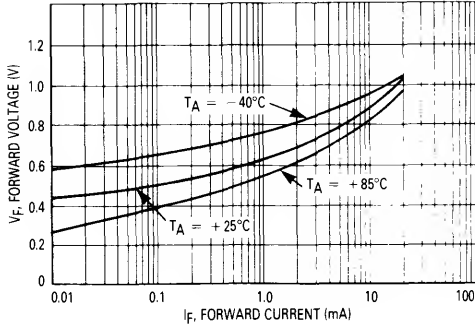


FIGURE 10 — TEMPERATURE DRIFT

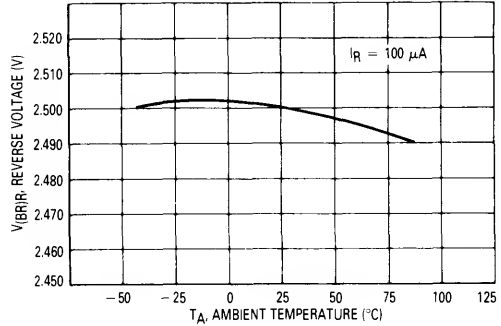


FIGURE 11 — NOISE VOLTAGE

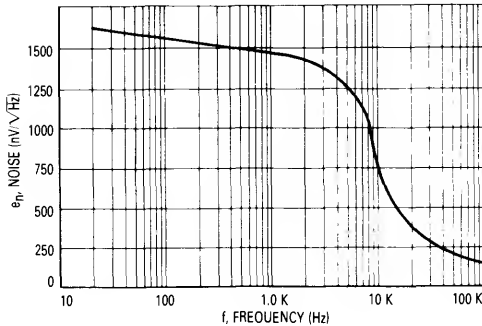
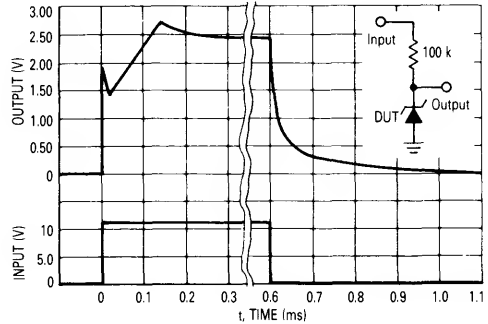


FIGURE 12 — RESPONSE TIME



MC1403,A
MC1503

LOW VOLTAGE REFERENCE

A precision band-gap voltage reference designed for critical instrumentation and D/A converter applications. This unit is designed to work with Motorola MC1508 and MC3510 D/A converters, and MC14433 A/D systems. Low temperature drift is a prime design consideration.

- Output Voltage: $2.5 \text{ V} \pm 25 \text{ mV}$
- Input Voltage Range: 4.5 V to 40 V
- Quiescent Current: 1.2 mA Typ
- Output Current: 10 mA
- Temperature Coefficient: $10 \text{ ppm}/^\circ\text{C Typ}$
- Guaranteed Temperature Drift Specification
- Equivalent to AD580
- Standard 8-Pin DIP, and 8-Pin SOIC Package

Typical Applications

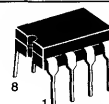
- Voltage Reference for 8–12 Bit D/A Converters
- Low T_C Zener Replacement
- High Stability Current Reference
- Voltmeter System Reference

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage	V_I	40	V
Storage Temperature	T_{stg}	-65 to 150	$^\circ\text{C}$
Junction Temperature	T_J	+175	$^\circ\text{C}$
Operating Ambient Temperature Range	T_A	-55 to +125	$^\circ\text{C}$
MC1503		0 to +70	$^\circ\text{C}$
MC1403,A			

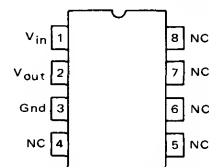
PRECISION LOW VOLTAGE REFERENCE

**LASER TRIMMED
 SILICON MONOLITHIC
 INTEGRATED CIRCUIT**



U SUFFIX
 CERAMIC PACKAGE
 CASE 693

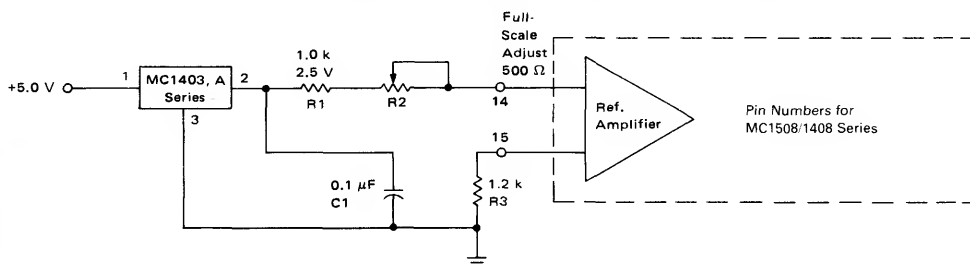
D SUFFIX
 PLASTIC PACKAGE
 CASE 751
 (SO-8)



ORDERING INFORMATION

Device	Temperature Range	Package
MC1503U	-55 to +125 $^\circ\text{C}$	Ceramic DIP
MC1403D		SO-8
MC1403U	0 to +70 $^\circ\text{C}$	Ceramic DIP
MC1403AU		Ceramic DIP

FIGURE 1 – A REFERENCE FOR MOTOROLA MONOLITHIC D/A CONVERTERS



**PROVIDING THE REFERENCE CURRENT
 FOR MOTOROLA MONOLITHIC D/A CONVERTERS**

The MC1403/1503 makes an ideal reference for the Motorola monolithic D/A converters. The MC1408/1508 converter requires a stable current reference of nominally 2.0 mA . This can be easily obtained from the MC1403/1503 with the addition of a series resistor, R_1 . A variable resistor, R_2 , is recommended to provide means for full-scale adjust on the D/A converter.

The resistor R_3 improves temperature performance by matching the impedance on both inputs of the D/A reference amplifier. The capacitor decouples any noise present on the reference line. It is essential if the D/A converter is located any appreciable distance from the reference.

A single MC1403/1503 reference can provide the required current input for up to five of the monolithic D/A converters.

MC1403,A, MC1503

ELECTRICAL CHARACTERISTICS ($V_{in} = 15\text{ V}$, $T_A = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($I_O = 0\text{ mA}$)	V_{OUT}	2.475	2.5	2.525	V
Temperature Coefficient of Output Voltage MC1503 MC1403* MC1403A	$\Delta V_O/\Delta T$	— — —	— 10 10	55 40 25	ppm/ $^\circ\text{C}$
Output Voltage Change (over specified temperature range) MC1503 -55°C to $+125^\circ\text{C}$ MC1403* 0°C to $+70^\circ\text{C}$ MC1403A	ΔV_O	— — —	— — —	25 7.0 4.4	mV
Line Regulation ($I_O = 0\text{ mA}$) ($15\text{ V} \leq V_I \leq 40\text{ V}$) ($4.5\text{ V} \leq V_I \leq 15\text{ V}$)	Reg_{line}	— —	1.2 0.6	4.5 3.0	mV
Load Regulation ($0\text{ mA} < I_O < 10\text{ mA}$)	Reg_{load}	—	—	10	mV
Quiescent Current ($I_O = 0\text{ mA}$)	I_Q	—	1.2	1.5	mA

*This test is not applicable to the MC1403D surface mount device.

5

FIGURE 2 — MC1403/1503 SCHEMATIC

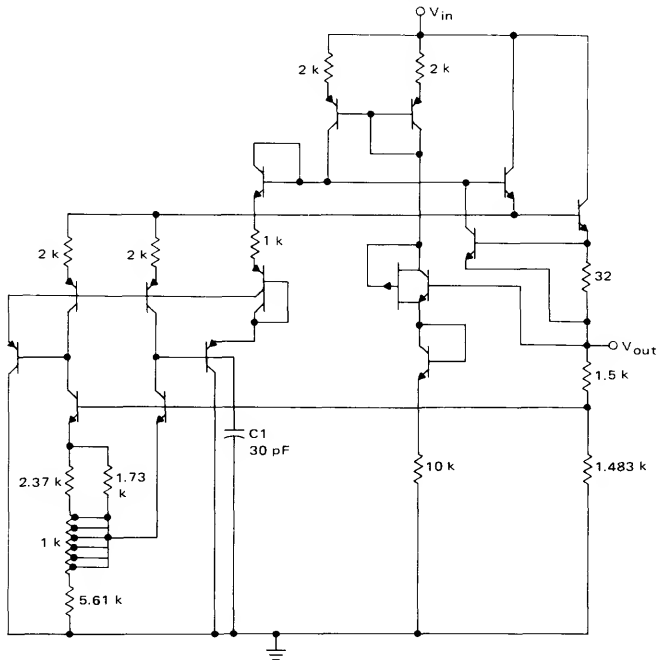


FIGURE 3 – TYPICAL CHANGE IN V_{out} versus V_{in}
(NORMALIZED TO $V_{in} = 15\text{ V}$ @ $T_C = 25^\circ\text{C}$)

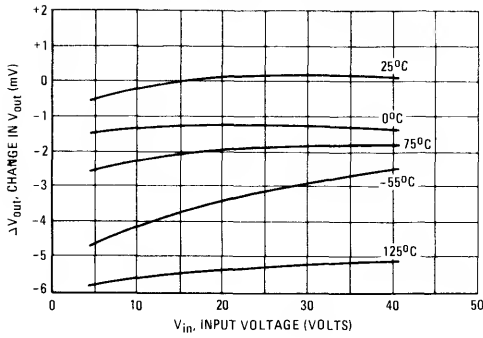


FIGURE 4 – CHANGE IN OUTPUT VOLTAGE
versus LOAD CURRENT
(NORMALIZED TO V_{out} @ $V_{in} = 15\text{ V}$, $I_{out} = 0\text{ mA}$)

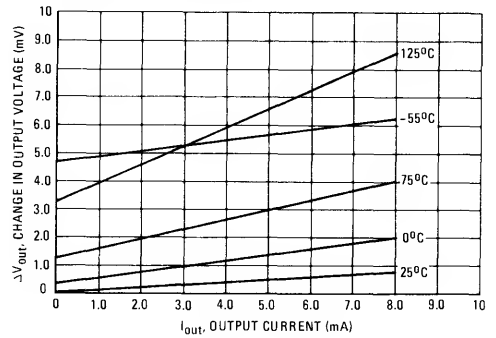


FIGURE 5 – QUIESCENT CURRENT versus TEMPERATURE
($V_{in} = 15\text{ V}$, $I_{out} = 0\text{ mA}$)

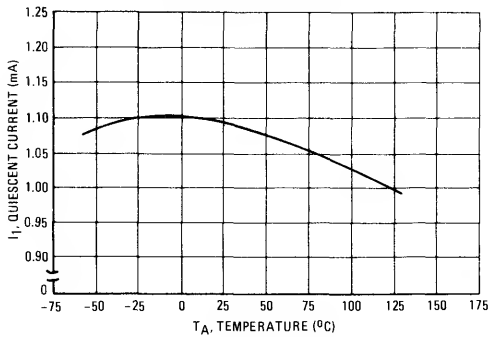


FIGURE 6 – CHANGE IN V_{out} versus TEMPERATURE
(NORMALIZED TO V_{out} @ $V_{in} = 15\text{ V}$)

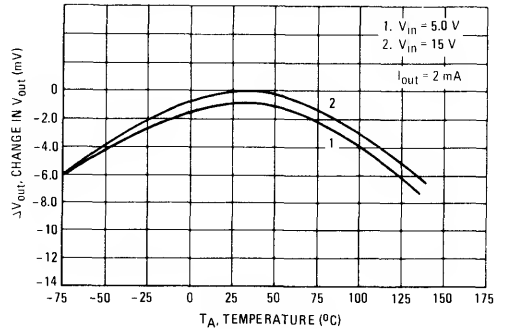
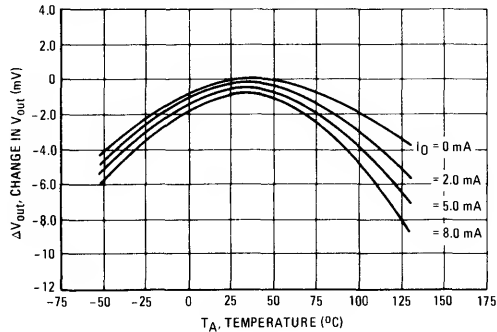


FIGURE 7 – CHANGE IN V_{out} versus TEMPERATURE
(NORMALIZED TO $T_A = I_0$, $V_{in} = 15\text{ V}$, $I_{out} = 0\text{ mA}$)



MC1403,A, MC1503

3-1/2-DIGIT VOLTMETER — COMMON ANODE DISPLAYS, FLASHING OVERRANGE

An example of a 3-1/2-digit voltmeter using the MC14433 is shown in the circuit diagram of Figure 8. The reference voltage for the system uses an MC1403 2.5 V reference IC. The full scale potentiometer can calibrate for a full scale of 199.9 mV or 1.999 V. When switching from 2 V to 200 mV operation, R_1 is also changed, as shown on the diagram.

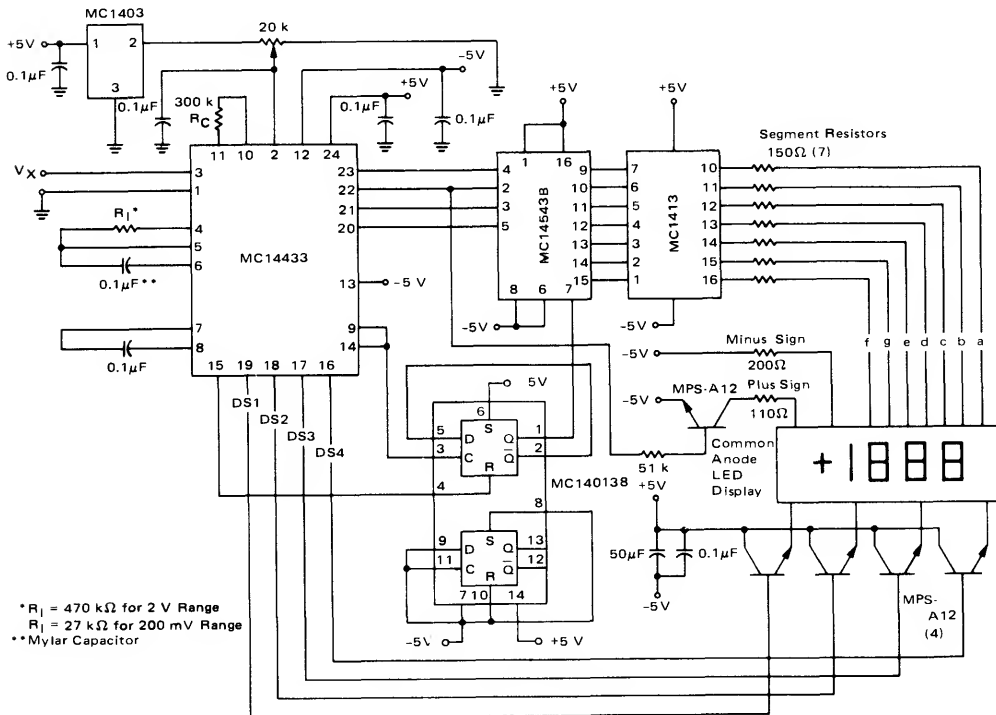
When using R_C equal to 300 k Ω , the clock frequency for the system is about 66 kHz. The resulting conversion time is approximately 250 ms.

When the input is overrange, the display flashes on and off. The flashing rate is one-half the conversion rate.

This is done by dividing the EOC pulse rate by 2 with 1/2 MC14013B flip-flop and blanking the display using the blanking input of the MC14543B.

The display uses an LED display with common anode digit lines driven with an MC14543B decoder and an MC1413 LED driver. The MC1413 contains 7 Darlington transistor drivers and resistors to drive the segments of the display. The digit drive is provided by four MPS-A12 Darlington transistors operating in an emitter-follower configuration. The MC14543B, MC14013B and LED displays are referenced to VEE via pin 13 of the MC14433. This places the full power supply voltage across the display. The current for the display may be adjusted by the value of the segment resistors shown as 150 ohms in Figure 8.

FIGURE 8 — 3-1/2-DIGIT VOLTMETER



VOLTAGE REFERENCE FAMILY

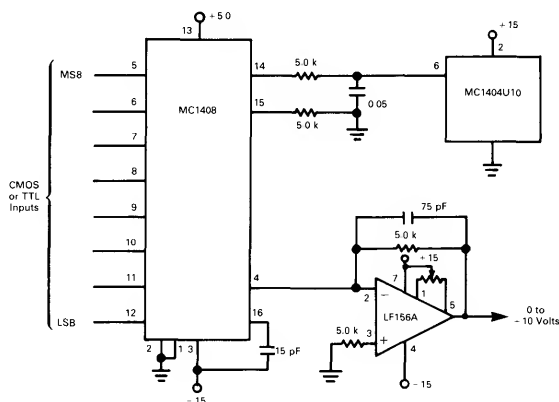
The MC1404 series of ICs is a family of temperature-compensated voltage references for precision data conversion applications, such as A/D, D/A, V/F, and F/V. Advances in laser-trimming and ion-implanted devices, as well as monolithic fabrication techniques, make these devices stable and accurate to 12 bits over both military and commercial temperature ranges. In addition to excellent temperature stability, these parts offer excellent long-term stability and low noise.

- Output Voltages: Standard, 5.0 V, 6.25 V, 10 V
- Trimmable Output: $> \pm 6\%$
- Wide Input Voltage Range: $V_{ref} + 2.5 \text{ V}$ to 40 V
- Low Quiescent Current: 1.25 mA Typical
- Temperature Coefficient: 10 ppm/°C Typical
- Low Output Noise: 12 μV p-p Typical
- Excellent Ripple Rejection: $> 80 \text{ dB}$ Typical

TYPICAL APPLICATIONS

- Voltage Reference for 8 – 12 Bit D/A Converters
- Low T_C Zener Replacement
- High Stability Current Reference
- MPU D/A and A/D Applications

FIGURE 1 — VOLTAGE OUTPUT 8-BIT DAC USING MC1404U10

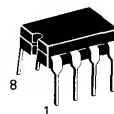


MC1404 MC1404A MC1504

PRECISION LOW DRIFT VOLTAGE REFERENCES

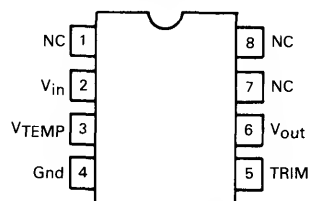
5.0, 6.25, and 10-VOLT OUTPUT VOLTAGES

LASER TRIMMED SILICON
MONOLITHIC INTEGRATED CIRCUIT



U SUFFIX
CERAMIC PACKAGE
CASE 693

PIN ASSIGNMENTS



ORDERING INFORMATION

PACKAGE Ceramic DIP

Device	Temperature Range
5.0 Volts	
MC1504U5	-55°C to $+125^{\circ}\text{C}$
MC1404U5	0°C to $+70^{\circ}\text{C}$
MC1404AU5	0°C to $+70^{\circ}\text{C}$
6.25 Volts	
MC1504U6	-55°C to $+125^{\circ}\text{C}$
MC1404U6	0°C to $+70^{\circ}\text{C}$
MC1404AU6	0°C to $+70^{\circ}\text{C}$
10 Volts	
MC1504U10	-55°C to $+125^{\circ}\text{C}$
MC1404U10	0°C to $+70^{\circ}\text{C}$
MC1404AU10	0°C to $+70^{\circ}\text{C}$

MC1404,A, MC1504

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	V_{in}	40	V
Storage Temperature	T_{stg}	- 65 to + 150	°C
Junction Temperature	T_J	+ 175	°C
Operating Ambient Temperature Range MC1504 MC1404,A	T_A	- 55 to + 125 0 to + 70	°C

ELECTRICAL CHARACTERISTICS ($V_{in} = 15$ Volts, $T_A = 25^\circ\text{C}$ and Trim Terminal not connected unless otherwise noted)

Characteristic	Symbol	MC1404,A			MC1504			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($I_O = 0$ mA) MC1404U5, AU5/MC1504U5 MC1404U6, AU6/MC1504U6 MC1404U10, AU10/MC1504U10	V_O	4.95 6.19 9.9	5.0 6.25 10	5.05 6.31 10.1	4.95 6.19 9.9	5.0 6.25 10	5.05 6.31 10.1	Volt
Output Voltage Tolerance	—	—	± 0.1	± 1.0	—	± 0.1	± 1.0	%
Output Trim Range (Figure 10) ($R_p = 100$ k Ω)	ΔV_{TRIM}	± 6.0	—	—	± 6.0	—	—	%
Output Voltage Temperature Coefficient, Over Full Temperature Range MC1404, MC1504 MC1404A	$\Delta V_O/\Delta T$	— —	10 10	40 25	— —	— —	55 —	ppm/°C
Maximum Output Voltage Change Over Temperature Range MC1404U5, MC1504U5 MC1404AU5 MC1404U6, MC1504U6 MC1404AU6 MC1404U10, MC1504U10 MC1404AU10	ΔV_O	— — — — — —	— — — — — —	14 9.0 17.5 11 28 18	— — — — — —	— — — — — —	50 — 62 — 99 —	mV
Line Regulation (1) ($V_{in} = V_{out} + 2.5$ V to 40 V, $I_{out} = 0$ mA)	Reg _{line}	—	2.0	6.0	—	2.0	6.0	mV
Load Regulation (1) ($0 \leq I_O \leq 10$ mA)	Reg _{load}	—	—	10	—	—	10	mV
Quiescent Current ($I_O = 0$ mA)	I_O	—	1.2	1.5	—	1.2	1.5	mA
Short Circuit Current	I_{sc}	—	20	45	—	—	45	mA
Long Term Stability	—	—	25	—	—	25	—	ppm/1000 hrs

Note 1: Includes thermal effects.

DYNAMIC CHARACTERISTICS ($V_{in} = 15$ V, $T_A = 25^\circ\text{C}$ all voltage ranges unless otherwise noted)

Characteristic	Symbol	MC1404,A			MC1504			Unit
		Min	Typ	Max	Min	Typ	Max	
Turn-On Settling Time (to $\pm 0.01\%$)	t_S	—	50	—	—	50	—	μs
Output Noise Voltage — P to P (Bandwidth 0.1 to 10 Hz)	V_n	—	12	—	—	12	—	μV
Small-Signal Output Impedance 120 Hz 500 Hz	r_o	— —	0.15 0.2	— —	— —	0.15 0.2	— —	Ω
Power Supply Rejection Ratio	PSRR	70	80	—	70	80	—	dB

5

TYPICAL CHARACTERISTICS

FIGURE 2 – SIMPLIFIED DEVICE DIAGRAM

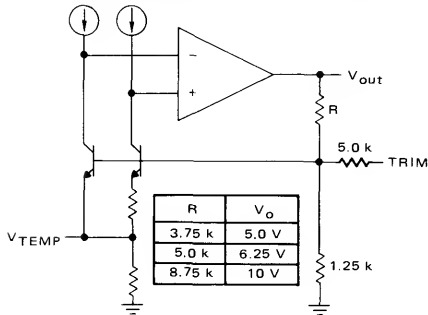


FIGURE 3 – LINE REGULATION versus TEMPERATURE

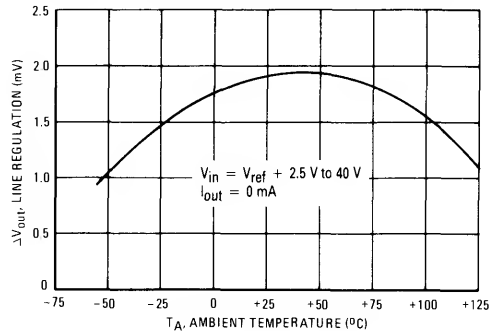


FIGURE 4 – OUTPUT VOLTAGE versus TEMPERATURE
MC1404U10

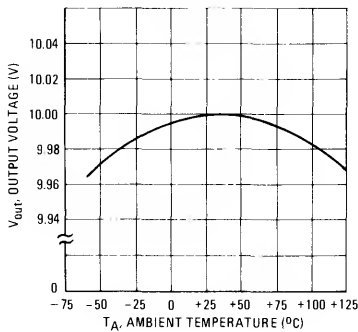


FIGURE 5 – LOAD REGULATION versus TEMPERATURE

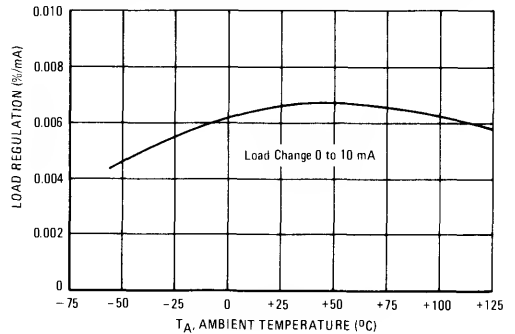


FIGURE 6 – POWER SUPPLY REJECTION RATIO
versus FREQUENCY

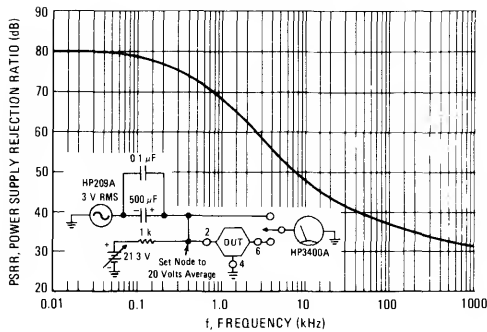
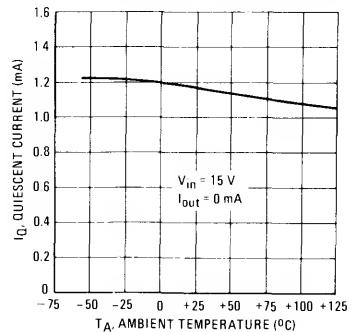


FIGURE 7 – QUIESCENT CURRENT versus TEMPERATURE



MC1404,A, MC1504

FIGURE 8 – SHORT CIRCUIT CURRENT versus TEMPERATURE

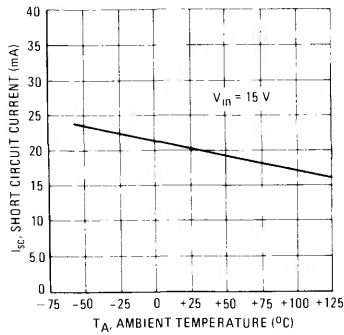


FIGURE 9 – V_{TEMP} OUTPUT versus TEMPERATURE

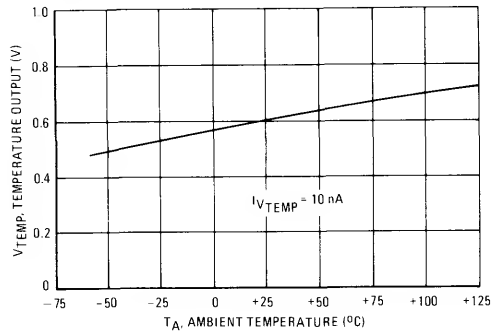
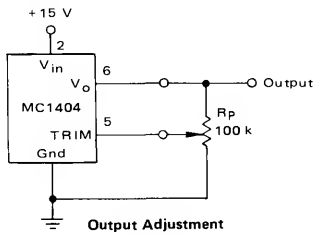


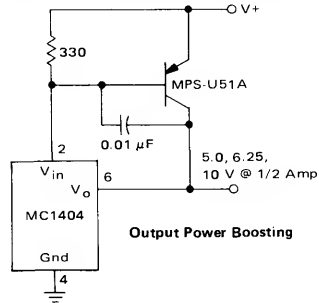
FIGURE 10 – OUTPUT TRIM CONFIGURATION



The MC1404 trim terminal can be used to adjust the output voltage over a $\pm 6\%$ range. For example, the output can be set to 10.000 V or to 10.240 V for binary applications. For trimming, Bourns type 3059, 100 k Ω or 200 k Ω trimpot is recommended.

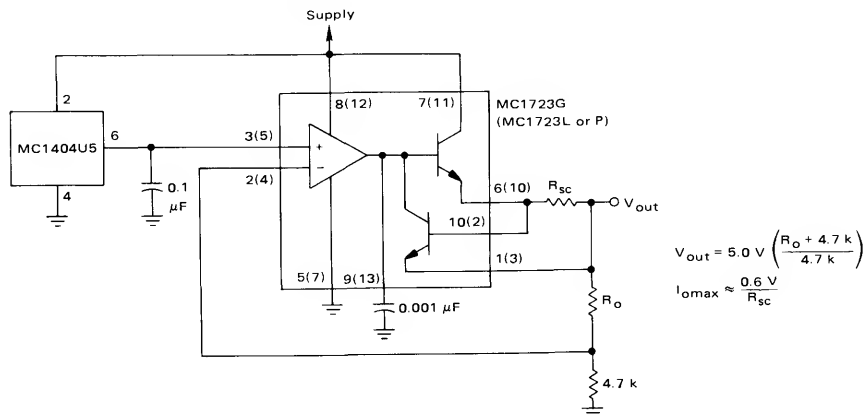
Although Figure 10 illustrates a wide trim range, temperature coefficients may become unpredictable for trim $> \pm 6.0\%$.

FIGURE 11 – PRECISION SUPPLY USING MC1404



The addition of a power transistor, a resistor, and a capacitor converts the MC1404 into a precision supply with one ampere current capability. At $V^+ = 15$ V, the MC1404 can carry in excess of 14 mA of load current with good regulation. If the power transistor current gain exceeds 75, a one ampere supply can be realized.

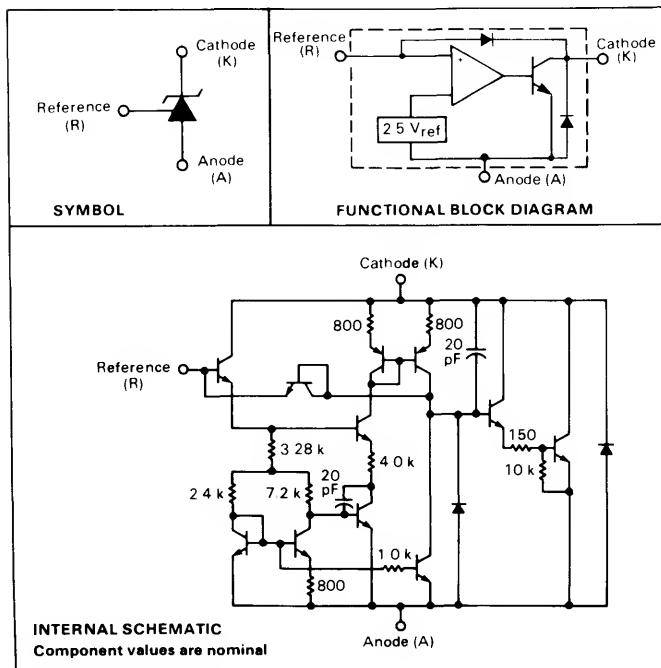
FIGURE 12 – ULTRA STABLE REFERENCE FOR MC1723 VOLTAGE REGULATOR



PROGRAMMABLE PRECISION REFERENCES

The TL431A integrated circuits are three-terminal programmable shunt regulator diodes. These monolithic IC voltage references operate as a low temperature coefficient zener which is programmable from V_{ref} to 36 volts with two external resistors. These devices exhibit a wide operating current range of 1.0 to 100 mA with a typical dynamic impedance of 0.22 Ω . The characteristics of these references make them excellent replacements for zener diodes in many applications such as digital voltmeters, power supplies, and op amp circuitry. The 2.5 volt reference makes it convenient to obtain a stable reference from 5.0 volt logic supplies, and since the TL431A operates as a shunt regulator, it can be used as either a positive or negative voltage reference.

- Programmable Output Voltage to 36 Volts
- Voltage Reference Tolerance: $\pm 1.0\%$ (TL431A)
- Low Dynamic Output Impedance, 0.22 Ω Typical
- Sink Current Capability of 1.0 to 100 mA
- Equivalent Full-Range Temperature Coefficient of 50 ppm/°C Typical
- Temperature Compensated for Operation over Full Rated Operating Temperature Range
- Low Output Noise Voltage



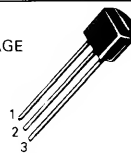
TL431A Series

PROGRAMMABLE PRECISION REFERENCES

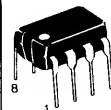
SILICON MONOLITHIC INTEGRATED CIRCUITS

LP SUFFIX PLASTIC PACKAGE CASE 29

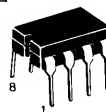
Pin 1 Reference
 2 Anode
 3 Cathode



P SUFFIX PLASTIC PACKAGE CASE 626



(Top View)
 Cathode 1, 2, 3, 4
 Reference 8
 N.C. 7, 6, 5
 Anode



JG SUFFIX CERAMIC PACKAGE CASE 693



**D SUFFIX
PLASTIC PACKAGE
CASE 751
(SOP-8)**
 PIN 1 CATHODE 5. N.C.
 2 ANODE 6. ANODE
 3 ANODE 7. ANODE
 4 N.C. 8. REFERENCE

SOP-8 is an internally modified SO-8 Package. Pins 2, 3, 6 and 7 are electrically common to the die attach flag. This internal lead frame modification decreases package thermal resistance and increases power dissipation capability when appropriately mounted on a printed circuit board. SOP-8 conforms to all external dimensions of the standard SO-8 Package.

ORDERING INFORMATION

Device	Temperature Range	Package
TL431CLP,ACLP	0 to +70°C	Plastic TO-92
TL431CP,ACP		Plastic DIP
TL431CD,ACD		SOP-8
TL431CJG		Ceramic DIP
TL431ILP,AILP	-40 to +85°C	Plastic TO-92
TL431IP,AIP		Plastic DIP
TL531IJG	-55 to +125°C	Ceramic DIP
TL431MJG		Ceramic DIP

TL431,A Series

MAXIMUM RATINGS (Full operating ambient temperature range applies unless otherwise noted.)

Rating	Symbol	Value	Unit
Cathode To Anode Voltage	V_{KA}	37	V
Cathode Current Range, Continuous	I_K	-100 to +150	mA
Reference Input Current Range, Continuous	I_{ref}	-0.05 to +10	mA
Operating Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range TL431M TL431I, TL431AI TL431C, TL431AC	T_A	-55 to +125 -40 to +85 0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Total Power Dissipation (at $T_A = 25^\circ\text{C}$ Derate above 25°C Ambient Temperature D, LP Suffix Plastic Package P Suffix Plastic Package JG Suffix Ceramic Package	P_D	0.70 1.10 1.25	W
Total Power Dissipation (at $T_C = 25^\circ\text{C}$ Derate above 25°C Case Temperature D, LP Suffix Plastic Package P Suffix Plastic Package JG Suffix Ceramic Package	P_D	1.5 3.0 3.3	W

THERMAL CHARACTERISTICS

Characteristics	Symbol	D, LP Suffix Package	P Suffix Package	JG Suffix package	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	178	114	100	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83	41	38	°C/W

RECOMMENDED OPERATING CONDITIONS

Condition/Value	Symbol	Min	Max	Unit
Cathode To Anode Voltage	V_{KA}	V_{ref}	36	V
Cathode Current	I_K	1.0	100	mA

ELECTRICAL CHARACTERISTICS (Ambient temperature at 25°C unless otherwise noted)

Characteristic	Symbol	TL431M			TL431I			TL431C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reference Input Voltage (Figure 1) $V_{KA} = V_{ref}$, $I_K = 10\text{ mA}$ $T_A = +25^\circ\text{C}$ $T_A = T_{low}$ to T_{high} (Note 1)	V_{ref}	2.440 2.396	2.495 —	2.550 2.594	2.440 2.410	2.495 —	2.550 2.580	2.440 2.423	2.495 —	2.550 2.567	V
Reference Input Voltage Deviation Over Temperature Range (Figure 1, Note 1, 2, 4) $V_{KA} = V_{ref}$, $I_K = 10\text{ mA}$	ΔV_{ref}	—	15	44	—	7.0	30	—	3.0	17	mV
Ratio of Change in Reference Input Voltage to Change in Cathode to Anode Voltage $I_K = 10\text{ mA}$ (Figure 2), $\Delta V_{KA} = 10\text{ V}$ to V_{ref} $\Delta V_{KA} = 36\text{ V}$ to 10 V	$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	—	-1.4 -1.0	-2.7 -2.0	—	-1.4 -1.0	-2.7 -2.0	—	-1.4 -1.0	-2.7 -2.0	mV/V
Reference Input Current (Figure 2) $I_K = 10\text{ mA}$, $R_1 = 10\text{ k}$, $R_2 = \infty$ $T_A = +25^\circ\text{C}$ $T_A = T_{low}$ to T_{high} (Note 1)	I_{ref}	—	1.8 —	4.0 7.0	—	1.8 —	4.0 6.5	—	1.8 —	4.0 5.2	μA
Reference Input Current Deviation Over Temperature Range (Figure 2, Note 1, 4) $I_K = 10\text{ mA}$, $R_1 = 10\text{ k}$, $R_2 = \infty$	ΔI_{ref}	—	1.0	3.0	—	0.8	2.5	—	0.4	1.2	μA
Minimum Cathode Current For Regulation $V_{KA} = V_{ref}$ (Figure 1)	I_{min}	—	0.5	1.0	—	0.5	1.0	—	0.5	1.0	mA
Off-State Cathode Current (Figure 3) $V_{KA} = 36\text{ V}$, $V_{ref} = 0\text{ V}$	I_{off}	—	2.6	1000	—	2.6	1000	—	2.6	1000	nA
Dynamic Impedance (Figure 1, Note 3) $V_{KA} = V_{ref}$, $\Delta I_K = 1.0\text{ mA}$ to 100 mA $f \leq 1.0\text{ kHz}$	Z_{ka}	—	0.22	0.5	—	0.22	0.5	—	0.22	0.5	Ω

TL431,A Series

ELECTRICAL CHARACTERISTICS (Ambient temperature at 25°C unless otherwise noted)

Characteristic	Symbol	TL431AI			TL431AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Reference Input Voltage (Figure 1) $V_{KA} = V_{ref}$, $I_K = 10$ mA $T_A = +25^\circ\text{C}$ $T_A = T_{low}$ to T_{high}	V_{ref}	2.47 2.44	2.495 —	2.52 2.55	2.47 2.453	2.495 —	2.52 2.537	V
Reference Input Voltage Deviation Over Temperature Range (Figure 1, Notes 1, 2, 4) $V_{KA} = V_{ref}$, $I_K = 10$ mA	ΔV_{ref}	—	7.0	30	—	3.0	17	mV
Ratio of Change in Reference Input Voltage to Change in Cathode to Anode Voltage $I_K = 10$ mA (Figure 2), $\Delta V_{KA} = 10$ V to V_{ref} $\Delta V_{KA} = 36$ V to 10 V	$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	— —	-1.4 -1.0	-2.7 -2.0	— —	-1.4 -1.0	-2.7 -2.0	mV/V
Reference Input Current (Figure 2) $I_K = 10$ mA, $R_1 = 10$ k, $R_2 = \infty$ $T_A = +25^\circ\text{C}$ $T_A = T_{low}$ to T_{high} (Note 1)	I_{ref}	— —	1.8 —	4.0 6.5	— —	1.8 —	4.0 5.2	μA
Reference Input Current Deviation Over Temperature Range (Figure 2, Notes 1 and 4) $I_K = 10$ mA, $R_1 = 10$ k, $R_2 = \infty$	ΔI_{ref}	—	0.8	2.5	—	0.4	1.2	μA
Minimum Cathode Current For Regulation $V_{KA} = V_{ref}$ (Figure 1)	I_{min}	—	0.5	1.0	—	0.5	1.0	mA
Off-State Cathode Current (Figure 3) $V_{KA} = 36$ V, $V_{ref} = 0$ V	I_{off}	—	2.6	1000	—	2.6	1000	nA
Dynamic Impedance (Figure 1, Note 3) $V_{KA} = V_{ref}$, $\Delta I_K = 1.0$ mA to 100 mA $f \leq 1.0$ kHz	Z_{ka}	—	0.22	0.5	—	0.22	0.5	Ω

Note 1:

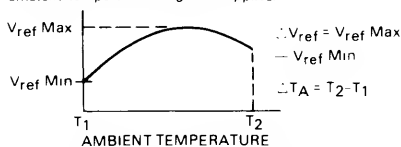
- $T_{low} = -55^\circ\text{C}$ for TL431MJG
- -40°C for TL431AIP, TL431AILP, TL431IP, TL431ILP, TL431JG
- 0°C for TL431ACP, TL431ACLP, TL431CP, TL431CLP, TL431CJG, TL431CD, TL431ACD

$T_{high} = +125^\circ\text{C}$ for TL431MJG

- $+85^\circ\text{C}$ for TL431AIP, TL431AILP, TL431IP, TL431ILP, TL431JG
- $+70^\circ\text{C}$ for TL431ACP, TL431ACLP, TL431CP, TL431CLP, TL431CJG, TL431CD, TL431ACD

Note 2:

The deviation parameter ΔV_{ref} is defined as the differences between the maximum and minimum values obtained over the full operating ambient temperature range that applies.



The average temperature coefficient of the reference input voltage, αV_{ref} , is defined as

$$\alpha V_{ref} \frac{\text{ppm}}{^\circ\text{C}} = \frac{\left(\frac{\Delta V_{ref}}{V_{ref} @ 25^\circ\text{C}} \right) \times 10^6}{\Delta T_A} = \frac{\Delta V_{ref} \times 10^6}{\Delta T_A (V_{ref} @ 25^\circ\text{C})}$$

αV_{ref} can be positive or negative depending on whether V_{ref} Min or V_{ref} Max occurs at the lower ambient temperature (Refer to Figure 6)

Example $\Delta V_{ref} = 8.0$ mV and slope is positive, $V_{ref} @ 25^\circ\text{C} = 2.495$ V, $\Delta T_A = 70^\circ\text{C}$

$$\alpha V_{ref} = \frac{0.008 \times 10^6}{70 (2.495)} = 45.8 \text{ ppm}/^\circ\text{C}$$

Note 3:

The dynamic impedance Z_{ka} is defined as: $|Z_{ka}| = \frac{\Delta V_{KA}}{\Delta I_K}$

When the device is programmed with two external resistors, R_1 and R_2 , (refer to Figure 2) the total dynamic impedance of the circuit is defined as:

$$|Z_{ka}| \approx |Z_{ka}| \left(1 + \frac{R_1}{R_2} \right)$$

Note 4:

This test is not applicable to surface mount (D suffix) devices.

FIGURE 1 — TEST CIRCUIT FOR $V_{KA} = V_{ref}$

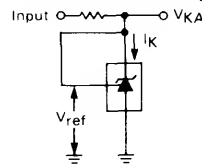


FIGURE 2 — TEST CIRCUIT FOR $V_{KA} > V_{ref}$

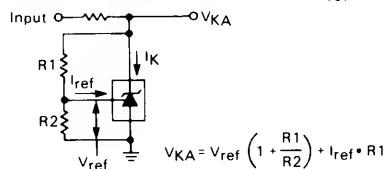


FIGURE 3 — TEST CIRCUIT FOR I_{off}

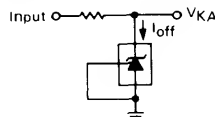


FIGURE 4 — CATHODE CURRENT versus CATHODE VOLTAGE

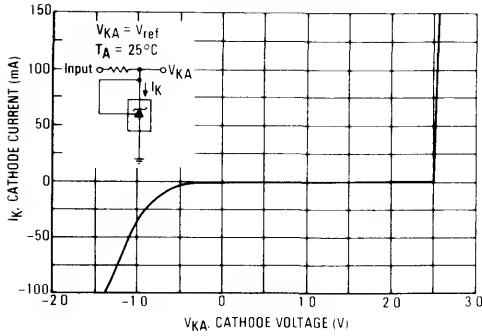


FIGURE 5 — CATHODE CURRENT versus CATHODE VOLTAGE

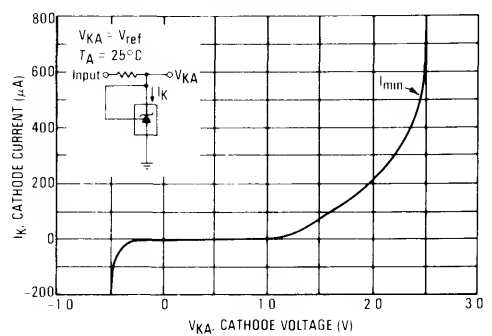


FIGURE 6 — REFERENCE INPUT VOLTAGE versus AMBIENT TEMPERATURE

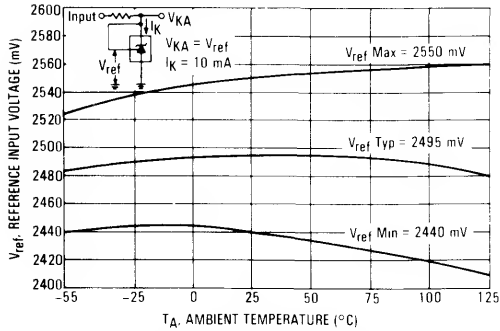


FIGURE 7 — REFERENCE INPUT CURRENT versus AMBIENT TEMPERATURE

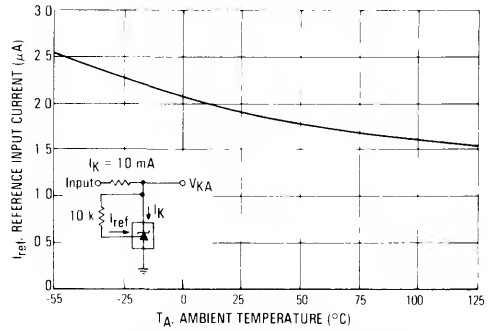


FIGURE 8 — CHANGE IN REFERENCE INPUT VOLTAGE versus CATHODE VOLTAGE

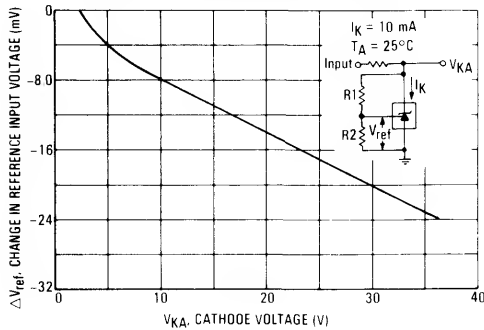
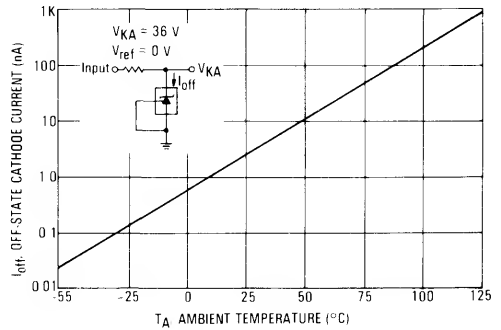
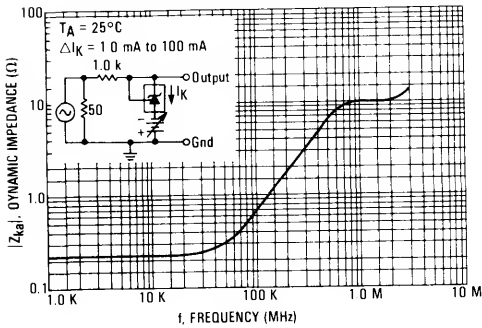


FIGURE 9 — OFF-STATE CATHODE CURRENT versus AMBIENT TEMPERATURE

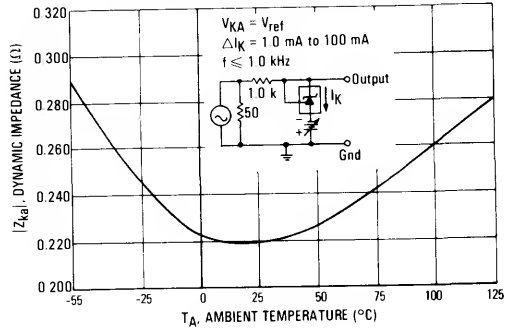


TL431,A Series

**FIGURE 10 — DYNAMIC IMPEDANCE
versus FREQUENCY**



**FIGURE 11 — DYNAMIC IMPEDANCE
versus AMBIENT TEMPERATURE**



**FIGURE 12 — OPEN LOOP VOLTAGE GAIN
versus FREQUENCY**

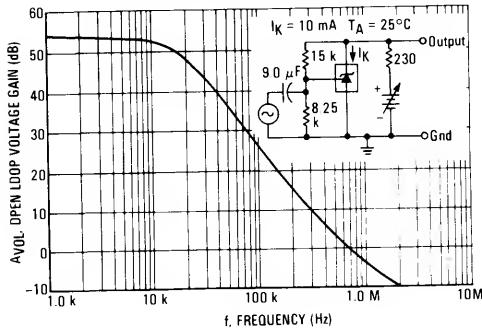


FIGURE 13 — SPECTRAL NOISE DENSITY

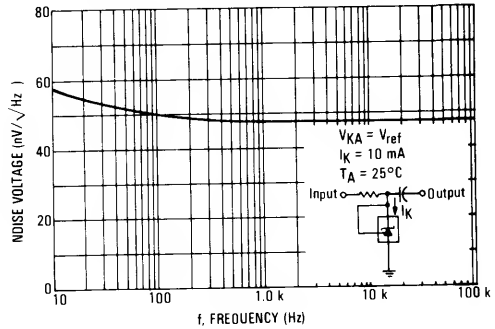


FIGURE 14 — PULSE RESPONSE

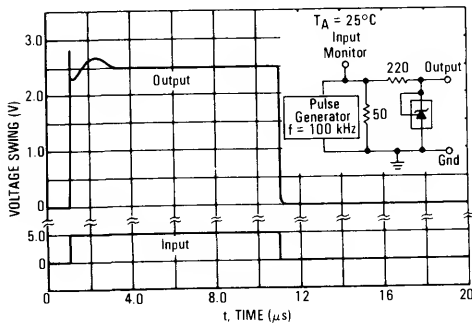


FIGURE 15 — STABILITY BOUNDARY CONDITIONS

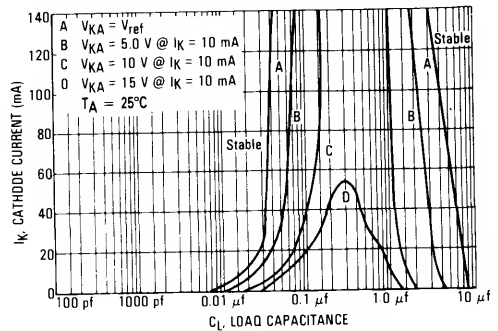


FIGURE 16 — TEST CIRCUIT FOR CURVE A OF STABILITY BOUNDARY CONDITIONS

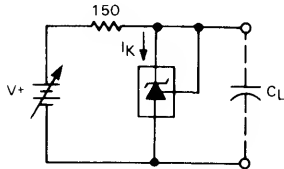
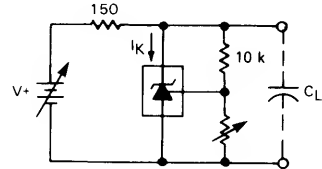


FIGURE 17 — TEST CIRCUIT FOR CURVES B, C, AND D OF STABILITY BOUNDARY CONDITIONS



5

TYPICAL APPLICATIONS

FIGURE 18 — SHUNT REGULATOR

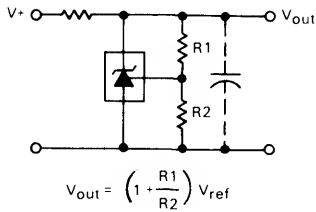


FIGURE 19 — HIGH CURRENT SHUNT REGULATOR

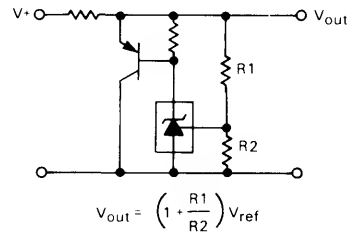


FIGURE 20 — OUTPUT CONTROL OF A THREE-TERMINAL FIXED REGULATOR

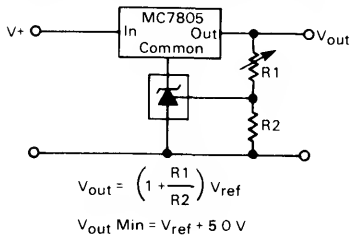


FIGURE 21 — SERIES PASS REGULATOR

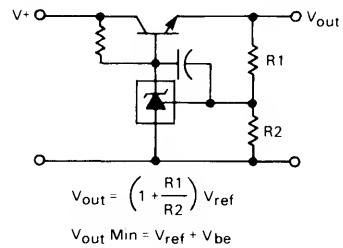


FIGURE 22 — CONSTANT CURRENT SOURCE

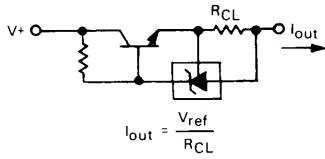


FIGURE 24 — TRIAC CROWBAR

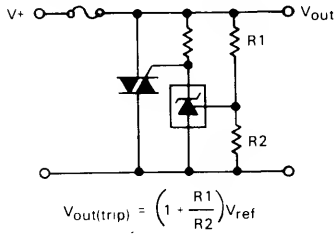
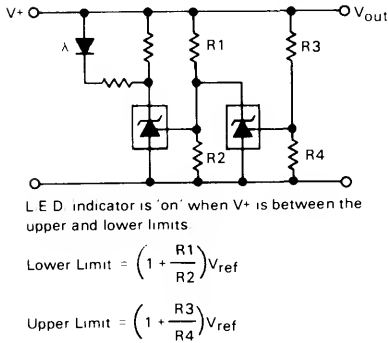


FIGURE 26 — VOLTAGE MONITOR



LED indicator is 'on' when V+ is between the upper and lower limits

$$\text{Lower Limit} = \left(1 + \frac{R1}{R2}\right)V_{ref}$$

$$\text{Upper Limit} = \left(1 + \frac{R3}{R4}\right)V_{ref}$$

FIGURE 28 — LINEAR OHMMETER

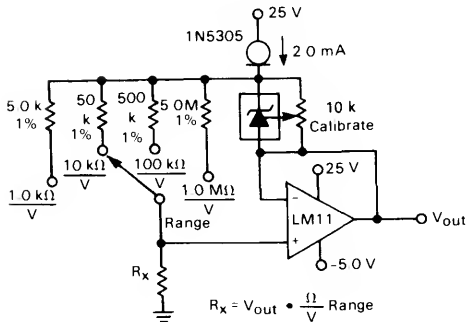


FIGURE 23 — CONSTANT CURRENT SINK

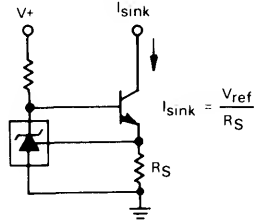


FIGURE 25 — SCR CROWBAR

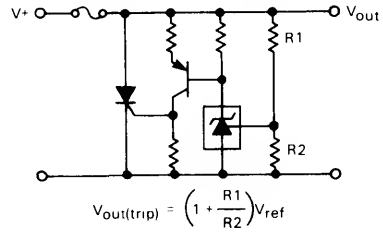
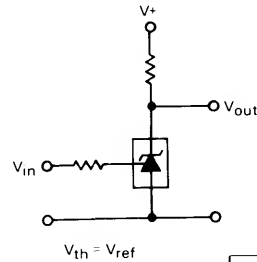
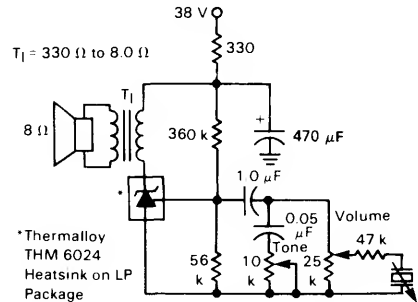


FIGURE 27 — SINGLE-SUPPLY COMPARATOR WITH TEMPERATURE-COMPENSATED THRESHOLD



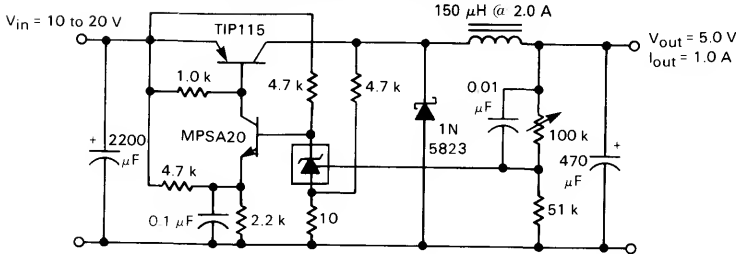
V _{in}	V _{out}
< V _{ref}	V ₊
> V _{ref}	≈ 2.0 V

FIGURE 29 — SIMPLE 400 mW PHONO AMPLIFIER

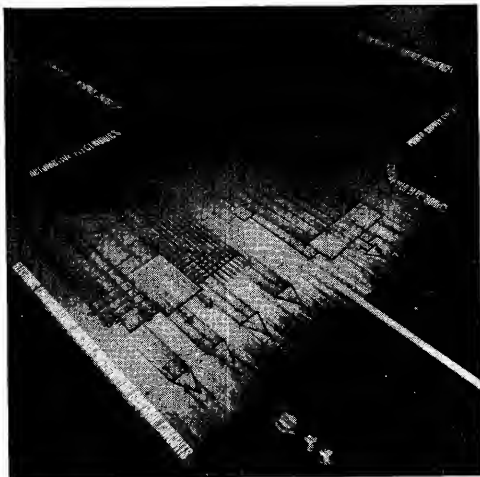


*Thermalloy
THM 6024
Heatsink on LP
Package

FIGURE 30 — HIGH EFFICIENCY STEP-DOWN SWITCHING CONVERTER



TEST	CONDITIONS	RESULTS
Line Regulation	$V_{in} = 10 \text{ V to } 20 \text{ V}$, $I_o = 1.0 \text{ A}$	53 mV (1.1%)
Load Regulation	$V_{in} = 15 \text{ V}$, $I_o = 0 \text{ A to } 1.0 \text{ A}$	25 mV (0.5%)
Output Ripple	$V_{in} = 10 \text{ V}$, $I_o = 1.0 \text{ A}$	50 mV _{p-p} P.A.R.D.
Output Ripple	$V_{in} = 20 \text{ V}$, $I_o = 1.0 \text{ A}$	100 mV _{p-p} P.A.R.D.
Efficiency	$V_{in} = 15 \text{ V}$, $I_o = 1.0 \text{ A}$	82%



In Brief . . .

Motorola's line of digital-to-analog and analog-to-digital converters includes several well established industry standards, and many are available in various linearity grades so as to suit most any application.

The A/D converters have 7 and 8-bit flash converters suitable for NTSC and PAL systems, CMOS 8 to 10-bit converters, as well as other high-speed digitizing applications.

The D/A converters have 6 and 8-bit devices, video speed (for NTSC and PAL) devices, and triple video DAC with on-board color palette for color graphics applications.

Data Conversion

Selector Guide

A-D Converters	6-2
D-A Converters	6-3
A-D/D-A Converters	6-3

Alphanumeric Listing	6-4
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Related Application Notes	6-4
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Data Sheets	6-5
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Data Conversion

The line of data conversion products which Motorola offers spans a wide spectrum of speed and resolution/accuracy. Features, including bus compatibility, minimize external parts count and provide easy interface to microprocessor systems. Various technologies, such as Bipolar and CMOS, are utilized to achieve functional capability, accuracy and production repeatability. Bipolar technology generally results in higher speed, while CMOS devices offer greatly reduced power consumption.

A-D Converters

CMOS

Resolution (Bits)	Device	Nonlinearity (Max)	Conversion Time	Input Voltage Range	Supplies (V)	Temperature Range	Package Suffix	Comments
8	MC145040	$\pm 1/2$ LSB	10 μ s	0 to V _{DD}	+ 5.0, $\pm 10\%$	-40°C to + 85°C	P/738 FN/775	Requires External Clock, 11-Ch MUX
	MC145041		20 μ s					Includes Internal Clock, 11-Ch MUX
	MC14442						P/710 FN/776	μ P Compatible 11-Channel MUX S.A.R.
	MC14549B MC14559B	successive approximation registers					+ 3.0 to + 18	-55°C to + 125°C -40°C to + 85°C
8-10	MC14443/47	$\pm 0.5\%$ Full Scale	300 μ s	Variable w/Supply	+ 5.0 to + 18	-40°C to + 85°C	P/648 DW/751G	μ P Compatible, Single Slope, 6-Channel MUX
3-1/2 Digit	MC14433	$\pm 0.05\%$ ± 1 Count	40 ms	± 2.0 V ± 200 mV	+ 5.0 to + 8.0 - 2.8 to - 8.0		P/709 DW/751E	Dual Slope

Bipolar

7	MC10321	$\pm 1/2$ LSB	40 ns	0 to 2.0 V_{p-p} Max	+ 5.0 V and - 3.0 V to - 6.0 V	0°C to + 70°C	P/738 DW/751D	Video Speed, Grey Code TTL Outputs
8	MC10319	± 1 LSB					L/623 P/709 DW/751F Die Form	Video Speed Flash Converter, Internal Grey Code TTL Outputs

D-A Converters

CMOS

Resolution (Bits)	Device	Suffix	Accuracy @ 25°C (Max)	Max Settling Time ($\pm 1/2$ LSB)	Supplies (V)	Temperature Range	Package	Comments
6	MC144110	P DW	—	—	+5.0 to +15	0°C to +85°C	707 751G	Serial input, Hex DAC, 6 outputs
	MC144111	P DW					646 751G	Serial input, Quad DAC, 4 outputs

Bipolar

8	DAC-08	Q	$\pm 1/2$ LSB	150 ns	± 4.5 to ± 18	-55°C to $+125^{\circ}\text{C}$	620	High-Speed Multiplying	
		AQ	$\pm 1/4$ LSB	135 ns		0°C to $+70^{\circ}\text{C}$			620 648 D/751B
		C	± 1 LSB	150 ns					
		E	$\pm 1/2$ LSB	135 ns					
		H	$\pm 1/4$ LSB						
	MC1408	L6/P6	± 2 LSB	300 ns Typ	$+5.0$, -5.0 to -15	0°C to $+75^{\circ}\text{C}$	620 648		Multiplying
		L7/P7	± 1 LSB						
		L8/P8	$\pm 1/2$ LSB			-55°C to $+125^{\circ}\text{C}$	620		
	MC1508	L8							
	MC10318	P	$\pm 1/2$ LSB	10 ns Typ	-5.2	0°C to $+70^{\circ}\text{C}$	648		ECL input Logic Levels Video Applications
4 x 3	MC10320	L	$\pm 1/4$ LSB	3.0 ns	$+5.0$ or ± 5.0		733	125 MHz Color Graphics Triple DAC	
	MC10320-1					90 MHz Color			
8	MC10322	P	$\pm 1/2$ LSB	5.0 ns	$+5.0$, -5.2	-40°C to $+85^{\circ}\text{C}$	649	TTL 40 MHz Min	
	MC10324				-5.2			ECL 40 MHz Min	

A-D/D-A Converters

CMOS — For Telecommunications

Resolution (Bits)	Device	Monotonicity (Bits)	Conversion Time	Input Voltage Range	Supplies (V)	Temperature Range	Package	Comments
13	MC145402	13	62.5 μ s	± 3.28 V peak	± 5.0 to 6.0	-40°C to +85°C	L 620	Digital signal processing (e.g., echo cancelling, high-speed modems, phone systems with conferencing)

DATA CONVERTERS

A-D Converters

Device	Function	Page
MC10319	High Speed 8-Bit D-to-A Flash Converter	6-39
MC10321	High Speed 7-Bit A-to-D Flash Converter	6-57

D-A Converters

Device	Function	Page
DAC-08	High Speed 8-Bit Multiplying D-to-A Converter	6-5
MC1408	8-Bit Multiplying D-to-A Converter	6-15
MC1508	8-Bit Multiplying D-to-A Converter	6-15
MC10318P	High Speed 8-Bit D-to-A Converters	6-27
MC10320, 20-1	Triple 4-Bit Color Palette Video DAC	See Chapter 9
MC10322	8-Bit Video DAC with TTL Inputs	6-75
MC10324	8-Bit Video DAC with ECL Inputs	6-76

RELATED APPLICATION NOTES

Application Note	Title	Related Device
EB-51	Successive Approximation BCD A-to-D Converter	MC1408, MC1508
AN702	High Speed Digital-To-Analog And Analog-To-Digital Techniques	General Information
AN926	Techniques for Improving The Settling Time of a DAC and Op Amp Combination	Various

HIGH SPEED 8-BIT MULTIPLYING D-TO-A CONVERTER

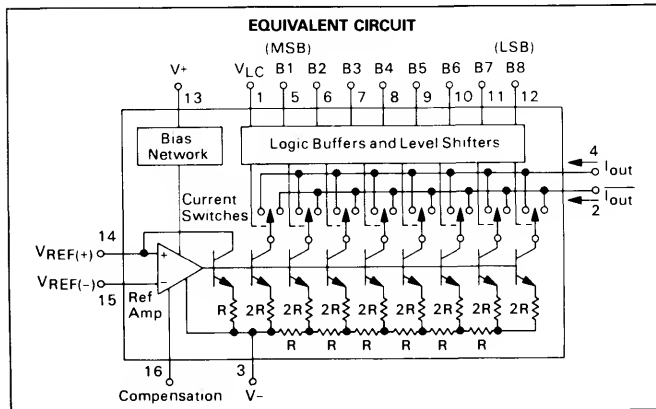
The DAC-08 series is a monolithic 8-bit high speed multiplying digital-to-analog converter, capable of settling to within 1/2 LSB (0.19%) in 85 ns. Monotonic multiplying performance is retained over a wide 40-to-1 reference current range. Full scale and reference currents are matched to within 1 LSB, therefore eliminating the need for full scale trim in most applications.

Dual complementary current outputs with high voltage compliance provide added versatility and allow differential mode of operation to effectively double the peak-to-peak output swing. In many applications, output current-to-voltage conversion can be accomplished without requiring an external op amp. Noise-immune inputs permit direct interface with TTL and DTL levels when the logic threshold control, V_{LC} (Pin 1) is grounded. All other logic family thresholds are attainable by adjusting the voltage level of Pin 1. Performance characteristics are virtually unchanged over the entire ± 4.5 V to ± 18 V power supply range. Power consumption is typically 33 mW with ± 5.0 V supplies.

The DAC-08 is available in several versions, with nonlinearity as tight as $\pm 0.1\%$ ($\pm 1/4$ LSB) over temperature. All versions are guaranteed monotonic over 8 bits. For an extra margin of performance, Motorola utilizes thin-film resistors permitting very accurate resistive values which are extremely stable over temperature.

High performance characteristics along with low cost, make the DAC-08 an excellent selection for applications such as CRT displays, waveform generation, high speed modems, and high speed analog-to-digital converters.

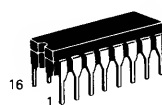
- Fast Settling Time — 85 ns
- Full Scale Current Prematched to ± 1 LSB
- Nonlinearity Over Temperature to $\pm 0.1\%$ Max
- Differential Current Outputs
- High Voltage Compliance Outputs -10 V to $+18$ V
- Wide Range Multiplying Capability
- Inputs Compatible With TTL, DTL, CMOS, PMOS, ECL, HTL
- Low Full Scale Current Drift
- Wide Power Supply Range ± 4.5 V to ± 18 V
- Low Power Consumption
- Thin-Film Resistors
- Low Cost



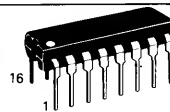
DAC-08

HIGH SPEED 8-BIT MULTIPLYING D-TO-A CONVERTER

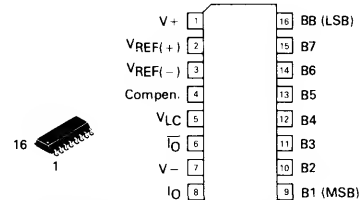
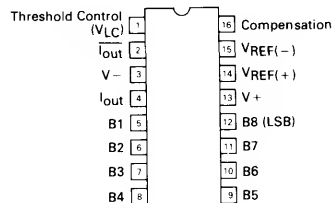
SILICON MONOLITHIC
INTEGRATED CIRCUIT



Q SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648



D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO-16)

(Top View)

ORDERING INFORMATION

Device	Nonlinearity	Temperature Range	Package
DAC-08AQ	$\pm 0.1\%$	-55°C to $+125^{\circ}\text{C}$	Ceramic
DAC-08Q	$\pm 0.19\%$		Ceramic
DAC-08HQ	$\pm 0.1\%$		Ceramic
DAC-08EQ	$\pm 0.19\%$		Ceramic
DAC-08CQ	$\pm 0.39\%$		Ceramic
DAC-08CD	$\pm 0.39\%$		SO-16
DAC-08ED	$\pm 0.19\%$		SO-16
DAC-08HP	$\pm 0.1\%$		Plastic
DAC-08EP	$\pm 0.19\%$		Plastic
DAC-08CP	$\pm 0.39\%$		Plastic

DAC-08

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
V ⁺ Supply to V-Supply	—	36	V
Logic Inputs	—	V- to V- Plus 36	V
Logic Threshold Control	V _{LC}	V- to V ⁺	V
Analog Current Outputs	I _{out}	See Figure 7	mA
Reference Inputs (V14, V15)	V _{REF}	V- to V ⁺	V
Reference Input Differential Voltage (V14 to V15)	V _{REF(D)}	±18	V
Reference Input Current (I14)	I _{REF}	5 0	mA
Operating Temperature Range DAC-08AQ, Q DAC-08HQ, EQ, CQ, HP, EP, CP, ED, CD	T _A	-55 to +125 0 to +70	°C
Storage Temperature	T _A	-65 to +150	°C
Power Dissipation Derate above 100°C	P _D R _{θJA}	500 10	mW mW/°C

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, I_{REF} = 2.0 mA, T_A = -55°C to +125°C, unless otherwise noted.)

Characteristic	Symbol	DAC-08A			DAC-08			Unit
		Min	Typ	Max	Min	Typ	Max	
Resolution	—	8	8	8	8	8	8	Bits
Monotonicity	—	8	8	8	8	8	8	Bits
Nonlinearity, T _A = 0°C to +70°C	NL	—	—	±0.1	—	—	±0.19	%FS
Settling Time to ±1/2 LSB, Figure 24 (All Bits Switched On or Off, T _A = 25°C)(Note 1)	t _s	—	85	—	—	85	—	ns
Propagation Delay, T _A = 25°C (Note 1)	—	—	—	—	—	—	—	ns
Each Bit	t _{PLH}	—	35	—	—	35	—	ns
All Bits Switched	t _{PHL}	—	35	—	—	35	—	ns
Full Scale Tempco	TC _{FS}	—	±10	—	—	±10	—	ppm/°C
Output Voltage Compliance Full Scale Current Change < 1/2 LSB, R _{out} > 20 megohm typ	V _{OC}	-10	—	+18	-10	—	+18	V
Full Range Current (V _{REF} = 10.000 V; R14, R15 = 5 000 kΩ, T _A = 25°C)	I _{FR4}	1 984	1 992	2 000	1.94	1.99	2.04	mA
Full Range Symmetry (I _{FR4} - I _{FR2})	I _{FRS}	—	±0.5	±4.0	—	±1.0	±8.0	μA
Zero Scale Current	I _{ZS}	—	0.1	1.0	—	0.2	2.0	μA
Output Current Range V- = -5.0 V V- = -8.0 V to -18 V	I _{OR1} I _{OR2}	0 0	— —	2.1 4.2	0 0	— —	2.1 4.2	mA
Logic Input Levels (V _{LC} = 0 V) Logic "0" Logic "1"	V _{IL} V _{IH}	— 2.0	— —	0.8 —	— 2.0	— —	0.8 —	V
Logic Input Current (V _{LC} = 0 V) Logic Input "0" (V _{IN} = -10 V to +0.8 V) Logic Input "1" (V _{IN} = +2.0 V to +18 V)	I _{IL} I _{IH}	— —	-2.0 0.002	-10 10	— —	-2.0 0.002	-10 10	μA
Logic Input Swing, V- = -15 V	V _{IS}	-10	—	+18	-10	—	+18	V
Logic Threshold Range, V _S = ±15 V	V _{THR}	-10	—	+13.5	-10	—	+13.5	V
Reference Bias Current	I ₁₅	—	-1.0	-3.0	—	-1.0	-3.0	μA
Reference Input Slew Rate Figure 19 (Note 1)	di/dt	—	8.0	—	—	8.0	—	mA/μs
Power Supply Sensitivity (I _{REF} = 1.0 mA) V ⁺ = 4.5 V to 18 V V- = -4.5 V to -18 V	PSSI _{FS} PSSI _{FS}	— —	±0.0003 ±0.002	±0.01 ±0.01	— —	±0.0003 ±0.002	±0.01 ±0.01	%/%
Power Supply Current V _S = ±5.0 V, I _{REF} = 1.0 mA V _S = +5.0 V, -15 V, I _{REF} = 2.0 mA V _S = ±15 V, I _{REF} = 2.0 mA	I ⁺ I ⁻ I ⁺ I ⁻ I ⁺ I ⁻	— — — — — —	2.3 -4.3 2.4 -6.4 2.5 -6.5	3.8 -5.8 3.8 -7.8 3.8 -7.8	— — — — — —	2.3 -4.3 2.4 -6.4 2.5 -6.5	3.8 -5.8 3.8 -7.8 3.8 -7.8	mA
Power Dissipation V _S = ±5.0 V, I _{REF} = 1.0 mA V _S = +5.0 V, -15 V, I _{REF} = 2.0 mA V _S = ±15 V, I _{REF} = 2.0 mA	P _D	— — —	33 103 135	48 136 174	— — —	33 108 135	48 136 174	mW

Note 1. Parameter is not 100% tested; guaranteed by design.

DAC-08

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15\text{ V}$, $I_{REF} = 2.0\text{ mA}$, $T_A = 0^\circ\text{C}$ to 70°C , unless otherwise noted.)

Characteristic	Symbol	DAC-08H			DAC-08E			DAC-08C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Resolution	—	8	8	8	8	8	8	8	8	8	Bits
Monotonicity	—	8	8	8	8	8	8	8	8	8	Bits
Nonlinearity, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$	NL	—	—	± 0.1	—	—	± 0.19	—	—	± 0.39	%FS
Settling Time to $\pm 1/2$ LSB (All Bits Switched On or Off, $T_A = 25^\circ\text{C}$) Figure 24 (Note 1)	t_s	—	85	—	—	85	—	—	85	—	ns
Propagation Delay, $T_A = 25^\circ\text{C}$ (Note 1)											ns
Each Bit	t_{PLH}	—	35	—	—	35	—	—	35	—	
All Bits Switched	t_{PHL}	—	35	—	—	35	—	—	35	—	
Full Scale Tempo	TC_{FS}	—	± 10	—	—	± 10	—	—	± 10	—	ppm/ $^\circ\text{C}$
Output Voltage Compliance Full Scale Current Change < $1/2$ LSB, $R_{out} > 20\text{ megohm typ.}$	V_{OC}	-10	—	+18	-10	—	+18	-10	—	+18	V
Full Range Current ($V_{REF} = 10.000\text{ V}$; $R_{14}, R_{15} = 5.000\text{ k}\Omega$) $T_A = 25^\circ\text{C}$	I_{FR4}	1.984	1.992	2.000	1.94	1.99	2.04	1.94	1.99	2.04	mA
Full Range Symmetry ($I_{FR4} - I_{FR2}$)	I_{FRS}	—	± 0.5	± 4.0	—	± 1.0	± 8.0	—	± 2.0	± 16.0	μA
Zero Scale Current	I_{ZS}	—	0.1	1.0	—	0.2	2.0	—	0.2	4.0	μA
Output Current Range $V_- = -5.0\text{ V}$ $V_- = -8.0\text{ V to } -18\text{ V}$	I_{OR1} I_{OR2}	0 0	— —	2.1 4.2	0 0	— —	2.1 4.2	0 0	— —	2.1 4.2	mA
Logic Input Levels ($V_{LC} = 0\text{ V}$) Logic "0" Logic "1"	V_{IL} V_{IH}	— 2.0	— —	0.8 —	— 2.0	— —	0.8 —	— 2.0	— —	0.8 —	V
Logic Input Current ($V_{LC} = 0\text{ V}$) Logic Input "0" ($V_{in} = -10\text{ V to } +0.8\text{ V}$) Logic Input "1" ($V_{in} = +2.0\text{ V to } +18\text{ V}$)	I_{IL} I_{IH}	— —	-2.0 0.002	-10 10	— —	-2.0 0.002	-10 10	— —	-2.0 0.002	-10 10	μA
Logic Input Swing, $V_- = -15\text{ V}$	V_{IS}	-10	—	+18	-10	—	+18	-10	—	+18	V
Logic Threshold Range, $V_S = \pm 15\text{ V}$	V_{THR}	-10	—	+13.5	-10	—	+13.5	-10	—	+13.5	V
Reference Bias Current	I_{15}	—	-1.0	-3.0	—	-1.0	-3.0	—	-1.0	-3.0	μA
Reference Input Slew Rate Figure 19 (Note 1)	dl/dt	—	8.0	—	—	8.0	—	—	8.0	—	mA/ μs
Power Supply Sensitivity ($I_{REF} = 1.0\text{ mA}$) $V_+ = 4.5\text{ V to } 18\text{ V}$ $V_- = -4.5\text{ V to } -18\text{ V}$	PSS_{IFS+} PSS_{IFS-}	— —	± 0.0003 ± 0.002	± 0.01 ± 0.01	— —	± 0.0003 ± 0.002	± 0.01 ± 0.01	— —	± 0.0003 ± 0.002	± 0.01 ± 0.01	%/%
Power Supply Current $V_S = \pm 5.0\text{ V}$, $I_{REF} = 1.0\text{ mA}$ $V_S = +5.0\text{ V}$, -15 V , $I_{REF} = 2.0\text{ mA}$ $V_S = \pm 15\text{ V}$, $I_{REF} = 2.0\text{ mA}$	I_+ I_- I_+ I_- I_+ I_-	— — — — — —	2.3 -4.3 2.4 -6.4 2.5 -6.5	3.8 -5.8 3.8 -7.8 3.8 -7.8	— — — — — —	2.3 -4.3 2.4 -6.4 2.5 -6.5	3.8 -25.8 3.8 -7.8 3.8 -7.8	— — — — — —	2.3 -4.3 2.4 -6.4 2.5 -6.5	3.8 -5.8 3.8 -7.8 3.8 -7.8	mA
Power Dissipation $V_S = \pm 5.0\text{ V}$, $I_{REF} = 1.0\text{ mA}$ $V_S = +5.0\text{ V}$, -15 V , $I_{REF} = 2.0\text{ mA}$ $V_S = \pm 15\text{ V}$, $I_{REF} = 2.0\text{ mA}$	P_D	— — —	33 108 135	48 136 174	— — —	33 108 135	48 136 174	— — —	33 108 135	48 136 174	mW

Note 1. Parameter is not 100% tested; guaranteed by design.

TYPICAL PERFORMANCE CURVES

FIGURE 1 — FULL SCALE CURRENT versus REFERENCE CURRENT

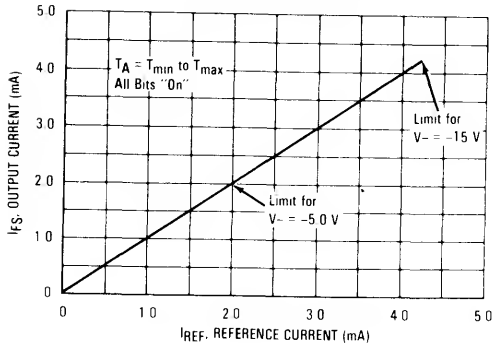


FIGURE 2 — REFERENCE AMP COMMON MODE RANGE

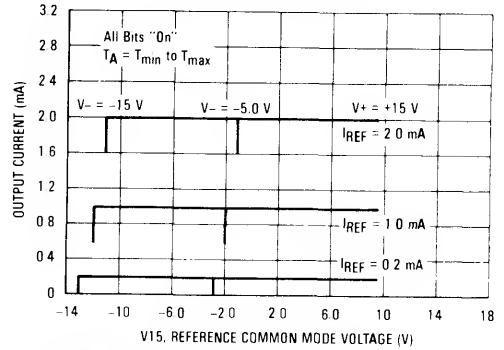
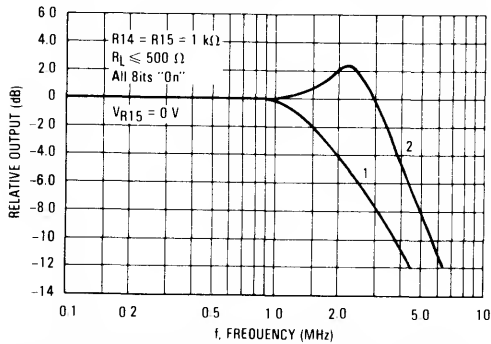


FIGURE 3 — REFERENCE INPUT FREQUENCY RESPONSE



Curve 1 — $C_C = 15 \text{ pF}$, $V_{IN} = 2.0 \text{ V p-p}$ Centered at $+1.0 \text{ V}$ (Large-Signal)
Curve 2 — $C_C = 15 \text{ pF}$, $V_{IN} = 50 \text{ mV p-p}$ Centered at $+200 \text{ mV}$ (Small-Signal)

FIGURE 4 — LSB PROPAGATION DELAY versus I_{FS}

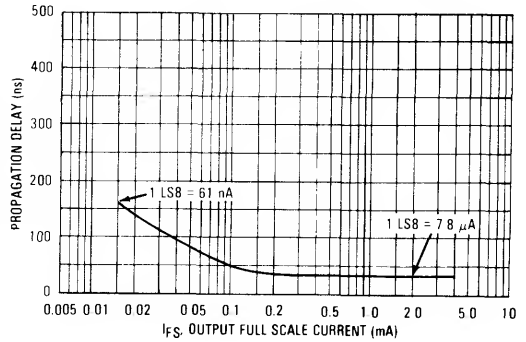


FIGURE 5 — LOGIC INPUT CURRENT versus INPUT VOLTAGE

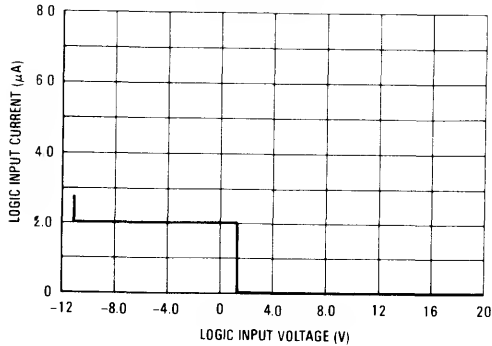
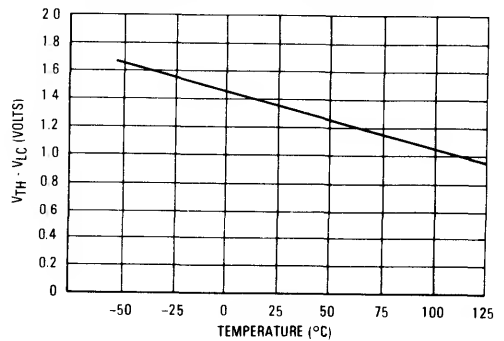


FIGURE 6 — $V_{TH} \cdot V_{LC}$ versus TEMPERATURE



TYPICAL PERFORMANCE CURVES

FIGURE 7 — OUTPUT CURRENT versus OUTPUT VOLTAGE
(Output Voltage Compliance)

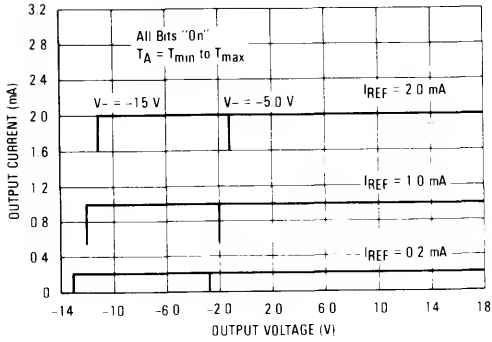


FIGURE 8 — OUTPUT VOLTAGE COMPLIANCE versus TEMPERATURE

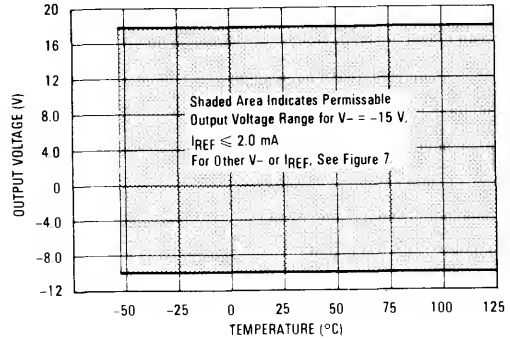
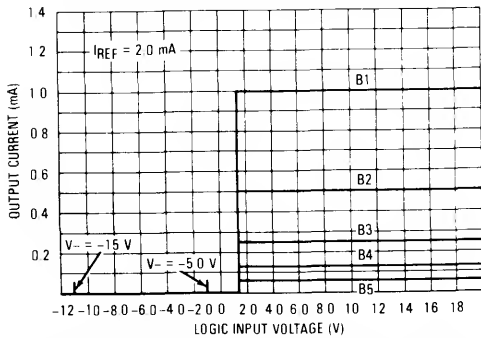


FIGURE 9 — BIT TRANSFER CHARACTERISTICS



NOTE: B1-B8 have identical transfer characteristics. Bits are fully switched with less than 1/2 LSB error, at less than ± 100 mV from actual threshold. These switching points are guaranteed to lie between 0.8 V and 2.0 V over operating temperature range ($V_{LC} = 0$ V).

FIGURE 11 — POWER SUPPLY CURRENT versus V-

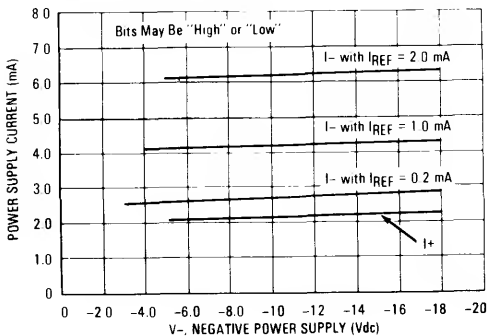


FIGURE 10 — POWER SUPPLY CURRENT versus V+

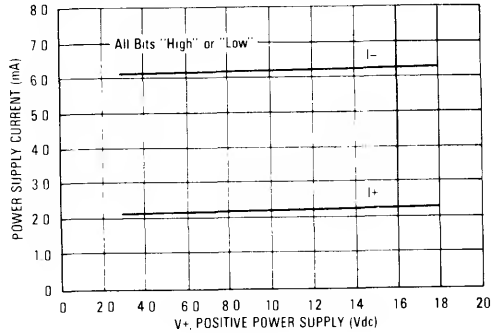
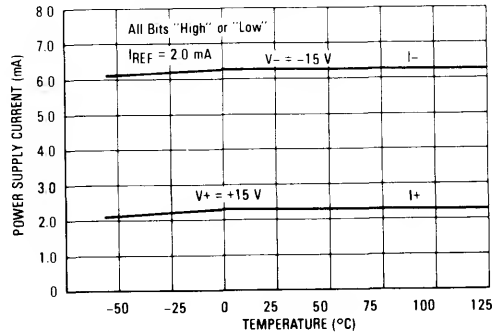


FIGURE 12 — POWER SUPPLY CURRENT versus TEMPERATURE



DAC-08

BASIC CIRCUIT CONFIGURATIONS

FIGURE 13 — RECOMMENDED FULL SCALE ADJUSTMENT CIRCUIT

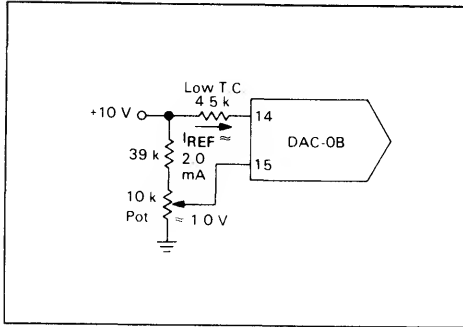


FIGURE 14 — POSITIVE LOW IMPEDANCE OUTPUT OPERATION

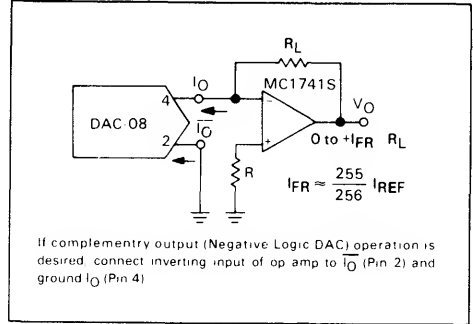


FIGURE 15 — NEGATIVE LOW IMPEDANCE OUTPUT OPERATION

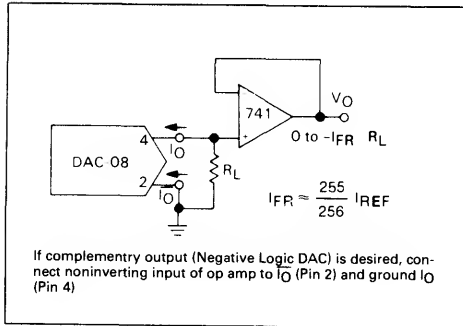


FIGURE 16 — BASIC POSITIVE REFERENCE OPERATION

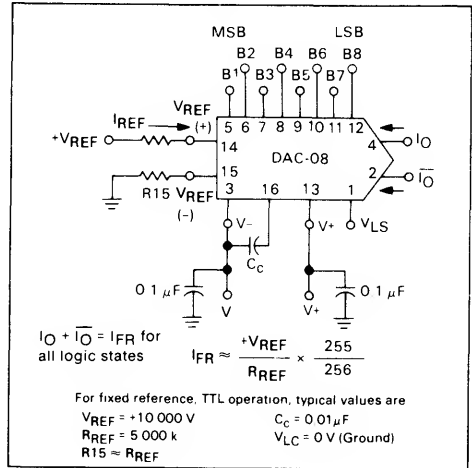
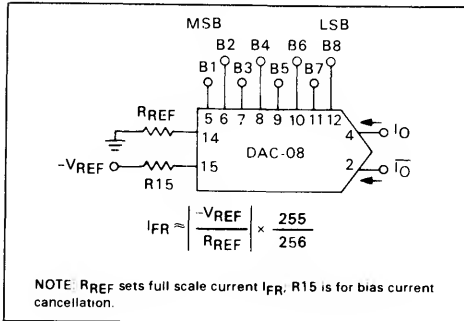


FIGURE 17 — BASIC NEGATIVE REFERENCE OPERATION



DAC-08

BASIC CIRCUIT CONFIGURATIONS

FIGURE 18 — ACCOMMODATING BIPOLAR REFERENCES

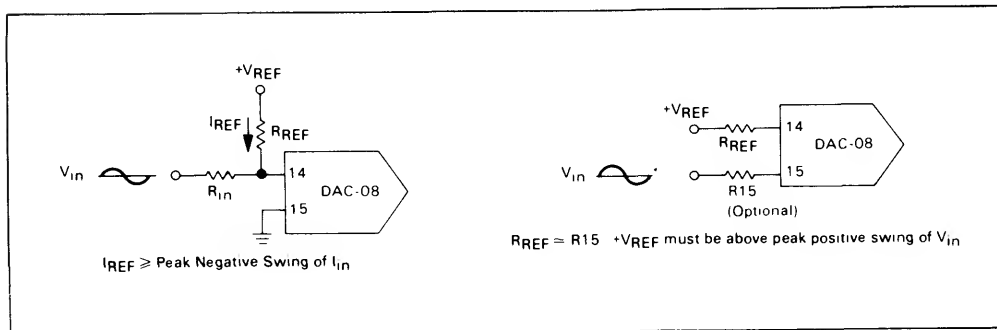


FIGURE 19 — PULSED REFERENCE OPERATION

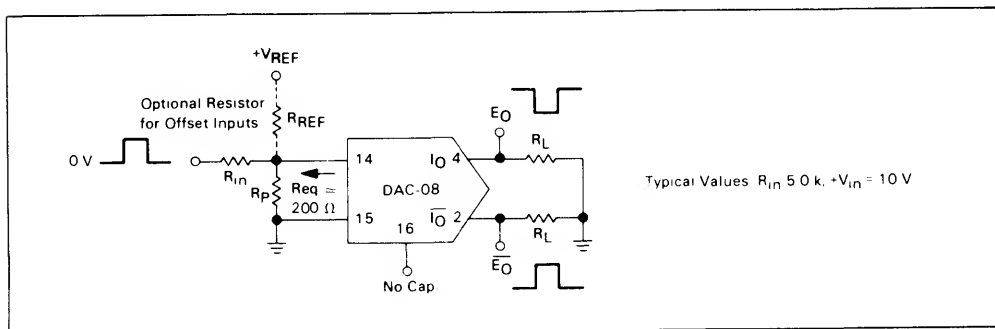
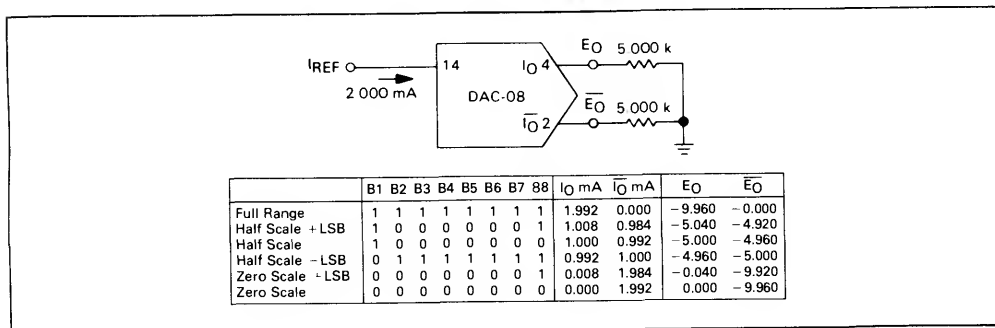


FIGURE 20 — BASIC UNIPOLAR NEGATIVE OPERATION



DAC-08

BASIC CIRCUIT CONFIGURATIONS

FIGURE 21 BASIC BIPOLAR OUTPUT OPERATION

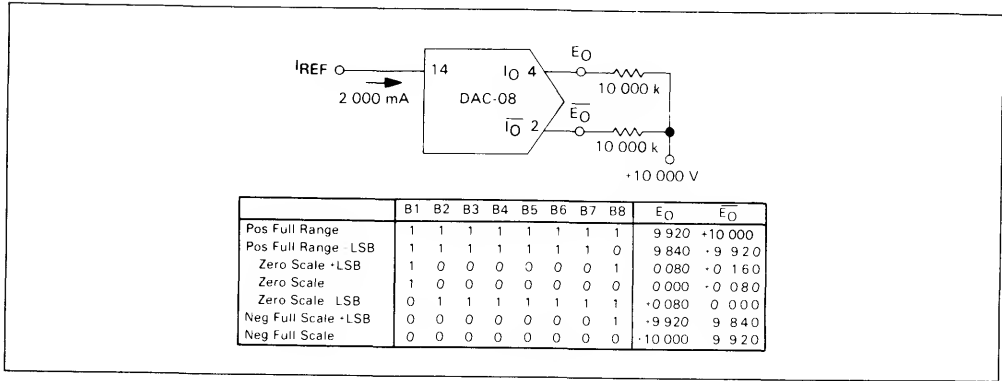
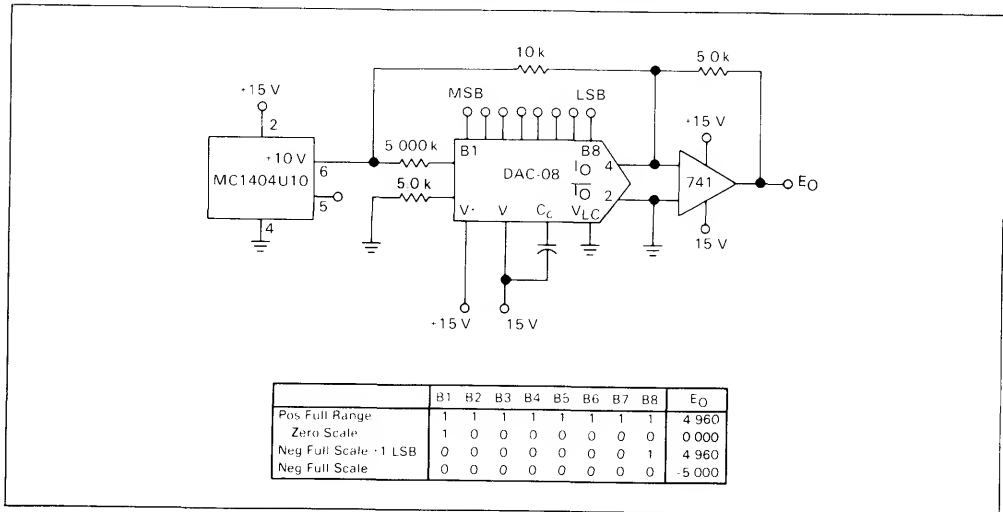
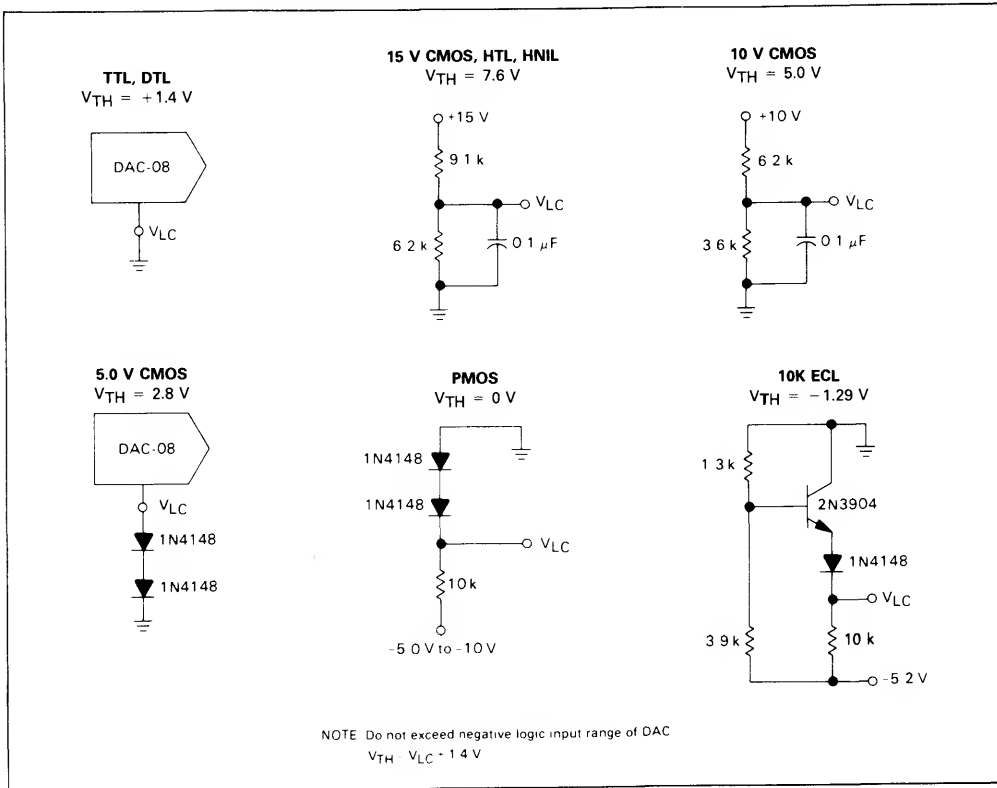


FIGURE 22 OFFSET BINARY OPERATION



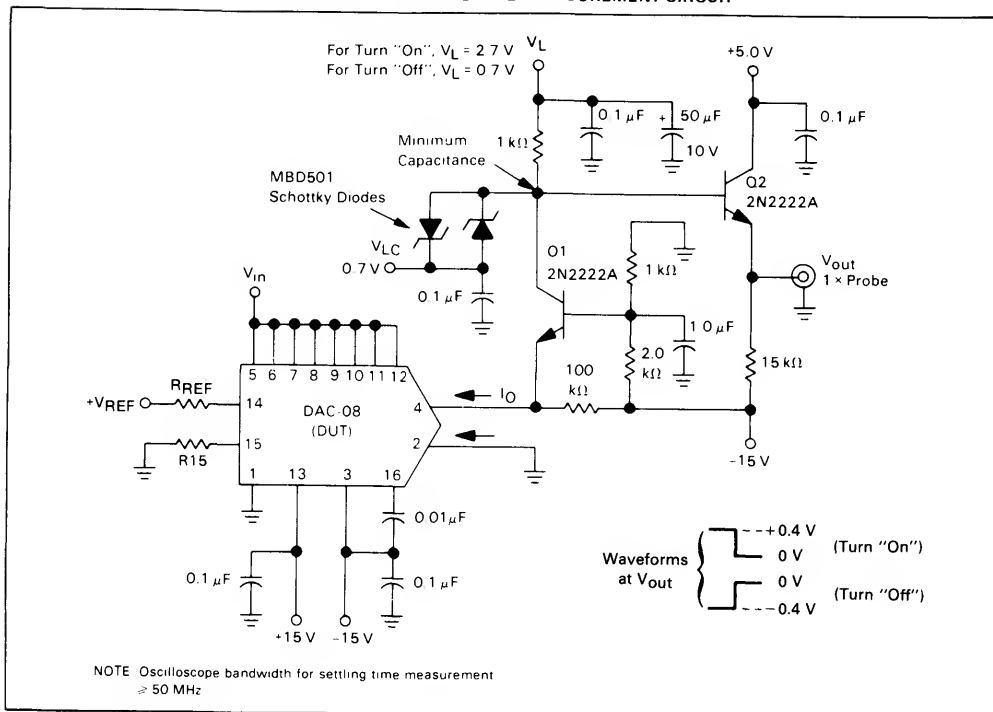
DAC-08

FIGURE 23 — INTERFACING WITH VARIOUS LOGIC FAMILIES



DAC-08

FIGURE 24 — SETTLING TIME MEASUREMENT CIRCUIT



MC1408
MC1508

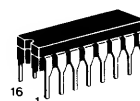
**EIGHT-BIT MULTIPLYING
DIGITAL-TO-ANALOG CONVERTER**

... designed for use where the output current is a linear product of an eight-bit digital word and an analog input voltage.

- Eight-Bit Accuracy Available in Both Temperature Ranges
Relative Accuracy: $\pm 0.19\%$ Error maximum
(MC1408L8, MC1408P8, MC1508L8)
- Seven and Six-Bit Accuracy Available with MC1408 Designated by 7 or 6 Suffix after Package Suffix
- Fast Settling Time — 300 ns typical
- Noninverting Digital Inputs are MTTL and CMOS Compatible
- Output Voltage Swing — +0.4 V to -5.0 V
- High-Speed Multiplying Input
Slew Rate 4.0 mA/ μ s
- Standard Supply Voltages: +5.0 V and -5.0 V to -15 V

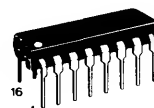
**EIGHT-BIT MULTIPLYING
DIGITAL-TO-ANALOG
CONVERTER**

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



6

FIGURE 1 — D-to-A TRANSFER CHARACTERISTICS

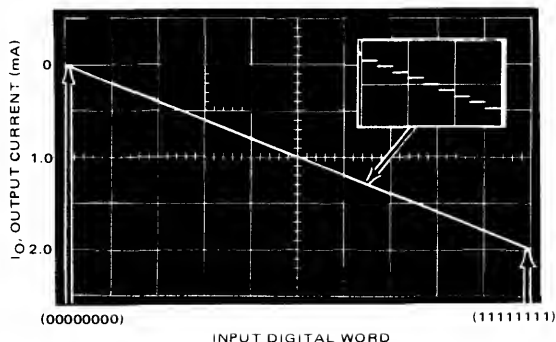
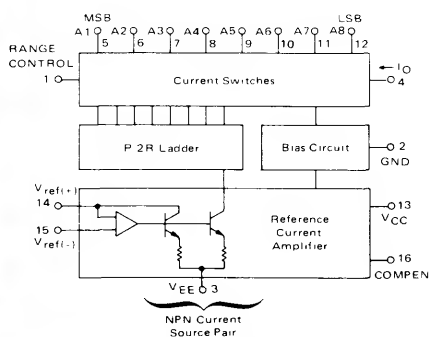


FIGURE 2 — BLOCK DIAGRAM



TYPICAL APPLICATIONS

- Tracking A-to-D Converters
- Successive Approximation A-to-D Converters
- 2 1/2 Digit Panel Meters and DVM's
- Waveform Synthesis
- Sample and Hold
- Peak Detector
- Programmable Gain and Attenuation
- CRT Character Generation
- Audio Digitizing and Decoding
- Programmable Power Supplies
- Analog-Digital Multiplication
- Digital-Digital Multiplication
- Analog-Digital Division
- Digital Addition and Subtraction
- Speech Compression and Expansion
- Stepping Motor Drive

MC1408, MC1508

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V _{CC} V _{EE}	+5.5 -16.5	Vdc
Digital Input Voltage	V ₅ thru V ₁₂	0 to +5.5	Vdc
Applied Output Voltage	V _O	+0.5,-5.2	Vdc
Reference Current	I ₁₄	5.0	mA
Reference Amplifier Inputs	V ₁₄ ,V ₁₅	V _{CC} ,V _{EE}	Vdc
Operating Temperature Range MC1508 MC1408 Series	T _A	-55 to +125 0 to +75	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = -15 Vdc, $\frac{V_{ref}}{R_{14}} = 2.0$ mA, MC1508L8: T_A = -55°C to +125°C. MC1408L Series: T_A = 0 to +75°C unless otherwise noted. All digital inputs at high logic level.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Relative Accuracy (Error relative to full scale I _O) MC1508L8, MC1408L8, MC1408P8 MC1408P7, MC1408L7, See Note 1 MC1408P6, MC1408L6, See Note 1	4	E _r	—	—	± 0.19 ± 0.39 ± 0.78	%
Settling Time to within ±1/2 LSB [includes t _{PLH}] (T _A = +25°C) See Note 2	5	t _S	—	300	—	ns
Propagation Delay Time T _A = +25°C	5	t _{PLH} , t _{PHL}	—	30	100	ns
Output Full Scale Current Drift		TCI _O	—	-20	—	PPM/°C
Digital Input Logic Levels (MSB) High Level, Logic "1" Low Level, Logic "0"	3	V _{IH} V _{IL}	2.0 —	— —	— 0.8	Vdc
Digital Input Current (MSB) High Level, V _{IH} = 5.0 V Low Level, V _{IL} = 0.8 V	3	I _{IH} I _{IL}	— —	0 -0.4	0.04 -0.8	mA
Reference Input Bias Current (Pin 15)	3	I ₁₅	—	-1.0	-5.0	μA
Output Current Range V _{EE} = -5.0 V V _{EE} = -15 V, T _A = 25°C	3	I _{OR}	0 0	2.0 2.0	2.1 4.2	mA
Output Current V _{ref} = 2.000 V, R ₁₄ = 1000 Ω	3	I _O	1.9	1.99	2.1	mA
Output Current (All bits low)	3	I _{O(min)}	—	0	4.0	μA
Output Voltage Compliance (E _r ≤ 0.19% at T _A = +25°C) Pin 1 grounded Pin 1 open, V _{EE} below -10 V	3	V _O	—	—	-0.55, +0.4 -5.0, +0.4	Vdc
Reference Current Slew Rate	6	SR I _{ref}	—	4.0	—	mA/μs
Output Current Power Supply Sensitivity		PSRR(-)	—	0.5	2.7	μA/V
Power Supply Current (All bits low)	3	I _{CC} I _{EE}	— —	+13.5 -7.5	+22 -13	mA
Power Supply Voltage Range (T _A = +25°C)	3	V _{CCR} V _{EE}	+4.5 -4.5	+5.0 -15	+5.5 -16.5	Vdc
Power Dissipation All bits low V _{EE} = -5.0 Vdc V _{EE} = -15 Vdc All bits high V _{EE} = -5.0 Vdc V _{EE} = -15 Vdc	3	P _D	— — — —	105 190 90 160	170 305 — —	mW

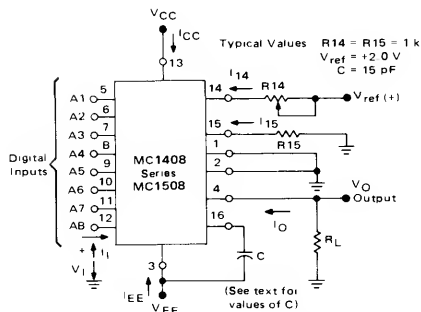
Note 1. All current switches are tested to guarantee at least 50% of rated output current.

Note 2. All bits switched.

MC1408, MC1508

TEST CIRCUITS

FIGURE 3 — NOTATION DEFINITIONS TEST CIRCUIT



V_1 and I_1 apply to inputs A1 thru A8

The resistor tied to pin 15 is to temperature compensate the bias current and may not be necessary for all applications.

$$I_O = K \left\{ \frac{A_1}{2} + \frac{A_2}{4} + \frac{A_3}{8} + \frac{A_4}{16} + \frac{A_5}{32} + \frac{A_6}{64} + \frac{A_7}{128} + \frac{A_8}{256} \right\}$$

$$\text{where } K \cong \frac{V_{ref}}{R_{14}}$$

and $A_N = "1"$ if A_N is at high level
 $A_N = "0"$ if A_N is at low level

FIGURE 4 — RELATIVE ACCURACY TEST CIRCUIT

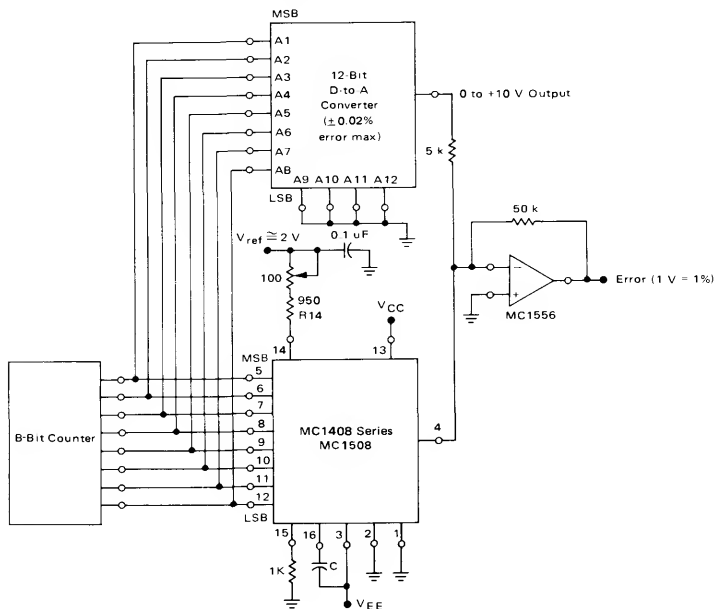
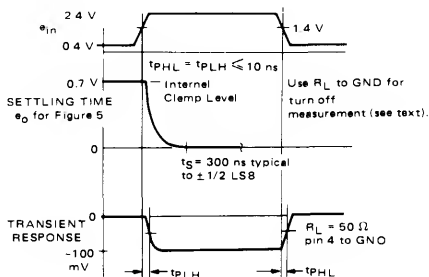
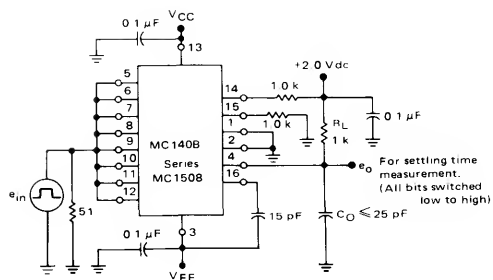


FIGURE 5 — TRANSIENT RESPONSE and SETTLING TIME



MC1408, MC1508

TEST CIRCUITS (continued)

FIGURE 6 — REFERENCE CURRENT SLEW RATE MEASUREMENT

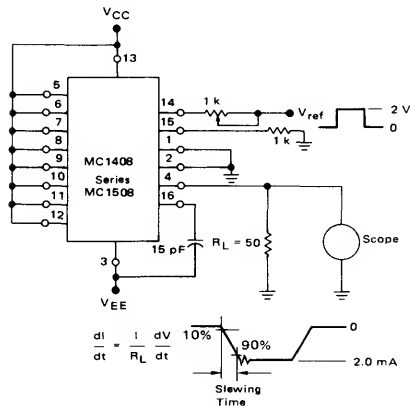


FIGURE 7 — POSITIVE V_{ref}

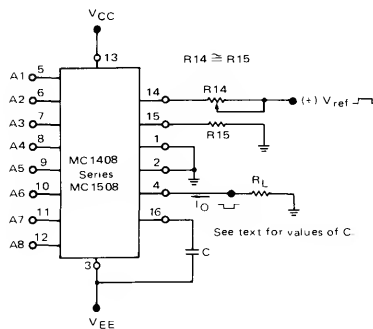
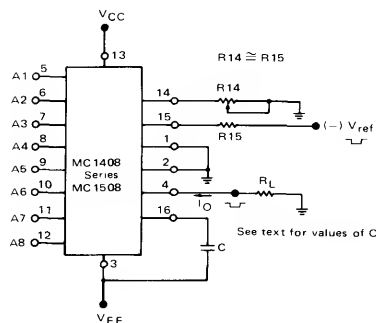
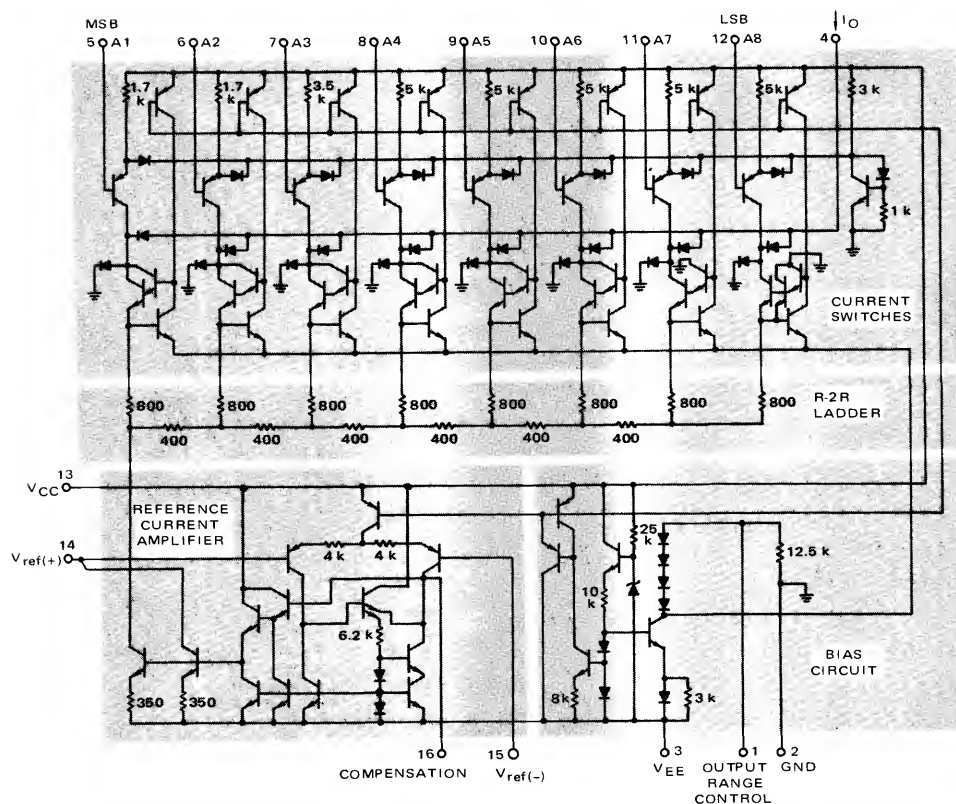


FIGURE 8 — NEGATIVE V_{ref}



MC1408, MC1508

FIGURE 9 — MC1408, MC1508 SERIES EQUIVALENT
CIRCUIT SCHEMATIC
DIGITAL INPUTS



CIRCUIT DESCRIPTION

The MC1408 consists of a reference current amplifier, an R-2R ladder, and eight high-speed current switches. For many applications, only a reference resistor and reference voltage need be added.

The switches are noninverting in operation, therefore a high state on the input turns on the specified output current component. The switch uses current steering for high speed, and a termination amplifier consisting of an active load gain stage with unity gain feedback. The termination amplifier holds the parasitic capacitance of the ladder at a constant voltage during switching, and provides

a low impedance termination of equal voltage for all legs of the ladder.

The R-2R ladder divides the reference amplifier current into binary-related components, which are fed to the switches. Note that there is always a remainder current which is equal to the least significant bit. This current is shunted to ground, and the maximum output current is 255/256 of the reference amplifier current, or 1.992 mA for a 2.0 mA reference amplifier current if the NPN current source pair is perfectly matched.

GENERAL INFORMATION

Reference Amplifier Drive and Compensation

The reference amplifier provides a voltage at pin 14 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input current, I14, must always flow into pin 14 regardless of the setup method or reference voltage polarity.

Connections for a positive reference voltage are shown in Figure 7. The reference voltage source supplies the full current I14. For bipolar reference signals, as in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R15 with only a small sacrifice in accuracy and temperature drift. Another method for bipolar inputs is shown in Figure 25.

The compensation capacitor value must be increased with increases in R14 to maintain proper phase margin; for R14 values of 1.0, 2.5 and 5.0 kilohms, minimum capacitor values are 15, 37, and 75 pF. The capacitor should be tied to VEE as this increases negative supply rejection.

A negative reference voltage may be used if R14 is grounded and the reference voltage is applied to R15 as shown in Figure 8. A high input impedance is the main advantage of this method. Compensation involves a capacitor to VEE on pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 3.0 volts above the VEE supply. Bipolar input signals may be handled by connecting R14 to a positive reference voltage equal to the peak positive input level at pin 15.

When a dc reference voltage is used, capacitive bypass to ground is recommended. The 5.0-V logic supply is not recommended as a reference voltage. If a well regulated 5.0-V supply which drives logic is to be used as the reference, R14 should be decoupled by connecting it to +5.0 V through another resistor and bypassing the junction of the two resistors with 0.1 μ F to ground. For reference voltages greater than 5.0 V, a clamp diode is recommended between pin 14 and ground.

If pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

Output Voltage Range

The voltage on pin 4 is restricted to a range of -0.55 to +0.4 volts at +25°C, due to the current switching methods employed in the MC1408. When a current switch is turned "off", the positive voltage on the output terminal can turn "on" the output diode and increase the output current level. When a current switch is turned "on", the negative output voltage range is restricted. The base of the termination circuit Darlington transistor is one diode voltage below ground when pin 1 is grounded, so a negative voltage below the specified safe level will drive the low current device of the Darlington into saturation, decreasing the output current level.

The negative output voltage compliance of the MC1408 may be extended to -5.0 V volts by opening the circuit at pin 1. The negative supply voltage must be more negative than -10 volts. Using a full scale current of 1.992 mA and load resistor of 2.5 kilohms between pin 4 and ground will yield a voltage output of 256 levels between 0 and -4.980 volts. Floating pin 1 does not affect the converter speed or power dissipation. However, the value of the load resistor determines the switching time due to increased voltage swing. Values of R_L up to 500 ohms do not significantly affect performance, but a 2.5-kilohm load increases "worst case" settling time to 1.2 μ s (when all bits are switched on).

Refer to the subsequent text section on Settling Time for more details on output loading.

If a power supply value between -5.0 V and -10 V is desired, a voltage of between 0 and -5.0 V may be applied to pin 1. The value of this voltage will be the maximum allowable negative output swing.

Output Current Range

The output current maximum rating of 4.2 mA may be used only for negative supply voltages typically more negative than -8.0 volts, due to the increased voltage drop across the 350-ohm resistors in the reference current amplifier.

Accuracy

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full scale current. The relative accuracy of the MC1408 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the MC1408 has a very low full scale current drift with temperature.

The MC1408/MC1508 Series is guaranteed accurate to within $\pm 1/2$ LSB at +25°C at a full scale output current of 1.992 mA. This corresponds to a reference amplifier output current drive to the ladder network of 2.0 mA, with the loss of one LSB = 8.0 μ A which is the ladder remainder shunted to ground. The input current to pin 14 has a guaranteed value of between 1.9 and 2.1 mA, allowing some mismatch in the NPN current source pair. The accuracy test circuit is shown in Figure 4. The 12-bit converter is calibrated for a full scale output current of 1.992 mA. This is an optional step since the MC1408 accuracy is essentially the same between 1.5 and 2.5 mA. Then the MC1408 circuits' full scale current is trimmed to the same value with R14 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accurate D-to-A converter. 16-bit accuracy implies a total error of $\pm 1/2$ of one part in 65,536, or $\pm 0.00076\%$, which is much more accurate than the $\pm 0.19\%$ specification provided by the MC1408x8.

Multiplying Accuracy

The MC1408 may be used in the multiplying mode with eight-bit accuracy when the reference current is varied over a range of 256:1. The major source of error is the bias current of the termination amplifier. Under "worst case" conditions, these eight amplifiers can contribute a total of 1.6 μ A extra current at the output terminal. If the reference current in the multiplying mode ranges from 16 μ A to 4.0 mA, the 1.6 μ A contributes an error of 0.1 LSB. This is well within eight-bit accuracy referenced to 4.0 mA.

A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the MC1408 is monotonic for all values of reference current above 0.5 mA. The recommended range for operation with a dc reference current is 0.5 to 4.0 mA.

MC1408, MC1508

GENERAL INFORMATION (Continued)

Settling Time

The "worst case" switching condition occurs when all bits are switched "on", which corresponds to a low-to-high transition for all bits. This time is typically 300 ns for settling to within $\pm 1/2$ LSB, for 8-bit accuracy, and 200 ns to 1/2 LSB for 7 and 6-bit accuracy. The turn off is typically under 100 ns. These times apply when $R_L \leq 500$ ohms and $C_O \leq 25$ pF.

The slowest single switch is the least significant bit, which turns "on" and settles in 250 ns and turns "off" in 80 ns. In applications where the D-to-A converter functions in a positive-going ramp mode, the "worst case" switching condition does not occur, and a settling time of less than 300 ns may be realized. Bit A7 turns "on" in 200 ns and "off" in 80 ns, while bit A6 turns "on" in 150 ns and "off" in 80 ns.

The test circuit of Figure 5 requires a smaller voltage swing for the current switches due to internal voltage clamping in the MC-1408. A 1.0-kilohm load resistor from pin 4 to ground gives a typical settling time of 400 ns. Thus, it is voltage swing and not the output RC time constant that determines settling time for most applications.

Extra care must be taken in board layout since this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100 μ F supply bypassing for low frequencies, and minimum scope lead length are all mandatory.

TYPICAL CHARACTERISTICS

($V_{CC} = +5.0$ V, $V_{EE} = -15$ V, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 10 — LOGIC INPUT CURRENT versus INPUT VOLTAGE

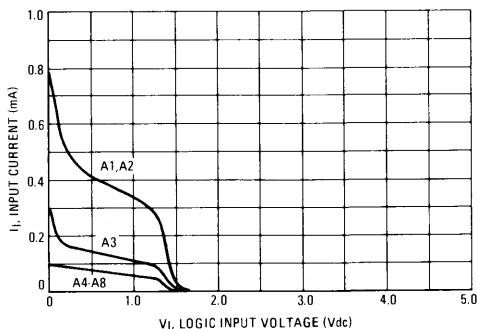


FIGURE 11 — TRANSFER CHARACTERISTIC versus TEMPERATURE (A5 thru A8 thresholds lie within range for A1 thru A4)

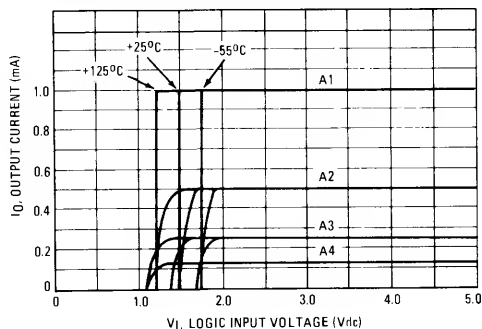


FIGURE 12 — OUTPUT CURRENT versus OUTPUT VOLTAGE (See text for pin 1 restrictions)

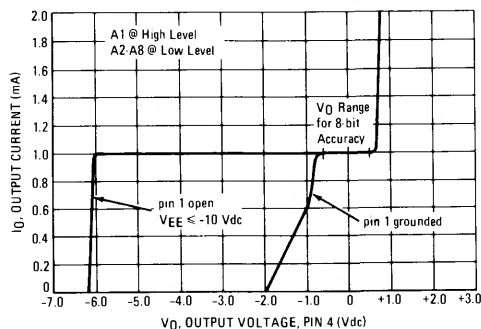
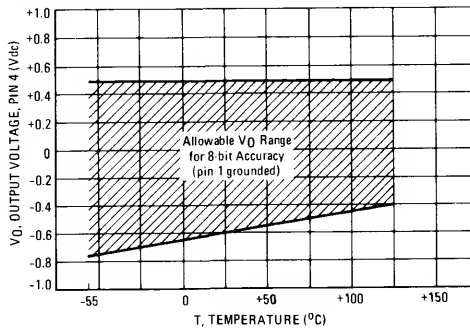


FIGURE 13 — OUTPUT VOLTAGE versus TEMPERATURE (Negative range with pin 1 open is -5.0 Vdc over full temperature range)



MC1408, MC1508

TYPICAL CHARACTERISTICS (continued)
($V_{CC} = +5.0\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 14 — REFERENCE INPUT FREQUENCY RESPONSE

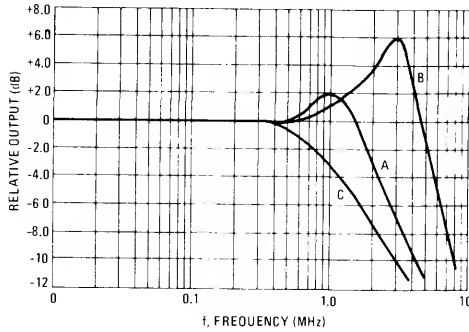


FIGURE 15 — TYPICAL POWER SUPPLY CURRENT versus TEMPERATURE (all bits low)

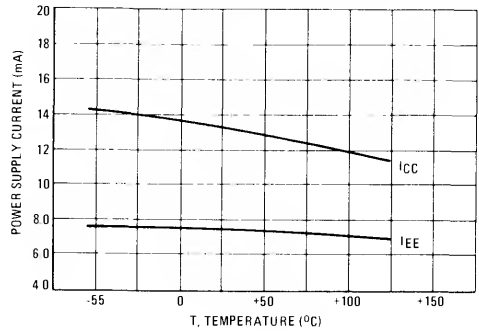
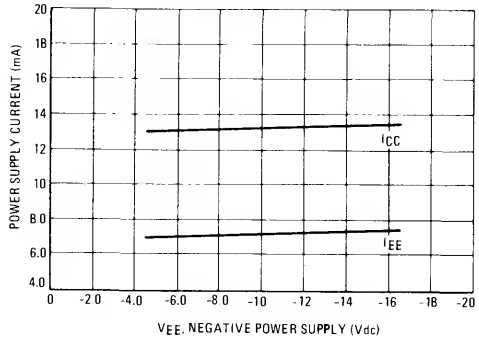
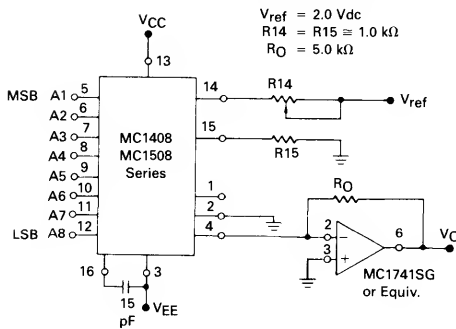


FIGURE 16 — TYPICAL POWER SUPPLY CURRENT versus V_{EE} (all bits low)



APPLICATIONS INFORMATION

FIGURE 17 — OUTPUT CURRENT TO VOLTAGE CONVERSION



Theoretical V_O

$$V_O = \frac{V_{ref}}{R_{14}} (R_O) \left[\frac{A_1}{2} + \frac{A_2}{4} + \frac{A_3}{8} + \frac{A_4}{16} + \frac{A_5}{32} + \frac{A_6}{64} + \frac{A_7}{128} + \frac{A_8}{256} \right]$$

Adjust V_{ref} , R_{14} or R_O so that V_O with all digital inputs at high level is equal to 9.961 volts.

$$V_O = \frac{2\text{ V}}{1\text{ k}} (5\text{ k}) \left[\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256} \right] = 10\text{ V} \left[\frac{255}{256} \right] = 9.961\text{ V}$$

MC1408, MC1508

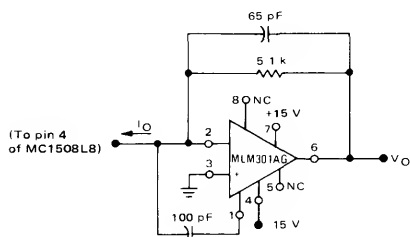
APPLICATIONS INFORMATION (continued)

Voltage outputs of a larger magnitude are obtainable with this circuit which uses an external operational amplifier as a current to voltage converter. This configuration automatically keeps the output of the MC1408 at ground potential and the operational amplifier can generate a positive voltage limited only by its positive supply voltage. Frequency response and settling time are primarily determined by the characteristics of the operational amplifier. In addition, the operational amplifier must be compensated for unity gain, and in some cases overcompensation may be desirable.

Note that this configuration results in a positive output voltage only, the magnitude of which is dependent on the digital input.

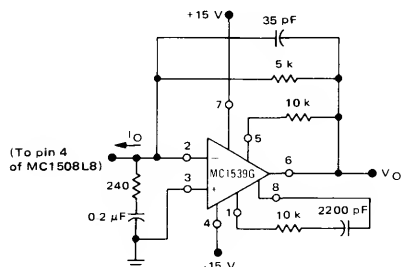
The following circuit shows how the MLM301AG can be used in a feedforward mode resulting in a full scale settling time on the order of 2.0 μ s.

FIGURE 18



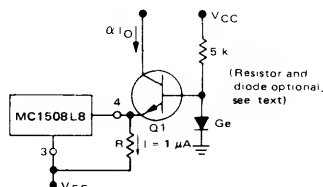
An alternative method is to use the MC1539G and input compensation. Response of this circuit is also on the order of 2.0 μ s. See Motorola Application Note AN-459 for more details on this concept.

FIGURE 19



The positive voltage range may be extended by cascading the output with a high beta common base transistor, Q1, as shown.

FIGURE 20 – EXTENDING POSITIVE VOLTAGE RANGE



The output voltage range for this circuit is 0 volts to BV_{CBO} of the transistor. If pin 1 is left open, the transistor base may be grounded, eliminating both the resistor and the diode. Variations in beta must be considered for wide temperature range applications. An inverted output waveform may be obtained by using a load resistor from a positive reference voltage to the collector of the transistor. Also, high-speed operation is possible with a large output voltage swing, because pin 4 is held at a constant voltage. The resistor (R) to V_{EE} maintains the transistor emitter voltage when all bits are "off" and insures fast turn-on of the least significant bit.

Combined Output Amplifier and Voltage Reference

For many of its applications the MC1408 requires a reference voltage and an operational amplifier. Normally the operational amplifier is used as a current to voltage converter and its output need only go positive. With the popular MC1723G voltage regulator both of these functions are provided in a single package with the added bonus of up to 150 mA of output current. See Figure 21. The MC1723G uses both a positive and negative power supply. The reference voltage of the MC1723G is then developed with respect to the negative voltage and appears as a common-mode signal to the reference amplifier in the D-to-A converter. This allows use of its output amplifier as a classic current-to-voltage converter with the non-inverting input grounded.

Since ± 15 V and $+5.0$ V are normally available in a combination digital-to-analog system, only the -5.0 V need be developed. A resistor divider is sufficiently accurate since the allowable range on pin 5 is from -2.0 to -8.0 volts. The 5.0 kilohm pulldown resistor on the amplifier output is necessary for fast negative transitions.

Full scale output may be increased to as much as 32 volts by increasing R_O and raising the $+15$ V supply voltage to 35 V maximum. The resistor divider should be altered to comply with the maximum limit of 40 volts across the MC1723G. C_O may be decreased to maintain the same $R_O C_O$ product if maximum speed is desired.

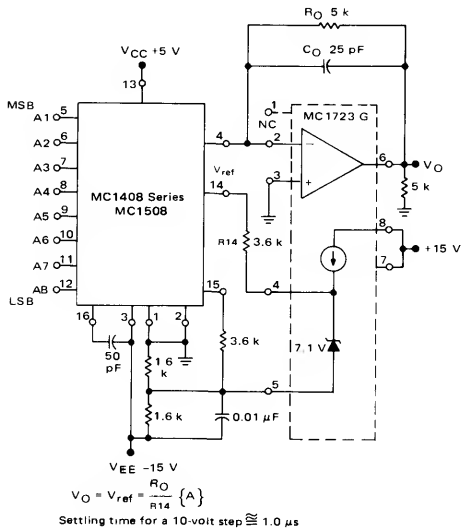
MC1408, MC1508

APPLICATIONS INFORMATION (continued)

Programmable Power Supply

The circuit of Figure 21 can be used as a digitally programmed power supply by the addition of thumbwheel switches and a BCD-to-binary converter. The output voltage can be scaled in several ways, including 0 to +25.5 volts in 0.1-volt increments, ± 0.05 volt; or 0 to 5.1 volts in 20 mV increments, ± 10 mV.

FIGURE 21 — COMBINED OUTPUT AMPLIFIER and VOLTAGE REFERENCE CIRCUIT



Bipolar or Negative Output Voltage

The circuit of Figure 22 is a variation from the standard voltage output circuit and will produce bipolar output signals. A positive current may be sourced into the summing node to offset the output voltage in the negative direction. For example, if approximately 1.0 mA is used a bipolar output signal results which may be described as a 8-bit "1's" complement offset binary. V_{ref} may be used as this auxiliary reference. Note that R_O has been doubled to 10 kilohms because of the anticipated 20 V(p-p) output range.

FIGURE 22 — BIPOLAR OR NEGATIVE OUTPUT VOLTAGE CIRCUIT

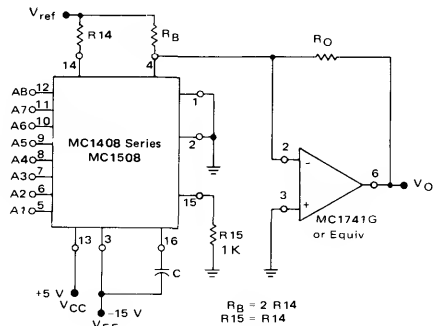
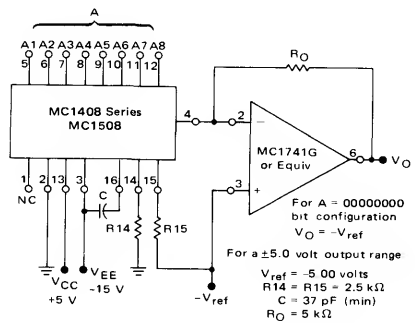


FIGURE 23 — BIPOLAR OR INVERTED NEGATIVE OUTPUT VOLTAGE CIRCUIT



Decrease R_O to 2.5 k Ω for a 0 to -5.0-volt output range. This application provides somewhat lower speed, as previously discussed in the Output Voltage Range section of the General Information.

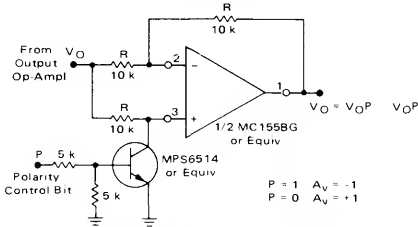
MC1408, MC1508

APPLICATIONS INFORMATION (continued)

Polarity Switching Circuit, 8-Bit Magnitude Plus Sign D-to-A Converter

Bipolar outputs may also be obtained by using a polarity switching circuit. The circuit of Figure 24 gives 8-bit magnitude plus a sign bit. In this configuration the operational amplifier is switched between a gain of +1.0 and -1.0. Although another operational amplifier is required, no more space is taken when a dual operational amplifier such as the MC1558G is used. The transistor should be selected for a very low saturation voltage and resistance.

FIGURE 24 — POLARITY SWITCHING CIRCUIT (8-Bit Magnitude Plus Sign D-to-A Converter)



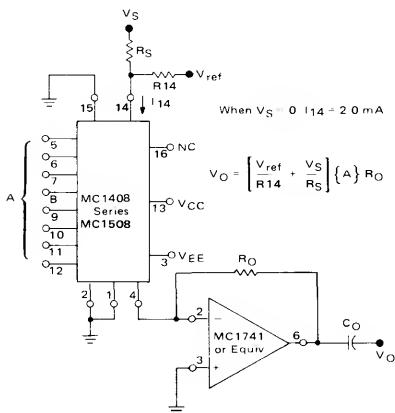
Programmable Gain Amplifier or Digital Attenuator

When used in the multiplying mode the MC1408 can be applied as a digital attenuator. See Figure 25. One advantage of this technique is that if $R_S = 50$ ohms, no compensation capacitor is needed. The small and large signal bandwidths are now identical and are shown in Figure 14.

The best frequency response is obtained by not allowing I_{14} to reach zero. However, the high impedance node, pin 16, is clamped to prevent saturation and insure fast recovery when the current through R14 goes to zero. R_S can be set for a ± 1.0 mA variation in relation to I_{14} . I_{14} can never be negative.

The output current is always unipolar. The quiescent dc output current level changes with the digital word which makes ac coupling necessary.

FIGURE 25 — PROGRAMMABLE GAIN AMPLIFIER OR DIGITAL ATTENUATOR CIRCUIT



Panel Meter Readout

The MC1408 can be used to read out the status of BCD or binary registers or counters in a digital control system. The current output can be used to drive directly an analog panel meter. External meter shunts may be necessary if a meter of less than 2.0 mA full scale is used. Full scale calibration can be done by adjusting R14 or V_{ref} .

FIGURE 26 — PANEL METER READOUT CIRCUIT

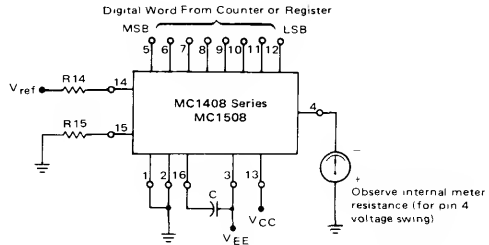
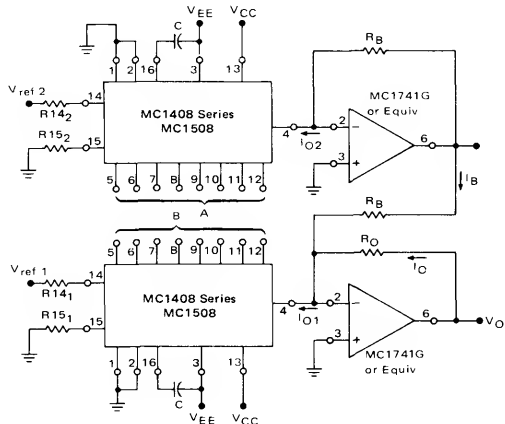


FIGURE 27 — DC COUPLED DIGITAL ATTENUATOR and DIGITAL SUBTRACTION



$$I_{O1} = I_{O1} - I_{O2} \quad I_{O2} = \frac{V_{ref1}}{R_{141}} \{A\} \quad \frac{V_{ref2}}{R_{142}} \{B\} \quad I_{O2} - I_{O1}$$

Digital Subtraction: Let $\frac{V_{ref1}}{R_{141}} = \frac{V_{ref2}}{R_{142}}$ Programmable Amplifier Connect Digital Inputs so A = B

$$V_O = \frac{V_{ref1}}{R_{141}} R_O \{A\} - \{B\} \quad V_O = \{A\} \left[\frac{V_{ref1}}{R_{141}} - \frac{V_{ref2}}{R_{142}} \right]$$

6

FIGURE 36 – TWO-DIGIT BCD CONVERSION

4.0 mA and 0.4 mA with the outputs connected to sum the currents. The error of the D-to-A converter handling the least significant bits will be scaled down by a factor of ten and thus an MC1408L6 may be used for the least significant word.

The diagram shows an 8-bit digital-to-analog converter circuit. It consists of an MC1408 Series DAC (MC1508), an 8-Bit Binary Counter, a Comparator, and an output resistor R_O . The DAC is connected to the counter's outputs (LSB to MSB) via resistors R_{14} and R_{15} . The counter is clocked and reset. The comparator compares the DAC output (V_{ref}) with the input (V_{in}) to produce the digital output (Clock).

$$C = \frac{V_{in}/R_O}{V_{ref}/R_{14}}$$

The circuit shown is a simple counter-ramp converter. An UP/DOWN counter and dual threshold comparator can be used to provide faster operation and continuous conversion.

$$C = \frac{V_{in}/R_O}{V_{ref}/R_1}$$

**HIGH SPEED
8-BIT DIGITAL-TO-ANALOG CONVERTER**

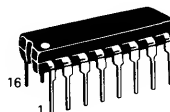
The MC10318 is a high-speed D/A converter capable of data conversion rates in excess of 25 MHz. The digital inputs are compatible with MECL 10,000 Series Logic. Complementary current outputs provide up to 56 mA full scale capability. The MC10318 is 8-bit accurate, and over temperature to meet the requirements of many applications, including: high-speed instrumentation and test equipment, storage oscilloscopes, display processing, radar systems, and digital video systems (broadcast and receiver applications).

- Fast Settling Time — 10 ns (Typ to $\pm 0.19\%$)
- 8-Bit Accurate (0.19%)
- Inputs MECL 10,000 Compatible
- Complementary Current Outputs
- Output Compliance: -1.3 V to $+2.5\text{ V}$
- Single MECL Supply: -5.2 V
- Standard 16-Pin Dual-In-Line Package

MC10318P

**HIGH SPEED
8-BIT DIGITAL-TO-ANALOG
CONVERTER**

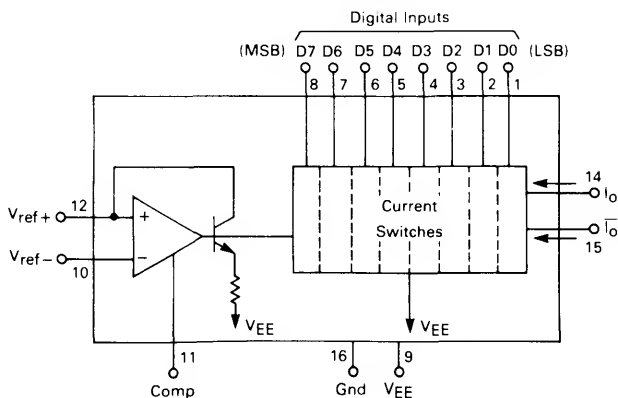
**SILICON MONOLITHIC
INTEGRATED CIRCUIT**



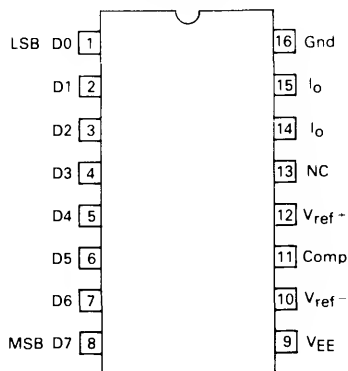
P SUFFIX
PLASTIC PACKAGE
CASE 648

6

BLOCK DIAGRAM



**PIN CONNECTIONS
(TOP VIEW)**



MC10318P

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V _{EE}	-6.0 to +0.5	Vdc
Digital Input Voltage	V _I	0 to V _{EE}	Vdc
Applied Output Voltage	V _O	+5.0 to V _{EE}	Vdc
Reference Current	I _{ref} (12)	5.0	mA
Output Current	I _{FS}	-75	mA
Reference Amplifier Input Range	V _{ref}	-0.5 to V _{EE}	Vdc
Reference Amplifier Differential Inputs	V _{ref} (D)	±5.0	Vdc
Operating Temperature Range	T _A	0 to +70	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C
Junction Temperature	T _J	+130	°C
Thermal Resistance, Junction to Ambient	Still Air With 500 LFPM R _{θJA}	67 50	°C/W

DC CHARACTERISTICS (V_{EE} = -5.2 V, ±5% T_A = 0°C to +70°C after thermal equilibrium is reached.)

Characteristics	Fig.	Symbol	Min	Typ	Max	Unit
Nonlinearity (Integral) (Pin 14 or 15) (@ I _{FS} = 51 mA, 25.5 mA)		—	—	—	±0.19	%FS
Zero Scale Output Current (Pin 14 or 15) (T _A = 25°C)	10	I _{ZS}	—	5.0	50	μA
Zero Scale Output Current Temperature Drift (Pin 14 or 15) 0 < T _A < 25°C 25°C < T _A < 70°C		I _{ZS} ΔT	— —	±17 ±2.0	—	nA/°C
Full Scale Output Current (Pin 14 or 15) (I _{ref} = 3.2 mA, D0-D7 = 1)	10	I _{FS}	-46	-51	-56	mA
Full Scale Output Current Temperature Drift (Pin 14 or 15) 0 < T _A < 25°C 25°C < T _A < 70°C		ΔI _{FS} /°C	— —	±50 ±10	—	ppm/°C
Full Scale Output Sensitivity to Power Supply Variations (Pin 14 or 15) (-4.94 V < V _{EE} < -5.46 V)		I _{FS} PSS	—	±0.005	±0.02	%/%
Full Scale Symmetry (I _{FS} — I _{FS})	10	I _{FSS}	—	±21	±100	μA
Output Voltage Compliance (Pin 14 or 15) Full Scale Current Change ≤ 1/2 LSB (Specified Nonlinearity) (T _A = 25°C)		V _{OC}	-1.3	—	+2.5	V
Output Resistance (Pin 14 or 15) (T _A = 25°C)	12	R _O	—	69	—	kΩ
Reference Amplifier Offset Voltage (T _A = 25°C)		V _{IO}	—	±3.2	—	mV
Reference Amplifier Offset Voltage Temperature Drift 0 < T _A < 25°C 25°C < T _A < 70°C		ΔV _{IO} /ΔT	— —	±10 ±4.0	—	μV/°C
Reference Amplifier Bias Current (Pin 10) (I _{ref} = 3.2 mA)		I _{IB}	—	4.0	15	μA
Reference Amplifier Bias Current Temperature Drift (I _{ref} = 3.2 mA) 0 < T _A < 25°C 25°C < T _A < 70°C		ΔI _{IB} /ΔT	— —	-40 -10	—	nA/°C
Reference Amplifier Common Mode Range (V _{EE} = -5.2 V) (T _A = 25°C)		V _{ICR}	—	±1.15	—	V
Reference Amplifier Common Mode Rejection Ratio (T _A = 25°C) (I _{ref} = 3.2 mA, V _{ICR} = 0 to -2.0 V, Pins 1-8 = Logic 1)		V _{ICMRR}	—	58	—	dB
Reference Amplifier Input Impedance (Pin 10) (T _A = 25°C)		R _{IN}	—	1.0	—	MΩ
Power Supply Current (Pins 1 thru 8 Open, I _{ref} = 3.2 mA, Includes I _O + I _{IO})		I _{EE}	—	90	130	mA

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MC10318P

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{EE} = -5.2\text{ V}$, $\pm 5\%$)

Characteristics	Fig.	Symbol	Min	Typ	Max	Unit
Feedthrough Current — All Bits Off $f = 10\text{ kHz}$ $f = 100\text{ kHz}$	9	I_{FC}	— —	2.0 18	— —	$\mu\text{A p-p}$
Distortion — (ωI_O) (Sinewave applied to reference amplifier Input, D0–D7 = Logic 1) $C = 0.01\text{ }\mu\text{F}$, $f = 20\text{ kHz}$ $C = 0.01\text{ }\mu\text{F}$, $f = 65\text{ kHz}$ $C = 0.001\text{ }\mu\text{F}$, $f = 340\text{ kHz}$ $C = 0.001\text{ }\mu\text{F}$, $f = 600\text{ kHz}$ $C = 240\text{ pF}$, $f = 600\text{ kHz}$		THD THD THD THD THD	— — — — —	1.0 5.0 1.0 2.0 0.8	— — — — —	%
Reference Amplifier Slew Rate (Step change at Pin 10, all bits on) $C = 0.01\text{ }\mu\text{F}$ $C = 0.001\text{ }\mu\text{F}$ $C = 240\text{ pF}$	13		— — —	0.5 5.0 20	— — —	$\text{mA }\mu\text{s}$
Settling Time (to $\pm 0.19\%$ of Full Scale) 1 LSB Change All Bits Switched	1,22	t_s	— —	7.0 10	— —	ns
Propagation Delay	2	t_p	—	5.0	—	ns
Output Glitch Energy (with De-Skewing Capacitors) (Input Change: 01111111 \longleftrightarrow 10000000)			—	50	—	LSB-ns
Glitch Duration			—	5.0	—	ns

DIGITAL INPUT VOLTAGE LEVELS				
Volts (See Note)				
T_A	V_{IHmax}	V_{IHmin}	V_{ILmax}	V_{ILmin}
0°C	-0.845	-1.151	-1.516	-1.868
25°C	-0.810	-1.105	-1.505	-1.850
70°C	-0.727	-1.052	-1.480	-1.830

FUNCTIONAL PIN DESCRIPTION

D0–D7 (Pins 1–8) The eight ECL digital inputs compatible with MECL 10,000 series devices. Logic "0" is nominally -1.8 V, and Logic "1" is nominally -0.9 V.

V_{ref} (Pin 10) The high impedance input of the reference amplifier. This input is normally grounded, but may be used for ac applications involving modulation, digitally controlled gain, etc. Normal operating range is from ground to $V_{EE} - 2.9\text{ V}$ (nominally -2.3 V).

V_{ref} (Pin 12) The noninverting input of the reference amplifier. The inverted output of the reference amplifier is internally fed back to this input, thus causing it to track Pin 10. A nominal 3.2 mA is to be supplied to this pin from an external (stable and noise free) voltage source and current setting resistor.

Comp. (Pin 11) A nominal 0.01 μF capacitor is connected to this pin and to ground to stabilize the reference amplifier. Lower values of capacitor may be used if a good PC board layout is used, where frequencies higher than 10 kHz are applied to the reference amplifier.

I_O , $I_{\bar{O}}$ (Pins 14,15) The complementary current outputs. Current flow is into the DAC and varies linearly with I_{ref} and the digital input code. I_{out} increases as the digital input increases. Output compliance range is -1.3 V to +2.5 V.

V_{EE} (Pin 9) The power supply pin. V_{EE} is nominal -5.2 V, $\pm 5\%$.

Gnd (Pin 16) The ground pin. This line should be as noise-free as possible in order to obtain a noise-free output.

NOTE: $V_{EE} = -5.2\text{ V}$, $\pm 5\%$. Inputs are MECL 10,000 compatible within the temperature and power supply ranges listed. See MECL System Design Handbook for further details. See Fig. 19 in this data sheet.

FIGURE 1 — SETTLING TIME

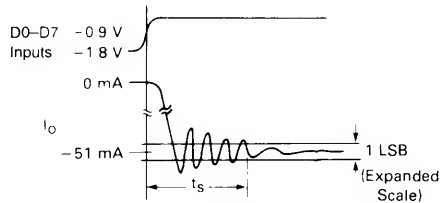
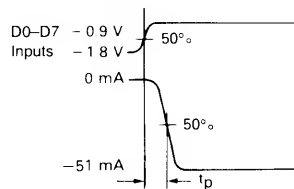


FIGURE 2 — PROPAGATION DELAY



REFERENCE AMPLIFIER RESPONSE

Inverting Input (V_{ref-})
Test Circuit of Fig. 14

Noninverting Input (V_{ref+})
Test Circuit of Fig. 11

FIGURE 3 — FREQUENCY RESPONSE

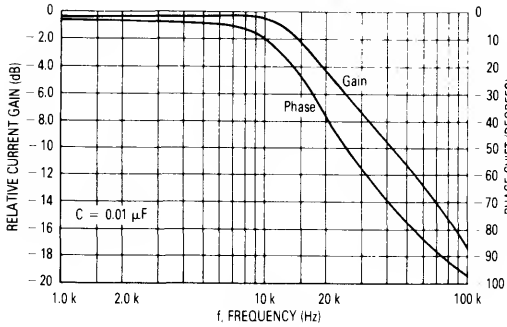


FIGURE 6 — FREQUENCY RESPONSE

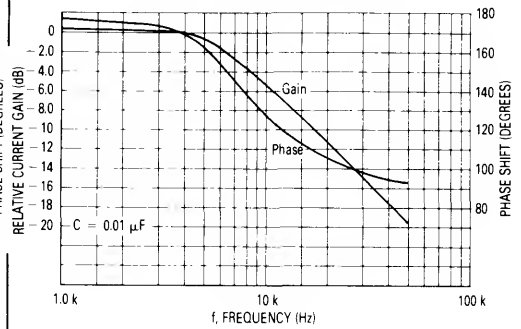


FIGURE 4 — FREQUENCY RESPONSE

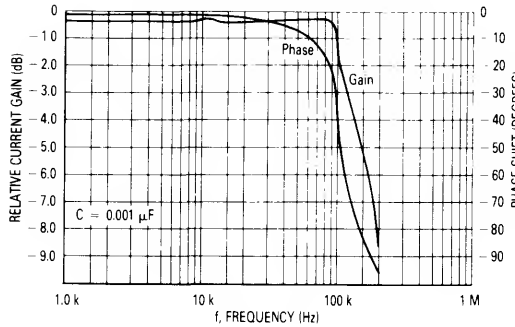


FIGURE 7 — FREQUENCY RESPONSE

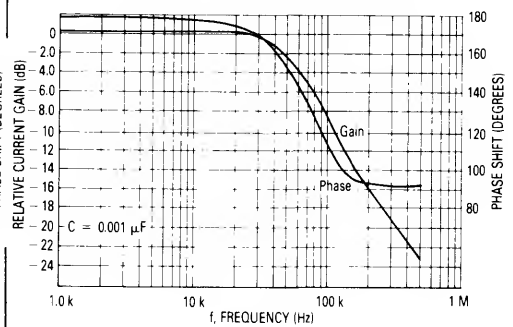


FIGURE 5 — FREQUENCY RESPONSE

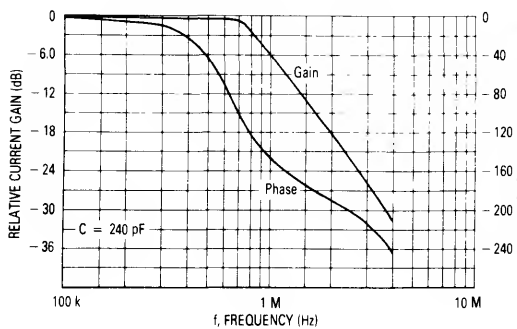
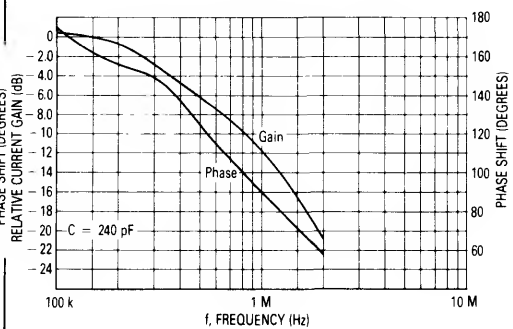


FIGURE 8 — FREQUENCY RESPONSE



MC10318P

TEST CIRCUITS

FIGURE 9 — FEEDTHROUGH MEASUREMENT

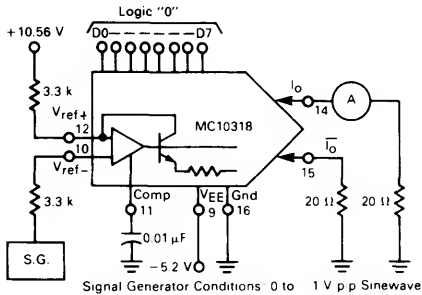


FIGURE 10 — ZERO/FULL SCALE CURRENT

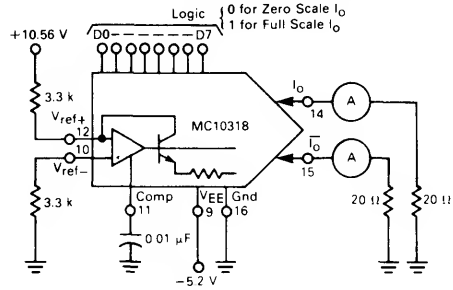
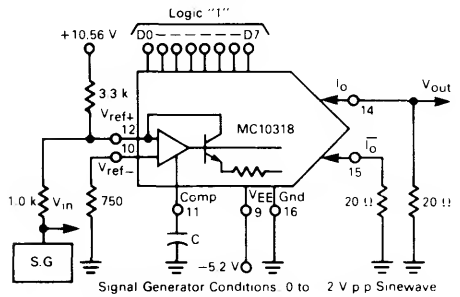


FIGURE 11 — GAIN/PHASE MEASUREMENT



Reference dB Level: See Text

See Figures 6-8

FIGURE 12 — OUTPUT RESISTANCE

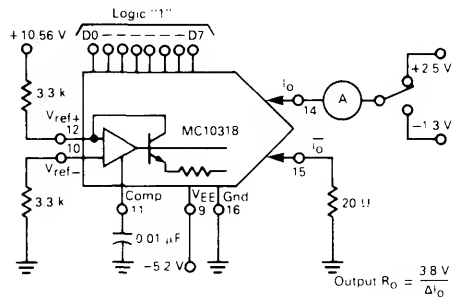


FIGURE 13 — REFERENCE AMPLIFIER SLEW RATE

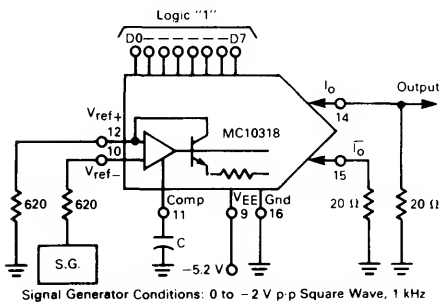
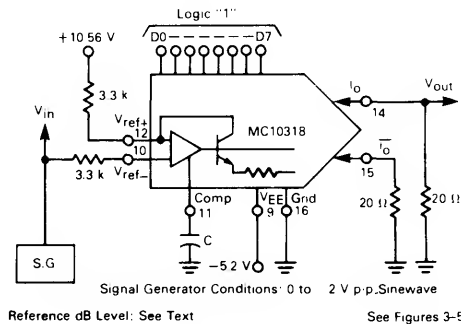


FIGURE 14 — GAIN/PHASE MEASUREMENT



OPERATIONAL INFORMATION

Typical DAC Operation

The MC10318 is designed to be operated with an I_{ref} (Pin 12) of 3.2 mA, resulting in a full scale output current (I_O) of 51 mA when D0 through D7 are at a Logical "1" (-0.9 V). The transfer equation for I_O is therefore:

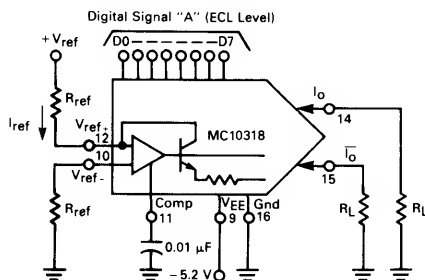
$$I_O = I_{ref} \times 16 \times \frac{A}{256}$$

("A" is the binary value of the digital input).

Typically V_{ref} (Pin 10) is connected to Ground, and I_{ref} is supplied to V_{ref} (Pin 12) by means of an external supply V_r (See Figure 15). A resistor inserted between Pin 10 and Ground will minimize temperature drift, and should have a value equivalent to that connected to Pin 12. Any noise or ripple present on the reference current will be present on the output current, and the stability of the reference directly affects the output current's stability. The ground connection for V_{ref} should be chosen with care so as not to pick up noise (digital or otherwise).

The complementary outputs (I_O and \bar{I}_O) are high impedance current sources having a compliance range of 3.8 V (-1.3 to -2.5 V). I_O increases with increasing digital input, while \bar{I}_O decreases. Their sum is a constant equal to $15.94 \times I_{ref}$. Neither output can be left open — an unused output must be connected to ground or a load resistor. Typically both outputs should be loaded similarly for best speed and accuracy performance. A compensation capacitor must be connected between Pin 11 and Ground to stabilize the amplifier. A $0.01 \mu\text{F}$ ceramic is satisfactory for most applications, and should be located physically close to the device. The ground side of the capacitor should be noise-free. When operated as above, the output(s) will be controlled by the digital inputs, and the MC10318 can be used for various functions such as waveform generation, process control, ADC conversion, and others.

FIGURE 15 — TYPICAL OPERATION



Common Mode Range — AC Operation

The reference amplifier inputs (Pins 10 and 12) may be used to control the output current in conjunction

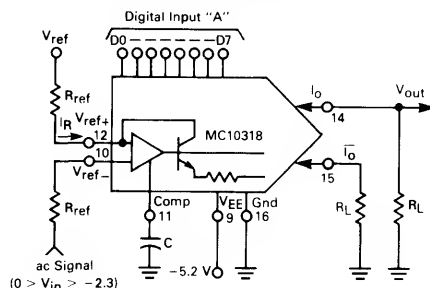
with the digital inputs for applications such as digitally controlled gain of an ac signal, digitally controlled amplitude modulation, and others. Either the positive or negative input of the reference amplifier may be used, depending on the application. There are, however, differences in the manner in which an ac signal is to be applied.

1) When applying a signal to the V_{ref} (Pin 10) input (See Figure 16), the signal must be kept within the range of 0 to -2.3 V. The input has a high impedance (typically 1 Megohm). The V_{ref} pin (Pin 12) will track this signal, causing I_{ref} to vary, in turn causing I_O and \bar{I}_O to vary. The ac component of I_O (and \bar{I}_O) will be in phase with the applied signal. The ac gain of the circuit shown is:

$$\frac{\Delta V_{out}}{\Delta V_{in}} = \frac{A \times R_L}{16 \times R_R}$$

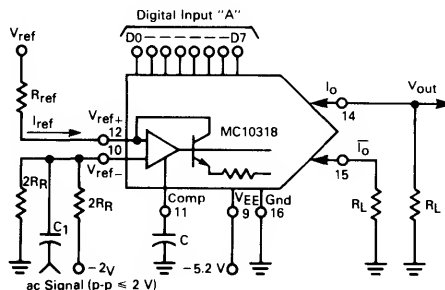
Applying the above to the test circuit of Figure 14 yields a gain of 0.0966, which is the 0 dB reference level for the curves of Figures 3-5.

FIGURE 16 — AC OPERATION, NONINVERTING



If the peak values of the applied ac signal cannot be kept within the above mentioned voltage range, an alternate circuit is shown in Figure 17.

FIGURE 17 — AC OPERATION, NONINVERTING (ALTERNATE)



The compensation capacitor (Pin 11) of Figures 16 and 17 is to be nominally $0.01 \mu\text{F}$ for best overall stability. If frequencies higher than 10 kHz are to be applied to the reference input, a smaller value capacitor will be necessary as indicated by Figures 3-5. However, greater care will be necessary in the breadboarding and PC layout to prevent instabilities caused by unintended feedback paths.

2) When applying a signal to the V_{ref} (Pin 12) input (see Figure 18), the effect is a direct modulation of the reference current supplied by V_{ref} . Pin 12 is a virtual ground, and therefore the current I_{ref} is equal to:

$$I_{\text{ref}} = \frac{V_{\text{ref}} + V_i}{R_{\text{ref}} + R_i}$$

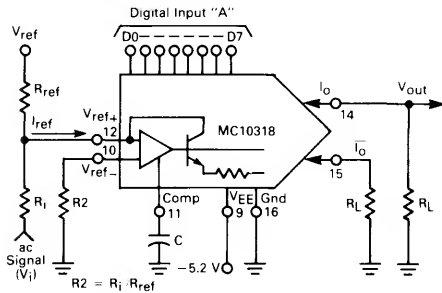
I_O and \bar{I}_O will vary with the reference current, but the ac component will be 180° out of phase with the applied signal. The ac gain of the circuit shown is:

$$\frac{\Delta V_{\text{out}}}{\Delta V_i} = \frac{-A \times R_L}{16 \times R_i}$$

Applying the above to the test circuit of Figure 11 yields a gain of -0.3188 , which is the 0 dB reference level for the curves of Figures 6-8.

The reference current I_{ref} must always flow into Pin 12, requiring that the values of V_{ref} , R_{ref} , R_i , and V_i be chosen so as to guarantee this.

FIGURE 18 — AC OPERATION, INVERTING



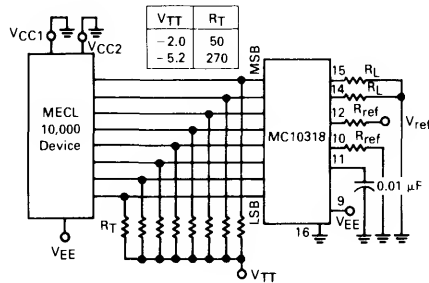
The compensation capacitor (Pin 11) of Figure 18 is to be nominally $0.01 \mu\text{F}$ for best overall stability. If frequencies higher than 4 kHz are to be applied, a smaller value capacitor will be necessary as indicated by Figures 6-8. However, greater care will be necessary in the breadboarding and PC layout to prevent instabilities caused by unintended feedback paths.

DIGITAL INTERFACE

The digital inputs (Pins 1-8) are compatible with MECL 10,000 series devices over the temperature and V_{EE} range listed on page 3. Standard MECL 10,000 de-

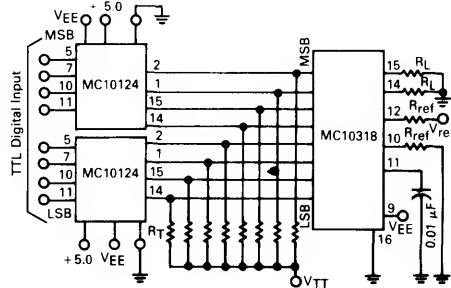
sign guidelines apply, and should be implemented. Maximum speed response requires careful PC board layout and choice of components. See Motorola's MECL System Design Handbook for a complete explanation of specifications and characteristics. Figure 19 shows a typical ECL interconnection with recommended values for optimum speed performance. Other values of R_T and V_{TT} may be used, but at a slight increase in overall propagation delay. Unused inputs should not be left open, but should be connected to a Logic 0 (-1.8 V), or a Logic 1 (-0.9 V). Resistors R_T should be connected at the receiving end of the interconnection, i.e. physically located adjacent to the MC10318 inputs, for best speed performance.

FIGURE 19 — STANDARD MECL INTERFACE



Interfacing a TTL system to the MC10318 is easily accomplished by the use of two MC10124 devices (see Figure 20).

FIGURE 20 — TTL INTERFACE



OUTPUT CHARACTERISTICS

The MC10318 DAC has been designed specifically for high speed operation by incorporating ECL structured inputs, bit switching circuits which are small in size and

simple in operation, and high-current complementary outputs (which permits current steering rather than on-off switching). In this manner, very short propagation delays and settling times are possible.

Output Glitch

All DAC's will produce a glitch at the output when various bits are switched in opposite directions, due to differences in transition times of the switching transistors. During the switching period, typically the output current will momentarily seek a value other than the desired final value, and then return to and settle at the final value. This glitch can be several LSBs in magnitude, but of a very short duration (5–6 ns). In some instances, the output current may overshoot, and then undershoot before reaching the final value, resulting in a "glitch doublet."

The glitch is most apparent when switching the higher order bits, and in the case of the MC10318, the maximum glitch generally occurs when switching bit D5 and the lower 5 bits (typically 85 LSB-ns). Switching bit D6 and the lower 6 bits produces a similar but slightly reduced glitch. Switching bit D7 and the seven lower bits (major carry transition) results in a glitch of typically 50 LSB-ns, with an amplitude of 17 LSBs. Switching of lower order bits while maintaining the higher ones constant produces glitches typically of less than 1 LSB in magnitude, and less than 10 ns in duration, and are generally not considered to be of significance.

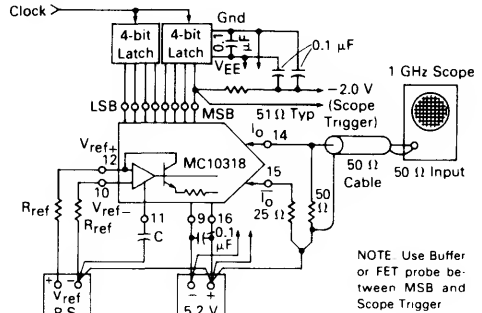
Glitches can be removed from the output by filtering, or by using a sample-and-hold circuit on the output, or by using de-skewing capacitors on the higher order bits.

Output glitch is generally specified in terms of glitch energy, which is the area under the curve of the waveform. Most glitches appear as a triangle, and so the area is simply $\frac{1}{2} \times t \times \Delta I$, where t is the duration of the glitch, and ΔI is the amplitude normalized in terms of LSBs. In the case of a glitch doublet, having both positive and negative amplitude, the areas are summed algebraically. It is possible, therefore to have a glitch with zero energy, although having amplitudes of several LSB's.

In applications where the output glitch is of concern, steps can be taken to minimize its magnitude. The two main factors to consider are: 1) That the 8 bits of data reach the MC10318 simultaneously; and 2) that the PC board layout prevent noise from reaching the MC10318.

It is obvious that if the updated 8 bits are not received by the DAC simultaneously, even an ideal DAC will not produce an ideal waveform. Where simultaneous transmission by the sending device(s) cannot be guaranteed (such as two cascaded counters), latches should be used ahead of the MC10318. The latches should then be clocked after their inputs have settled. Suggested latches are the MC10133/MC10153/MC10168 at the ECL level, and the SN74LS273 at the TTL level.

FIGURE 21 — PRECISION HIGH-SPEED MEASUREMENTS



Nonlinearity

Integral nonlinearity has been specified, rather than differential nonlinearity, as this is a better indicator of the maximum error to be expected. Integral nonlinearity is measured by comparing the **actual** output (at each digital value) with the expected ideal value. The expected values lie along a straight line between zero and the full scale output current. The MC10318 will not differ from the **ideal** value by more than the specified nonlinearity.

PC Board Layout

A proper PC board layout is very important in order to obtain the full benefits of the MC10318's high-speed characteristics. Each of the current paths (I_O , \bar{I}_O , I_{EE} , I_{ref} , etc.) must be carefully considered to avoid interference, and isolation from other circuits on the board (particularly digital) is essential. Bypassing of all supplies is, of course, necessary, and in some cases, bypassing to V_{EE} may be more beneficial than bypassing to Ground. Sockets should be avoided as the extra pin-to-pin capacitance can slow down the ECL edges and/or the output settling time. PC board layout should include the following guidelines:

- 1) A dedicated ground track from the power supply to Pin 16 (Gnd);
- 2) A single dedicated ground track from the power supply to the **two** load resistors associated with I_O and \bar{I}_O — this results in a constant dc current in this track;
- 3) A separate ground for the circuitry associated with V_{ref+} , V_{ref-} , and Comp (Pins 10–12). Any noise on this ground will feed through the reference amplifier and show up on the output;
- 4) The compensation capacitor must be physically adjacent to Pin 11;
- 5) Bypass V_{EE} (Pin 9) with a 0.1 μF to the ground line feeding the load resistors;
- 6) Provide proper terminations at the inputs — the suggested values for R_T and V_{TT} will provide best speed response;

6

- 6

Settling Time

The settling time is defined as the time from the 50% point of the input transition to the point at which the output enters into and stays within $\pm 1/2$ LSB (the error band) of the final value. Minimum settling time occurs when the output enters the error band at the maximum slew rate, and then settles out within the band. In actuality, however, the output's slew rate will lessen prior to entering the error band, and then may exit and enter the band once or twice as it settles to its final value. The settling time is determined by the last time the output enters the error band. See Figure 1.

When testing for settling time, the measurement technique used will have an effect on the result. Simply connecting scope probes to an input and output is generally not satisfactory due to the capacitive loading (typically 10–20 pF) of the probes. The rise (fall) time of an ECL input can be significantly increased by such a probe, with the result that the inputs of the MC10318 may be skewed from each other, which, in turn, affects the output. However, probes with low input capacitance, on the order of 2 pF or less (such as FET probes), can be used with very little degradation of the waveforms. The overall propagation delay of the probe (from tip to scope input) must be taken into account, as this can be on the order of 10 ns.

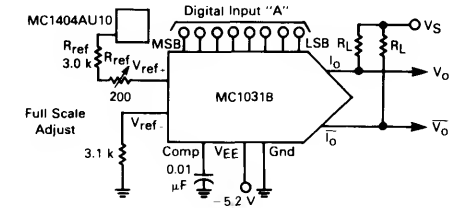
When attempting to view the output on a scope, several factors need to be considered. If the output swing is a full scale transition (e.g., 1.0 V), 1 LSB is 3.9 mV. The scope's amplifier must then be set at a sensitive range (5 mV/cm or 10 mV/cm), with the result that the scope's amplifier will be saturated when the MC10318's output is at the initial value. When the device inputs are switched, the output approaches the final value, but the scope's amplifier will require some time to come out of saturation, and then may overshoot, causing a false indication. In order to overcome this problem, the MC10318 was tested for settling time by connecting the output to a dual high-speed comparator configured as a window detector. The window is 1 LSB wide, centered about the final value. The outputs of the comparators are then monitored on a scope, as they indicate when the MC10318 output is settled within the error band. Propagation delays of the comparators, scope probes, and cable lengths are taken into account. See Figure 22. This method of monitoring the DAC's output, although indirect, does not cause changes to the output waveform because of probe loading, characteristics of the scope, or noise which the probe (and cable) may pick up.

APPLICATIONS

Voltage Output

There are two methods of converting the current output of the MC10318 to voltage outputs, depending on the voltage swing desired. For a limited range (<3.8 V p-p) the circuit of Figure 23 can be used.

FIGURE 23 — VOLTAGE OUTPUT

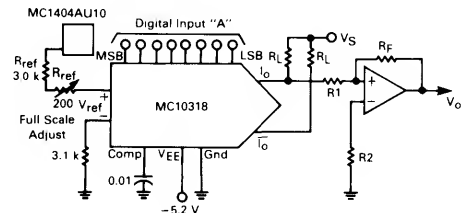


V _S	R _L	V _O	V _O
0 V	25.5	0 to -1.3 V	-1.3 V to 0 V
+2.5	49	+2.5 to 0 V	0 to +2.5 V
+2.5	74.5	+2.5 to -1.3 V	-1.3 to +2.5 V
+1.0	39	+1.0 to -1.0 V	-1.0 to +1.0 V

$$V_O = -\frac{V_{ref} \times A \times R_L}{R_{ref} \times 16} + V_S$$

Where a larger voltage swing is required, an op amp is required at the output. The choice of op amp will be based on whether accuracy or speed is of primary importance. Where repeatable and stable accuracy is required, the op amp characteristics to consider are open-loop gain, offset voltage, bias current, and temperature drift. Where speed is paramount, a wideband amplifier should be used. Slew rate, propagation delay, and settling time of the op amp are the primary factors to evaluate. The PC board should be designed for high frequency operation, possibly using Microstrip or Stripline techniques. See Figure 24 for a suggested circuit.

FIGURE 24 — VOLTAGE OUTPUT



R _{ref}	R _L	V _S	R ₁	R _F	V _O
3125	20	0	1.0 k	5.0 k	0 to +5
3125	20	0	1.0 k	10 k	0 to +10
3125	40	+1.02	2.0 k	10 k	-5 to +5
3125	40	+1.02	2.0 k	20 k	-10 to +10

$$V_O = \frac{V_{ref} \times A \times R_L \times R_F}{R_{ref} \times 16 \times (R_1 + R_L)} - \frac{V_S \times R_F}{(R_1 + R_L)}$$

Connecting I_O and \bar{I}_O as shown in the above figures places a constant dc load (51 mA) on the V_S supply, thus facilitating its design. The Gain Adjust resistor should be a 20 turn trimpot, as this will result in one turn equaling approximately 1 LSB of adjustment (for the recommended values in the figure). All of the resistors should have similar temperature coefficients for best temperature stability.

MC10318P

WAVEFORM GENERATION

FIGURE 25 — SAWTOOTH GENERATOR

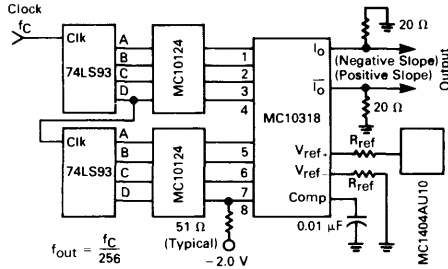


FIGURE 26 — TRIANGLE GENERATOR

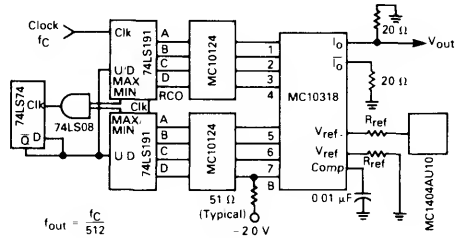


FIGURE 27 — SINEWAVE GENERATOR

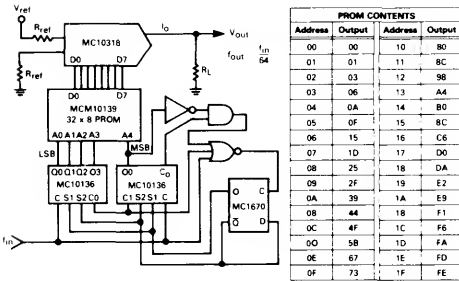
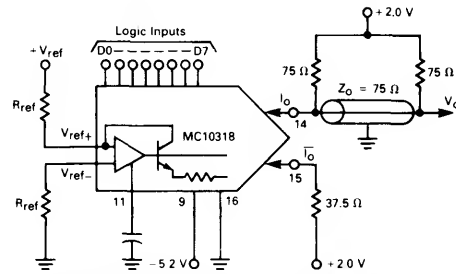
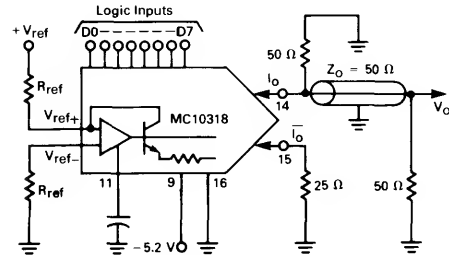


FIGURE 28 — OUTPUT CONNECTED TO 75 Ω LINE



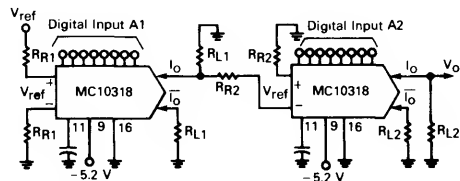
NOTE: Terminating Resistors and Z_0 must be matched to within 0.4% to keep initial reflection below 1/2 LSB in magnitude.

FIGURE 29 — OUTPUT CONNECTED TO 50 Ω LINE



NOTE: Terminating Resistors and Z_0 must be matched to within 0.4% to keep initial reflection below 1/2 LSB in magnitude.

FIGURE 30 — DIGITAL MULTIPLICATION



Suggested Values	
V_{ref}	-1.0 V
R_{R1}	3079*
R_{L1}	20
R_{R2}	330
R_{L2}	20

$$V_o = -\frac{A1 \times A2 \times V_{ref} \times R_{L1} \times R_{L2}}{R_{R1} \times R_{R2} \times 256}$$

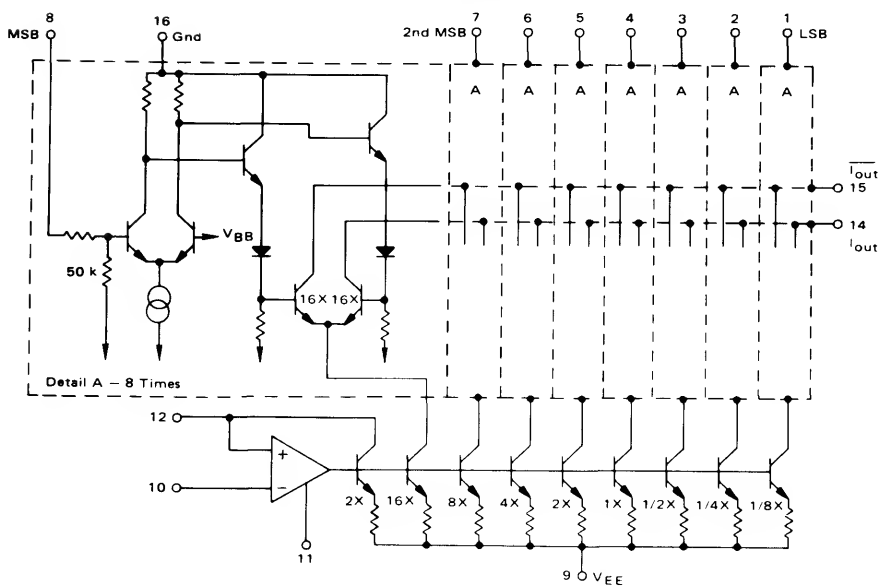
(With suggested values, V_o range is 0 to -1.0 V)

* 3.0 k Resistor + 100 Ω Tmpot

NOTES:

- When generating waveforms at low frequencies, filtering the output is recommended to smooth out the steps.
- In many applications, bipolar voltage output may be obtained by monitoring the differential voltage at Pins 14 and 15 (with equal load resistors).
- When connecting the outputs to transmission lines (See Figures 28 and 29), proper transmission line theory and techniques must be used for optimum performance.

FIGURE 31 — MC10318 EQUIVALENT CIRCUIT



HIGH SPEED
8-BIT ANALOG-TO-DIGITAL CONVERTER

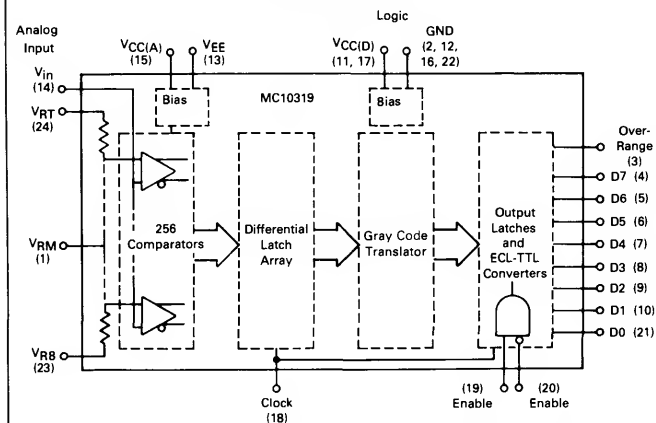
The MC10319 is an 8-bit high speed parallel flash A/D converter. The device employs an internal Gray Code structure to eliminate large output errors on fast slewing input signals. It is fully TTL compatible, requiring a +5.0 V supply and a wide tolerance negative supply of -3.0 to -6.0 V. Three-state TTL outputs allow direct drive of a data bus or common I/O memory.

The MC10319 contains 256 parallel comparators across a precision input reference network. The comparator outputs are fed to latches and then to an encoder network, to produce an 8-bit data byte plus an overrange bit. The data is latched and converted to 3-state LS-TTL outputs. The overrange bit is always active to allow for either sensing of the overrange condition or ease of interconnecting a pair of devices to produce a 9-bit A/D converter.

Applications include Video Display and Radar processing, high speed instrumentation and TV Broadcast encoding.

- Internal Gray Code for Speed and Accuracy, Binary Outputs
- 8-Bit Resolution/9-Bit Typical Accuracy
- Easily Interconnected for 9-Bit Conversion
- 3-State LS-TTL Outputs with True and Complement Enable Inputs
- 25 MHz Sampling Rate
- Wide Input Range: 1.0-2.0 V_{p-p} Between ± 2.0 V
- Low Input Capacitance: 60 pF
- Low Power Dissipation: 618 mW
- No Sample/Hold Required for Video Bandwidth Signals
- Single Clock Cycle Conversion

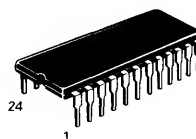
BLOCK DIAGRAM



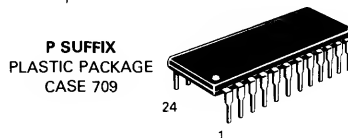
MC10319

HIGH SPEED
8-BIT ANALOG-TO-DIGITAL
FLASH CONVERTER

SILICON MONOLITHIC
INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 623

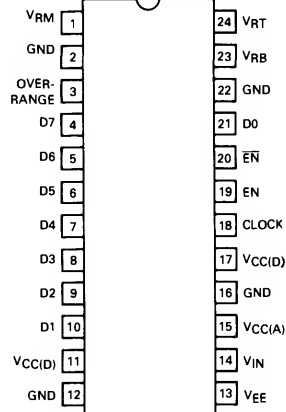


P SUFFIX
PLASTIC PACKAGE
CASE 709



DW SUFFIX
PLASTIC PACKAGE
CASE 751E
SO-24L

PIN DIAGRAM
(L and P only)



ORDERING INFORMATION

Device	Temperature Range	Package
MC10319DW	0° to +70°C	SO-24L
MC10319L		Ceramic
MC10319P		Plastic

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Supply Voltage	$V_{CC(A),(D)}$ V_{EE}	+ 7.0 − 7.0	Vdc
Positive Supply Voltage Differential	$V_{CC(D)} - V_{CC(A)}$	− 0.3 to + 0.3	Vdc
Digital Input Voltage (Pins 18–20)	$V_{I(D)}$	− 0.5 to + 7.0	Vdc
Analog Input Voltage (Pins 1, 14, 23, 24)	$V_{I(A)}$	− 2.5 to + 2.5	Vdc
Reference Voltage Span (Pin 24–Pin 23)	—	2.3	Vdc
Applied Output Voltage (Pins 4–10, 21 in 3-State)	—	− 0.3 to + 7.0	Vdc
Junction Temperature	T_J	+ 150	°C
Storage Temperature	T_{stg}	− 65 to + 150	°C

Devices should not be operated at these values. The "Recommended Operating Limits" provide guidelines for actual device operation.

RECOMMENDED OPERATING LIMITS

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage (Pin 15) (Pins 11, 17)	$V_{CC(A)}$ $V_{CC(D)}$	+ 4.5	+ 5.0	+ 5.5	Vdc
$V_{CC(D)} - V_{CC(A)}$	ΔV_{CC}	− 0.1	0	+ 0.1	Vdc
Power Supply Voltage (Pin 13)	V_{EE}	− 6.0	− 5.0	− 3.0	Vdc
Digital Input Voltages (Pins 18–20)	$V_{I(D)}$	0	—	+ 5.0	Vdc
Analog Input (Pin 14)	$V_{I(A)}$	− 2.1	—	+ 2.1	Vdc
Voltage @ V_{RT} (Pin 24)	V_{RT}	− 1.0	—	+ 2.1	Vdc
Voltage @ V_{RB} (Pin 23)	V_{RB}	− 2.1	—	+ 1.0	Vdc
$V_{RT} - V_{RB}$	ΔV_R	+ 1.0	—	+ 2.1	Vdc
$V_{RB} - V_{EE}$	—	1.3	—	—	Vdc
Applied Output Voltage (Pins 4–10, 21 in 3-State)	V_O	0	—	5.5	Vdc
Clock Pulse Width — High Low	t_{CKH} t_{CKL}	5.0 15	20 20	— —	ns
Clock Frequency	f_{CLK}	0	—	25	MHz
Operating Ambient Temperature	T_A	0	—	+ 70	°C

ELECTRICAL CHARACTERISTICS ($0^\circ < T_A < 70^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$, $V_{EE} = -5.2\text{ V}$, $V_{RT} = +1.0\text{ V}$, $V_{RB} = -1.0\text{ V}$, except where noted.)

Parameter	Symbol	Min	Typ	Max	Unit
TRANSFER CHARACTERISTICS ($f_{CKL} = 25\text{ MHz}$)					
Resolution	N	—	—	8.0	Bits
Monotonicity	MON	Guaranteed			Bits
Integral Nonlinearity	INL	—	$\pm 1/4$	± 1.0	LSB
Differential Nonlinearity	DNL	—	—	± 1.0	LSB
Differential Phase (See Figure 16)	DP	—	1.0	—	Deg.
Differential Gain (See Figure 16)	DG	—	1.0	—	%
Power Supply Rejection Ratio ($4.5\text{ V} < V_{CC} < 5.5\text{ V}$, $V_{EE} = -5.2\text{ V}$) ($-6.0\text{ V} < V_{EE} < -3.0\text{ V}$, $V_{CC} = +5.0\text{ V}$)	PSRR	— —	0.1 0	— —	LSB/V

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ELECTRICAL CHARACTERISTICS — continued ($0^\circ < T_A < 70^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$, $V_{EE} = -5.2\text{ V}$, $V_{RT} = +1.0\text{ V}$, $V_{RB} = -1.0\text{ V}$, except where noted.)

Parameter	Symbol	Min	Typ	Max	Unit
ANALOG INPUT (PIN 14)					
Input Current ($\alpha V_{in} = V_{RB}$ (See Figure 5))	I_{INL}	-100	0	—	μA
Input Current ($\alpha V_{in} = V_{RT}$ (See Figure 5))	I_{INH}	—	60	150	μA
Input Capacitance ($V_{RT} - V_{RB} = 2.0\text{ V}$, See Figure 4)	C_{in}	—	36	—	pF
Input Capacitance ($V_{RT} - V_{RB} = 1.0\text{ V}$, See Figure 4)	C_{in}	—	55	—	pF
Bipolar Offset Error	V_{OS}	—	0.1	—	LSB

REFERENCE

Ladder Resistance (V_{RT} to V_{RB} , $T_A = 25^\circ\text{C}$)	R_{ref}	104	130	156	Ω
Temperature Coefficient	T_C	—	+0.29	—	$\%^\circ\text{C}$
Ladder Capacitance (Pin 1 open)	C_{ref}	—	25	—	pF

ENABLE INPUTS ($V_{CC} = 5.5\text{ V}$) (See Figure 6)

Input Voltage — High (Pins 19–20)	V_{IHE}	2.0	—	—	V
Input Voltage — Low (Pins 19–20)	V_{ILE}	—	—	0.8	V
Input Current ($\alpha 2.7\text{ V}$)	I_{IHE}	—	0	20	μA
Input Current ($\alpha 0.4\text{ V}$ ($\alpha \overline{EN}$ ($0 < EN < 5.0\text{ V}$))	I_{IL1}	-400	-100	—	μA
Input Current ($\alpha 0.4\text{ V}$ (αEN ($\overline{EN} = 0\text{ V}$))	I_{IL2}	-400	-100	—	μA
Input Current ($\alpha 0.4\text{ V}$ (αEN ($\overline{EN} = 2.0\text{ V}$))	I_{IL3}	-20	-2.0	—	μA
Input Clamp Voltage ($I_{IK} = -18\text{ mA}$)	V_{IKE}	-1.5	-1.3	—	V

CLOCK INPUT ($V_{CC} = 5.5\text{ V}$)

Input Voltage High	V_{IHC}	2.0	—	—	Vdc
Input Voltage Low	V_{ILC}	—	—	0.8	Vdc
Input Current ($\alpha 0.4\text{ V}$ (See Figure 7))	I_{ILC}	-400	-80	—	μA
Input Current ($\alpha 2.7\text{ V}$ (See Figure 7))	I_{IHC}	-100	-20	—	μA
Input Clamp Voltage ($I_{IK} = -18\text{ mA}$)	V_{IKC}	-1.5	-1.3	—	Vdc

DIGITAL OUTPUTS

High Output Voltage ($I_{OH} = -400\text{ }\mu\text{A}$, $V_{CC} = 4.5\text{ V}$, See Figure 8)	V_{OH}	2.4	3.0	—	V
Low Output Voltage ($I_{OL} = 4.0\text{ mA}$, See Figure 9)	V_{OL}	—	0.35	0.4	V
Output Short Circuit Current* ($V_{CC} = 5.5\text{ V}$)	I_{SC}	—	35	—	mA
Output Leakage Current ($0.4 < V_O < 2.4\text{ V}$, See Figure 3, $V_{CC} = 5.5\text{ V}$, D0–D7 in 3-State Mode)	I_{LK}	-50	—	+50	μA
Output Capacitance (D0–D7 in 3-State Mode)	C_{out}	—	9.0	—	pF

*Only one output is to be shorted at a time, not to exceed 1 second.

POWER SUPPLIES

$V_{CC(A)}$ Current ($4.5\text{ V} < V_{CC(A)} < 5.5\text{ V}$) (Outputs unloaded)	$I_{CC(A)}$	10	17	25	mA
$V_{CC(D)}$ Current ($4.5\text{ V} < V_{CC(D)} < 5.5\text{ V}$) (Outputs unloaded)	$I_{CC(D)}$	50	90	133	mA
V_{EE} Current ($-6.0\text{ V} < V_{EE} < -3.0\text{ V}$)	I_{EE}	-14	-10	-6.0	mA
Power Dissipation ($V_{RT} - V_{RB} = 2.0\text{ V}$) (Outputs unloaded)	P_D	—	618	995	mW

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TIMING CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{CC} = +5.0\text{ V}$, $V_{EE} = -5.2\text{ V}$, $V_{RT} = +1.0\text{ V}$, $V_{RB} = -1.0\text{ V}$,
See System Timing Diagram.)

Parameter	Symbol	Min	Typ	Max	Unit
INPUTS					
Min Clock Pulse Width — High	t_{CKH}	—	5.0	—	ns
Min Clock Pulse Width — Low	t_{CKL}	—	15	—	ns
Max Clock Rise, Fall Time	$t_{R,F}$	—	100	—	ns
Clock Frequency	f_{CLK}	0	30	25	MHz
OUTPUTS					
New Data Valid from Clock Low	t_{CKDV}	—	19	—	ns
Aperture Delay	t_{AD}	—	4.0	—	ns
Hold Time	t_H	—	6.0	—	ns
Data High to 3-State from Enable Low*	t_{EHZ}	—	27	—	ns
Data Low to 3-State from Enable Low*	t_{ELZ}	—	18	—	ns
Data High to 3-State from Enable High*	$t_{\bar{E}HZ}$	—	32	—	ns
Data Low to 3-State from Enable High*	$t_{\bar{E}LZ}$	—	18	—	ns
Valid Data from Enable High (Pin 20 = 0 V)*	t_{EDV}	—	15	—	ns
Valid Data from Enable Low (Pin 19 = 5.0 V)*	$t_{\bar{E}DV}$	—	16	—	ns
Output Transition Time* (10%–90%)	t_{tr}	—	8.0	—	ns

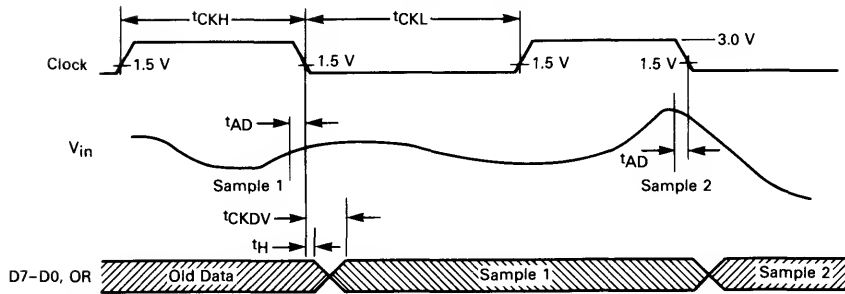
*See Figure 2 for output loading.

PIN DESCRIPTIONS

Symbol	Pin L,P Suffix	DW Suffix	Description
V_{RM}	1	1	The midpoint of the reference resistor ladder. Bypassing can be done at this point to improve performance at high frequencies.
GND	2, 12 16, 22	2, 13, 17 18, 25, 26	Digital ground. The pins should be connected directly together, and through a low impedance path to the power supply.
OVR	3	3	Overrange output. Indicates V_{in} is more positive than V_{RT} 1/2 LSB. This output does not have 3-state capability.
D7–D0	4–10, 21	4–10, 24	Digital Outputs. D7 (Pin 4) is the MSB. D0 (Pin 21 or 24) is the LSB. LSTTL compatible with 3-state capability.
$V_{CC(D)}$	11, 17	11, 12 19, 20	Power supply for the digital section. +5.0 V, $\pm 10\%$ required. Reference to digital ground.
V_{EE}	13	14	Negative Power supply. Nominally -5.2 V , it can range from -3.0 to -6.0 V , and must be more negative than V_{RB} by $>1.3\text{ V}$. Reference to analog gnd.
V_{in}	14	15	Signal voltage input. This voltage is compared to the reference to generate a digital equivalent. Input impedance is nominally 16–33K in parallel with 36 pF.
$V_{CC(A)}$	15	16	Power supply for the analog section. +5.0 V, $\pm 10\%$ required. Reference to analog ground.
CLK	18	21	Clock input. TTL compatible.
EN	19	22	Enable input. TTL compatible, a logic 1 (and $\bar{E}N$ at a logic 0) enables the data outputs. A logic 0 puts the outputs in a 3-state mode.
$\bar{E}N$	20	23	Enable input. TTL compatible, a logic 0 (and EN at a logic 1) enables the data outputs. A logic 1 puts the outputs in a 3-state mode.
V_{RB}	23	27	The bottom (most negative point) of the internal reference resistor ladder.
V_{RT}	24	28	The top (most positive point) of the internal reference resistor ladder.

MC10319

FIGURE 1 — SYSTEM TIMING DIAGRAM



t_{CKDV} and t_H measured at output levels of 0.8 and 2.4 volts.

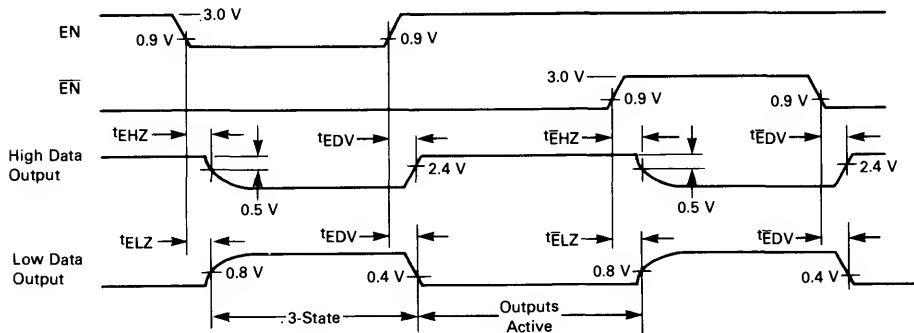


FIGURE 2 — DATA OUTPUT TEST CIRCUIT

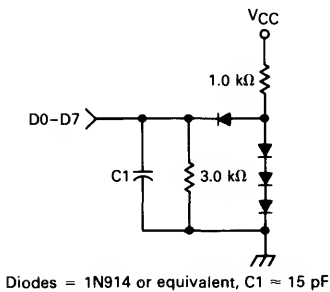


FIGURE 3 — OUTPUT 3-STATE LEAKAGE CURRENT

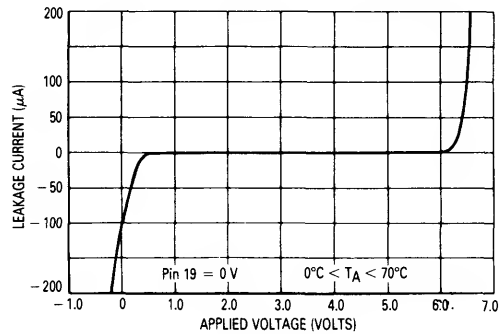


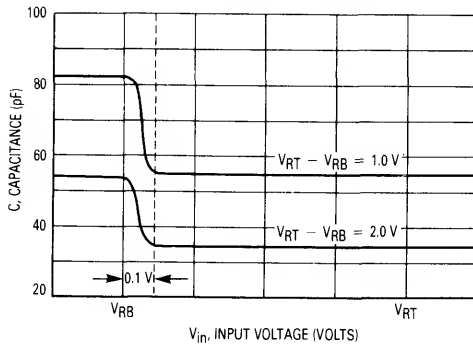
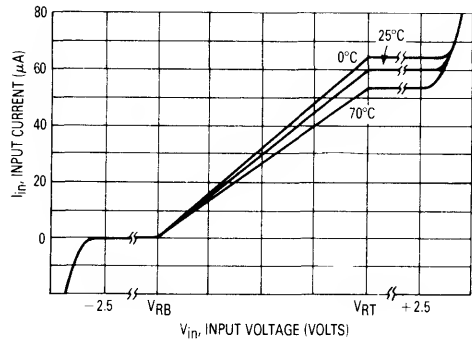
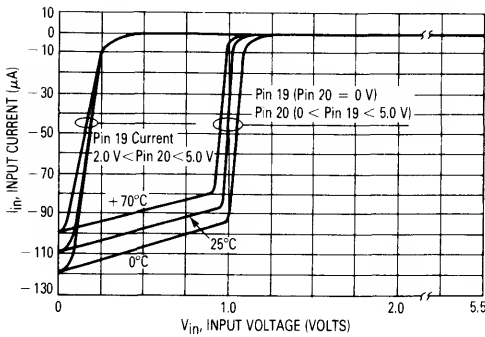
FIGURE 4 — INPUT CAPACITANCE @ V_{IN} (PIN 14)FIGURE 5 — INPUT CURRENT @ V_{IN} (PIN 14)FIGURE 6 — INPUT CURRENT @ ENABLE, $\overline{\text{ENABLE}}$ 

FIGURE 7 — CLOCK INPUT CURRENT

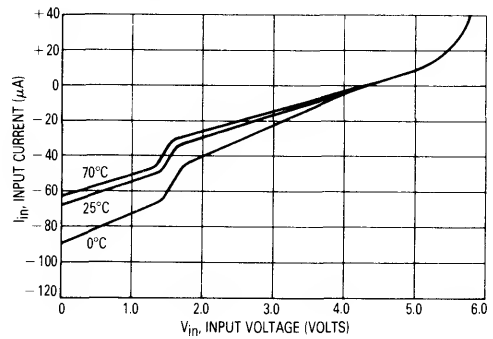


FIGURE 8 — OUTPUT VOLTAGE versus OUTPUT CURRENT

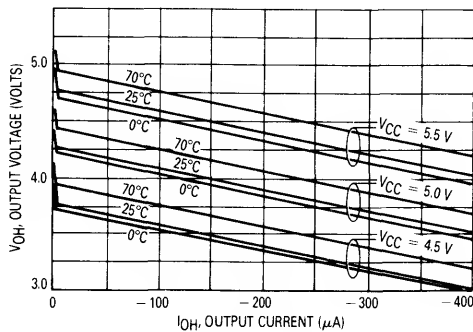


FIGURE 9 — OUTPUT VOLTAGE versus OUTPUT CURRENT

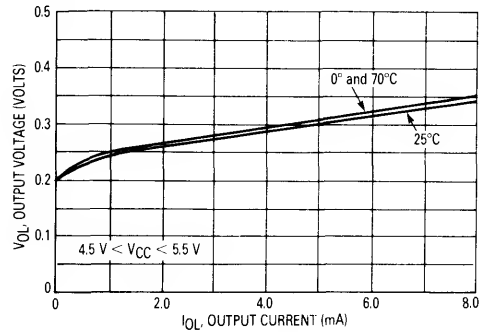


FIGURE 10 — SUPPLY CURRENT versus TEMPERATURE

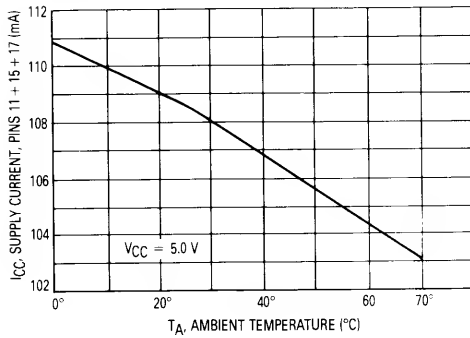


FIGURE 11 — SUPPLY CURRENT versus TEMPERATURE

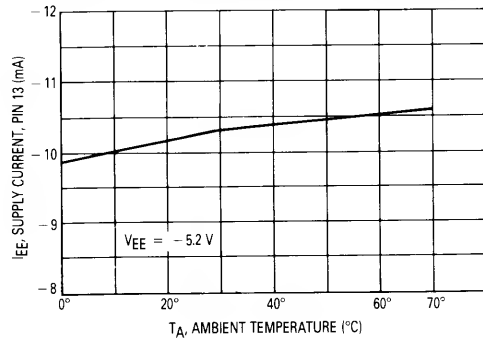


FIGURE 12 — DIFFERENTIAL LINEARITY ERROR

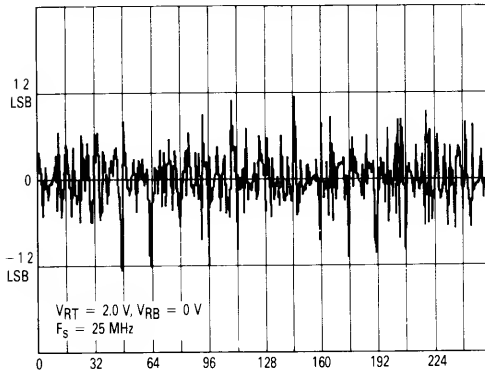


FIGURE 13 — INTEGRAL LINEARITY ERROR

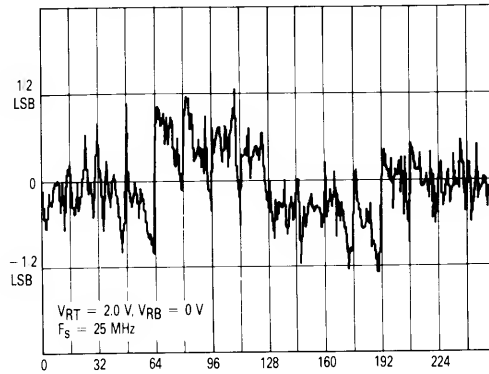


FIGURE 14 — DIFFERENTIAL LINEARITY ERROR

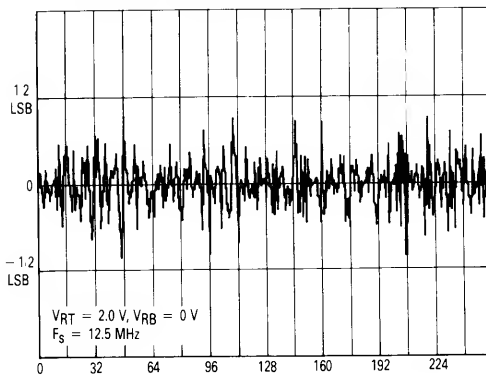
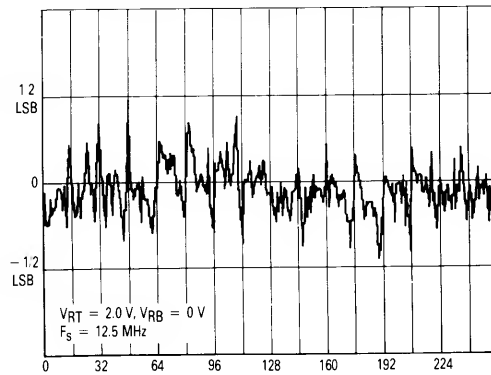


FIGURE 15 — INTEGRAL LINEARITY ERROR



DESIGN GUIDELINES

INTRODUCTION

The MC10319 is a high-speed, 8-bit, parallel ("Flash") type analog-to-digital converter containing 256 comparators at the front end. See Figure 17 for a block diagram. The comparators are arranged such that one input of each is referenced to evenly spaced voltages, derived from the reference resistor ladder. The other input of the comparators is connected to the input signal (V_{in}). Some of the comparator's differential outputs will be "true," while other comparators will have "not true" outputs, depending on their relative position. Their outputs are then latched, and converted to an 8-bit Grey code by the Differential Latch Array. The Grey code ensures any input errors due to cross talk, feed-thru, or timing disparities, result in glitches at the output of only a few LSBs, rather than the more traditional 1/2 scale and 1/4 scale glitches.

The Grey code is then translated to an 8-bit binary code, and the differential levels are translated to TTL levels before being applied to the output latches. EN-ABLE inputs at this final stage permit the TTL outputs (except Overrange) to be put into a high impedance (3-state) condition.

ANALOG SECTION

SIGNAL INPUT

The signal voltage to be digitized (V_{in}) is applied simultaneously to one input of each of the 256 comparators through Pin 14. The other inputs of the comparators are connected to 256 evenly spaced voltages derived from the reference ladder. The output code depends on the relative position of the input signal and the reference voltages. The comparators have a bandwidth of >50 MHz, which is more than sufficient for the allowable (Nyquist theory) input frequency of 12.5 MHz.

The current into Pin 14 varies linearly from 0 (when $V_{in} = V_{RB}$) to $\approx 60 \mu A$ (when $V_{in} = V_{RT}$). If V_{in} is taken below V_{RB} or above V_{RT} , the input current will remain at the value corresponding to V_{RB} and V_{RT} respectively (see Figure 5). However, V_{in} must be maintained within the absolute range of ± 2.5 volts (with respect to ground) — otherwise excessive currents will result at Pin 14, due to internal clamps.

The input capacitance at Pin 14 is typically 36 pF if $[V_{RT} - V_{RB}]$ is 2.0 volts, and increases to 55 pF if $[V_{RT} - V_{RB}]$ is reduced to 1.0 volt (see Figure 4). The capacitance is constant as V_{in} varies from V_{RT} down to ≈ 0.1 volt above V_{RB} . Taking V_{in} to V_{RB} will show an increase in the capacitance of $\approx 50\%$. If V_{in} is taken above V_{RT} , or below V_{RB} , the capacitance will stay at the values corresponding to V_{RT} and V_{RB} , respectively.

The source impedance of the signal voltage should be maintained below 100 Ω (at the frequencies of interest) in order to avoid sampling errors.

REFERENCE

The reference resistor ladder is composed of a string of equal value resistors so as to provide 256 equally spaced voltages for the comparators (see Figure 17 for the actual configuration). The voltage difference between adjacent comparators corresponds to 1 LSB of the input range. The first comparator (closest to V_{RB}) is referenced 1/2 LSB above V_{RB} , and the 256th comparator (for the overrange) is referenced 1/2 LSB below V_{RT} . The total resistance of the ladder is nominally 130 Ω , $\pm 20\%$, requiring 15.4 mA (≈ 2.0 volts), and 7.7 mA (≈ 1.0 volt). There is a nominal warm-up change of $\approx +9.0\%$ in the ladder resistance due to the $+0.29\%/^{\circ}C$ temperature coefficient.

The minimum recommended span $[V_{RT} - V_{RB}]$ is 1.0 volt. A lower span will allow offsets and nonlinearities to become significant. The maximum recommended span is 2.1 volts due to power limitations of the resistor ladder. The span may be anywhere within the range of -2.1 to $+2.1$ volts with respect to ground, and V_{RB} must be at least 1.3 volts more positive than V_{EE} . The reference voltages must be stable and free of noise and spikes, since the accuracy of a conversion is directly related to the quality of the reference.

In most applications, the reference voltages will remain fixed. In applications involving a varying reference for modulation or signal scrambling, the modulating signal may be applied to V_{RT} , or V_{RB} , or both. The output will vary inversely with the reference signal, introducing a nonlinearity into the transfer function. The addition of the modulating signal and the dc level applied to the reference must be such that the absolute voltage at V_{RT} and V_{RB} are maintained within the values listed in the Recommended Operating Limits. The RMS value of the span must be maintained ≤ 2.1 volts.

V_{RM} (Pin 1) is the midpoint of the resistor ladder, excluding the Overrange comparator. The voltage at V_{RM} is:

$$\frac{V_{RT} + V_{RB}}{2.0} - 1/2 \text{ LSB}$$

In most applications, bypassing this pin to ground (0.1 μF) is sufficient to maintain accuracy. In applications involving very high frequencies, and where linearity is critical, it may be necessary to trim the voltage at the midpoint. A means for accomplishing this is indicated in Figure 18.

POWER SUPPLIES

$V_{CC(A)}$ is the positive power supply for the comparators, and $V_{CC(D)}$ is the positive power supply for the digital portion. Both are to be $+5.0$ volts, $\pm 10\%$, and the two are to be within 100 millivolts of each other. There is indirect internal coupling between $V_{CC(D)}$ and $V_{CC(A)}$. If they are powered separately, and one supply fails, there will be current flow through the MC10319 to the failed supply.

$I_{CC(A)}$ is nominally 17 mA, and does not vary with clock frequency or with V_{IN} . It does vary linearly with $V_{CC(A)}$. $I_{CC(D)}$ is nominally 90 mA, and is independent of clock frequency. It does vary, however, by 6–7 mA as V_{IN} is changed, with the lowest current occurring when $V_{IN} = V_{RT}$. It varies linearly with $V_{CC(D)}$.

V_{EE} is the negative power supply for the comparators, and is to be within the range -3.0 to -6.0 volts. Additionally, V_{EE} must be at least 1.3 volts more negative than V_{RB} . I_{EE} is a nominal -10 mA, and is independent of clock frequency, V_{IN} , and V_{EE} .

For proper operation, the supplies **must** be bypassed **at the IC**. A $10\ \mu\text{F}$ tantalum, in parallel with a $0.1\ \mu\text{F}$ ceramic is recommended for each supply to ground.

DIGITAL SECTION

CLOCK

The Clock input is TTL compatible with a typical frequency range of 0 to 30 MHz. There is no duty cycle limitations, but the minimum low and high times must be adhered to. See Figure 7 for the input current requirements.

The conversion sequence is shown in Figure 19, and is as follows:

- On the rising edge, the data output latches are latched with old data, and the comparator output latches are released to follow the input signal (V_{IN}).
- During the high time, the comparators track the input signal. The data output latches retain the old data.
- On the falling edge, the comparator outputs are latched with the data immediately prior to this edge. The conversion to digital occurs within the device, and the data output latches are released to indicate the new data within 20 ns.
- During the clock low time, the comparator outputs remain latched, and the data output latches remain transparent.

A summary of the sequence is that data present at V_{IN} just prior to the Clock falling edge is digitized and available at the data outputs immediately after that same falling edge.

The comparator output latches provide the circuit with an effective sample-and-hold function, eliminating the need for an external sample-and-hold.

ENABLE INPUTS

The two Enable inputs are TTL compatible, and are used to change the data outputs (D7–D0) from active to 3-state. This capability allows cascading two MC10319s into a 9-bit configuration, flip-flopping two MC10319s into a 50 MHz configuration, connecting the outputs directly to a data bus, multiplexing multiple converters, etc. See the Applications Information section for more details. For the outputs to be active, Pin 19 must be a Logic "1," and Pin 20 must be a Logic "0." Changing either input will put the outputs into the high impedance mode. The Enable inputs affect **only** the state of the outputs — they do not inhibit a conversion. The input current into Pins 19 and 20 is shown in Figure 6, and the input — output timing is shown in Figure 1 and 20. Leaving either pin open is equivalent to a Logic "1," although good design practice dictates that an input should never be left open.

The Overage output (Pin 3) is not affected by the Enable inputs as it does not have 3-state capability.

OUTPUTS

The data outputs are TTL level outputs with high impedance capability. Pin 4 is the MSB (D7), and Pin 21 is the LSB (D0). The eight outputs are active as long as the Enable inputs are true (Pin 19 = high, Pin 20 = low). The timing of the outputs relative to the Clock input and the Enable inputs is shown in Figures 1 and 20. Figures 8 and 9 indicate the output voltage versus load current, while Figure 3 indicates the leakage current when in the high impedance mode.

The output code is natural binary, depicted in the table below.

The Overage output (Pin 3) goes high when the input, V_{IN} , is more positive than $V_{RT} - 1/2$ LSB. This output is always active — it does not have high impedance capability. Besides being used to indicate an input overrange, it is additionally used for cascading two MC10319s to form a 9-bit A/D converter (see Figure 27).

Input	V _{RT} , V _{RB} (volts)			Output Code	Overrange
	2.048 V, 0 V	+1.0 V, -1.0 V	+1.0 V, 0 V		
>V _{RT} - 1/2 LSB	>2.044 V	>0.9961 V	>0.9980 V	FFH	1
V _{RT} - 1/2 LSB	2.044 V	0.9961 V	0.9980 V	FFH	0 ↔ 1
V _{RT} - 1 LSB	2.040 V	0.992 V	0.9961 V	FFH	0
V _{RT} - 1-1/2 LSB	2.036 V	0.988 V	0.9941 V	FEH ↔ FFH	0
Midpoint	1.024 V	0.000 V	0.5000 V	80H	0
V _{RB} + 1/2 LSB	4.0 mV	-0.9961 V	1.95 mV	00H ↔ 01H	0
<V _{RB}	<0 V	<-1.0 V	<0 V	00H	0

APPLICATIONS INFORMATION

POWER SUPPLIES, GROUNDING

The PC board layout, and the quality of the power supplies and the ground system **at the IC** are very important in order to obtain proper operation. Noise, from any source, coming into the device on V_{CC} , V_{EE} , or ground can cause an incorrect output code due to interaction with the analog portion of the circuit. At the same time, noise generated within the MC10319 can cause incorrect operation if that noise does not have a clear path to ac ground.

Both the V_{CC} and V_{EE} power supplies must be decoupled to ground **at the IC** (within 1" max) with a 10 μ F tantalum and a 0.1 μ F ceramic. Tantalum capacitors are recommended since electrolytic capacitors simply have too much inductance at the frequencies of interest. The quality of the V_{CC} and V_{EE} supplies should then be checked at the IC with a high frequency scope. Noise spikes (always present when digital circuits are present) can easily exceed 400 mV peak, and if they get into the analog portion of the IC, the operation can be disrupted. Noise can be reduced by inserting resistors and/or inductors between the supplies and the IC.

If switching power supplies are used, there will usually be spikes of 0.5 volts or greater at frequencies of 50–200 kHz. These spikes are generally more difficult to reduce because of their greater energy content. In extreme cases, 3-terminal regulators (MC78L05ACP, MC7905.2CT), with appropriate high frequency filtering, should be used and dedicated to the MC10319.

The ripple content of the supplies should not allow their magnitude to exceed the values in the Recommended Operating Limits.

The PC board tracks supplying V_{CC} and V_{EE} to the MC10319 should preferably not be at the tail end of the bus distribution, after passing through a maze of digital circuitry. The MC10319 should be close to the power supply, or the connector where the supply voltages enter the board. If the V_{CC} and V_{EE} lines are supplying considerable current to other parts of the boards, then it is preferable to have dedicated lines from the supply or connector directly to the MC10319.

The four ground pins (2, 12, 16, 22) must be connected directly together. Any long path between them can cause stability problems due to the inductance (≈ 25 MHz) of the PC tracks. The ground return for the signal source must be noise free.

REFERENCE VOLTAGE CIRCUITS

Since the accuracy of the conversion is directly related to the quality of the references, it is imperative that accurate and stable voltages be provided to V_{RT} and V_{RB} . If the reference span is 2 volts, then 1/2 LSB is only 3.9 millivolts, and it is desirable that V_{RT} and V_{RB} be accurate to within this amount, and furthermore, that they

do not drift more than this amount once set. Over the temperature range of 0 to 70°C, a maximum temperature coefficient of 28 ppm/°C is required.

The voltage supplies used for digital circuits should preferably **not** be used as a source for generating V_{RT} and V_{RB} , due to the noise spikes (50–400 mV) present on the supplies and on their ground lines. Generally ± 15 volts, or ± 12 volts, are available for analog circuits, and are usually clean compared to supplies used for digital circuits, although ripple may be present in varying amounts. Ripple is easier to filter out than spikes, however, and so these supplies are preferred.

Figure 21 depicts a circuit which can provide an extremely stable voltage to V_{RT} **at the current required** (the maximum reference current is 19.2 mA @ 2.0 volts). The MC1403 series of reference sources has very low temperature coefficients, good noise rejection, and a high initial accuracy, allowing the circuit to be built without an adjustment pot if the V_{RT} voltage is to remain fixed at one value. Using 0.1% wirewound resistors for the divider provides sufficient accuracy and stability in many cases. Alternately, resistor networks provide high ratio accuracies, and close temperature tracking. If the application requires V_{RT} to be changed periodically, the two resistors can be replaced with a 20 turn, cermet potentiometer. Wirewound potentiometers should not be used for this type of application since the pot's slider jumps from winding to winding, and an exact setting can be difficult to obtain. Cermet pots allow for a smooth continuous adjustment.

In Figure 21, R1 reduces the power dissipation in the transistor, and can be carbon composition. The 0.1 μ F capacitor in the feedback path provides stability in the unity gain configuration. Recommended op amps are: LM358, MC34001 series, LM308A, LM324, and LM11C. Offset drift is the key parameter to consider in choosing an op amp, and the LM308A has the lowest drift of those mentioned. Bypass capacitors are not shown in Figure 21, but should always be provided at the input to the 2.5 volt reference, and at the power supply pins of the op amp.

Figure 22 shows a simpler and more economical circuit, using the LM317LZ regulator, but with lower initial accuracy and temperature stability. The op amp/current booster is not needed since the LM317LZ can supply the current directly. In a well controlled environment, this circuit will suffice for many applications. Because of the lower initial accuracy, an adjustment pot is a necessity.

Figure 23 shows two circuits for providing the voltage to V_{RB} . The circuits are similar to those of Figures 21 and 22, and have similar accuracy and stability. The output transistor is a PNP in this case since the circuit must sink the reference current.

VIDEO APPLICATIONS

The MC10319 is suitable for digitizing video signals directly without signal conditioning, although the standard 1 volt p-p video signal can be amplified to a 2.0 volt p-p signal for slightly better accuracy. Figure 24 shows the input (top trace) and reconstructed output of a standard NTSC test signal, sampled at 25 MSPS, consisting of a sync pulse, 3.58 MHz color burst, a 3.58 MHz signal in a Sin^2x envelope, a pulse, a white level signal, and a black level signal. Figure 25 shows a Sin^2x pulse that has been digitized and reconstructed at 25 MSPS. The width of the pulse is ≈ 450 ns at the base. Figure 26 shows an application circuit for digitizing video.

9-BIT A/D CONVERTER

Figure 27 shows how two MC10319s can be connected to form a 9-bit converter. In this configuration, the outputs (D7–D0) of the two 8-bit converters are paralleled. The outputs of one device are active, while the outputs of other are in the 3-state mode. The selection is made by the Overrange output of the lower MC10319, which controls Enable inputs on the two devices. Additionally, this output provides the 9th bit.

The reference ladders are connected in series, providing the 512 steps required for 9 bits. The input voltage range is determined by V_{RT} of the upper MC10319, and V_{RB} of the lower device. A minimum of 1.0 volt is required across each converter. The 500 Ω pot (20 turn cermet) allows for adjustment of the midpoint since the reference resistors of the two MC10319s may not be identical in value. Without the adjustment, a non-equal voltage division would occur, resulting in a nonlinear

conversion. If the references are to be symmetrical about ground (e.g., ± 1.0 volt), the adjustment can be eliminated, and the midpoint connected to ground.

The use of latches on the outputs is optional, depending on the application.

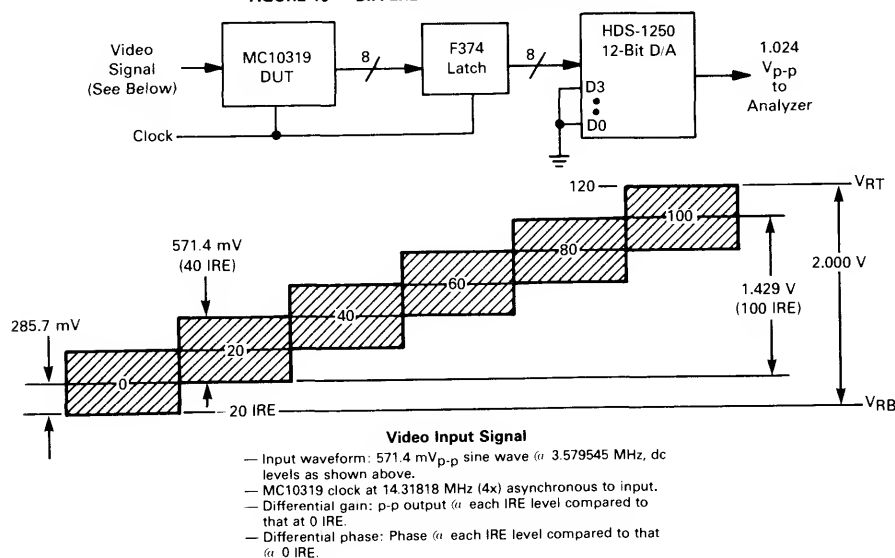
50 MHz, 8-BIT A/D CONVERTER

Figure 28 shows how two MC10319s can be connected together in a flip-flop arrangement in order to have an effective conversion speed of 50 MHz. The 74F74 D-type flip-flop provides a 25 MHz clock to each converter, and at the same time, controls the ENABLES so as to alternately enable and disable the outputs. The Overranges do not have 3-state capability, and so cannot be paralleled. Instead they are OR'd together. The use of latches is optional, and depends on the application. Data should be latched, or written to RAM (in a DMA operation), on the high-to-low transition of the 50 MHz clock.

NEGATIVE VOLTAGE REGULATOR

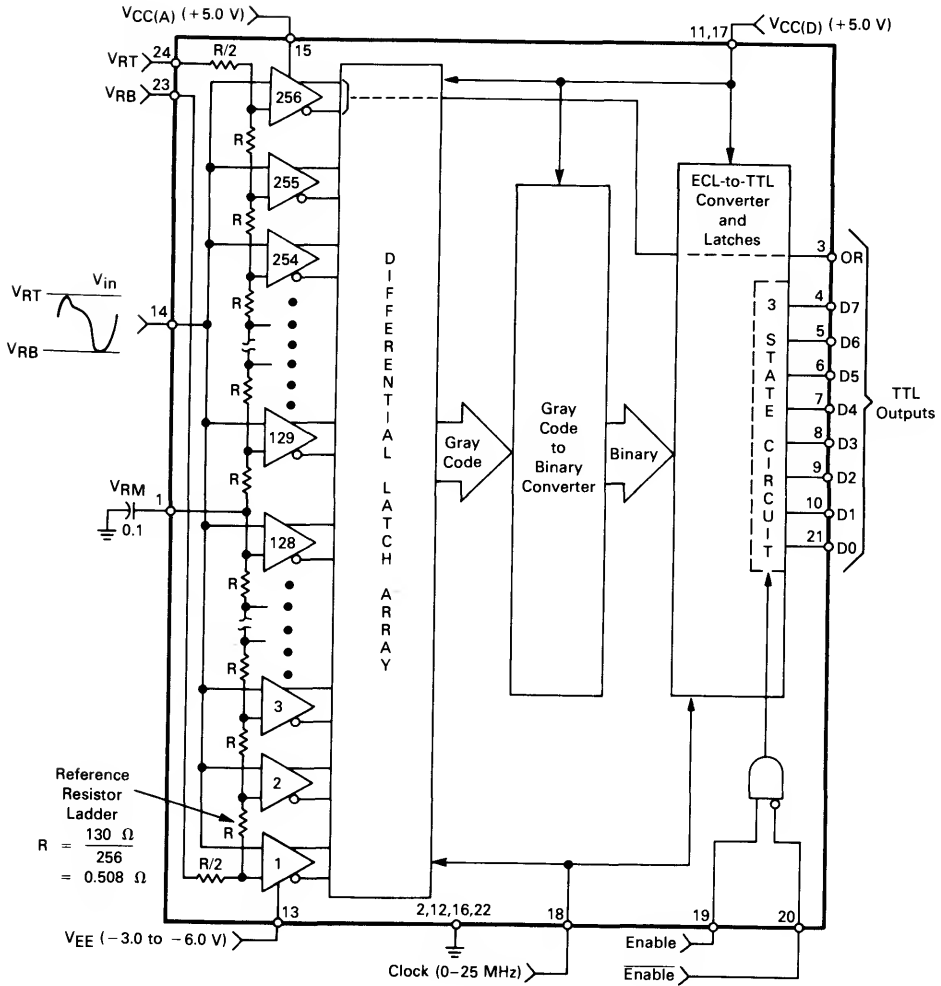
In the cases where a negative power supply is not available — neither the -3.0 to -6.0 volts, nor a higher negative voltage from which to derive it — the circuit of Figure 29 can be used to generate -5.0 volts from the $+5.0$ volts supply. The PC board space required is small (≈ 2.0 in²), and it can be located physically close to the MC10319. The MC34063 is a switching regulator, and in Figure 29 is configured in an inverting mode of operation. The regulator operating specifications are also given.

FIGURE 16 — DIFFERENTIAL PHASE AND GAIN TEST



MC10319

FIGURE 17 — MC10319



MC10319

FIGURE 18 — ADJUSTING V_{RM} FOR IMPROVED LINEARITY

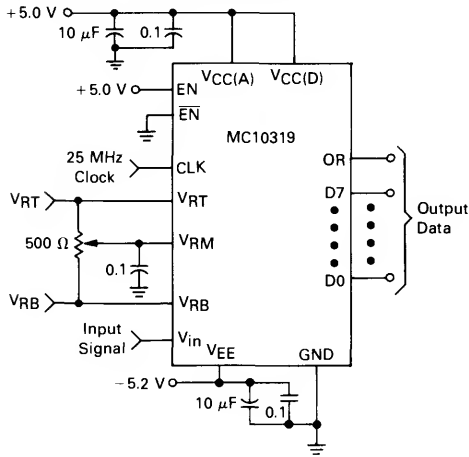


FIGURE 19 — CONVERSION SEQUENCE

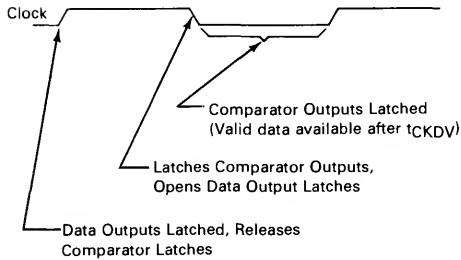
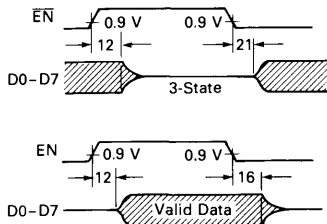


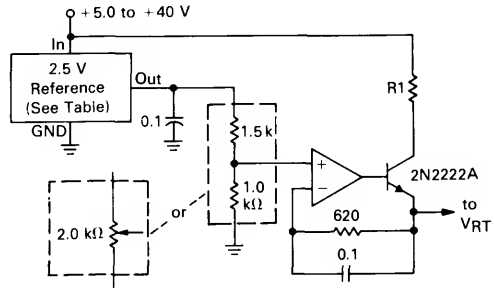
FIGURE 20 — ENABLE TO OUTPUT CRITICAL TIMING



Timing (t_r) D7-D0 measured where waveform starts to change. Indicated time values are typical at 25°C, and are in ns.

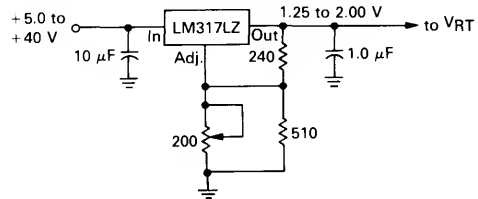
FIGURE 21 — PRECISION V_{RT} VOLTAGE SOURCE

$R1 = 100 \Omega$ for +5.0 V
620 Ω for +15 V



2.5 V References	MC1403U	MC1403AU
Line Regulation	0.5 mV	0.5 mV
T _C (ppm/°C) max	40	25
ΔV_{out} for 0-70°C	7.0 mV	4.4 mV
Initial Accuracy	± 1%	± 1%

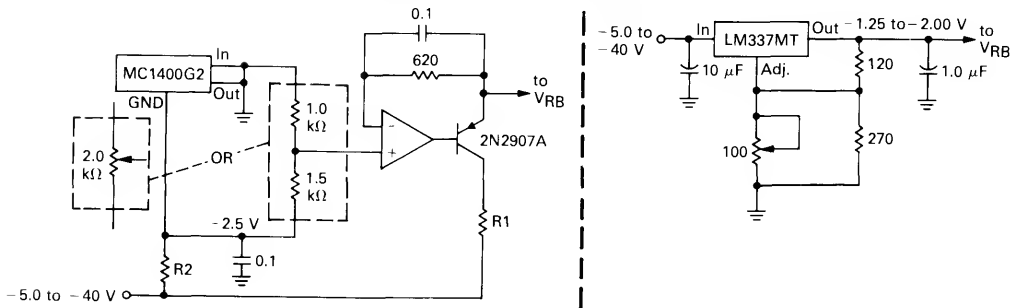
FIGURE 22 — V_{RT} VOLTAGE SOURCE



LM317LZ	
Line Regulation	1.0 mV
T _C (ppm/°C) max	60
ΔV_{out} for 0-70°C	8.4 mV
Initial Accuracy	± 4%

MC10319

FIGURE 23 — V_{RB} VOLTAGE SOURCES



R1 = 100 Ω for -5.0 V
 620 Ω for -15 V
 R2 = 620 Ω for -5.0 V
 3.0 kΩ for -15 V

	MC1400G2	LM337MT
Line Regulation	1.0 mV	1.0 mV
T_C (ppm/°C) max	25	48
ΔV_{out} for 0-70°C	4.4 mV	6.7 mV
Initial Accuracy	± 0.2%	± 4%

6

FIGURE 24 — COMPOSITE VIDEO WAVEFORM

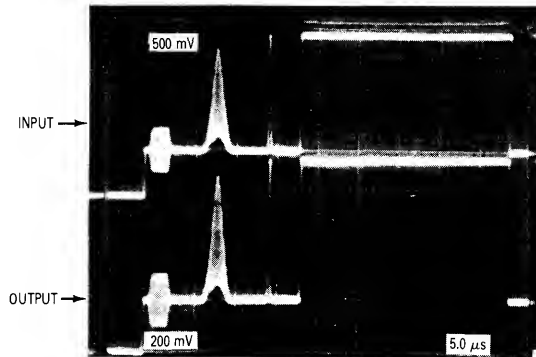
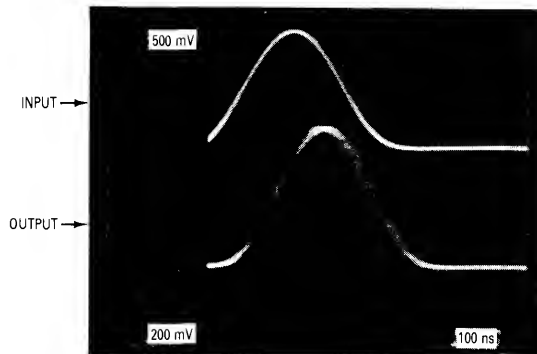
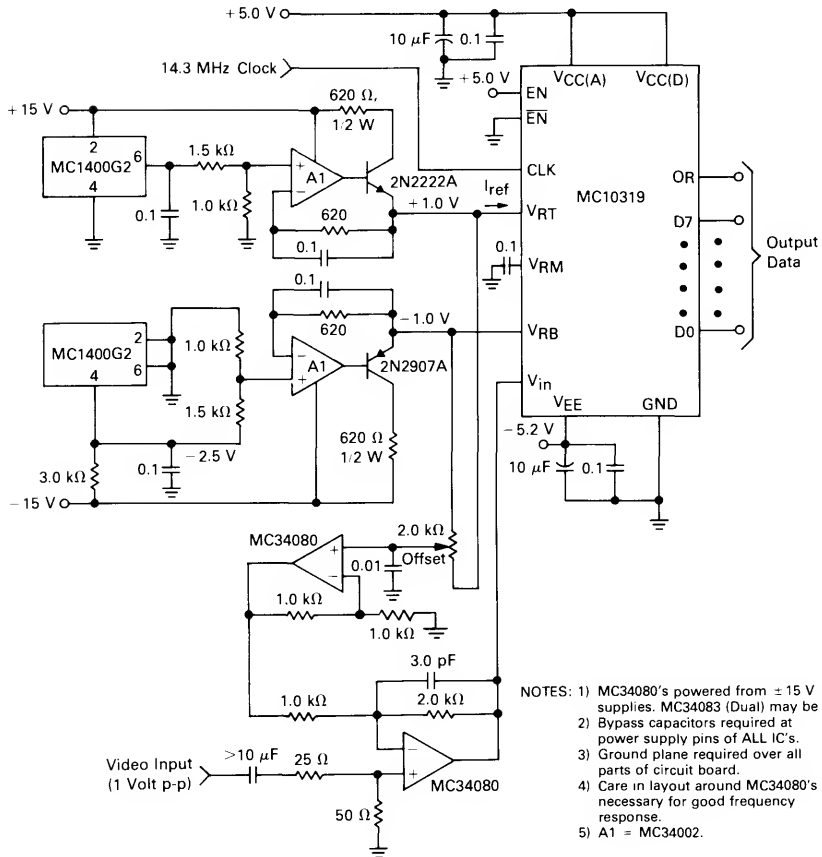


FIGURE 25 — $\sin^2 X$ WAVEFORM



MC10319

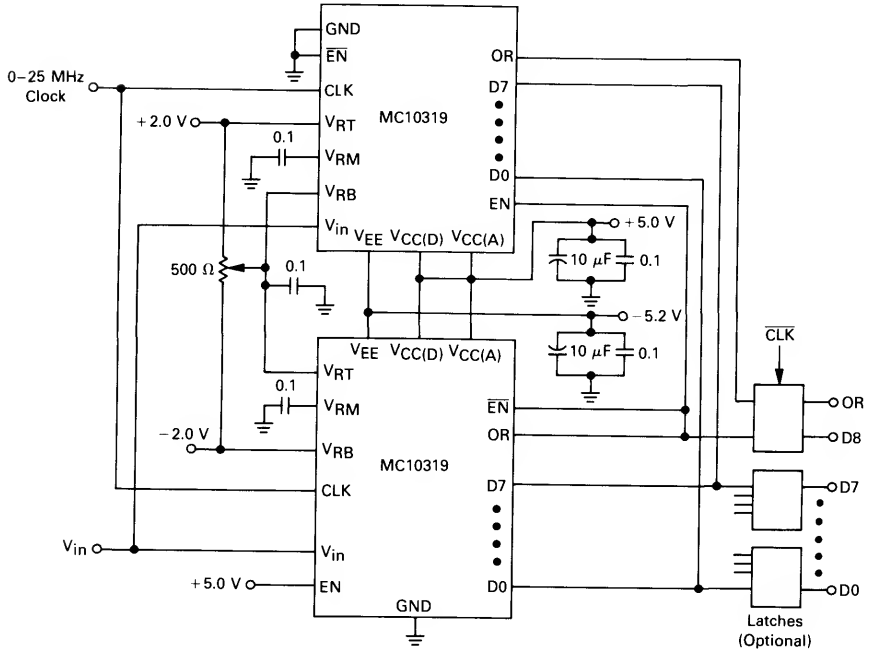
FIGURE 26 — APPLICATION CIRCUIT FOR DIGITIZING VIDEO



- NOTES: 1) MC34080's powered from ± 15 V supplies. MC34083 (Dual) may be used.
 2) Bypass capacitors required at power supply pins of ALL IC's.
 3) Ground plane required over all parts of circuit board.
 4) Care in layout around MC34080's necessary for good frequency response.
 5) A1 = MC34002.

MC10319

FIGURE 27 — 9-BIT A/D CONVERTER



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MC10319

FIGURE 28 — 50 MHz 8-BIT A/D CONVERTER

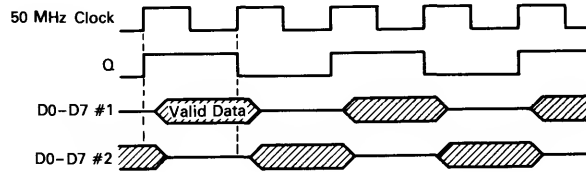
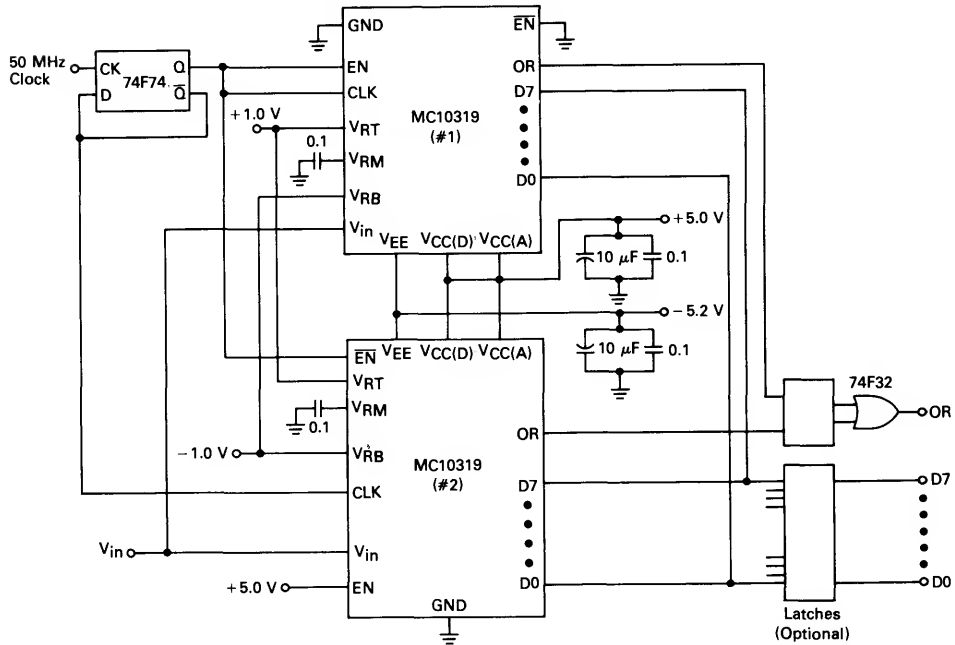
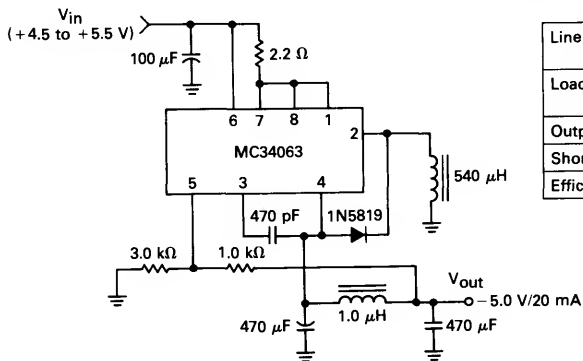


FIGURE 29 — -5.0 VOLT REGULATOR



Line Regulation	$4.5\text{ V} < V_{in} < 5.5\text{ V}$, $I_{out} = 10\text{ mA}$	0.16%
Load Regulation	$V_{in} = 5.0\text{ V}$, $8.0\text{ mA} < I_{out} < 20\text{ mA}$	0.4%
Output Ripple	$V_{in} = 5.0\text{ V}$, $I_{out} = 20\text{ mA}$	2 mV_{p-p}
Short Circuit I_{out}	$V_{in} = 5.0\text{ V}$, $R_1 = 0.1\text{ }\Omega$	140 mA
Efficiency	$V_{in} = 5.0\text{ V}$, $I_{out} = 50\text{ mA}$	52%

GLOSSARY

APERTURE DELAY — The time difference between the sampling signal (typically a clock edge) and the actual analog signal converted. The actual signal converted may occur before or after the sampling signal, depending on the internal configuration of the converter.

BIPOLAR INPUT — A mode of operation whereby the analog input (of an A-D), or output (of a DAC), includes both negative and positive values. Examples are -1.0 to $+1.0$ V, -5.0 to $+5.0$ V, -2.0 to $+8.0$ V, etc.

BIPOLAR OFFSET ERROR — The difference between the actual and ideal locations of the 00_H to 01_H transition, where the ideal location is $1/2$ LSB above the most negative reference voltage.

BIPOLAR ZERO ERROR — The error (usually expressed in LSBs) of the input voltage location (of an A-D) of the 80_H to 81_H transition. The ideal location is $1/2$ LSB above zero volts in the case of an A-D setup for a symmetrical bipolar input (e.g., -1.0 to $+1.0$ V).

DIFFERENTIAL NONLINEARITY — The maximum deviation in the actual step size (one transition level to another) from the ideal step size. The ideal step size is defined as the Full Scale Range divided by 2^n (n = number of bits). This error must be within ± 1 LSB for proper operation.

ECL — Emitter coupled logic.

FULL SCALE RANGE (ACTUAL) — The difference between the actual minimum and maximum end points of the analog input (of an A-D).

FULL SCALE RANGE (IDEAL) — The difference between the actual minimum and maximum end points of the analog input (of an A-D), plus one LSB.

GAIN ERROR — The difference between the actual and expected gain (end point to end point), with respect to the reference, of a data converter. The gain error is usually expressed in LSBs.

GREY CODE — Also known as *reflected binary code*, it is a digital code such that each code differs from adjacent codes by only one bit. Since more than one bit is never changed at each transition, race condition errors are eliminated.

INTEGRAL NONLINEARITY — The maximum error of an A-D, or DAC, transfer function from the ideal straight line connecting the analog end points. This parameter is sensitive to dynamics, and test conditions must be specified in order to be meaningful. This parameter is the best overall indicator of the device's performance.

LSB — Least Significant Bit. It is the lowest order bit of a binary code.

LINE REGULATION — The ability of a voltage regulator to maintain a certain output voltage as the input to the regulator is varied. The error is typically expressed as a percent of the nominal output voltage.

LOAD REGULATION — The ability of a voltage regulator to maintain a certain output voltage as the load current is varied. The error is typically expressed as a percent of the nominal output voltage.

MONOTONICITY — The characteristic of the transfer function whereby increasing the input code (of a DAC), or the input signal (of an A-D), results in the output never decreasing.

MSB — Most Significant Bit. It is the highest order bit of a binary code.

NATURAL BINARY CODE — A binary code defined by:

$$N = A_n 2^n + \dots + A_3 2^3 + A_2 2^2 + A_1 2^1 + A_0 2^0$$

where each "A" coefficient has a value of 1 or 0. Typically, all zeroes correspond to a zero input voltage of an A-D, and all ones correspond to the most positive input voltage.

NYQUIST THEORY — See Sampling Theorem.

OFFSET BINARY CODE — Applicable only to bipolar input (or output) data converters, it is the same as Natural Binary, except that all zeroes correspond to the most negative input voltage (of an A-D), while all ones correspond to the most positive input.

POWER SUPPLY SENSITIVITY — The change in a data converter's performance with changes in the power supply voltage(s). This parameter is usually expressed in percent of full scale versus ΔV .

QUANTIZATION ERROR — Also known as digitization error or uncertainty. It is the inherent error involved in digitizing an analog signal due to the finite number of steps at the digital output versus the infinite number of values at the analog input. This error is a minimum of $\pm 1/2$ LSB.

RESOLUTION — The smallest change which can be discerned by an A-D converter, or produced by a DAC. It is usually expressed as the number of bits, n , where the converter has 2^n possible states.

SAMPLING THEOREM — Also known as the Nyquist Theorem. It states that the sampling frequency of an A-D must be no less than $2x$ the highest frequency (of interest) of the analog signal to be digitized in order to preserve the information of that analog signal.

UNIPOLAR INPUT — A mode of operation whereby the analog input range (of an A-D), or output range (of a DAC), includes values of a signal polarity. Examples are 0 to $+2.0$ V, 0 to -5.0 V, $+2.0$ to $+8.0$ V, etc.

UNIPOLAR OFFSET ERROR — The difference between the actual and ideal locations of the 00_H to 01_H transition, where the ideal location is $1/2$ LSB above the most negative input voltage.

**HIGH SPEED 7-BIT ANALOG-TO-DIGITAL
FLASH CONVERTER**

The MC10321 is a 7-bit high speed parallel flash A/D converter, which employs an internal Grey Code structure to eliminate large output errors on fast slewing input signals. It is fully TTL compatible, requiring a +5.0 volt supply, and a negative supply between -3.0 and -6.0 volts. Three-state TTL outputs allow direct connection to a data bus or common I/O memory.

The MC10321 contains 128 parallel comparators wired along a precision input reference network. The comparator outputs are fed to latches, and then to an encoder network which produces a 7-bit data byte, plus an overrange bit. The data is latched and converted to three-state LSTTL levels. Enable inputs permit setting the outputs to a three-state condition. The overrange bit is always active to allow for sensing of the overrange condition, and to ease the interconnection of two MC10321s into an 8-bit configuration.

The MC10321 is available in a 20-pin standard plastic and SOIC packages.

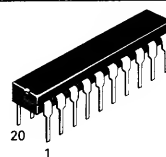
Applications include Video displays (digital TV, picture-in-picture, special effects), radar processing, high speed instrumentation, and TV broadcast.

- Internal Grey Code for Speed and Accuracy
- 25 MHz Sampling Rate
- 7-Bit Resolution with 8-Bit Accuracy
- Easily Cascadable into an 8-Bit System
- Three-State LSTTL Outputs with True and Complement Enable Inputs
- Low Input Capacitance: 25 pF
- No Clock Kick-Out Currents on Input or Reference
- Wide Input Range: 1.0-2.1 Volts within a ± 2.1 Volt Range
- No Sample and Hold Required for Video Applications
- Edge Triggered Conversion — No Pipeline Delay
- True and Complement Enable Inputs for Three-State Control
- Standard DIP and Surface Mount Packages Available
- Operating Temperature Range: -40° to +85°C

MC10321

**HIGH SPEED
7-BIT ANALOG-TO-DIGITAL
FLASH CONVERTER**

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**



P SUFFIX
PLASTIC PACKAGE
CASE 738

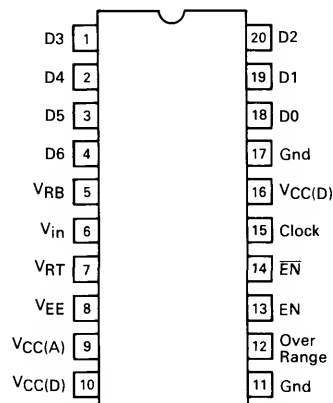


DW SUFFIX
PLASTIC PACKAGE
CASE 751D
(SO-20)

6

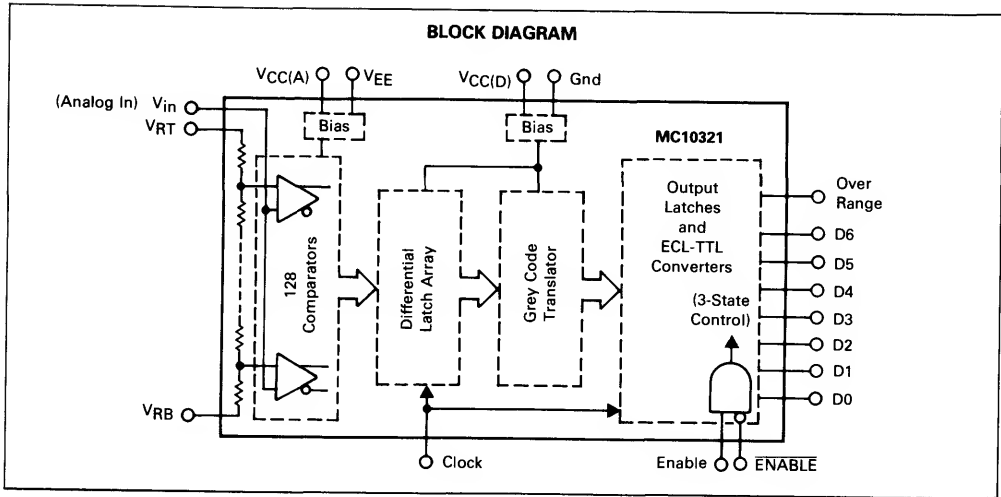
PIN CONNECTIONS

(Top View)



ORDERING INFORMATION

Device	Temperature Range	Package
MC10321P	-40° to +85°C	Plastic DIP
MC10321DW		SO-20



6

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Supply Voltage	$V_{CC(A)}, V_{CC(D)}$ V_{EE}	+7.0 -7.0	Vdc
Positive Supply Voltage Differential	$V_{CC(D)} - V_{CC(A)}$	-0.3, +0.3	Vdc
Digital Input Voltage (Pins 13-15)	$V_{I(D)}$	-0.5, +7.0	Vdc
Analog Input Voltage (Pins 5, 6, 7)	$V_{I(A)}$	-2.5, +2.5	Vdc
Reference Voltage Span (Pin 7-Pin 5)	—	+2.3	Vdc
Applied Output Voltage (D0-D6 in 3-State)	—	-0.3, +7.0	Vdc
Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	-65, +150	°C

Devices should not be operated at these values. The "Recommended Operating Limits" provide guidelines for actual device operation.

RECOMMENDED OPERATING LIMITS

Parameter	Symbol	Min	Typ	Max	Units
Power Supply Voltage (Pin 9)	$V_{CC(A)}$	+4.5	+5.0	+5.5	Vdc
Power Supply Voltage (Pins 10, 16)	$V_{CC(D)}$	+4.5	+5.0	+5.5	Vdc
$V_{CC(D)} - V_{CC(A)}$	ΔV_{CC}	-0.1	0	+0.1	Vdc
Power Supply Voltage (Pin 8)	V_{EE}	-6.0	-5.0	-3.0	Vdc
Digital Input Voltages (Pins 13-15)	—	0	—	$V_{CC(D)}$	Vdc
Analog Input (Pin 6)	V_{in}	-2.1	—	+2.1	Vdc
Voltage @ V_{RT} (Pin 7)	V_{RT}	-1.0	—	+2.1	Vdc
@ V_{RB} (Pin 5)	V_{RB}	-2.1	—	+1.0	Vdc
$V_{RT} - V_{RB}$	ΔV_R	+1.0	—	+2.1	Vdc
$V_{RB} - V_{EE}$	—	1.3	—	—	Vdc
Applied Output Voltage (Pins D0-D6 in 3-State)	V_O	0	—	$V_{CC(D)}$	Vdc
Clock Pulse Width — High	t_{CKH}	5.0	—	—	ns
— Low	t_{CKL}	15	—	—	ns
Clock Frequency	f_{CLK}	0	—	25	MHz
Operating Ambient Temperature	T_A	-40	—	+85	°C

All limits are not necessarily functional concurrently.

MC10321

ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$, $V_{EE} = -5.2\text{ V}$, $V_{RT} = +1.0\text{ V}$, $V_{RB} = -1.0\text{ V}$, except where noted)

Characteristic	Symbol	Min	Typ	Max	Units
TRANSFER CHARACTERISTICS ($f_{CKL} = 25\text{ MHz}$)					
Resolution	N	—	—	7.0	Bits
Monotonicity	MON	Guaranteed			Bits
Integral Nonlinearity	INL	—	$\pm 1/4$	± 1.0	LSB
Differential Nonlinearity	DNL	—	—	± 1.0	LSB
Differential Phase (See Figure 11)	DP	—	2.0	—	Deg.
Differential Gain (See Figure 11)	DG	—	2.0	—	%
Power Supply Rejection Ratio ($4.5\text{ V} < V_{CC} < 5.5\text{ V}$, $V_{EE} = -5.2\text{ V}$) ($-6.0\text{ V} < V_{EE} < -3.0\text{ V}$, $V_{CC} = +5.0\text{ V}$)	PSRR	—	0.02 0	—	LSB/V
ANALOG INPUT (Pin 6)					
Input Current @ $V_{in} = V_{RB} - 0.1\text{ V}$ (See Figure 4) @ $V_{in} = V_{RT} + 0.1\text{ V}$ (See Figure 4)	I_{INL} I_{INH}	—	+1.0 +60	+5.0 +150	μA
Input Capacitance ($1.0\text{ V} < (V_{RT} - V_{RB}) < 2.0\text{ V}$)	C_{in}	—	22	—	pF
Bipolar Offset Error	V_{OS}	—	0.1	—	LSB
REFERENCE					
Ladder Resistance (V_{RT} to V_{RB} , $T_A = 25^\circ\text{C}$)	R_{ref}	100	140	175	Ω
Temperature Coefficient	T_C	—	+0.29	—	$^\circ\text{C}/^\circ\text{C}$
Ladder Capacitance (Pin 1 Open)	C_{ref}	—	5.0	—	pF
ENABLE INPUTS ($V_{CC} = 5.5\text{ V}$)					
Input Voltage — High — Low	V_{IHE} V_{ILE}	2.0 —	— —	— 0.8	V
Input Current @ 2.4 Volts (See Figure 5) @ 0.4 Volts (See Figure 5)	I_{IHE} I_{ILE}	— -200	+0.2 -120	2.0 —	μA
Input Clamp Voltage ($I_{IK} = -18\text{ mA}$)	V_{IKE}	-1.5	-1.3	—	V
CLOCK INPUT ($V_{CC} = 5.5\text{ V}$)					
Input Voltage — High — Low	V_{IHC} V_{ILC}	2.0 —	— —	— 0.8	Vdc
Input Current @ 0.4 V (See Figure 6) @ 2.7 V (See Figure 6)	I_{ILC} I_{IHC}	-150 -80	-80 -40	—	μA
Input Clamp Voltage ($I_{IK} = -18\text{ mA}$)	V_{IKC}	-1.5	-1.3	—	Vdc
DIGITAL OUTPUTS					
High Output Voltage ($I_{OH} = -400\text{ }\mu\text{A}$ @ D6-D0, OR, $V_{CC} = 4.5\text{ V}$, See Figure 7)	V_{OH}	2.4	3.0	—	V
Low Output Voltage ($I_{OL} = 4.0\text{ mA}$ @ D6-D0, OR, $V_{CC} = 4.5\text{ V}$, See Figure 8)	V_{OL}	—	0.3	0.4	V
Output Short Circuit Current* (D6-D0, OR, $V_{CC} = 5.5\text{ V}$)	I_{SC}	—	-35	—	mA
Output Leakage Current ($0.4 < V_O < 2.4\text{ V}$, See Figure 3, $V_{CC} = 5.5\text{ V}$, D0-D6 in 3-State Mode)	I_{LK}	-10	—	+10	μA
Output Capacitance (D0-D6 in 3-State Mode)	C_{out}	—	5.0	—	pF
*Only one output to be shorted at a time, not to exceed 1 second.					
POWER SUPPLIES					
$V_{CC(A)}$ Current ($4.5\text{ V} < V_{CC(A)} < 5.5\text{ V}$, Outputs Unloaded)	$I_{CC(A)}$	10	13	16	mA
$V_{CC(D)}$ Current ($4.5\text{ V} < V_{CC(D)} < 5.5\text{ V}$, Outputs Unloaded)	$I_{CC(D)}$	40	60	80	mA
V_{EE} Current ($-6.0\text{ V} < V_{EE} < -3.0\text{ V}$)	I_{EE}	-16	-13	-8.0	mA
Power Dissipation ($V_{RT} - V_{RB} = 2.0\text{ V}$, Outputs Unloaded)	P_D	—	459	668	mW

MC10321

TIMING CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{CC} = +5.0\text{ V}$, $V_{EE} = -5.2\text{ V}$, $V_{RT} = +1.0\text{ V}$, $V_{RB} = -1.0\text{ V}$,
See System Timing Diagram)

Parameter	Symbol	Min	Typ	Max	Units
INPUTS					
Min Clock Pulse Width — High	t_{CKH}	—	5.0	—	ns
— Low	t_{CKL}	—	15	—	ns
Max Clock Rise, Fall Time	$t_{R,F}$	—	100	—	ns
Clock Frequency	f_{CLK}	0	30	25	MHz
OUTPUTS					
New Data Valid from Clock Low	t_{CKDV}	—	22	—	ns
Aperture Delay	t_{AD}	—	3.0	—	ns
Hold Time	t_H	—	6.0	—	ns
Data High to 3-State from Enable Low*	t_{EHZ}	—	22	—	ns
Data Low to 3-State from Enable Low*	t_{ELZ}	—	17	—	ns
Data High to 3-State from ENABLE High*	$t_{E'HZ}$	—	27	—	ns
Data Low to 3-State from ENABLE High*	$t_{E' LZ}$	—	19	—	ns
Valid Data from Enable High (Pin 14 = 0 V)*	t_{EDV}	—	13	—	ns
Valid Data from ENABLE Low (Pin 13 = 5.0 V)*	$t_{E'DV}$	—	20	—	ns
Output Transition Time (10%–90%)*	t_{tr}	—	6.0	—	ns

*See Figure 2 for output loading.

TEMPERATURE CHARACTERISTICS

Parameter	Typical Value @ 25°C	Typical Change –40 to $+85^\circ\text{C}$
I_{CC} (+5.0 V Supply Current)	73 mA	–100 $\mu\text{A}/^\circ\text{C}$
I_{EE} (–5.2 V Supply Current)	–13 mA	+7.0 $\mu\text{A}/^\circ\text{C}$
Ladder Resistance	140 Ω	+0.29%/°C
V_{OL} (Output Low Voltage @ 4.0 mA)	0.3 V	+8.0 $\mu\text{V}/^\circ\text{C}$
V_{OH} (Output High Voltage @ –400 μA)	3.0 V	2.1 mV/°C
Differential Nonlinearity	—	–0.0008 LSB/°C
Integral Nonlinearity	0.25 LSB	–0.001 LSB/°C

PIN DESCRIPTIONS

Symbol	Pin	Description
GND	11,17	Power supply ground. The two pins should be connected directly together, and through a low impedance path to the power supply.
OR	12	Overrange output. Indicates V_{in} is more positive than V_{RT} –1/2 LSB. This output does not have 3-state capability, and therefore is always active.
D6–D0	1–4, 18–20	Digital Outputs. D6 (Pin 4) is the MSB, D0 (Pin 18) is the LSB. LSTTL compatible with 3-state capability.
$V_{CC(D)}$	10,16	Power supply for the digital section. +5.0 V, $\pm 10\%$ required.
V_{EE}	8	Negative Power supply. Nominally –5.2 V, it can range from –3.0 to –6.0 V, and must be more negative than V_{RB} by $>1.3\text{ V}$.
V_{in}	6	Signal voltage input. This voltage is compared to the reference to generate a digital equivalent. Input impedance is nominally 16–33 k Ω (See Figure 4) in parallel with 22 pF.

PIN DESCRIPTIONS

Symbol	Pin	Description
$V_{CC(A)}$	9	Power supply for the analog section. +5.0 V, $\pm 10\%$ required.
CLK	15	Clock input, TTL compatible, and can range from dc to 25 MHz. Conversion occurs on the negative edge of the clock.
EN	13	Enable input. TTL compatible, a Logic "1" (and Pin 14 a Logic "0") enables the data outputs. A Logic "0" sets the outputs (except Overrange) to a 3-state mode.
EN	14	ENABLE input. TTL compatible, a Logic "0" (and Pin 13 a Logic "1") enables the data outputs. A Logic "1" sets the outputs (except Overrange) to a 3-state mode.
V_{RB}	5	The bottom (most negative point) of the internal reference resistor ladder. The ladder resistance is typically 140 Ω to V_{RT} .
V_{RT}	7	The top (most positive point) of the internal reference resistor ladder.

Pin assignments are the same for the standard DIP package and the surface mount package.

MC10321

FIGURE 1 — SYSTEM TIMING DIAGRAM

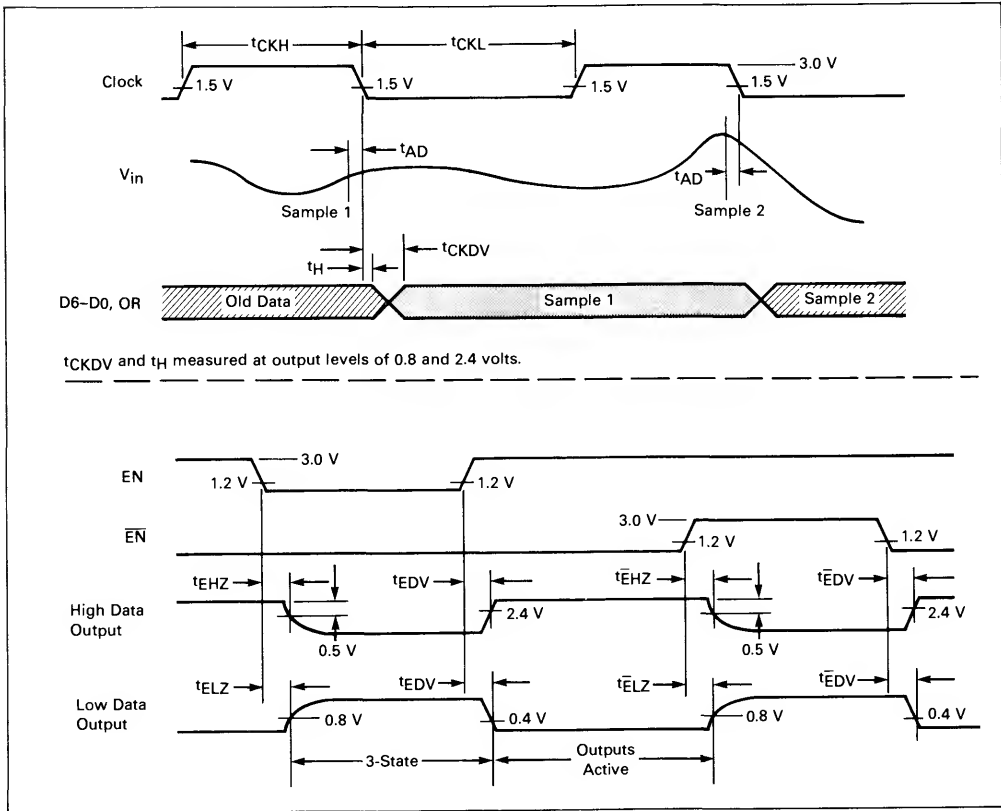


FIGURE 2 — DATA OUTPUT TEST CIRCUIT

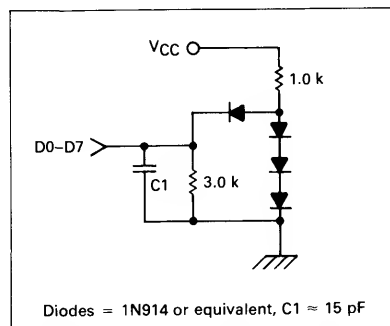


FIGURE 3 — OUTPUT 3-STATE LEAKAGE CURRENT

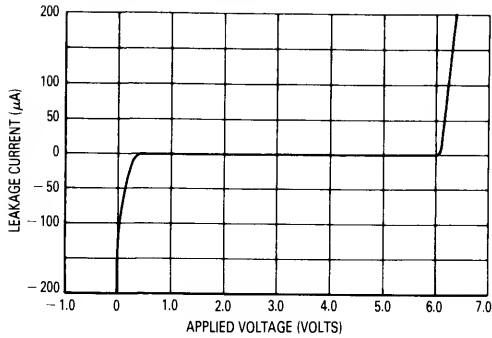
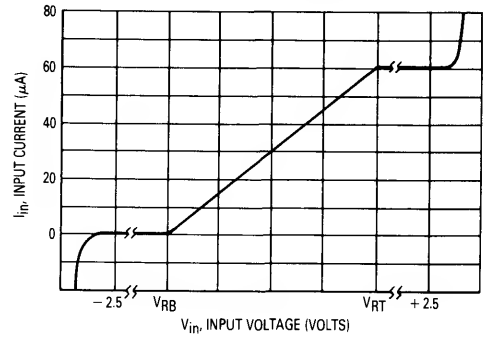
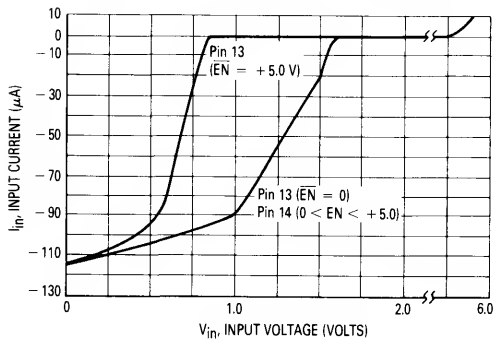
FIGURE 4 — INPUT CURRENT @ V_{in} FIGURE 5 — INPUT CURRENT AT ENABLE, $\overline{\text{ENABLE}}$ 

FIGURE 6 — CLOCK INPUT CURRENT

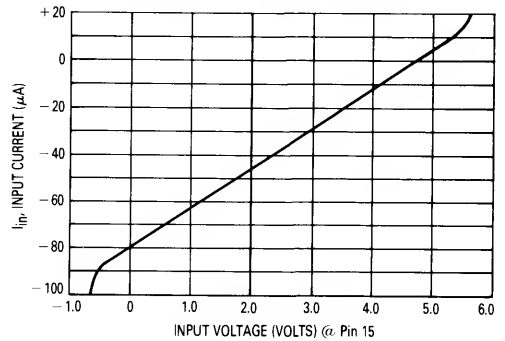


FIGURE 7 — OUTPUT VOLTAGE versus OUTPUT CURRENT

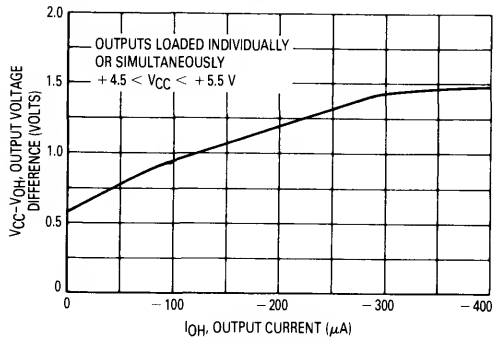


FIGURE 8 — OUTPUT VOLTAGE versus OUTPUT CURRENT

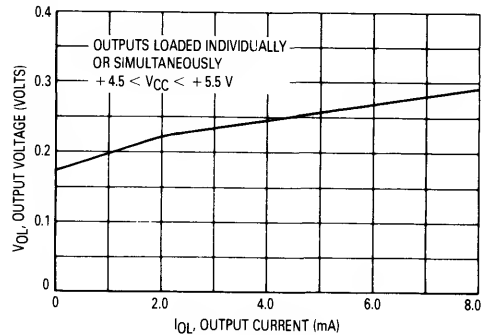
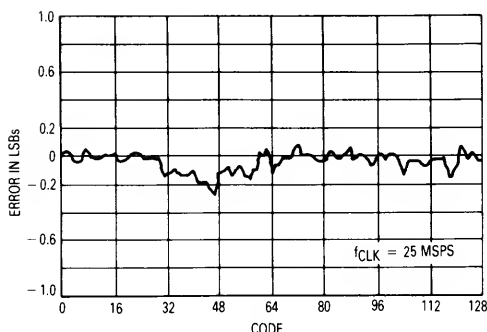
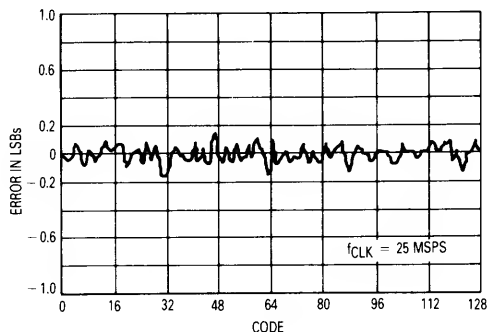


FIGURE 9 — INTEGRAL LINEARITY ERROR IN LSBs
versus CODEFIGURE 10 — DIFFERENTIAL LINEARITY ERROR
IN LSBs versus LOWER CODE

DESIGN GUIDELINES

INTRODUCTION

The MC10321 is a high speed, 7-bit parallel ("Flash") type Analog-to-Digital converter containing 128 comparators at the front end. See Figure 12 for a block diagram. The comparators are arranged such that one input of each is referenced to evenly spaced voltages, derived from the reference resistor ladder. The other input of each of the comparators is connected to the input signal (V_{IN}). Some of the comparator's differential outputs will be "true," while other comparators will have "not true" outputs, depending on their relative position. Their outputs are then latched, and converted to a 7-bit Grey code by the Differential Latch Array. The Grey code ensures that errors caused at the input stage, due to cross talk, feed-thru, or timing disparities, result in glitches at the output of only a few LSBs, rather than the more traditional 1/2 scale and 1/4 scale glitches.

The Grey code is then translated to a 7-bit binary code, and the differential levels are translated to TTL levels before being applied to the output latches. ENABLE inputs (EN and \overline{EN}) at this final stage permit the TTL outputs (except Overrange) to be put into a high impedance (3-state) condition.

ANALOG SECTION

SIGNAL INPUT

The signal voltage to be digitized (V_{IN}) is applied simultaneously to one input of each of the 128 comparators through Pin 6. The other inputs of the comparators are connected to 128 evenly spaced voltages derived from the reference ladder. The output code depends on the relative position of the input signal to the reference voltages. The comparators have a bandwidth of >50 MHz, which is more than sufficient for the allowable (Nyquist theory) input frequency of 12.5 MHz.

The current into Pin 6 varies linearly from 0 (when $V_{IN} = V_{RB}$) to $\approx 60 \mu A$ (when $V_{IN} = V_{RT}$). If V_{IN} is taken below V_{RB} or above V_{RT} , the input current will remain at the value corresponding to V_{RB} and V_{RT} respectively

(see Figure 4). However, V_{IN} must be maintained within the absolute range of ± 2.5 volts (with respect to ground) — otherwise excessive currents will result at Pin 6.

The input capacitance at Pin 6 is typically 22 pF, and is constant as V_{IN} varies from V_{RT} to V_{RB} .

The source impedance of the signal voltage should be maintained below 100 Ω (at the frequencies of interest) in order to avoid sampling errors.

REFERENCE

The reference resistor ladder is composed of a string of equal value resistors so as to provide 128 equally spaced voltages for the comparators (see Figure 12 for the actual configuration). The voltage difference between adjacent comparators corresponds to 1 LSB of the input range. The first comparator (closest to V_{RB}) is referenced 1/2 LSB above V_{RB} , and the 128th comparator (for the overrange) is referenced 1/2 LSB below V_{RT} . The total resistance of the ladder is nominally 140 Ω , $\pm 25\%$, requiring 14.3 mA @ 2.0 volts and 7.14 mA @ 1.0 volt. There is a nominal warm up change of $\approx +8.0\%$ in the ladder resistance due to the $+0.29\%/^{\circ}C$ temperature coefficient.

The minimum recommended span [$V_{RT} - V_{RB}$] is 1.0 volt. A lower span will allow offsets and nonlinearities to become significant. The maximum recommended span is 2.1 volts due to power limitations of the resistor ladder. The span may be anywhere within the range of -2.1 to $+2.1$ volts with respect to ground, and V_{RB} must be at least 1.3 volts more positive than V_{EE} . The reference voltages must be stable and free of noise and spikes, since the accuracy of a conversion is directly related to the quality of the reference.

In most applications, the reference voltages will remain fixed. In applications involving a varying reference for modulation or signal scrambling, the modulating signal may be applied to V_{RT} , or V_{RB} , or both. The output will vary inversely with the reference signal, introducing a nonlinearity into the transfer function. The addition of the modulating signal and the dc level

applied to the reference must be such that the absolute voltage at V_{RT} and V_{RB} are maintained within the values listed in the Recommended Operating Limits. The RMS value of the span must be maintained ≤ 2.1 volts.

POWER SUPPLIES

$V_{CC}(A)$ (Pin 9) is the positive power supply for the comparators, and $V_{CC}(D)$ (Pins 10, 16) is the positive power supply for the digital portion. Both are to be $+5.0$ volts, $\pm 10\%$, and the two are to be within 100 millivolts of each other. There is indirect internal coupling between $V_{CC}(D)$ and $V_{CC}(A)$. If they are powered separately, and one supply fails, there will be current flow through the MC10321 to the failed supply.

$I_{CC}(A)$ is nominally 13 mA, and does not vary with clock frequency or with V_{IN} , but does vary slightly with $V_{CC}(A)$. $I_{CC}(D)$ is nominally 60 mA, and is independent of clock frequency. It does vary, however, by 4–5 mA as V_{IN} is varied from V_{RT} to V_{RB} , and varies directly with $V_{CC}(D)$.

V_{EE} is the negative power supply for the comparators, and is to be within the range -3.0 to -6.0 volts. Additionally, V_{EE} must be at least 1.3 volts more negative than V_{RB} . I_{EE} is a nominal -13 mA, and is independent of clock frequency, V_{IN} and V_{EE} .

For proper operation, the supplies must be bypassed at the IC. A 10 μ F tantalum, in parallel with a 0.1 μ F ceramic is recommended for each supply to ground.

DIGITAL SECTION

CLOCK

The Clock input (Pin 15) is TTL compatible with a typical frequency range of 0 to 30 MHz. There is no duty cycle limitation, but the minimum low and high times must be adhered to. See Figure 6 for the input current requirements.

The conversion sequence is shown in Figure 13, and is as follows:

- On the rising edge, the data output latches are latched with old data, and the comparator output latches are released to follow the input signal (V_{IN}).

- During the high time, the comparators track the input signal. The data output latches retain the old data.

- On the falling edge, the comparator outputs are latched with the data immediately prior to this edge. The conversion to digital occurs within the device, and the data output latches are released to indicate the new data in ≈ 22 ns.

- During the clock low time, the comparator outputs remain latched, and the data output latches remain transparent.

A summary of the sequence is that data present at V_{IN} just prior to the Clock falling edge is digitized and available at the data outputs immediately after that same falling edge. The minimum amount of time the data must be present prior to the clock falling edge (aperture delay) is 2.0–6.0 ns, typically 3.0 ns.

The comparator output latches provide the circuit with an effective sample-and-hold function, eliminating the need for an external sample-and-hold.

ENABLE INPUTS

The two Enable inputs (Pins 13, 14) are TTL compatible, and are used to change the data outputs (D6–D0) from active to 3-state. This capability allows cascading two MC10321s into an 8-bit configuration, connecting the outputs directly to a data bus, multiplexing multiple converters, etc. See the Applications Information section for more details. For the outputs to be active, Pin 13 must be Logic "1," and Pin 14 must be a Logic "0." Changing either input will put the outputs into the high impedance mode. The Enable inputs affect **only** the state of the outputs — they do not inhibit a conversion. Both pins have a nominal threshold of ≈ 1.2 volts, their input currents are shown in Figure 5, and their input-output timing is shown in Figure 1 and 14. Leaving either pin open is equivalent to a Logic "1," although good design practice dictates that an input should never be left open.

The Overrange output (Pin 12) is not affected by the Enable inputs as it does not have 3-state capability.

OUTPUTS

The data outputs (Pins 1–4, 12, 18–20) are TTL level outputs with high impedance capability (except Overrange). Pin 4 is the MSB (D6), and Pin 18 is the LSB (D0). The seven outputs are active as long as the Enable inputs are true ($EN = \text{high}$, $\overline{EN} = \text{low}$). The timing of the outputs relative to the Clock input and the Enable inputs is shown in Figures 1 and 14. Figures 7 and 8 indicate the output voltage versus load current, while Figure 3 indicates the leakage current when in the high impedance mode.

The output code is natural binary, depicted in Table 1.

The Overrange output (Pin 12) goes high when the input, V_{IN} , is more positive than $V_{RT} - 1/2$ LSB. This output is always active — it does not have high impedance capability. Besides used to indicate an input overrange, it is additionally used for cascading two MC10321s to form an 8-bit A/D converter (see Figure 21).

TABLE 1

Input	V_{RT}, V_{RB} (Volts)			Output Code	Overrange
	2.048, 0	+1.0 V, -1.0 V	+1.0 V, 0 V		
$>V_{RT} - 1/2$ LSB	>2.040 V	>0.9922 V	>0.9961 V	7FH	1
$V_{RT} - 1/2$ LSB	2.040 V	0.9922 V	0.9961 V	7FH	$0 \leftrightarrow 1$
$V_{RT} - 1$ LSB	2.032 V	0.9844 V	0.9922 V	7FH	0
$V_{RT} - 1 1/2$ LSB	2.024 V	0.9766 V	0.9883 V	$7E_H \leftrightarrow 7F_H$	0
Midpoint	1.024 V	0.000 V	0.5000 V	40H	0
$V_{RB} + 1/2$ LSB	8.0 mV	-0.9922 V	3.9 mV	$00_H \leftrightarrow 01_H$	0
$< V_{RB} + 1/2$ LSB	<8.0 mV	<-0.9922 V	<3.9 mV	00H	0

APPLICATIONS INFORMATION

POWER SUPPLIES, GROUNDING

The PC board layout, and the quality of the power supplies and the ground system at the IC are very important in order to obtain proper operation. Noise, from any source, coming into the device on V_{CC} , V_{EE} , or ground can cause an incorrect output code due to interaction with the analog portion of the circuit. At the same time, noise generated within the MC10321 can cause incorrect operation if that noise does not have a clear path to ac ground.

Both the V_{CC} and V_{EE} power supplies must be decoupled to ground at the IC (within 1" max) with a 10 μ F tantalum and a 0.1 μ F ceramic. Tantalum capacitors are recommended since electrolytic capacitors simply have too much inductance at the frequencies of interest. The quality of the V_{CC} and V_{EE} supplies should then be checked at the IC with a high frequency scope. Noise spikes (always present when digital circuits are present) can easily exceed 400 mV peak, and if they get into the analog portion of the IC, the operation can be disrupted. Noise can be reduced by inserting resistors and/or inductors between the supplies and the IC.

If switching power supplies are used, there will usually be spikes of 0.5 volts or greater at frequencies of 50–200 kHz. These spikes are generally more difficult to reduce because of their greater energy content. In extreme cases, 3-terminal regulators (MC78L05ACP, MC7905.2CT), with appropriate high frequency filtering, should be used and dedicated to the MC10321.

The ripple content of the supplies should not allow their magnitude to exceed the values in the Recommended Operating Limits.

The PC board tracks supplying V_{CC} and V_{EE} to the MC10321 should preferably not be at the tail end of the bus distribution, after passing through a maze of digital circuitry. The MC10321 should be close to the power supply, or the connector where the supply voltages enter the board. If the V_{CC} and V_{EE} lines are supplying considerable current to other parts of the boards, then it is preferable to have dedicated lines from the supply or connector directly to the MC10321.

The two ground pins (11, 17) must be connected directly together. Any long path between them can cause stability problems due to the inductance (@ 25 MHz) of the PC tracks. The ground return for the signal source must be noise free.

REFERENCE VOLTAGE CIRCUITS

Since the accuracy of the conversion is directly related to the quality of the references, it is imperative that accurate and stable voltages be provided to V_{RT} and V_{RB} . If the reference span is 2.0 volts, then 1/2 LSB is only 7.8 millivolts, and it is desirable that V_{RT} and V_{RB} be accurate to within this amount, and furthermore, that they do not drift more than this amount once set. Over

the temperature range of -40 to $+85^{\circ}\text{C}$, a maximum temperature coefficient of 31 ppm/ $^{\circ}\text{C}$ is required.

The voltage supplies used for digital circuits should preferably **not** be used as a source for generating V_{RT} and V_{RB} , due to the noise spikes (up to 500 mV) present on the supplies and on their ground lines. Generally ± 15 volts, or ± 12 volts, are available for analog circuits, and are usually clean compared to supplies used for digital circuits, although ripple may be present in varying amounts. Ripple is easier to filter out than spikes, however, and so these supplies are preferred.

Figure 15 depicts a circuit which can provide an extremely stable voltage to V_{RT} at the current required (the maximum reference current is 20 mA @ 2.0 volts). The MC1403 series of references have very low temperature coefficients, good noise rejection, and a high initial accuracy, allowing the circuit to be built without an adjustment pot if the V_{RT} voltage is to remain fixed at one value. Using 0.1% wirewound resistors for the divider provides sufficient accuracy and stability in many cases. Alternately, resistor networks provide high ratio accuracies, and close temperature tracking. If the application requires V_{RT} to be changed periodically, the two resistors can be replaced with a 20 turn, cermet potentiometer. Wirewound potentiometers should not be used for this type of application since the pot's slider jumps from winding to winding, and an exact setting can be difficult to obtain. Cermet pots allow for a smooth continuous adjustment.

In Figure 15, R1 reduces the power dissipation in the transistor, and can be carbon composition. The 0.1 μ F capacitor in the feedback path provides stability in the unity gain configuration. Recommended op amps are: LM358, MC34001 series, LM308A, LM324, and LM11C. Offset drift is the key parameter to consider in choosing an op amp, and the LM308A has the lowest drift of those mentioned. Bypass capacitors are not shown in Figure 15, but should always be provided at the input to the 2.5 volt reference, and at the power supply pins of the op amp.

Figure 16 shows a simpler and more economical circuit, using the LM317LZ regulator, but with lower initial accuracy and temperature stability. The op amp/current booster is not needed since the LM317LZ can supply the current directly. In a well controlled environment, this circuit will suffice for many applications. Because of the lower initial accuracy, an adjustment pot is a necessity.

Figure 17 shows two circuits for providing the voltage to V_{RB} . The circuits are similar to those of Figures 15 and 16, and have similar accuracy and stability. The MC1403 reference is used in conjunction with an op amp configured as an inverter, providing the negative voltage. The output transistor is a PNP in this case since the circuit must sink the reference current.

VIDEO APPLICATIONS

The MC10321 is suitable for digitizing video signals directly without signal conditioning, although the standard 1.0 volt p-p video signal can be amplified to a 2.0 volt p-p signal for slightly better accuracy. Figure 18 shows the input (top trace) and reconstructed output of a standard NTSC test signal, sampled at 25 MSPS, consisting of a sync pulse, 3.58 MHz color burst, a 3.58 MHz signal in a Sin^2x envelope, a pulse, a white level signal, and a black level signal. Figure 19 shows a Sin^2x pulse that has been digitized and reconstructed at 25 MSPS. The width of the pulse is ≈ 225 ns at the base. Figure 20 shows an application circuit for digitizing video.

8-BIT A/D CONVERTER

Figure 21 shows how two MC10321s can be connected to form an 8-bit converter. In this configuration, the outputs (D6–D0) of the two 7-bit converters are paralleled. The outputs of one device are active, while the outputs of the other are in the 3-state mode. The selection is made by the OVERRANGE output of the lower MC10321, which controls Enable inputs on the two devices. Additionally, this output provides the 8th bit.

The reference ladders are connected in series, providing the 256 steps required for 8 bits. The input voltage range is determined by V_{RT} of the upper MC10321, and V_{RB} of the lower device. A minimum of 1.0 volt is required across each converter. The 500 Ω pot (20 turn cermet) allows for adjustment of the midpoint since the reference resistors of the two MC10321s may not be identical in value. Without the adjustment, a nonequal

voltage division could occur, resulting in a nonlinear conversion. If the references are to be symmetrical about ground (e.g., ± 1.0 volt or ± 2.0 volts), the adjustment can be eliminated, and the midpoint connected to ground.

The use of latches on the outputs is optional, depending on the application. If latches are required, SN74LS173As are recommended.

50 MHz, 7 BIT A/D CONVERTER

Figure 22 shows how two MC10321s can be connected together in a flip-flop arrangement in order to have an effective conversion speed of 50 MHz. The 74F74D-type flip-flop provides a 25 MHz clock to each converter, and at the same time, controls the SELECT input to the MC74F257 multiplexers to alternately select the outputs of the two converters. A brief timing diagram is shown in the figure.

NEGATIVE VOLTAGE REGULATOR

In the cases where a negative power supply is not available — neither the -3.0 to -6.0 volts, nor a higher negative voltage from which to derive it — the circuit of Figure 23 can be used to generate -5.0 volts from the $+5.0$ volts supply. The PC board space required is small (≈ 2.0 in²), and it can be located physically close to the MC10321. The MC34063 is a switching regulator, and in Figure 23 is configured in an inverting mode of operation. The regulator operating specifications are given in the figure.

6

GLOSSARY

APERTURE DELAY — The time difference between the sampling signal (typically a clock edge) and the actual analog signal converted. The actual signal converted may occur before or after the sampling signal, depending on the internal configuration of the converter.

BIPOLAR INPUT — A mode of operation whereby the analog input (of an A-D), or output (of a DAC), includes both negative and positive values. Examples are -1.0 to $+1.0$ V, -5.0 to $+5.0$ V, -2.0 to $+8.0$ V, etc.

BIPOLAR OFFSET ERROR — The difference between the actual and ideal locations of the 00_H to 01_H transition, where the ideal location is $1/2$ LSB above the most negative reference voltage.

BIPOLAR ZERO ERROR — The error (usually expressed in LSBs) of the input voltage location (of a 7-bit A/D) of the 40_H to 41_H transition. The ideal location is $1/2$ LSB above zero volts in the case of an A/D set up for a symmetrical bipolar input (e.g., -1.0 to $+1.0$ V).

DIFFERENTIAL NONLINEARITY — The maximum deviation in the actual step size (one transition level to

another) from the ideal step size. The ideal step size is defined as the Full Scale Range divided by 2^n (n = number of bits). This error must be within ± 1 LSB for proper operation.

FULL SCALE RANGE (ACTUAL) — The difference between the actual minimum and maximum end points of the analog input (of an A-D).

FULL SCALE RANGE (IDEAL) — The difference between the actual minimum and maximum end points of the analog input (of an A-D), plus one LSB.

GAIN ERROR — The difference between the actual and expected gain (end point to end point), with respect to the reference of a data converter. The gain error is usually expressed in LSBs.

GREY CODE — Also known as **reflected binary code**, it is a digital code such that each code differs from adjacent codes by only one bit. Since more than one bit is never changed at each transition, race condition errors are eliminated.

INTEGRAL NONLINEARITY — The maximum error of an A/D, or DAC, transfer function from the ideal straight line connecting the analog end points. This parameter is sensitive to dynamics, and test conditions must be specified in order to be meaningful. This parameter is the best overall indicator of the device's performance.

LSB — Least Significant Bit. It is the lowest order bit of a binary code.

LINE REGULATION — The ability of a voltage regulator to maintain a certain output voltage as the input to the regulator is varied. The error is typically expressed as a percent of the nominal output voltage.

LOAD REGULATION — The ability of a voltage regulator to maintain a certain output voltage as the load current is varied. The error is typically expressed as a percent of the nominal output voltage.

MONOTONICITY — The characteristic of the transfer function whereby increasing the input code (of a DAC), or the input signal (of an A/D), results in the output never decreasing.

MSB — Most Significant Bit. It is the highest order bit of a binary code.

NATURAL BINARY CODE — A binary code defined by:

$$N = A_n 2^n + \dots + A_3 2^3 + A_2 2^2 + A_1 2^1 + A_0 2^0$$

where each "A" coefficient has a value of 1 or 0. Typically, all zeroes corresponds to a zero input voltage of an A/D, and all ones corresponds to the most positive input voltage.

NYQUIST THEORY — See Sampling Theorem.

OFFSET BINARY CODE — Applicable only to bipolar input (or output) data converters, it is the same as Natural Binary, except that all zeroes corresponds to the most negative input voltage (of an A/D), while all ones corresponds to the most positive input.

POWER SUPPLY SENSITIVITY — The change in a data converters performance with changes in the power supply voltage(s). This parameter is usually expressed in percent of full scale versus ΔV .

QUANTIZATION ERROR — Also known as digitization error or uncertainty. It is the inherent error involved in digitizing an analog signal due to the finite number of steps at the digital output versus the infinite number of values at the analog input. This error is a minimum of $\pm 1/2$ LSB.

RESOLUTION — The smallest change which can be discerned by an A/D converter, or produced by a DAC. It is usually expressed as the number of bits, n , where the converter has 2^n possible states.

SAMPLING THEOREM — Also known as the Nyquist Theorem. It states that the sampling frequency of an A/D must be no less than $2x$ the highest frequency (of interest) of the analog signal to be digitized in order to preserve the information of that analog signal.

UNIPOLAR INPUT — A mode of operation whereby the analog input range (of an A/D), or output range (of a DAC), includes values of a single polarity. Examples are 0 to +2.0 V, 0 to -5.0 V, +2.0 to +8.0 V, etc.

UNIPOLAR OFFSET ERROR — The difference between the actual and ideal locations of the 00_H to 01_H transition, where the ideal location is $1/2$ LSB above the most negative input voltage.

FIGURE 11 — DIFFERENTIAL PHASE AND GAIN TEST

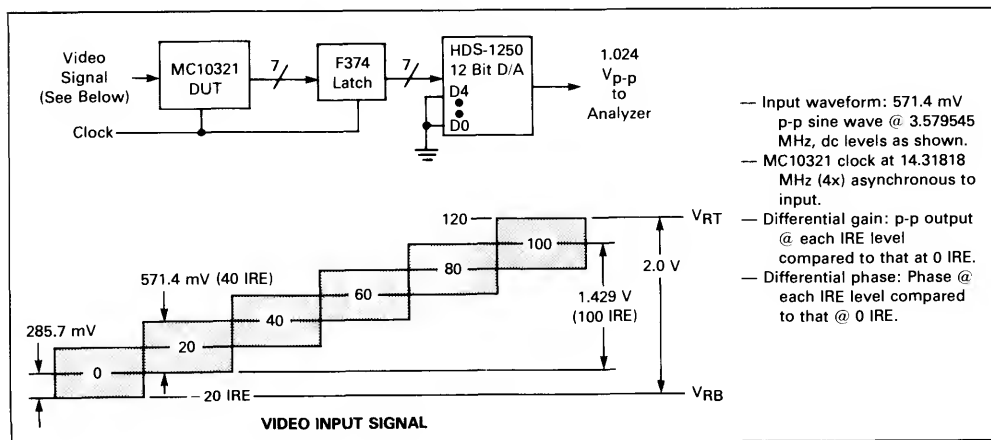
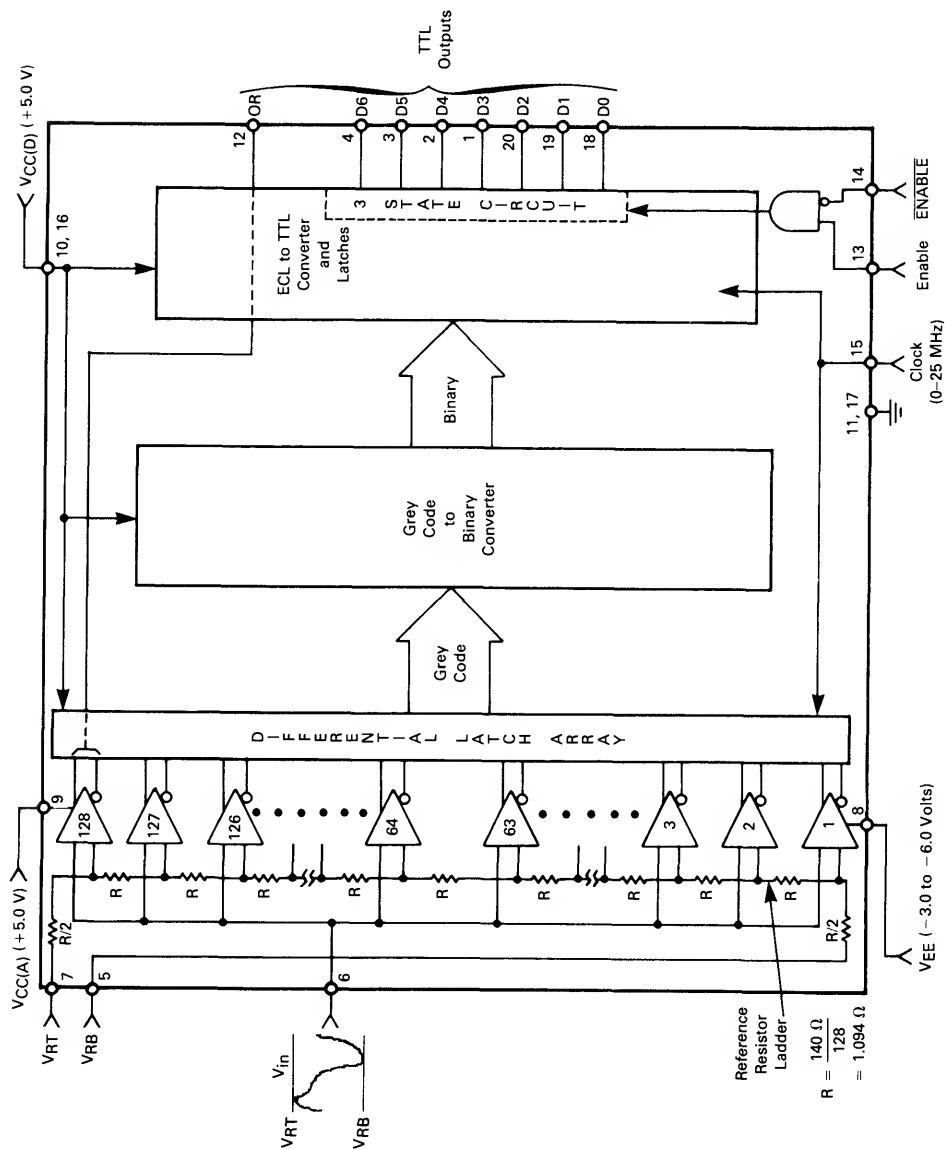


FIGURE 12 — MC10321



MC10321

FIGURE 13 — CONVERSION SEQUENCE

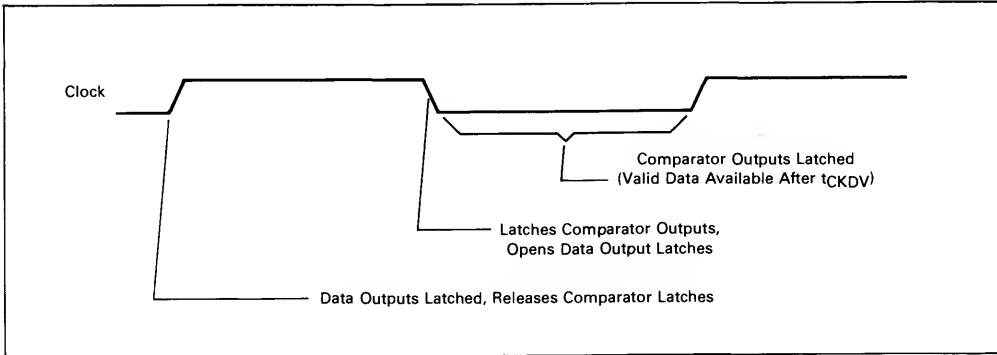


FIGURE 14 — ENABLE TO OUTPUT CRITICAL TIMING

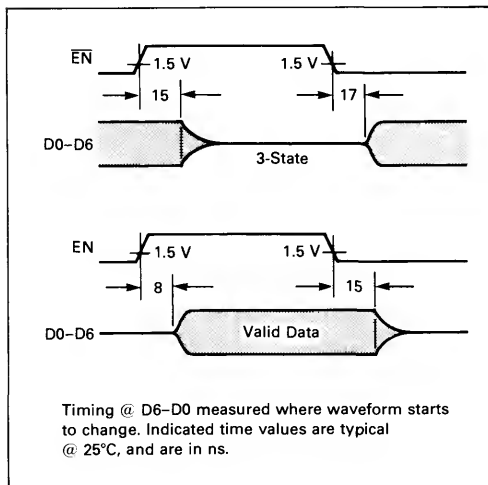


FIGURE 15 — PRECISION V_{RT} VOLTAGE SOURCE

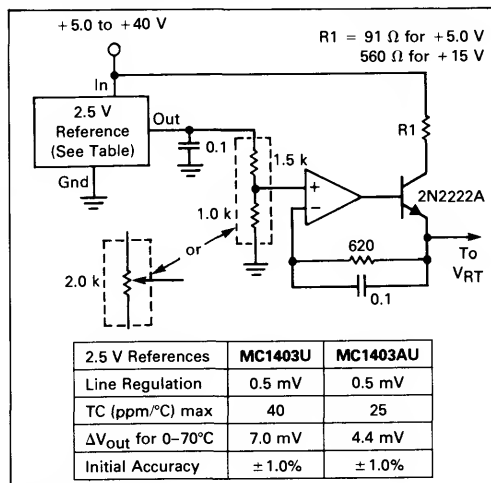
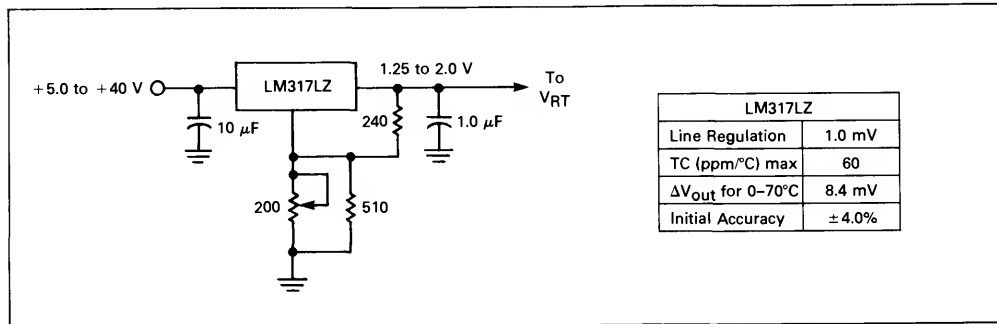


FIGURE 16 — V_{RT} VOLTAGE SOURCE



MC10321

FIGURE 17 — V_{RB} VOLTAGE SOURCES

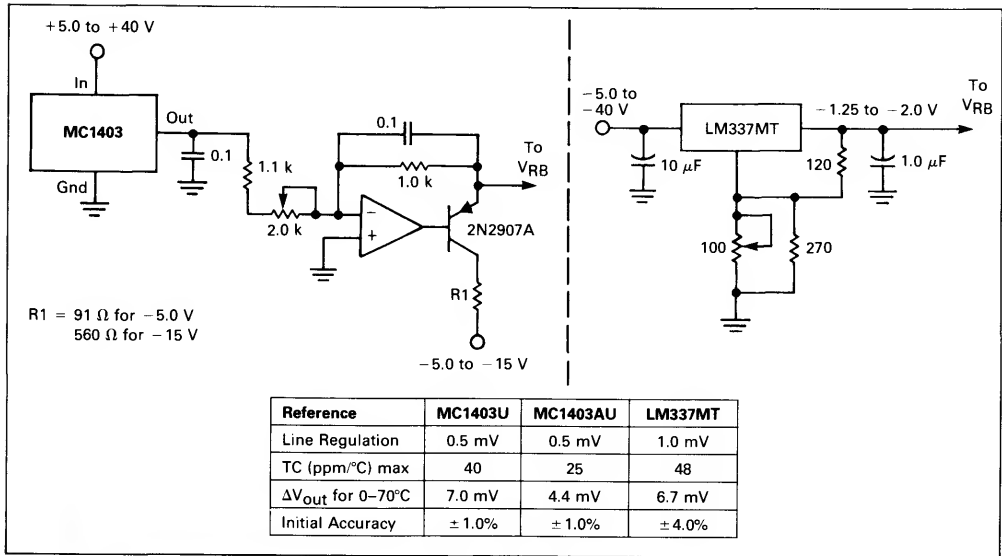


FIGURE 18

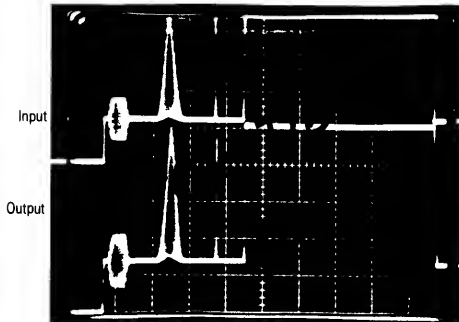
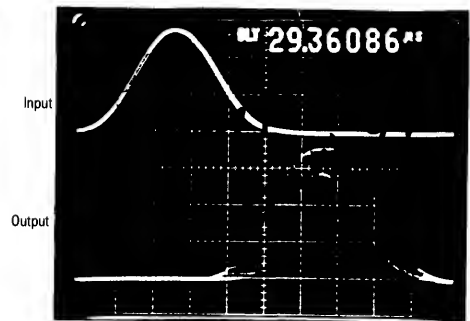
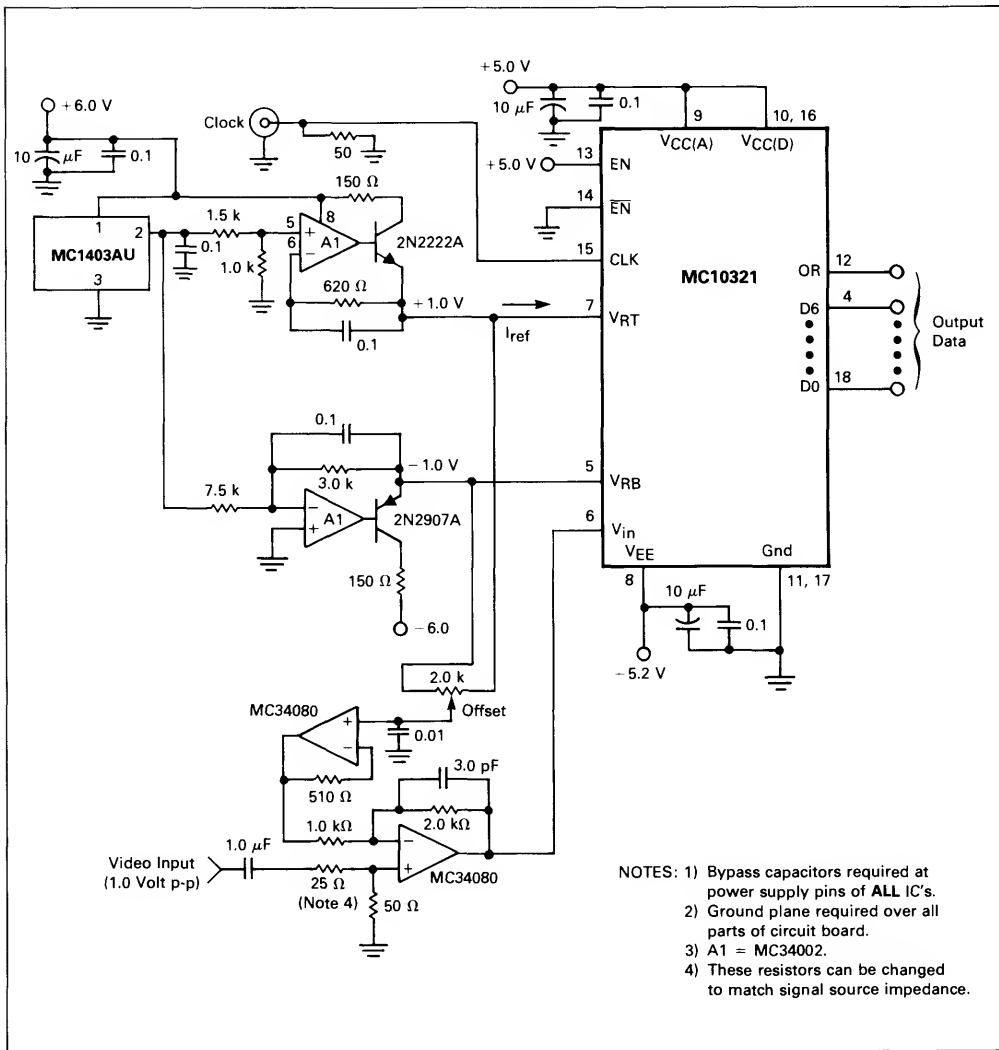


FIGURE 19



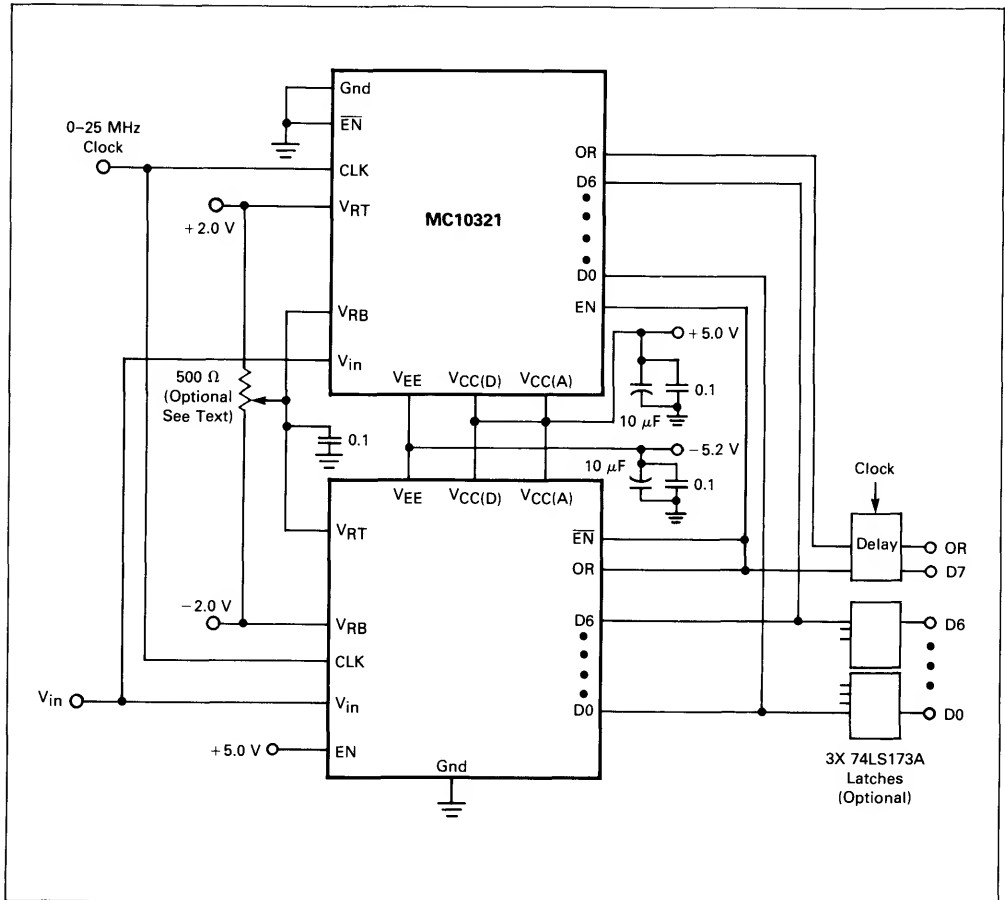
MC10321

FIGURE 20 — APPLICATION CIRCUIT FOR DIGITIZING VIDEO



MC10321

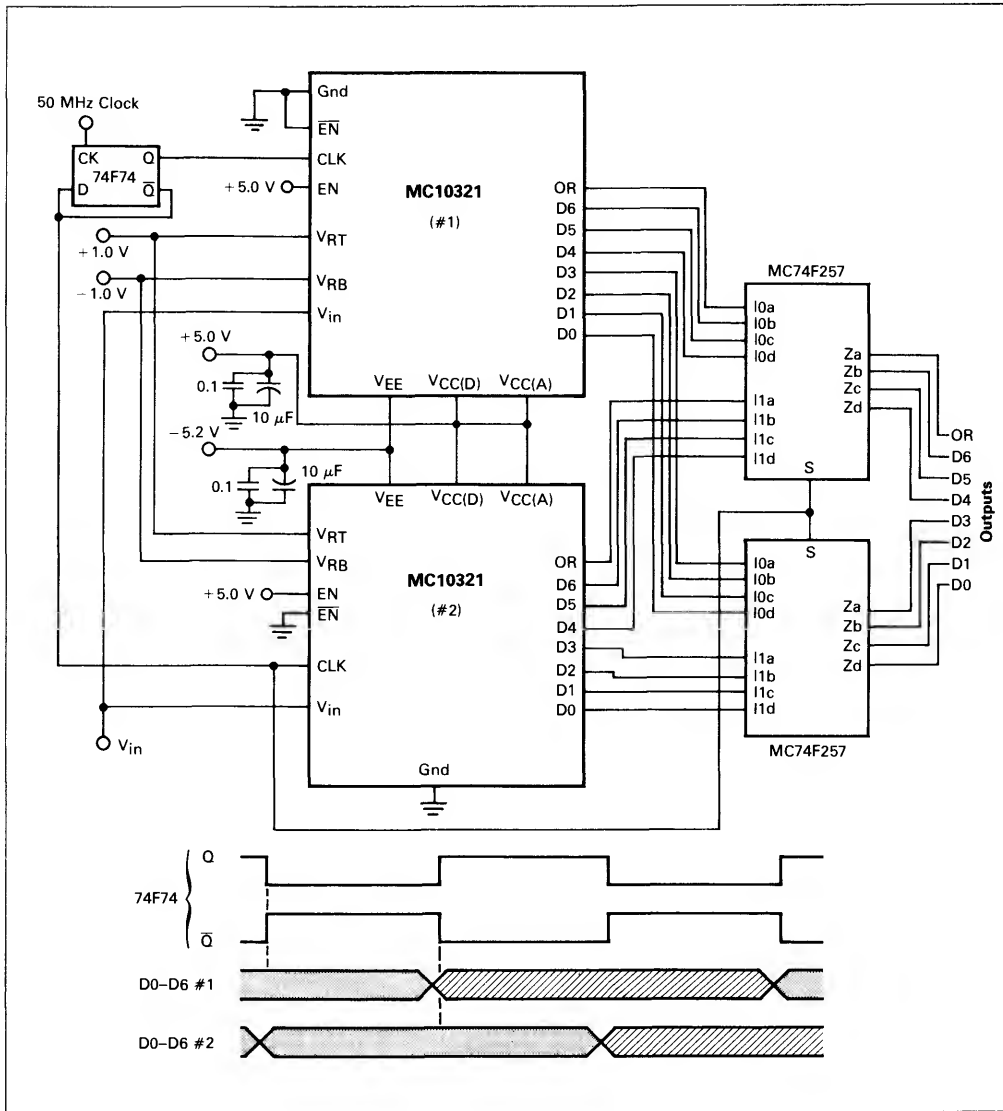
FIGURE 21 — 8-BIT A/D CONVERTER



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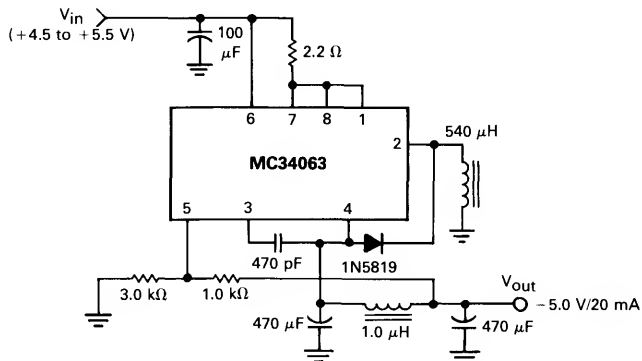
MC10321

FIGURE 22 — 50 MHz 7 BIT A/D CONVERTER



MC10321

FIGURE 23 — -5.0 VOLT REGULATOR



Line Regulation	$4.5\text{ V} < V_{in} < 5.5\text{ V}$, $I_{out} = 10\text{ mA}$	0.16%
Load Regulation	$V_{in} = 5.0\text{ V}$, $8.0\text{ mA} < I_{out} < 20\text{ mA}$	0.4%
Output Ripple	$V_{in} = 5.0\text{ V}$, $I_{out} = 20\text{ mA}$	2.0 mV p-p
Short Circuit I_{out}	$V_{in} = 5.0\text{ V}$, $R_L = 0.1\text{ Ω}$	140 mA
Efficiency	$V_{in} = 5.0\text{ V}$, $I_{out} = 50\text{ mA}$	52%

Product Preview

8-BIT VIDEO DAC WITH TTL INPUTS

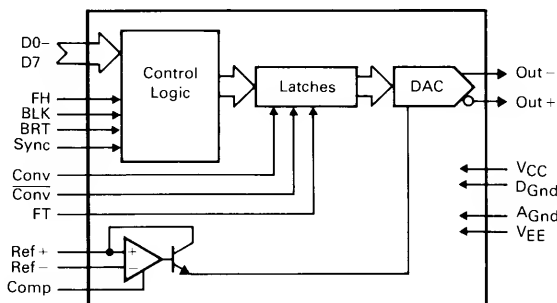
The MC10322 is a 40 MegaSample Per Second (MSPS) 8-bit video DAC capable of directly driving a 75 ohm cable with appropriate terminations to EIA-170 and EIA-343-A video levels. The logic inputs (data and controls) are TTL compatible. Input buffers negate the need for external latches, unless the transparent mode is selected.

Video controls (Force High, Blank, Bright, and Sync) permit an easy interface to standard video systems. The Clock (Convert) inputs can be differential or single-ended. Complementary outputs are provided for custom displays or special effects.

The MC10322 is fabricated with Motorola's MOSAIC process which provides high speed with low power consumption. The MC10322 is available in a 24 pin plastic DIP package.

- 40 MSPS Minimum Conversion Rate
- TTL Compatible Inputs
- 8-Bit Linearity
- Latched Data and Video Control Inputs, or Transparent Mode
- Video Controls: Force High, Blank, Bright, Sync.
- Differential Current Outputs Can Each Drive 0–60 Ohms
- Modulation Capability (Multiplying Mode)
- PSRR > 60 dB
- Operates from +5.0 and –5.2 V Power Supplies
- Power Dissipation: Typically 359 mW
- Available in 24 Pin Plastic DIP Package

BLOCK DIAGRAM

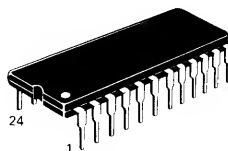


This document contains information on a new product. Specifications and information herein are subject to change without notice. Specifications listed are target specifications only. MOSAIC is a trademark of Motorola, Inc.

MC10322

8-BIT VIDEO DAC WITH TTL INPUTS

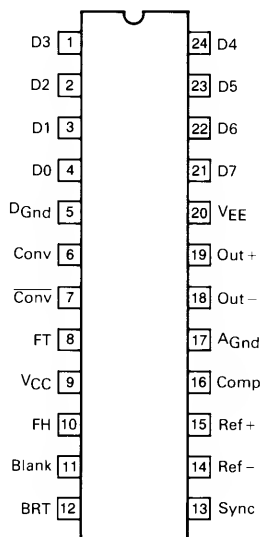
**SILICON MONOLITHIC
INTEGRATED CIRCUIT**



P SUFFIX
PLASTIC PACKAGE
CASE 649

6

PIN CONNECTIONS



(Top View)

Product Preview

8-BIT VIDEO DAC WITH TTL INPUTS

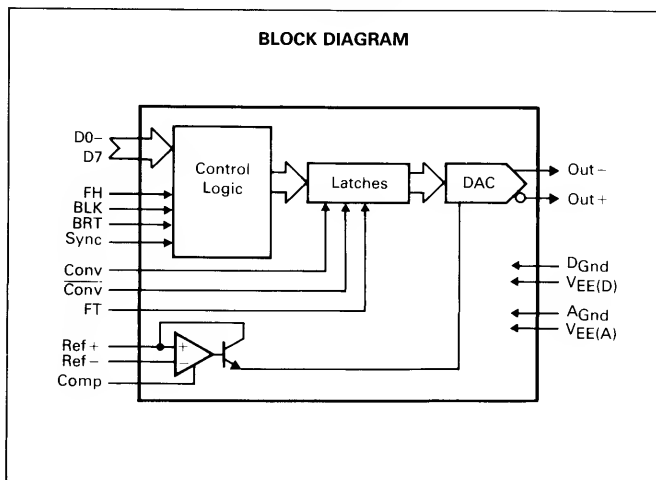
The MC10324 is a 40 MegaSample Per Second (MSPS) 8-bit video DAC capable of directly driving a 75 ohm cable with appropriate terminations to EIA-170 and EIA-343-A video levels. The logic inputs (data and controls) are ECL compatible. Input buffers negate the need for external latches, unless the transparent mode is selected.

Video controls (Force High, Blank, Bright, and Sync) permit an easy interface to standard video systems. The Clock (Convert) inputs can be differential or single-ended. Complementary outputs are provided for custom displays or special effects.

The MC10324 is fabricated with Motorola's MOSAIC process which provides high speed with low power consumption. The MC10324 is available in a 24 pin plastic DIP package.

- 40 MSPS Minimum Conversion Rate
- ECL Compatibility
- 8-Bit Linearity
- Latched Data and Video Control Inputs, or Transparent Mode
- Video Controls: Force High, Blank, Bright, Sync.
- Differential Current Outputs Can Each Drive 0–60 Ohms
- Modulation Capability (Multiplying Mode)
- PSRR >60 dB
- Operates from –5.2 V Power Supply
- Power Dissipation: Typically 348 mW
- Available in 24 Pin Plastic DIP Package
- Pin Compatible with TRW's TDC1018

BLOCK DIAGRAM

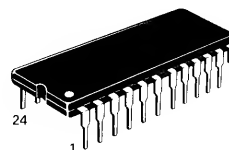


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MC10324

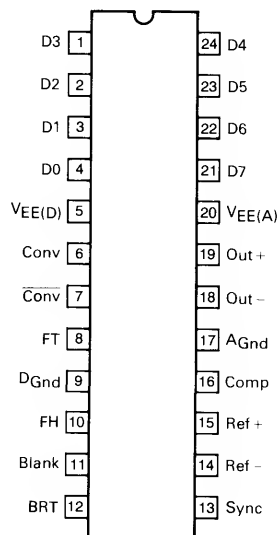
8-BIT VIDEO DAC WITH ECL INPUTS

SILICON MONOLITHIC INTEGRATED CIRCUIT

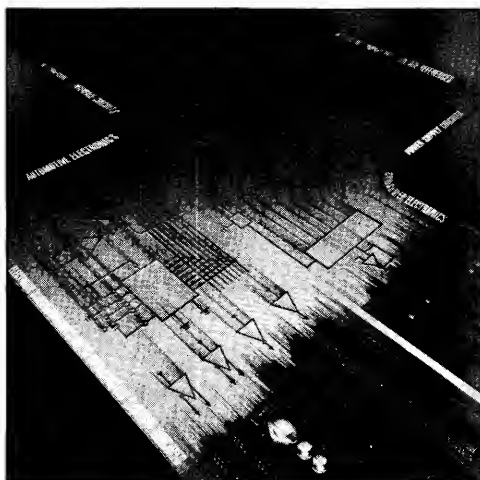


P SUFFIX
PLASTIC PACKAGE
CASE 649

PIN CONNECTIONS



(Top View)



In Brief . . .

Described in this section is Motorola's line of interface circuits, which provide the means for interfacing microprocessor or digital systems to the external world, or to other systems.

Included are devices for reading and writing to a floppy disk or tape drive system, devices which allow a microprocessor to communicate with its own array of memory and peripheral I/O circuits.

The line drivers, receivers, and transceivers permit communications between systems over cables of several thousand feet in length, and at data rates of up to several megahertz. The common EIA data transmission standards, several European standards, IEEE-488, and IBM 360/370 are addressed by these devices.

The peripheral drivers are designed to handle high current loads such as relay coils, lamps, stepper motors, and others. Input levels to these drivers can be TTL, CMOS, High Voltage MOS, or other user defined levels. The display drivers are designed for LCD, LED, incandescent and other types of displays, and provide various forms of decoding.

Interface Circuits

Selector Guide

Magnetic Read/Write Interface and Control.	7-2
Microprocessor Bus Interface.	7-4
Single-Ended Bus Transceivers.	7-5
Line Receivers.	7-5
Line Drivers	7-6
Line Transceivers	7-6
Peripheral Drivers.	7-7
Alphanumeric Listing	7-8
Related Application Notes	7-9
Data Sheets	7-10

Interface Circuits

Magnetic Read/Write Interface and Control

Motorola's line of circuits in this category are well established industry standards for reading and writing in a floppy disk system. The write circuits are designed for both straddle erase and tunnel erase heads, and provide

both the writing and erasing functions. The read circuits include all circuitry for peak detection, filtering, wave shaping, and guaranteed peak shift specifications.

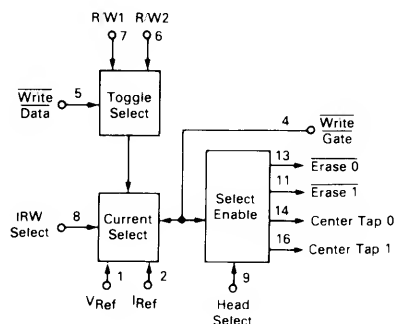
Floppy Disk Write Controllers

Straddle Erase Controller

MC3469P — $T_A = 0^\circ$ to $+70^\circ\text{C}$, Case 648

Designed to provide the entire interface between floppy disk heads and the head control and write data signals for straddle-erase heads.

Provisions are made for selecting a range of accurately controlled write currents and for head selection during both read and write operation. Additionally, provisions are included for externally adjusting degauss period and inner/outer track compensation.

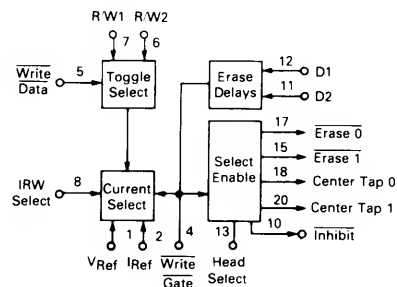


Tunnel/Straddle Erase Controller

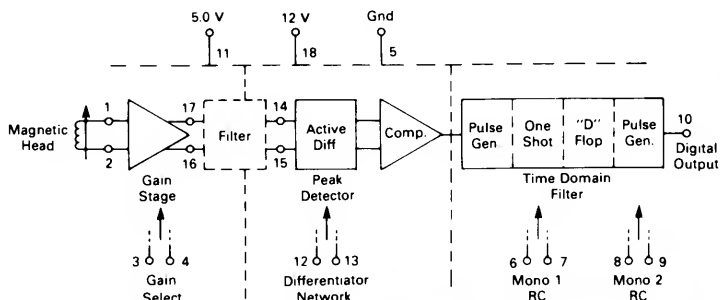
MC3471P — $T_A = 0^\circ$ to $+70^\circ\text{C}$, Case 738

Provides the entire interface between the write data and head control signals and the heads (write and erase) for either tunnel or straddle-erase floppy disk systems.

Has provisions for external adjustment of degauss period, inner/outer track compensation, and the delay from write gate to erase turn-on and turn-off.



Floppy Disk Read Amplifier System



MC3470P,AP — $T_A = 0^\circ$ to $+70^\circ\text{C}$, Case 707

Designed as monolithic Read Amplifier System for obtaining digital information from floppy disk storage. These devices accept differential ac signals produced by the magnetic head and provides a digital output pulse that corresponds to each peak of the input signal. A gain stage amplifies the input waveform and applies it to an external filter network, enabling the active differentiator and time domain filter to produce the desired output. These devices provide all the active circuitry to perform the floppy disk Read amplifier function, and guarantee to have a maximum peak shift of 5.0%, adjustable to zero, for the MC3470P and 2.0%, adjustable to zero, for the MC3470AP.

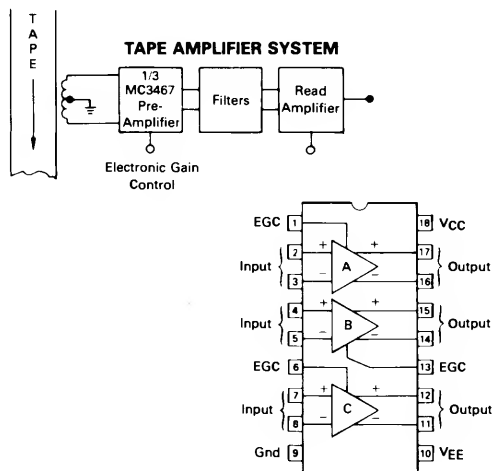
Device	Peak Shift ($f = 250\text{ kHz}$, $V_{ID} = 1.0\text{ V}_{pp}$)	Differential Input Voltage Gain ($f = 200\text{ kHz}$, $V_{ID} = 5.0\text{ mV [RMS]}$)		Input Common Mode Range (5% Max THD)	
		V/V		V	
	% Max	Min	Max	Min	Max
MC3470P	5.0	80	130	-0.1	1.5
MC3470AP	2.0	100	130		

Magnetic Tape Sense Amplifier

MC3467P — $T_A = 0^\circ$ to $+70^\circ\text{C}$, Case 707

The MC3467 provides three independent preamplifiers with individual electronic gain control, optimized for use in 9-track magnetic tape memory systems where low noise and low distortion are paramount objectives.

The electronic gain control allows each amplifier's gain to be set anywhere from essentially zero to a maximum of approximately 100 V/V. Minimum small-signal bandwidth is 10 MHz, and Common-Mode Input Voltage range is 1.5 V min.



Microprocessor Bus Interface

Motorola offers a spectrum of line drivers and receivers which provide interfaces to many industry standard specifications. Many of the devices add key

operational features, such as hysteresis, short circuit protection, clamp diode protection, or special control functions.

Address and Control Bus Extenders

These devices are designed to extend the drive capabilities of today's standard microprocessors. All devices are fabricated with Schottky TTL technology for high speed.

VOL(max) @ 48 mA	VOH(min) @ -5.2 mA	Propagation Delay Max (ns)	Buffers Per Package	Device	Package Suffix	Comments
0.5	2.4	13	6	MC8T95/ MC6885	L/620 P/648	Noninverting
0.5	2.4	11	6	MC8T96/ MC6886	L/620 P/648	Inverting
0.5	2.4	13	6	MC8T97/ MC6887	L/620 P/648	Noninverting
0.5	2.4	11	6	MC8T98/ MC6888	L/620 P/648	Inverting

Hex 3-State Buffers/Inverters — $T_A = 0^\circ$ to $+75^\circ\text{C}$

These devices differ in that the noninverting MC8T95/MC6885 and inverting MC8T96/MC6886 provide a two-input Enable which controls all six buffers, while the noninverting MC8T97/MC6887 and inverting MC8T98/MC6888

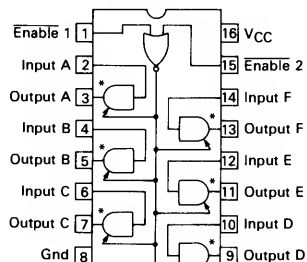
provide two Enable inputs — one controlling four buffers and the other controlling the remaining two buffers.

#These devices may be ordered by either of the paired numbers.

MC8T95/MC6885# — Noninverting

MC8T96/MC6886# — Inverting

Two-input Enable controls all six buffers.

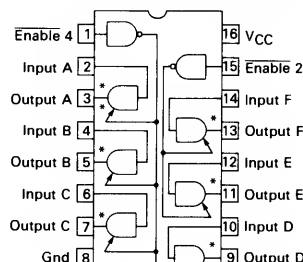


*Add inverter for
MC6886/MC8T96.

MC8T97/MC6887# — Noninverting

MC8T98/MC6888# — Inverting

Two Enable inputs, one controlling four buffers and the other controlling the remaining two buffers.



*Add inverter for
MC6888/MC8T98.

Microprocessor Data Bus Extenders

Driver Characteristics		Receiver Characteristics	Transceivers Per Package	Device	Package Suffix	Comments
Output Current (mA)	Propagation Delay Max (ns)	Propagation Delay Max (ns)				
48	14	14	4	MC8T26A (MC6880A)	P/648 L/620	Inverting Logic
48	17	17	4	MC8T28 (MC6889)	P/648 L/620	Noninverting Logic

Single-Ended Bus Transceivers

For Instrumentation Bus, Meets GPIB/IEEE Standard 488

Driver Characteristics		Receiver Characteristics	Transceivers Per Package	Device	Package Suffix	Comments
Output Current (mA)	Propagation Delay Max (ns)	Propagation Delay Max (ns)				
48	50	50	4	MC3446A	P 648	MOS Compatible, Input Hysteresis
48	30	50	8	MC3447	P3 724 L 623 P 649	Input Hysteresis, Open Collector, 3-State Outputs with Terminations
48	17	25	4	MC3448A	P 648 D 751B L 620	Input Hysteresis, Open Collector, 3-State Outputs with Terminations
100	30	30	4	MC3440A	P 648	Input Hysteresis, Enable for 3 Drivers
				MC3441A		Common Enable, Input Hysteresis

For High-Current Party-Line Bus for Industrial and Data Communications

100	15	15	4	MC26S10	P 648 D 751B L 620	Open Collector, Outputs, Common Enable
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Line Receivers

General-Purpose

S = Single D = Differ- ential	Type* Of Output	Prop Delay Time Max (ns)	Party- Line Opera- tion	Strobe Or Enable	Power Supplies (V)	Device	Package Suffix	Receivers Per Package	Companion Drivers	Comments
D	TP	25	Yes	Yes	+ 5	MC3450	D 751B	4	MC3453	Quad version of MC75107/8
D	OC	25	Yes	Yes	+ 5	MC3452	P 648 L 620	4		
D	TP	25	Yes	Yes	+ 5	MC75107	P 646	2	MC75S110	Dual version of MC3450/2
D	OC	25	Yes	Yes	+ 5	MC75108	L 632	2		
S	TP	30	Yes	Yes	+ 5	MC3437	P 648 L 620	6		Input Hysteresis

360/370 I/O Interface

S	TP	30	Yes	No	+ 5	MC75125 MC75127	P 648 L 620	7	MC3481 MC3485	Schottky Circuitry
S	TP	30	Yes	Yes	+ 5	MC75128 MC75129	P 738 L 732	8	MC3481 MC3485	Active high strobe Active low strobe

*OC = Open Collector, TP = Totem-pole output

EIA Standard

S = Single D = Differ- ential	Type* Of Output	Prop Delay Time Max (ns)	Party- Line Opera- tion	Strobe Or Enable	Power Supplies (V)	Device	Package Suffix	Receivers Per Package	Companion Drivers	EIA Standard
S	R	85	No	No	- 5	MC1489 MC1489A	D 751A P 648 L 632	4	MC1488	EIA-232-D
S, D	TP	30	Yes	Yes	+ 5	AM26LS32	P 648	4	AM26LS31	EIA-422/423
S, D	TP	30	Yes	Yes	+ 5	MC3486	D 751B L 620	4	MC3487	
S, D	TP	35	Yes	Yes	+ 5	SN75173	N 648	4	SN75172	EIA-422/423/485
S, D	TP	35	Yes	Yes	+ 5	SN75175	D 751B J 620	4	SN75174	

*R = Resistor Pull-up, TP = Totem-pole output

Line Drivers

General Purpose

Output Current Capability (mA)	Prop Delay Time Max (ns)	S = Single Ended D = Differential	Party-Line Operation	Strobe Or Enable	Power Supplies (V)	Device	Package Suffix	Drivers Per Package	Companion Receivers	Comments
15	15	D	Yes	Yes	± 5	MC3453	P/648 L/620	4	MC3450 MC3452	Quad version of MC75S110
15	15	D	Yes	Yes	± 5	MC75S110	P/646 L/632	2	MC75107 MC75108	Dual version of MC3453

360/370 I/O Interface

60	45	S	Yes	Yes	+ 5	MC3481	P/648 L/620	4	MC75125 MC75127	Short Circuit Fault Flag
60	45	S	Yes	Yes	+ 5	MC3485	P/648 L/620	4	MC75128 MC75129	Short Circuit Fault Flag

EIA Standard

Output Current Capability (mA)	Prop Delay Time Max (ns)	S = Single Ended D = Differential	Party-Line Operation	Strobe Or Enable	Power Supplies (V)	Device	Package Suffix	Drivers Per Package	Companion Receivers	Comments
85 85	35 35	D D	Yes Yes	Yes Yes	+ 5 + 5	SN75172 SN75174	N/648 J/620	4 4	SN75173 SN75175	EIA-485
48	20	D	Yes	Yes	+ 5	MC3487	P/648 D/751B L/620	4	MC3486	EIA-422 with 3-State Outputs
48	20	D	Yes	Yes	+ 5	AM26LS31	P/648 D/751B D/620	4	AM26LS32	
20	—	S	No	No	± 12	MC3488A (μA9636A)	P1/626 D/751B U/693	2	MC3486 AM26LS32	EIA-423/232-D
10	350	S	No	Yes	± 9 to ± 12	MC1488	P/646 D/751A L/632	4	MC1489 MC1489A	EIA-232-D
60	300	S/D		422-Yes 423-No	± 5	AM26LS30	P/648 L/620 D/751B	422-2 423-4	AM26LS32 MC3486	EIA-422 EIA-423 Switchable

Line Transceivers

Driver Prop Delay (Max ns)	Receiver Prop Delay (Max ns)	CE = Common Enable DE = Driver Enable RE = Receiver Enable	Party-Line Operation	Power Supply (V)	Device	Package Suffix	Drivers Per Package	Receivers Per Package	EIA Standard
20	30	DE, RE	Yes	+ 5	MC34050	L/620 D/751B P/648	2	2	EIA-422
20	30	DE	Yes	+ 5	MC34051	L/620 P/648	2	2	EIA-422

Peripheral Drivers

Output Current Capability (mA)	Input Capability	Propagation Delay Time Max (μ s)	Output Clamp Diode	Off State Voltage Max (V)	Device	Drivers Per Package	Package/ Suffix	Logic Function
300	TTL, DTL	1.0	Yes	70	MC1472	2	P1/626 U/693	NAND
500	TTL, CMOS, PMOS	1.0	Yes	50	ULN2801	8	A/707	Invert
500	14 V to 25 V PMOS	1.0	Yes	50	ULN2802	8	A/707	Invert
500	TTL, CMOS	1.0	Yes	50	ULN2803	8	A/707	Invert
500	6.0 V to 15 V MOS	1.0	Yes	50	ULN2804	8	A/707	Invert
500	TTL, CMOS PMOS	1.0	Yes	50	MC1411,B	7	P/648	Invert
500	14 V to 25 V PMOS	1.0	Yes	50	MC1412,B	7	P/648	Invert
500	TTL, 5.0 V CMOS	1.0	Yes	50	MC1413,B	7	P/648	Invert
500	8.0 V to 18 V MOS	1.0	Yes	50	MC1416,B	7	P/648	Invert
1500	TTL, 5.0 V CMOS	1.0	Yes	50	ULN2068B	4	B/648	Invert
1500	TTL, 5.0 V CMOS	1.0	No	50	ULN2074B	4	B/648	Collector, Emitter available at Pins

INTERFACE CIRCUITS

Memory Interface and Control

Device	Function	Page
MC3467	Triple Preamplifier	7-94
MC3469P	Floppy Disk Write Controller	7-99
MC3470P,AP	Floppy Disk Read Amplifier System	7-109
MC3471P	Floppy Disk Write Controller/Head Driver	7-123

Microprocessor Bus Interface

Device	Function	Page
MC8T26A	Quad Three-State Bus Transceiver	7-27
MC8T28	Noninverting Bus Transceiver	7-32
MC8T95	Hex Three-State Buffer/Inverter	7-37
MC8T96	Hex Three-State Buffer/Inverter	7-37
MC8T97	Hex Three-State Buffer/Inverter	7-37
MC8T98	Hex Three-State Buffer/Inverter	7-37
MC6875,A	MC6800 Clock Generator/Driver	7-150
MC6880A	Quad Three-State Bus Transceiver	7-27
MC6885	Hex Three-State Buffer/Inverter	7-37
MC6886	Hex Three-State Buffer/Inverter	7-37
MC6887	Hex Three-State Buffer/Inverter	7-37
MC6888	Hex Three-State Buffer/Inverter	7-37
MC6889	Noninverting Bus Transceiver	7-32

Single-Ended Bus Transceivers

Device	Function	Page
MC26S10	Quad Open-Collector Bus Transceiver	7-59
MC3440A	Quad Interface Bus Transceiver	7-65
MC3441A	Quad Interface Bus Transceiver	7-65
MC3446A	Quad Interface Bus Transceiver	7-69
MC3447	Bidirectional Instrumentation Bus Transceiver	7-72
MC3448A	Quad Three-State Bus Transceiver	7-78

Line Receivers

Device	Function	Page
AM26LS32	Quad EIA-422/3 Line Receiver with Three-State Outputs	7-24
MC1489,A	Quad MDTL Line Receiver	7-54
MC3437	Hex Unified Bus Receiver	7-62
MC3450	Quad Line Receiver	7-83
MC3452	Quad Line Receiver	7-83
MC3486	Quad EIA-422/423 Line Receiver	7-139
MC75107	Dual Line Receiver	7-168
MC75108	Dual Line Receiver	7-168
MC75125	Seven-Channel Line Receivers	7-178
MC75127	Seven-Channel Line Receivers	7-178
MC75128	Eight-Channel Line Receivers	7-182
MC75129	Eight-Channel Line Receivers	7-182
SN75173	Quad EIA-422A/3 Line Receiver with Three-State Output	7-188
SN75175	Quad EIA-422A/3 Line Receiver with Three-State Output	7-188

Line Drivers

Device	Function	Page
AM26LS30	Dual Differential Quad Single-Ended Line Driver	7-10
AM26LS31	Quad EIA-422 Line with Three-State Output	7-21
MC1488	Quad MDTL Line Driver	7-48
MC3453	Quad Line Driver	7-90
MC3481	Quad Single-Ended Line Driver	7-134
MC3485	Quad Single-Ended Line Driver	7-134
MC3487	Quad EIA-422 Line Driver with Three-State Outputs	7-142
MC3488A	Dual EIA-423/232C Driver	7-146
MC75S110	Dual Line Driver	7-173
SN75172	Quad EIA-485 Line Driver with Three-State Output	7-186
SN75174	Quad EIA-485 Line Driver with Three-State Output	7-186

Line Transceivers

Device	Function	Page
MC34050	Dual EIA-422/423 Transceiver	7-161
MC34051	Dual EIA-422/423 Transceiver	7-161

Peripheral Drivers

Device	Function	Page
MC1411,B	Peripheral Driver Array	7-41
MC1412,B	Peripheral Driver Array	7-41
MC1413,B	Peripheral Driver Array	7-41
MC1416,B	Peripheral Driver Array	7-41
MC1472	Dual Peripheral Positive NAND Driver	7-45
ULN2068B	Quad 1.5 A Darlington Switch	7-193
ULN2074B	Quad 1.5 A Darlington Switch	7-197
ULN2801	Octal Peripheral Driver Array	7-201
ULN2802	Octal Peripheral Driver Array	7-201
ULN2803	Octal Peripheral Driver Array	7-201
ULN2804	Octal Peripheral Driver Array	7-201

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RELATED APPLICATION NOTES

Application Note	Title	Related Device
AN708A	Line Driver and Receiver Considerations	Several
AN781A	Revised Data Interface Standards	Several
AN917	Reading and Writing in Floppy Disk Systems Using Motorola Integrated Circuits	MC3469, MC3470, MC3471

AM26LS30

Advance Information

DUAL DIFFERENTIAL (EIA-422A)/QUAD SINGLE-ENDED (EIA-423A) LINE DRIVERS

The AM26LS30 is a low power Schottky set of line drivers which can be configured as two differential drivers which comply with EIA-422-A standards, or as four single-ended drivers which comply with EIA-423-A standards. A mode select pin and appropriate choice of power supplies determine the mode. Each driver can source and sink currents in excess of 50 mA.

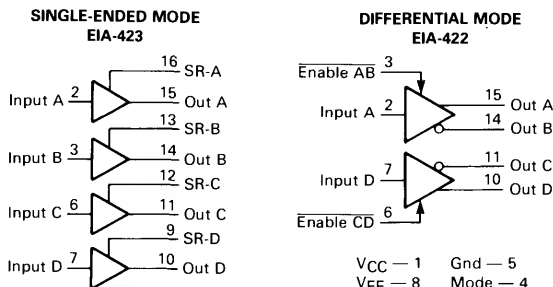
In the differential mode (EIA-422-A), the drivers can be used up to 10 Mbaud. A disable pin for each driver permits setting the outputs into a high impedance mode within a ± 10 volt common mode range.

In the single-ended mode (EIA-423-A), each driver has a slew rate control pin which permits setting the slew rate of the output signal so as to comply with EIA-423-A and FCC requirements and to reduce crosstalk. When operated from symmetrical supplies (± 5.0 volts), the outputs exhibit zero imbalance.

The AM26LS30 is available in a 16-pin plastic DIP, a ceramic package, and a SOIC surface mount package. Ambient operating temperature range is -40° to $+85^{\circ}\text{C}$.

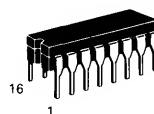
- Operates as Two Differential EIA-422-A Drivers, or Four Single-Ended EIA-423-A Drivers
- High Impedance Outputs in Differential Mode
- Short Circuit Current Limit in Both Source and Sink Modes
- ± 10 Volts Common Mode Range on High Impedance Outputs
- $+15$ Volt Range on Inputs
- Low Current PNP Inputs Compatible with TTL, CMOS, and MOS Outputs
- Individual Output Slew Rate Control in Single-Ended Mode
- Operating Ambient Temperature: -40° to $+85^{\circ}\text{C}$
- Available in Three Package Types
- Replacement for the AMD AM26LS30 and National Semiconductor DS3691

BLOCK DIAGRAMS



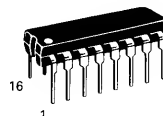
DUAL DIFFERENTIAL/ QUAD SINGLE-ENDED LINE DRIVERS

SILICON MONOLITHIC INTEGRATED CIRCUIT



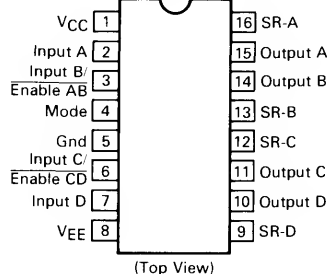
DC SUFFIX
 CERAMIC PACKAGE
 CASE 620

PC SUFFIX
 PLASTIC PACKAGE
 CASE 648



D SUFFIX
 PLASTIC PACKAGE
 CASE 751B
 (SO-16)

PIN CONNECTIONS



ORDERING INFORMATION

Part No.	Ambient Temperature Range	Package Type
AM26LS30PC	-40° to $+85^{\circ}\text{C}$	Plastic DIP
AM26LS30DC		Ceramic DIP
MC26LS30D		SO-16

This document contains information on a new product. Specifications and information herein are subject to change without notice.

AM26LS30

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	$-0.5, +7.0$ $-7.0, +0.5$	Vdc
Input Voltage (All Inputs)	V_{in}	$-0.5, +20$	Vdc
Applied Output Voltage (When in High Impedance Mode) ($V_{CC} = 5.0$ V, Pin 4 = Logic 0, Pins 3, 6 = Logic 1)	V_{za}	± 15	Vdc
Output Voltage with $V_{CC}, V_{EE} = 0$ V	V_{zb}	± 15	Vdc
Output Current	I_O	Self limiting	—
Junction Temperature	T_J	$-65, +150$	°C

Devices should not be operated at these limits. The "Recommended Operating Conditions" provides conditions for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage (Differential Mode)	V_{CC} V_{EE}	$+4.75$ -0.5	5.0 0	$+5.25$ $+0.3$	Vdc
Power Supply Voltage (Single-Ended Mode)	V_{CC} V_{EE}	$+4.75$ -5.25	5.0 -5.0	5.25 -4.75	Vdc
Input Voltage (All Inputs)	V_{in}	0	—	$+15$	Vdc
Applied Output Voltage (when in High Impedance Mode)	V_{za}	-10	—	$+10$	Vdc
Applied Output Voltage, $V_{CC} = 0$	V_{zb}	-10	—	$+10$	Vdc
Output Current	I_O	-65	—	$+65$	mA
Operating Ambient Temperature (See text)	T_A	-40	—	$+85$	°C

All limits are not necessarily functional concurrently.

ELECTRICAL CHARACTERISTICS (EIA-422-A differential mode, Pin 4 ≤ 0.8 V, $-40^\circ\text{C} < T_A < +85^\circ\text{C}$,
 $+4.75\text{ V} \leq V_{CC} \leq +5.25\text{ V}$, $V_{EE} = \text{Gnd}$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage — Figure 1 Differential, $R_L = \infty$, $V_{CC} = 5.25$ V Differential, $R_L = 100\ \Omega$, $V_{CC} = 4.75$ V Change in Differential Voltage*, $R_L = 100\ \Omega$ Offset Voltage, $R_L = 100\ \Omega$ Change in Offset Voltage*, $R_L = 100\ \Omega$	V_{OD1} V_{OD2} ΔV_{OD2} V_{OS} ΔV_{OS}	— 2.0 — — —	4.2 2.6 10 2.5 10	6.0 — 400 3.0 400	Vdc Vdc mVdc Vdc mVdc
Output Current (each output) Power Off Leakage, $V_{CC} = 0$, $-10\text{ V} \leq V_O \leq +10\text{ V}$ High Impedance Mode, $V_{CC} = 5.25\text{ V}$, $-10\text{ V} \leq V_O \leq +10\text{ V}$ Short Circuit Current (Note 2) High Output Shorted to Pin 5 ($T_A = 25^\circ\text{C}$) High Output Shorted to Pin 5 ($-40^\circ\text{C} < T_A < +85^\circ\text{C}$) Low Output Shorted to $+6.0\text{ V}$ ($T_A = 25^\circ\text{C}$) Low Output Shorted to $+6.0\text{ V}$ ($-40^\circ\text{C} < T_A < +85^\circ\text{C}$)	I_{OLK} I_{OZ} I_{SC-} I_{SC-} I_{SC+} I_{SC+}	-100 -100 -150 -150 60 50	0 0 -95 — 75 —	$+100$ $+100$ -60 -50 150 150	μA μA mA mA mA mA
Inputs Low Level Voltage High Level Voltage Current i_{in} $V_{in} = 2.4$ V Current i_{in} $V_{in} = 15$ V Current i_{in} $V_{in} = 0.4$ V Current, $0 \leq V_{in} \leq 15\text{ V}$, $V_{CC} = 0$ Clamp Voltage ($I_{in} = -12\text{ mA}$)	V_{IL} V_{IH} I_{IH} I_{HH} I_{IL} I_{IX} V_{IK}	— 2.0 — — -200 — -1.5	— — 0 0 -8.0 0 —	0.8 — 40 100 — — —	Vdc Vdc μA μA μA μA Vdc
Power Supply Current ($V_{CC} = +5.25\text{ V}$, Outputs Open) ($0 \leq \text{Enable} \leq V_{CC}$)	I_{CC}	—	16	30	mA

* V_{in} switched from 0.8 to 2.0 volts.

NOTES: 1. Offset voltages, and input voltages, measured with respect to Pin 5.
 2. Only one output shorted at a time, for not more than 1 second.
 3. Typical values established at $+25^\circ\text{C}$ and $+5.0$ volt supply.

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TIMING CHARACTERISTICS (EIA-422-A differential mode, Pin 4 \approx 0.8 V, $T_A = +25^\circ\text{C}$, $V_{CC} = 5.0$ V, $V_{EE} = \text{Gnd}$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Differential Output Rise Time, Figure 2	t_r	—	70	200	ns
Differential Output Fall Time, Figure 2	t_f	—	70	200	ns
Propagation Delay Time — Input to Differential Output					ns
Input Low to High, Figure 2	t_{PDH}	—	90	200	
Input High to Low, Figure 2	t_{PDL}	—	90	200	
Skew Timing, Figure 2					ns
$ t_{PDH} - t_{PDL} $ for Each Driver	t_{SK1}	—	9.0	—	
Max-Min t_{PDH} Within a Package	t_{SK2}	—	2.0	—	
Max-Min t_{PDL} Within a Package	t_{SK3}	—	2.0	—	
Enable Timing, Figure 3					ns
Enable to Active High Differential Output	t_{PZH}	—	150	300	
Enable to Active Low Differential Output	t_{PZL}	—	190	350	
Enable to 3-State Output From Active High	t_{PHZ}	—	80	350	
Enable to 3-State Output From Active Low	t_{PLZ}	—	110	300	

ELECTRICAL CHARACTERISTICS (EIA-423-A single-ended mode, Pin 4 \geq 2.0 V, $-40^\circ\text{C} < T_A < +85^\circ\text{C}$, $4.75\text{ V} \leq |V_{CC}|, |V_{EE}| \leq 5.25\text{ V}$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($V_{CC} = V_{EE} = 4.75\text{ V}$)					Vdc
Single-Ended Voltage, $R_L = \infty$, Figure 4	$ V_{O1} $	4.0	4.2	6.0	
Single-Ended Voltage, $R_L = 450\ \Omega$, Figure 4	$ V_{O2} $	3.6	3.95	6.0	
Voltage Imbalance*, $R_L = 450\ \Omega$	$ \Delta V_{O2} $	—	0.05	0.4	
Slew Control Current (Pins 16, 13, 12, 9)	I_{SLEW}	—	± 120	—	μA
Output Current (Each Output)					μA
Power Off Leakage, $V_{CC} = V_{EE} = 0$, $-6.0\text{ V} \leq V_O \leq +6.0\text{ V}$	I_{OLK}	-100	0	+100	
Short Circuit Current (Output Short to Ground, Note 2)					
$V_{in} \leq 0.8\text{ V}$ ($T_A = 25^\circ\text{C}$)	I_{SC+}	60	80	150	mA
$V_{in} \leq 0.8\text{ V}$ ($-40^\circ\text{C} < T_A < +85^\circ\text{C}$)	I_{SC+}	50	—	150	mA
$V_{in} \geq 2.0\text{ V}$ ($T_A = 25^\circ\text{C}$)	I_{SC-}	-150	-95	-60	mA
$V_{in} \geq 2.0\text{ V}$ ($-40^\circ\text{C} < T_A < +85^\circ\text{C}$)	I_{SC-}	-150	—	-50	mA
Inputs					
Low Level Voltage	V_{iL}	—	—	0.8	Vdc
High Level Voltage	V_{iH}	2.0	—	—	Vdc
Current @ $V_{in} = 2.4\text{ V}$	I_{iH}	—	0	40	μA
Current @ $V_{in} = 15\text{ V}$	I_{iHH}	—	0	100	μA
Current @ $V_{in} = 0.4\text{ V}$	I_{iL}	-200	-8.0	—	μA
Current, $0 \leq V_{in} \leq 15\text{ V}$, $V_{CC} = 0$	I_{iX}	—	0	—	μA
Clamp Voltage ($I_{in} = -12\text{ mA}$)	V_{iK}	-1.5	—	—	Vdc
Power Supply Current (Outputs Open)					mA
$V_{CC} = 5.25\text{ V}$, $V_{EE} = -5.25\text{ V}$, $V_{in} = 0.4\text{ V}$	I_{CC}	—	17	30	
	I_{EE}	-22	-2.0	—	

*Imbalance is the difference between $|V_{O2}|$ with $V_{in} < 0.8\text{ V}$ and $|V_{O2}|$ with $V_{in} = 2.0\text{ V}$.

NOTES: 1. All voltages measured with respect to Pin 5.

2. Only one output shorted at a time, for not more than 1 second.

3. Typical values established at $+25^\circ\text{C}$, $V_{CC} = +5.0\text{ V}$, $V_{EE} = -5.0\text{ V}$

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TIMING CHARACTERISTICS (EIA-423-A single-ended mode, Pin 4 \geq 2.0 V, $T_A = 25^\circ\text{C}$, $V_{CC} = +5.0\text{ V}$, $V_{EE} = -5.0\text{ V}$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Timing					
Output Rise Time, Figure 5, $C_C = 0$	t_r	—	65	300	ns
Output Fall Time, Figure 5, $C_C = 0$	t_f	—	65	300	ns
Output Rise Time, Figure 5, $C_C = 50\text{ pF}$	t_r	—	3.0	—	μs
Output Fall Time, Figure 5, $C_C = 50\text{ pF}$	t_f	—	3.0	—	μs
Rise Time Coefficient (Figure 15)	CRT	—	0.06	—	$\mu\text{s/pF}$
Propagation Delay Time — Input to Single Ended Output					ns
Input Low to High, Figure 5, $C_C = 0$	t_{PDH}	—	100	300	
Input High to Low, Figure 5, $C_C = 0$	t_{PDL}	—	100	300	
Skew Timing, $C_C = 0$, Figure 5					ns
$ t_{PDH} - t_{PDL} $ for Each Driver	t_{SK4}	—	15	—	
Max-Min t_{PDH} Within a Package	t_{SK5}	—	2.0	—	
Max-Min t_{PDL} Within a Package	t_{SK6}	—	5.0	—	

TABLE 1

Operation	V _{CC}	V _{EE}	Inputs				Outputs				
			Mode	A	B	C	D	A	B	C	D
Differential (EIA-422-A)	+ 5.0	Gnd	0	0	0	0	0	0	1	1	0
			0	1	0	0	1	1	0	0	1
			0	X	1	0	1	Z	Z	0	1
			0	1	0	0	0	1	0	1	0
			0	0	0	0	1	0	1	0	1
			0	1	0	1	X	1	0	Z	Z
Single-Ended (EIA-423-A)	+ 5.0	− 5.0	1	0	0	0	0	0	0	0	0
			1	1	0	0	0	1	0	0	0
			1	0	1	0	0	0	1	0	0
			1	0	0	1	0	0	0	1	0
			1	0	0	0	1	0	0	0	1
X	0	X	X	X	X	X	Z	Z	Z	Z	

X = Don't Care
Z = High Impedance (Off)

FIGURE 1 — DIFFERENTIAL OUTPUT TEST

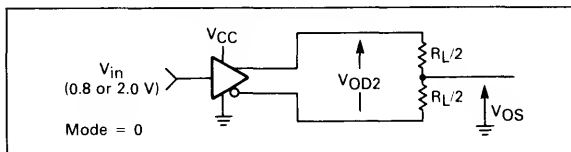
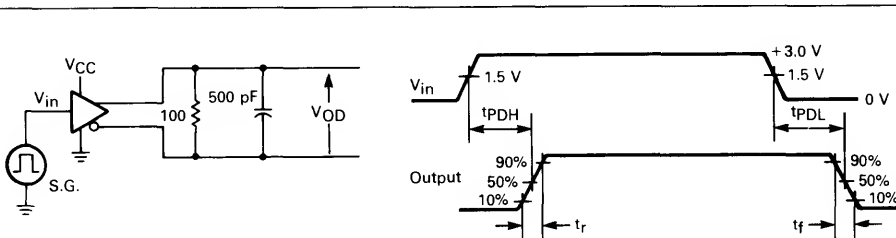


FIGURE 2 — DIFFERENTIAL MODE RISE/FALL TIME AND DATA PROPAGATION DELAY



NOTES:

1. S.G. set to: $f \leq 1.0\text{ MHz}$; duty cycle = 50%; $t_r, t_f \leq 10\text{ ns}$.
2. $t_{SK1} = |t_{PDH} - t_{PDL}|$ for each driver.
3. t_{SK2} computed by subtracting the shortest t_{PDH} from the longest t_{PDH} of the 2 drivers within a package.
4. t_{SK3} computed by subtracting the shortest t_{PDL} from the longest t_{PDL} of the 2 drivers within a package.

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FIGURE 3 — DIFFERENTIAL MODE ENABLE TIMING

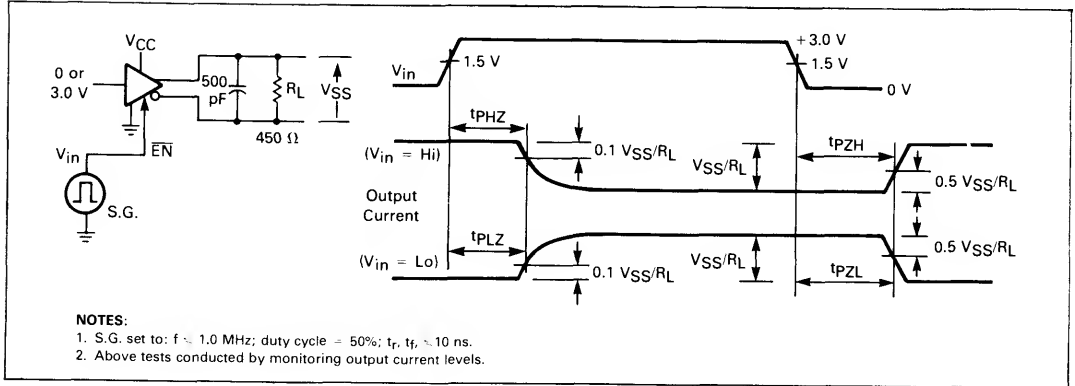


FIGURE 4 — SINGLE-ENDED OUTPUT TEST

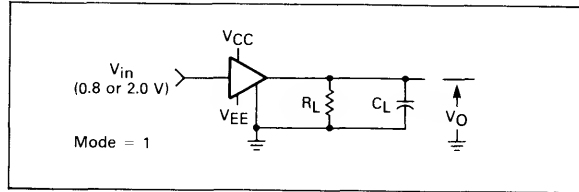
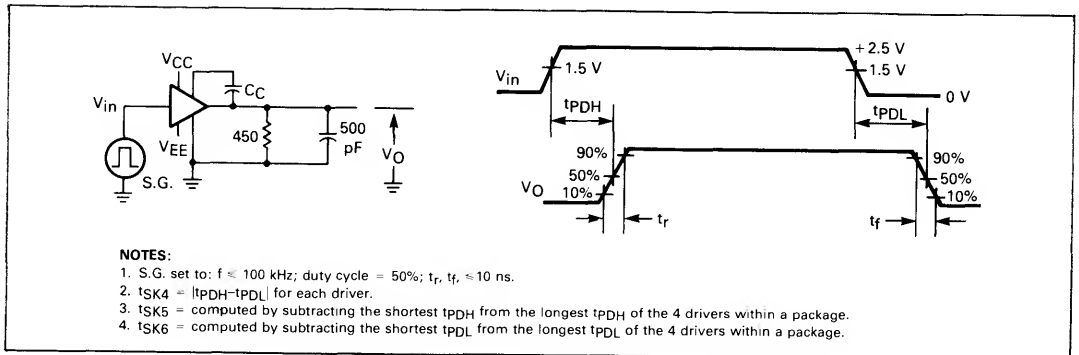


FIGURE 5 — SINGLE-ENDED MODE RISE/FALL TIME AND DATA PROPAGATION DELAY



AM26LS30

FIGURE 6 — DIFFERENTIAL OUTPUT VOLTAGE versus LOAD CURRENT

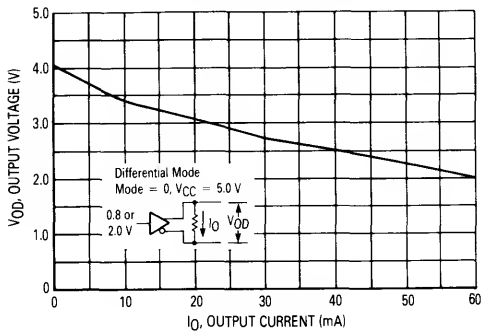


FIGURE 7 — INTERNAL BIAS CURRENT versus LOAD CURRENT

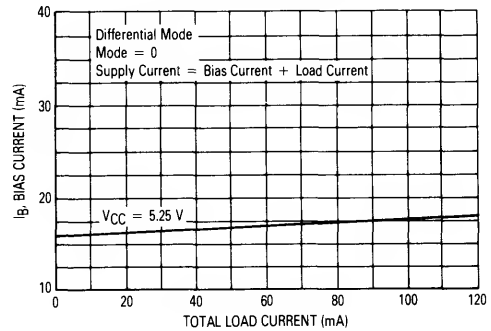


FIGURE 8 — SHORT CIRCUIT CURRENT versus OUTPUT VOLTAGE

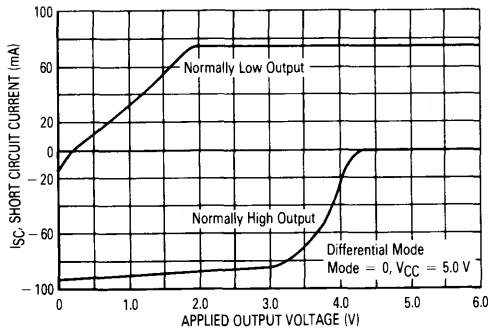


FIGURE 9 — INPUT CURRENT versus INPUT VOLTAGE

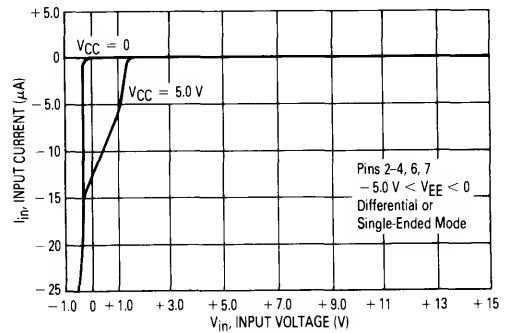


FIGURE 10 — OUTPUT VOLTAGE versus OUTPUT SOURCE CURRENT

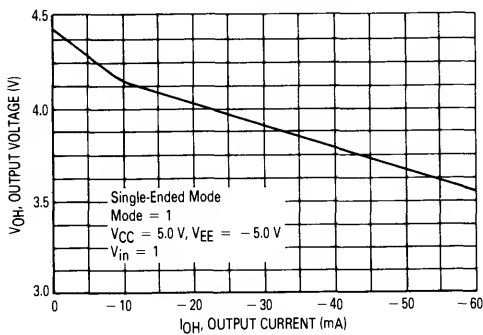
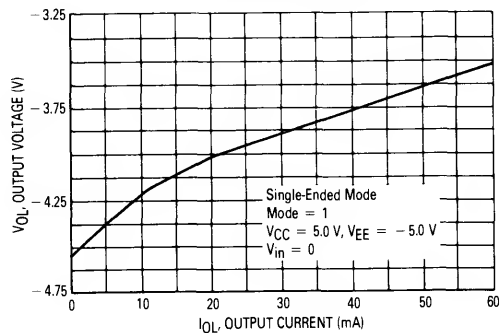


FIGURE 11 — OUTPUT VOLTAGE versus OUTPUT SINK CURRENT



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FIGURE 12 — INTERNAL POSITIVE BIAS CURRENT
versus LOAD CURRENT

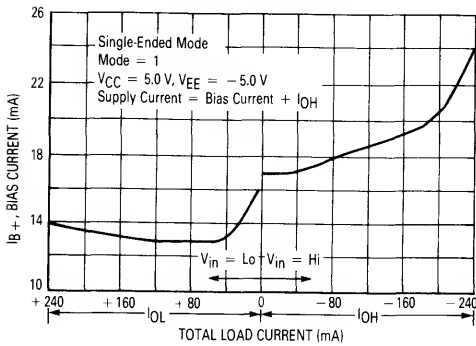


FIGURE 13 — INTERNAL NEGATIVE BIAS CURRENT
versus LOAD CURRENT

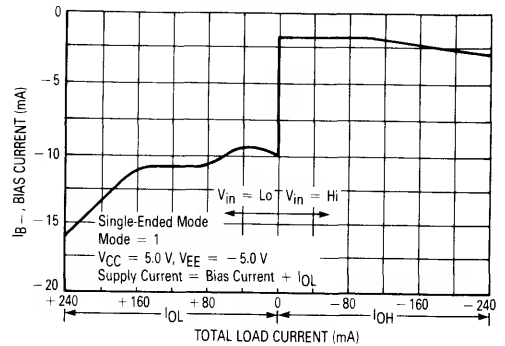


FIGURE 14 — SHORT CIRCUIT CURRENT
versus OUTPUT VOLTAGE

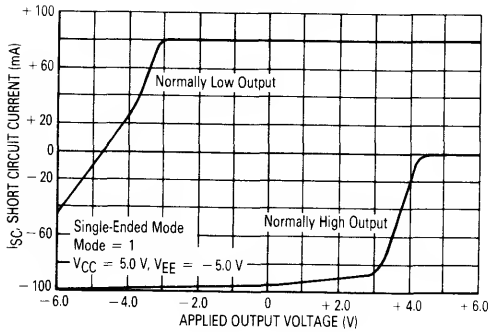


FIGURE 15 — SHORT CIRCUIT CURRENT
versus TEMPERATURE

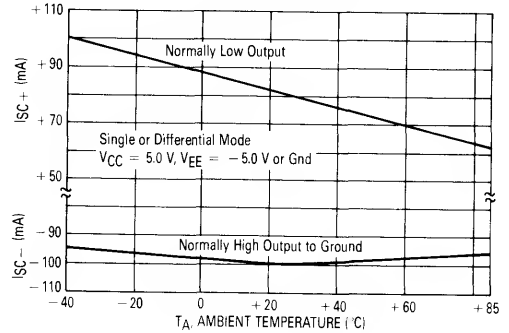
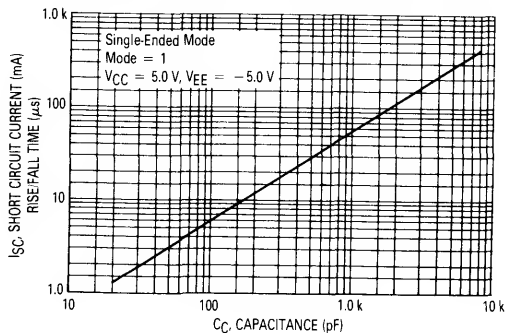


FIGURE 16 — RISE/FALL TIME versus CAPACITANCE



APPLICATIONS INFORMATION

Description

The AM26LS30 is a dual function line driver — it can be configured as two differential output drivers which comply with EIA-422-A standard, or as four single-ended drivers which comply with EIA-423-A standard. The mode of operation is selected with the Mode pin (Pin 4) and appropriate power supplies (see Table 1). Each of the four outputs is capable of sourcing and sinking 60 to 70 mA while providing sufficient voltage to ensure proper data transmission.

As differential drivers, data rates to 10 Mbaud can be transmitted over a twisted pair for a distance determined by the cable characteristics. EIA-422-A standard provides guidelines for cable length versus data rate. The advantage of a differential (balanced) system over a single-ended system is greater noise immunity, common mode rejection, and higher data rates.

Where extraneous noise sources are not a problem, the AM26LS30 may be configured as single-ended drivers transmitting data rates to 100 kbaud. Crosstalk among wires within a cable is controlled by the use of the slew rate control pins on the AM26LS30.

Mode Selection (Differential Mode)

In this mode (Pins 4 and 8 at ground), only a +5.0 V supply $\pm 5\%$ is required at V_{CC} . Pins 2 and 7 are the driver inputs, while Pins 10, 11, 14 and 15 are the outputs (see the Block Diagram). The two outputs of a driver are always complementary and the differential voltage available at each pair of outputs is shown in Figure 6 for $V_{CC} = 5.0$ volts. The differential output voltage will vary directly with V_{CC} . A "High" output can only source current, while a "Low" output can only sink current (except for short circuit current — see Figure 8).

The two outputs will be in a high impedance mode when the respective Enable input (Pin 3 or 6) is high, or if $V_{CC} \leq 1.1$ volts. Output leakage current over a common mode range of ± 10 V is typically less than $1.0 \mu A$.

The outputs have short circuit current limiting typically less than 100 mA over a voltage range of 0 to +6.0 V (see Figure 8). Short circuits should not be allowed to last indefinitely as the IC may be damaged.

Pins 9, 12, 13, and 16 are normally not used when in this mode, and should be left open.

(Single-Ended Mode)

In this mode (Pin 4 ≥ 2.0 V) V_{CC} requires +5.0 V, and V_{EE} requires -5.0 V, both $\pm 5\%$. Pins 2, 3, 6, and 7 are inputs for the four drivers, and Pins 15, 14, 11, and 10 (respectively) are the outputs. The four drivers are independent of each other, and each output will be at a positive or a negative voltage depending on its input state, the load current, and the supply voltage. Figures 10 and 11 indicate the high and low output voltages for $V_{CC} = 5.0$ V, and $V_{EE} = -5.0$ V. The graph of Figure 10 will vary directly with V_{CC} , and the graph of Figure 11 will vary directly with V_{EE} . A "High" output can only

source current, while a "Low" output can only sink current (except short circuit current — see Figure 14).

The outputs will be in a high impedance mode only if $V_{CC} \leq 1.1$ V. Changing V_{EE} to 0 volts does not set the outputs to a high impedance mode. Leakage current over a common mode range of ± 10 volts is typically less than $1.0 \mu A$.

The outputs have short circuit current limiting typically less than 100 mA over a voltage range of ± 6.0 V (see Figure 14). Short circuits should not be allowed to last indefinitely as the IC may be damaged.

Capacitors connected between Pins 9, 12, 13, and 16 and their respective outputs will provide slew rate limiting of the output transition. Figure 16 indicates the required capacitor value to obtain a desired rise or fall time (measured between the 10% and 90% points). The positive and negative transition times will be within $\approx \pm 5\%$ of each other. Each output may be set to a different slew rate if desired.

Inputs

The five inputs determine the state of the outputs in accordance with Table 1. All inputs (regardless of the operating mode) have a nominal threshold of +1.3 V, and their voltage must be kept within the range of 0 V to +15 V for proper operation. If an input is taken more than 0.3 V below ground, excessive currents will flow, and the proper operation of the drivers will be affected. An open pin is equivalent to a logic high, but good design practices dictate that inputs should never be left open. Unused inputs should be connected to ground. The characteristics of the inputs are shown in Figure 9.

Power Supplies

V_{CC} requires +5.0 V, $\pm 5\%$, regardless of the mode of operation. The supply current is determined by the IC's internal bias requirements, and the total load current. The internally required current is a function of the load current and is shown in Figure 7 for the differential mode.

In the single-ended mode, V_{EE} must be -5.0 V, $\pm 5\%$ in order to comply with EIA-423-A standards. Figures 12 and 13 indicate the internally required bias currents as a function of total load current (the sum of the four output loads). The discontinuity at 0 load current exists due to a change in bias current when the inputs are switched. The supply currents vary $\approx \pm 2.0$ mA as V_{CC} and V_{EE} are varied from [4.75 V] to [5.25 V].

Sequencing of the supplies during power-up/power-down is not required.

Bypass capacitors (0.1 μF minimum on each supply pin) are recommended to ensure proper operation. Capacitors reduce noise induced onto the supply lines by the switching action of the drivers, particularly where long P.C. board tracks are involved. Additionally, the capacitors help absorb transients induced onto the drivers' outputs from the external cable (from ESD, motor noise, nearby computers, etc.).

Operating Temperature Range

The maximum ambient operating temperature, listed as +85°C, is actually a function of the system use, i.e., specifically how many drivers within a package are used, and at what current levels they are operating. The maximum power which may be dissipated within the package is determined by:

$$P_{DMax} = \frac{T_{Jmax} - T_A}{R_{\theta JA}}$$

where: $R_{\theta JA}$ = the package thermal resistance which is typically:

- 67°C/W for the DIP (PC) package
- 100°C/W for the ceramic (DC) package
- 120°C/W for the SOIC (D) package

T_{Jmax} = the maximum allowable junction temperature (150°C)

T_A = the ambient air temperature near the IC package

1. Differential Mode Power Dissipation

For the differential mode, the power dissipated within the package is calculated from:

$$P_D = [(V_{CC} - V_{OD}) \times I_O] \text{ each driver} + (V_{CC} \times I_B)$$

where: V_{CC} = the supply voltage

V_{OD} = is taken from Figure 6 for the known value of I_O

I_B = the internal bias current (Figure 7)

As indicated in the equation, the first term (in brackets) must be calculated and summed for each of the two drivers, while the last term is common to the entire package. Note that the term $(V_{CC} - V_{OD})$ is constant for a given value of I_O and does not vary with V_{CC} . For an application involving the following conditions:

$T_A = +85^\circ\text{C}$, $I_O = 60 \text{ mA}$ (each driver), $V_{CC} = 5.25 \text{ V}$, the suitability of the various package types is calculated as follows:

The power dissipated is:

$$P_D = [3.0 \text{ V} \times 60 \text{ mA} \times 2] + (5.25 \text{ V} \times 18 \text{ mA})$$

$$P_D = 454 \text{ mW}$$

The junction temperature calculates to:

$$T_J = 85^\circ\text{C} + (0.454 \text{ W} \times 67^\circ\text{C/W}) = 115^\circ\text{C} \text{ for the DIP package,}$$

$$T_J = 85^\circ\text{C} + (0.454 \text{ W} \times 100^\circ\text{C/W}) = 130^\circ\text{C} \text{ for the ceramic package,}$$

$$T_J = 85^\circ\text{C} + (0.454 \text{ W} \times 120^\circ\text{C/W}) = 139^\circ\text{C} \text{ for the SOIC package.}$$

Since the maximum allowable junction temperature is not exceeded in any of the above cases, any of the packages can be used in this application.

2. Single-Ended Mode Power Dissipation

For the single-ended mode, the power dissipated within the package is calculated from:

$$P_D = (I_B + \times V_{CC}) + (I_B - \times V_{EE}) + [(I_O \times (V_{CC} - V_{OH})) \text{ each driver}]$$

The above equation assumes I_O has the same magnitude for both output states, and makes use of the fact that the absolute value of the graphs of Figures 10 and 11 are nearly identical. I_{B+} and I_{B-} are obtained from the right half of Figures 12 and 13, and $(V_{CC} - V_{OH})$ can be obtained from Figure 10. Note that the term $(V_{CC} - V_{OH})$ is constant for a given value of I_O and does not vary with V_{CC} . For an application involving the following conditions:

$T_A = +85^\circ\text{C}$, $I_O = -60 \text{ mA}$ (each driver), $V_{CC} = 5.25 \text{ V}$, $V_{EE} = -5.25 \text{ V}$, the suitability of the various package types is calculated as follows:

The power dissipated is:

$$P_D = (24 \text{ mA} \times 5.25 \text{ V}) + (-3 \text{ mA} \times -5.25 \text{ V}) + (60 \text{ mA} \times 1.45 \text{ V} \times 4)$$

$$P_D = 490 \text{ mW}$$

The junction temperature calculates to:

$$T_J = 85^\circ\text{C} + (0.490 \text{ W} \times 67^\circ\text{C/W}) = 118^\circ\text{C} \text{ for the DIP package}$$

$$T_J = 85^\circ\text{C} + (0.490 \text{ W} \times 100^\circ\text{C/W}) = 134^\circ\text{C} \text{ for the Ceramic package}$$

$$T_J = 85^\circ\text{C} + (0.490 \text{ W} \times 120^\circ\text{C/W}) = 144^\circ\text{C} \text{ for the SOIC package}$$

Since the maximum allowable junction temperature is not exceeded in any of the above cases, any of the packages can be used in this application.

SYSTEM EXAMPLES

Differential System

An example of a typical EIA-422-A system is shown in Figure 17. Although EIA-422-A does not specifically address multiple driver situations, the AM26LS30 can be used in this manner since the outputs can be put into a high impedance mode. It is, however, the system designer's responsibility to ensure the Enable pins are properly controlled so as to prevent two drivers on the same cable from being "on" at the same time.

The limit on the number of receivers and drivers which may be connected on one system is determined by the input current of each receiver, the maximum leakage current of each "off" driver, and the DC current through each terminating resistor. The sum of these currents must not exceed the capability of the "on" driver (≈ 60 mA). If the cable is of any significant length, with receivers at various points along its length, the common mode voltage may vary along its length, and this parameter must be considered when calculating the maximum driver current.

The cable requirements are defined not only by its AC characteristics and the data rate, but also by its DC resistance. The maximum resistance must be such that the minimum voltage across any receiver inputs is never less than 200 mV.

The ground terminals of each driver and receiver in Figure 17 must be connected together by a dedicated wire (or the shield) in the cable so as to provide a common reference. Chassis grounds or power line grounds should not be relied on for this common connection as they may generate significant common mode differences. Additionally, they usually do not provide a sufficiently low impedance at the frequencies of interest.

Single-Ended System

An example of a typical EIA-423-A system is shown in Figure 18. Multiple drivers on a single data line is not possible since the drivers cannot be put into a high impedance mode. Although each driver is shown connected to a single receiver, multiple receivers can be driven from a single driver as long as the total load current of the receivers and the terminating resistor does not exceed the capability of the driver (≈ 60 mA). If the cable is of any significant length, with receivers at various points along its length, the common mode voltage may vary along its length, and this parameter must be considered when calculating the maximum driver current.

The cable requirements are defined not only by its AC characteristics and the data rate, but also by its DC resistance. The maximum resistance must be such that the minimum voltage across any receiver inputs is never less than 200 mV.

The ground terminals of each driver and receiver in Figure 18 must be connected together by a dedicated wire (or the shield) in the cable so as to provide a common reference. Chassis grounds or power line grounds should not be relied on for this common connection as they may generate significant common mode differences. Additionally, they usually do not provide a sufficiently low impedance for the frequencies of interest.

Additional Modes of Operation

If compliance with EIA-422-A or EIA-423-A standard is not required in a particular application, the AM26LS30 can be operated in two other modes.

A) The device may be operated in the differential mode (Pin 4 = 0) with V_{EE} connected to any voltage between ground and -5.25 V. Outputs in the low state will be referenced to V_{EE} , resulting in a differential output voltage greater than that shown in Figure 6. The Enable pins will operate the same as previously described.

B) The device may be operated in the single-ended mode (Pin 4 = 1) with V_{EE} connected to any voltage between ground and -5.25 V. Outputs in the high state will be at a voltage as shown in Figure 10, while outputs in a low state will be referenced to V_{EE} .

Termination Resistors

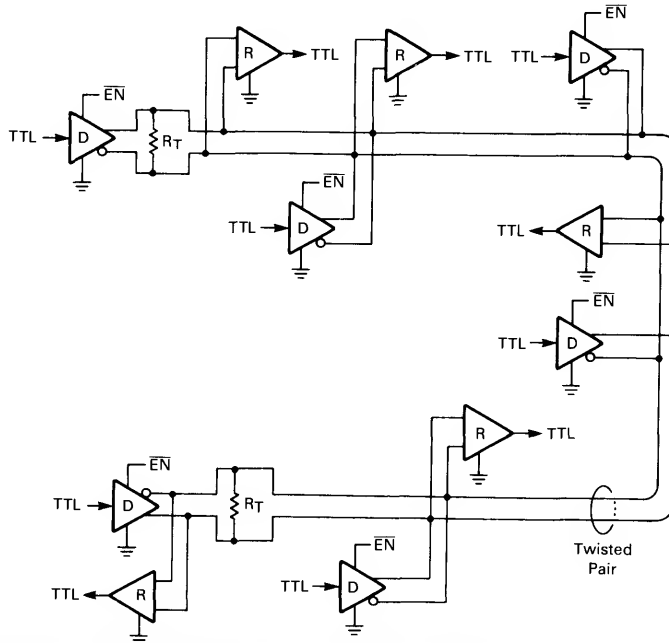
Transmission line theory states that, in order to preserve the shape and integrity of a waveform traveling along a cable, the cable must be terminated in an impedance equal to its characteristic impedance. In a system such as that depicted in Figure 17, in which data can travel in both directions, both physical ends of the cable must be terminated. Stubs leading to each receiver and driver should be as short as possible.

In a system such as that depicted in Figure 18, in which data normally travels in one direction only, a terminator is theoretically required only at the receiving end of the cable. However, if the cable is in a location where noise spikes of several volts can be induced onto it, then a terminator (preferably a series resistor) should be placed at the driver end to prevent damage to the driver.

Leaving off the terminations will generally result in reflections which can have amplitudes of several volts above V_{CC} or several volts below ground or V_{EE} . These overshoots/undershoots can disrupt the driver and/or receiver, create false data, and in some cases, damage components on the bus.

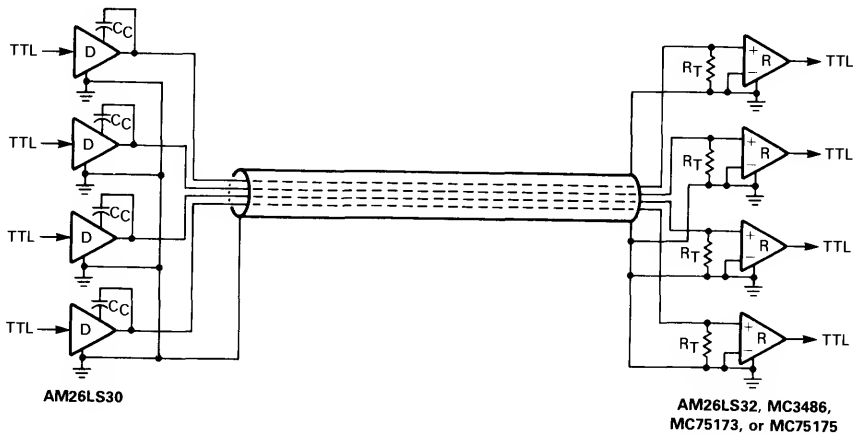
AM26LS30

FIGURE 17 — EIA-422-A EXAMPLE



Terminating resistors R_T should be located at the physical ends of the cable.
 Stubs should be as short as possible.
 Receivers = AM26LS32, MC3486, MC75173 or MC75175.
 Circuit grounds must be connected together through a dedicated wire.

FIGURE 18 — EIA-423-A EXAMPLE



QUAD LINE DRIVER WITH NAND ENABLED THREE-STATE OUTPUTS

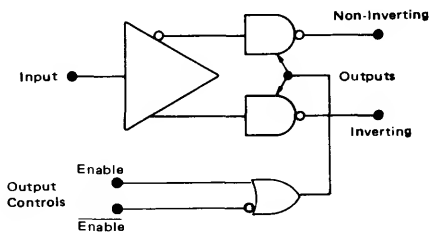
The Motorola AM26LS31 is a quad differential line driver intended for digital data transmission over balanced lines. It meets all the requirements of EIA-422 Standard and Federal Standard 1020.

The AM26LS31 provides an enable/disable function common to all four drivers as opposed to the split enables on the MC3487 EIA-422 driver.

The high impedance output state is assured during power down.

- Full EIA-422 Standard Compliance
- Single +5.0 V Supply
- Meets Full $V_O = 6.0\text{ V}$, $V_{CC} = 0\text{ V}$, $I_O < 100\text{ }\mu\text{A}$ Requirement
- Output Short Circuit Protection
- Complementary Outputs for Balanced Line Operation
- High Output Drive Capability
- Advanced LS Processing
- PNP Inputs for MOS Compatibility

DRIVER BLOCK DIAGRAM



TRUTH TABLE

Input	Control Inputs (E/ \bar{E})	Non-Inverting Output	Inverting Output
H	H/L	H	L
L	H/L	L	H
X	L/H	Z	Z

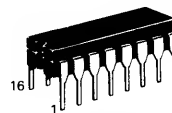
L = Low Logic State
H = High Logic State
X = Irrelevant
Z = Third-State (High Impedance)

*Note that the surface mount MC26LS31D devices use the same die as in the ceramic and plastic DIP AM26LS31DC devices, but with an MC prefix to prevent confusion with the package suffixes.

AM26LS31

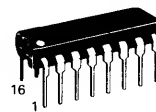
QUAD EIA-422 LINE DRIVER WITH THREE-STATE OUTPUTS

SILICON MONOLITHIC INTEGRATED CIRCUIT



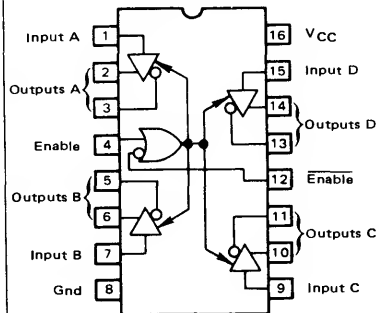
DC SUFFIX
CERAMIC PACKAGE
CASE 620

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO-16)



PC SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
AM26LS31DC	0 to 70°C	Ceramic DIP
AM26LS31PC		Plastic DIP
MC26LS31D*		SO-16

AM26LS31

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.0	Vdc
Input Voltage	V_I	5.5	Vdc
Operating Ambient Temperature Range	T_A	0 to +70	°C
Operating Junction Temperature Range	T_J		°C
Ceramic Package		175	
Plastic Package		150	
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted specifications apply $4.75 \text{ V} \leq V_{CC} \leq 5.25 \text{ V}$ and $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$. Typical values measured at $V_{CC} = 5.0 \text{ V}$, and $T_A = 25^\circ\text{C}$.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage — Low Logic State	V_{IL}	—	—	0.8	Vdc
Input Voltage — High Logic State	V_{IH}	2.0	—	—	Vdc
Input Current — Low Logic State ($V_{IL} = 0.4 \text{ V}$)	I_{IL}	—	—	-360	μA
Input Current — High Logic State ($V_{IH} = 2.7 \text{ V}$) ($V_{IH} = 7.0 \text{ V}$)	I_{IH}	—	—	+20 +100	μA
Input Clamp Voltage ($I_{IK} = -18 \text{ mA}$)	V_{IK}	—	—	-1.5	V
Output Voltage — Low Logic State ($I_{OL} = 20 \text{ mA}$)	V_{OL}	—	—	0.5	V
Output Voltage — High Logic State ($I_{OH} = -20 \text{ mA}$)	V_{OH}	2.5	—	—	V
Output Short Circuit Current ($V_{IH} = 2.0 \text{ V}$) Note 1	I_{OS}	-30	—	-150	mA
Output Leakage Current — Hi-Z State ($V_{OL} = 0.5 \text{ V}$, $V_{IL(E)} = 0.8 \text{ V}$, $V_{IH(E)} = 2.0 \text{ V}$) ($V_{OH} = 2.5 \text{ V}$, $V_{IL(E)} = 0.8 \text{ V}$, $V_{IH(E)} = 2.0 \text{ V}$)	$I_{O(Z)}$	—	—	-20 +20	μA
Output Leakage Current — Power OFF ($V_{OH} = 6.0 \text{ V}$, $V_{CC} = 0 \text{ V}$) ($V_{OL} = -0.25 \text{ V}$, $V_{CC} = 0 \text{ V}$)	$I_{O(off)}$	—	—	+100 -100	μA
Output Offset Voltage Difference, Note 2	$V_{OS} - \bar{V}_{OS}$	—	—	± 0.4	V
Output Differential Voltage, Note 2	V_{OD}	2.0	—	—	V
Output Differential Voltage Difference, Note 2	$ \Delta V_{OD} $	—	—	± 0.4	V
Power Supply Current (Output Disabled) Note 3	I_{CCX}	—	60	80	mA

1. Only one output may be shorted at a time.
2. See EIA Specification EIA-422 for exact test conditions.
3. Circuit in three-state condition.

SWITCHING CHARACTERISTICS ($V_{CC} = 5.0 \text{ V}$, $T_A = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Times					ns
High to Low Output	t_{PHL}	—	—	20	
Low to High Output	t_{PLH}	—	—	20	
Output Skew		—	—	6.0	ns
Propagation Delay — Control to Output ($C_L = 10 \text{ pF}$, $R_L = 75 \Omega$ to Gnd) ($C_L = 10 \text{ pF}$, $R_L = 180 \Omega$ to V_{CC}) ($C_L = 30 \text{ pF}$, $R_L = 75 \Omega$ to Gnd) ($C_L = 30 \text{ pF}$, $R_L = 180 \Omega$ to V_{CC})	$t_{PHZ(E)}$ $t_{PLZ(E)}$ $t_{PZH(E)}$ $t_{PZL(E)}$	— — — —	— — — —	30 35 40 45	ns

AM26LS31

FIGURE 1 — THREE-STATE ENABLE TEST CIRCUIT AND WAVEFORMS

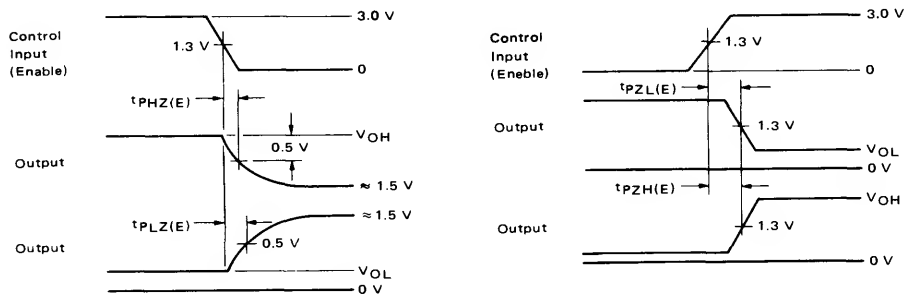
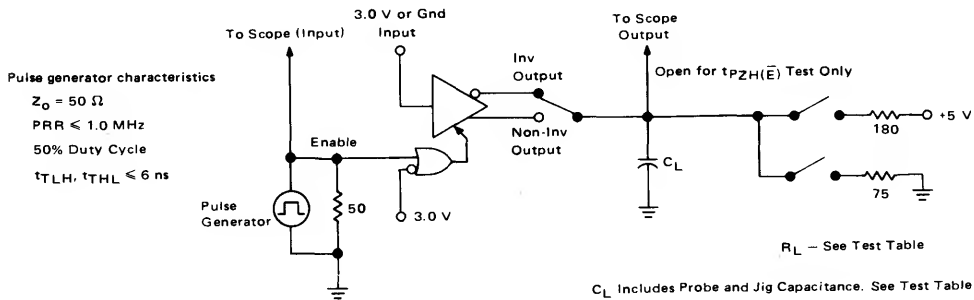
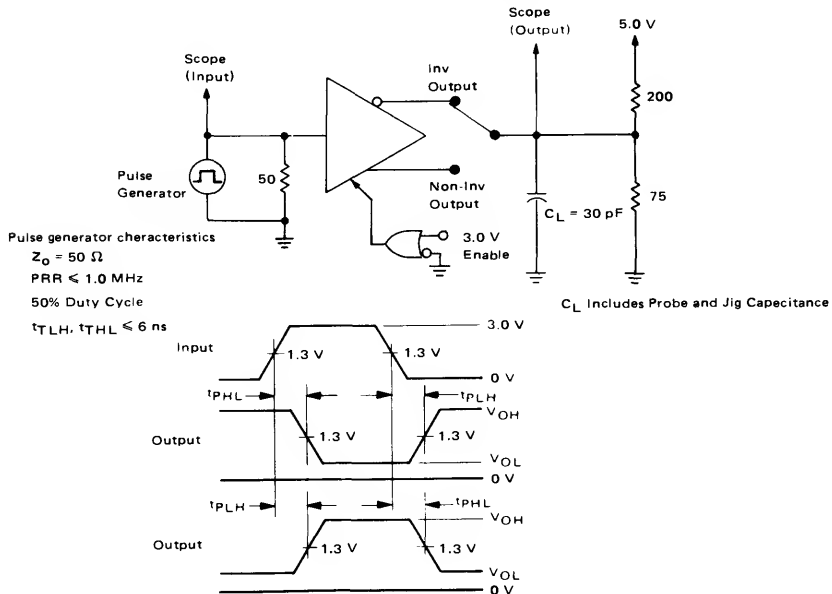


FIGURE 2 — PROPAGATION DELAY TIMES INPUT TO OUTPUT WAVEFORMS AND TEST CIRCUIT



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

AM26LS32

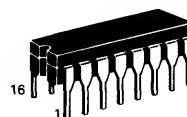
QUAD EIA-422/423 LINE RECEIVER

Motorola's Quad EIA-422/3 Receiver features four independent receiver chains which comply with EIA Standards for the Electrical Characteristics of Balanced/Unbalanced Voltage Digital Interface Circuits. Receiver outputs are 74LS compatible, three-state structures which are forced to a high impedance state when Pin 4 is a Logic "0" and Pin 12 is a Logic "1." A PNP device buffers each output control pin to assure minimum loading for either Logic "1" or Logic "0" inputs. In addition, each receiver chain has internal hysteresis circuitry to improve noise margin and discourage output instability for slowly changing input waveforms. A summary of AM26LS32 features include:

- Four Independent Receiver Chains
- Three-State Outputs
- High Impedance Output Control Inputs (PIA Compatible)
- Internal Hysteresis — 30 mV (Typ) @ Zero Volts Common Mode
- Fast Propagation Times — 25 ns (Typ)
- TTL Compatible
- Single 5 V Supply Voltage
- Fail-Safe Input-Output Relationship. Output Always High When Inputs Are Open, Terminated or Shorted
- 6 k Minimum Input Impedance

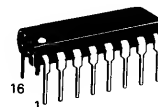
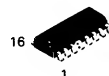
QUAD EIA-422/3 LINE RECEIVER WITH THREE-STATE OUTPUTS

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**



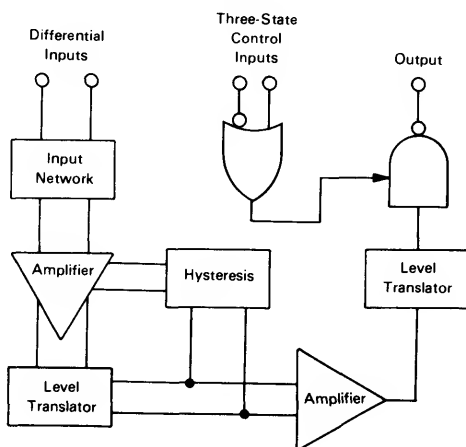
DC SUFFIX
CERAMIC PACKAGE
CASE 620

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO-16)

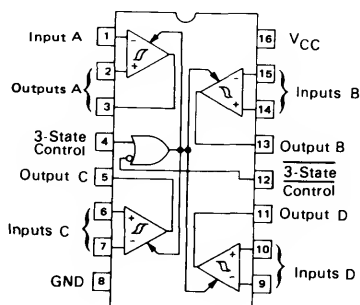


PC SUFFIX
PLASTIC PACKAGE
CASE 648

RECEIVER CHAIN BLOCK DIAGRAM



PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature	Package
AM26LS32DC	0 to 70°C	Ceramic DIP
AM26LS32PC		Plastic DIP
MC26LS32D*		SO-16

*Note that the surface mount MC26LS32D devices use the same die as in the ceramic and plastic DIP AM26LS32DC devices, but with an MC prefix to prevent confusion with the package suffixes.

AM26LS32

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Input Common Mode Voltage	V_{ICM}	± 25	Vdc
Input Differential Voltage	V_{ID}	± 25	Vdc
Three-State Control Input Voltage	V_I	7.0	Vdc
Output Sink Current	I_O	50	mA
Storage Temperature	T_{stg}	-65 to +150	°C
Operating Junction Temperature	T_J		°C
Ceramic Package		+175	
Plastic Package		+150	

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	4.75 to 5.25	Vdc
Operating Ambient Temperature	T_A	0 to +70	°C
Input Common Mode Voltage Range	V_{ICR}	-7.0 to +7.0	Vdc
Input Differential Voltage Range	V_{IDR}	6.0	Vdc

ELECTRICAL CHARACTERISTICS (Unless otherwise noted minimum and maximum limits apply over recommended temperature and power supply voltage ranges. Typical values are for $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$ and $V_{IC} = 0\text{ V}$. See Note 1.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage — High Logic State (Three-State Control)	V_{IH}	2.0	—	—	V
Input Voltage — Low Logic State (Three-State Control)	V_{IL}	—	—	0.8	V
Differential Input Threshold Voltage (Note 2) (-7.0 V $\leq V_{IC} \leq 7.0\text{ V}$, $V_{IH} = 2.0\text{ V}$) ($I_O = -0.4\text{ mA}$, $V_{OH} \geq 2.7\text{ V}$) ($I_O = 8.0\text{ mA}$, $V_{OL} \leq 0.45\text{ V}$)	$V_{TH(D)}$	—	—	0.2 -0.2	V
Input Bias Current ($V_{CC} = 0\text{ V}$ or 5.25 V) (Other Inputs at $-15\text{ V} \leq V_{in} \leq +15\text{ V}$) $V_{in} = +15\text{ V}$ $V_{in} = -15\text{ V}$	$I_{IB(D)}$	—	—	2.3 -2.8	mA
Input Resistance ($-15\text{ V} \leq V_{in} \leq +15\text{ V}$)	R_{in}	6.0 K	—	—	Ohms
Input Balance and Output Level (-7.0 V $\leq V_{IC} \leq 7.0\text{ V}$, $V_{IH} = 2.0\text{ V}$, See Note 3) ($I_O = -0.4\text{ mA}$, $V_{ID} = 0.4\text{ V}$) ($I_O = 8.0\text{ mA}$, $V_{ID} = -0.4\text{ V}$)	V_{OH} V_{OL}	2.7 —	— —	— 0.45	V
Output Third State Leakage Current ($V_{I(D)} = +3.0\text{ V}$, $V_{IL} = 0.8\text{ V}$, $V_O = 0.4\text{ V}$) ($V_{I(D)} = -3.0\text{ V}$, $V_{IL} = 0.8\text{ V}$, $V_O = 2.4\text{ V}$)	I_{OZ}	—	—	-20 20	μA
Output Short Circuit Current ($V_{I(D)} = 3.0\text{ V}$, $V_{IH} = 2.0\text{ V}$, $V_O = 0\text{ V}$, See Note 4)	I_{OS}	-15	—	-85	mA
Input Current — Low Logic State (Three-State Control) ($V_{IL} = 0.4\text{ V}$)	I_{IL}	—	—	-360	μA
Input Current — High Logic State (Three-State Control) ($V_{IH} = 2.7\text{ V}$) ($V_{IH} = 5.5\text{ V}$)	I_{IH}	—	—	20 100	μA
Input Clamp Diode Voltage (Three-State Control) ($I_{IC} = -18\text{ mA}$)	V_{IK}	—	—	-1.5	V
Power Supply Current ($V_{IL} = 0\text{ V}$) (All Inputs Grounded)	I_{CC}	—	—	70	mA

NOTES:

1. All currents into device pins are shown as positive, out of device pins are negative. All voltages referenced to ground unless otherwise noted.
2. Differential input threshold voltage and guaranteed output levels are done simultaneously for worst case.
3. Refer to EIA-422/3 for exact conditions. Input balance and guaranteed output levels are done simultaneously for worst case.
4. Only one output at a time should be shorted.

AM26LS32

SWITCHING CHARACTERISTICS (Unless otherwise noted, $V_{CC} = 5.0 \text{ V}$ and $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time — Differential Inputs to Output (Output High to Low) (Output Low to High)	$t_{PHL(D)}$ $t_{PLH(D)}$	— —	— —	30 30	ns
Propagation Delay Time — Three-State Control to Output (Output Low to Third State) (Output High to Third State) (Output Third State to High) (Output Third State to Low)	t_{PLZ} t_{PHZ} t_{PZH} t_{PZL}	— — — —	— — — —	35 35 30 30	ns

FIGURE 1 - PROPAGATION DELAY DIFFERENTIAL INPUT TO OUTPUT

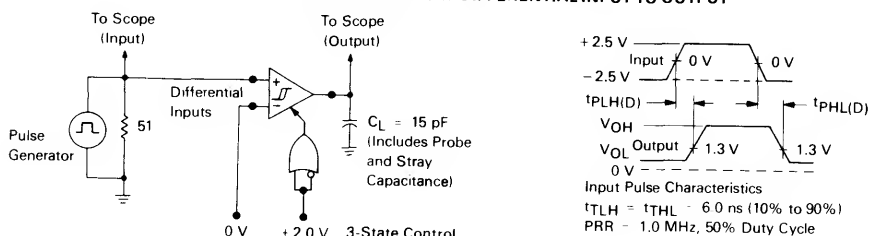
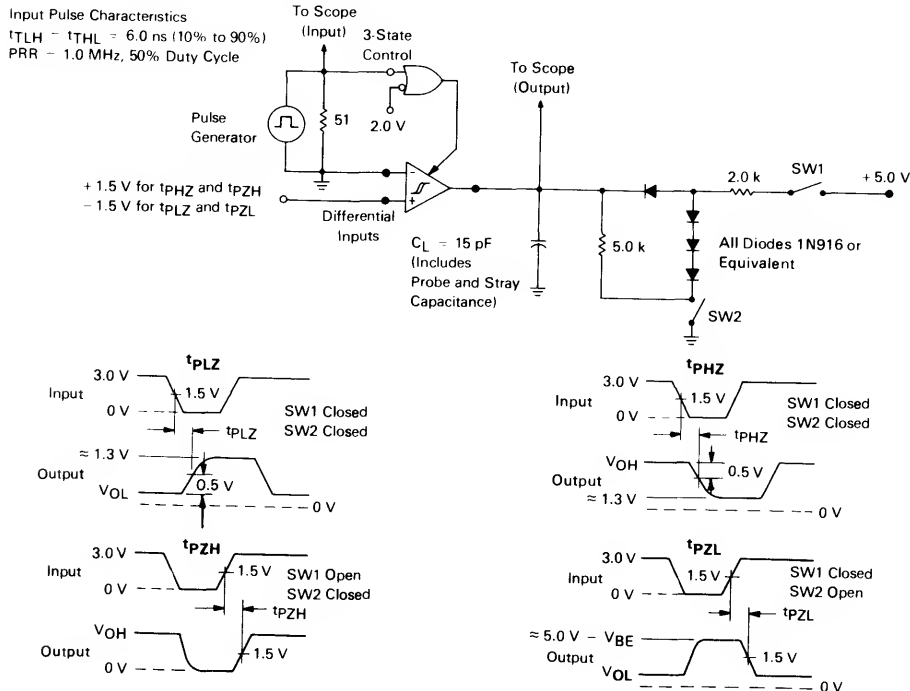


FIGURE 2 - PROPAGATION DELAY THREE-STATE CONTROL INPUT TO OUTPUT



QUAD THREE-STATE BUS TRANSCEIVER

This quad three-state bus transceiver features both excellent MOS or MPU compatibility, due to its high impedance PNP transistor input, and high-speed operation made possible by the use of Schottky diode clamping. Both the -48 mA driver and -20 mA receiver outputs are short-circuit protected and employ three-state enabling inputs.

The device is useful as a bus extender in systems employing the M6800 family or other comparable MPU devices. The maximum input current of $200 \mu\text{A}$ at any of the device input pins assures proper operation despite the limited drive capability of the MPU chip. The inputs are also protected with Schottky-barrier diode clamps to suppress excessive undershoot voltages.

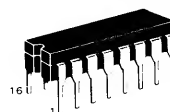
The MC8T26A is identical to the NE8T26A and it operates from a single $+5$ V supply.

- High Impedance Inputs
- Single Power Supply
- High Speed Schottky Technology
- Three-State Drivers and Receivers
- Compatible with M6800 Family Microprocessor

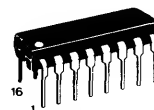
MC8T26A (MC6880A)

QUAD THREE-STATE BUS TRANSCEIVER

MONOLITHIC SCHOTTKY INTEGRATED CIRCUITS



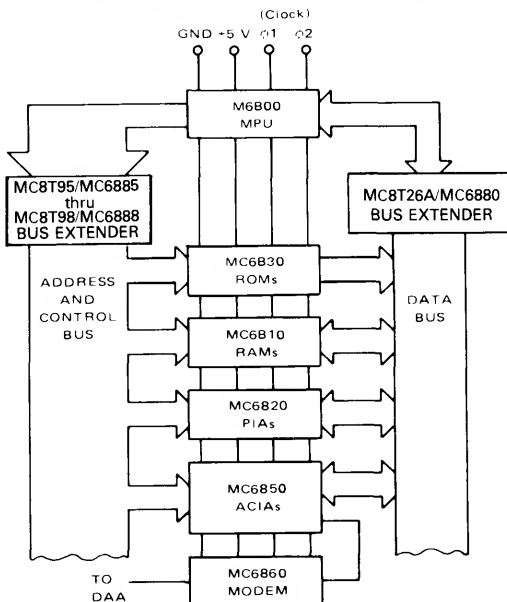
L SUFFIX
 CERAMIC PACKAGE
 CASE 620



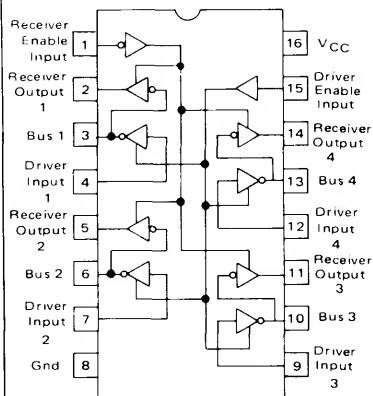
P SUFFIX
 PLASTIC PACKAGE
 CASE 648

7

MICROPROCESSOR BUS EXTENDER APPLICATION



PIN CONNECTIONS — MC8T26A (MC6880A)



ORDERING INFORMATION

Device	Alternate	Temperature Range	Package
MC8T26AL	MC6880AL	0 to $+75^{\circ}\text{C}$	Ceramic DIP
MC8T26AP	MC6880AP		Plastic DIP

MC8T26A

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V _{CC}	8.0	V _{dc}
Input Voltage	V _I	5.5	V _{dc}
Junction Temperature	T _J	175	°C
Ceramic Package		150	
Plastic Package			
Operating Ambient Temperature Range	T _A	0 to +75	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (4.75 V ≤ V_{CC} ≤ 5.25 V and 0°C ≤ T_A ≤ 75°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current — Low Logic State (Receiver Enable Input, V _{IL} (RE) = 0.4 V) (Driver Enable Input, V _{IL} (DE) = 0.4 V) (Driver Input, V _{IL} (D) = 0.4 V) (Bus (Receiver) Input, V _{IL} (B) = 0.4 V)	I _{IL} (RE) I _{IL} (DE) I _{IL} (D) I _{IL} (B)	— — — —	— — — —	-200 -200 -200 -200	μA
Input Disabled Current — Low Logic State (Driver Input, V _{IL} (D) = 0.4 V)	I _{IL} (D) DIS	—	—	-25	μA
Input Current: High Logic State (Receiver Enable Input, V _{IH} (RE) = 5.25 V) (Driver Enable Input, V _{IH} (DE) = 5.25 V) (Driver Input, V _{IH} (D) = 5.25 V) (Receiver Input, V _{IH} (B) = 5.25 V)	I _{IH} (RE) I _{IH} (DE) I _{IH} (D) I _{IH} (B)	— — — —	— — — —	25 25 25 100	μA
Input Voltage — Low Logic State (Receiver Enable Input) (Driver Enable Input) (Driver Input) (Receiver Input)	V _{IL} (RE) V _{IL} (DE) V _{IL} (D) V _{IL} (B)	— — — —	— — — —	0.85 0.85 0.85 0.85	V
Input Voltage — High Logic State (Receiver Enable Input) (Driver Enable Input) (Driver Input) (Receiver Input)	V _{IH} (RE) V _{IH} (DE) V _{IH} (D) V _{IH} (B)	2.0 2.0 2.0 2.0	— — — —	— — — —	V
Output Voltage — Low Logic State (Bus Driver) Output, I _{OL} (B) = 48 mA) (Receiver Output, I _{OL} (R) = 20 mA)	V _{OL} (B) V _{OL} (R)	— —	— —	0.5 0.5	V
Output Voltage — High Logic State (Bus (Driver) Output, I _{OH} (B) = -10 mA) (Receiver Output, I _{OH} (R) = -2.0 mA) (Receiver Output, I _{OH} (R) = -100 μA, V _{CC} = 5.0 V)	V _{OH} (B) V _{OH} (R) V _{OH} (R)	2.4 2.4 3.5	3.1 3.1 —	— — —	V
Output Disabled Leakage Current — High Logic State (Bus Driver) Output, V _{OH} (B) = 2.4 V) (Receiver Output, V _{OH} (R) = 2.4 V)	I _{OHL} (B) I _{OHL} (R)	— —	— —	100 100	μA
Output Disabled Leakage Current — Low Logic State (Bus Output, V _{OL} (B) = 0.5 V) (Receiver Output, V _{OL} (R) = 0.5 V)	I _{OLL} (B) I _{OLL} (R)	— —	— —	-100 -100	μA
Input Clamp Voltage (Driver Enable Input I _{ID} (DE) = -12 mA) (Receiver Enable Input I _{IC} (RE) = +12 mA) (Driver Input I _{IC} (D) = -12 mA)	V _{IC} (DE) V _{IC} (RE) V _{IC} (D)	— — —	— — —	-1.0 -1.0 -1.0	V
Output Short Circuit Current, V _{CC} = 5.25 V, Note 1 (Bus (Driver) Output) (Receiver Output)	I _{OS} (B) I _{OS} (R)	-50 -30	— —	-150 -75	mA
Power Supply Current (V _{CC} = 5.25 V)	I _{CC}	—	—	87	mA

Note 1. Only one output may be short-circuited at a time.

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Characteristic	Symbol	Figure	Min	Max	Unit
Propagation Delay Time from Receiver (Bus) Input to High Logic State Receiver Output	t _{PLH} (R)	1	—	14	ns
Propagation Delay Time from Receiver (Bus) Input to Low Logic State Receiver Output	t _{PHL} (R)	1	—	14	ns
Propagation Delay Time from Driver Input to High Logic State Driver (Bus) Output	t _{PLH} (D)	2	—	14	ns
Propagation Delay Time from Driver Input to Low Logic State Driver (Bus) Output	t _{PHL} (D)	2	—	14	ns
Propagation Delay Time from Receiver Enable Input to High Impedance (Open) Logic State Receiver Output	t _{PLZ} (RE)	3	—	15	ns
Propagation Delay Time from Receiver Enable Input to Low Logic Level Receiver Output	t _{PZL} (RE)	3	—	20	ns
Propagation Delay Time from Driver Enable Input to High Impedance Logic State Driver (Bus) Output	t _{PLZ} (DE)	4	—	20	ns
Propagation Delay Time from Driver Enable Input to Low Logic State Driver (Bus) Output	t _{PZL} (DE)	4	—	25	ns

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MC8T26A

FIGURE 2 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM DRIVER INPUT TO BUS (DRIVER) OUTPUT, $t_{PLH(D)}$ AND $t_{PHL(D)}$

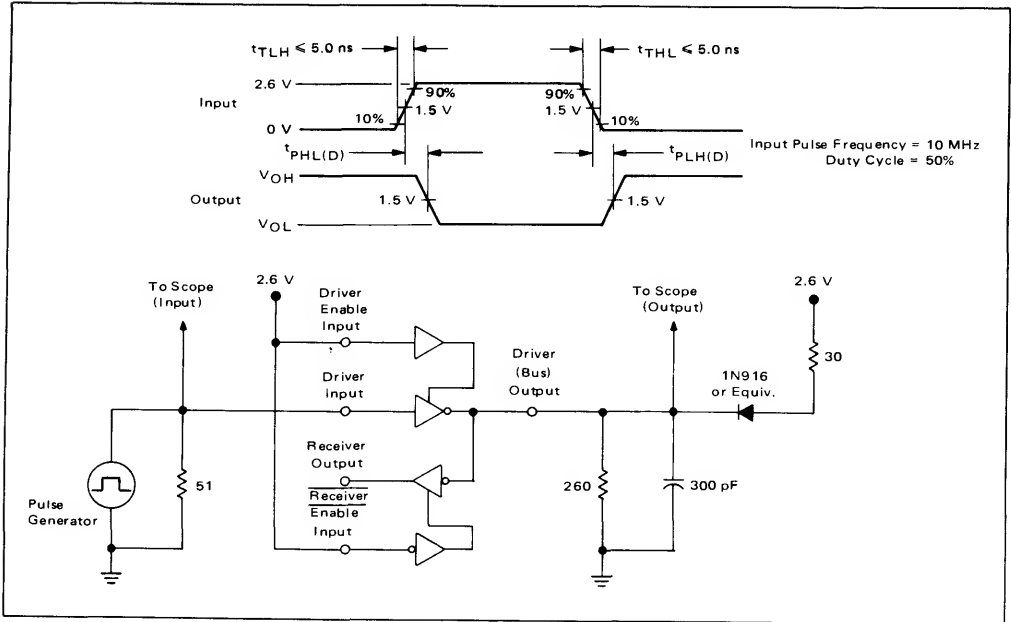
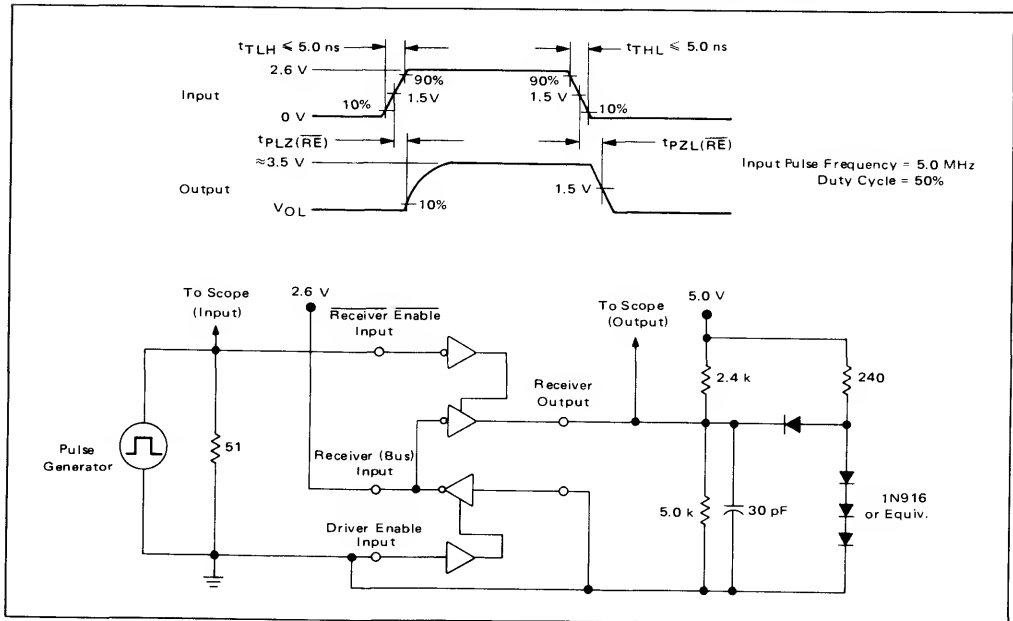


FIGURE 3 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM RECEIVER ENABLE INPUT TO RECEIVER OUTPUT, $t_{PLZ(RE)}$ AND $t_{PZL(RE)}$



MC8T26A

FIGURE 4 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIMES FROM DRIVER ENABLE INPUT TO DRIVER (BUS) OUTPUT, $t_{PLZ(DE)}$ AND $t_{PLZ(DE)}$

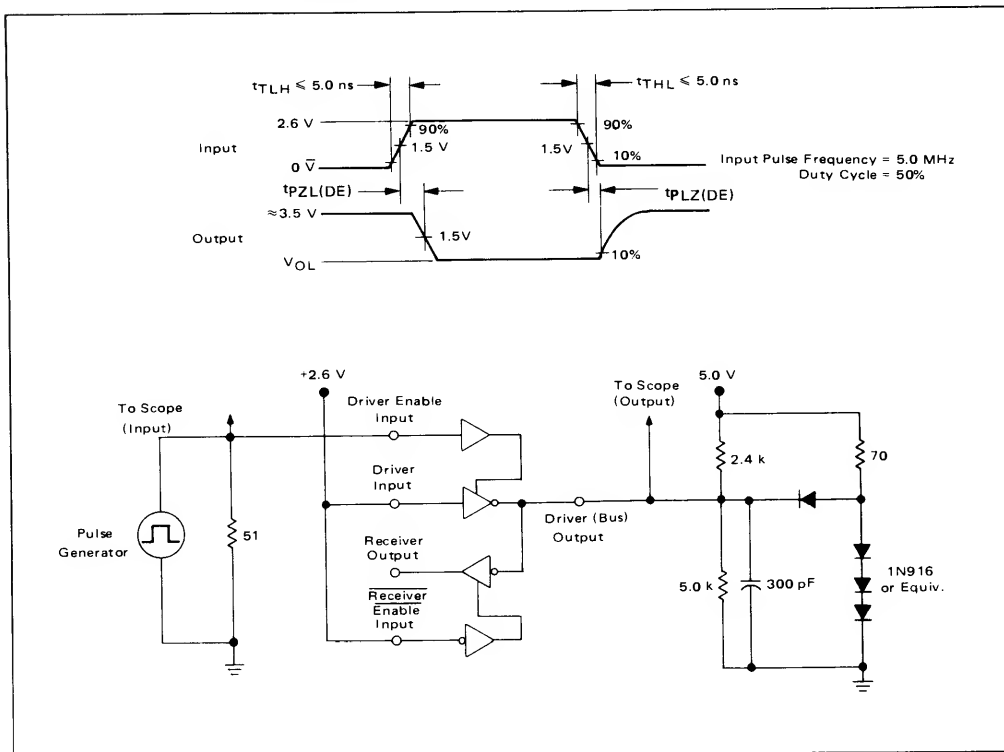
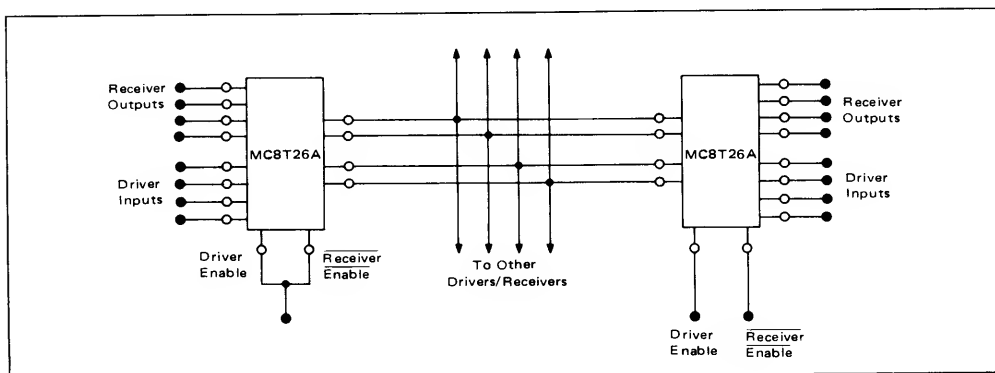


FIGURE 5 – BIDIRECTIONAL BUS APPLICATIONS



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

NONINVERTING QUAD THREE-STATE BUS TRANSCEIVER

This quad three-state bus transceiver features both excellent MOS or MPU compatibility, due to its high impedance PNP transistor input, and high-speed operation made possible by the use of Schottky diode clamping. Both the -48 mA driver and -20 mA receiver outputs are short circuit protected and employ three-state enabling inputs.

The device is useful as a bus extender in systems employing the M6800 family or other comparable MPU devices. The maximum input current of $200 \mu\text{A}$ at any of the device input pins assures proper operation despite the limited drive capability of the MPU chip. The inputs are also protected with Schottky-barrier diode clamps to suppress excessive undershoot voltages.

Propagation delay times for the driver portion are 17 ns maximum while the receiver portion runs 17 ns. The MC8T28 is identical to the NE8T28 and it operates from a single $+5$ V supply.

- High Impedance Inputs
- Single Power Supply
- High Speed Schottky Technology
- Three-State Drivers and Receivers
- Compatible with M6800 Family Microprocessor
- Non-Inverting

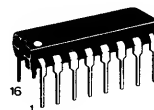
MC8T28 (MC6889)

NONINVERTING BUS TRANSCEIVER

MONOLITHIC SCHOTTKY INTEGRATED CIRCUITS

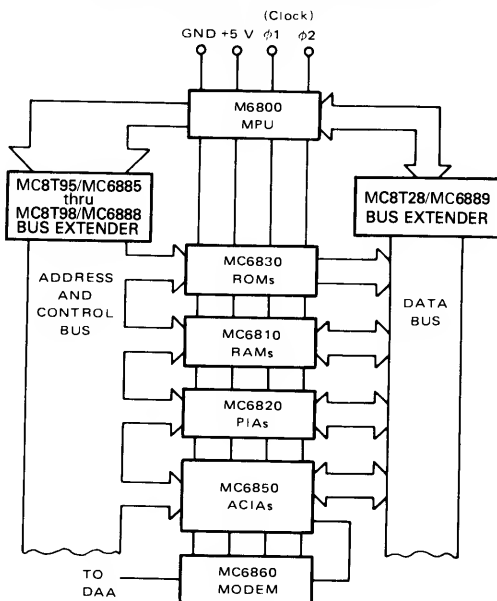


L SUFFIX
CERAMIC PACKAGE
CASE 620

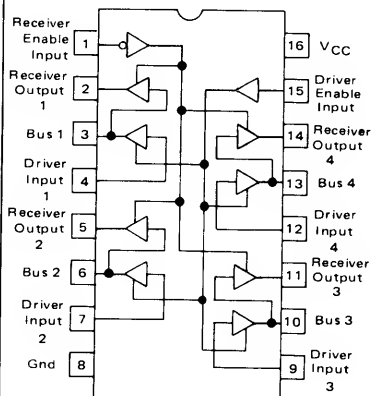


P SUFFIX
PLASTIC PACKAGE
CASE 648

MICROPROCESSOR BUS EXTENDER APPLICATION



PIN CONNECTIONS — MC8T28 (MC6889)



ORDERING INFORMATION

Device	Alternate	Temperature Range	Package
MC8T28L	MC6889L	0 to $+75^{\circ}\text{C}$	Ceramic DIP
MC8T28P	MC6889P		Plastic DIP

MC8T28

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V _{CC}	8.0	Vdc
Input Voltage	V _I	5.5	Vdc
Junction Temperature	T _J	175	°C
Ceramic Package		150	
Plastic Package			
Operating Ambient Temperature Range	T _A	0 to +75	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (4.75 V < V_{CC} < 5.25 V and 0°C < T_A < 75°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current – Low Logic State (Receiver Enable Input, V _{IL} (RE) = 0.4 V) (Driver Enable Input, V _{IL} (DE) = 0.4 V) (Driver Input, V _{IL} (D) = 0.4 V) (Bus (Receiver) Input, V _{IL} (B) = 0.4 V)	I _{IL} (RE) I _{IL} (DE) I _{IL} (D) I _{IL} (B)	– – – –	– – – –	-200 -200 -200 -200	μA
Input Disabled Current – Low Logic State (Driver Input, V _{IL} (D) = 0.4 V)	I _{IL} (D) DIS	–	–	-25	μA
Input Current-High Logic State (Receiver Enable Input, V _{IH} (RE) = 5.25 V) (Driver Enable Input, V _{IH} (DE) = 5.25 V) (Driver Input, V _{IH} (D) = 5.25 V)	I _{IH} (RE) I _{IH} (DE) I _{IH} (D)	– – –	– – –	25 25 25	μA
Input Voltage – Low Logic State (Receiver Enable Input) (Driver Enable Input) (Driver Input) (Receiver Input)	V _{IL} (RE) V _{IL} (DE) V _{IL} (D) V _{IL} (B)	– – – –	– – – –	0.85 0.85 0.85 0.85	V
Input Voltage – High Logic State (Receiver Enable Input) (Driver Enable Input) (Driver Input) (Receiver Input)	V _{IH} (RE) V _{IH} (DE) V _{IH} (D) V _{IH} (B)	2.0 2.0 2.0 2.0	– – – –	– – – –	V
Output Voltage – Low Logic State (Bus Driver) Output, I _{OL} (B) = 48 mA (Receiver Output, I _{OL} (R) = 20 mA)	V _{OL} (B) V _{OL} (R)	– –	– –	0.5 0.5	V
Output Voltage – High Logic State (Bus (Driver) Output, I _{OH} (B) = -10 mA) (Receiver Output, I _{OH} (R) = -2.0 mA) (Receiver Output, I _{OH} (R) = -100/μA, V _{CC} = 5.0 V)	V _{OH} (B) V _{OH} (R)	2.4 2.4 3.5	3.1 3.1 –	– – –	V
Output Disabled Leakage Current – High Logic State (Bus Driver) Output, V _{OH} (B) = 2.4 V) (Receiver Output, V _{OH} (R) = 2.4 V)	I _{OHL} (B) I _{OHL} (R)	– –	– –	100 100	μA
Output Disabled Leakage Current – Low Logic State (Bus Output, V _{OL} (B) = 0.5 V) (Receiver Output, V _{OL} (R) = 0.5 V)	I _{OLL} (B) I _{OLL} (R)	– –	– –	-100 -100	μA
Input Clamp Voltage (Driver Enable Input I _{ID} (DE) = -12 mA) (Receiver Enable Input I _{IC} (RE) = +12 mA) (Driver Input I _{IC} (D) = -12 mA)	V _{IC} (DE) V _{IC} (RE) V _{IC} (D)	– – –	– – –	-1.0 -1.0 -1.0	V
Output Short Circuit Current, V _{CC} = 5.25 V, Note 1 (Bus (Driver) Output) (Receiver Output)	I _{OS} (B) I _{OS} (R)	-50 -30	– –	-150 -75	mA
Power Supply Current (V _{CC} = 5.25 V)	I _{CC}	–	–	110	mA

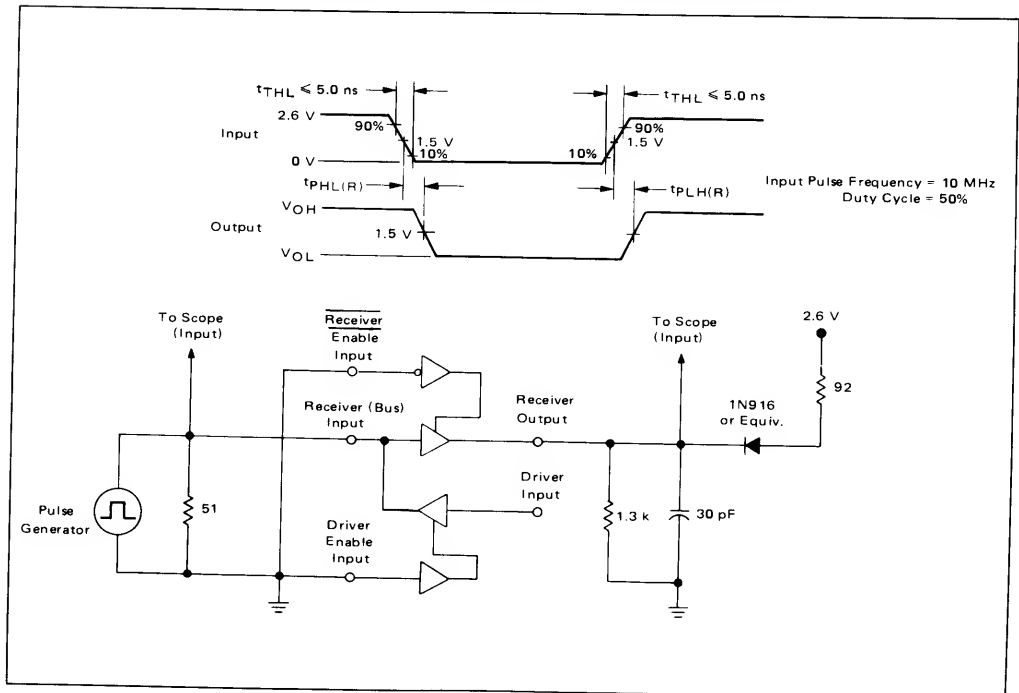
Note 1. Only one output may be short-circuited at a time.

MC8T28

SWITCHING CHARACTERISTICS (Unless otherwise noted, $V_{CC} = 5.0\text{ V}$ and $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	Min	Max	Unit
Propagation Delay Time—Receiver ($C_L = 30\text{ pF}$)	$t_{PLH}(R)$	—	17	ns
	$t_{PHL}(R)$	—	17	ns
Propagation Delay Time—Driver ($C_L = 300\text{ pF}$)	$t_{PLH}(D)$	—	17	ns
	$t_{PHL}(D)$	—	17	ns
Propagation Delay Time—Enable ($C_L = 30\text{ pF}$)	$t_{PZL}(R)$	—	23	ns
	$t_{PLZ}(R)$	—	18	ns
	$t_{PZL}(D)$	—	28	ns
	$t_{PLZ}(D)$	—	23	ns

FIGURE 1 — TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY FROM BUS (RECEIVER) INPUT TO RECEIVER OUTPUT, $t_{PLH}(R)$ AND $t_{PHL}(R)$



MC8T28

FIGURE 2 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM DRIVER INPUT TO BUS (DRIVER) OUTPUT, $t_{PLH(D)}$ AND $t_{PLH(D)}$

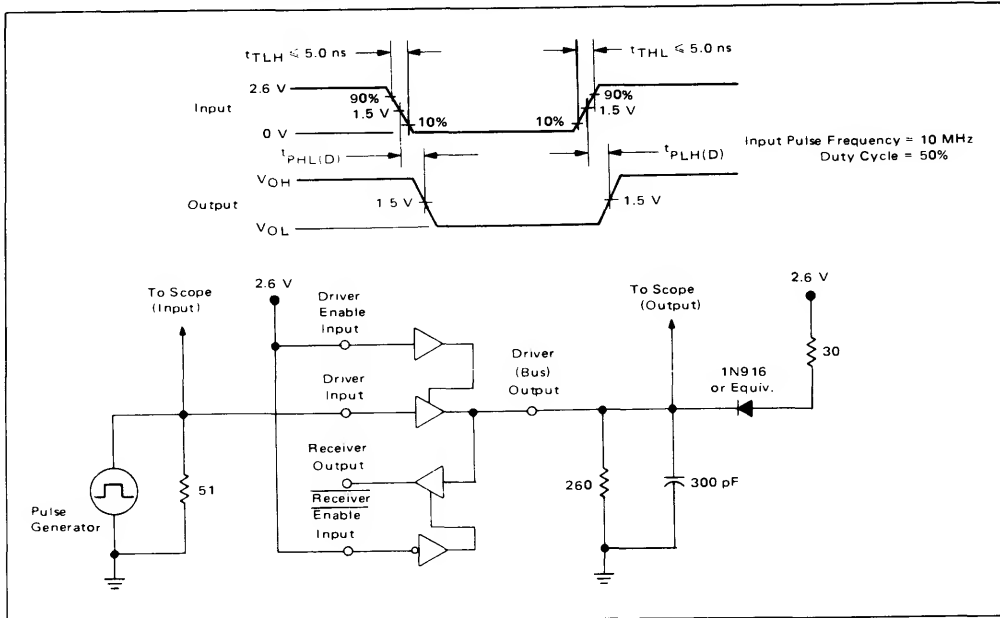
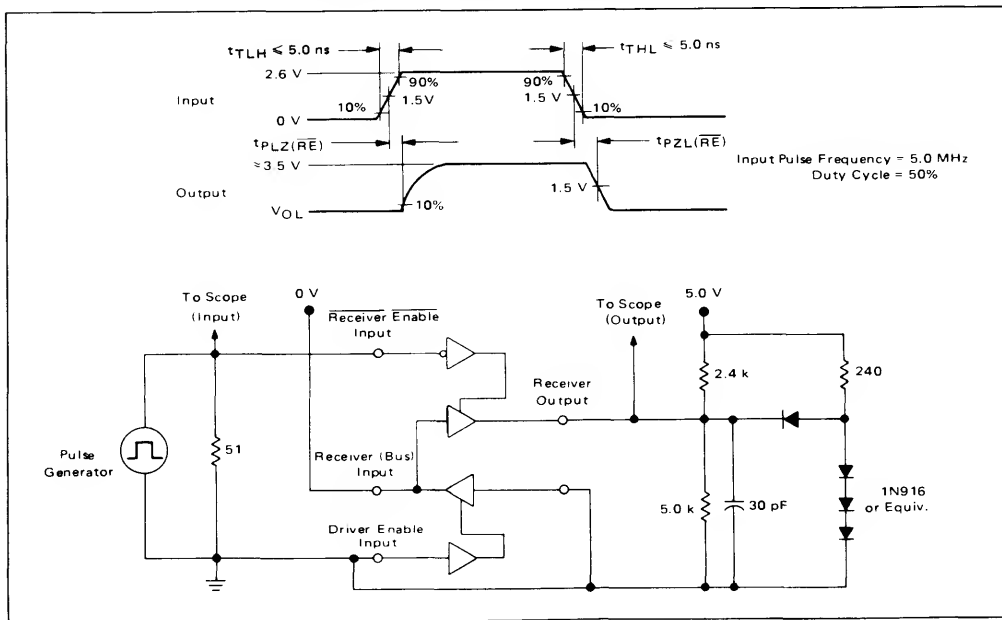


FIGURE 3 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM RECEIVER ENABLE INPUT TO RECEIVER OUTPUT, $t_{PLZ(RE)}$ AND $t_{PZL(RE)}$



MC8T28

FIGURE 4 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIMES FROM DRIVER ENABLE INPUT TO DRIVER (BUS) OUTPUT, $t_{PLZ(DE)}$ AND $t_{PLZ(DE)}$

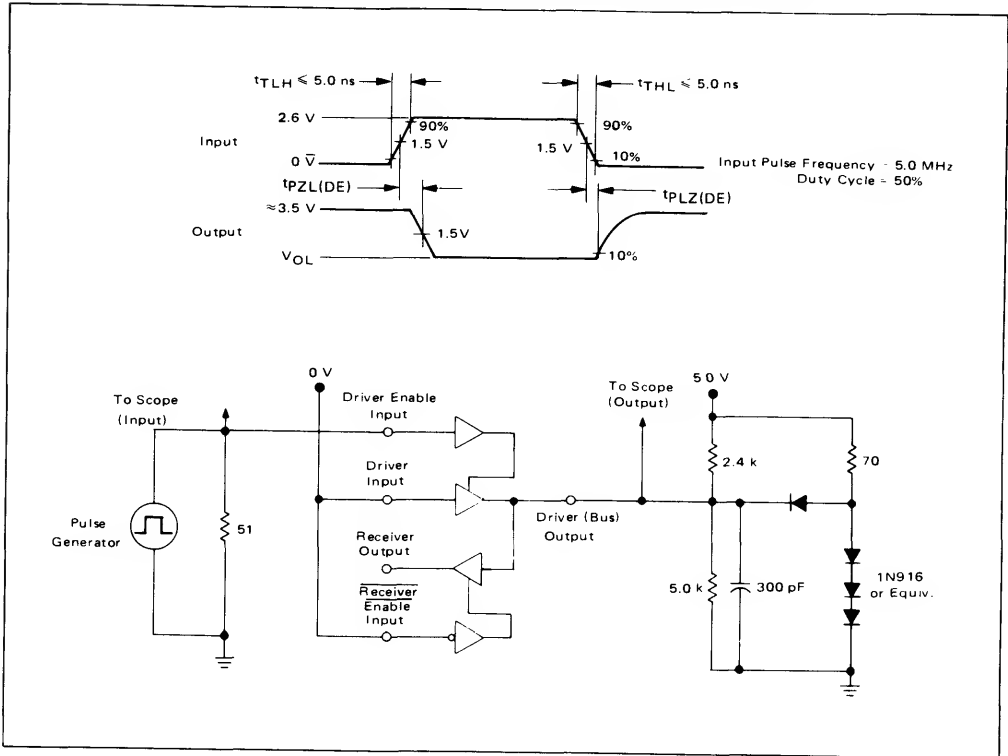
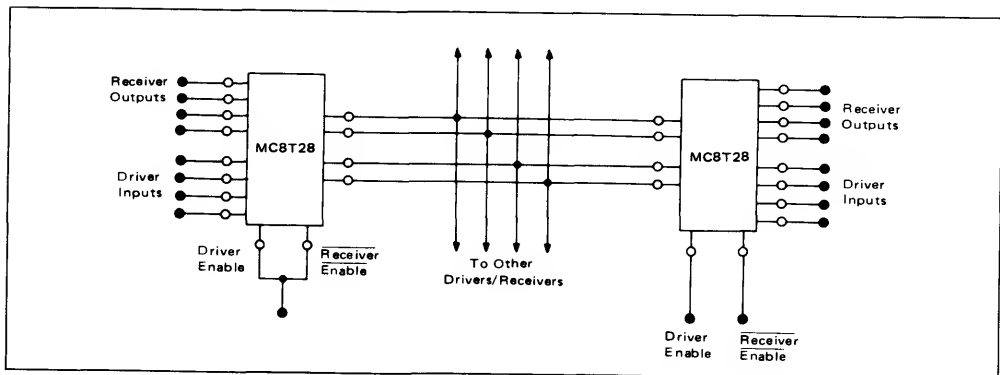


FIGURE 5 – BIDIRECTIONAL BUS APPLICATIONS



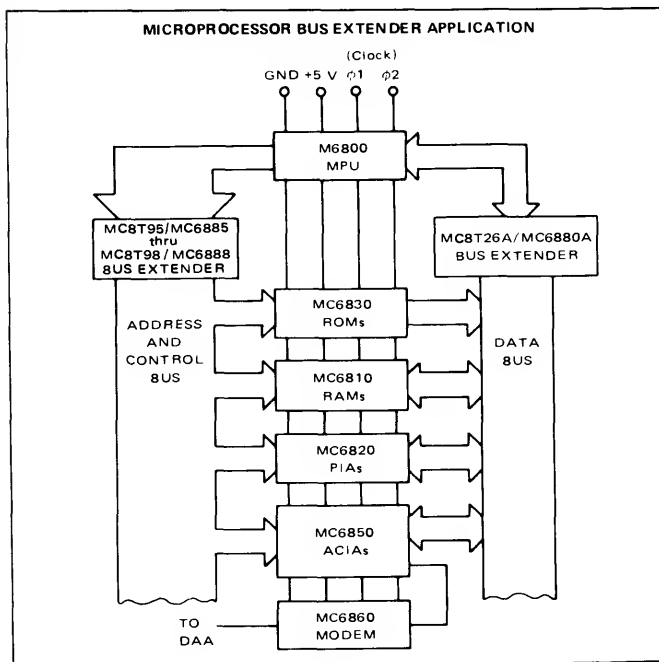
HEX THREE-STATE BUFFER INVERTERS

This series of devices combines three features usually found desirable in bus-oriented systems: 1) High impedance logic inputs insure that these devices do not seriously load the bus; 2) Three-state logic configuration allows buffers not being utilized to be effectively removed from the bus; 3) Schottky technology allows high-speed operation.

The devices differ in that the non-inverting MC8T95/MC6885 and inverting MC8T96/MC6886 provide a two-input Enable which controls all six buffers, while the non-inverting MC8T97/MC6887 and inverting MC8T98/MC6888 provide two Enable inputs — one controlling four buffers and the other controlling the remaining two buffers.

The units are well-suited for Address buffers on the M6800 or similar microprocessor application.

- High Speed — 8.0 ns (Typ)
- Three-State Logic Configuration
- Single +5 V Power Supply Requirement
- Compatible with 74LS Logic or M6800 Microprocessor Systems
- High Impedance PNP Inputs Assure Minimal Loading of the Bus



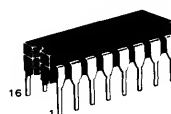
MC8T95 (MC6885)

MC8T96 (MC6886)

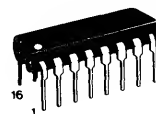
MC8T97 (MC6887)

MC8T98 (MC6888)

HEX THREE-STATE BUFFER/INVERTERS

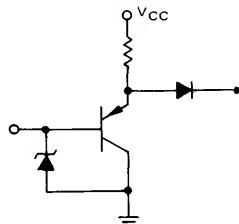


L SUFFIX
 CERAMIC PACKAGE
 CASE 620

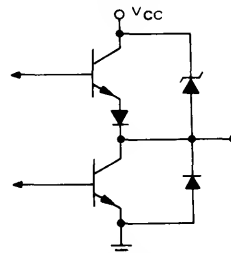


P SUFFIX
 PLASTIC PACKAGE
 CASE 648

INPUT EQUIVALENT CIRCUIT



OUTPUT EQUIVALENT CIRCUIT



ORDERING INFORMATION

(Temperature Range for the following devices = 0 to +75°C)

DEVICE	ALTERNATE	PACKAGE
MC8T95L	MC6885L	Ceramic DIP
MC8T96L	MC6886L	Ceramic DIP
MC8T97L	MC6887L	Ceramic DIP
MC8T98L	MC6888L	Ceramic DIP
MC8T95P	MC6885P	Plastic DIP
MC8T96P	MC6886P	Plastic DIP
MC8T97P	MC6887P	Plastic DIP
MC8T98P	MC6888P	Plastic DIP

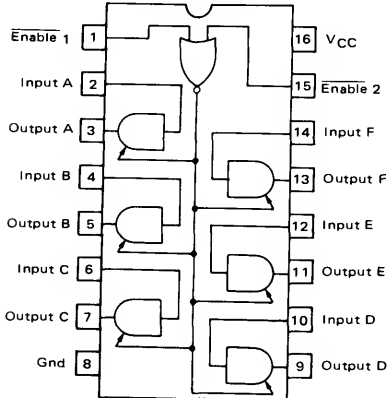
MC8T95, MC8T96, MC8T97, MC8T98

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.0	Vdc
Input Voltage	V_I	5.5	Vdc
Operating Ambient Temperature Range	T_A	0 to +75	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J		$^\circ\text{C}$
Plastic Package		150	
Ceramic Package		175	

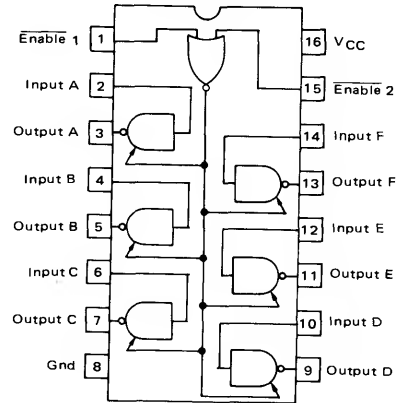
PIN CONNECTIONS AND TRUTH TABLES

MC8T95/MC6885



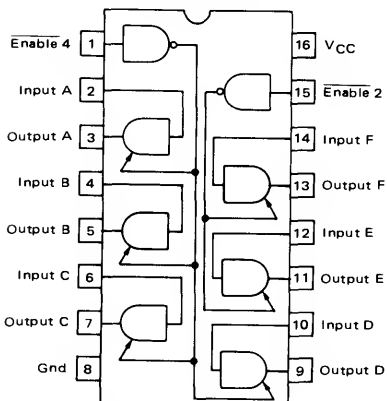
Enable 2	Enable 1	Input	Output
L	L	L	L
L	L	H	H
L	H	X	Z
H	L	X	Z
H	H	X	Z

MC8T96/MC6886



Enable 2	Enable 1	Input	Output
L	L	L	H
L	L	H	L
L	H	X	Z
H	L	X	Z
H	H	X	Z

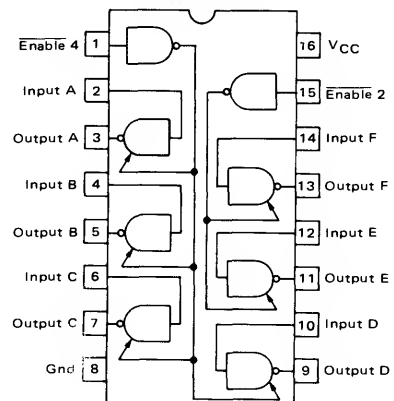
MC8T97/MC6887



Enable	Input	Output
L	L	L
L	H	H
H	X	Z

L = Low Logic State
H = High Logic State
Z = Third (High Impedance) State
X = Irrelevant

MC8T98/MC6888



Enable	Input	Output
L	L	H
L	H	L
H	X	Z

MC8T95, MC8T96, MC8T97, MC8T98

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, $0^{\circ}\text{C} \leq T_A \leq 75^{\circ}\text{C}$ and $4.75\text{ V} \leq V_{CC} \leq 5.25\text{ V}$)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage — High Logic State ($V_{CC} = 4.75\text{ V}$, $T_A = 25^{\circ}\text{C}$)	V_{IH}	2.0	—	—	V
Input Voltage — Low Logic State ($V_{CC} = 4.75\text{ V}$, $T_A = 25^{\circ}\text{C}$)	V_{IL}	—	—	0.8	V
Input Current — High Logic State ($V_{CC} = 5.25\text{ V}$, $V_{IH} = 2.4\text{ V}$)	I_{IH}	—	—	40	μA
Input Current — Low Logic State ($V_{CC} = 5.25\text{ V}$, $V_{IL} = 0.5\text{ V}$, $V_{IL(E)} = 0.5\text{ V}$)	I_{IL}	—	—	-400	μA
Input Current — High Impedance State ($V_{CC} = 5.25\text{ V}$, $V_{IL(I)} = 0.5\text{ V}$, $V_{IH(E)} = 2.0\text{ V}$)	$I_{IH(E)}$	—	—	-40	μA
Output Voltage — High Logic State ($V_{CC} = 4.75\text{ V}$, $I_{OH} = -5.2\text{ mA}$)	V_{OH}	2.4	—	—	V
Output Voltage — Low Logic State ($I_{OL} = 48\text{ mA}$)	V_{OL}	—	—	0.5	V
Output Current — High Impedance State ($V_{CC} = 5.25\text{ V}$, $V_{OH} = 2.4\text{ V}$) ($V_{CC} = 5.25\text{ V}$, $V_{OL} = 0.5\text{ V}$)	I_{OZ}	— —	— —	40 -40	μA
Output Short-Circuit Current ($V_{CC} = 5.25\text{ V}$, $V_O = 0$) (only one output can be shorted at a time)	I_{OS}	-40	-80	-115	mA
Power Supply Current ($V_{CC} = 5.25\text{ V}$) MC8T95, MC8T97, MC6885, MC6887 MC8T96, MC8T98, MC6886, MC6888	I_{CC}	— —	65 59	98 89	mA
Input Clamp Voltage ($V_{CC} = 4.75\text{ V}$, $I_{IC} = -12\text{ mA}$)	V_{IC}	—	—	-1.5	V
Output V_{CC} Clamp Voltage ($V_{CC} = 0$, $I_{OC} = 12\text{ mA}$)	V_{OC}	—	—	1.5	V
Output Gnd Clamp Voltage ($V_{CC} = 0$, $I_{OC} = -12\text{ mA}$)	V_{OC}	—	—	-1.5	V
Input Voltage ($I_I = 1.0\text{ mA}$)	V_I	5.5	—	—	V

SWITCHING CHARACTERISTICS ($V_{CC} = 5.0\text{ V}$, $T_A = 25^{\circ}\text{C}$ unless otherwise noted.)

Characteristic	Symbol	MC8T95/97 MC6885/87			MC8T96/98 MC6886/88			Unit
		Min	Typ	Max	Min	Typ	Max	
Propagation Delay Time — High to Low State ($C_L = 50\text{ pF}$) ($C_L = 250\text{ pF}$) ($C_L = 375\text{ pF}$) ($C_L = 500\text{ pF}$)	t_{PHL}	3.0 — — —	— 16 20 23	12 — — —	4.0 — — —	— 15 18 22	11 — — —	ns
Propagation Delay Time — Low to High State ($C_L = 50\text{ pF}$) ($C_L = 250\text{ pF}$) ($C_L = 375\text{ pF}$) ($C_L = 500\text{ pF}$)	t_{PLH}	3.0 — — —	— 25 33 42	13 — — —	3.0 — — —	— 22 28 35	10 — — —	ns
Transition Time — High to Low State ($C_L = 250\text{ pF}$) ($C_L = 375\text{ pF}$) ($C_L = 500\text{ pF}$)	t_{THL}	— — —	10 11 14	— — —	— — —	10 13 15	— — —	ns
Transition Time — Low to High State ($C_L = 250\text{ pF}$) ($C_L = 375\text{ pF}$) ($C_L = 500\text{ pF}$)	t_{TLH}	— — —	32 42 60	— — —	— — —	28 38 53	— — —	ns
Propagation Delay Time — High State to Third State ($C_L = 5.0\text{ pF}$)	$t_{PHZ(\bar{E})}$	—	—	10	—	—	10	ns
Propagation Delay Time — Low State to Third State ($C_L = 5.0\text{ pF}$)	$t_{PLZ(\bar{E})}$	—	—	12	—	—	16	ns
Propagation Delay Time — Third State to High State ($C_L = 50\text{ pF}$)	$t_{PZH(\bar{E})}$	—	—	25	—	—	22	ns
Propagation Delay Time — Third State to Low State ($C_L = 50\text{ pF}$)	$t_{PZL(\bar{E})}$	—	—	25	—	—	24	ns

MC8T95, MC8T96, MC8T97, MC8T98

FIGURE 1 – TEST CIRCUIT FOR SWITCHING CHARACTERISTICS

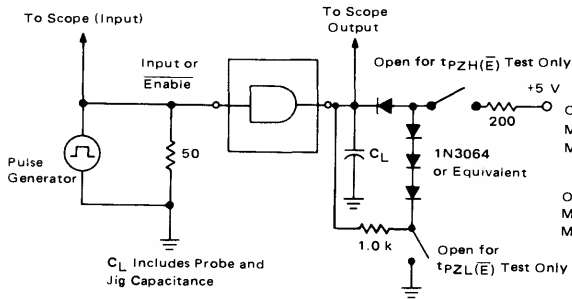


FIGURE 2 – WAVEFORMS FOR PROPAGATION DELAY TIMES INPUT TO OUTPUT

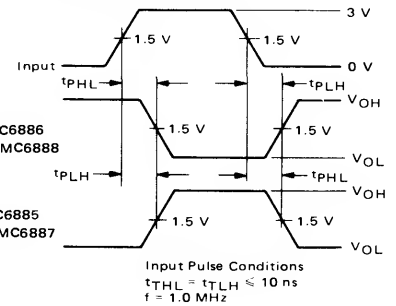
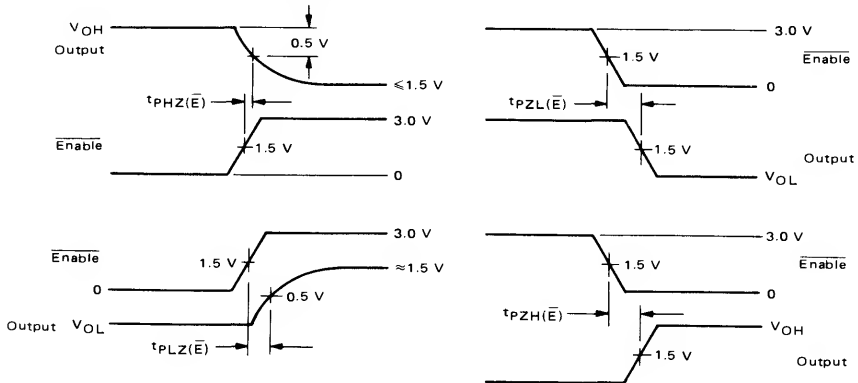


FIGURE 3 – WAVEFORMS FOR PROPAGATION DELAY TIMES – ENABLE TO OUTPUT



H = High-Logic State, L = Low-Logic State, Z = High Impedance State

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

HIGH VOLTAGE, HIGH CURRENT DARLINGTON TRANSISTOR ARRAYS

The seven NPN Darlington connected transistors in these arrays are well suited for driving lamps, relays, or printer hammers in a variety of industrial and consumer applications. Their high breakdown voltage and internal suppression diodes insure freedom from problems associated with inductive loads. Peak inrush currents to 600 mA permit them to drive incandescent lamps.

The MC1411,B device is a general purpose array for use with DTL, TTL, PMOS, or CMOS Logic. The MC1412,B contains a zener diode and resistor in series with the input to limit input current for use with 14 to 25 Volt PMOS Logic. The MC1413,B with a 2.7 k Ω series input resistor is well suited for systems utilizing a 5 Volt TTL or CMOS Logic. The MC1416,B uses a series 10.5 k Ω resistor and is useful in 8 to 18 Volt MOS systems.

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ and rating apply to any one device in the package unless otherwise noted.)

Rating	Symbol	Value	Unit
Output Voltage	V_O	50	V
Input Voltage (Except MC1411)	V_I	30	V
Collector Current — Continuous	I_C	500	mA
Base Current — Continuous	I_B	25	mA
Operating Ambient Temperature Range MC1411-16 MC1411B-16B	T_A	-20 to +85 -40 to +85	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-55 to +150	$^\circ\text{C}$
Junction Temperature	T_J	150	$^\circ\text{C}$
Thermal Resistance — Junction to Ambient P Suffix D Suffix	θ_{JA}	67 100	$^\circ\text{C/W}$

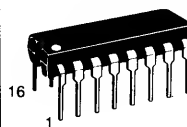
ORDERING INFORMATION

Plastic DIP	SOIC	Ambient Temperature Range
MC1411P (ULN2001A) MC1412P (ULN2002A) MC1413P (ULN2003A) MC1416P (ULN2004A)	MC1411D MC1412D MC1413D MC1416D	-20 $^\circ$ to +85 $^\circ\text{C}$
MC1411BP (ULN2001A) MC1412BP (ULN2002A) MC1413BP (ULN2003A) MC1416BP (ULN2004A)	MC1411BD MC1412BD MC1413BD MC1416BD	-40 $^\circ$ to +85 $^\circ\text{C}$

**MC1411,B
MC1412,B
MC1413,B
MC1416,B**

PERIPHERAL DRIVER ARRAYS

**SILICON MONOLITHIC
INTEGRATED CIRCUITS**

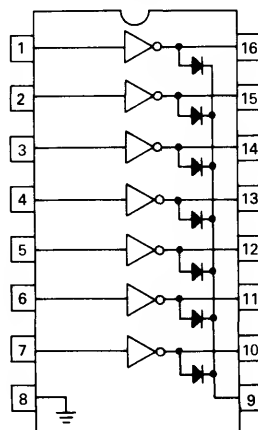


P SUFFIX
PLASTIC PACKAGE
CASE 648



D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO-16)

PIN CONNECTIONS



MC1411,B, MC1412,B, MC1413,B, MC1416,B

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Output Leakage Current ($V_O = 50\text{ V}$, $T_A = +85^\circ\text{C}$) ($V_O = 50\text{ V}$, $T_A = +25^\circ\text{C}$) ($V_O = 50\text{ V}$, $T_A = +85^\circ\text{C}$, $V_I = 6.0\text{ V}$) ($V_O = 50\text{ V}$, $T_A = +85^\circ\text{C}$, $V_I = 1.0\text{ V}$)	All Types All Types MC1412,B MC1416,B	I_{CEX}	— — — —	— — — —	100 50 500 500	μA
Collector-Emitter Saturation Voltage ($I_C = 350\text{ mA}$, $I_B = 500\text{ }\mu\text{A}$) ($I_C = 200\text{ mA}$, $I_B = 350\text{ }\mu\text{A}$) ($I_C = 100\text{ mA}$, $I_B = 250\text{ }\mu\text{A}$)	All Types All Types All Types	$V_{CE(sat)}$	— — —	1.1 0.95 0.85	1.6 1.3 1.1	V
Input Current — On Condition ($V_I = 17\text{ V}$) ($V_I = 3.85\text{ V}$) ($V_I = 5.0\text{ V}$) ($V_I = 12\text{ V}$)	MC1412,B MC1413,B MC1416,B MC1416,B	$I_{I(on)}$	— — — —	0.85 0.93 0.35 1.0	1.3 1.35 0.5 1.45	mA
Input Voltage — On Condition ($V_{CE} = 2.0\text{ V}$, $I_C = 300\text{ mA}$) ($V_{CE} = 2.0\text{ V}$, $I_C = 200\text{ mA}$) ($V_{CE} = 2.0\text{ V}$, $I_C = 250\text{ mA}$) ($V_{CE} = 2.0\text{ V}$, $I_C = 300\text{ mA}$) ($V_{CE} = 2.0\text{ V}$, $I_C = 125\text{ mA}$) ($V_{CE} = 2.0\text{ V}$, $I_C = 200\text{ mA}$) ($V_{CE} = 2.0\text{ V}$, $I_C = 275\text{ mA}$) ($V_{CE} = 2.0\text{ V}$, $I_C = 350\text{ mA}$)	MC1412,B MC1413,B MC1413,B MC1413,B MC1416,B MC1416,B MC1416,B MC1416,B	$V_{I(on)}$	— — — — — — — —	— — — — — — — —	13 2.4 2.7 3.0 5.0 6.0 7.0 8.0	V
Input Current — Off Condition ($I_C = 500\text{ }\mu\text{A}$, $T_A = +85^\circ\text{C}$)	All Types	$I_{I(off)}$	50	100	—	μA
DC Current Gain ($V_{CE} = 2.0\text{ V}$, $I_C = 350\text{ mA}$)	MC1411,B	h_{FE}	1000	—	—	—
Input Capacitance		C_I	—	15	30	pF
Turn-On Delay Time (50% E_I to 50% E_O)		t_{on}	—	0.25	1.0	μs
Turn-Off Delay Time (50% E_I to 50% E_O)		t_{off}	—	0.25	1.0	μs
Clamp Diode Leakage Current ($V_R = 50\text{ V}$)	$T_A = +25^\circ\text{C}$ $T_A = +85^\circ\text{C}$	I_R	— —	— —	50 100	μA
Clamp Diode Forward Voltage ($I_F = 350\text{ mA}$)		V_F	—	1.5	2.0	V

TYPICAL PERFORMANCE CURVES — $T_A = 25^\circ\text{C}$

FIGURE 1 — OUTPUT CURRENT versus INPUT VOLTAGE

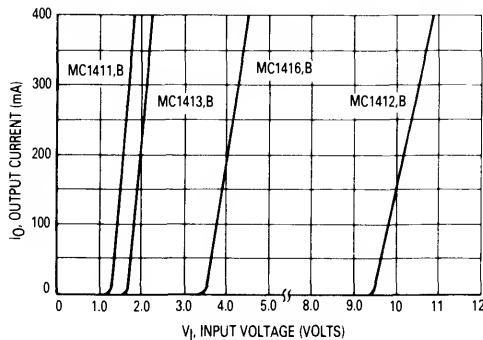
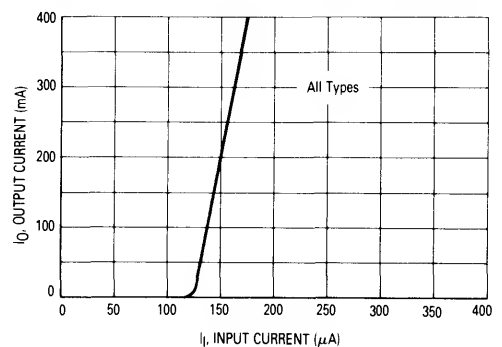


FIGURE 2 — OUTPUT CURRENT versus INPUT CURRENT



MC1411,B, MC1412,B, MC1413,B, MC1416,B

TYPICAL CHARACTERISTIC CURVES — $T_A = 25^\circ\text{C}$ (continued)

FIGURE 3 — TYPICAL OUTPUT CHARACTERISTICS

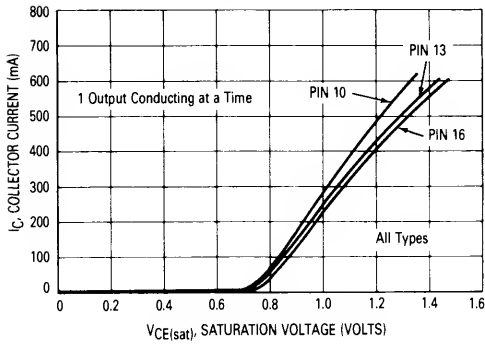


FIGURE 4 — INPUT CHARACTERISTICS — MC1412,B

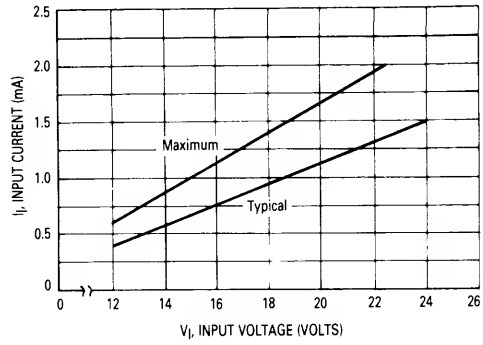


FIGURE 5 — INPUT CHARACTERISTICS — MC1413,B

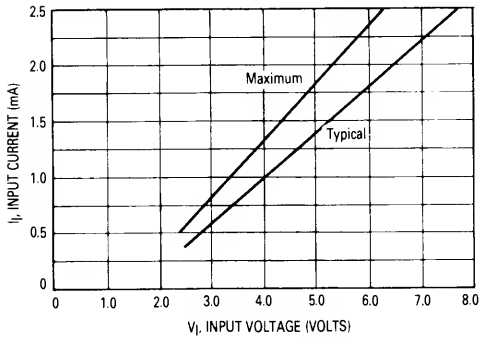


FIGURE 6 — INPUT CHARACTERISTICS — MC1416,B

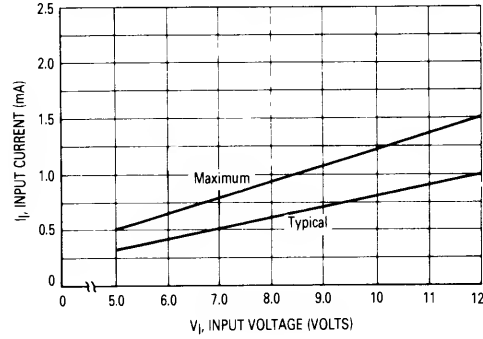
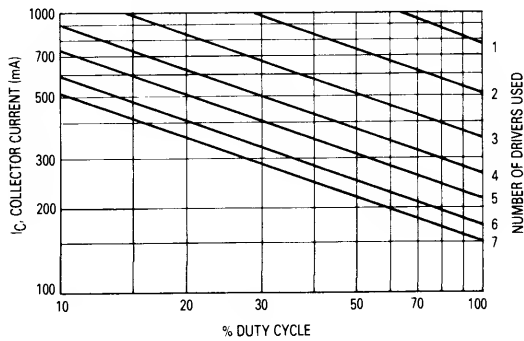
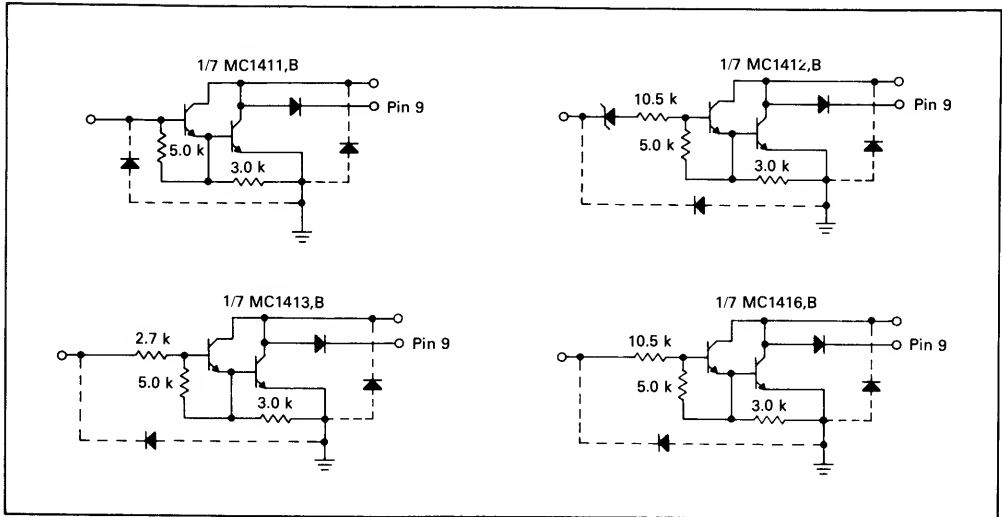


FIGURE 7 — MAXIMUM COLLECTOR CURRENT
versus DUTY CYCLE
(AND NUMBER OF DRIVERS IN USE)



MC1411,B, MC1412,B, MC1413,B, MC1416,B

FIGURE 8 — REPRESENTATIVE CIRCUIT SCHEMATICS



**DUAL PERIPHERAL-HIGH-VOLTAGE
 POSITIVE "NAND" DRIVER**

The dual driver consists of a pair of PNP buffered AND gates connected to the bases of a pair of high voltage NPN transistors. They are similar to the MC75452 drivers but with the added advantages of: 1) 70 Volt capability 2) output suppression diodes and 3) PNP buffered inputs for MOS compatibility. These features make the MC1472 ideal for mating MOS logic or microprocessors to lamps, relays, printer hammers and incandescent displays.

- 300 mA Output Capability (each transistor)
- 70 Vdc Breakdown Voltage
- Internal Output Clamp Diodes
- Low Input Loading for MOS Compatibility (PNP buffered)

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Rating	Value	Unit
Supply Voltage	7.0	Volts
Input Voltage	5.5	Volts
Output Voltage	80	Volts
Clamp Voltage	80	Volts
Output Current (Continuous)	300	mA
Operating Junction Temperature		$^\circ\text{C}$
Ceramic Package	+175	
Plastic Package	+150	
Storage Temperature Range	-65 to +150	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS

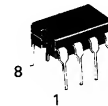
Rating	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	Volts
Operating Ambient Temperature	T_A	0	70	$^\circ\text{C}$
Output Voltage	V_O	V_{CC}	70	Volts
Clamp Voltage	V_C	V_O	70	Volts

ORDERING INFORMATION

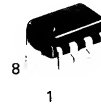
Device	Temperature Range	Package
MC1472U	0 to +70 $^\circ\text{C}$	Ceramic DIP
MC1472P1	0 to +70 $^\circ\text{C}$	Plastic DIP

MC1472

**DUAL PERIPHERAL
 POSITIVE "NAND" DRIVER
 SILICON MONOLITHIC
 INTEGRATED CIRCUITS**

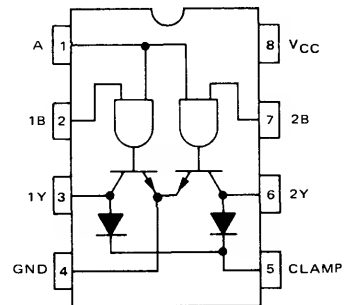


U SUFFIX
 CERAMIC PACKAGE
 CASE 693



P1 SUFFIX
 PLASTIC PACKAGE
 CASE 626

PIN CONNECTIONS



Positive Logic: $Y = AB^*$

TRUTH TABLE

A	B	Y
L	L	H ("OFF" STATE)
L	H	
H	L	
H	H	L ("ON" STATE)

H = Logic One
 L = Logic Zero

MC1472

ELECTRICAL CHARACTERISTICS (Unless otherwise noted min/max limits apply across the 0°C to 70°C temperature range with $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$. All typical values are for $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ Volts}$.)

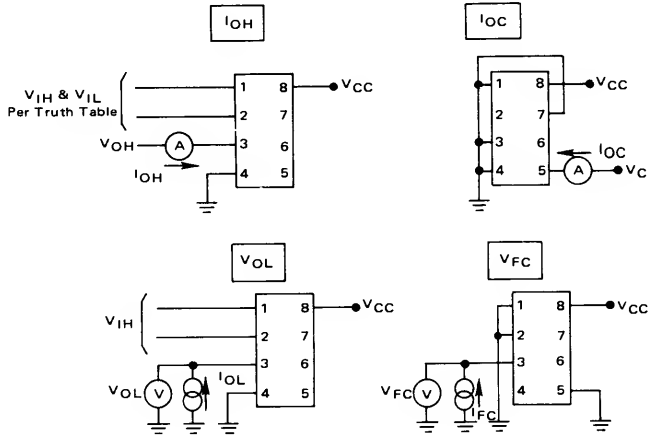
Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage — High Logic State	V_{IH}	2.0	—	5.5	Vdc
Input Voltage — Low Logic State	V_{IL}	0	—	0.8	Vdc
Input Current — Low Logic State ($V_{IL} = 0.4\text{ V}$) A Input B Input	I_{IL}	—	—	-0.3 -0.15	mA
Input Current — High Logic State ($V_{IH} = 2.4\text{ V}$) A Input B Input ($V_{IH} = 5.5\text{ V}$) A Input B Input	I_{IH}	— — — —	— — — —	40 20 200 100	μA
Input Clamp Voltage ($I_{CC} = -12\text{ mA}$)	V_{IK}	—	—	-1.5	V
Output Leakage Current — High Logic State ($V_O = 70\text{ V}$, See Test Figure)	I_{OH}	—	—	100	μA
Output Voltage — Low Logic State ($I_{OL} = 100\text{ mA}$) ($I_{OL} = 300\text{ mA}$)	V_{OL}	— —	— —	0.4 0.7	V
Output Clamp Diode Leakage Current ($V_C = 70\text{ V}$, See Test Figure)	I_{OC}	—	—	100	V
Output Clamp Forward Voltage ($I_{FC} = 300\text{ mA}$, See Test Figure)	V_{FC}	—	—	1.7	V
Power Supply Current (All Inputs at V_{IH}) (All Inputs at V_{IL})	I_{CC}	— —	— —	70 15	mA

NOTE: All currents into device pins are shown as positive, out of device pins as negative. All voltages referenced to ground unless otherwise noted.

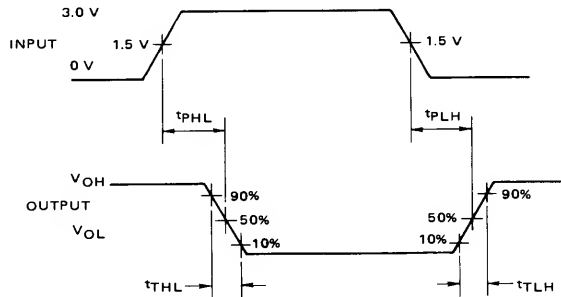
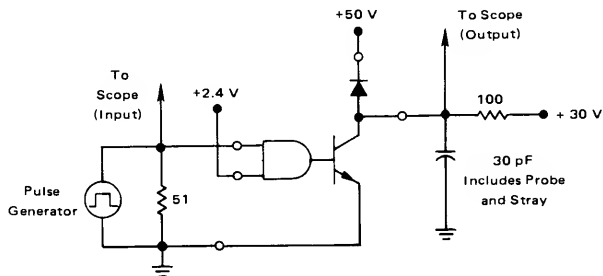
SWITCHING CHARACTERISTICS $V_{CC} = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time Output High to Low Output Low to High	t_{PHL} t_{PLH}	— —	— —	1.0 0.75	μs
Output Transition Time Output High to Low Output Low to High	t_{THL} t_{TLH}	— —	— —	0.1 0.1	μs

TEST CIRCUITS



SWITCHING TEST CIRCUIT AND WAVEFORM



MC1488

QUAD LINE DRIVER

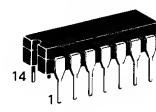
The MC1488 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. EIA-232D.

Features:

- Current Limited Output
 ± 10 mA typ
- Power-Off Source Impedance
300 Ohms min
- Simple Slew Rate Control with External Capacitor
- Flexible Operating Supply Range
- Compatible with All Motorola MDTL and MTTL Logic Families

QUAD MDTL LINE DRIVER EIA-232D

SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 632

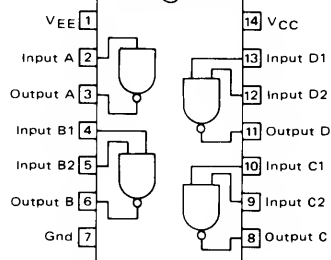


P SUFFIX
PLASTIC PACKAGE
CASE 646

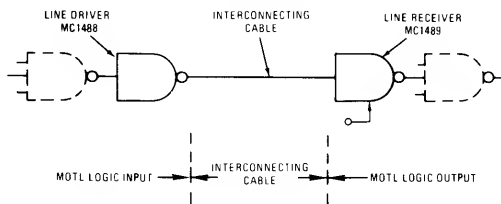
D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)



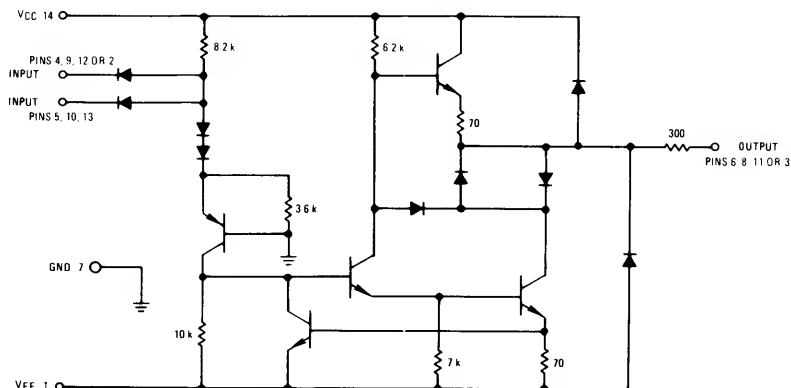
PIN CONNECTIONS



TYPICAL APPLICATION



CIRCUIT SCHEMATIC (1/4 OF CIRCUIT SHOWN)



MC1488

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+15 -15	Vdc
Input Voltage Range	V_{IR}	$-15 \leq V_{IR} \leq 7.0$	Vdc
Output Signal Voltage	V_O	± 15	Vdc
Power Derating (Package Limitation, Ceramic and Plastic Dual-In-Line Package) Derate above $T_A = +25^\circ\text{C}$	P_D $1/R_{\theta JA}$	1000 6.7	mW $\text{mW}/^\circ\text{C}$
Operating Ambient Temperature Range	T_A	0 to $+75$	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to $+175$	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($V_{CC} = +9.0 \pm 1\% \text{ Vdc}$, $V_{EE} = -9.0 \pm 1\% \text{ Vdc}$, $T_A = 0$ to 75°C unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Input Current — Low Logic State ($V_{IL} = 0$)	1	I_{IL}	—	1.0	1.6	mA
Input Current — High Logic State ($V_{IH} = 5.0 \text{ V}$)	1	I_{IH}	—	—	10	μA
Output Voltage — High Logic State ($V_{IL} = 0.8 \text{ Vdc}$, $R_L = 3.0 \text{ k}\Omega$, $V_{CC} = +9.0 \text{ Vdc}$, $V_{EE} = -9.0 \text{ Vdc}$) ($V_{IL} = 0.8 \text{ Vdc}$, $R_L = 3.0 \text{ k}\Omega$, $V_{CC} = +13.2 \text{ Vdc}$, $V_{EE} = -13.2 \text{ Vdc}$)	2	V_{OH}	+6.0 +9.0	+7.0 +10.5	— —	Vdc
Output Voltage — Low Logic State ($V_{IH} = 1.9 \text{ Vdc}$, $R_L = 3.0 \text{ k}\Omega$, $V_{CC} = +9.0 \text{ Vdc}$, $V_{EE} = -9.0 \text{ Vdc}$) ($V_{IH} = 1.9 \text{ Vdc}$, $R_L = 3.0 \text{ k}\Omega$, $V_{CC} = +13.2 \text{ Vdc}$, $V_{EE} = -13.2 \text{ Vdc}$)	2	V_{OL}	-6.0 -9.0	-7.0 -10.5	— —	Vdc
Positive Output Short-Circuit Current, Note 1	3	I_{OS+}	+6.0	+10	+12	mA
Negative Output Short-Circuit Current, Note 1	3	I_{OS-}	-6.0	-10	-12	mA
Output Resistance ($V_{CC} = V_{EE} = 0$, $ V_O = \pm 2.0 \text{ V}$)	4	r_o	300	—	—	Ohms
Positive Supply Current ($R_I = \infty$) ($V_{IH} = 1.9 \text{ Vdc}$, $V_{CC} = +9.0 \text{ Vdc}$) ($V_{IL} = 0.8 \text{ Vdc}$, $V_{CC} = +9.0 \text{ Vdc}$) ($V_{IH} = 1.9 \text{ Vdc}$, $V_{CC} = +12 \text{ Vdc}$) ($V_{IL} = 0.8 \text{ Vdc}$, $V_{CC} = +12 \text{ Vdc}$) ($V_{IH} = 1.9 \text{ Vdc}$, $V_{CC} = +15 \text{ Vdc}$) ($V_{IL} = 0.8 \text{ Vdc}$, $V_{CC} = +15 \text{ Vdc}$)	5	I_{CC}	— — — — — —	+15 +4.5 +19 +5.5 — —	+20 +6.0 +25 +7.0 +34 +12	mA
Negative Supply Current ($R_L = \infty$) ($V_{IH} = 1.9 \text{ Vdc}$, $V_{EE} = -9.0 \text{ Vdc}$) ($V_{IL} = 0.8 \text{ Vdc}$, $V_{EE} = -9.0 \text{ Vdc}$) ($V_{IH} = 1.9 \text{ Vdc}$, $V_{EE} = -12 \text{ Vdc}$) ($V_{IL} = 0.8 \text{ Vdc}$, $V_{EE} = -12 \text{ Vdc}$) ($V_{IH} = 1.9 \text{ Vdc}$, $V_{EE} = -15 \text{ Vdc}$) ($V_{IL} = 0.8 \text{ Vdc}$, $V_{EE} = -15 \text{ Vdc}$)	5	I_{EE}	— — — — — —	-13 — -18 — — —	-17 -500 -23 -500 -34 -2.5	mA μA mA μA mA mA
Power Consumption ($V_{CC} = 9.0 \text{ Vdc}$, $V_{EE} = -9.0 \text{ Vdc}$) ($V_{CC} = 12 \text{ Vdc}$, $V_{EE} = -12 \text{ Vdc}$)		P_C	— —	— —	333 576	mW

SWITCHING CHARACTERISTICS ($V_{CC} = +9.0 \pm 1\% \text{ Vdc}$, $V_{EE} = -9.0 \pm 1\% \text{ Vdc}$, $T_A = +25^\circ\text{C}$.)

Propagation Delay Time ($z_l = 3.0 \text{ k}$ and 15 pF)	6	t_{PLH}	—	275	350	ns
Fall Time ($z_l = 3.0 \text{ k}$ and 15 pF)	6	t_{THL}	—	45	75	ns
Propagation Delay Time ($z_l = 3.0 \text{ k}$ and 15 pF)	6	t_{PHL}	—	110	175	ns
Rise Time ($z_l = 3.0 \text{ k}$ and 15 pF)	6	t_{TLH}	—	55	100	ns

Note 1. Maximum Package Power Dissipation may be exceeded if all outputs are shorted simultaneously.

7

MC1488

CHARACTERISTIC DEFINITIONS

FIGURE 1 – INPUT CURRENT

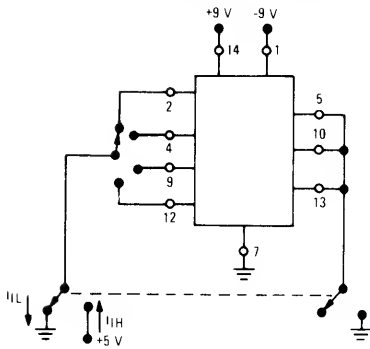


FIGURE 2 – OUTPUT VOLTAGE

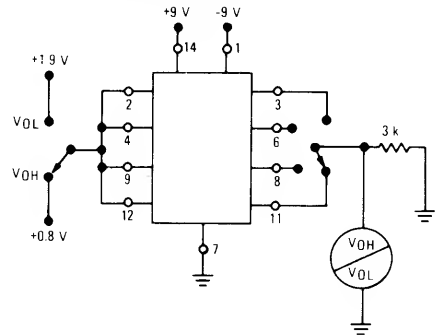


FIGURE 3 – OUTPUT SHORT-CIRCUIT CURRENT

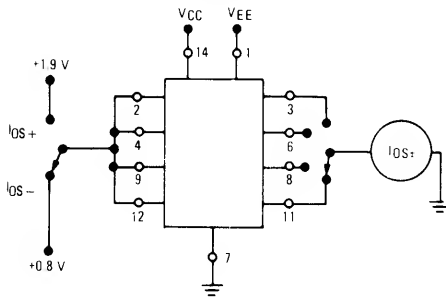


FIGURE 4 – OUTPUT RESISTANCE (POWER-OFF)

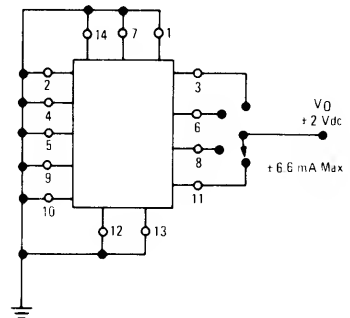


FIGURE 5 – POWER-SUPPLY CURRENTS

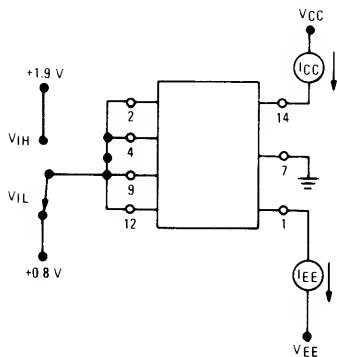
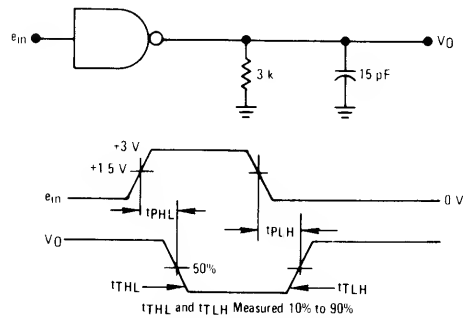


FIGURE 6 – SWITCHING RESPONSE

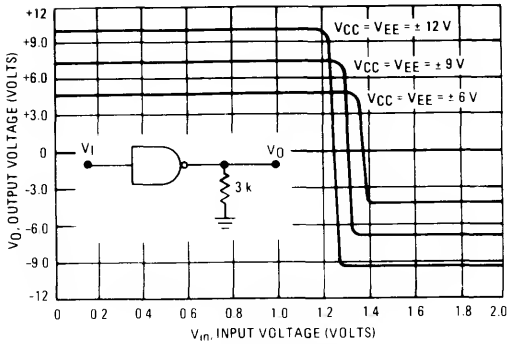


MC1488

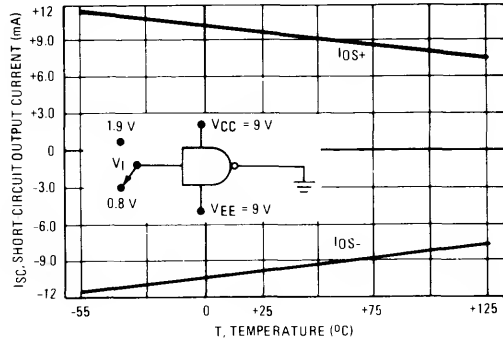
TYPICAL CHARACTERISTICS

($T_A = +25^\circ\text{C}$ unless otherwise noted.)

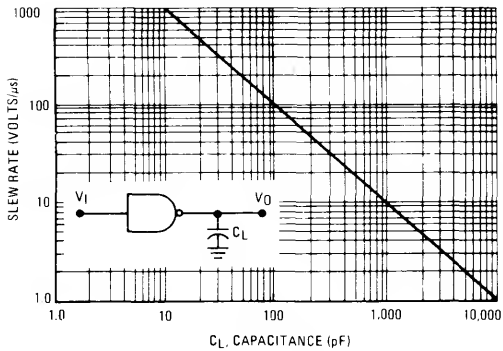
**FIGURE 7 — TRANSFER CHARACTERISTICS
versus POWER-SUPPLY VOLTAGE**



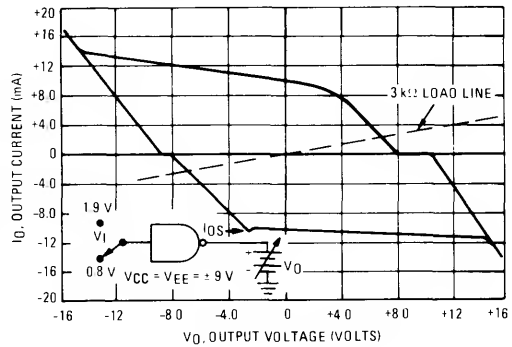
**FIGURE 8 — SHORT-CIRCUIT OUTPUT CURRENT
versus TEMPERATURE**



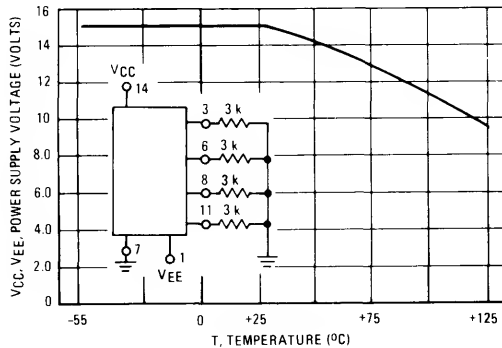
**FIGURE 9 — OUTPUT SLEW RATE
versus LOAD CAPACITANCE**



**FIGURE 10 — OUTPUT VOLTAGE
AND CURRENT-LIMITING CHARACTERISTICS**



**FIGURE 11 — MAXIMUM OPERATING TEMPERATURE
versus POWER-SUPPLY VOLTAGE**



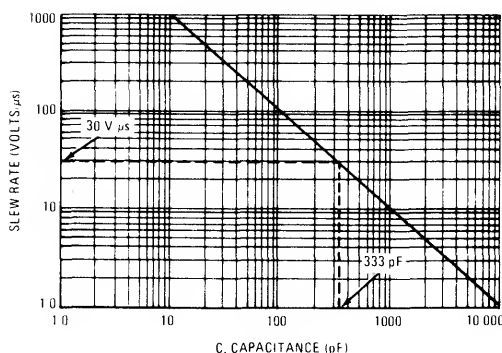
APPLICATIONS INFORMATION

The Electronic Industries Association EIA-232D specification detail the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the EIA-232D defined levels. The EIA-232D requirements as applied to drivers are discussed herein.

The required driver voltages are defined as between 5 and 15-volts in magnitude and are positive for a Logic "0" and negative for a Logic "1." These voltages are so defined when the drivers are terminated with a 3000 to 7000-ohm resistor. The MC1488 meets this voltage requirement by converting a DTL/TTL logic level into EIA-232D levels with one stage of inversion.

The EIA-232D specification further requires that during transitions, the driver output slew rate must not exceed 30 volts

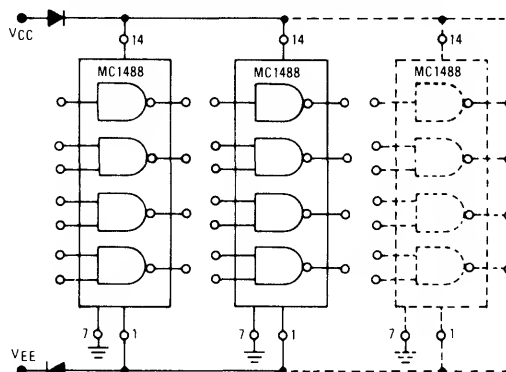
FIGURE 12 — SLEW RATE versus CAPACITANCE
FOR $I_{SC} = 10$ mA



per microsecond. The inherent slew rate of the MC1488 is much too fast for this requirement. The current limited output of the device can be used to control this slew rate by connecting a capacitor to each driver output. The required capacitor can be easily determined by using the relationship $C = I_{OS} \times \Delta T / \Delta V$ from which Figure 12 is derived. Accordingly, a 330 pF capacitor on each output will guarantee a worst case slew rate of 30 volts per microsecond.

The interface driver is also required to withstand an accidental short to any other conductor in an interconnecting cable. The worst possible signal on any conductor would be another driver using a plus or minus 15 volt, 500 mA source. The MC1488 is designed to indefinitely withstand such a short to all four outputs in a package as long as the power-supply voltages are greater than 9.0 volts (i.e., $V_{CC} \geq 9.0$ V; $V_{EE} \leq -9.0$ V). In some power-supply designs, a loss of system power causes a low impedance on the power-supply outputs. When this occurs, a low impedance to ground would exist at the power inputs to the MC1488 effectively shorting the 300 ohm output resistors to ground. If all four outputs were then shorted to plus or minus 15 volts, the power dissipation in these resistors

FIGURE 13 — POWER-SUPPLY PROTECTION
TO MEET POWER-OFF FAULT CONDITIONS



would be excessive. Therefore, if the system is designed to permit low impedances to ground at the power-supplies of the drivers, a diode should be placed in each power-supply lead to prevent overheating in this fault condition. These two diodes, as shown in Figure 13, could be used to decouple all the driver packages in a system. (These same diodes will allow the MC1488 to withstand momentary shorts to the ± 25 volt limits specified in the earlier Standard EIA-232B.) The addition of the diodes also permits the MC1488 to withstand faults with power-supplies of less than the 9.0 volts stated above.

The maximum short-circuit current allowable under fault conditions is more than guaranteed by the previously mentioned 10 mA output current limiting.

Other Applications

The MC1488 is an extremely versatile line driver with a myriad of possible applications. Several features of the drivers enhance this versatility:

1. Output Current Limiting — this enables the circuit designer to define the output voltage levels independent of power-supplies and can be accomplished by diode clamping of the output pins. Figure 14 shows the MC1488 used as a DTL to MOS translator where the high level voltage output is clamped one diode above ground. The resistor divider shown is used to reduce the output voltage below the 300 mV above ground MOS input level limit.

2. Power Supply Range — as can be seen from the schematic drawing of the drivers, the positive and negative driving elements of the device are essentially independent and do not require matching power-supplies. In fact, the positive supply can vary from a minimum seven volts (required for driving the negative pulldown section) to the maximum specified 15 volts. The negative supply can vary from approximately -2.5 volts to the minimum specified -15 volts. The MC1488 will drive the output to within 2 volts of the positive or negative supplies as long as the current output limits are not exceeded. The combination of the current-limiting and supply-voltage features allow a wide combination of possible outputs within the same quad package. Thus if only a portion of the four drivers are used for driving EIA-232D lines, the remainder could be used for DTL to MOS or even DTL to DTL translation. Figure 15 shows one such combination.

MC1488

FIGURE 14 - MDTL/MTTL-TO-MOS TRANSLATOR

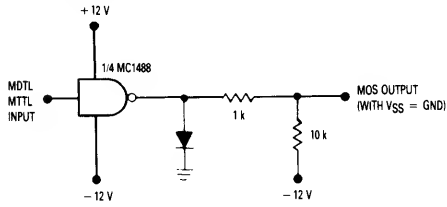
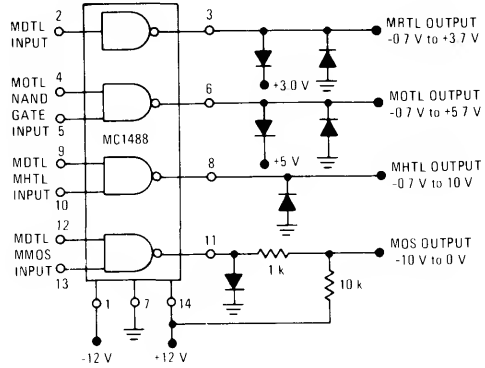


FIGURE 15 - LOGIC TRANSLATOR APPLICATIONS



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

MC1489 MC1489A

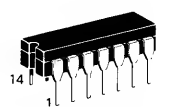
QUAD LINE RECEIVERS

The MC1489 monolithic quad line receivers are designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. EIA-232D.

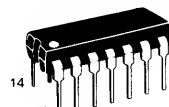
- Input Resistance — 3.0 k to 7.0 kilohms
- Input Signal Range — ± 30 Volts
- Input Threshold Hysteresis Built In
- Response Control
 - a) Logic Threshold Shifting
 - b) Input Noise Filtering

QUAD MDTL LINE RECEIVERS EIA-232D

SILICON MONOLITHIC
INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 632

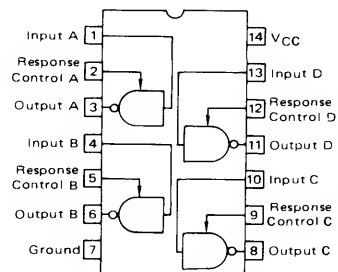
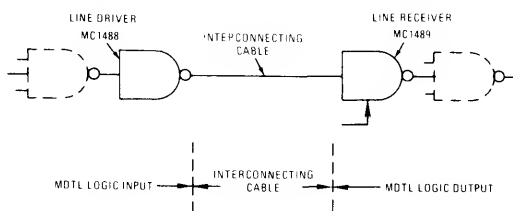


P SUFFIX
PLASTIC PACKAGE
CASE 646

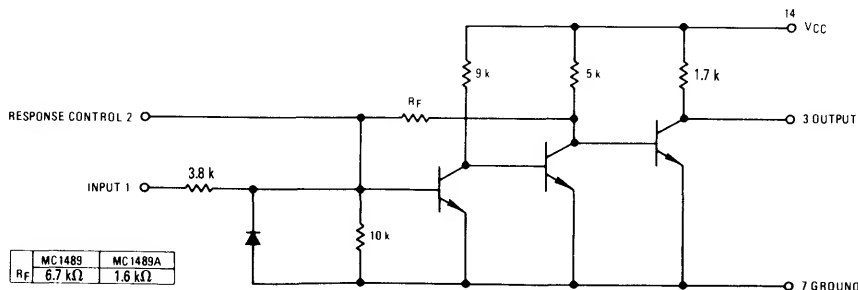
D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)



TYPICAL APPLICATION



EQUIVALENT CIRCUIT SCHEMATIC (1/4 OF CIRCUIT SHOWN)



MC1489, MC1489A

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	10	Vdc
Input Voltage Range	V_{IR}	± 30	Vdc
Output Load Current	I_L	20	mA
Power Dissipation (Package Limitation, Ceramic and Plastic Dual In-Line Package) Derate above $T_A = +25^\circ\text{C}$	P_D $1/\theta_{JA}$	1000 6.7	mW mW/ $^\circ\text{C}$
Operating Ambient Temperature Range	T_A	0 to $+75$	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to $+175$	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS (Response control pin is open.) ($V_{CC} = +5.0\text{ Vdc} \pm 10\%$, $T_A = 0$ to $+75^\circ\text{C}$ unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
Positive Input Current ($V_{IH} = +25\text{ Vdc}$) ($V_{IH} = +3.0\text{ Vdc}$)	I_{IH}	3.6 0.43	—	8.3 —	mA
Negative Input Current ($V_{IL} = -25\text{ Vdc}$) ($V_{IL} = -3.0\text{ Vdc}$)	I_{IL}	-3.6 -0.43	—	-8.3 —	mA
Input Turn-On Threshold Voltage ($T_A = +25^\circ\text{C}$, $V_{OL} \leq 0.45\text{ V}$)	V_{IH}	1.0 1.75	— 1.95	1.5 2.25	Vdc
Input Turn-Off Threshold Voltage ($T_A = +25^\circ\text{C}$, $V_{OH} \geq 2.5\text{ V}$, $I_L = -0.5\text{ mA}$)	V_{IL}	0.75 0.75	— 0.8	1.25 1.25	Vdc
Output Voltage High ($V_{IH} = 0.75\text{ V}$, $I_L = -0.5\text{ mA}$) (Input Open Circuit, $I_L = -0.5\text{ mA}$)	V_{OH}	2.5 2.5	4.0 4.0	5.0 5.0	Vdc
Output Voltage Low ($V_{IL} = 3.0\text{ V}$, $I_L = 10\text{ mA}$)	V_{OL}	—	0.2	0.45	Vdc
Output Short-Circuit Current	I_{OS}	—	-3.0	-4.0	mA
Power Supply Current (All Gates "on," $I_{out} = 0\text{ mA}$, $V_{IH} = +5.0\text{ Vdc}$)	I_{CC}	—	16	26	mA
Power Consumption ($V_{IH} = +5.0\text{ Vdc}$)	P_C	—	80	130	mW

SWITCHING CHARACTERISTICS ($V_{CC} = 5.0\text{ Vdc} \pm 1\%$, $T_A = +25^\circ\text{C}$, See Figure 1.)

Propagation Delay Time ($R_L = 3.9\text{ k}\Omega$)	t_{PLH}	—	25	85	ns
Rise Time ($R_L = 3.9\text{ k}\Omega$)	t_{TLH}	—	120	175	ns
Propagation Delay Time ($R_L = 390\text{ k}\Omega$)	t_{PHL}	—	25	50	ns
Fall Time ($R_L = 390\text{ k}\Omega$)	t_{THL}	—	10	20	ns

TEST CIRCUITS

FIGURE 1 — SWITCHING RESPONSE

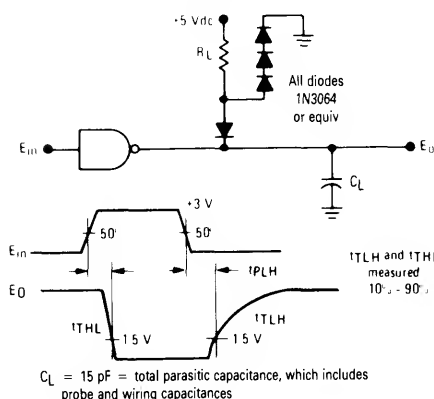
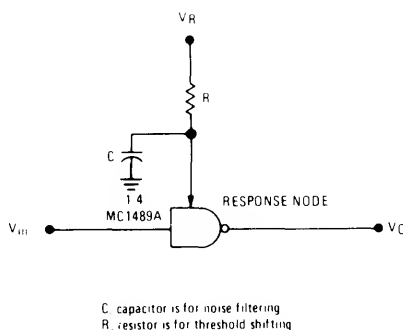


FIGURE 2 — RESPONSE CONTROL NODE



MC1489, MC1489A

TYPICAL CHARACTERISTICS

($V_{CC} = 5.0$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted)

FIGURE 3 — INPUT CURRENT

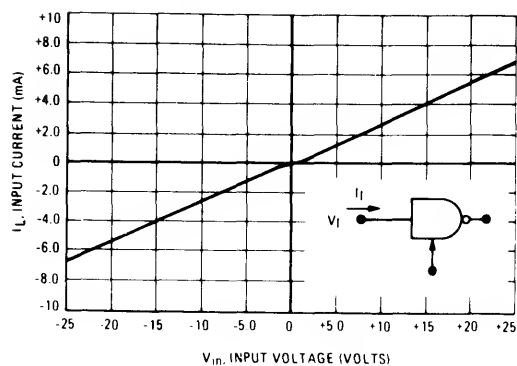


FIGURE 4 — MC1489 INPUT THRESHOLD VOLTAGE ADJUSTMENT

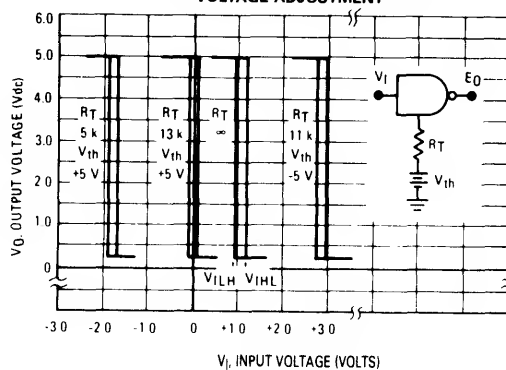


FIGURE 5 — MC1489A INPUT THRESHOLD VOLTAGE ADJUSTMENT

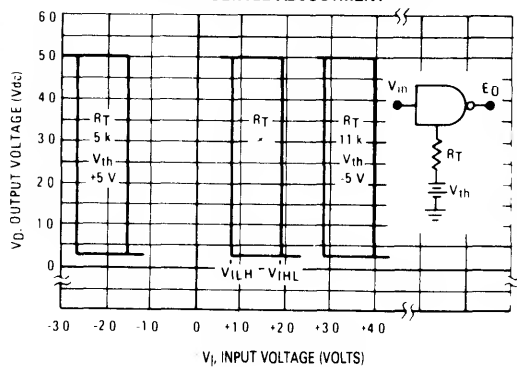


FIGURE 6 — INPUT THRESHOLD VOLTAGE versus TEMPERATURE

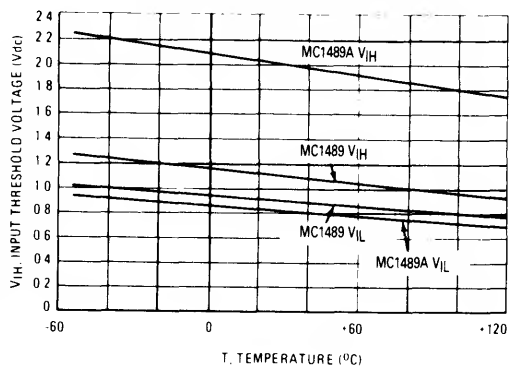
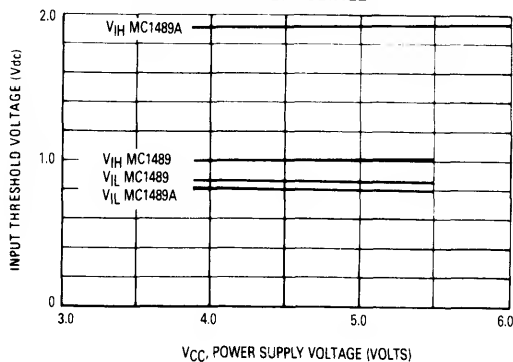


FIGURE 7 — INPUT THRESHOLD versus POWER-SUPPLY VOLTAGE



MC1489, MC1489A

APPLICATIONS INFORMATION

General Information

The Electronic Industries Association (EIA) has released the EIA-232D specification detailing the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the EIA-232D defined levels. The EIA-232D requirements as applied to receivers are discussed herein.

The required input impedance is defined as between 3000 ohms and 7000 ohms for input voltages between 3.0 and 25 volts in magnitude; and any voltage on the receiver input in an open circuit condition must be less than 2.0 volts in magnitude. The MC1489 circuits meet these requirements with a maximum open circuit voltage of one V_{BE} .

The receiver shall detect a voltage between -3.0 and -25 volts as a Logic "1" and inputs between $+3.0$ and $+25$ volts as a Logic "0." On some interchange leads, an open circuit of power "OFF" condition (300 ohms or more to ground) shall be decoded as an "OFF" condition or Logic "1." For this reason, the input hysteresis thresholds of the MC1489 circuits are all above ground. Thus an open or grounded input will cause the same output as a negative or Logic "1" input.

Device Characteristics

The MC1489 interface receivers have internal feedback from the second stage to the input stage providing input

hysteresis for noise rejection. The MC1489 input has typical turn-on voltage of 1.25 volts and turn-off of 1.0 volt for a typical hysteresis of 250 mV. The MC1489A has typical turn-on of 1.95 volts and turn-off of 0.8 volt for typically 1.15 volts of hysteresis.

Each receiver section has an external response control node in addition to the input and output pins, thereby allowing the designer to vary the input threshold voltage levels. A resistor can be connected between this node and an external power supply. Figures 2, 4 and 5 illustrate the input threshold voltage shift possible through this technique.

This response node can also be used for the filtering of high-frequency, high energy noise pulses. Figures 8 and 9 show typical noise-pulse rejection for external capacitors of various sizes.

These two operations on the response node can be combined or used individually for many combinations of interfacing applications. The MC1489 circuits are particularly useful for interfacing between MOS circuits and MDTL/MTTL logic systems. In this application, the input threshold voltages are adjusted (with the appropriate supply and resistor values) to fall in the center of the MOS voltage logic levels. (See Figure 10)

The response node may also be used as the receiver input as long as the designer realizes that he may not drive this node with a low impedance source to a voltage greater than one diode above ground or less than one diode below ground. This feature is demonstrated in Figure 11 where two receivers are slaved to the same line that must still meet the EIA-232D impedance requirement.

FIGURE 8 — TYPICAL TURN-ON THRESHOLD versus CAPACITANCE FROM RESPONSE CONTROL PIN TO GND

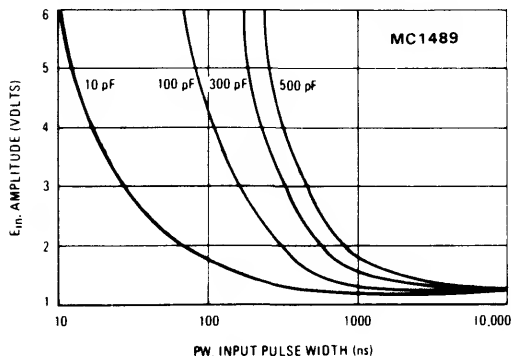
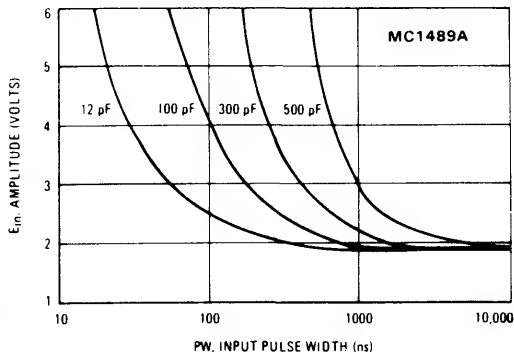


FIGURE 9 — TYPICAL TURN-ON THRESHOLD versus CAPACITANCE FROM RESPONSE CONTROL PIN TO GND



MC1489, MC1489A

FIGURE 10 — TYPICAL TRANSLATOR APPLICATION —
MOS TO DTL OR TTL

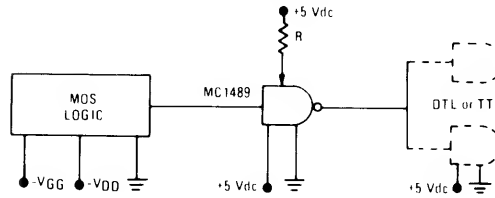
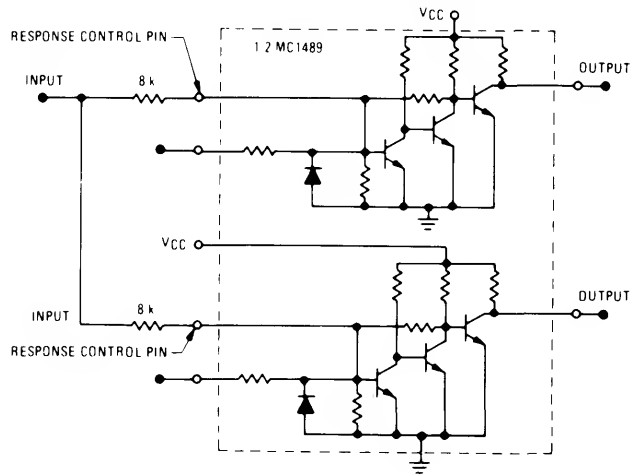


FIGURE 11 — TYPICAL PARALLELING OF TWO MC1489,A RECEIVERS TO MEET EIA-232D



QUAD OPEN-COLLECTOR BUS TRANSCEIVER

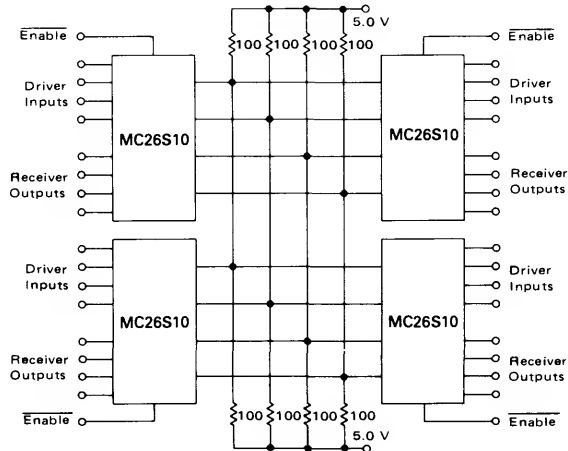
This quad transceiver is designed to mate Schottky TTL or NMOS logic to a low impedance bus. The Enable and Driver inputs are PNP buffered to ensure low input loading. The Driver (Bus) output is open-collector and can sink up to 100 mA at 0.8 V, thus the bus can drive impedances as low as 100 Ω . The receiver output is active pull-up and can drive ten Schottky TTL loads.

An active-low Enable controls all four drivers allowing the outputs of different device drivers to be connected together for party-line operation. The line can be terminated at both ends and still give considerable noise margin at the receiver. Typical receiver threshold is 2.0 V.

Advanced Schottky processing is utilized to assure fast propagation delay times. Two ground pins are provided to improve ground current handling and allow close decoupling between V_{CC} and ground at the package. Both ground pins should be tied to the ground bus external to the package.

- Driver Can Sink 100 mA at 0.8 V (Max)
- PNP Inputs for Low-Logic Loading
- Typical Driver Delay = 10 ns
- Typical Receiver Delay = 10 ns
- Schottky Processing for High Speed
- Inverting Driver

TYPICAL APPLICATION

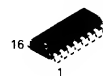


MC26S10

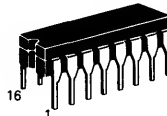
QUAD OPEN-COLLECTOR BUS TRANSCEIVER

**SCHOTTKY
SILICON MONOLITHIC
INTEGRATED CIRCUIT**

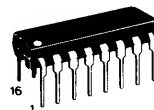
D SUFFIX
 PLASTIC PACKAGE
 CASE 751B
 (SO-16)



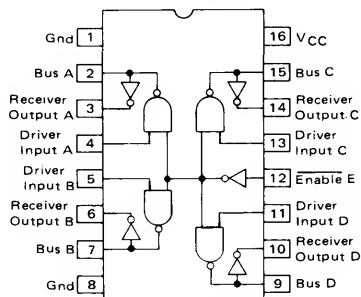
L SUFFIX
 CERAMIC PACKAGE
 CASE 620



P SUFFIX
 PLASTIC PACKAGE
 CASE 648



PIN CONNECTIONS



TRUTH TABLE

Enable	Driver Input	Bus	Receiver Output
L	L	H	L
L	H	L	H
H	X	Y	Y

L = Low Logic State
 H = High Logic State
 X = Irrelevant
 Y = Assumes condition controlled by other elements on the bus

MC26S10

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V _{CC}	-0.5 to +7.0	V _{dc}
Input Voltage	V _I	-0.5 to +5.5	V _{dc}
Input Current	I _I	-3.0 to +5.0	mA
Output Voltage — High Impedance State	V _O (Hi-Z)	-0.5 to V _{CC}	V
Output Current—Bus	I _O (B)	200	mA
Output Current—Receiver	I _O (R)	30	mA
Operating Ambient Temperature	T _A	0 to +70	°C
Storage Temperature	T _{stg}	-65 to +150	°C
Junction Temperature	T _J		°C
Ceramic Package		175	
Plastic Package		150	

ELECTRICAL CHARACTERISTICS (Unless otherwise noted V_{CC} = 4.75 to 5.25 V and T_A = 0 to +70°C. Typical values measured at V_{CC} = 5.0 V and T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage — Low Logic State (Driver and Enable Inputs)	V _{IL}	—	—	0.8	V
Input Voltage — High Logic State (Driver and Enable Inputs)	V _{IH}	2.0	—	—	V
Input Clamp Voltage (Driver and Enable Inputs) (I _{IK} = -1B mA)	V _{IK}	—	—	-1.2	V
Input Current — Low Logic State (V _{IL} = 0.4 V) (Enable Input) (Driver Inputs)	I _{IL}	—	—	-0.36 -0.54	mA
Input Current — High Logic State (V _{IH} = 2.7 V) (Enable Input) (Driver Inputs)	I _{IH}	—	—	20 30	μA
Input Current — Maximum Voltage (V _{IH1} = 5.5 V) (Enable or Driver Inputs)	I _{IH1}	—	—	100	μA
Driver Output Voltage — Low Logic State (I _{OL} = 40 mA) (I _{OL} = 70 mA) (I _{OL} = 100 mA)	V _{OL} (D)	—	0.33 0.42 0.51	0.5 0.7 0.8	V
Driver (Bus) Leakage Current (V _{OH} = 4.5 V) (V _{OL} = 0.8 V)	I _O (D)	—	—	100 -50	μA
Driver (Bus) Leakage Current (V _{CC} = 0 V, V _{OH} = 4.5 V)	I _{O1} (D)	—	—	100	μA
Receiver Input High Threshold (V _{IH} (E) = 2.4 V)	V _{TH} (R)	2.25	2.0	—	V
Receiver Input Low Threshold (V _{IH} (E) = 2.4 V)	V _{TL} (R)	—	2.0	1.75	V
Receiver Output Voltage — Low Logic State (I _{OL} = 20 mA)	V _{OL} (R)	—	—	0.5	V
Receiver Output Voltage — High Logic State (I _{OH} = -1.0 mA)	V _{OH} (R)	2.7	3.4	—	V
Receiver Output Short-Circuit Current (Note 1)	I _{OS} (R)	-1B	—	-60	mA
Power Supply Current — Output Low State (V _{IL} (E) = 0 V)	I _{CC}	—	45	70	mA

NOTE 1: One output shorted at a time. Duration not to exceed 1.0 second.

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time Driver Input to Output	t _{PLH} (D) t _{PHL} (D)	— —	10 10	15 15	ns
Propagation Delay Time Enable Input to Output	t _{PLH} (E) t _{PHL} (E)	— —	14 13	18 18	ns
Propagation Delay Time Bus to Receiver Output	t _{PLH} (R) t _{PHL} (R)	— —	10 10	15 15	ns
Rise and Fall Time of Driver Output	t _{TLH} (D) t _{THL} (D)	4.0 2.0	10 4.0	— —	ns

SWITCHING WAVEFORMS AND CIRCUITS

FIGURE 1 — DATA INPUT TO BUS OUTPUT (DRIVER)

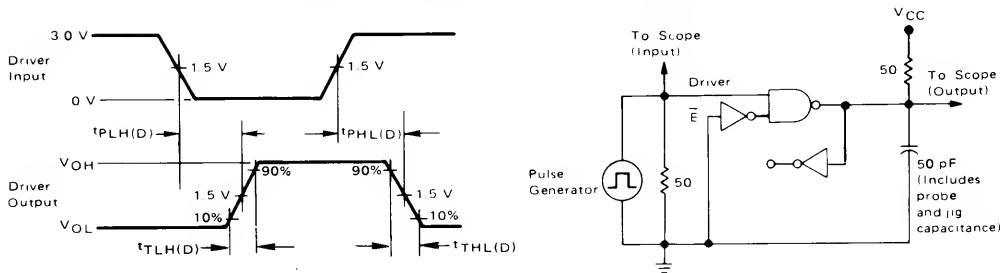


FIGURE 2 — ENABLE INPUT TO BUS OUTPUT (DRIVER)

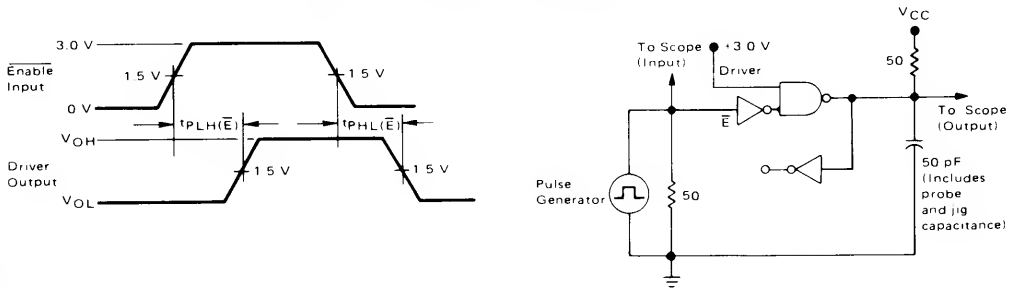
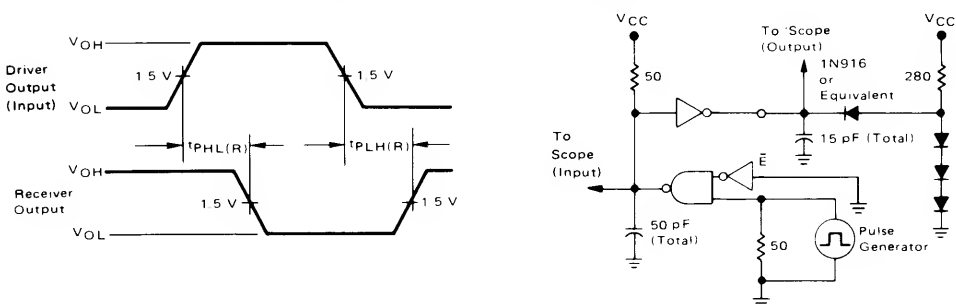


FIGURE 3 — BUS INPUT TO RECEIVER OUTPUT



MC3437

HEX BUS RECEIVER WITH INPUT HYSTERESIS

These high-speed bus receivers are useful in bus organized data transmission systems employing terminated 120 Ω lines. The receivers feature input hysteresis to obtain improved noise immunity. The receivers low input current requirement allows up to 27 driver/receiver pairs to share a common bus. A pair of Disable Inputs are provided. These Disable Inputs along with the receiver outputs are MTTL compatible.

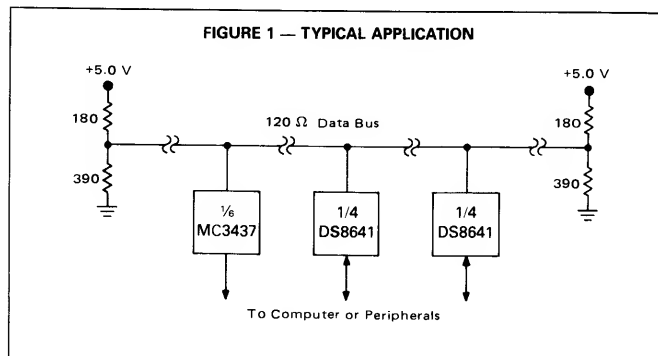
- Built in receiver hysteresis
- Receiver input threshold is not affected by temperature
- Propagation delay time - 20 ns (Typ)
- Direct Replacement for DM8837

7

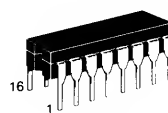
MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted.)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	7.0	Vdc
Input Voltage	V_I	5.5	Vdc
Power Dissipation Derate above 25°C	P_D	625 3.85	mW mW/ $^\circ\text{C}$
Operating Ambient Temperature Range	T_A	0 to 70	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

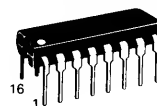
FIGURE 1 — TYPICAL APPLICATION



HEX BUS RECEIVER SILICON MONOLITHIC INTEGRATED CIRCUIT

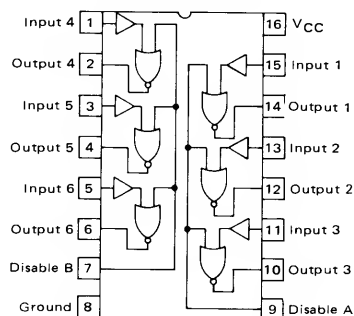


L SUFFIX
 CERAMIC PACKAGE
 CASE 620



P SUFFIX
 PLASTIC PACKAGE
 CASE 648

PIN CONNECTIONS



TRUTH TABLE

Input	Disable	Output
O	L	H
O	H	L
I	L	L
I	H	L

O = $< 1.6\text{V}$
 I = $> 2.5\text{V}$
 H = High Logic State
 L = Low Logic State

MC3437

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, specifications apply for $0 \leq T_A \leq 70^\circ\text{C}$ and $4.75 \text{ V} \leq V_{CC} \leq 5.25 \text{ V}$.)

Characteristic	Symbol	Min	Typ	Max	Unit
Receiver Input Threshold Voltage — High Logic State ($V_{IL}(\text{DA}) = 0.8 \text{ V}$, $I_{OL} = 16 \text{ mA}$, $V_{OL} \leq 0.4 \text{ V}$)	$V_{ILH}(\text{R})$	1.80	2.25	2.50	V
Receiver Input Threshold Voltage — Low Logic State ($V_{IL}(\text{DA}) = 0.8 \text{ V}$, $I_{OH} = -400 \mu\text{A}$, $V_{OH} \geq 2.4 \text{ V}$)	$V_{IHL}(\text{R})$	1.05	1.30	1.55	V
Receiver Input Current ($V_{I}(\text{R}) = 4.0 \text{ V}$, $V_{CC} = 5.25 \text{ V}$) ($V_{I}(\text{R}) = 4.0 \text{ V}$, $V_{CC} = 0 \text{ V}$)	$I_{I}(\text{R})$	— —	15 1.0	50 50	μA
Disable Input Voltage — High Logic State ($V_{I}(\text{R}) = 0.5 \text{ V}$, $V_{OL} \leq 0.4 \text{ V}$, $I_{OL} = 16 \text{ mA}$)	$V_{IH}(\text{DA})$	2.0	—	—	V
Disable Input Voltage — Low Logic State ($V_{I}(\text{R}) = 0.5 \text{ V}$, $V_{OH} \geq 2.4 \text{ V}$, $I_{OH} = -400 \mu\text{A}$)	$V_{IL}(\text{DA})$	—	—	0.8	V
Output Voltage — High Logic State ($V_{I}(\text{R}) = 0.5 \text{ V}$, $V_{IL}(\text{DA}) = 0.8 \text{ V}$, $I_{OH} = -400 \mu\text{A}$)	V_{OH}	2.4	—	—	V
Output Voltage — Low Logic State ($V_{I}(\text{R}) = 4.0 \text{ V}$, $V_{IL}(\text{DA}) = 0.8 \text{ V}$, $I_{OL} = 16 \text{ mA}$)	V_{OL}	—	0.25	0.4	V
Disable Input Current — High Logic State ($V_{IH}(\text{DA}) = 2.4 \text{ V}$) ($V_{IH}(\text{DA}) = 5.5 \text{ V}$)	$I_{IH}(\text{DA})$	— —	— —	80 2.0	μA mA
Disable Input Current — Low Logic State ($V_{I}(\text{R}) = 4.0 \text{ V}$, $V_{IL}(\text{DA}) = 0.4 \text{ V}$)	$I_{IL}(\text{DA})$	—	—	-3.2	mA
Output Short Circuit Current ($V_{I}(\text{R}) = 0.5 \text{ V}$, $V_{IL}(\text{DA}) = 0 \text{ V}$, $V_{CC} = 5.25 \text{ V}$)	I_{OS}	-18	—	-55	mA
Power Supply Current ($V_{I}(\text{R}) = 0.5 \text{ V}$, $V_{IL}(\text{DA}) = 0 \text{ V}$)	I_{CC}	—	45	65	mA
Input Clamp Diode Voltage ($I_{I}(\text{R}) = -12 \text{ mA}$, $I_{I}(\text{DA}) = -12 \text{ mA}$,	V_I	—	-1.0	-1.5	V

SWITCHING CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0 \text{ V}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time from Receiver Input to High Logic State Output	$t_{PLH}(\text{R})$	—	20	30	ns
Propagation Delay Time from Receiver Input to Low Logic State Output	$t_{PHL}(\text{R})$	—	18	30	ns
Propagation Delay Time from Disable Input to High Logic State Output	$t_{PLH}(\text{DA})$	—	9.0	15	ns
Propagation Delay Time from Disable Input to Low Logic State Output	$t_{PHL}(\text{DA})$	—	4.0	15	ns

MC3437

FIGURE 2 — SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS

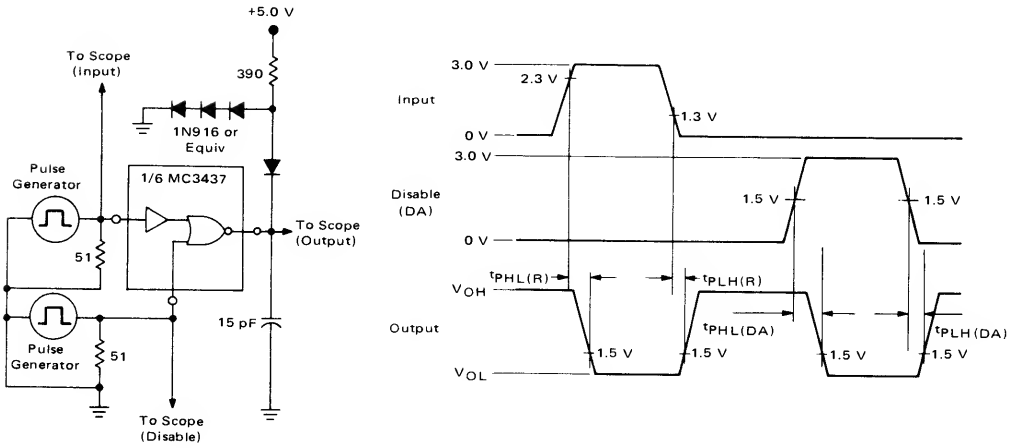


FIGURE 3 — TYPICAL HYSTERESIS

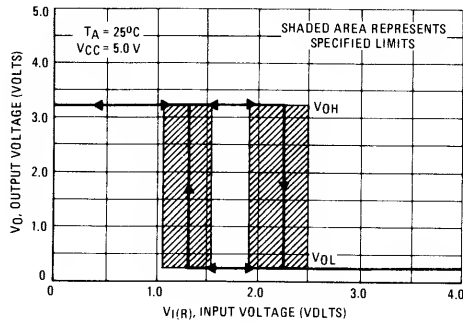
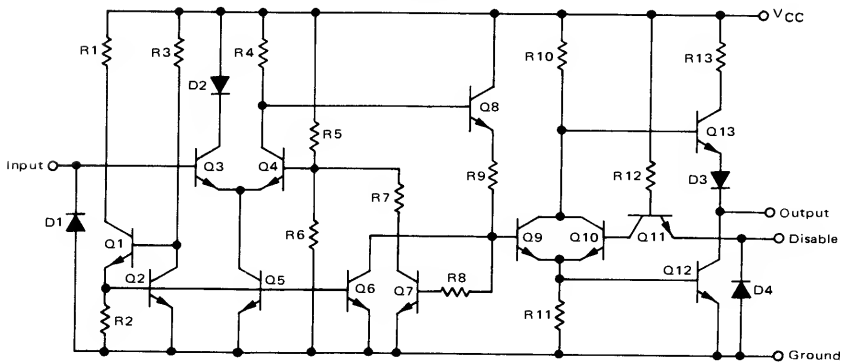


FIGURE 4 — REPRESENTATIVE CIRCUIT SCHEMATIC
(1/6 Shown)



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

QUAD GENERAL-PURPOSE INTERFACE BUS (GPIB) TRANSCEIVERS

The MC3440A, MC3441A are quad bus transceivers intended for usage in instruments and programmable calculators equipped for interconnection into complete measurement systems. These transceivers allow the bidirectional flow of digital data and commands between the various instruments. Each of the transceiver versions provides four open-collector drivers and four receivers featuring input hysteresis.

The MC3440A version consists of three drivers controlled by a common Enable input and a single driver without an Enable input. Terminations are provided in the device.

The MC3441A differs in that all four drivers are controlled by the common Enable input. Again, the terminations are provided.

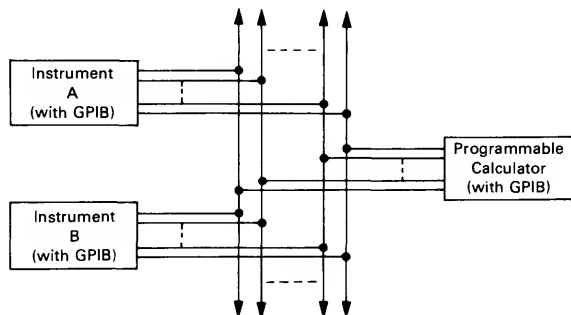
- Receiver Input Hysteresis Provides Excellent Noise Rejection
- Open-Collector Driver Outputs Permit Wire-OR Connection
- Tailored to Meet the Standards Set by the IEEE and IEC Committees on Instrument Interface (488-1978)
- Terminations comply with IEEE 488-1978; terminations removed when device is unpowered
- Provides Electrical Compatibility with General-Purpose Interface Bus

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted.) (Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Input Voltage	V_I	5.5	Vdc
Driver Output Current	$I_{O(D)}$	150	mA
Power Dissipation (Package Limitation) Derate above 25°C	P_D	830 6.7	mW mW/ $^\circ\text{C}$
Operating Ambient Temperature Range	T_A	0 to $+70$	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to $+150$	$^\circ\text{C}$

Note 1: Devices should not be operated at these values. The "Electrical Characteristics" provide conditions for actual device operation.

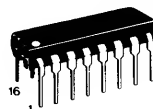
TYPICAL APPLICATION — GPIB MEASUREMENT SYSTEM



MC3440A MC3441A

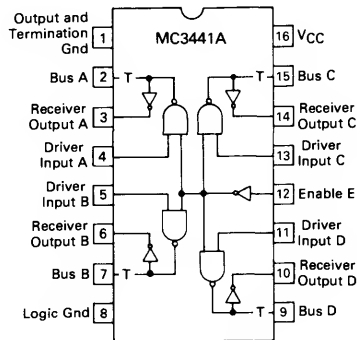
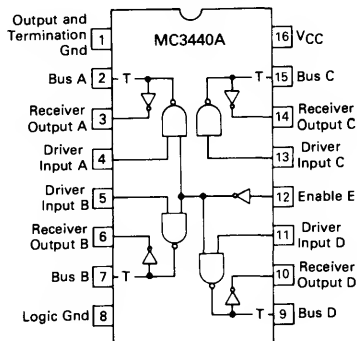
QUAD INTERFACE BUS TRANSCEIVERS

SILICON MONOLITHIC INTEGRATED CIRCUITS

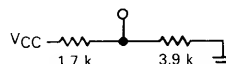


P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS



— T — = Bus Termination



MC3440A, MC3441A

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ and $0 \leq T_A \leq 70^\circ\text{C}$, typical values are at $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$)

Characteristic	Symbol	Min	Typ	Max	Unit
DRIVER PORTION					
Input Voltage — High Logic State	$V_{IH(D)}$	2.0	—	—	V
Input Voltage — Low Logic State	$V_{IL(D)}$	—	—	0.8	V
Input Current — High Logic State ($V_{IH} = 2.4\text{ V}$)	$I_{IH(D)}$	—	—	40	μA
Input Current — Low Logic State ($V_{IL} = 0.4\text{ V}$, $V_{CC} = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$)	$I_{IL(D)}$	—	—	-0.25	mA
Input Clamp Voltage ($I_{IK} = -12\text{ mA}$)	$V_{IK(D)}$	—	—	-1.5	V
Output Voltage — High Logic State ($V_{IH(S)} = 2.4\text{ V}$ or $V_{IL(D)} = 0.8\text{ V}$)	$V_{OH(D)}$	2.5	—	—	V
Output Voltage — Low Logic State ($V_{IH(S)} = 2.0\text{ V}$, $V_{IL(E)} = 0.8\text{ V}$, $I_{OL(D)} = 48\text{ mA}$) ($V_{IH(D)} = 2.0\text{ V}$, $V_{IL(E)} = 0.8\text{ V}$, $I_{OL(D)} = 100\text{ mA}$)	$V_{OL(D)}$	—	—	0.5 0.80	V

RECEIVER PORTION					
Input Hysteresis	—	400	580	—	mV
Input Threshold Voltage — Low to High Output Logic State ($V_{CC} = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$)	$V_{ILH(R)}$	0.8	0.98	—	V
Input Threshold Voltage — High to Low Output Logic State ($V_{CC} = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$)	$V_{IHL(R)}$	—	1.56	2.0	V
Output Voltage — High Logic State ($V_{IL(R)} = 0.8\text{ V}$, $I_{OH(R)} = -400\text{ }\mu\text{A}$)	$V_{OH(R)}$	2.4	—	—	V
Output Voltage — Low Logic State ($V_{IH(R)} = 2.0\text{ V}$, $I_{OL(R)} = 16\text{ mA}$)	$V_{OL(R)}$	—	—	0.5	V
Output Short-Circuit Current ($V_{IL(R)} = 0.8\text{ V}$) (Only one output may be shorted at a time)	$I_{OS(R)}$	-20	—	-55	mA

BUS TERMINATION PORTION

Bus Voltage ($V_{IL(D)} = 0.8\text{ V}$) ($I_{BUS} = -12\text{ mA}$) (No Load)	V_{BUS}	— 2.50	— —	-1.5 3.70	V
Bus Current ($V_{IL(D)} = 0.8\text{ V}$, $V_{BUS} \geq 5.0\text{ V}$) ($V_{IL(D)} = 0.8\text{ V}$, $V_{BUS} \leq 5.5\text{ V}$) ($V_{IL(D)} = 0.8\text{ V}$, $V_{BUS} = 0.5\text{ V}$) ($V_{CC} = 0, 0 \leq V_{BUS} \leq 2.75\text{ V}$)	I_{BUS}	0.7 — -1.3 —	— — — —	— 2.5 -3.2 +0.04	mA

TOTAL DEVICE POWER CONSUMPTION

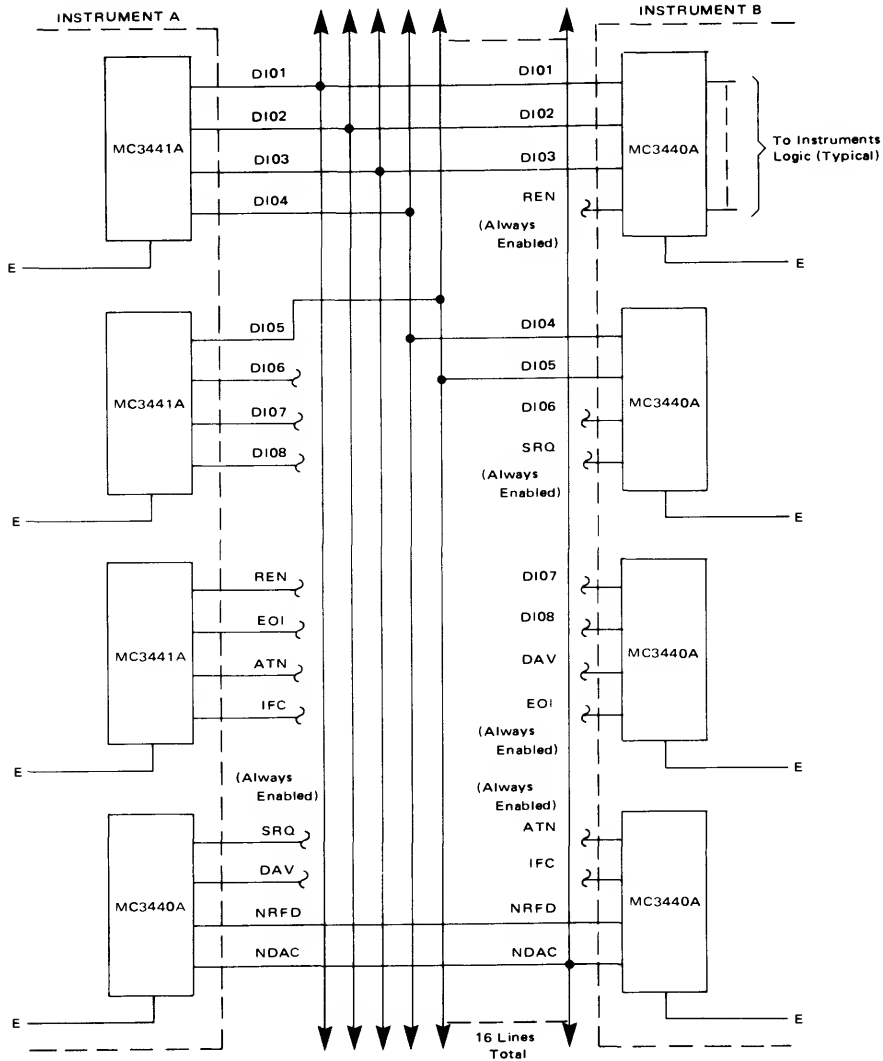
Power Supply Current ($V_{IH(D)} = 2.4\text{ V}$, $V_{IL(E)} = 0\text{ V}$)	I_{CC}	30	56	75	mA
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SWITCHING CHARACTERISTICS ($V_{CC} = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	Min	Typ	Max	Unit
DRIVER PORTION					
Propagation Delay Time from Driver Input to Low Logic State Bus Output	$t_{PHL(D)}$	—	13	30	ns
Propagation Delay Time from Driver Input to High Logic State Bus Output	$t_{PLH(D)}$	—	17	30	ns
Propagation Delay Time from Enable Input to Low Logic State Bus Output	$t_{PHL(E)}$	—	25	40	ns
Propagation Delay Time from Enable Input to High Logic State Bus Output	$t_{PLH(E)}$	—	25	40	ns
RECEIVER PORTION					
Propagation Delay Time from Bus Input to High Logic State Receiver Output	$t_{PLH(R)}$	—	15	30	ns
Propagation Delay Time from Bus Input to Low Logic State Receiver Output	$t_{PHL(R)}$	—	15	30	ns

MC3440A, MC3441A

GENERAL PURPOSE INTERFACE BUS APPLICATION



GPIB SIGNALS:

8 Line Data Bus: DI01 – DI08

5 General Interrupt Transfer Control Bus:

REN – Remote Enable
SRQ – Service Request
EOI – End or Identify
ATN – Attention
IFC – Interface Clear

3 Data Byte Transfer Control Bus

DAV – Data Valid
NRFD – Not Ready for Data
NDAC – Not Data Accepted

16 Total Signal Lines

MC3440A, MC3441A

FIGURE 1 — TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM RECEIVER INPUT (BUS) TO OUTPUT

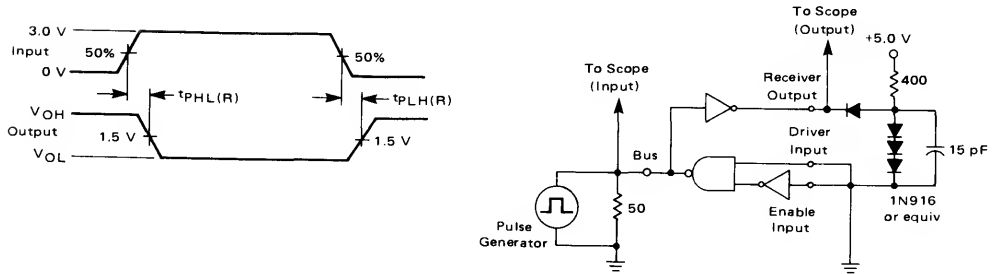


FIGURE 2 — TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM DRIVER AND COMMON ENABLE INPUTS TO OUTPUT (BUS)

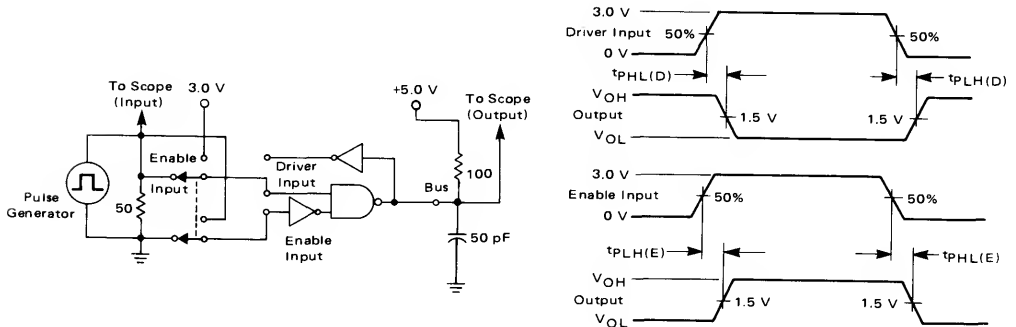
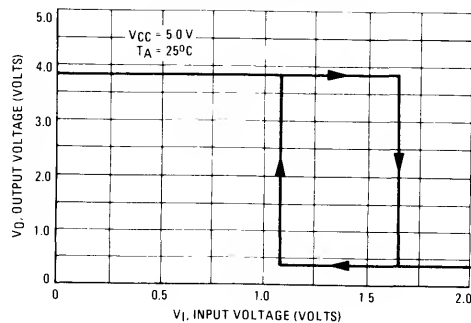


FIGURE 3 — TYPICAL RECEIVER HYSTERESIS CHARACTERISTICS



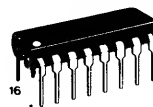
**QUAD GENERAL-PURPOSE INTERFACE
 BUS (GPIB) TRANSCEIVER**

The MC3446A is a quad bus transceiver intended for usage in instruments and programmable calculators equipped for interconnection into complete measurement systems. This transceiver allows the bidirectional flow of digital data and commands between the various instruments. The transceiver provides four open-collector drivers and four receivers featuring hysteresis.

- Tailored to Meet the IEEE Standard 488-1978 (Digital Interface for Programmable Instrumentation) and the Proposed IEC
- Provides Electrical Compatibility with General-Purpose Interface Bus (GPIB)
- MOS Compatible with High Impedance Inputs
- Driver Output Guaranteed Off During Power Up/Power Down
- Low Power — Average Power Supply Current = 12 mA
- Terminations Provided: Terminations Removed When Device is Unpowered

MC3446A

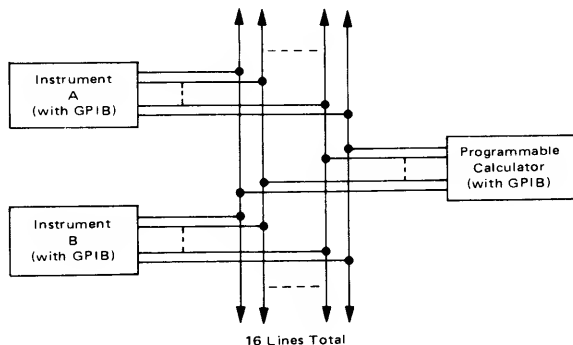
**QUAD INTERFACE
 BUS TRANSCEIVER
 SILICON MONOLITHIC
 INTEGRATED CIRCUIT**



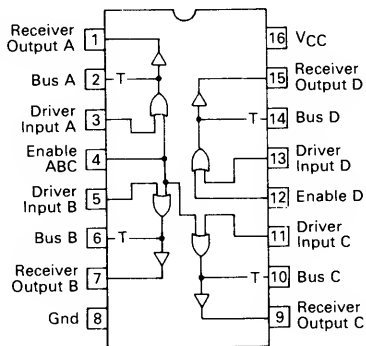
P SUFFIX
 PLASTIC PACKAGE
 CASE 648

7

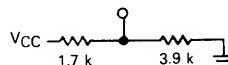
TYPICAL MEASUREMENT SYSTEM APPLICATION



PIN CONNECTIONS



— T — = Bus Termination



MC3446A

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V _{CC}	7.0	Vdc
Input Voltage	V _I	5.5	Vdc
Driver Output Current	I _{O(D)}	150	mA
Junction Temperature	T _J	150	°C
Operating Ambient Temperature Range	T _A	0 to +70	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, 4.5 V ≤ V_{CC} ≤ 5.5 V and 0 ≤ T_A ≤ 70°C, typical values are at T_A = 25°C, V_{CC} = 5.0 V)

Characteristic	Symbol	Min	Typ	Max	Unit
DRIVER PORTION					
Input Voltage — High Logic State	V _{IH(D)}	2.0	—	—	V
Input Voltage — Low Logic State	V _{IL(D)}	—	—	0.8	V
Input Current — High Logic State (V _{IH} = 2.4 V)	I _{IH(D)}	—	5.0	40	μA
Input Current — Low Logic State (V _{IL} = 0.4 V, V _{CC} = 5.0 V, T _A = 25°C)	I _{IL(D)}	—	-0.2	-0.25	mA
Input Clamp Voltage (I _{IK} = -12 mA)	V _{IK(D)}	—	—	-1.5	V
Output Voltage — High Logic State (1) (V _{IH(S)} = 2.4 V or V _{IH(D)} = 2.0 V)	V _{OH(D)}	2.5	3.3	3.7	V
Output Voltage — Low Logic State (V _{IL(S)} = 0.8 V, V _{IL(D)} = 0.8 V, I _{OL(D)} = 48 mA)	V _{OL(D)}	—	—	0.5	
Input Breakdown Current (V _{I(D)} = 5.5 V)	I _{IB(D)}	—	—	1.0	mA

RECEIVER PORTION

Input Hysteresis	—	400	625	—	mV
Input Threshold Voltage — Low to High Output Logic State	V _{ILH(R)}	—	1.66	2.0	V
Input Threshold Voltage — High to Low Output Logic State	V _{IHL(R)}	0.8	1.03	—	V
Output Voltage — High Logic State (V _{IH(R)} = 2.0 V, I _{OH(R)} = -400 μA)	V _{OH(R)}	2.4	—	—	V
Output Voltage — Low Logic State (V _{IL(R)} = 0.8 V, I _{OL(R)} = 8.0 mA)	V _{OL(R)}	—	—	0.5	V
Output Short-Circuit Current (V _{IH(R)} = 2.0 V) (Only one output may be shorted at a time)	I _{OS(R)}	4.0	—	14	mA

BUS LOAD CHARACTERISTICS

Bus Voltage (V _{IH(E)} = 2.4 V) (I _{BUS} = -12 mA)	V _(BUS)	2.5	3.3	3.7	V
Bus Current (V _{IH(O)} = 2.4 V, V _{BUS} = 5.0 V) (V _{IH(D)} = 2.4 V, V _{BUS} = 0.5 V) (V _{BUS} ≤ 5.5 V) (V _{CC} = 0, 0 V ≤ V _{BUS} ≤ 2.75 V)	I _(BUS)	0.7	—	—	mA
		-1.3	—	-3.2	
		—	—	2.5	
		—	—	0.04	

TOTAL DEVICE POWER CONSUMPTION

Power Supply Current (All Drivers OFF) (All Drivers ON)	I _{CC}	—	12	19	mA
		—	32	40	

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
DRIVER PORTION					
Propagation Delay Time from Driver Input to Low Logic State Bus Output	t _{PHL(D)}	—	—	50	ns
Propagation Delay Time from Driver Input to High Logic State Bus Output	t _{PLH(D)}	—	—	40	ns
Propagation Delay Time from Enable Input to Low Logic State Bus Output	t _{PHL(E)}	—	—	50	ns
Propagation Delay Time from Enable Input to High Logic State Bus Output	t _{PLH(E)}	—	—	50	ns
RECEIVER PORTION					
Propagation Delay Time from Bus Input to High Logic State Receiver Output	t _{PLH(R)}	—	—	50	ns
Propagation Delay Time from Bus Input to Low Logic State Receiver Output	t _{PHL(R)}	—	—	40	ns

FIGURE 1 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM RECEIVER INPUT (BUS) TO OUTPUT

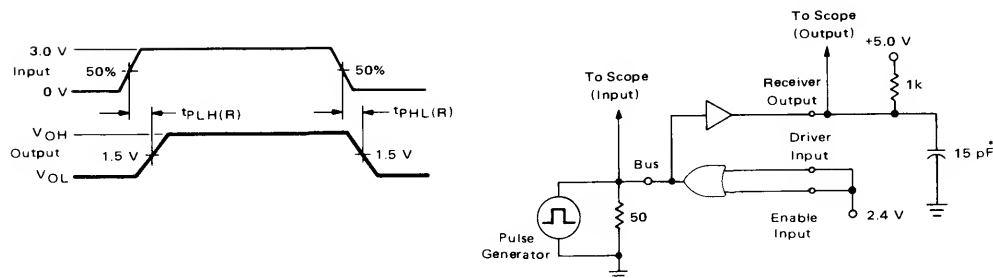
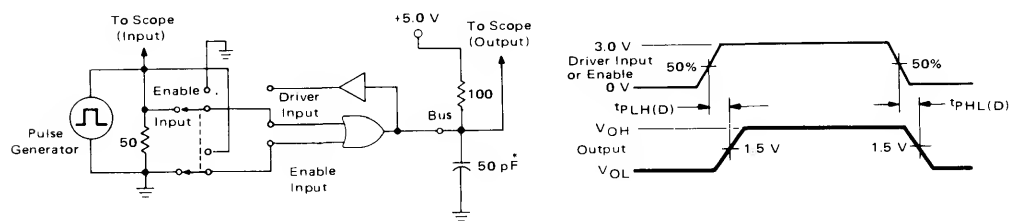


FIGURE 2 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM DRIVER AND COMMON ENABLE INPUTS TO OUTPUT (BUS)



* Includes Probe and Jig Capacitance

FIGURE 3 – TYPICAL RECEIVER HYSTERESIS CHARACTERISTICS

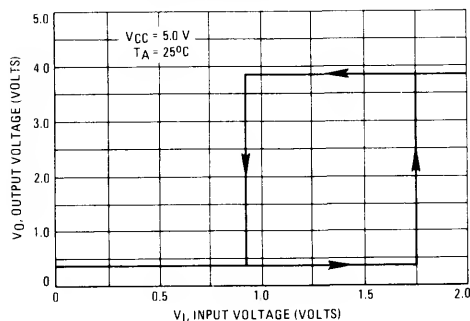
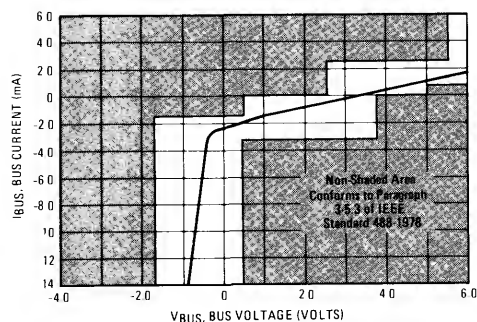


FIGURE 4 – TYPICAL BUS LOAD LINE



MC3447

**BIDIRECTIONAL INSTRUMENTATION
 BUS (GPIB) TRANSCEIVER**

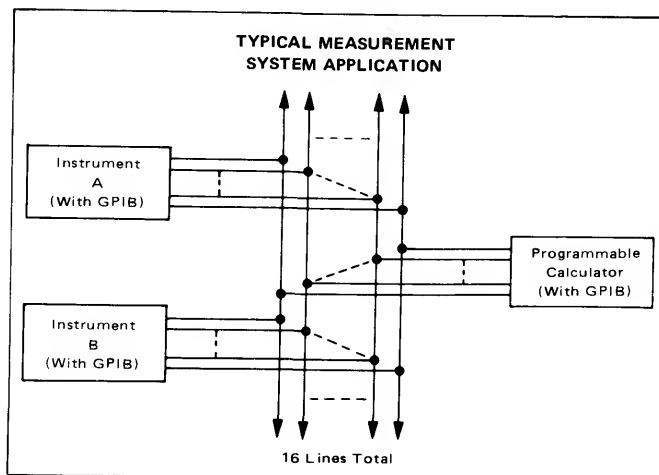
This bidirectional bus transceiver is intended as the interface between TTL or MOS logic and the IEEE Standard Instrumentation Bus (488-1978, often referred to as GPIB). The required bus termination is internally provided.

Low power consumption has been achieved by trading a minimum of speed for low current drain on non-critical channels. A fast channel is provided for critical ATN and EOI paths.

Each driver/receiver pair forms the complete interface between the bus and an instrument. Either the driver or the receiver of each channel is enabled by a Send/Receive input with the disabled output of the pair forced to a high impedance state. The receivers have input hysteresis to improve noise margin, and their input loading follows the bus standard specifications.

- Low Power —
 Average Power Supply Current = 30 mA Listening
 75 mA Talking
- Eight Driver/Receiver Pairs
- Three-State Outputs
- High Impedance Inputs
- Receiver Hysteresis — 600 mV (Typ)
- Fast Propagation Times — 15–20 ns (Typ)
- TTL Compatible Receiver Outputs
- Single +5 Volt Supply
- Open Collector Driver Output with Terminations
- Power Up/Power Down Protection
 (No Invalid Information Transmitted to Bus)
- No Bus Loading When Power is Removed From Device
- Terminations Provided: Termination Removed When Device is Unpowered

**TYPICAL MEASUREMENT
 SYSTEM APPLICATION**

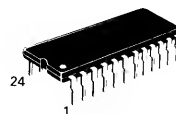


**OCTAL BIDIRECTIONAL
 BUS TRANSCEIVER
 WITH
 TERMINATION NETWORKS**

**SILICON MONOLITHIC
 INTEGRATED CIRCUIT**

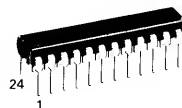


L SUFFIX
 CERAMIC PACKAGE
 CASE 623

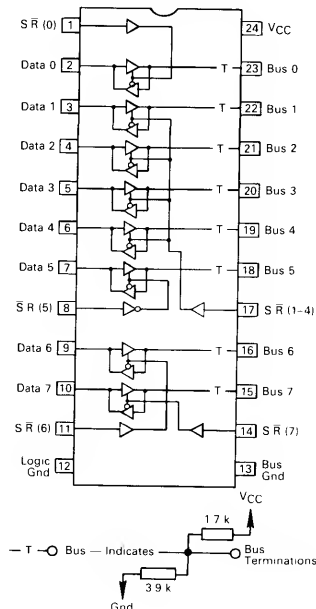


P SUFFIX
 PLASTIC PACKAGE
 CASE 649

P3 SUFFIX
 PLASTIC PACKAGE
 CASE 724



PIN CONNECTIONS



MC3447

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V _{CC}	7.0	Vdc
Input Voltage	V _I	5.5	Vdc
Driver Output Current	I _{O(D)}	150	mA
Junction Temperature	T _J	150	°C
Operating Ambient Temperature Range	T _A	0 to +70	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted 4.50 V < V_{CC} ≤ 5.50 V and 0 ≤ T_A < 70°C; typical values are at T_A = 25°C, V_{CC} = 5.0 V)

Characteristic — Note 1	Symbol	Min	Typ	Max	Unit	
Bus Voltage (Bus Pin Open) ($V_{I(S/\bar{R})} = 0.8\text{ V}$) ($I_{(Bus)} = -12\text{ mA}$)	$V_{(Bus)}$ $V_{IC(Bus)}$	2.5 —	— —	3.7 -1.5	V	
Bus Current ($5.0\text{ V} < V_{(Bus)} \leq 5.5\text{ V}$) ($V_{(Bus)} = 0.5\text{ V}$) ($V_{CC} = 0\text{ V}$, $0\text{ V} \leq V_{(Bus)} \leq 2.75\text{ V}$)	$I_{(Bus)}$	0.7 -1.3 —	— — —	2.5 -3.2 +0.04	mA	
Receiver Input Hysteresis ($V_{I(S/\bar{R})} = 0.8\text{ V}$)	—	400	600	—	mV	
Receiver Input Threshold ($V_{I(S/\bar{R})} = 0.8\text{ V}$)	Low to High High to Low	$V_{ILH(R)}$ $V_{IHL(R)}$	— 0.8	1.6 1.0	2.0 —	V
Receiver Output Voltage — High Logic State ($V_{I(S/\bar{R})} = 0.8\text{ V}$, $I_{OH(R)} = -200\text{ }\mu\text{A}$, $V_{(Bus)} = 2.0\text{ V}$)	$V_{OH(R)}$	2.4	—	—	V	
Receiver Output Voltage — Low Logic State ($V_{I(S/\bar{R})} = 0.8\text{ V}$, $I_{OL(R)} = 4.0\text{ mA}$, $V_{(Bus)} = 0.8\text{ V}$)	$V_{OL(R)}$	—	—	0.5	V	
Receiver Output Short Circuit Current ($V_{I(S/\bar{R})} = 0.8\text{ V}$, $V_{(Bus)} = 2.0\text{ V}$)	$I_{OS(R)}$	-4.0	—	-20	mA	
Driver Input Voltage — High Logic State ($V_{I(S/\bar{R})} = 2.0\text{ V}$)	$V_{IH(D)}$	2.0	—	—	V	
Driver Input Voltage — Low Logic State ($V_{I(S/\bar{R})} = 2.0\text{ V}$)	$V_{IL(D)}$	—	—	0.8	V	
Driver Input Current — Data Pins ($V_{I(S/\bar{R})} = 2.0\text{ V}$) ($0.5 < V_{I(D)} \leq 2.7\text{ V}$) ($V_{I(D)} = 5.5\text{ V}$)	$I_{I(D)}$ $I_{IB(D)}$	-100 —	— —	40 200	μA	
Input Current — Send/Receive ($0.5 < V_{I(S/\bar{R})} \leq 2.7\text{ V}$) ($V_{I(S/\bar{R})} = 5.5\text{ V}$)	$I_{I(S/\bar{R})}$ $I_{IB(S/\bar{R})}$	-250 —	— —	20 100	μA	
Driver Input Clamp Voltage ($V_{I(S/\bar{R})} = 2.0\text{ V}$, $I_{IC(D)} = -18\text{ mA}$)	$V_{IC(D)}$	—	—	-1.5	V	
Driver Output Voltage — High Logic State ($V_{I(S/\bar{R})} = 2.0\text{ V}$, $V_{IH(D)} = 2.0\text{ V}$)	$V_{OH(D)}$	2.5	—	—	V	
Driver Output Voltage — Low Logic State (Note 2) ($V_{I(S/\bar{R})} = 2.0\text{ V}$, $V_{IL(D)} = 0.8\text{ V}$, $I_{OL(D)} = 48\text{ mA}$)	$V_{OL(D)}$	—	—	0.5	V	
Power Supply Current (Listening Mode — All Receivers On) (Talking Mode — All Drivers On)	I_{CCL} I_{CCH}	— —	30 75	45 95	mA	

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted)

Propagation Delay of Driver (Output Low to High) (Output High to Low)	t _{PLH(D)} t _{PHL(D)}	— —	7.0 16	15 30	ns
Propagation Delay of Receiver (Channels 0 to 5, 7) (Output Low to High) (Output High to Low)	t _{PLH(R)} t _{PHL(R)}	— —	28 15	50 30	ns
Propagation Delay of Receiver (Channel 6, Note 3) (Output Low to High) (Output High to Low)	t _{PLH(R)} t _{PHL(R)}	— —	17 12	30 22	ns

- NOTES: 1. Specified test conditions for V_{I(S/R)} are 0.8 V (Low) and 2.0 V (High). Where V_{I(S/R)} is specified as a test condition, V_{I(S/R)} uses the opposite logic levels.
2. The IEEE 488-1979 Bus Standard changes V_{OL(D)} from 0.4 to 0.5 V maximum to permit the use of Schottky technology.
3. In order to meet the IEEE 488-1978 Standard for total system delay on the ATN and EOI channels, a fast receiver has been provided on Channel 6 (Pins 9 and 16).

MC3447

SWITCHING CHARACTERISTICS (continued) ($V_{CC} = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time — Send/Receiver to Data					ns
Logic High to Third State	$t_{PHZ}(R)$	—	15	30	
Third State to Logic High	$t_{PZH}(R)$	—	15	30	
Logic Low to Third State	$t_{PLZ}(R)$	—	15	25	
Third State to Logic Low	$t_{PZL}(R)$	—	10	25	
Propagation Delay Time — Send/Receiver to Bus					ns
Logic Low to Third State	$t_{PLZ}(D)$	—	13	25	
Third State to Logic Low	$t_{PZL}(D)$	—	30	50	

PROPAGATION DELAY TEST CIRCUITS AND WAVEFORMS

FIGURE 1 — BUS INPUT TO DATA OUTPUT (RECEIVER)

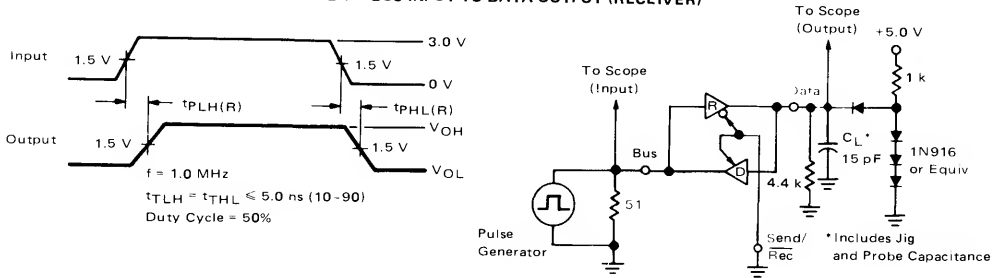


FIGURE 2 — DATA INPUT TO BUS OUTPUT (DRIVER)

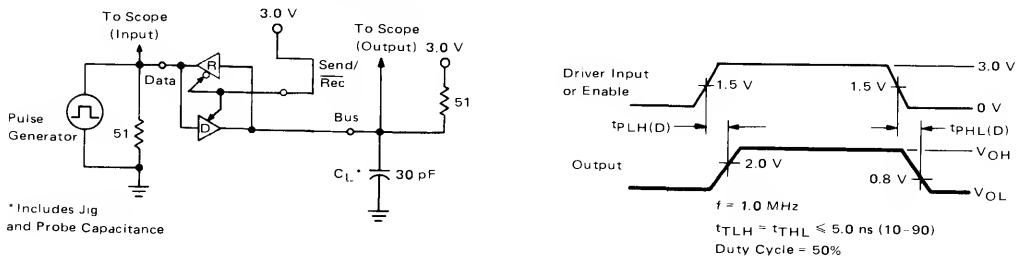
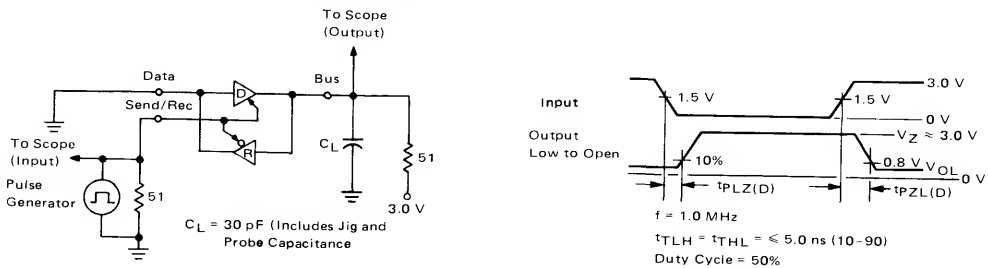


FIGURE 3 — SEND/RECEIVE INPUT TO BUS OUTPUT (DRIVER)



MC3447

FIGURE 4 – SEND/RECEIVE INPUT TO DATA OUTPUT (RECEIVER)

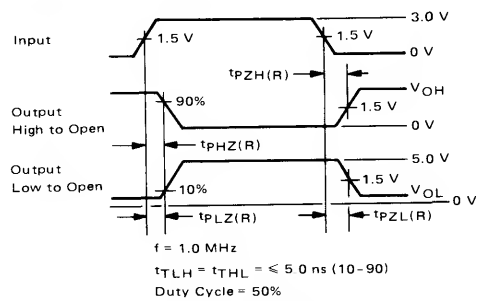
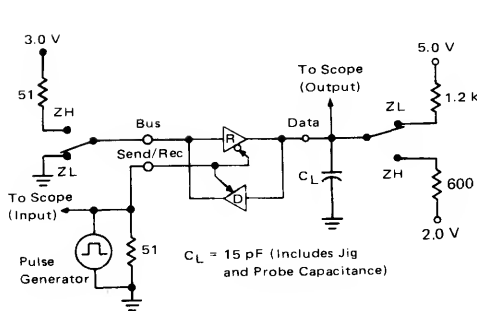


FIGURE 5 – TYPICAL RECEIVER HYSTERESIS CHARACTERISTICS

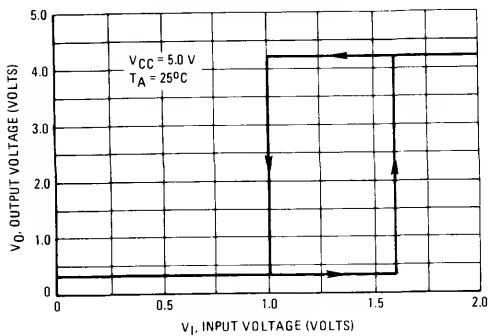


FIGURE 6 – TYPICAL BUS LOAD LINE

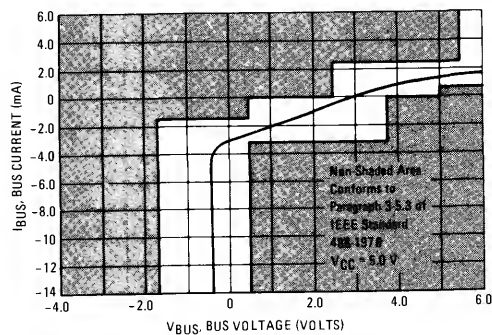
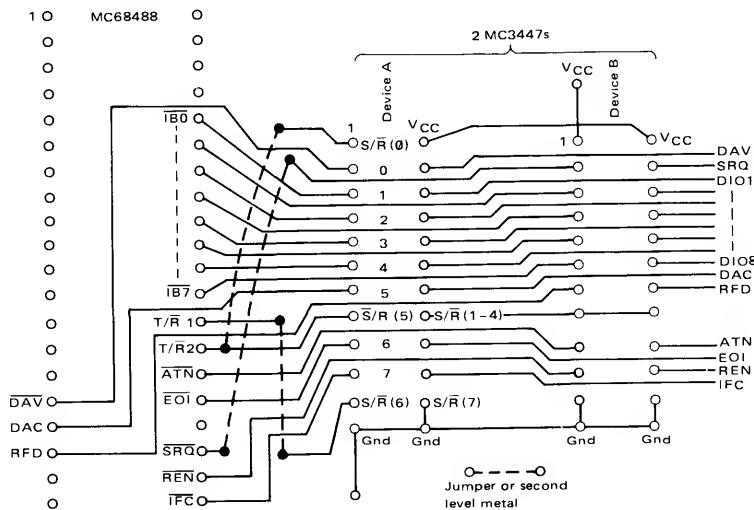


FIGURE 7 – SUGGESTED PRINTED CIRCUIT BOARD LAYOUT USING MC3447s AND MC68488



7

The diagram illustrates the connection between an IEEE 488-1978 BUS and an MC6802 or MC6800 MPU via the MC68488 GPIA. On the left, the IEEE 488-1978 BUS is represented by a dashed box containing 16 MC3447s transceivers. These transceivers are connected to the MC68488 GPIA pins: DAV, DIO1, DIO3, DIO5, DIO7, NDAC, EO1, IFC, SRO, DIO2, DIO4, DIO6, DIO8, NRFD, ATN, and REN. The MC68488 GPIA is a central component with pins for T/R 1, T/R 2, DAV, IB0, IB2, IB4, IB6, DAC, EO1, IFC, SRQ, IB1, IB3, IB5, IB7, RFD, ATN, REN, and Trig. The Trig pin is connected to the +5V supply. The MC68488 GPIA is connected to the MC6802 or MC6800 MPU. The MPU has pins for DB0, DB7, R/W, RS0, RS2, Address, IRQ, D0, D7, A0, and A15. The connection between the MC68488 GPIA and the MPU is as follows: DB0 to D0, DB7 to D7, R/W to R/W, RS0 to A0, RS2 to A15, Address to Address, IRQ to IRQ, and A15 to A15. The MC68488 GPIA is also connected to the +5V supply and ground.

NOTE 1: Although the MC3447 transceivers are noninverting, the 488-1978 bus callouts appear inverted with respect to the MC68488 pin designations. This is because the 488-1978 Standard is defined for negative logic, while all M6800 MPU components make use of positive logic format.

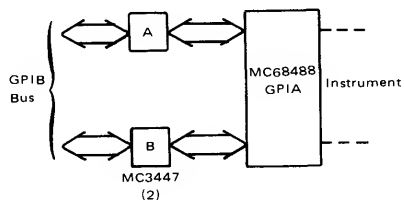
MOTOROLA LINEAR/INTERFACE DEVICES

MC3447

FIGURE 9 – SUGGESTED PIN DESIGNATIONS FOR USE WITH MC68488

MC68488 Connections		MC3447 Pin Designations				MC68488 Connections	
A	B					A	B
$\overline{T/R}$ 2	V_{CC}	$\overline{S/R}$ (0)	1	24	V_{CC}	V_{CC}	V_{CC}
\overline{DAV}	\overline{SRQ}	Data 0 0	2	23	Bus 0	\overline{DAV}	\overline{SRO}
$\overline{IB0}$	$\overline{IB1}$	Data 1	3	22	Bus 1	DIO 1	DIO 2
$\overline{IB2}$	$\overline{IB3}$	Data 2	4	21	Bus 2	DIO 3	DIO 4
$\overline{IB4}$	$\overline{IB5}$	Data 3	5	20	Bus 3	DIO 5	DIO 6
$\overline{IB6}$	$\overline{IB7}$	Data 4	6	19	Bus 4	DIO 7	DIO 8
DAC	RFD	Data 5	7	18	Bus 5	NDAC	NRFD
$\overline{T/R}$ 2	$\overline{T/R}$ 2	$\overline{S/R}$ (5)	8	17	$\overline{S/R}$ (1-4)	$\overline{T/R}$ 2	$\overline{T/R}$ 2
EOI	\overline{ATN}	Data 6	9	16	Bus 6	EOI	\overline{ATN}
IFC	\overline{REN}	Data 7	10	15	Bus 7	IFC	\overline{REN}
$\overline{T/R}$ 1	Gnd	$\overline{S/R}$ (6)	11	14	$\overline{S/R}$ (7)	Gnd	Gnd
Gnd	Gnd	Logic Gnd	12	13	Bus Gnd	Gnd	Gnd

7



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

BIDIRECTIONAL INSTRUMENTATION BUS (GPIB) TRANSCEIVER

This bidirectional bus transceiver is intended as the interface between TTL or MOS logic and the IEEE Standard Instrumentation Bus (488-1978, often referred to as GPIB). The required bus termination is internally provided.

Each driver/receiver pair forms the complete interface between the bus and an instrument. Either the driver or the receiver of each channel is enabled by its corresponding Send/Receive input with the disabled output of the pair forced to a high impedance state. An additional option allows the driver outputs to be operated in an open collector⁽¹⁾ or active pull-up configuration. The receivers have input hysteresis to improve noise margin, and their input loading follows the bus standard specifications.

- Four Independent Driver/Receiver Pairs
- Three-State Outputs
- High Impedance Inputs
- Receiver Hysteresis — 600 mV (Typ)
- Fast Propagation Times — 15–20 ns (Typ)
- TTL Compatible Receiver Outputs
- Single +5 Volt Supply
- Open Collector Driver Output Option⁽¹⁾
- Power Up/Power Down Protection
- (No Invalid Information Transmitted to Bus)
- No Bus Loading When Power Is Removed From Device
- Terminations Provided: Termination Removed When Device is Unpowered

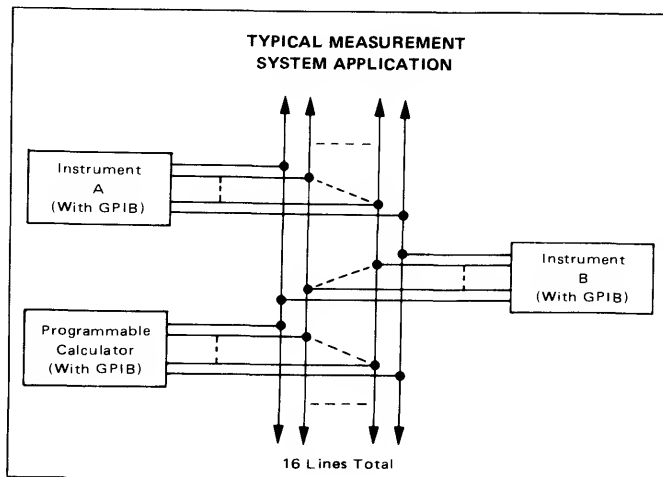
(1) Selection of the "Open Collector" configuration, in fact, selects an open collector device with a passive pull-up load/termination which conforms to Figure 7, IEEE 488-1978 Bus Standard.

TRUTH TABLE

Send/Rec.	Enable	Info. Flow	Comments
0	X	Bus → Data	—
1	1	Data → Bus	Active Pull-Up
1	0	Data → Bus	Open Col.

X - Don't Care

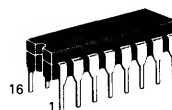
TYPICAL MEASUREMENT
SYSTEM APPLICATION



MC3448A

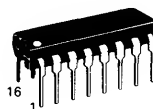
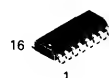
QUAD THREE-STATE BUS TRANSCEIVER WITH TERMINATION NETWORKS

SILICON MONOLITHIC INTEGRATED CIRCUIT



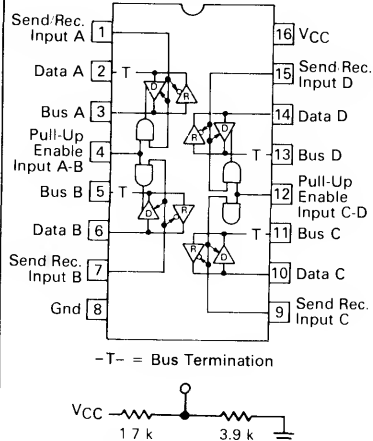
L SUFFIX
CERAMIC PACKAGE
CASE 620

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO-16)



P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS



MC3448A

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V _{CC}	7.0	V _{dc}
Input Voltage	V _I	5.5	V _{dc}
Driver Output Current	I _{O(D)}	150	mA
Junction Temperature	T _J	150	°C
Operating Ambient Temperature Range	T _A	0 to +70	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted 4.75 V ≤ V_{CC} ≤ 5.25 V and 0 ≤ T_A ≤ 70°C; typical values are at T_A = 25°C, V_{CC} = 5.0 V)

Characteristic	Symbol	Min	Typ	Max	Unit
Bus Voltage (Bus Pin Open) (V _{I(S/R)} = 0.8 V) (I _{I(BUS)} = -12 mA)	V _(BUS) V _{IC(BUS)}	2.75 —	— —	3.7 -1.5	V
Bus Current (5.0 V ≤ V _(BUS) ≤ 5.5 V) (V _(BUS) = 0.5 V) (V _{CC} = 0 V, 0 V ≤ V _(BUS) ≤ 2.75 V)	I _(BUS)	0.7 -1.3 —	— — —	2.5 -3.2 +0.04	mA
Receiver Input Hysteresis (V _{I(S/R)} = 0.8 V)	—	400	600	—	mV
Receiver Input Threshold (V _{I(S/R)} = 0.8 V, Low to High) (V _{I(S/R)} = 0.8 V, High to Low)	V _{ILH(R)} V _{IHL(R)}	— 0.8	1.6 1.0	1.8 —	V
Receiver Output Voltage — High Logic State (V _{I(S/R)} = 0.8 V, I _{OH(R)} = -800 μA, V _(BUS) = 2.0 V)	V _{OH(R)}	2.7	—	—	V
Receiver Output Voltage — Low Logic State (V _{I(S/R)} = 0.8 V, I _{OL(R)} = 16 mA, V _(BUS) = 0.8 V)	V _{OL(R)}	—	—	0.5	V
Receiver Output Short Circuit Current (V _{I(S/R)} = 0.8 V, V _(BUS) = 2.0 V)	I _{OS(R)}	-15	—	-75	mA
Driver Input Voltage — High Logic State (V _{I(S/R)} = 2.0 V)	V _{IH(D)}	2.0	—	—	V
Driver Input Voltage — Low Logic State (V _{I(S/R)} = 2.0 V)	V _{IL(D)}	—	—	0.8	V
Driver Input Current — Data Pins (V _{I(S/R)} = V _{I(E)} = 2.0 V) (0.5 ≤ V _{I(D)} ≤ 2.7 V) (V _{I(D)} = 5.5 V)	I _{I(D)} I _{IB(D)}	-200 —	— —	40 200	μA
Input Current — Send/Receive (0.5 ≤ V _{I(S/R)} ≤ 2.7 V) (V _{I(S/R)} = 5.5 V)	I _{I(S/R)} I _{IB(S/R)}	-100 —	— —	20 100	μA
Input Current — Enable (0.5 ≤ V _{I(E)} ≤ 2.7 V) (V _{I(E)} = 5.5 V)	I _{I(E)} I _{IB(E)}	-200 —	— —	20 100	μA
Driver Input Clamp Voltage (V _{I(S/R)} = 2.0 V, I _{IC(D)} = -18 mA)	V _{IC(D)}	—	—	-1.5	V
Driver Output Voltage — High Logic State (V _{I(S/R)} = 2.0 V, V _{IH(D)} = 2.0 V, V _{IH(E)} = 2.0 V, I _{OH} = -5.2 mA)	V _{OH(D)}	2.5	—	—	V
Driver Output Voltage — Low Logic State (Note 1) (V _{I(S/R)} = 2.0 V, I _{OL(D)} = 48 mA)	V _{OL(D)}	—	—	0.5	V
Output Short Circuit Current (V _{I(S/R)} = 2.0 V, V _{IH(D)} = 2.0 V, V _{IH(E)} = 2.0 V)	I _{OS(D)}	-30	—	-120	mA
Power Supply Current (Listening Mode — All Receivers On) (Talking Mode — All Drivers On)	I _{CCL} I _{CCH}	— —	63 106	85 125	mA

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted)

Propagation Delay of Driver (Output Low to High) (Output High to Low)	t _{PLH(D)} t _{PHL(D)}	— —	— —	15 17	ns
Propagation Delay of Receiver (Output Low to High) (Output High to Low)	t _{PLH(R)} t _{PHL(R)}	— —	— —	25 23	ns

NOTE 1. A modification of the IEEE 48B-1978 Bus Standard changes V_{OL(D)} from 0.4 to 0.5 V maximum to permit the use of Schottky technology.

SWITCHING CHARACTERISTICS (continued) ($V_{CC} = 5.0 \text{ V}$, $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time — Send/Receive to Data					ns
Logic High to Third State	$t_{PHZ}(R)$	—	—	30	
Third State to Logic High	$t_{PZH}(R)$	—	—	30	
Logic Low to Third State	$t_{PLZ}(R)$	—	—	30	
Third State to Logic Low	$t_{PZL}(R)$	—	—	30	
Propagation Delay Time — Send/Receive to Bus					ns
Logic High to Third State	$t_{PHZ}(D)$	—	—	30	
Third State to Logic High	$t_{PZH}(D)$	—	—	30	
Logic Low to Third State	$t_{PLZ}(D)$	—	—	30	
Third State to Logic Low	$t_{PZL}(D)$	—	—	30	
Turn-On Time — Enable to Bus					ns
Pull-Up Enable to Open Collector	$t_{POFF}(E)$	—	—	30	
Open Collector to Pull-Up Enable	$t_{PON}(E)$	—	—	20	

PROPAGATION DELAY TEST CIRCUITS AND WAVEFORMS

FIGURE 1 — BUS INPUT TO DATA OUTPUT (RECEIVER)

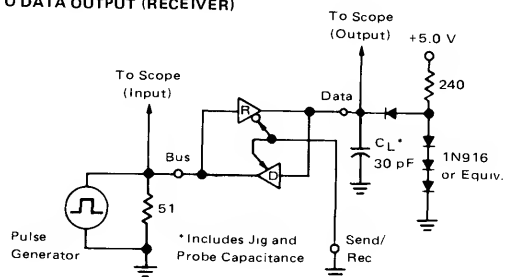
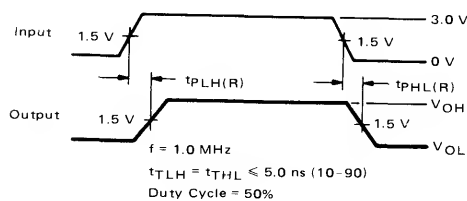


FIGURE 2 — DATA INPUT TO BUS OUTPUT (DRIVER)

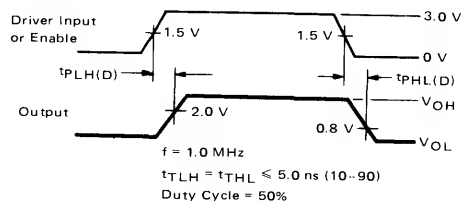
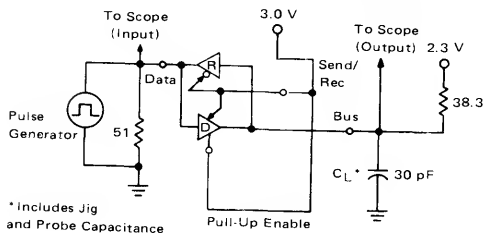


FIGURE 3 — SEND/RECEIVE INPUT TO BUS OUTPUT (DRIVER)

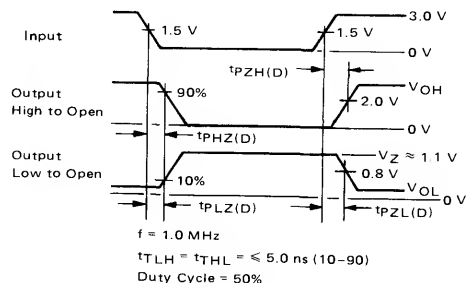
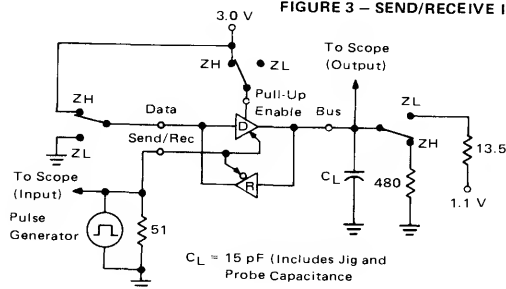


FIGURE 4 – SEND/RECEIVE INPUT TO DATA OUTPUT (RECEIVER)

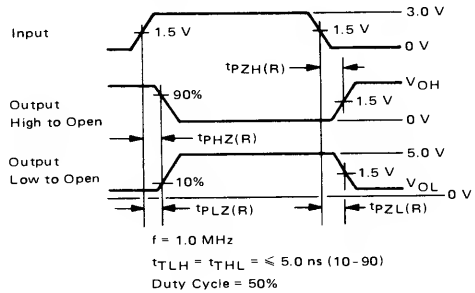
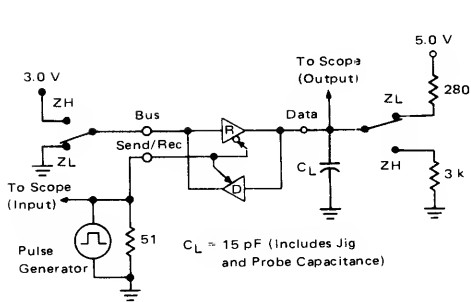


FIGURE 5 – ENABLE INPUT TO BUS OUTPUT (DRIVER)

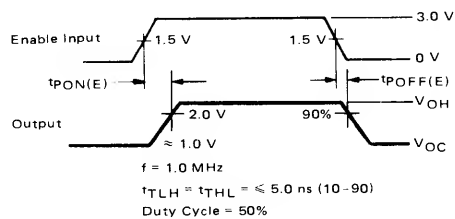
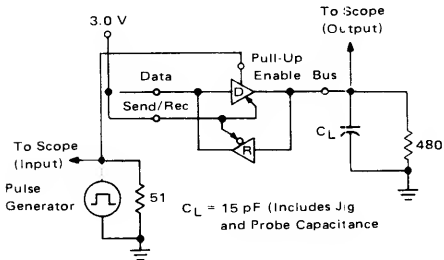


FIGURE 6 – TYPICAL RECEIVER HYSTERESIS CHARACTERISTICS

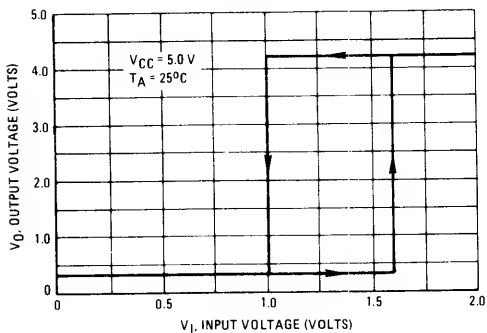
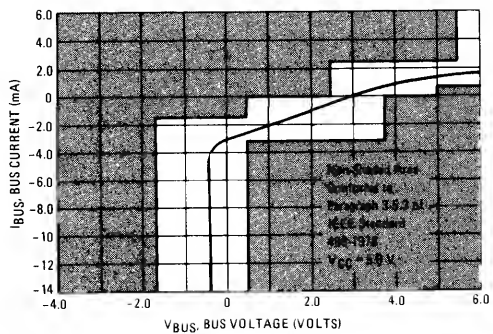
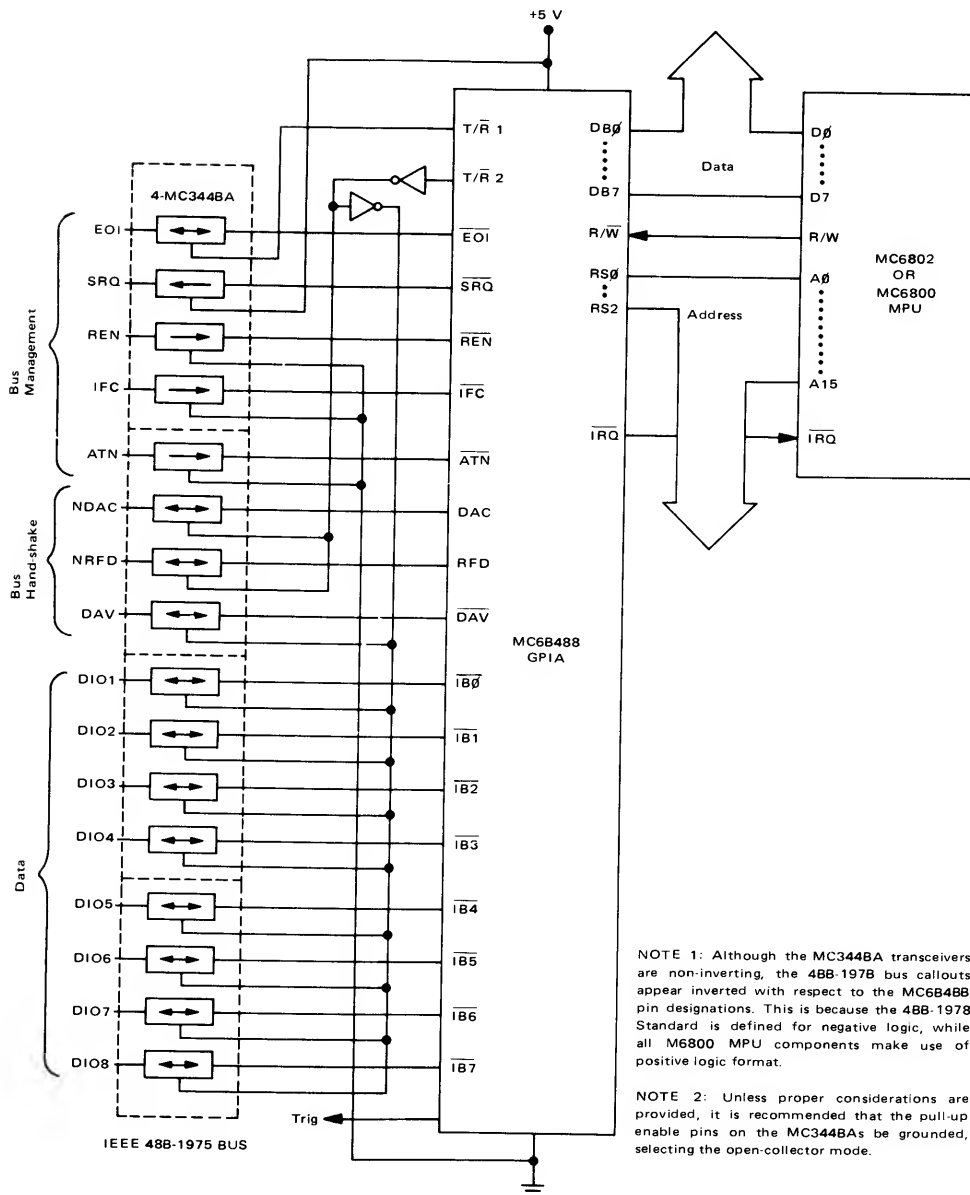


FIGURE 7 – TYPICAL BUS LOAD LINE



MC3448A

FIGURE 8 — SIMPLE SYSTEM CONFIGURATION



QUAD MTTL COMPATIBLE
LINE RECEIVERS

The MC3450 features four MC75107 type active pullup line receivers with the addition of a common three-state strobe input. When the strobe input is at a logic zero, each receiver output state is determined by the differential voltage across its respective inputs. With the strobe high, the receiver outputs are in the high impedance state.

The MC3452 is the same as the MC3450 except that the outputs are open collector which permits the implied "AND" function.

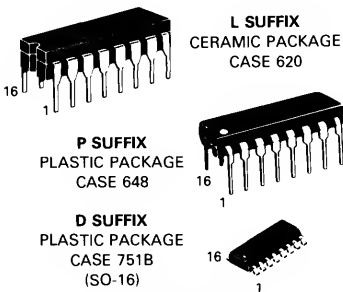
The strobe input on both devices is buffered to present a strobe loading factor of only one for all four receivers and inverted to provide best compatability with standard decoder devices.

- Receiver Performance Identical to the Popular MC75107/MC75108 Series
- Four Independent Receivers with Common Strobe Input
- Implied "AND" Capability with Open Collector Outputs
- Useful as a Quad 1103 type Memory Sense Amplifier

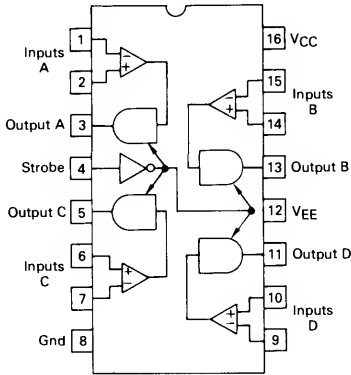
MC3450
MC3452

QUAD LINE RECEIVERS
WITH COMMON THREE-STATE
STROBE INPUT

SILICON MONOLITHIC
INTEGRATED CIRCUITS



PIN CONNECTIONS

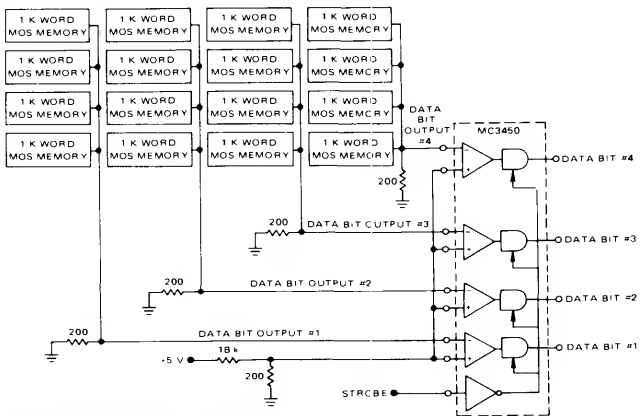


TRUTH TABLE

Input	Strobe	Output	
		MC3450	MC3452
$V_{ID} \geq +25\text{ mV}$	L	H	Off
	H	Z	Off
$-25\text{ mV} \leq V_{ID} \leq +25\text{ mV}$	L	I	I
	H	Z	Off
$V_{ID} \leq -25\text{ mV}$	L	L	L
	H	Z	Off

L = Low Logic State
H = High Logic State
Z = Third (High Impedance) State
I = Indeterminate State

FIGURE 1 — A TYPICAL MOS MEMORY SENSING APPLICATION FOR A
4 k WORD BY 4-BIT MEMORY ARRANGEMENT EMPLOYING
1103 TYPE MEMORY DEVICES



Only four MC3450 devices are required for
a 4 k word by 16-bit memory system.

MC3450, MC3452

MAXIMUM RATINGS (T_A = 0 to +70°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltages	V _{CC} , V _{EE}	±7.0	V _{dc}
Differential Mode Input Signal Voltage Range	V _{IDR}	±6.0	V _{dc}
Common Mode Input Voltage Range	V _{ICR}	±5.0	V _{dc}
Strobe Input Voltage	V _{I(S)}	5.5	V _{dc}
Power Dissipation (Package Limitation)	P _D		
Ceramic Dual In-Line Package		1000	mW
Derate above T _A = +25°C		6.6	mW/°C
Plastic Dual In-Line Package		1000	mW
Derate above T _A = +25°C		6.6	mW/°C
Operating Temperature Range	T _A	0 to +70	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltages	V _{CC} V _{EE}	+4.75 -4.75	+5.0 -5.0	+5.25 -5.25	V _{dc}
Output Load Current	I _{OL}	—	—	16	mA
Differential Mode Input Voltage Range	V _{IDR}	-5.0	—	+5.0	V _{dc}
Common Mode Input Voltage Range	V _{ICR}	-3.0	—	+3.0	V _{dc}
Input Voltage Range (any input to Ground)	V _{IR}	-5.0	—	+3.0	V _{dc}

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 V_{dc}, V_{EE} = -5.0 V_{dc}, T_A = 0 to +70°C unless otherwise noted.)

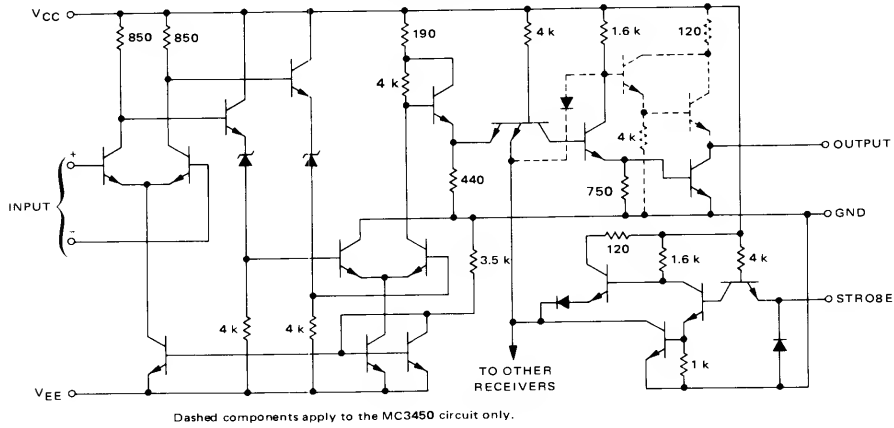
Characteristic	Symbol	Fig.	MC3450			MC3452			Unit
			Min	Typ	Max	Min	Typ	Max	
High Level Input Current to Receiver Input	I _{IH(I)}	7	—	—	75	—	—	75	μA
Low Level Input Current to Receiver Input	I _{IL(I)}	8	—	—	-10	—	—	-10	μA
High Level Input Current to Strobe Input V _{IH(S)} = +2.4 V V _{IH(S)} = +5.25 V	I _{IH(S)}	5	—	—	40 1.0	—	—	40 1.0	μA mA
Low Level Input Current to Strobe Input V _{IL(S)} = +0.4 V	I _{IL(S)}	5	—	—	-1.6	—	—	-1.6	mA
High Level Output Voltage	V _{OH}	3	2.4	—	—	—	—	—	V _{dc}
High Level Output Leakage Current	I _{CEX}	3	—	—	—	—	—	250	μA
Low Level Output Voltage	V _{OL}	3	—	—	0.5	—	—	0.5	V _{dc}
Short-Circuit Output Current	I _{OS}	6	-18	—	-70	—	—	—	mA
Output Disable Leakage Current	I _{off}	9	—	—	40	—	—	—	μA
High Logic Level Supply Current from V _{CC}	I _{CCH}	4	—	45	60	—	45	60	mA
High Logic Level Supply Current from V _{EE}	I _{EEH}	4	—	-17	-30	—	-17	-30	mA

SWITCHING CHARACTERISTICS (V_{CC} = +5.0 V_{dc}, V_{EE} = -5.0 V_{dc}, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	Fig.	MC3450			MC3452			Unit
			Min	Typ	Max	Min	Typ	Max	
High to Low Logic Level Propagation Delay Time (Differential Inputs)	t _{PHL(D)}	10	—	—	25	—	—	25	ns
Low to High Logic Level Propagation Delay Time (Differential Inputs)	t _{PLH(D)}	10	—	—	25	—	—	25	ns
Open State to High Logic Level Propagation Delay Time (Strobe)	t _{PZH(S)}	11	—	—	21	—	—	—	ns
High Logic Level to Open State Propagation Delay Time (Strobe)	t _{PHZ(S)}	11	—	—	18	—	—	—	ns
Open State to Low Logic Level Propagation Delay Time (Strobe)	t _{PZL(S)}	11	—	—	27	—	—	—	ns
Low Logic Level to Open State Propagation Delay Time (Strobe)	t _{PLZ(S)}	11	—	—	29	—	—	—	ns
High Logic to Low Logic Level Propagation Delay Time (Strobe)	t _{PHL(S)}	12	—	—	—	—	—	25	ns
Low Logic to High Logic Level Propagation Delay Time (Strobe)	t _{PLH(S)}	12	—	—	—	—	—	25	ns

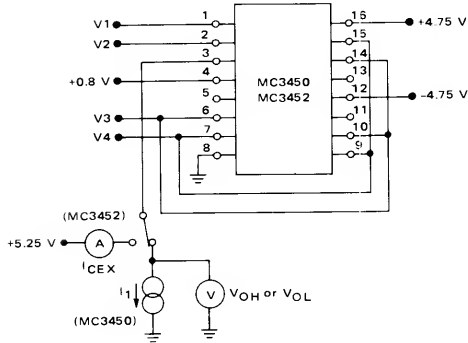
MC3450, MC3452

FIGURE 2 – CIRCUIT SCHEMATIC
(1/4 Circuit Shown)



TEST CIRCUITS

FIGURE 3 – I_{CEX} , V_{OH} , AND V_{OL}



TEST TABLE

	V1		V2		V3		V4		
	MC3450	MC3452	MC3450	MC3452	MC3450	MC3452	MC3450	MC3452	I1
V_{OH}	+2.975 V	—	+3.0 V	—	+3.0 V	—	GND	—	+0.4 mA
	-3.0 V	—	-2.975 V	—	GND	—	-3.0 V	—	
I_{CEX}	—	+2.975 V	—	+3.0 V	—	+3.0 V	—	GND	
	—	-3.0 V	—	-2.975 V	—	GND	—	-3.0 V	
V_{OL}	+3.0 V	+3.0 V	+2.975 V	+2.975 V	GND	GND	+3.0 V	+3.0 V	+16 mA
	-2.975 V	-2.975 V	-3.0 V	-3.0 V	-3.0 V	-3.0 V	GND	GND	

Channel A shown under test. Other channels are tested similarly.

FIGURE 4 – I_{CCH} AND I_{EEH}

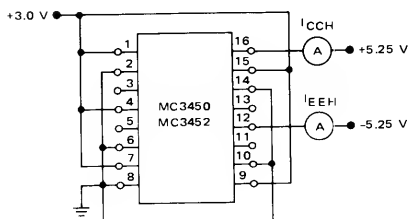
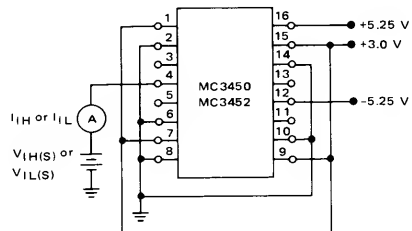


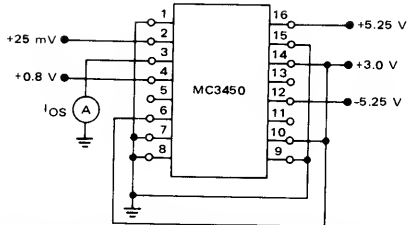
FIGURE 5 – $I_{IH}(S)$ AND $I_{IL}(S)$



MC3450, MC3452

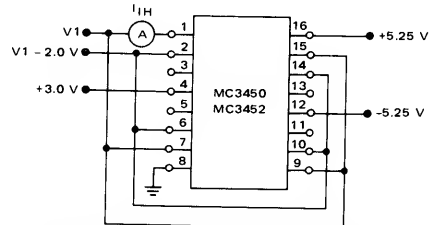
TEST CIRCUITS (continued)

FIGURE 6 – I_{OS}



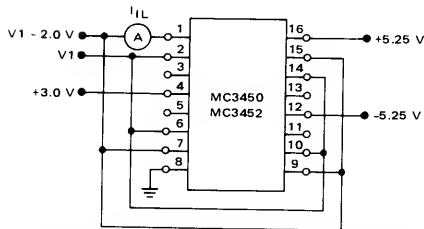
Channel A shown under test, other channels are tested similarly. Only one output shorted at a time.

FIGURE 7 – I_{IH}



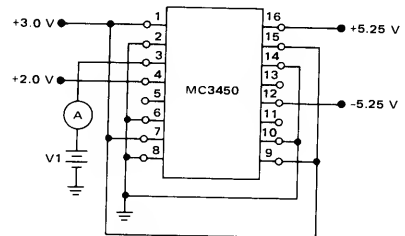
Channel A(-) shown under test, other channels are tested similarly. Devices are tested with V1 from +3.0 V to -3.0 V.

FIGURE 8 – I_{IL}



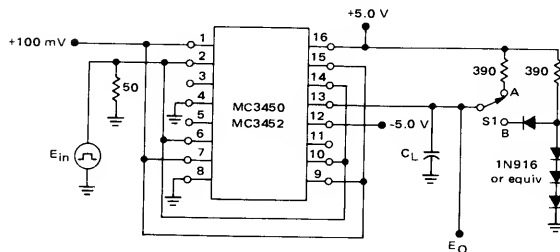
Channel A(-) shown under test, other channels are tested similarly. Devices are tested with V1 from +3.0 V to -3.0 V.

FIGURE 9 – I_{off}



Output of Channel A shown under test, other outputs are tested similarly for V1 = 0.4 V and +2.4 V.

FIGURE 10 – RECEIVER PROPAGATION DELAY $t_{PLH(D)}$ AND $t_{PHL(D)}$



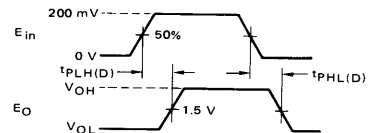
Output of Channel 8 shown under test, other channels are tested similarly.

S1 at "A" for MC3452

S1 at "B" for MC3450

C_L = 15 pF total for MC3452

C_L = 50 pF total for MC3450



E_{in} waveform characteristics:

t_{PLH} and $t_{PHL} \leq 10$ ns measured 10% to 90%

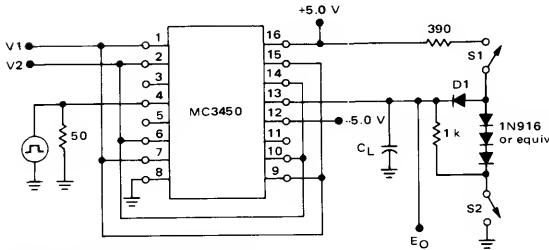
PRR = 1.0 MHz

Duty Cycle = 500 ns

MC3450, MC3452

TEST CIRCUITS (continued)

FIGURE 11 – STROBE PROPAGATION DELAY TIMES $t_{PLZ}(S)$, $t_{PZL}(S)$, $t_{PHZ}(S)$ and $t_{PZH}(S)$



Output of Channel B shown under test, other channels are tested similarly.

	V1	V2	S1	S2	C_L
$t_{PLZ}(S)$	100 mV	GND	Closed	Closed	15 pF
$t_{PZL}(S)$	100 mV	GND	Closed	Open	50 pF
$t_{PHZ}(S)$	GND	100 mV	Closed	Closed	15 pF
$t_{PZH}(S)$	GND	100 mV	Open	Closed	50 pF

C_L includes jig and probe capacitance

E_{in} waveform characteristics

t_{TLH} and $t_{THL} \leq 10$ ns measured 10% to 90%

PRR = 1.0 MHz

Duty Cycle = 50%

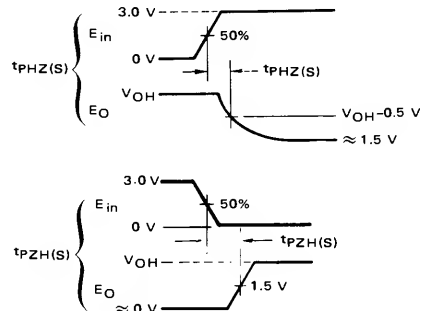
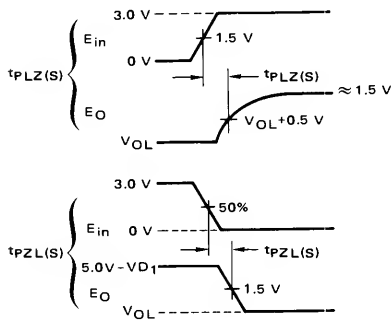
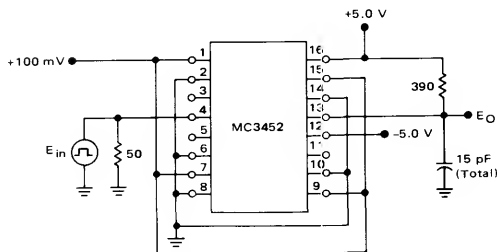
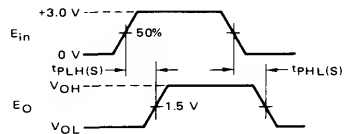


FIGURE 12 – STROBE PROPAGATION DELAY $t_{PLH}(S)$ AND $t_{PHL}(S)$



Output of Channel B shown under test, other channels are tested similarly.



E_{in} waveform characteristics:

t_{TLH} and $t_{THL} \leq 10$ ns measured 10% to 90%

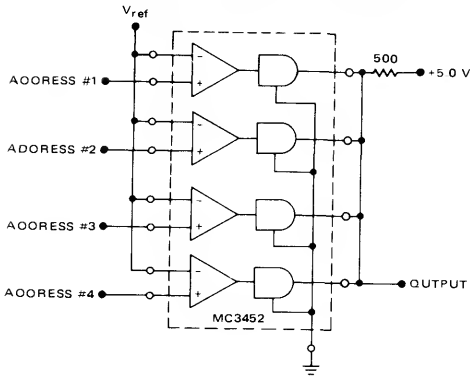
PRR = 1.0 MHz

Duty Cycle = 500 ns

MC3450, MC3452

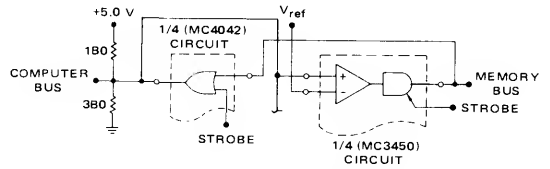
APPLICATIONS INFORMATION

FIGURE 13 – IMPLIED "AND" GATING



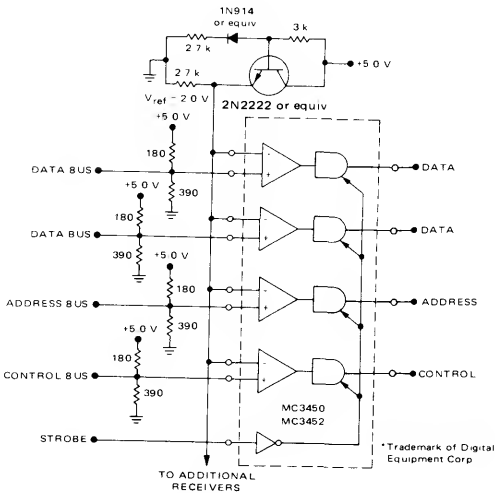
The MC3452 can be used for address decoding as illustrated above. All outputs of the MC3452 are tied together through a common resistor to +5.0 volts. In this configuration the MC3452 provides the "AND" function. All addresses have to be true before the output will go high. This scheme eliminates the need for an "AND" gate and enhances speed throughput for address decoding.

FIGURE 14 – BIDIRECTIONAL DATA TRANSMISSION



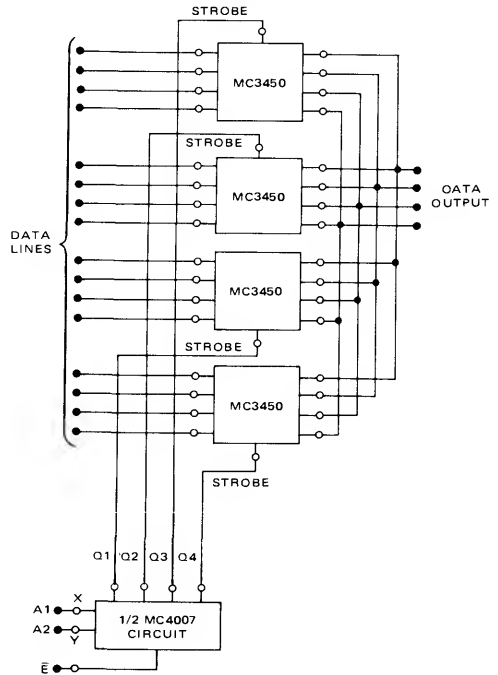
The three-state capability of the MC3450 permits bidirectional data transmission as illustrated.

FIGURE 15 – SINGLE-ENDED UNI-BUS* LINE RECEIVER APPLICATION FOR MINICOMPUTERS



The MC3450/3452 can be used for single-ended as well as differential line receiving. For single-ended line receiver applications, such as are encountered in minicomputers, the configuration shown in Figure 15 can be used. The voltage source, which generates V_{ref} , should be designed so that the V_{ref} voltage is halfway between $V_{OH(min)}$ and $V_{OL(max)}$. The maximum input overdrive required to guarantee a given logic state is extremely small, 25 mV maximum. This low-input overdrive enhances differential noise immunity. Also the high-input impedance of the line receiver permits many receivers to be placed on a single line with minimum load effects.

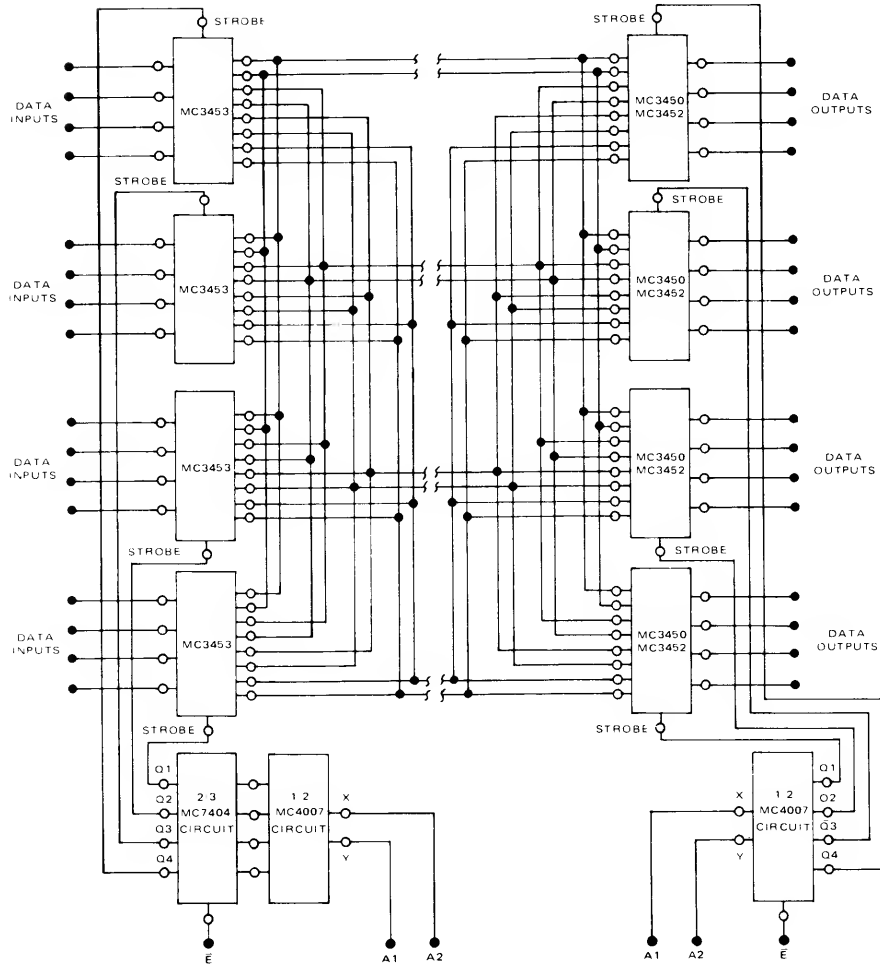
FIGURE 16 – WIRED "OR" DATA SELECTION USING THREE-STATE LOGIC



MC3450, MC3452

APPLICATIONS INFORMATION (continued)

FIGURE 17 — PARTY-LINE DATA TRANSMISSION SYSTEM WITH MULTIPLEX DECODING



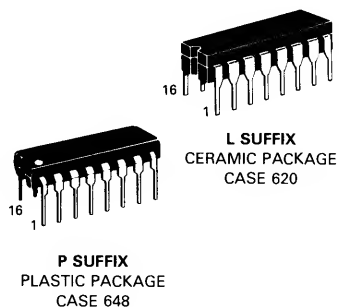
MC3453

MTTL COMPATIBLE QUAD LINE DRIVER

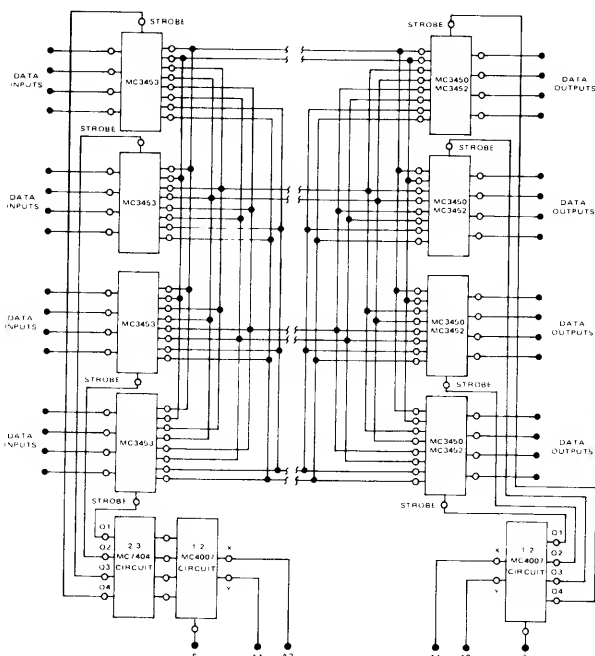
The MC3453 features four SN75110 type line drivers with a common inhibit input. When the inhibit input is high, a constant output current is switched between each pair of output terminals in response to the logic level at that channel's input. When the inhibit is low, all channel outputs are nonconductive (transistors biased to cut-off). This minimizes loading in party-line systems where a large number of drivers share the same line.

- Four Independent Drivers with Common Inhibit Input
- -3.0 Volts Output Common-Mode Voltage Over Entire Operating Range
- Improved Driver Design Exceeds Performance of Popular SN75110

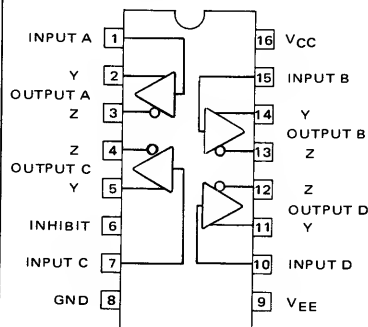
QUAD LINE DRIVER WITH COMMON INHIBIT INPUT SILICON MONOLITHIC INTEGRATED CIRCUIT



**FIGURE 1 - PARTY-LINE DATA TRANSMISSION SYSTEM WITH
MULTIPLEX DECODING**



PIN CONNECTIONS



TRUTH TABLE (positive logic)

Logic Input	Inhibit Input	Output Current	
		Z	Y
H	H	On	Off
L	H	Off	On
H	L	Off	Off
L	L	Off	Off

L = Low Logic Level
H = High Logic Level

MC3453

MAXIMUM RATINGS ($T_A = 0$ to $+70^\circ\text{C}$ unless otherwise noted.)

Ratings	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+7.0 -7.0	Volts
Logic and Inhibitor Input Voltages	V_{in}	5.5	Volts
Common-Mode Output Voltage Range	V_{OCR}	-5.0 to +12	Volts
Power Dissipation (Package Limitation) Plastic and Ceramic Dual In-Line Packages Derate above $T_A = +25^\circ\text{C}$	P_D	1000 6.6	mW mW/ $^\circ\text{C}$
Operating Ambient Temperature Range	T_A	0 to $+70$	$^\circ\text{C}$
Storage Temperature Range Plastic and Ceramic Dual In-Line Packages	T_{stg}	-65 to +150	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS (See Notes 1 and 2.)

Characteristic	Symbol	Min	Nom	Max	Unit
Power Supply Voltages	V_{CC} V_{EE}	+4.75 -4.75	+5.0 -5.0	+5.25 -5.25	Volts
Common-Mode Output Voltage Range Positive Negative	V_{OCR}	0 0	— —	+10 -3.0	Volts

Notes: 1. These voltage values are in respect to the ground terminal.
2. When not using all four channels, unused outputs **must** be grounded.

DEFINITIONS OF INPUT LOGIC LEVELS*

Characteristic	Symbol	Min	Max	Unit
High-Level Input Voltage (at any input)	V_{IH}	2.0	5.5	Volts
Low-Level Input Voltage (at any input)	V_{IL}	0	0.8	Volts

*The algebraic convention, where the most positive limit is designated maximum, is used with Logic Level Input Voltage Levels only.

ELECTRICAL CHARACTERISTICS ($T_A = 0$ to $+70^\circ\text{C}$ unless otherwise noted.)

Characteristic#	Symbol	Min	Typ#	Max	Unit
High-Level Input Current (Logic Inputs) ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$, $V_{IH} = 2.4 \text{ V}$) ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$, $V_{IH} = V_{CC} \text{ Max}$)	I_{IHL}	— —	— —	40 1.0	μA mA
Low-Level Input Current (Logic Inputs) ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$, $V_{IL} = 0.4 \text{ V}$)	I_{ILL}	—	—	-1.6	mA
High-Level Input Current (Inhibit Input) ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$, $V_{IH} = 2.4 \text{ V}$) ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$, $V_{IH} = V_{CC} \text{ Max}$)	I_{IHl}	— —	— —	40 1.0	μA mA
Low-Level Input Current (Inhibit Input) ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$, $V_{IL} = 0.4 \text{ V}$)	I_{ILl}	—	—	-1.6	mA
Output Current ("on" state) ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$) ($V_{CC} = \text{Min}$, $V_{EE} = \text{Min}$)	$I_{O(on)}$	— 6.5	11 11	15 —	mA
Output Current ("off" state) ($V_{CC} = \text{Min}$, $V_{EE} = \text{Min}$)	$I_{O(off)}$	—	5.0	100	μA
Supply Current from V_{CC} (with driver enabled) ($V_{IL} = 0.4 \text{ V}$, $V_{IH} = 2.0 \text{ V}$)	$I_{CC(on)}$	—	35	50	mA
Supply Current from V_{EE} (with driver enabled) ($V_{IL} = 0.4 \text{ V}$, $V_{IH} = 2.0 \text{ V}$)	$I_{EE(on)}$	—	65	90	mA
Supply Current from V_{CC} (with driver inhibited) ($V_{IL} = 0.4 \text{ V}$, $V_{IH} = 0.4 \text{ V}$)	$I_{CC(off)}$	—	35	50	mA
Supply Current from V_{EE} (with driver inhibited) ($V_{IL} = 0.4 \text{ V}$, $V_{IH} = 0.4 \text{ V}$)	$I_{EE(off)}$	—	25	40	mA

#All typical values are at $V_{CC} = +5.0 \text{ V}$, $V_{EE} = -5.0 \text{ V}$, $T_A = +25^\circ\text{C}$.

#For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable device type.

Ground unused inputs and outputs.

MC3453

SWITCHING CHARACTERISTICS ($V_{CC} = +5.0\text{ V}$, $V_{EE} = -5.0\text{ V}$, $T_A = +25^\circ\text{C}$.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time from Logic Input to Output Y or Z ($R_L = 50\text{ ohms}$, $C_L = 40\text{ pF}$)	t_{PLH_L} t_{PHL_L}	—	9.0 9.0	17 17	ns
Propagation Delay Time from Inhibit Input to Output Y or Z ($R_L = 50\text{ ohms}$, $C_L = 40\text{ pF}$)	t_{PLH_I} t_{PHL_I}	—	16 20	25 25	ns

FIGURE 2 — LOGIC INPUT TO OUTPUTS PROPAGATION DELAY TIME WAVEFORMS

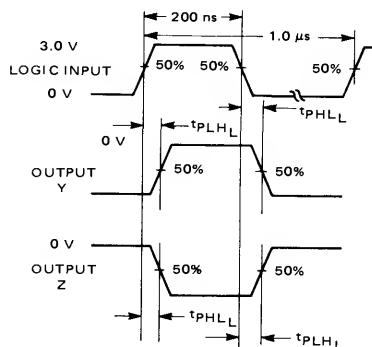
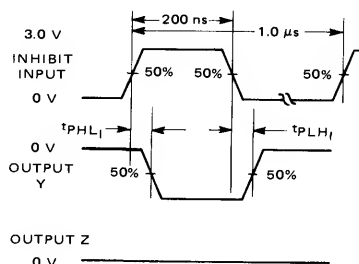
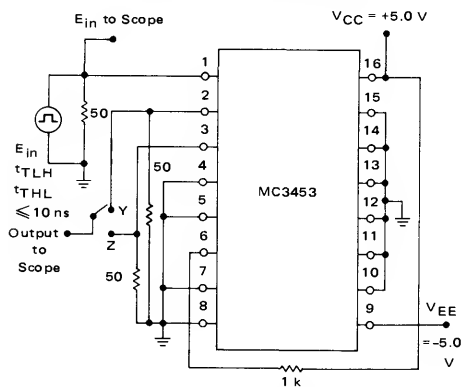


FIGURE 3 — INHIBIT INPUT TO OUTPUTS PROPAGATION DELAY TIME WAVEFORMS



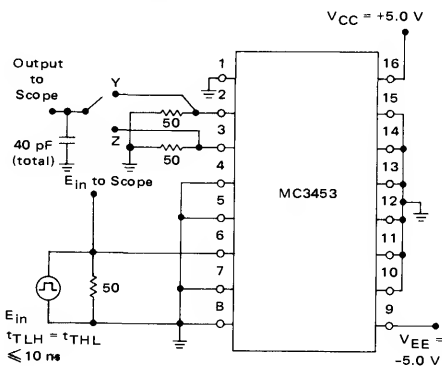
TEST CIRCUITS

FIGURE 4 — LOGIC INPUT TO OUTPUT PROPAGATION DELAY TIME TEST CIRCUIT



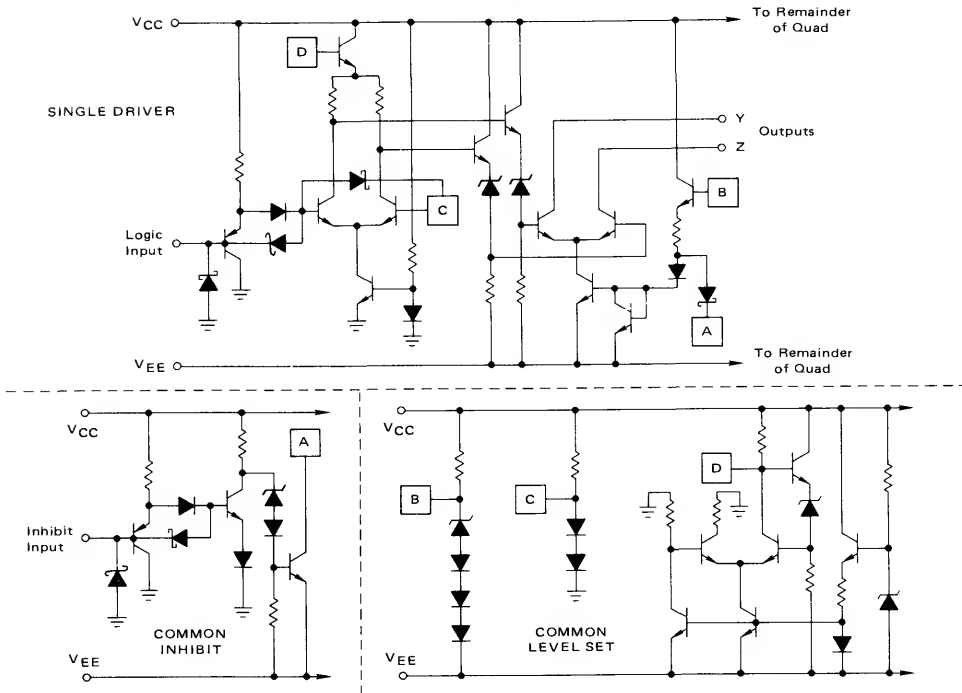
Channel A shown under test, the other channels are tested similarly.

FIGURE 5 — INHIBIT INPUT TO OUTPUT PROPAGATION DELAY TIME TEST CIRCUIT



Channel A shown under test, the other channels are tested similarly.

FIGURE 6 – CIRCUIT SCHEMATIC
(1/4 Circuit Shown)



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

MC3467

TRIPLE WIDEBAND PREAMPLIFIER WITH ELECTRONIC GAIN CONTROL (EGC)

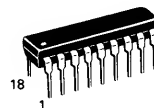
The MC3467 provides three independent preamplifiers with individual electronic gain control in a single 18-pin package. Each preamplifier has differential inputs and outputs allowing operation in completely balanced systems. The device is optimized for use in 9-track magnetic tape memory systems where low noise and low distortion are paramount objectives.

The electronic gain control allows each amplifier's gain to be set anywhere from essentially zero to a maximum of approximately 100 V/V.

- Wide Bandwidth – 15 MHz (Typ)
- Individual Electronic Gain Control
- Differential Input/Output

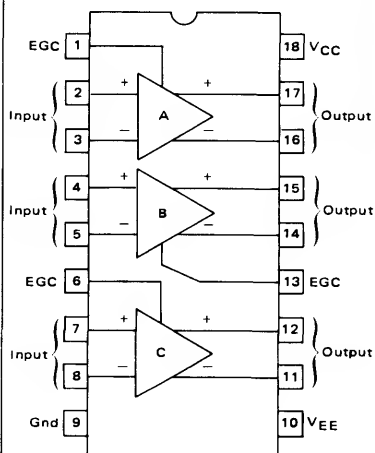
TRIPLE MAGNETIC TAPE MEMORY PREAMPLIFIER

SILICON MONOLITHIC
INTEGRATED CIRCUIT

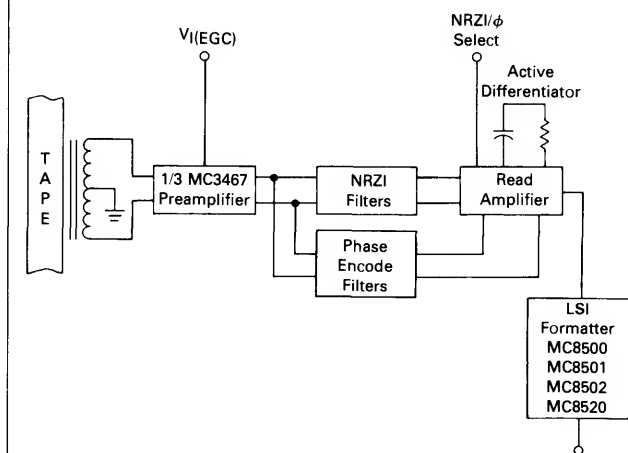


P SUFFIX
PLASTIC PACKAGE
CASE 707

PIN CONNECTIONS



TYPICAL APPLICATION HIGH PERFORMANCE 9-TRACK OPEN REEL TAPE SYSTEM



MC3467

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltages			V
Positive Supply Voltage	V _{CC}	6.0	
Negative Supply Voltage	V _{EE}	-9.0	
EGC Voltages (Pins 1, 6 and 13)	V _I (EGC)	-5.0 to V _{CC}	V
Input Differential Voltage	V _{ID}	±5.0	V
Input Common-Mode Voltage	V _{IC}	±5.0	V
Amplifier Output Short Circuit Duration (to Ground)	t _{sc}	10	s
Operating Ambient Temperature Range	T _A	0 to +70	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C
Junction Temperature	T _J	+150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = -6.0 V, f = 100 kHz, T_A = 0 to +70°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage Range					
Positive Supply Voltage	V _{CCR}	4.75	5.0	5.25	V
Negative Supply Voltage	V _{EE}	-5.5	-6.0	-7.0	V
Operating EGC Voltage	V _I (EGC)	0	—	V _{CC}	V
Differential Voltage Gain (Balanced) (V _I (EGC) = 0, e _i = 25 mVp-p) (See Figure 1)	A _{VD}	85	100	120	V/V
Differential Voltage Gain (V _I (EGC) = V _{CC})	A _{VD}	—	0.5	2.0	V/V
Maximum Input Differential Voltage (Balanced) (T _A = 25°C)	V _{IDR}	0.2	—	—	V _{pp}
Output Voltage Swing (Balanced) (Figure 1) (e _i = 200 mVp-p)	V _{OR}	6.0	8.0	—	V _{pp}
Input Common-Mode Range	V _{ICR}	±1.5	±2.0	—	V
Differential Output Offset Voltage (T _A = 25°C)	V _{OOD}	—	500	—	mV
Common-Mode Output Offset Voltage (T _A = 25°C)	V _{OOC}	—	500	—	mV
Common Mode Rejection Ratio (Figure 2) V _I (EGC) = 0, V _{CM} = 1.0 V _{pp} (f = 100 kHz) (f = 1.0 MHz)	CMRR	60 40	100 100	— —	dB
Small-Signal Bandwidth (Figure 1) (-3.0 dB, e _i = 1.0 mVp-p, T _A = 25°C)	BW	10	15	—	MHz
Input Bias Current	I _{IB}	—	5.0	15	μA
Output Sink Current (Figure 5)	I _{OS}	1.0	1.4	—	mA
Differential Noise Voltage Referred to Input (Figure 3) (V _I (EGC) = 0, R _S = 50 Ω, BW = 10 Hz to 1.0 MHz, T _A = 25°C)	e _n	—	3.5	—	μV _{RMS}
Positive Power Supply Current (Figure 4)	I _{CC}	—	30	40	mA
Negative Power Supply Current (Figure 4)	I _{EE}	—	-30	-40	mA
Input Resistance (T _A = 25°C)	r _i	12	25	—	kΩ
Input Capacitance (T _A = 25°C)	C _i	—	2.0	—	pF
Output Resistance (Unbalanced) (T _A = 25°C)	r _o	—	30	—	Ohms

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MC3467

FIGURE 1 – DIFFERENTIAL VOLTAGE GAIN, BANDWIDTH AND OUTPUT VOLTAGE SWING TEST CIRCUIT
(Channel A under test, other channels tested similarly)

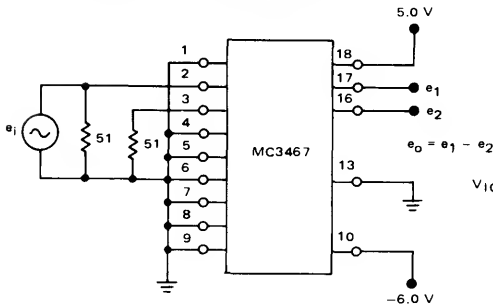


FIGURE 2 – COMMON-MODE REJECTION RATIO
(Channel A under test, other amplifiers tested similarly)

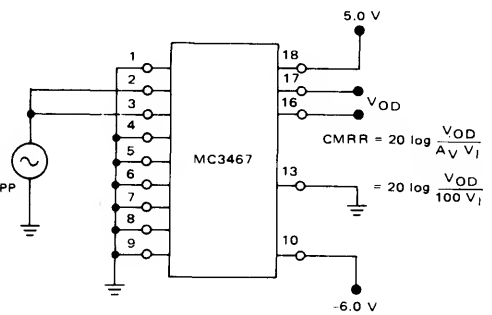


FIGURE 3 – DIFFERENTIAL NOISE VOLTAGE REFERRED TO THE INPUT

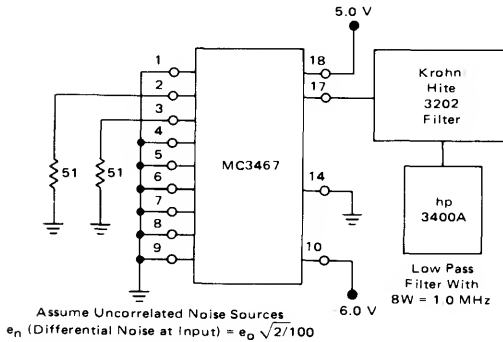


FIGURE 4 – POWER SUPPLY CURRENT TEST CIRCUIT

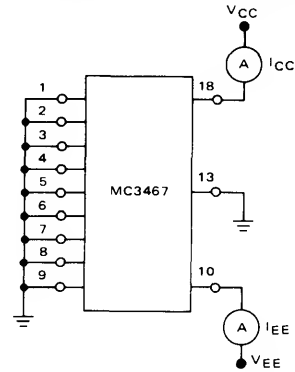


FIGURE 5 – OUTPUT SINK CURRENT TEST CIRCUIT
(Channel A under test, other channels tested similarly)

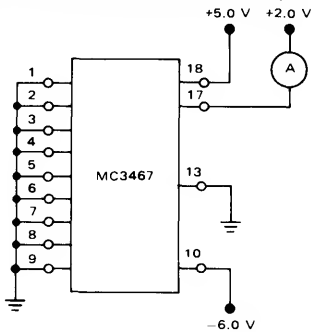
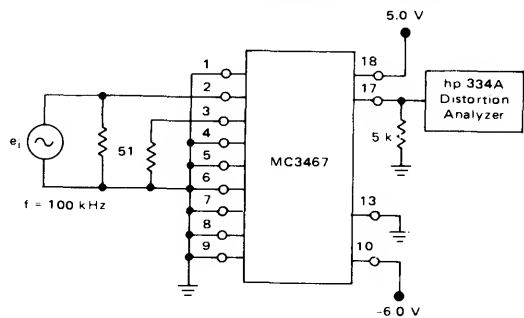
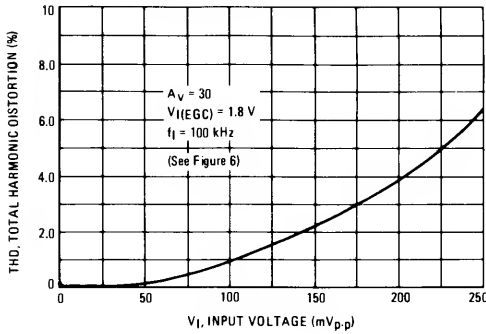


FIGURE 6 – TOTAL HARMONIC DISTORTION TEST CIRCUIT
(Channel A under test, other channels tested similarly)

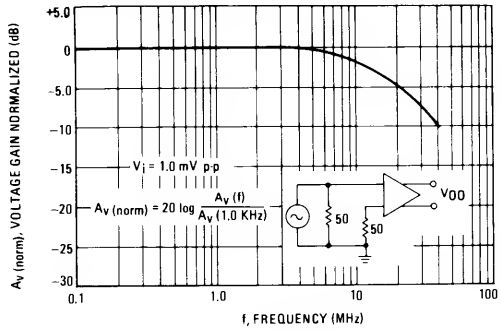


TYPICAL CHARACTERISTICS
 $(V_{CC} = 5.0 \text{ V}, V_{EE} = -6.0 \text{ V}, T_A = 25^\circ \text{ unless otherwise noted})$

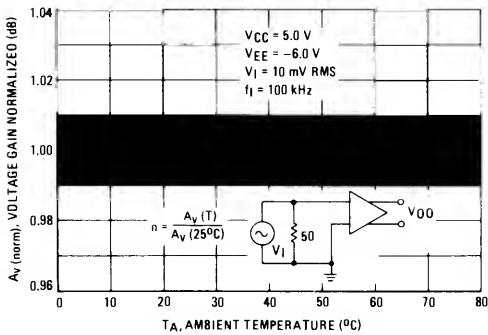
**FIGURE 7 – TOTAL HARMONIC DISTORTION (THD)
versus INPUT VOLTAGE**



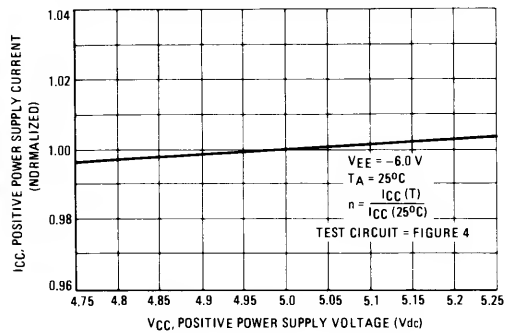
**FIGURE 8 – NORMALIZED VOLTAGE GAIN
versus FREQUENCY**



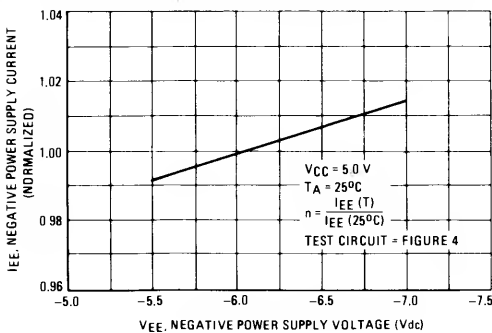
**FIGURE 9 – NORMALIZED VOLTAGE GAIN
versus AMBIENT TEMPERATURE**



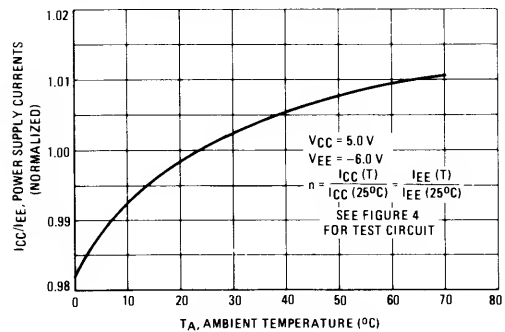
**FIGURE 10 – NORMALIZED POSITIVE POWER SUPPLY
CURRENT versus POSITIVE POWER SUPPLY VOLTAGE**



**FIGURE 11 – NORMALIZED NEGATIVE POWER SUPPLY
CURRENT versus NEGATIVE POWER SUPPLY VOLTAGE**



**FIGURE 12 – NORMALIZED POWER SUPPLY CURRENTS
versus AMBIENT TEMPERATURE**



MC3467

FIGURE 13 – DIFFERENTIAL VOLTAGE GAIN versus ELECTRONIC GAIN CONTROL VOLTAGE ($V_{I(EGC)}$)

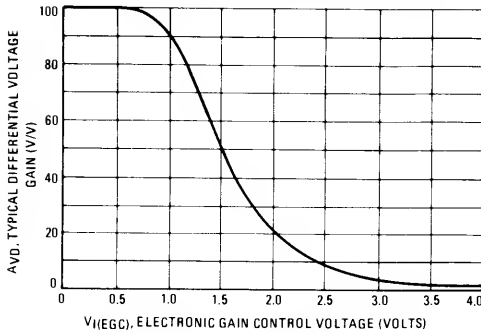


FIGURE 14 – COMMON-MODE REJECTION RATIO (CMRR) versus FREQUENCY

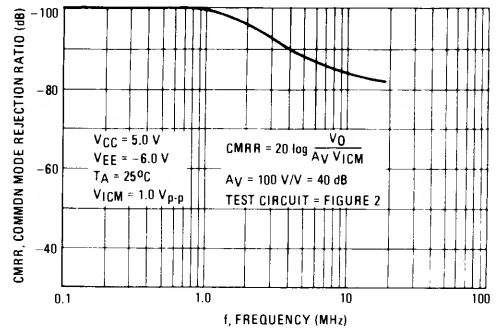


FIGURE 15 – PHASE SHIFT versus FREQUENCY

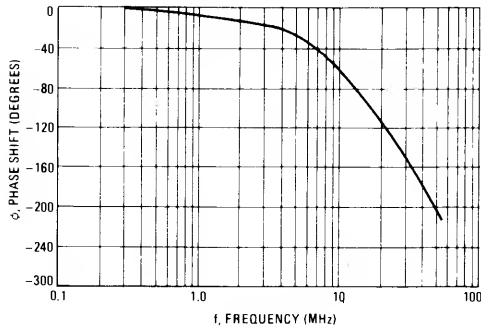
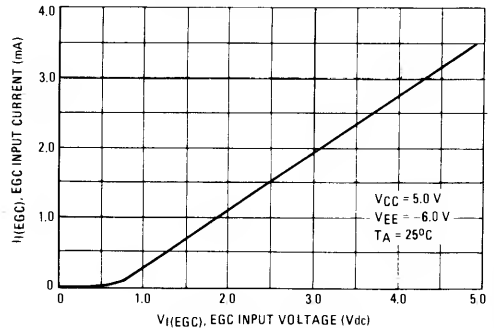
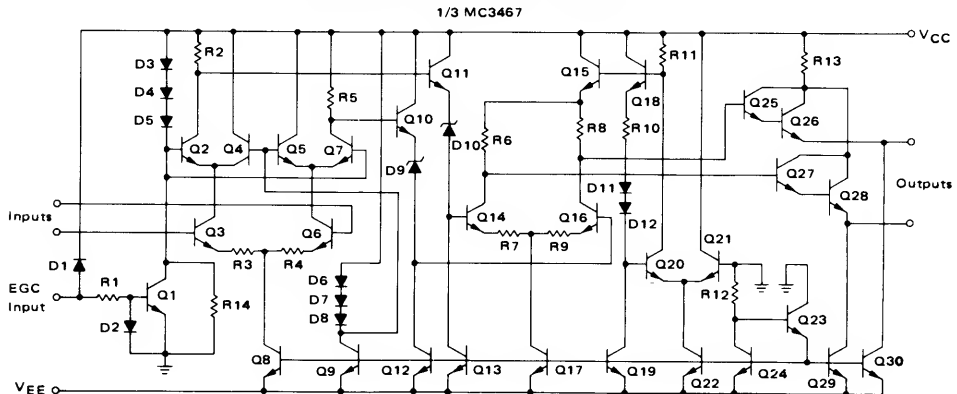


FIGURE 16 – TYPICAL EGC INPUT CURRENT versus EGC INPUT VOLTAGE



REPRESENTATIVE CIRCUIT SCHEMATIC



FLOPPY DISK WRITE CONTROLLER

The MC3469 is a monolithic WRITE Current Controller designed to provide the entire interface between floppy disk heads and the head control and write data signals for straddle-erase heads.

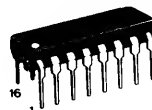
Provisions are made for selecting a range of accurately controlled write currents and for head selection during both read and write operation. Additionally, provisions are included for externally adjusting degauss period and inner/outer track compensation.

- Head Selection — Current Steering Through Write Head and Erase Coil in Write Mode
- Provides High Impedance (Read Data Enable) During Read Mode
- Head Current (Write) Guaranteed Using Laser Trimmed Internal Resistor (3.0 mA using $R_{ext} = 10\text{ k}\Omega$)
- IRW Select Input Provides for Inner/Outer Track Compensation
- Degauss Period Externally Adjustable
- Specified With $\pm 10\%$ Logic Supply and Head Supply (V_{BB}) from 10.8 V to 26.4 V
- Minimizes External Components
- See Application Note AN917 for Further Information

MC3469P

FLOPPY DISK WRITE CONTROLLER

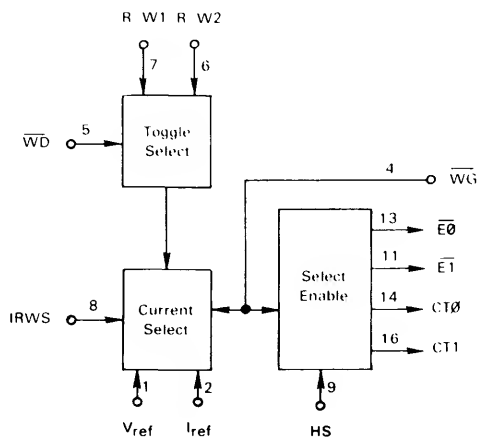
SILICON MONOLITHIC
INTEGRATED CIRCUIT



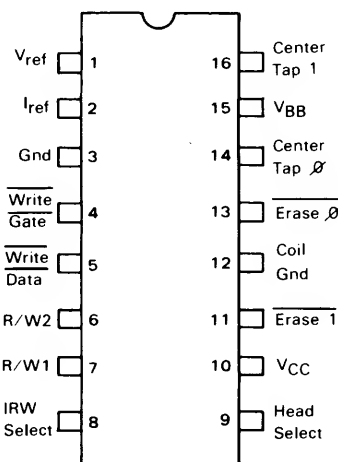
P SUFFIX
PLASTIC PACKAGE
CASE 648

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BLOCK DIAGRAM



PIN CONNECTIONS



MC3469P

MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 10)	V _{CC}	7.0	Vdc
Power Supply Voltage (Pin 15)	V _{BB}	30	Vdc
Input Voltage (Pins 4, 5, 8, 9)	V _I	5.75	Vdc
Storage Temperature	T _{stg}	-55 to +150	°C
Operating Junction Temperature	T _J	150	°C

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 10)	V _{CC}	+4.5 to +5.5	Vdc
Power Supply Voltage (Pin 15)	V _{BB}	+10.8 to +26.4	Vdc
Operating Ambient Temperature Range	T _A	0 to +70	°C

ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = 4.5 to 5.5 V, V_{BB} = 10.8 to 26.4 V unless otherwise noted. Typicals given for V_{CC} = 5.0 V, V_{BB} = 12 V and T_A = 25°C unless otherwise noted.)

Characteristics	Pins	Symbol	Min	Typ	Max	Unit
-----------------	------	--------	-----	-----	-----	------

DIGITAL INPUT VOLTAGES

Power Supply Current — V _{CC} V _{BB}		I _{CC} I _{BB}	— —	22 15	50 30	mA
High Level Input Voltage (V _{CC} = 4.5 V)	4, 8, 9	V _{IH}	2.0	—	—	V
Low Level Input Voltage (V _{CC} = 5.5 V)	4, 8, 9	V _{IL}	—	—	0.8	V
Input Clamp Voltage (I _{IK} = -12 mA)	4, 5, 8, 9	V _{IK}	—	-0.87	-1.5	V
Positive Threshold (V _{CC} = 5.0)	5	V _{T(+)}	1.5	1.75	2.0	V
Negative Threshold (V _{CC} = 5.0)	5	V _{T(-)}	0.7	0.98	1.3	V
Hysteresis (V _{T(+)} - V _{T(-)}) T _A = 0°C to +70°C T _A = 25°C		V _{HTS}	0.2 0.4	— 0.76	— —	V

DIGITAL INPUT CURRENTS

High Level Input Current (V _{CC} = 5.5 V, V _{BB} = 26.4 V, V _I = 2.4 V)	4, 5, 8, 9	I _{IH}	—	0.1	40	μA
Low Level Input Current (V _{CC} = 5.5 V, V _{BB} = 26.4 V, T _A = 25°C unless noted below)	4, 5, 8, 9	I _{IL}	—	—	-1.6	mA
V _{BB} = 12 V	4		—	0.36	—	
V _{BB} = 24 V	4		—	0.76	—	
V _{CC} = 5.0 V	5		—	0.46	—	
V _{CC} = 5.0 V	8, 9		—	0.39	—	

MC3469P

ELECTRICAL CHARACTERISTICS (continued) ($T_A = 0$ to $+70^\circ\text{C}$, $V_{CC} = 4.5$ to 5.5 V, $V_{BB} = 10.8$ to 26.4 V unless otherwise noted. Typicals given for $V_{CC} = 5.0$ V, $V_{BB} = 12$ V and $T_A = 25^\circ\text{C}$ unless otherwise noted.)

Characteristics	Pins	Symbol	Min	Typ	Max	Unit
CENTER-TAP and ERASE OUTPUTS						
Output High Voltage (See Figure 9) ($I_{OH} = -100$ mA, $V_{CC} = 4.5$ V) $V_{BB} = 10.8$ to 26.4 V	14, 16	V_{OH}	$V_{BB} - 1.5$	$V_{BB} - 1.0$	—	V
Output Low Voltage (See Figure 9) ($I_{OL} = 1.0$ mA) $V_{BB} = 12$ V $V_{BB} = 24$ V	14, 16	V_{OL}	— —	70 70	150 150	mV
Output High Leakage ($V_{OH} = 24$ V, $V_{CC} = 4.5$ V, $V_{BB} = 24$ V)	11, 13	I_{OH}	—	0.01	100	μA
Output Low Voltage (See Figure 10) ($I_{OL} = 90$ mA, $V_{CC} = 4.5$ V) $V_{BB} = 12$ V $V_{BB} = 24$ V	11, 13	V_{OL}	— —	0.27 0.27	0.60 0.60	V

CURRENT SOURCE

Reference Voltage	1	V_{ref}	—	5.7	—	V
Degauss Voltage (See Text) (Voltage Pin 1 – Voltage Pin 2)	1	V_{DEG}	—	1.0	—	V
Bias Voltage	2	V_F	—	0.7	—	V
Write Current Off Leakage ($V_{OH} = 35$ V)	6, 7	I_{OH}	—	0.03	15	μA
Saturation Voltage ($V_{BB} = 12$ V)	6, 7	V_{sat}	—	0.85	2.7	V
Current Sink Compliance (For $V_6, 7 = 4.0$ V to 24 V, $V_{WG} = 0.8$ V)	6, 7	$\Delta I / RW2, 1$	—	15	40	μA
Average Value Write Current ($(I_{Pin 6} + I_{Pin 7}) / 2$ for $V_{BB} = 10.8$ to 26.4 V) @ $I_R / W = I_{LOW}$, $R = 10$ k $T_A = 25^\circ\text{C}$ $T_A = 0$ to $+70^\circ\text{C}$ @ $I_R / W = I_{LOW}$, $R = 5.0$ k $T_A = 25^\circ\text{C}$ $T_A = 0$ to $+70^\circ\text{C}$ @ $I_R / W = I_{HI}$, $R = 10$ k ($I_{HI} = I_{LOW} + \% I_{LOW}$) $T_A = 25^\circ\text{C}$ $T_A = 0$ to $+70^\circ\text{C}$	6, 7	$I_R / W(L)$ $\Delta I_R / W(H)$	2.91 2.84 5.64 5.51 31.3 30.3	3.0 — 5.89 — 33.3 33.3	3.09 3.16 6.14 6.28 35.5 36.6	mA %
Difference in Write Current ($ I_{Pin 6} - I_{Pin 7} $) @ $I_R / W = I_{LOW}$, $V_{BB} = 10.8$ V to 26.4 V $R = 10$ k $T_A = 25^\circ\text{C}$ $T_A = 0$ to $+70^\circ\text{C}$ $R = 5.0$ k $T_A = 25^\circ\text{C}$ $T_A = 0$ to $+70^\circ\text{C}$	6, 7	$I_R / W \Delta$	— — — —	0.003 — — —	0.015 0.023 0.030 0.046	mA

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MC3469P

AC SWITCHING CHARACTERISTICS ($V_{CC} = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$, $V_{BB} = 24\text{ V}$, $I_{RWS} = 0.4$ and $I_{R/W} = 3.0\text{ mA}$ unless otherwise noted — refer to Figure 2 and Figure 11.)

Characteristics (Note 1)	f_{in} (Note 3)	Min	Typ	Max	Unit
1. Delay from Head Select going low through 0.8 V to CT0 going high through 20 V.	HS, Pin 9	—	1.6	4.0	μS
2. Delay from Head Select going low through 0.8 V to CT1 going low through 1.0 V.	HS, Pin 9	—	2.1	4.0	μS
3. Delay from Head Select going high through 2.4 V to CT0 going low through 1.0 V.	HS, Pin 9	—	1.7	4.0	μS
4. Delay from Head Select going high through 2.4 V to CT1 going high through 20 V.	HS, Pin 9	—	1.4	4.0	μS
5. Delay from \overline{WG} going low through 0.8 V to CT0 going low through 1.0 V.	\overline{WG} , Pin 4	—	1.3	4.0	μS
6. Delay from \overline{WG} going low through 0.8 V to CT1 going high through 20 V.	\overline{WG} , Pin 4	—	0.8	4.0	μS
7. Delay from \overline{WG} going low through 0.8 V to CT0 going high through 20 V.	\overline{WG} , Pin 4	—	0.75	4.0	μS
8. Delay from \overline{WG} going low through 0.8 V to CT1 going low through 1.0 V.	\overline{WG} , Pin 4	—	1.2	4.0	μS
9. After \overline{WG} goes high, delay from R/W1 turning off through 10% to CT0 going high through 20 V.	\overline{WG} , Pin 4	20	750	—	ns
10. After \overline{WG} goes high, delay from R/W1 turning off through 10% to CT1 going low through 1.0 V.	\overline{WG} , Pin 4	20	1200	—	ns
11. After \overline{WG} goes high, delay from R/W2 turning off through 10% to CT0 going low through 1.0 V.	\overline{WG} , Pin 4	20	1200	—	ns
12. After \overline{WG} goes high, delay from R/W2 turning off through 10% to CT1 going high through 20 V.	\overline{WG} , Pin 4	20	600	—	ns
13. Delay from \overline{WG} going low through 0.8 V to $\overline{E0}$ going low through 1.0 V.	\overline{WG} , Pin 4	—	0.085	4.0	μS
14. Delay from \overline{WG} going low through 0.8 V to $\overline{E1}$ going low through 1.0 V.	\overline{WG} , Pin 4	—	0.085	4.0	μS
15. Delay from \overline{WG} going high through 2.0 V to $\overline{E0}$ going high through 23 V.	\overline{WG} , Pin 4	—	0.7	4.0	μS
16. Delay from \overline{WG} going high through 2.0 V to $\overline{E1}$ going high through 23 V.	\overline{WG} , Pin 4	—	0.7	4.0	μS
17. After \overline{WG} goes low, delay from CT0 going low through 1.0 V to R/W1 turning on through 10%.	\overline{WG} , Pin 4	20	750	—	ns
18. After \overline{WG} goes low, delay from CT1 going low through 1.0 V to R/W2 turning on through 10%.	\overline{WG} , Pin 4	20	750	—	ns
19. After \overline{WG} goes low, fall time (10% to 90%) of R/W1.	\overline{WG} , Pin 4	—	5.0	200	ns
20. After \overline{WG} goes low, fall time (10% to 90%) of R/W2.	\overline{WG} , Pin 4	—	5.0	200	ns
21. Setup time, Head Select going low before \overline{WG} going low	\overline{WG} , Pin 4	4.0	—	—	μS
22. Write Data low Hold Time	\overline{WD} , Pin 5	200	—	—	ns
23. Write Data high Hold Time	\overline{WD} , Pin 5	500	—	—	ns
24. Delay from \overline{WG} going high through 2.0 V to R/W1 turning off through 10% of on value.	\overline{WG} , Pin 4	—	3.9	—	μS

- Notes 1. Test numbers refer to encircled numbers in Figure 2.
2. AC test waveforms applied to the designated pins as follows:

Pin	f_{in}	Amplitude	Duty Cycle
HS, Pin 9	50 kHz	0.4 to 2.4 V	50%
\overline{WG} , Pin 4	50 kHz	0.4 to 2.4 V	50%
\overline{WD} , Pin 5	1.0 MHz	0.2 to 2.4 V	50%

3. Test numbers refer to encircled numbers in Figure 4.
 $f_{in} = 1.0\text{ MHz}$, 50% Duty Cycle and Amplitude of 0.2 V to 2.4 V.

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AC SWITCHING CHARACTERISTICS (continued)

($V_{CC} = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$, $V_{BB} = 24\text{ V}$, $\overline{W}\overline{G} = 0.4$ unless otherwise noted — refer to Figure 3 and Figure 11.)

Characteristics (Note 3)	Min	Typ	Max	Unit
1. Delay from Write Data going low through 0.9 V to R/W1 turning on through 50%.	—	85	—	ns
2. Delay skew, difference of R/W1 turning off and R/W2 turning on through 50% after Write Data going low through 0.9 V.	—	1.0	± 40	ns
3. Delay from Write Data going low through 0.9 V to R/W1 turning off through 50%.	—	80	—	ns
4. Delay skew, difference of R/W1 turning on and R/W2 turning off 50% after Write Data going low through 0.9 V.	—	1.0	± 40	ns
5. Rise time, 10% to 90%, of R/W1	—	1.7	200	ns
6. Rise time, 10% to 90%, of R/W2	—	1.7	200	ns
7. Fall time, 90% to 10%, of R/W1	—	12	200	ns
8. Fall time, 90% to 10%, of R/W2	—	12	200	ns

PIN DESCRIPTION TABLE

Name	Symbol	Pin	Description
Head Select	HS	9	Head Select input selects between the head I/O pins: center-tap, erase, and read/write. A HIGH selects Head 0 and a LOW selects Head 1.
Write Gate	$\overline{W}\overline{G}$	4	Write Gate input selects the mode of operation. HIGH selects the read mode, while LOW selects the Write Control mode and forces the write current.
Write Data	$\overline{W}\overline{D}$	5	Write Data input controls the turn on/off of the write current. The internal divide-by-two flip-flop toggles on the negative going edge of this input to direct the current alternately to the two halves of the head coils.
IRW Select	IRWS	8	IRW Select input selects the amount of write current to be used. When LOW, the current equals the value found in Figure 5, according to the external resistor. When HIGH, the current equals the low current + 33%.
V_{ref} I_{ref}	V_{ref} I_{ref}	1 2	A resistor between these pins sets the write current. Laser trimming reliably produces 3 mA of current for a 10 k resistor. A capacitor from V_{ref} to Gnd will adjust the Degauss period.
Center-tap 0	CT0	14	Center-tap 0 output is connected to the center tap of Head 0. It will be pulled to Gnd or V_{BB} (+12 or +24) depending on mode and head selection.
Erase 0	$\overline{E}0$	13	Erase 0 will be LOW for writing on Head 0, and floating for other conditions.
Center-tap 1	CT1	16	Center-tap 1 output is connected to the center tap of Head 1. It will be pulled to Gnd or V_{BB} (+12 or +24) depending on mode and head selection.
Erase 1	$\overline{E}1$	11	Erase 1 will be LOW for writing on Head 1, and floating for other conditions.
R/W2	R/W2	6	R/W2 input is one of the differential inputs that sinks current during writing, being the opposite phase of R/W1. It will be connected to one side of the heads.
R/W1	R/W1	7	R/W1 input is one of the differential inputs that sinks current during writing, being the opposite phase of R/W2. It will be connected to one side of the heads.
	V_{CC}	10	+5 V Power
	V_{BB}	15	+12 V or +24 V Power
	Gnd	12	Coil grounds
	Gnd	3	Reference and logic ground

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FIGURE 1 — LOGIC DIAGRAM

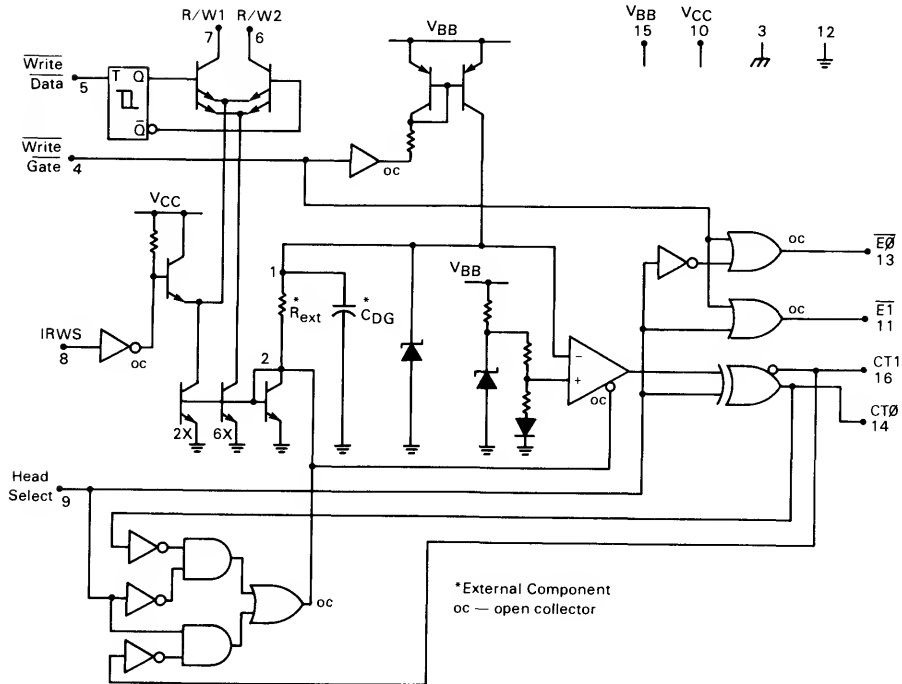
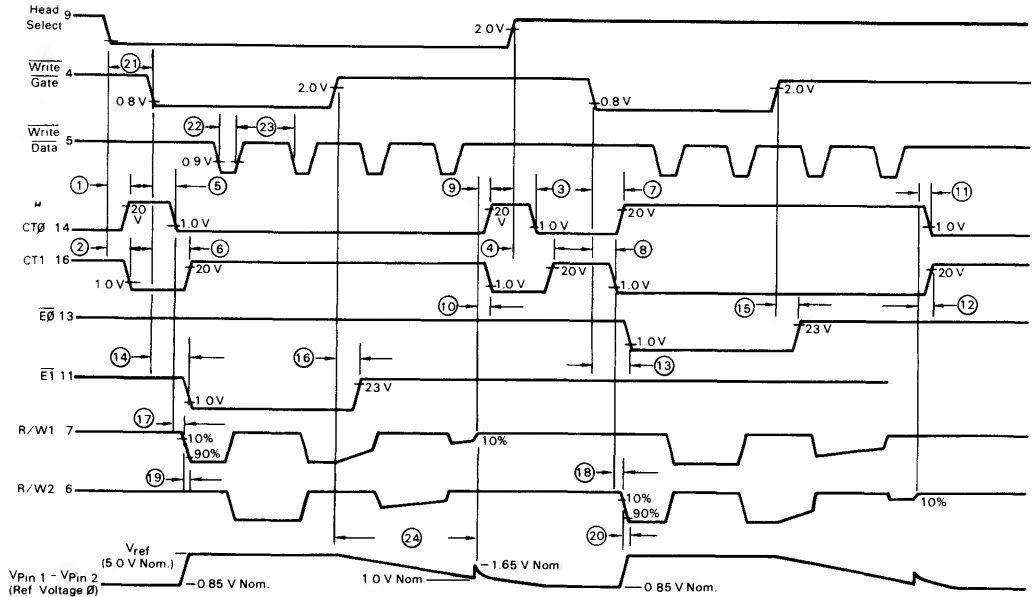
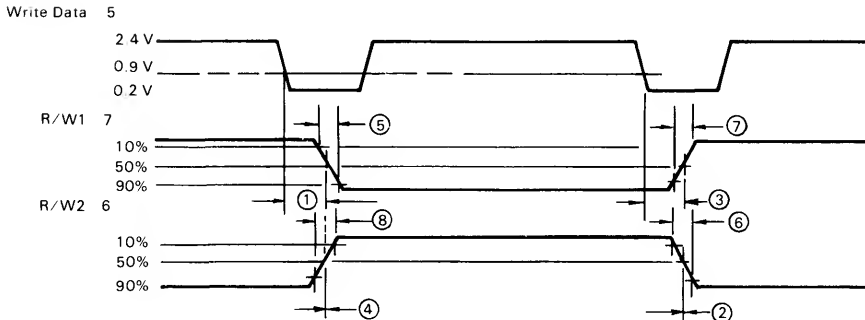


FIGURE 2 — AC TIMING DIAGRAM



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FIGURE 3 — R/W1 AND R/W2 RELATIONSHIP



APPLICATION INFORMATION

The MC3469P serves as a complete interface between the Write Control functional signals (Head Select, Write Data, Write Gate and inner track compensation, IRWS) and the head itself. A typical configuration is shown in Figure 4. L_E 's are erase coils.

WRITE CURRENT SELECTION

Although the MC3469P has been specified for 3.0 mA write current (with a 10 k Ω external resistor), a range of write current values can be chosen by varying R_{ext} using the plot in Figure 5. This current can also be derived using

$$\text{the relationship } I_{Write} \text{ (mA)} = \frac{30}{R_{ext} \text{ (k}\Omega\text{)}}$$

I_{Ref} , the current flowing in R_{ext} (required only for dissipation calculations) can be worst case using the fact that the differential voltage between Pins 1 and 2 (V_{Ref}) shown in Figure 3 never exceeds 5.0 volts. With a low value of $R_{ext} = 1.0 \text{ k}\Omega$, $P_D = 25 \text{ mW}$.

WRITE CURRENT DAMPING

Referring to Figure 4, resistors R_D are used to dampen any ringing that results from applying the relatively fast risetime write current pulse to the inductive head load. Values chosen will be a function of head characteristics and the desired damping. R_p serves as a common pullup resistor to the head supply V_{BB} .

FIGURE 4 — TYPICAL APPLICATION

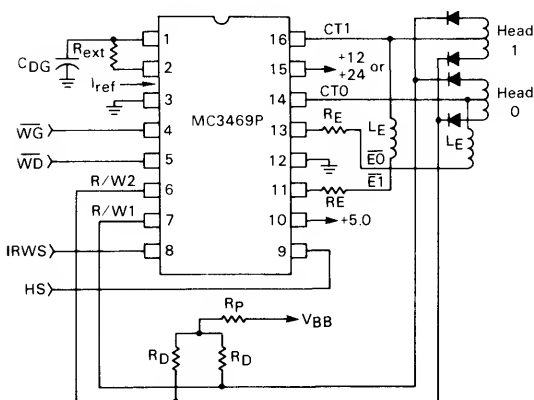
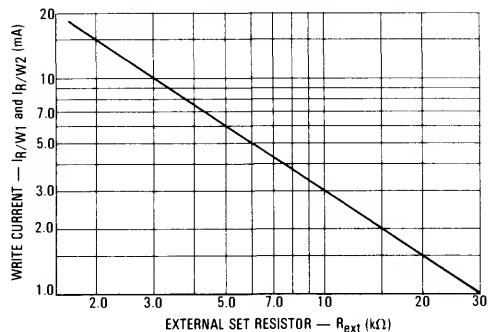


FIGURE 5 — WRITE CURRENT versus R_{ext}



DEGAUSS PERIOD

Degauss of the read/write head can be accomplished at the end of each write operation by attaching a capacitor from pin 1 to ground. The timing relationship that results is shown in Figure 7. A simplified diagram of this function is shown in Figure 6.

While \overline{WG} is low, the selected write current flows into pin 6 or pin 7 (R/W1 or R/W2) and is mirrored through the external resistor, R_{ext} . The degauss capacitor, C_{DG} , will be charged to approximately 5.7 volts. After \overline{WG} goes high, the voltage on C_{DG} begins to decay toward 0.7 V. When the voltage reaches the comparator threshold of 1.7 V, the comparator output triggers the internal logic to completely turn off the write current. At this point, the pulse amplitude on the R/W1 and R/W2 pins has returned to 10% of its maximum value.

Figure 7, Degauss Period shows the relationship be-

tween C_{DG} and Degauss Period for $R_{ext} = 10\text{ k}\Omega$. This period is equal to the exponential delay time for the voltage as mentioned plus some internal delay times.

POWER-UP WRITE CURRENT CONTROL

During power-up, under certain conditions (V_{BB} comes up first while \overline{WG} is low), there can be a write current transient on Pins 6 and 7 (R/W1 and R/W2) of sufficient magnitude to cause writing to occur if the head is loaded.

This transient can be eliminated by placing a capacitor from Pin 2 to ground. This also delays the write current when \overline{WG} goes low and this delay must be accounted for when the capacitor on Pin 2 is used. The delay is $3.0\text{ }\mu\text{s}$ for a 2700 pF capacitor, and $R_{ext} = 10\text{ k}\Omega$. Values up to 7000 pF may be used.

FIGURE 6 — SIMPLIFIED DEGAUSS CIRCUIT

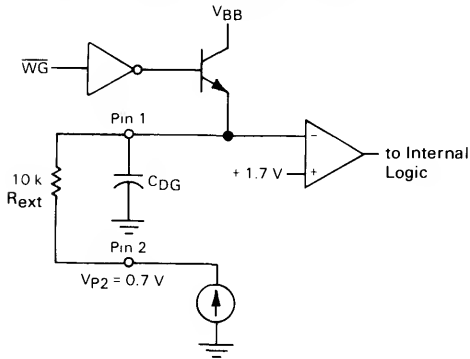
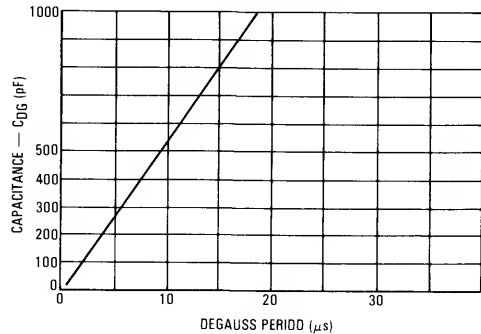
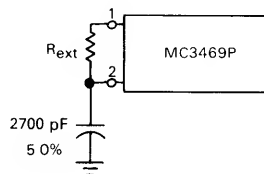
FIGURE 7 — DEGAUSS PERIOD versus CAPACITANCE (C_{DG})

FIGURE 8 — TURN-ON WRITE PROTECTION



TEST FIGURES

Measure V_T	Set				
	S_1	S_2	S_3	V_4^*	V_9^*
$V_{OH} (P14)$	On	Off	P14	0.8	2.0
				2.0	0.8
$V_{OH} (P16)$	On	Off	P16	2.0	2.0
				0.8	0.8
$V_{OL} (P14)$	Off	On	P14	0.8	0.8
				2.0	2.0
$V_{OL} (P16)$	Off	On	P16	2.0	0.8
				0.8	2.0

Measure V_T	Set	
	S1	V8,9
$V_{OL}(P11)$	P11	0.8V
$V_{OL}(P13)$	P13	2.0 V

[illegible]

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FLOPPY DISK READ AMPLIFIER

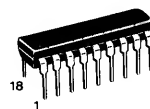
The MC3470 is a monolithic READ Amplifier System for obtaining digital information from floppy disk storage. It is designed to accept the differential ac signal produced by the magnetic head and produce a digital output pulse that corresponds to each peak of the input signal. The gain stage amplifies the input waveform and applies it to an external filter network, enabling the active differentiator and time domain filter to produce the desired output.

- Combines All the Active Circuitry To Perform the Floppy Disk Read Amplifier Function in One Circuit
- Guaranteed Maximum Peak Shift of 2.0% — MC3470A
- Improved (Positive) Gain T_C and Tolerance
- Improved Input Common Mode
- See Application Note AN917 for Further Information

MC3470P MC3470AP

FLOPPY DISK READ AMPLIFIER SYSTEM

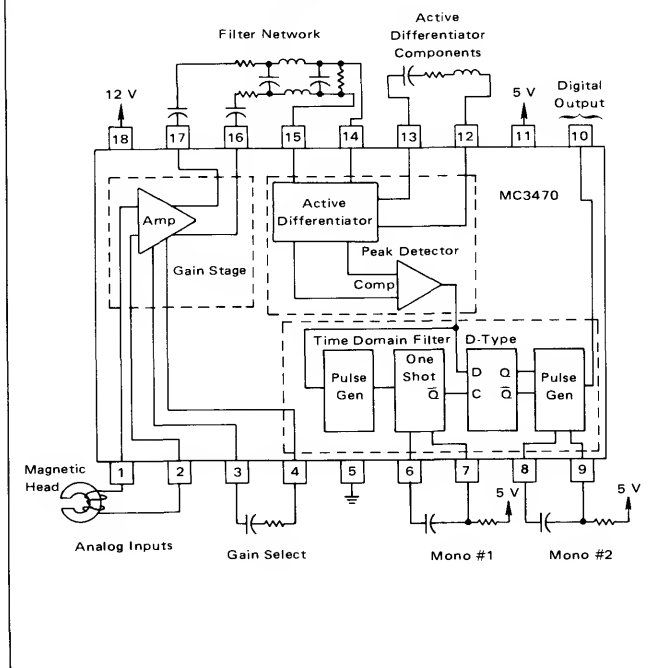
SILICON MONOLITHIC INTEGRATED CIRCUIT



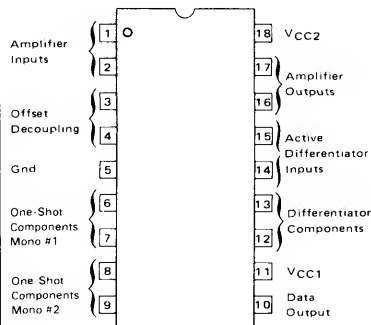
P SUFFIX
PLASTIC PACKAGE
CASE 707

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TYPICAL APPLICATION



PIN CONNECTION



MC3470P, MC3470AP

MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 11)	V _{CC1}	7.0	Vdc
Power Supply Voltage (Pin 18)	V _{CC2}	16	Vdc
Input Voltage (Pins 1 and 2)	V _I	-0.2 to +7.0	Vdc
Output Voltage (Pin 10)	V _O	-0.2 to +7.0	Vdc
Operating Ambient Temperature	T _A	0 to +70	°C
Storage Temperature	T _{stg}	-65 to +150	°C
Operating Junction Temperature Plastic Package	T _J	150	°C

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Power Supply Voltage	V _{CC}	V _{CC1} + 4.75 to +5.25 V _{CC2} +10 to +14	Vdc
Operating Ambient Temperature Range	T _A	0 to +70	°C

ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C, V_{CC1} = 4.75 to 5.25 V, V_{CC2} = 10 to 14 V unless otherwise noted)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Differential Voltage Gain (f = 200 kHz, V _{ID} = 5.0 mV(RMS))	2	A _{VD}	80 100	100 110	130 130	V/V
Input Bias Current	3	I _{IB}	—	-10	-25	μA
Input Common Mode Range Linear Operation (5% max THD)		V _{ICM}	-0.1	—	1.5	V
Differential Input Voltage Linear Operation (5% max THD)		V _{ID}	—	—	25	mVp-p
Output Voltage Swing Differential	2	V _{OD}	3.0	4.0	—	Vp-p
Output Source Current, Toggled		I _O	—	8.0	—	mA
Output Sink Current, Pins 16 and 17	4	I _{OS}	2.8	4.0	—	mA
Small Signal Input Resistance (T _A = 25°C)		r _i	100	250	—	kΩ
Small Signal Output Resistance, Single-Ended (T _A = 25°C, V _{CC1} = 5.0 V, V _{CC2} = 12 V)		r _o	—	15	—	Ω
Bandwidth, -3.0 dB (V _{ID} = 2.0 mV(RMS), T _A = 25°C V _{CC1} = 5.0 V, V _{CC2} = 12 V)	2, 17	BW	10	—	—	MHz
Common Mode Rejection Ratio (T _A = 25°C, f = 100 kHz, A _{VD} = 40 dB, V _{IN} = 200 mVp-p, V _{CC1} = 5.0 V, V _{CC2} = 12 V)	5	CMRR	50	—	—	dB
V _{CC1} Supply Rejection Ratio (T _A = 25°C, V _{CC2} = 12 V, 4.75 ≤ V _{CC1} ≤ 5.25 V, A _{VD} = 40 dB)		—	50	—	—	dB
V _{CC2} Supply Rejection Ratio (T _A = 25°C, V _{CC1} = 5.0 V, 10 V ≤ V _{CC2} ≤ 14 V, A _{VD} = 40 dB)		—	60	—	—	dB
Differential Output Offset (T _A = 25°C, V _{ID} = V _{IN} = 0 V)		V _{DO}	—	—	0.4	V
Common Mode Output Offset (V _{ID} = V _{IN} = 0 V, Differential and Common Mode)		V _{CO}	—	3.0	—	V
Differential Noise Voltage Referred to Input (BW = 10 Hz to 1.0 MHz, T _A = 25°C)	22	e _n	—	15	—	μV(RMS)
Supply Currents (V _{CC1} = 5.25 V, S ₁ to Pin 12 or Pin 13) (V _{CC2} = 14 V)	1	I _{CC1} I _{CC2}	— —	40 4.8	— —	mA

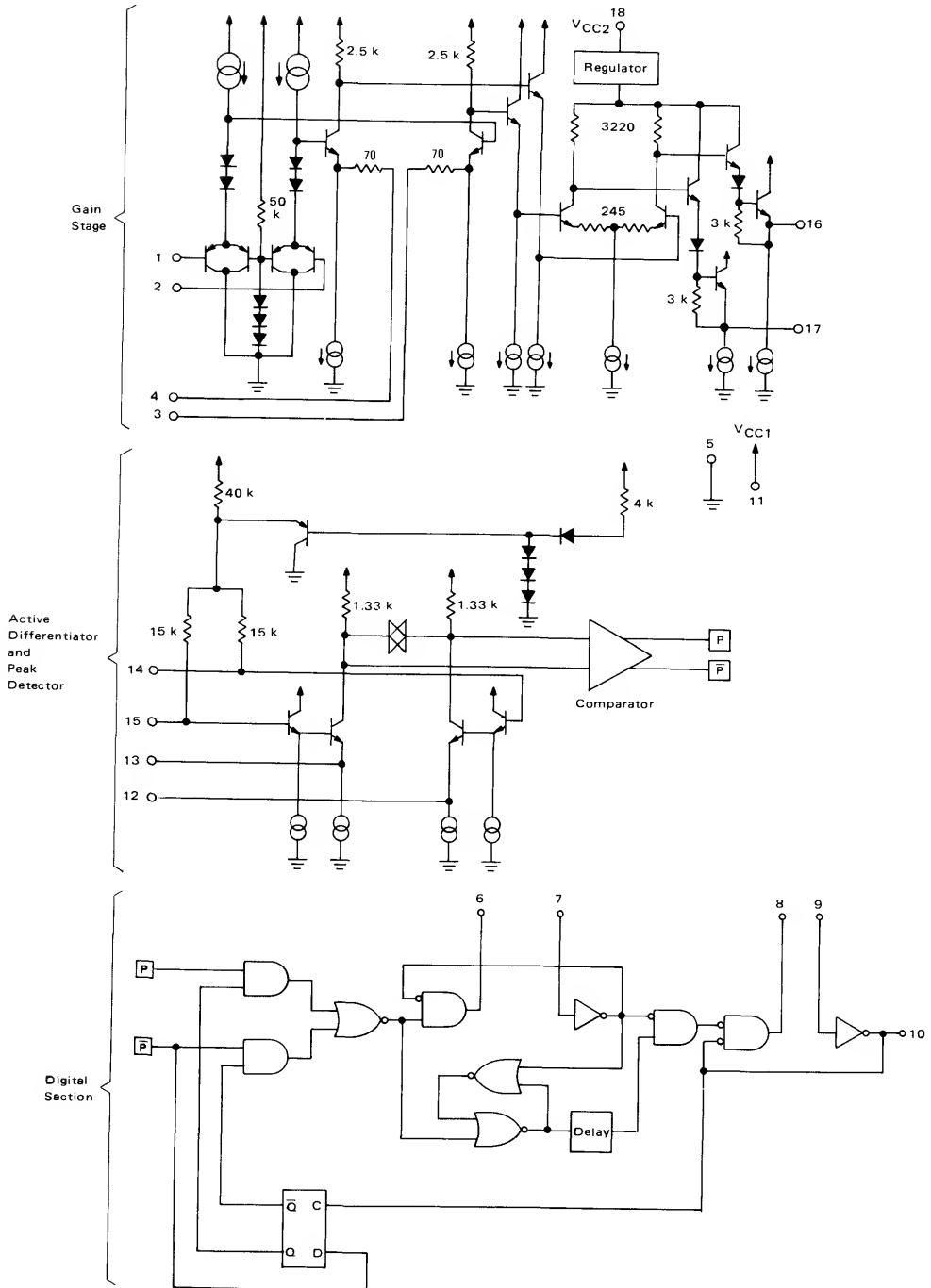
MC3470P, MC3470AP

ELECTRICAL CHARACTERISTICS (continued) ($T_A = 0$ to $+70^\circ\text{C}$, $V_{CC1} = 4.75$ to 5.25 V , $V_{CC2} = 10$ to 14 V unless otherwise noted)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
ACTIVE DIFFERENTIATOR SECTION						
Differentiator Output Sink Current, Pins 12 and 13 ($V_{OD} = V_{CC1}$)	6	I_{OD}	1.0	1.4	—	mA
Peak Shift ($f = 250\text{ kHz}$, $v_{ID} = 1.0\text{ Vp-p}$, $i_{cap} = 500\text{ }\mu\text{A}$, where $PS = 1/2 \frac{t_{PS1} - t_{PS2}}{t_{PS1} + t_{PS2}} \times 100\%$, $V_{CC1} = 5.0\text{ V}$, $V_{CC2} = 12\text{ V}$)	7, 8	PS	—	—	5.0 2.0	%
Differentiator Input Resistance, Differential		r_{ID}	—	30	—	$k\Omega$
Differentiator Output Resistance, Differential ($T_A = 25^\circ\text{C}$)		r_{oD}	—	40	—	Ω
DIGITAL SECTION						
Output Voltage High Logic Level, Pin 10 ($V_{CC1} = 4.75\text{ V}$, $V_{CC2} = 12\text{ V}$, $I_{OH} = -0.4\text{ mA}$)	9	V_{OH}	2.7	—	—	V
Output Voltage Low Logic Level, Pin 10 ($V_{CC1} = 4.75\text{ V}$, $V_{CC2} = 12\text{ V}$, $I_{OL} = 8.0\text{ mA}$)	10	V_{OL}	—	—	0.5	V
Output Rise Time, Pin 10	11, 12	t_{TLH}	—	—	20	ns
Output Fall Time, Pin 10	11, 12	t_{THL}	—	—	25	ns
Timing Range Mono #1 (t_{1A} and t_{1B})	13	$t_{1A, B}$	500	—	4000	ns
Timing Accuracy Mono #1 ($t_1 = 1.0\text{ }\mu\text{s} = 0.625 R_1 C_1 + 200\text{ ns}$) ($R_1 = 6.4\text{ k}\Omega$, $C_1 = 200\text{ pF}$) Accuracy guaranteed for R_1 in the range $1.5\text{ k}\Omega \leq R_1 \leq 10\text{ k}\Omega$ and C_1 in the range $150\text{ pF} \leq C_1 \leq 680\text{ pF}$. Note: To minimize current transients, C_1 should be kept as small as is convenient.	12, 13	E_{t1}	85	—	115	%
Timing Range Mono #2	11, 12	t_2	150	—	1000	ns
Timing Accuracy Mono #2 ($t_2 = 200\text{ ns} = 0.625 R_2 C_2$) ($R_2 = 1.6\text{ k}\Omega$, $C_2 = 200\text{ pF}$) Accuracy guaranteed for $1.5\text{ k}\Omega \leq R_2 \leq 10\text{ k}\Omega$. $100\text{ pF} \leq C_2 \leq 800\text{ pF}$	12, 13	E_{t2}	85	—	115	%

MC3470P, MC3470AP

MC3470 CIRCUIT SCHEMATIC



MC3470P, MC3470AP

FIGURE 1 – POWER SUPPLY CURRENTS, I_{CC1} AND I_{CC2}

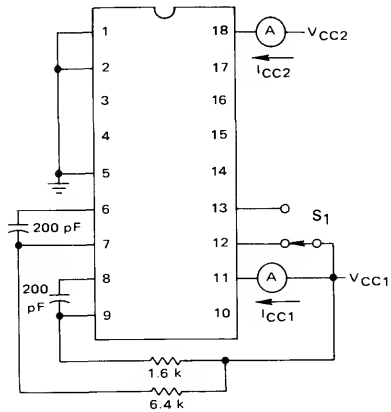


FIGURE 2 – VOLTAGE GAIN, BANDWIDTH, OUTPUT VOLTAGE SWING

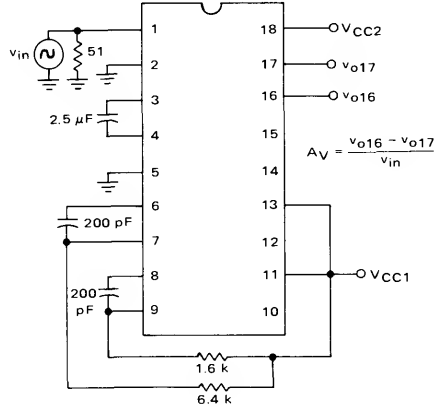


FIGURE 3 – AMPLIFIER INPUT BIAS CURRENT, I_{IB}

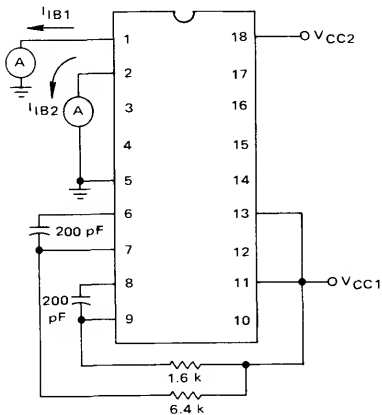
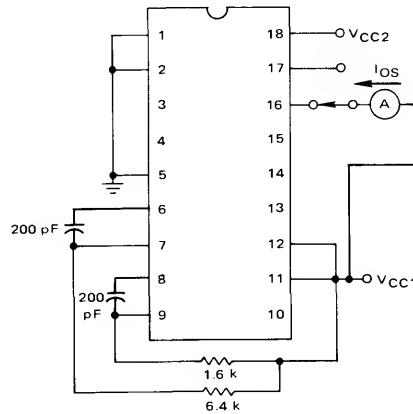
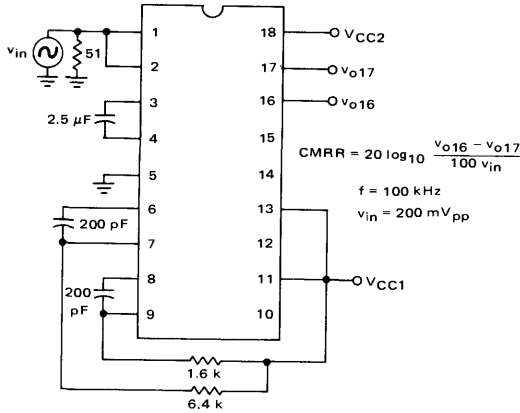


FIGURE 4 – AMPLIFIER OUTPUT SINK CURRENT, PINS 16 AND 17



MC3470P, MC3470AP

FIGURE 5 – AMPLIFIER COMMON MODE REJECTION RATIO, CMRR



NOTE: Measurements may be made with vector voltmeter hp 8405A or equivalent at 1.0 MHz to guarantee 100 kHz performance.

FIGURE 6 – DIFFERENTIATOR OUTPUT SINK CURRENT, PINS 12 AND 13

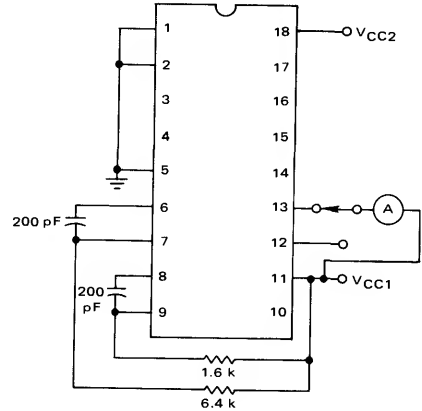


FIGURE 7 – PEAK SHIFT, PS
See Figure 8 for Output Waveform

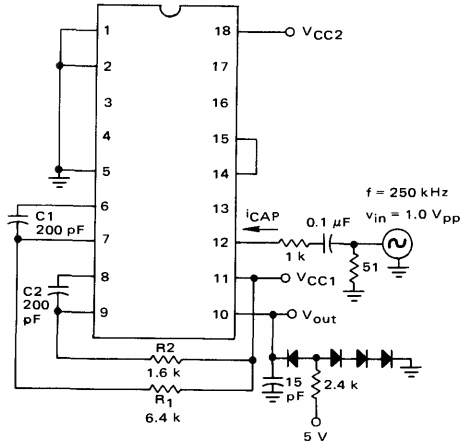
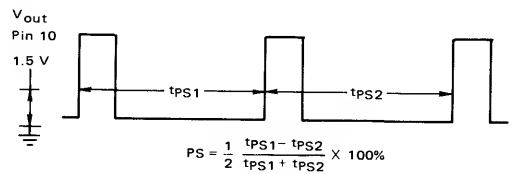


FIGURE 8 – PEAK SHIFT, PS
 $V_{in} = 1.0 \text{ V}_{pp}$ $f = 250 \text{ kHz}$
 Test schematic on Figure 7



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FIGURE 9 – DATA OUTPUT VOLTAGE HIGH, PIN 10

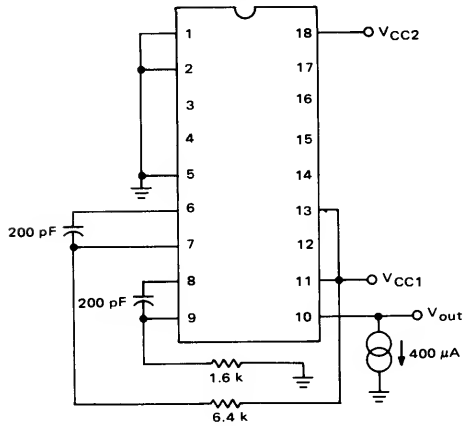


FIGURE 10 – DATA OUTPUT VOLTAGE LOW, PIN 10

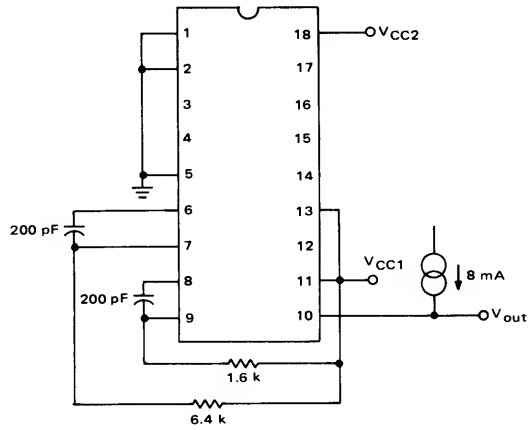


FIGURE 11 – DATA OUTPUT RISE TIME, t_{TLH}
DATA OUTPUT FALL TIME, t_{THL}
TIMING ACCURACY MONO #2, E_{t2}

V_{in} is same as shown on Figure 13, test schematic on Figure 12

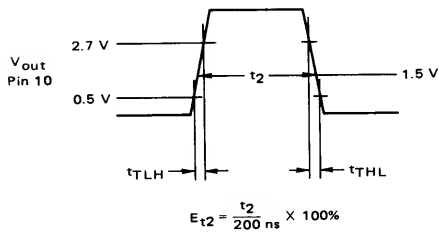
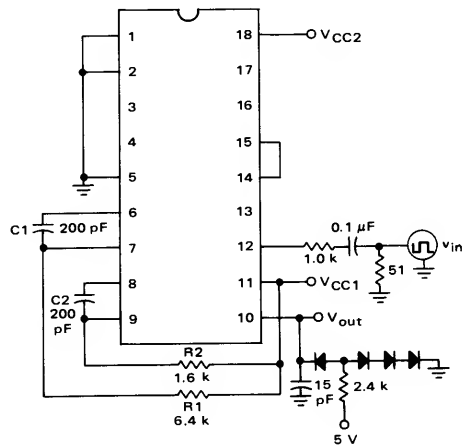


FIGURE 12 – TIMING ACCURACY, E_{t1} AND E_{t2}
DATA OUTPUT RISE AND FALL TIMES, t_{TLH} AND t_{THL}

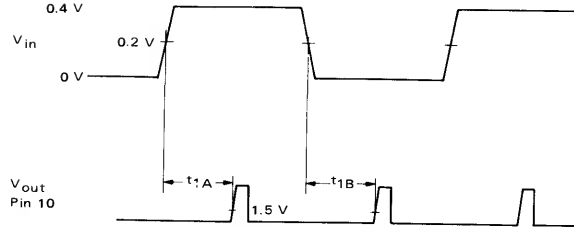
V_{in} shown on Figure 13



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FIGURE 13 – TIMING ACCURACY MONO #1, E_{t1}
 $t_{TLH} = t_{THL} < 10 \text{ ns}$ $f = 250 \text{ kHz}$ 50% Duty Cycle

Test Schematic on Figure 12

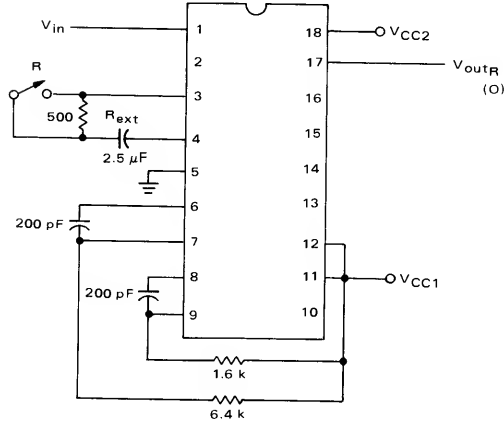


$$E_{t1A} = \frac{t_{1A}}{1000 \text{ ns}} \times 100\%$$

$$E_{t1B} = \frac{t_{1B}}{1000 \text{ ns}} \times 100\%$$

FIGURE 14 – AMPLIFIER OFFSET DECOUPLING IMPEDANCE, PINS 3 AND 4

$R_e + r_e$ and A_V with $R_{ext} = 500 \Omega$



$f = 250 \text{ kHz}$
 $V_{in} = 5 \text{ mV (RMS)}$

$$\frac{A_{VD}}{2} = \frac{V_{out}}{V_{in}}$$

$$r_e + R_e = \frac{R_{ext}}{2 \left(\frac{A_{VO}}{A_{VR}} - 1 \right)}$$

$$= \frac{500 \Omega}{2 \left(\frac{V_{outO}}{V_{outR}} - 1 \right)}$$

FIGURE 15 – NORMALIZED POWER SUPPLY CURRENT
 $(I_{CC}/I_{CC} \text{ } 25^\circ\text{C})$ versus TEMPERATURE

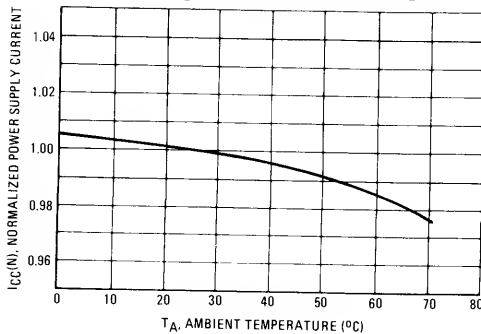
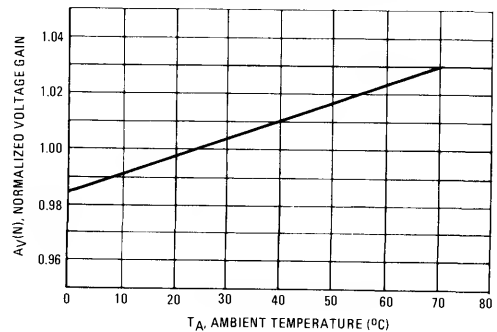


FIGURE 16 – NORMALIZED VOLTAGE GAIN
 $(A_V/A_V \text{ } 25^\circ\text{C})$ versus TEMPERATURE



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FIGURE 17 – PHASE AND NORMALIZED VOLTAGE GAIN versus FREQUENCY

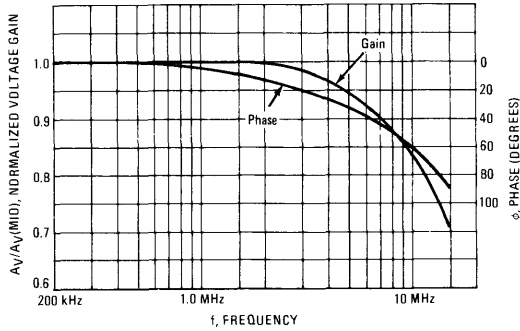


FIGURE 18 – NORMALIZED TIME DELAY $t_1/t_1(25^\circ\text{C})$ versus TEMPERATURE

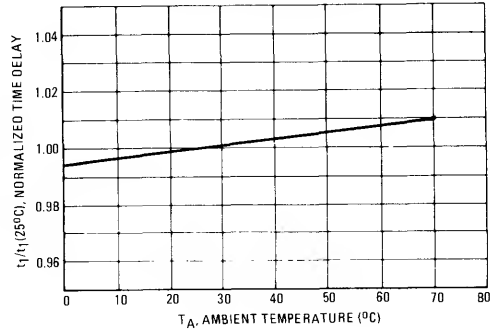


FIGURE 19 – NORMALIZED OUTPUT PULSE WIDTH, $t_2/t_2(25^\circ\text{C})$

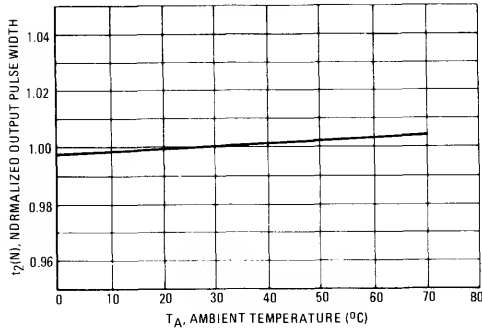


FIGURE 20 – NORMALIZED VOLTAGE GAIN, $A_{VR}/A_{VR}(25^\circ\text{C})$

See Figure 14, Switch Position R

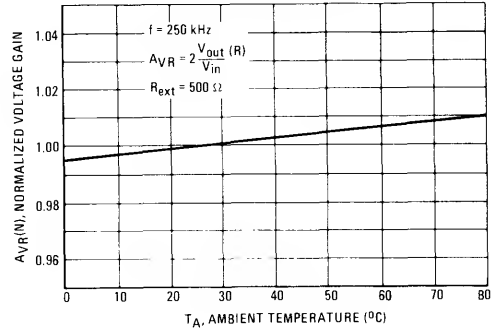


FIGURE 21 – EFFECTIVE EMITTER RESISTANCE DISTRIBUTION, PINS 3 AND 4

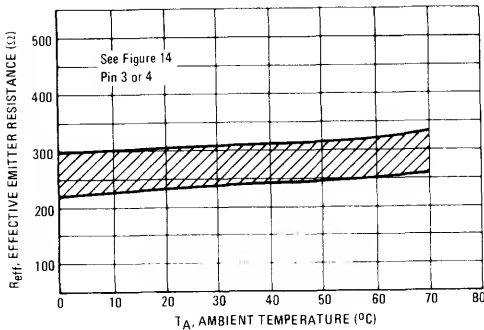
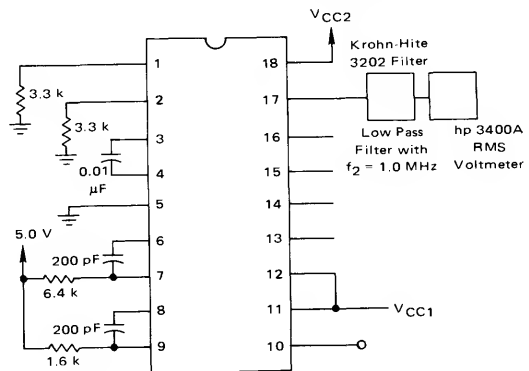


FIGURE 22 – DIFFERENTIAL NOISE VOLTAGE



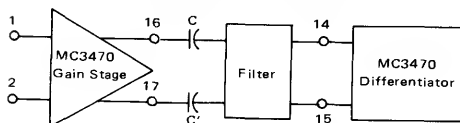
NOTE: Assume uncorrelated noise sources
 e_n (differential noise at input) = $e_o\sqrt{2/100}$

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APPLICATION INFORMATION

The MC3470 is designed to accept a differential ac input from the magnetic head of a floppy disk drive and produce a digital output pulse that corresponds to each peak of the ac input. The gain stage amplifies the input waveform and applies it to a filter network (Figure 23a),

FIGURE 23a — BLOCKING CAPACITORS USED TO ISOLATE THE DIFFERENTIATOR



enabling the active differentiator and time domain filter to produce the desired output.

FILTER CONSIDERATIONS

The filter is used to reduce any high frequency noise present on the desired signal. Its characteristics are dictated by the floppy disk system parameters as well as the coupling requirements of the MC3470. The filter design parameters are affected by the read head characteristics, maximum and minimum slew rates, system transient response, system delay distortion, filter center frequency, and other system parameters. This design criteria varies between manufacturers; consequently, the filter configuration also varies. The coupling requirements of the MC3470 are a result of the output structure of the gain stage and the input structure of the differentiator, and must be adhered to regardless of the filter configuration.

The differentiator has an internal biasing network on each input. Therefore, any dc voltage applied to these inputs will perturbate the bias level. Disturbing the bias level does not affect the waveform at the differentiator inputs, but it does cause peak shifting in the digital output (Pin 10). Since the output of the gain stage has an associated dc voltage level, it, as well as any biasing introduced in the filter, must be isolated from the differentiator via series blocking capacitors. The transient response is minimized if the blocking capacitors C and C' are placed before the filter as shown in Figure 23a. The charging and discharging of C and C' is controlled by the filter termination resistor instead of the high input impedance of the differentiator.

The filter design must also include the current-sinking capacity of the amplifier output. The current source in the output structure (see circuit schematic — Pins 16 and 17) is guaranteed to sink a current of 2.8 mA. If the current requirement of the filter exceeds 2.8 mA, the current source will saturate, the output waveform will be distorted, and inaccurate peak detection will occur in the differentiator. Therefore, the total impedance of the

filter must be greater than Z_{min} as calculated from

$$Z_{min} = \frac{(E_p A_{VD})_{max}}{2.8 \text{ mA}}$$

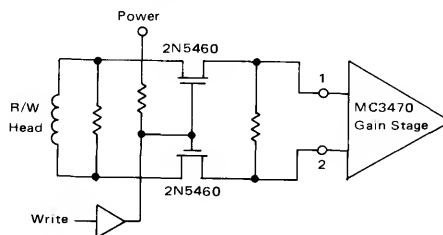
where E_p is the peak differential input voltage to the MC3470.

TRANSIENT RESPONSE

The worst-case transient response of the read channel occurs when dc switching at the amplifier input causes its output to be toggled. The dc voltage changes are a consequence of diode switching that takes place when control is transferred from the write channel to the read channel.

If the diode network is balanced, the dc change is a common mode input voltage to the amplifier. The switching of an unbalanced diode network creates a differential input voltage and a corresponding amplified swing in the outputs. The output swing will charge the blocking capacitor resulting in peak shifting in the digital output until the transient has decayed. Eliminating the differential dc changes at the amplifier input by matching the diode network or by coupling the read head to the amplifier via FET switches, as shown in Figure 23b, will minimize the filter transient response.

FIGURE 23b — FET SWITCHES USED TO COUPLE THE R/W HEAD TO THE MC3470



Two of the advantages FET switches have over diode switching are:

1. They isolate the read channel from dc voltage changes in the system; therefore, the transient response of the filter does not influence the system transient response.
2. The low voltage drop across the FETs keeps the input signal below the amplifier's internal clamp voltage; whereas, the voltage dropped across a diode switching network adds a dc bias to the input signal which may exceed the clamp voltage.

AMPLIFIER GAIN

For some floppy systems, it may become necessary to either reduce the gain of the amplifier or reduce the

See Application Note AN917 for further information.

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signal at the input to avoid exceeding the output swing capability of the amplifier. The voltage gain of the amplifier can be reduced by putting a resistor in series with the capacitor between Pins 3 and 4 (Figure 14). The relationship between the gain and the external resistor is given by

$$A_{VR} = A_{VO} \cdot \frac{2(r_e + R_e)}{2(r_e + R_e) + R_{ext}}$$

where $A_{VO} \triangleq$ voltage gain with the external resistor = 0,

$A_{VR} \triangleq$ voltage gain with the external resistor in,

$R_{ext} \triangleq$ the external resistor, and

$r_e + R_e \triangleq$ the resistance looking into Pin 3 or Pin 4.

Thus,

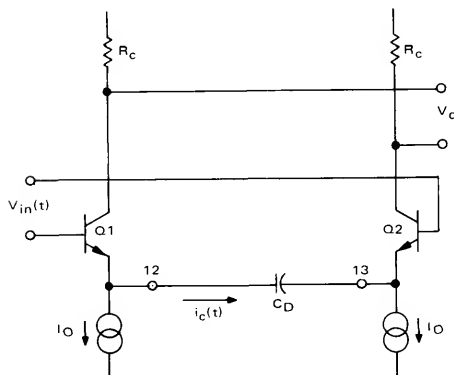
$$R_{ext} = 2 \left(\frac{A_{VO}}{A_{VR}} - 1 \right) (r_e + R_e).$$

A plot of $(r_e + R_e)$ versus temperature is shown in Figure 21. Figure 20 shows the normalized voltage gain versus temperature with the external resistor equal to 500 ohms.

ACTIVE DIFFERENTIATOR

The active differentiator in the MC3470 (simplified circuit shown in Figure 24), is implemented by coupling

FIGURE 24 — ACTIVE DIFFERENTIATOR NETWORK



the emitters of a differential amplifier with a capacitor resulting in a collector current that will be the derivative of the input voltage,

$$I = C dv/dt$$

If the output voltage is taken across a resistor through which the collector current is flowing, the resulting voltage will be the derivative of the input voltage.

$$V_O = 2R i_C = 2RC \frac{dv_{in}(t)}{dt}$$

V_O is applied to a comparator which will provide zero

crossing detection of the current waveform. Since the capacitor shifts the current 90° from the input voltage, the comparator performs peak detection of the input voltage.

The following terms will be used in determining the value of C to be used in the differentiator:

$E_P \triangleq$ peak differential voltage applied to MC3470 amplifier input.

$E_P \sin \omega t \triangleq$ voltage waveform applied to MC3470 amplifier input (for purposes of discussion, assume a sine wave).

$A_{VD} \triangleq$ differential voltage gain of input amplifier.

$v_{in}(t) \triangleq$ differential voltage waveform applied to the differentiator inputs.

$= E_P A_{VD} \sin \omega t$ (Note: The filter is assumed to be lossless.)

$i_C(t) \triangleq$ current through capacitor C_D .

$R_O \triangleq$ output resistance of Q1 (Q2) at Pin 12 (13).

If $v_{in}(t) = E_P A_{VD} \sin \omega t$, then the current through the capacitor C_D is given by

$$i_C(t) = C_D A_{VD} E_P \omega \cos \omega t$$

$$\text{and } V_O(t) = 2R C_D A_{VD} E_P \omega \cos \omega t.$$

Accurate zero crossing detection of $V_O(t)$ [peak detection of $v_{in}(t)$] occurs when the current waveform $i_C(t)$ crosses through zero in a minimum amount of time. This condition is satisfied by maximizing current slew rate. For a given value of ω , the maximum slew rate occurs for the maximum value of i_C or $\cos \omega t = 1$. Therefore,

$$i_C = C_D A_{VD} E_P \omega$$

The MC3470 current-sourcing capacity will determine the maximum value i_C ; therefore, C_D must be chosen such that the maximum i_C occurs at the maximum $A_{VD} E_P \omega$ product.

$$C_D = \frac{i_{C \max}}{(A_{VD} E_P \omega)_{\max}} = \frac{1 \text{ mA}}{(120)(E_P \omega)_{\max}}$$

If the peak value specified for i_C is exceeded, the current source (I_O in Figure 24) will saturate and distort the waveform at Pins 12 and 13. Consequently, the differentiator will not accurately locate the peaks and peak shifting will occur in the digital output.

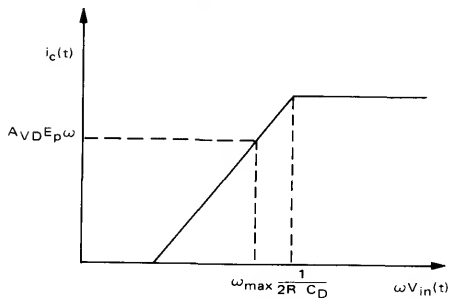
The effective output resistance R_O of Q1 (Q2) will create a pole (as shown in Figure 25) at $1/2 R_O C_D$. If this pole is ten times greater than the maximum operating frequency (ω_{\max}), the phase shift approaches 84°. Locating the pole at a frequency much greater than $10 \omega_{\max}$ needlessly extends the noise bandwidth thus:

$$2R_O = \frac{1}{C_D 10 \omega_{\max}}$$

If R_O is not large enough to satisfy this condition, a series

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FIGURE 25 — RESPONSE OF DIFFERENTIATOR USING ONLY C_D

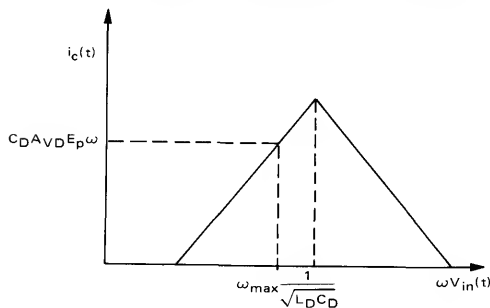


resistor can be added so that

$$R = 2R_0 + R_D = \frac{1}{C_D 10 \omega_{\max}}$$

To further reduce the noise bandwidth, a second pole can be added (as shown in Figure 26) by putting an

FIGURE 26 — COMPLETE RESPONSE OF DIFFERENTIATOR



inductor in series with the resistor and the capacitor. The values of R and L are determined by choosing the center frequency (ω_0) and the damping ratio (δ) to meet the systems requirements where

$$\omega_0 = \frac{1}{\sqrt{L C_D}}$$

$$\delta = \frac{R C_D}{2 \sqrt{L C_D}}$$

$$\omega_0 = 10 \omega_{\max} = \frac{1}{\sqrt{L C_D}}$$

where C_D is chosen for maximum i_c as shown previously.

Solving for L gives:

$$L = \frac{1}{100 C_D (\omega_{\max})^2}$$

Using this value for L gives:

$$\delta = \frac{R C_D}{2 \sqrt{\frac{C_D}{C_D (\omega_{\max})^2}}}$$

Solving for R gives:

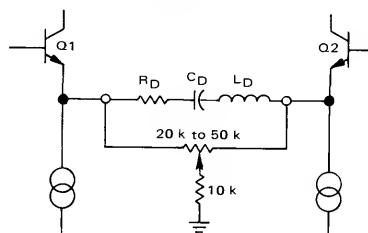
$$R = \frac{\delta}{5 C_D \omega_{\max}}$$

The total resistance (R) is the effective output resistance (R_0) plus the resistor added in the differentiator (R_D). Values of δ from 0.3 to 1 produce satisfactory results.

PEAK SHIFT CONSIDERATIONS

Peak shift, resulting from current imbalance in the differentiator, offset voltage in the comparator, etc., can be eliminated by nulling the current in the emitters of the differentiator with a potentiometer as shown in Figure 27.

FIGURE 27 — PEAK SHIFT COMPENSATION



The potentiometer across the differentiator components is adjusted until a symmetrical digital output cycle is obtained at Pin 10 for a sinusoidal input with the minimum anticipated $E_P \omega$ product.

DESIGN EQUATIONS FOR ONE-SHOTS

As shown in Figure 28, the MC3470 input waveform may have distortion at zero crossing, which can result in false triggering of the digital output. The time domain filter in the MC3470 can be used to eliminate the distortion by properly setting the period (t_1) of the one-shot timing elements on Pins 6 and 7. The following equation will optimize immunity to this signal distortion at zero crossing of the read head signal.

The timing equation for the time domain filter's one-shot is:

$$t_1 = R_1 C_1 K_1 + T_0$$

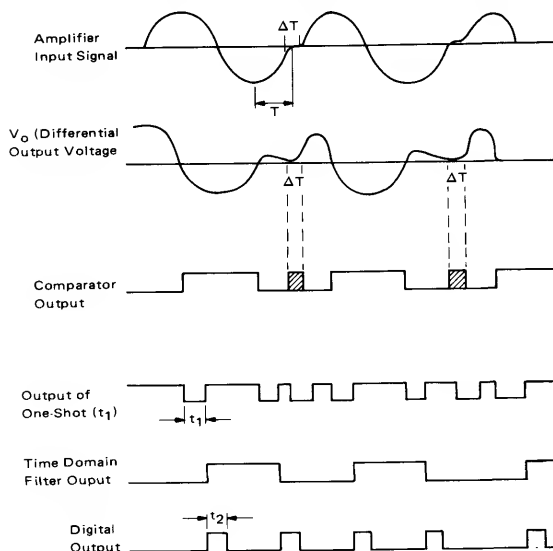
where $K_1 = 0.625$, $T_0 = 200$ ns.

Actual time will be within $\pm 15\%$ of t_1 due to variations in the MC3470.

If ΔT is the maximum period of distortion (see Figure

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FIGURE 28 — WAVEFORMS THROUGH THE READ CIRCUIT



28), then choose t_1 such that

$$\Delta T < t_1 < T - \frac{\Delta T}{2}$$

where $T = \frac{1}{4f_{(\max)}}$.

The width of the digital output pulse t_2 (Pin 10) is determined by

$$t_2 = R_2 C_2 K_2$$

where $K_2 = 0.625$.

Actual pulse width will be within $\pm 15\%$ of t_2 due to variations in the MC3470.

To preserve the specified accuracy of the MC3470, R_1 , R_2 , C_1 , and C_2 should remain in the ranges shown in the Electrical Characteristics. Also, to minimize current transients, it is important to keep the values of C_1 and C_2 as small as is convenient. For $t_1 = 1 \mu s$ and $t_2 = 200 ns$, suggested good values for the capacitors are

$$C_1 = 250 pF$$

$$C_2 = 160 pF$$

BOARD LAYOUT AND TESTING CONSIDERATIONS

An LSI package has many input/output pins in close proximity, some carrying high level signals and others low level signals. As carefully as the on-chip isolation of the devices connected to these pins is implemented by

the manufacturer, the coupling of signals or noise between external wires is under the control of the end-user who designs the integrated circuit into a piece of equipment. The designer should be familiar with the following layout procedures which will optimize the performance of the device. See Figure 29.

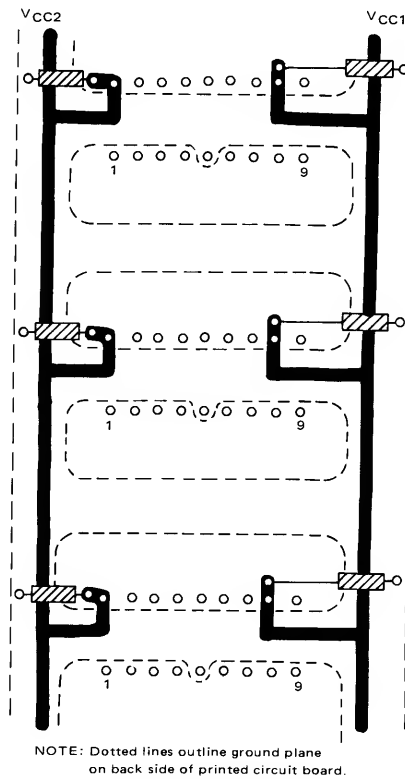
1. Build all circuits on printed circuit boards (including breadboards). Transmission line theory for flat conductors in a plane quite convincingly proves that coupling is far less than for round conductors in three dimensions.
2. Use a ground plane under the IC and over as much of the printed circuit board surface as possible without exceeding practical limits.
3. Avoid signal runs under the IC. Also avoid parallel runs of 1 inch or greater on the opposite or same side of board.
4. Use monolithic ceramic $0.1 \mu F$ capacitors for decoupling power supply transients: one from V_{CC1} to ground and one from V_{CC2} to ground for each IC package. Keep lead lengths to $1/4$ inch or less and place in close proximity to the IC.
5. Keep all signal runs as short as possible.

When evaluating the device for phase jitter and frequency response, a special test jig should be designed to reduce ground loops and coupling caused by instrumentation. Instrumentation test setups must be calibrated

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at each test frequency and differential equipment utilized where required. A valid evaluation of the performance of any read amplifier chain requires considerable care and thought.

FIGURE 29 — POWER AND GROUND DISTRIBUTION FOR MC3470 PRINTED CIRCUIT BOARD LAYOUT



FLOPPY DISK WRITE CONTROLLER/HEAD DRIVER

The MC3471 is a monolithic integrated Write Controller/Head Driver designed to provide the entire interface between the write data and head control signals and the heads (write and erase) for either Tunnel or straddle-erase floppy disk systems.

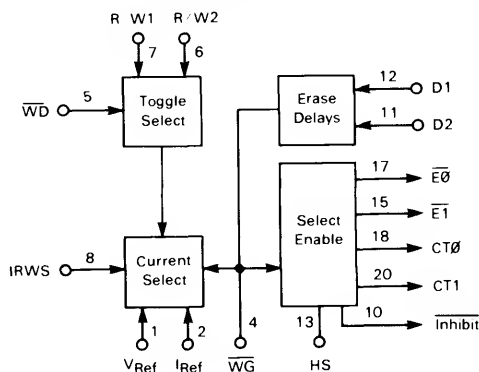
Provisions are made for selecting a range of accurately controlled write currents and for head selection during both read and write operation. Additionally, provisions are included for externally adjusting degauss period, inner/outer track compensation, and the delay from write gate to erase turn-on and turn-off.

Erase Delays are controlled by driving the delay inputs D1 and D2 with standard TTL open-collector logic (microprocessor compatible) or by using the external RC mode in which case the delay is one τ (K factor = 1.0).

In addition, an Inhibit output is provided which indicates that the heads are active during write, degauss, or erase.

- Head Selection — Current Steering Through Write Head and Erase Coil in Write Mode
- Adjustable On-Chip Delay of Erase Timing — Stable K Factor
- Delay Pins Logic Compatible for Direct Microprocessor Compatibility
- Inhibit Output Provided to Disable Read or Step During Head Active Time
- Provides High Impedance (Read Data Enable) During Read Mode
- Head Current (Write) Guaranteed $\pm 3\%$ (3.0 mA using $R_{ext} = 10 \text{ k}\Omega$)
- IRW Select Input Provides for Inner/Outer Track Compensation
- Degauss Period Externally Adjustable
- Specified With Head Supply (V_{BB}) from 10.8 V to 26.4 V
- Minimizes External Components
- See Application Note AN917 for Further Information

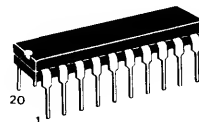
BLOCK DIAGRAM



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FLOPPY DISK WRITE CONTROLLER (WITH ERASE DELAY)

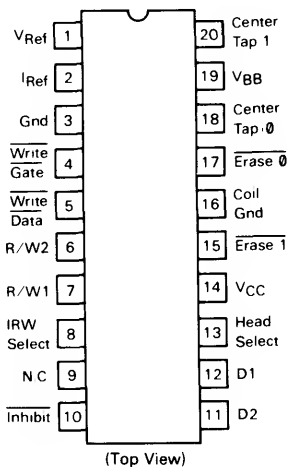
SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 738

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PIN CONNECTIONS



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MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 14)	V _{CC}	7.0	V _{dc}
Power Supply Voltage (Pin 19)	V _{BB}	30	V _{dc}
Input Voltage (Pins 4, 5, 8, 13)	V _I	5.75	V _{dc}
Output Applied Voltage (Pin 10)	V _O	7.0	V _{dc}
Open-Collector Sink Current (Pin 10)	I _O	25	mA
Storage Temperature	T _{stg}	-55 to +150	°C
Operating Junction Temperature	T _J	150	°C

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 14)	V _{CC}	+4.75 to +5.25	V _{dc}
Power Supply Voltage (Pin 19)	V _{BB}	+10.8 to +26.4	V _{dc}
Operating Ambient Temperature Range	T _A	0 to +70	°C

ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = 4.75 to 5.25 V, V_{BB} = 10.8 to 26.4 V unless otherwise noted. Typicals given for V_{CC} = 5.0 V, V_{BB} = 12 V and T_A = 25°C unless otherwise noted.)

Characteristics	Pins	Symbol	Min	Typ	Max	Unit
DIGITAL INPUT VOLTAGES						
Power Supply Current — V _{CC} V _{BB}		I _{CC} I _{BB}	— —	22 15	60 30	mA
High Level Input Voltage (V _{CC} = 4.75 V)	4, 8, 13	V _{IH}	2.0	—	—	V
Low Level Input Voltage (V _{CC} = 5.25 V)	4, 8, 13	V _{IL}	—	—	0.8	V
Input Clamp Voltage (I _{IK} = -12 mA)	4, 5, 8, 13	V _{IK}	—	-0.87	-1.5	V
Positive Threshold (V _{CC} = 5.0)	5	V _{T(+)}	1.5	1.75	2.0	V
Negative Threshold (V _{CC} = 5.0)	5	V _{T(-)}	0.7	0.98	1.3	V
Hysteresis (V _{T(+)} - V _{T(-)}). T _A = 0°C to +70°C T _A = 25°C	5	V _{HTS}	0.2 0.4	— 0.76	— —	V

DIGITAL INPUT CURRENTS

High Level Input Current (V _{CC} = 5.25 V, V _{BB} = 26.4 V, V _I = 2.4 V)	4, 5, 8, 13	I _{IH}	—	0.1	40	μA
Low Level Input Current (V _{CC} = 5.25 V, V _{BB} = 26.4 V, T _A = 25°C unless noted below)	4, 5, 8, 13	I _{IL}	—	—	-1.6	mA
V _{BB} = 12 V	4		—	0.36	—	
V _{BB} = 24 V	4		—	0.76	—	
V _{CC} = 5.0 V	5		—	0.46	—	
V _{CC} = 5.0 V	8, 13		—	0.39	—	

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ELECTRICAL CHARACTERISTICS (continued) ($T_A = 0$ to $+70^\circ\text{C}$, $V_{CC} = 4.75$ to 5.25 V, $V_{BB} = 10.8$ to 26.4 V unless otherwise noted. Typical values given for $V_{CC} = 5.0$ V, $V_{BB} = 12$ V and $T_A = 25^\circ\text{C}$ unless otherwise noted.)

Characteristics	Pins	Symbol	Min	Typ	Max	Unit
CENTER-TAP and ERASE OUTPUTS						
Output High Voltage (See Figure 14) ($I_{OH} = -100$ mA, $V_{CC} = 4.75$ V) $V_{BB} = 10.8$ to 26.4 V	18, 20	V_{OH}	$V_{BB}-1.5$	$V_{BB}-1.0$	—	V
Output Low Voltage (See Figure 14) ($I_{OL} = 10$ mA) $V_{BB} = 12$ V $V_{BB} = 24$ V	18, 20	V_{OL}	— —	70 70	150 150	mV
Output High Leakage Current ($V_{OH} = 24$ V, $V_{CC} = 4.75$ V, $V_{BB} = 24$ V)	15, 17	I_{OH}	—	0.01	100	μA
Output Low Voltage (See Figure 15) ($I_{OL} = 90$ mA, $V_{CC} = 4.75$ V) $V_{BB} = 12$ V $V_{BB} = 24$ V	15, 17	V_{OL}	— —	0.27 0.27	0.60 0.60	V

DIGITAL OUTPUT LEVEL (Inhibit)

High Level Output Current ($V_{OH} = 7.0$ V, $V_{CC} = 4.75$ V)	10	I_{OH}	—	—	100	μA
Low Level Output Voltage ($I_{OL} = 4.0$ mA, $V_{CC} = 4.75$ V)	10	V_{OL}	—	—	0.5	V

CURRENT SOURCE

Reference Voltage	1	V_{Ref}	—	5.7	—	V
Degauss Voltage (See Text) (Voltage Pin 1 - Voltage Pin 2)	1	V_{DEG}	—	1.0	—	V
Bias Voltage	2	V_F	—	0.7	—	V
Write Current Off Leakage ($V_{OH} = 30$ V)	6, 7	I_{OH}	—	0.03	15	μA
Saturation Voltage ($V_{BB} = 12$ V)	6, 7	V_{sat}	—	0.85	2.7	V
Current Sink Compliance (For $V_{G6, 7} = 4.0$ V to 24 V, $V_{WG} = 0.8$ V)	6, 7	$\Delta I_{RW2, 1}$	—	15	40	μA
Average Value Write Current ($(I_{Pin 6} + I_{Pin 7}) / 2$ for $V_{BB} = 10.8$ to 26.4 V) @ $I_{R/W} = I_{LOW}$, $R = 10$ k $T_A = 25^\circ\text{C}$ $T_A = 0$ to $+70^\circ\text{C}$ @ $I_{R/W} = I_{LOW}$, $R = 5.0$ k $T_A = 25^\circ\text{C}$ $T_A = 0$ to $+70^\circ\text{C}$ @ $I_{R/W} = I_{HI}$, $R = 10$ k ($I_{HI} = I_{LOW} + \% I_{LOW}$) $T_A = 25^\circ\text{C}$ $T_A = 0$ to $+70^\circ\text{C}$	6, 7	$I_{R/W(L)}$ $\Delta I_{R/W(H)}$	2.91 2.84 5.64 5.51 31.3 30.3	3.0 — 5.89 — 33.3 33.3	3.09 3.16 6.14 6.28 35.5 36.6	mA %
Difference in Write Current ($ I_{Pin 6} - I_{Pin 7} $) @ $I_{R/W} = I_{LOW}$, $V_{BB} = 10.8$ V to 26.4 V $R = 10$ k $T_A = 25^\circ\text{C}$ $T_A = 0$ to $+70^\circ\text{C}$ $R = 5.0$ k $T_A = 25^\circ\text{C}$ $T_A = 0$ to $+70^\circ\text{C}$	6, 7	$I_{R/W\Delta}$	— — — —	0.003 — — —	0.015 0.023 0.030 0.046	mA

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ERASE DELAY ACCURACY ($V_{CC} = 4.75$ to 5.25 V, $T_A = 0$ to $+70^\circ\text{C}$, $V_{BB} = 10.8$ to 26.4 V. — refer to Figure 9.)

Characteristics	Test	Min	Typ	Max	Unit
Delay Error, Pin 11, 12 D1, D2 = $RC \pm E_{D1,2}$, $30 \text{ k}\Omega \leq R \leq 300 \text{ k}\Omega$	$E_{D1,2}$	—	—	15	%

AC SWITCHING CHARACTERISTICS ($V_{CC} = 5.0$ V, $T_A = 25^\circ\text{C}$, $V_{BB} = 24$ V, $I_{RWS} = 0.4$ and $I_{RWV} = 3.0$ mA unless otherwise noted.)

Characteristics (Note 1)	f_{in} (Note 2)	Min	Typ	Max	Unit
1. Delay from Head Select going low through 0.8 V to CT0 going high through 20 V.	HS, Pin 13	—	1.6	4.0	μs
2. Delay from Head Select going low through 0.8 V to CT1 going low through 1.0 V.	HS, Pin 13	—	2.1	4.0	μs
3. Delay from Head Select going high through 2.0 V to CT0 going low through 1.0 V.	HS, Pin 13	—	1.7	4.0	μs
4. Delay from Head Select going high through 2.0 V to CT1 going high through 20 V.	HS, Pin 13	—	1.4	4.0	μs
5. Delay from \overline{WG} going low through 0.8 V to CT0 going low through 1.0 V.	\overline{WG} , Pin 4	—	1.3	4.0	μs
6. Delay from \overline{WG} going low through 0.8 V to CT1 going high through 20 V.	\overline{WG} , Pin 4	—	0.8	4.0	μs
7. Delay from \overline{WG} going low through 0.8 V to CT0 going high through 20 V.	\overline{WG} , Pin 4	—	0.75	4.0	μs
8. Delay from \overline{WG} going low through 0.8 V to CT1 going low through 1.0 V.	\overline{WG} , Pin 4	—	1.2	4.0	μs
9. After \overline{WG} goes high, delay from R/W1 turning off through 10% to CT0 going high through 20 V.	\overline{WG} , Pin 4	20	750	—	ns
10. After \overline{WG} goes high, delay from R/W1 turning off through 10% to CT1 going low through 1.0 V.	\overline{WG} , Pin 4	20	1200	—	ns
11. After \overline{WG} goes high, delay from R/W2 turning off through 10% to CT0 going low through 1.0 V.	\overline{WG} , Pin 4	20	1200	—	ns
12. After \overline{WG} goes high, delay from R/W2 turning off through 10% to CT1 going high through 20 V.	\overline{WG} , Pin 4	20	600	—	ns
13. After \overline{WG} goes low, delay from CT0 going low through 1.0 V to R/W1 turning on through 10%.	\overline{WG} , Pin 4	20	750	—	ns
14. After \overline{WG} goes low, delay from CT1 going low through 1.0 V to R/W2 turning on through 10%.	\overline{WG} , Pin 4	20	750	—	ns
15. After \overline{WG} goes low, fall time (10% to 90%) of R/W1.	\overline{WG} , Pin 4	—	5.0	200	ns
16. After \overline{WG} goes low, fall time (10% to 90%) of R/W2.	\overline{WG} , Pin 4	—	5.0	200	ns
17. Setup time, Head Select going low before \overline{WG} going low.	\overline{WG} , Pin 4	4.0	—	—	μs
18. Write Data low Hold Time	WD, Pin 5	200	—	—	ns
19. Write Data high Hold Time	WD, Pin 5	500	—	—	ns
20. Delay from \overline{WG} going high through 2.0 V to R/W1 turning off through 10% of on value.	\overline{WG} , Pin 4	—	3.9	—	μs
21. Delay from \overline{WG} going low thru 0.8 V to Inhibit going low thru 0.5 V	\overline{WG} , Pin 4	—	0.08	4.0	μs
22. After \overline{WG} goes high, delay from R/W1 turning off thru 10% to Inhibit going high thru 1.5 V (10 k pullup on Inhibit, Note 3)	\overline{WG} , Pin 4	20	750	—	ns
23. After \overline{WG} goes high, delay from $\overline{E1}$ going high thru 23 V to Inhibit going high thru 1.5 V (10 k pullup on Inhibit, Note 3)	WG	20	750	—	ns

Notes:

- Test numbers refer to encircled numbers in Figures 3 & 16.
- AC test waveforms applied to the designated pins as follows:

Pin	f_{in}	Amplitude	Duty Cycle
HS, Pin 13	50 kHz	0.4 to 2.4 V	50%
\overline{WG} , Pin 4	50 kHz	0.4 to 2.4 V	50%
WD, Pin 5	1.0 MHz	0.2 to 2.4 V	50%

- Test Conditions 22, or 23, whichever produces the longer delay, will control Inhibit.

AC SWITCHING CHARACTERISTICS (continued)(V_{CC} = 5.0 V, T_A = 25°C, V_{BB} = 24 V, W_G = 0.4 unless otherwise noted)

Characteristics (Note 4)	Min	Typ	Max	Unit
1. Delay from Write Data going low through 0.9 V to R/W1 turning on through 50%.	—	85	—	ns
2. Delay skew, difference of R/W1 turning off and R/W2 turning on through 50% after Write Data going low through 0.9 V.	—	1.0	±40	ns
3. Delay from Write Data going low through 0.9 V to R/W1 turning off through 50%.	—	80	—	ns
4. Delay skew, difference of R/W1 turning on and R/W2 turning off 50% after Write Data going low through 0.9 V.	—	1.0	±40	ns
5. Fall time, 10% to 90%, of R/W1	—	1.7	200	ns
6. Fall time, 10% to 90%, of R/W2	—	1.7	200	ns
7. Rise time, 90% to 10%, of R/W1	—	12	200	ns
8. Rise time, 90% to 10%, of R/W2	—	12	200	ns

Note 4. Test numbers refer to encircled numbers in Figures 2 & 15.
 f_{in} = 1.0 MHz, 50% Duty Cycle and Amplitude of 0.2 V to 2.4 V.

PIN DESCRIPTION TABLE

Name	Symbol	Pin	Description
Head Select	HS	13	Head Select input selects between the head I/O pins; center-tap, erase, and read/write. A HIGH selects Head 0 and a LOW selects Head 1.
Write Gate	W _G	4	Write Gate input selects the mode of operation. HIGH selects the read mode, while LOW selects the Write Control mode and forces the write current.
Write Data	W _D	5	Write Data input controls the turn on/off of the write current. The internal divide-by-two flip-flop toggles on the negative going edge of this input to direct the current alternately to the two halves of the head coils.
IRW Select	IRWS	8	IRW Select input selects the amount of write current to be used. When LOW, the current equals the value found in Figure 5, according to the external resistor. When HIGH, the current equals the low current + 33%.
V _{Ref} I _{Ref}	V _{Ref} I _{Ref}	1 2	A resistor between these pins sets the write current. (Refer to Figure 4.) A capacitor from V _{Ref} to Gnd will adjust the Degauss period.
Center-Tap 0	CT0	18	Center-Tap 0 output is connected to the center tap of Head 0. It will be pulled to Gnd or V _{BB} (+12 or +24) depending on mode and head selection.
Erase 0	E0	17	Erase 0 will be LOW for writing on Head 0, and floating for other conditions.
Center-Tap 1	CT1	20	Center-Tap 1 output is connected to the center tap of Head 1. It will be pulled to Gnd or V _{BB} (+12 or +24) depending on mode and head selection.
Erase 1	E1	15	Erase 1 will be LOW for writing on Head 1, and floating for other conditions.
R/W2	R/W2	6	R/W2 input is one of the differential inputs that sinks current during writing, being the opposite phase of R/W1. It will be connected to one side of the heads.
R/W1	R/W1	7	R/W1 input is one of the differential inputs that sinks current during writing, being the opposite phase of R/W2. It will be connected to one side of the heads.
	V _{CC}	14	+5.0 V Power
	V _{BB}	19	+12 V or +24 V Power
	Gnd	16	Coil grounds
	Gnd	3	Reference and logic ground
Delay 1	D1	12	Erase Turn-On Delay adjust (RC or Logic)
Delay 2	D2	11	Erase Turn-Off Delay adjust (RC or Logic)
Inhibit	Inhibit	10	Active low open-collector output provided to indicate heads are active in the write, degauss or erase mode. (Used for step or read inhibit.)

MC3471P

FIGURE 3 — AC TIMING DIAGRAM

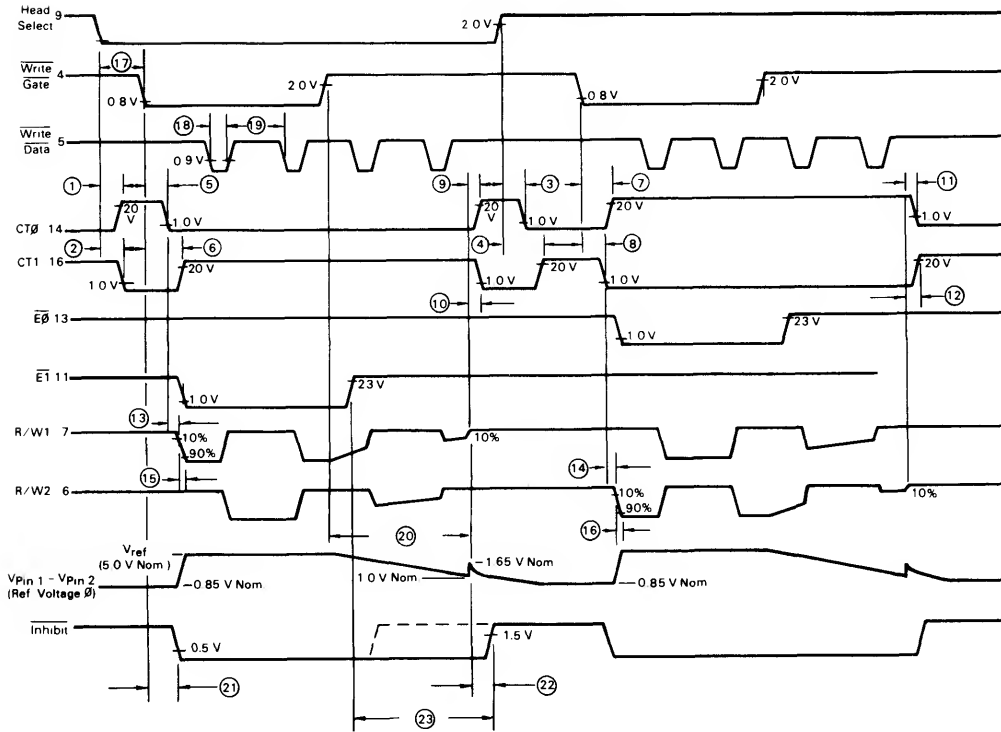
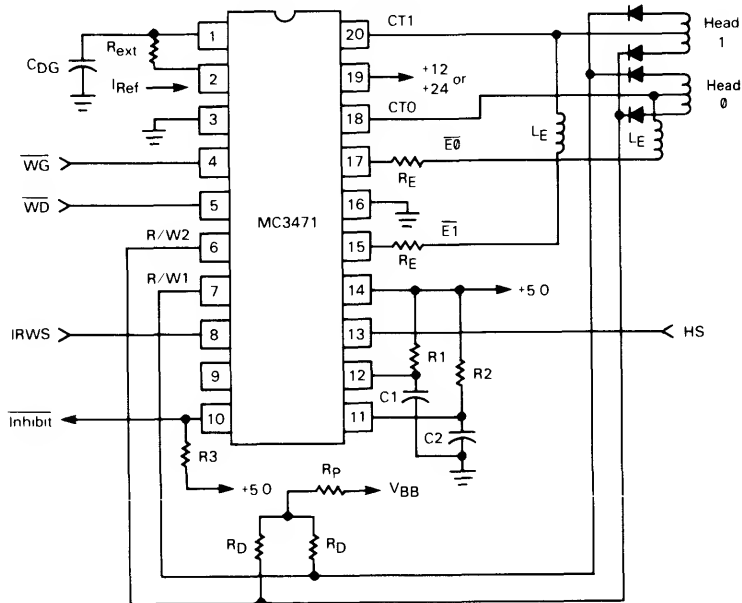


FIGURE 4 — TYPICAL APPLICATION



APPLICATION INFORMATION

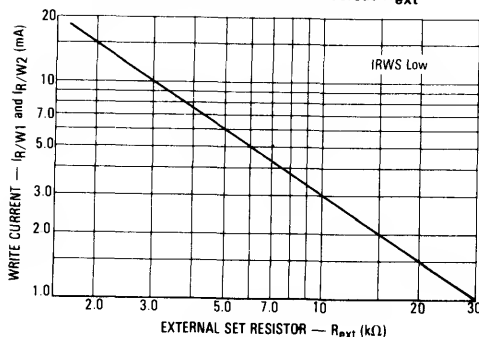
The MC3471P serves as a complete interface between the Write Control functional signals (Head Select, Write Data, Write Gate and inner track compensation, IRWS) and the head itself. A typical configuration is shown in Figure 4. L_E's are erase coils.

WRITE CURRENT SELECTION

Although the MC3471P has been specified for 3.0 mA write current (with a 10 k Ω external resistor), a range of write current values can be chosen by varying R_{ext} using the plot in Figure 5. This current can also be derived using

$$\text{the relationship } I_{\text{Write}} (\text{mA}) = \frac{30}{R_{\text{ext}} (\text{k}\Omega)}$$

I_{Ref}, the current flowing in R_{ext} (required only for dissipation calculations) can be worst case using the fact that the differential voltage between Pins 1 and 2 (V_{Ref}) shown in Figure 3 never exceeds 5.0 volts. With a low value of R_{ext} = 1.0 k Ω , P_D = 25 mW.

FIGURE 5 — WRITE CURRENT versus R_{ext}

WRITE CURRENT DAMPING

Referring to Figure 4, resistors R_D are used to dampen any ringing that results from applying the relatively fast risetime write current pulse to the inductive head load. Values chosen will be a function of head characteristics and the desired damping. R_p serves as a common pullup resistor to the head supply V_{BB}.

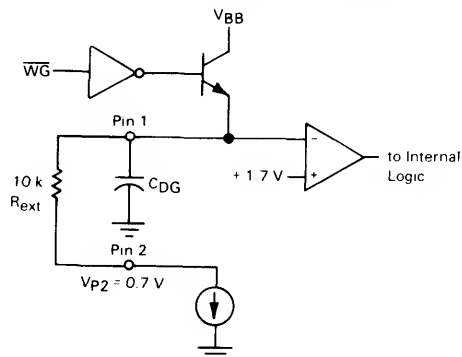
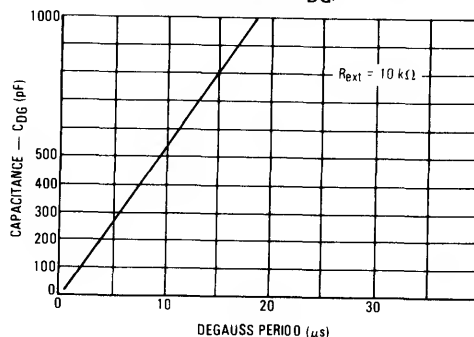
DEGAUSS PERIOD

Degauss of the read/write head can be accomplished at the end of each write operation by attaching a capacitor from Pin 1 to ground. The time relationship that results is shown in Figure 7. A simplified diagram of this function is shown in Figure 6.

While $\overline{\text{WG}}$ is low, the selected write current flows into Pin 6 or Pin 7 (R/W1 or R/W2) and is mirrored through the external resistor, R_{ext}. The degauss capacitor, C_{DG}, will be charged to approximately 5.7 volts. After $\overline{\text{WG}}$ goes high, the voltage on C_{DG} begins to decay toward 0.7 V. When the voltage reaches the comparator threshold of 1.7 V, the comparator output triggers the internal logic to completely turn off the write current. At this point, the pulse amplitude on the R/W1 and R/W2 pins has returned to 10% of its maximum value.

Figure 7, Degauss Period shows the relationship between C_{DG} and Degauss Period for R_{ext} = 10 k Ω . This period is equal to the exponential delay time for the voltage as mentioned plus internal delay times.

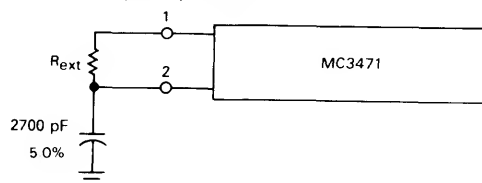
FIGURE 6 — SIMPLIFIED DEGAUSS CIRCUIT

FIGURE 7 — DEGAUSS PERIOD versus CAPACITANCE (C_{DG})

POWER-UP WRITE CURRENT CONTROL

During power-up, under certain conditions (V_{BB} comes up first while $\overline{\text{WG}}$ is low), there can be a write current transient on Pins 6 and 7 (R/W1 and R/W2) of sufficient magnitude to cause writing to occur if the head is loaded.

This transient can be eliminated by placing a capacitor from Pin 2 to ground. This also delays the write current when $\overline{\text{WG}}$ goes low and this delay must be accounted for when the capacitor on Pin 2 is used. The delay is 3.0 μ s for a 2700 pF capacitor, and R_{ext} = 10 k Ω . Values up to 7000 pF may be used.



See Application Note AN917 for further information.

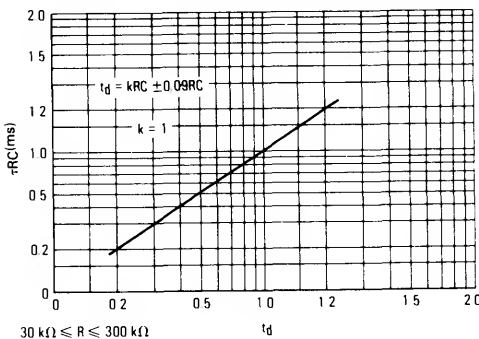
ERASE DELAY

The MC3471P can be used with both straddle and tunnel erase heads. When using the tunnel erase heads, it is necessary to delay the erase current in time with respect to \overline{WG} due to the physical placement of the erase gap behind the R/W gap on the heads. The amount of delay required depends upon the disk rotation velocity, recording density and format. Turn-on delay and turn-off delay must also be independent to guarantee erase is on for the entire block.

Nominal delays of 500 μ s turn-on; and 1.0 ms turn-off are available by adjusting the value of R1, R2 and C1, C2 shown in Figure 4. These delays are adjustable over a broad range as shown in Figure 9 to achieve any practical delay required. By using 5% capacitors and 1% resistors, total timing accuracy is better than $\pm 15\%$ over temperature and supply. Timing is shown in Figure 10.

In applications using logic or microprocessor controlled delays, the D1 and D2 inputs can be used directly to turn-on and turn-off the erase current. (Controlling outputs should be Open-collector w/10 k pullup). Figure 11 shows the relative timing involved for the microprocessor and logic controlled applications.

In straddle erase systems, the erase delays can be eliminated by pulling D1 and D2 high thru a 10 k Ω pullup resistor to +5.0 V.

FIGURE 9 — TYPICAL \overline{WG} TO $\overline{E0}$, 1 DELAY versus RC

ERASE CURRENT

The value of R_E , the erase current set resistor, is found by referring to Figure 12 and selecting the desired erase current.

Looking at the simplified erase current path in Figure 12, when writing, $\overline{CT0}$ will be high ($V_{OH(min)} = 22.5$ V) and $\overline{E0}$ will be low ($V_{OL(max)} = 0.6$ V). If the erase coil resistance is 10 Ω and 40 mA of erase current is desired then:

$$(R_E + 10 \Omega) \times 40 \text{ mA} = (22.5 - 0.6) \text{ V}$$

or

$$R_E = \frac{21.9 \text{ V}}{0.04 \text{ A}} - 10 \Omega = 537 \Omega$$

$$P_D = (537) (0.04)^2 = 0.86 \text{ W}$$

This gives the minimum value R_E for worst case V_{OH}/V_{OL} conditions. It is also recommended that a diode be used as indicated for inductive back emf suppression.

FIGURE 10 — DELAY INPUT FUNCTION/TIMING WITH RC ELEMENTS

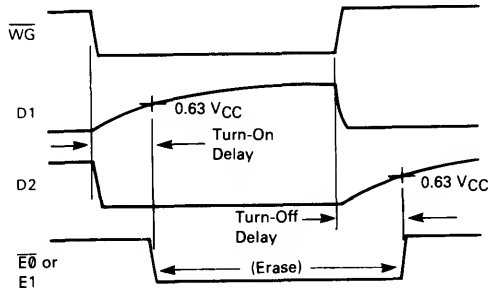
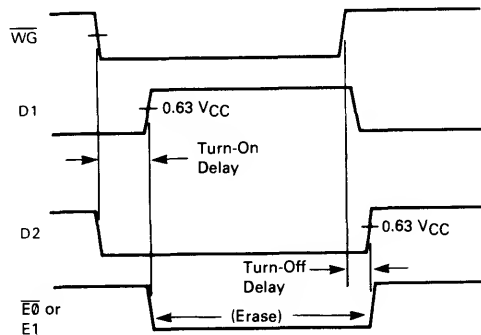
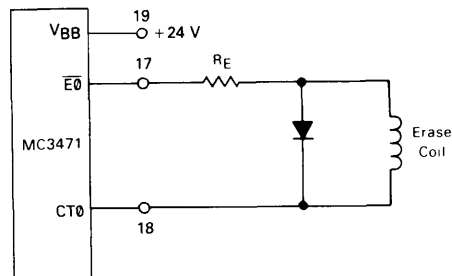
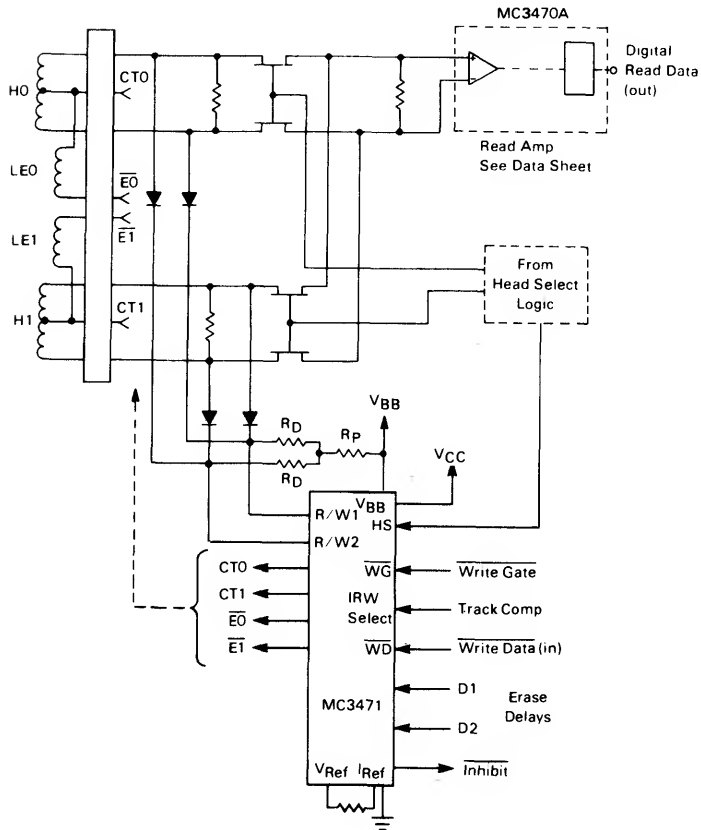


FIGURE 11 — DELAY INPUT FUNCTION/TIMING WITH LOGIC CONTROL

FIGURE 12 — ERASE CURRENT (R_E Selection)

MC3471P

FIGURE 13 – TYPICAL DUAL HEAD FLOPPY DISK SYSTEM USING FET GATE READ CHANNEL SELECTION AND MC3471/MC3470A



Function	CT0	CT1	E0	E1
Write 0	VBB	0 V	On	Off
Write 1	0 V	VBB	Off	On
Read 0	0 V	VBB	Off	Off
Read 1	VBB	0 V	Off	Off

7

LINEAR/INTERFACE DEVICES

7-133

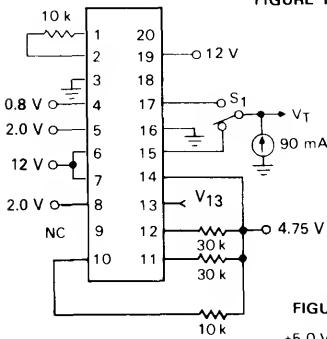
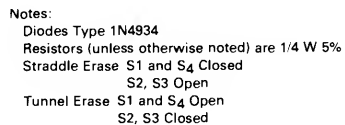


FIGURE 16 — TIMING TEST CIRCUIT

Measure	Set	
	S ₁	V ₁₃
V _T		
V _{OL} (P15)	P15	0.8V
V _{OL} (P17)	P17	2.0V

FIGURE 16 — TIMING TEST CIRCUIT



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

MC3481 MC3485

QUAD SINGLE-ENDED LINE DRIVER

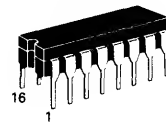
The MC3481 and MC3485 are quad single-ended line drivers specifically designed to meet the IBM 360/370 I/O specification (GA22-6974-3).

Output levels are guaranteed over the full range of output load and fault conditions. Compliance with the IBM requirements for fault protection, flagging, and power up/power down protection for the bus make this an ideal line driver for party line operations.

- Separate Enable and Fault Flags — MC3481
- Common Enable and Fault Flag — MC3485
- Power Up/Down Does Not Disturb Bus
- Schottky Circuitry for High-Speed — PNP Inputs
- Internal Bootstraps for Faster Rise Times
- Driver Output Current Foldback Protection
- MC3485 has LS Totem Pole Driver Output

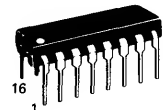
IBM 360/370 QUAD LINE DRIVER

SILICON MONOLITHIC
INTEGRATED CIRCUIT

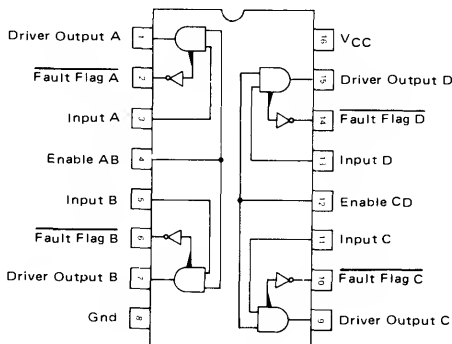


L SUFFIX
CERAMIC PACKAGE
CASE 620

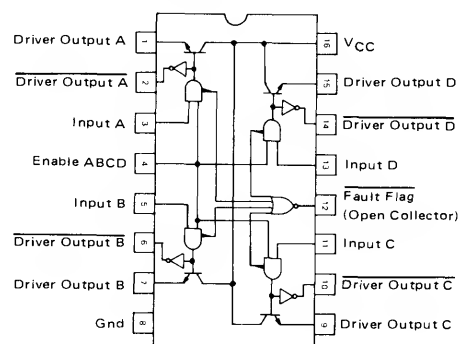
P SUFFIX
PLASTIC PACKAGE
CASE 648



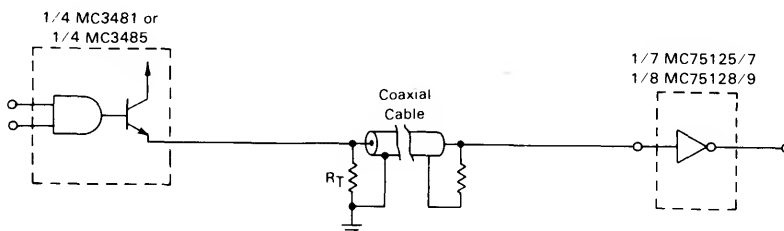
MC3481
DUAL ENABLE
INDIVIDUAL FAULT FLAG



MC3485
COMMON ENABLE
COMMON FAULT FLAG



TYPICAL APPLICATION



MC3481, MC3485

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+7.0	V
Input Voltage	V_I	10	V
Driver Output Voltage	V_O	5.5	V
Power Dissipation (Package Limitation)	P_D	1150	mW
Ceramic Package		962	
Plastic Package		7.7	mW/°C
Derate Above $T_A = 25^\circ\text{C}$	$1/R_{\theta JA}$		
Operating Ambient Temperature Range	T_A	0 to +70	°C
Junction Temperature	T_J	+175	°C
Ceramic Package		+150	
Storage Temperature Range	T_{stg}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.95	Vdc
High Level Output Current	I_{OH}	—	—	-59.3	mA
Operating Ambient Temperature Range	T_A	0	—	+70	°C

SWITCHING CHARACTERISTICS (See Note 1. Unless otherwise noted, these specifications apply over recommended temperature range. I/O Driver characteristics are guaranteed for $V_{CC} = 5.0\text{ V} \pm 10\%$ and Select-Out Driver characteristics are guaranteed for $V_{CC} = 5.25$ to 5.95 V . Typical values measured at $T_A = 25^\circ\text{C}$ and $V_{CC} = 5.0\text{ V}$. See Tables 1 and 2, Figures 1 and 2 for load conditions.)

Characteristics	Symbol	Min	Typ	Max	Unit
Propagation Delay Time					ns
High-to-Low-Level, Driver Output					
As I/O Driver	$t_{PHL}(D)$	—	18	—	
As Select-Out Driver	$t_{PHL}(DS)$	—	19	—	
Low-to-High-Level, Driver Output					
As I/O Driver	$t_{PLH}(D)$	—	20	—	
As Select-Out Driver	$t_{PLH}(DS)$	—	21	—	
High-to-Low-Level, Driver Output					
As I/O Driver	$t_{PHL}(\bar{D})$	—	25	—	
As Select-Out Driver	$t_{PHL}(\bar{DS})$	—	26	—	
Low-to-High-Level, Driver Output					
As I/O Driver	$t_{PLH}(\bar{D})$	—	25	—	
As Select-Out Driver	$t_{PLH}(\bar{DS})$	—	26	—	
High-to-Low-Level, Fault Flag — MC3481					
As I/O Driver	$t_{PHL}(\bar{F})$	—	45	—	
As Select-Out Driver	$t_{PHL}(\bar{FS})$	—	47	—	
Low-to-High-Level, Fault Flag — MC3481					
As I/O Driver	$t_{PLH}(\bar{F})$	—	40	—	
As Select-Out Driver	$t_{PLH}(\bar{FS})$	—	42	—	
Ratio of Propagation Delay Times					
As I/O Driver	$t_{PLH}(D)$	—	1.0	—	
	$t_{PHL}(D)$				

Notes 1. Reference IBM specification GA22-6974-3 for test terminology.

- The fault protection circuitry of the MC3481/85 requires relatively clean input voltage waveforms for current operation. Noise pulses which enter the threshold region (0.8 to 2.0 V) may cause the output to enter the fault protect mode. To exit the protect mode, it is necessary to gate an input of the effected driver to the low logic state.

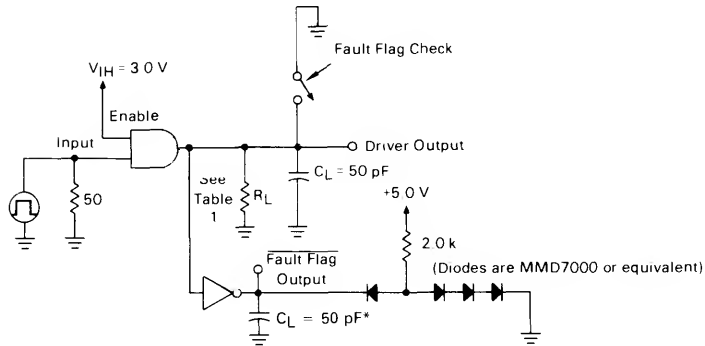
MC3481, MC3485

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, these specifications apply over recommended power supply and temperature ratings. Typical values measured at $T_A = 25^\circ\text{C}$ and $V_{CC} = +5.0\text{ V}$)

Characteristic	Symbol	MC3481			MC3485			Unit
		Min	Typ	Max	Min	Typ	Max	
High-Level Input Voltage Note 2	V_{IH}	2.0	—	—	2.0	—	—	V
Low-Level Input Voltage Note 2	V_{IL}	—	—	0.8	—	—	0.8	V
High-Level Input Current ($V_{CC} = 4.5\text{ V}$, $V_{IH} = 2.7\text{ V}$) - Input Enable ($V_{CC} = 4.5\text{ V}$, $V_{IH} = 5.5\text{ V}$) - Input Enable	I_{IH}	—	—	20 40 100 200	—	—	20 80 100 400	μA
Low-Level Input Current ($V_{CC} = 5.95\text{ V}$, $V_{IL} = 0.4\text{ V}$) - Input Enable	I_{IL}	—	—	-250 -500	—	—	-250 -1000	μA
Input Clamp Voltage ($I_{IC} = -18\text{ mA}$)	V_{IC}	—	—	-1.5	—	—	-1.5	V
High-Level Driver Output Voltage ($V_{CC} = 4.5\text{ V}$, $V_{IH} = 2.0\text{ V}$, $I_{OH} = -59.3\text{ mA}$) ($V_{CC} = 5.25\text{ V}$, $V_{IH} = 2.0\text{ V}$, $I_{OH} = -41\text{ mA}$)	$V_{OH(D)}$ $V_{OH(DS)}$	3.11 3.9	3.6 —	— —	3.11 3.9	3.6 —	— —	V
Low-Level Driver Output Voltage ($V_{CC} = 5.5\text{ V}$, $V_{IL} = 0.8\text{ V}$, $I_{OL} = -240\text{ }\mu\text{A}$) ($V_{CC} = 5.95\text{ V}$, $V_{IL} = 0.8\text{ V}$, $I_{OL} = -1.0\text{ mA}$)	$V_{OL(D)}$ $V_{OL(DS)}$	—	—	+0.15 +0.15	—	—	+0.15 +0.15	V
Driver Output Short Circuit Current ($V_{CC} = 5.5\text{ V}$, $V_{IH} = 2.0\text{ V}$, $V_{OS} = 0\text{ V}$) ($V_{CC} = 5.95\text{ V}$, $V_{IH} = 2.0\text{ V}$, $V_{OS} = 0\text{ V}$)	$I_{OS(D)}$ $I_{OS(DS)}$	—	—	-5.0 -5.0	—	—	-5.0 -5.0	mA
Driver Output Reverse Leakage Current ($V_{CC} = 4.5\text{ V}$, $V_{IL} = 0\text{ V}$, $V_O = 3.11\text{ V}$) ($V_{CC} = 0\text{ V}$, $V_{IL} = 0\text{ V}$, $V_O = 3.11\text{ V}$)	I_{OR1} I_{OR2}	—	—	+100 +200	—	—	+100 +200	μA
High-Level Driver Output Voltage ($V_{CC} = 4.5\text{ V}$, $V_{IL} = 0.8\text{ V}$, $I_{OH} = -400\text{ }\mu\text{A}$)	$V_{OH(\bar{D})}$	—	—	—	2.5	3.0	—	V
Low-Level Driver Output Voltage ($V_{CC} = 4.5\text{ V}$, $V_{IH} = 2.0\text{ V}$, $I_{OL} = +8.0\text{ mA}$)	$V_{OL(\bar{D})}$	—	—	—	—	—	0.5	V
Driver Output Short Circuit Current ($V_{CC} = 5.5\text{ V}$, $V_{OS} = 0\text{ V}$, only one output shorted at a time) ($V_{CC} = 5.95\text{ V}$, $V_{OS} = 0\text{ V}$, only one output shorted at a time)	$I_{OS(\bar{D})}$ $I_{OS(\bar{DS})}$	—	—	— —	-15 -15	-60 —	-100 -110	mA
High-Level Fault Flag Output Voltage ($V_{CC} = 4.5\text{ V}$, $I_{OH} = -400\text{ }\mu\text{A}$)	$V_{OH(\bar{F})}$	2.5	3.0	—	—	—	—	V
Low-Level Fault Flag Output Voltage ($V_{CC} = 4.5\text{ V}$, $V_{IH} = 2.0\text{ V}$, $I_{OL} = +8.0\text{ mA}$, Driver Output shorted to Ground)	$V_{OL(\bar{F})}$	—	—	0.5	—	—	0.5	V
Fault Flag Output Short Circuit Current ($V_{CC} = 5.5\text{ V}$, $V_{OS} = 0\text{ V}$, only one output shorted at a time) ($V_{CC} = 5.95\text{ V}$, $V_{OS} = 0\text{ V}$, only one output shorted at a time)	$I_{OS(\bar{F})}$ $I_{OS(\bar{FS})}$	-15 -15	— —	-100 -110	— —	— —	— —	mA
High-Level Fault Flag Output Current ($V_{CC} = 5.95\text{ V}$, $V_{OH} = 5.95\text{ V}$)	$I_{OH(\bar{F})}$	—	—	—	—	—	+100	μA
High-Level Power Supply Current ($V_{CC} = 5.5\text{ V}$, $V_{IH} = 2.0\text{ V}$, no output loading) ($V_{CC} = 5.95\text{ V}$, $V_{IH} = 2.0\text{ V}$, no output loading)	I_{CCH} I_{CCHS}	— —	50 —	70 80	— —	55 —	75 85	mA
Low-Level Power Supply Current ($V_{CC} = 5.5\text{ V}$, $V_{IL} = 0.8\text{ V}$, no output loading) ($V_{CC} = 5.95\text{ V}$, $V_{IL} = 0.8\text{ V}$, no output loading)	I_{CCL} I_{CCLS}	— —	35 —	55 70	— —	35 —	55 70	mA

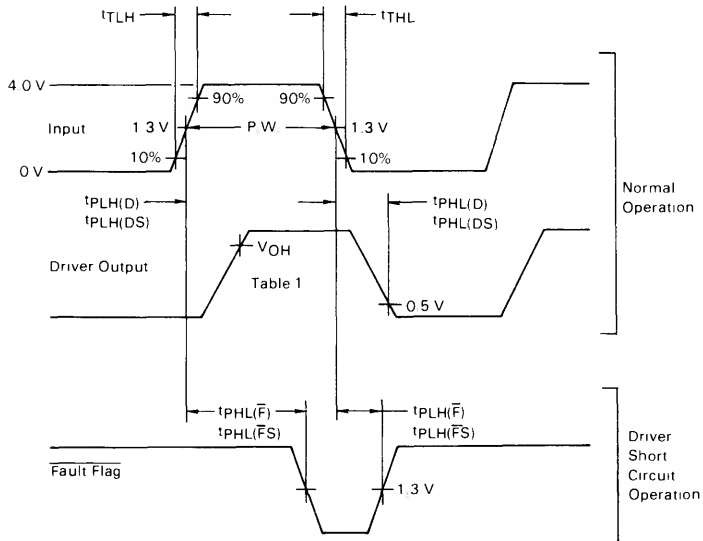
MC3481, MC3485

FIGURE 1 — MC3481 AC TEST CIRCUIT AND WAVEFORMS



* Load Capacitance shown includes Fixture and Probe Capacitance

Table 1	Driver Application	
	I/O	Select-Out
V_{OH}	3.11 V	3.9 V
Input Frequency	5 MHz	1 MHz
Input Pulse Width	100 ns	500 ns
Input Amplitude	0 V to 4 V	0 V to 4 V
Input t_{LH}	≤ 6 ns	≤ 6 ns
Input t_{HL}	≤ 6 ns	≤ 6 ns
Load Resistance (R_L)	50	90



MC3481, MC3485

FIGURE 2 — MC3485 AC TEST CIRCUIT AND WAVEFORMS

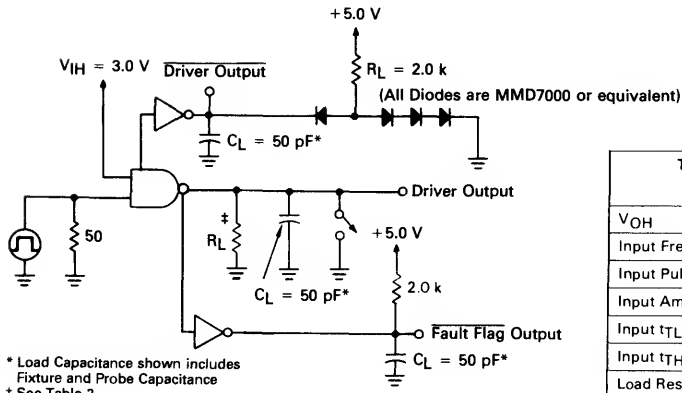
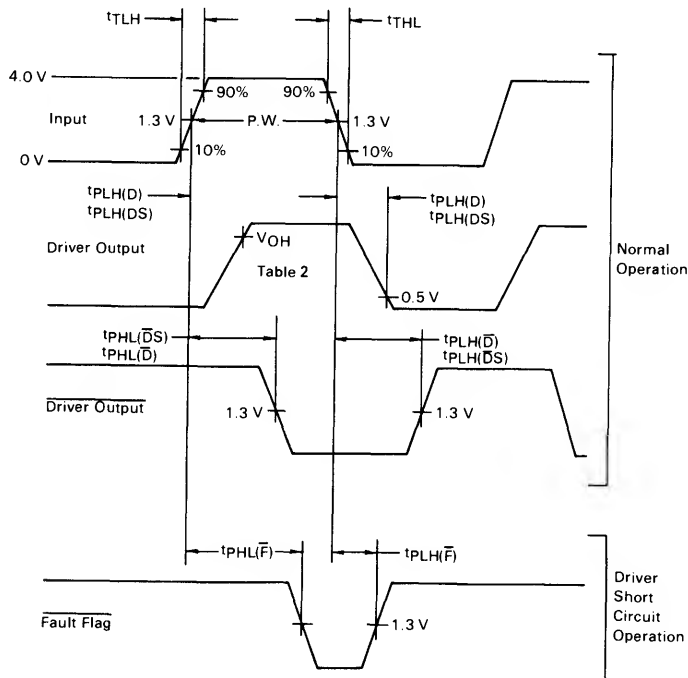


Table 2	Driver Application	
	I/O	Select-Out
V_{OH}	3.11 V	3.9 V
Input Frequency	5 MHz	1 MHz
Input Pulse Width	100 ns	500 ns
Input Amplitude	0 V to 4 V	0 V to 4 V
Input t_{TLH}	≤ 6 ns	≤ 6 ns
Input t_{THL}	≤ 6 ns	≤ 6 ns
Load Resistance (R_L)	50	90

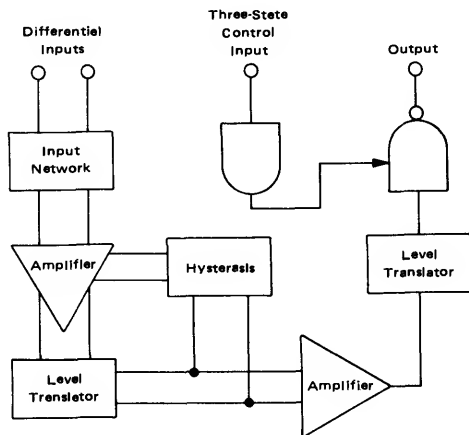


QUAD EIA-422/423 LINE RECEIVER

Motorola's Quad EIA-422/3 Receiver features four independent receiver chains which comply with EIA Standards for the Electrical Characteristics of Balanced/Unbalanced Voltage Digital Interface Circuits. Receiver outputs are 74LS compatible, three-state structures which are forced to a high impedance state when the appropriate output control pin reaches a logic zero condition. A PNP device buffers each output control pin to assure minimum loading for either logic one or logic zero inputs. In addition, each receiver chain has internal hysteresis circuitry to improve noise margin and discourage output instability for slowly changing input waveforms. A summary of MC3486 features include:

- Four Independent Receiver Chains
- Three-State Outputs
- High Impedance Output Control Inputs (PIA Compatible)
- Internal Hysteresis ~ 30 mV (Typ) @ Zero Volts Common Mode
- Fast Propagation Times ~ 25 ns (Typ)
- TTL Compatible
- Single 5.0 V Supply Voltage
- DS 3486 Provides Second Source

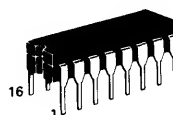
RECEIVER CHAIN BLOCK DIAGRAM



MC3486

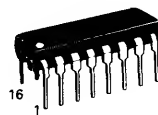
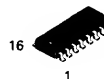
QUAD EIA-422/3 LINE RECEIVER WITH THREE-STATE OUTPUTS

SILICON MONOLITHIC
INTEGRATED CIRCUIT



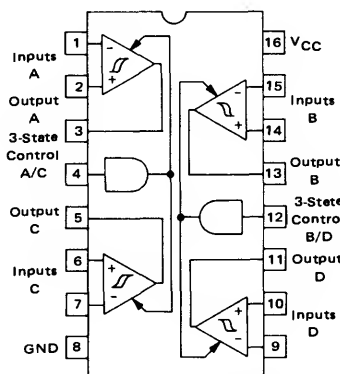
L SUFFIX
CERAMIC PACKAGE
CASE 620

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO-16)



P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
MC3486L	0 to +70°C	Ceramic DIP
MC3486P		Plastic DIP
MC3486D		SO-16

MC3486

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.0	Vdc
Input Common Mode Voltage	V_{ICM}	± 15	Vdc
Input Differential Voltage	V_{ID}	± 25	Vdc
Three-State Control Input Voltage	V_I	8.0	Vdc
Output Sink Current	I_O	50	mA
Storage Temperature	T_{stg}	-65 to +150	$^{\circ}\text{C}$
Operating Junction Temperature	T_J		$^{\circ}\text{C}$
Ceramic Package		+175	
Plastic Package		+150	

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	4.75 to 5.25	Vdc
Operating Ambient Temperature	T_A	0 to +70	$^{\circ}\text{C}$
Input Common Mode Voltage Range	V_{ICR}	-7.0 to +7.0	Vdc
Input Differential Voltage Range	V_{IDR}	6.0	Vdc

ELECTRICAL CHARACTERISTICS (Unless otherwise noted minimum and maximum limits apply over recommended temperature and power supply voltage ranges. Typical values are for $T_A = 25^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V}$ and $V_{IK} = 0\text{ V}$. See Note 1.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage — High Logic State (Three-State Control)	V_{IH}	2.0	—	—	V
Input Voltage — Low Logic State (Three-State Control)	V_{IL}	—	—	0.8	V
Differential Input Threshold Voltage, Note 2 ($-7.0\text{ V} \leq V_{IC} \leq 7.0\text{ V}$, $V_{IH} = 2.0\text{ V}$) ($I_O = -0.4\text{ mA}$, $V_{OH} \geq 2.7\text{ V}$) ($I_O = 8.0\text{ mA}$, $V_{OL} \geq 0.5\text{ V}$)	$V_{TH(D)}$	—	—	0.2 -0.2	V
Input Bias Current ($V_{CC} = 0\text{ V}$ or 5.25) (Other Inputs at 0 V) ($V_I = -10\text{ V}$) ($V_I = -3.0\text{ V}$) ($V_I = +3.0\text{ V}$) ($V_I = +10\text{ V}$)	$I_{IB(D)}$	—	—	-3.25 -1.50 +1.50 +3.25	mA
Input Balance and Output Level ($-7.0\text{ V} \leq V_{IC} \leq 7.0\text{ V}$, $V_{IH} = 2.0\text{ V}$, Note 3) ($I_O = -0.4\text{ mA}$, $V_{ID} = 0.4\text{ V}$) ($I_O = 8.0\text{ mA}$, $V_{ID} = -0.4\text{ V}$)	V_{OH} V_{OL}	2.7 —	— —	— 0.5	V
Output Third State Leakage Current ($V_{I(D)} = +3.0\text{ V}$, $V_{IL} = 0.8\text{ V}$, $V_{OL} = 0.5\text{ V}$) ($V_{I(D)} = -3.0\text{ V}$, $V_{IL} = 0.8\text{ V}$, $V_{OH} = 2.7\text{ V}$)	I_{OZ}	—	—	-40 40	μA
Output Short-Circuit Current ($V_{I(D)} = 3.0\text{ V}$, $V_{IH} = 2.0\text{ V}$, $V_O = 0\text{ V}$, Note 4)	I_{OS}	-15	—	-100	mA
Input Current — Low Logic State (Three-State Control) ($V_{IL} = 0.5\text{ V}$)	I_{IL}	—	—	-100	μA
Input Current — High Logic State (Three-State Control) ($V_{IH} = 2.7\text{ V}$) ($V_{IH} = 5.25\text{ V}$)	I_{IH}	—	—	20 100	μA
Input Clamp Diode Voltage (Three-State Control) ($I_{IK} = -10\text{ mA}$)	V_{IK}	—	—	-1.5	V
Power Supply Current ($V_{IL} = 2.0\text{ V}$)	I_{CC}	—	—	85	mA

NOTES:

1. All currents into device pins are shown as positive, out of device pins are negative. All voltages referenced to ground unless otherwise noted.
2. Differential input threshold voltage and guaranteed output levels are done simultaneously for worst case.
3. Refer to EIA-422/3 for exact conditions. Input balance and guaranteed output levels are done simultaneously for worst case.
4. Only one output at a time should be shorted.

MC3486

SWITCHING CHARACTERISTICS (Unless otherwise noted, $V_{CC} = 5.0\text{ V}$ and $T_A = 25^\circ\text{C}$.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time – Differential Inputs to Output (Output High to Low) (Output Low to High)	$t_{PHL}(D)$ $t_{PLH}(D)$	— —	— —	35 30	ns
Propagation Delay time – Three-State Control to Output (Output Low to Third State) (Output High to Third State) (Output Third State to High) (Output Third State to Low)	t_{PLZ} t_{PHZ} t_{PZH} t_{PZL}	— — — —	— — — —	35 35 30 30	ns

FIGURE 1 – SWITCHING TEST CIRCUIT AND WAVEFORMS

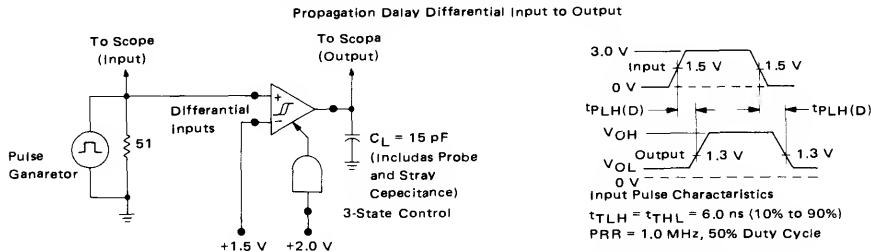
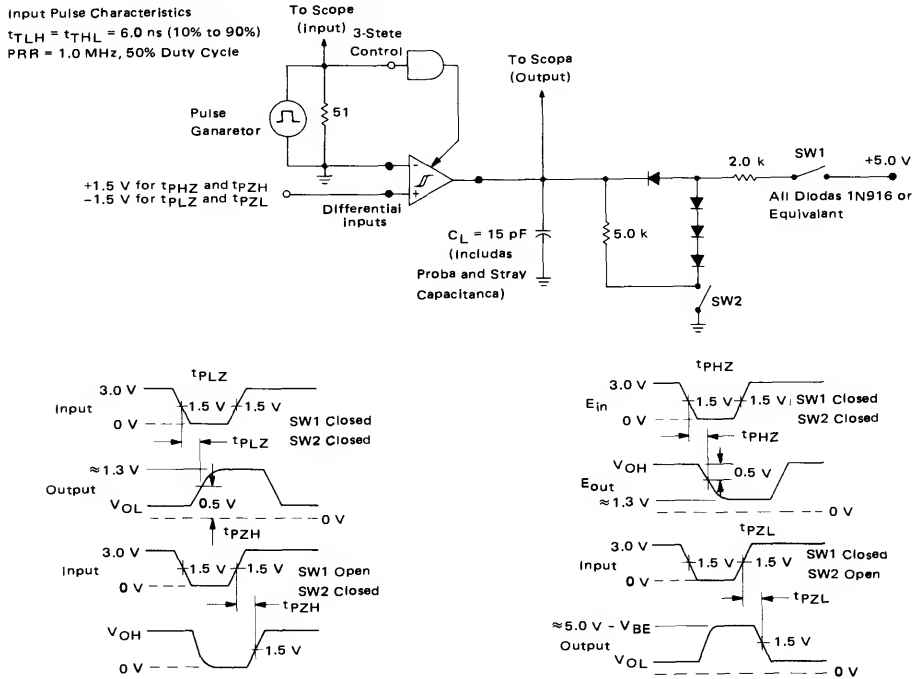


FIGURE 2 – PROPAGATION DELAY THREE-STATE CONTROL INPUT TO OUTPUT



MC3487

QUAD LINE DRIVER WITH THREE-STATE OUTPUTS

Motorola's Quad EIA-422 Driver features four independent driver chains which comply with EIA Standards for the Electrical Characteristics of Balanced Voltage Digital Interface Circuits. The outputs are three-state structures which are forced to a high impedance state when the appropriate output control pin reaches a logic zero condition. All input pins are PNP buffered to minimize input loading for either logic one or logic zero inputs. In addition, internal circuitry assures a high impedance output state during the transition between power up and power down. A summary of MC3487 features include:

- Four Independent Driver Chains
- Three-State Outputs
- PNP High Impedance Inputs (PIA Compatible)
- Fast Propagation Times (Typ 15 ns)
- TTL Compatible
- Single 5 V Supply Voltage
- Output Rise and Fall Times Less Than 20 ns
- DS 3487 Provides Second Source

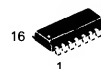
QUAD EIA-422 LINE DRIVER WITH THREE-STATE OUTPUTS

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**



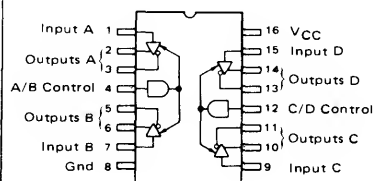
L SUFFIX
CERAMIC PACKAGE
CASE 620

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO-16)

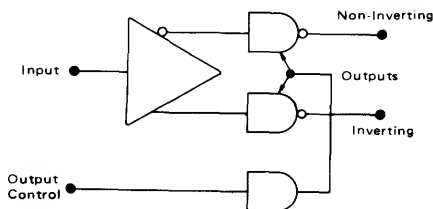


P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS



DRIVER BLOCK DIAGRAM



TRUTH TABLE

Input	Control Input	Non-Inverting Output	Inverting Output
H	H	H	L
L	H	L	H
X	L	Z	Z

L = Low Logic State
H = High Logic State
X = Irrelevant
Z = Third-State (High Impedance)

MC3487

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.0	Vdc
Input Voltage	V_I	5.5	Vdc
Operating Ambient Temperature Range	T_A	0 to +70	°C
Operating Junction Temperature Range	T_J		°C
Ceramic Package		175	
Plastic Package		150	
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted specifications apply $4.75\text{ V} \leq V_{CC} \leq 5.25\text{ V}$ and $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$.
Typical values measured at $V_{CC} = 5.0\text{ V}$, and $T_A = 25^\circ\text{C}$.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage — Low Logic State	V_{IL}	—	—	0.8	Vdc
Input Voltage — High Logic State	V_{IH}	2.0	—	—	Vdc
Input Current — Low Logic State ($V_{IL} = 0.5\text{ V}$)	I_{IL}	—	—	-400	μA
Input Current — High Logic State ($V_{IH} = 2.7\text{ V}$) ($V_{IH} = 5.5\text{ V}$)	I_{IH}	— —	— —	+50 +100	μA
Input Clamp Voltage ($I_{IK} = -18\text{ mA}$)	V_{IK}	—	—	-1.5	V
Output Voltage — Low Logic State ($I_{OL} = 48\text{ mA}$)	V_{OL}	—	—	0.5	V
Output Voltage — High Logic State ($I_{OH} = -20\text{ mA}$)	V_{OH}	2.5	—	—	V
Output Short-Circuit Current ($V_{IH} = 2.0\text{ V}$, Note 1)	I_{OS}	-40	—	-140	mA
Output Leakage Current — Hi-Z State ($V_{IL} = 0.5\text{ V}$, $V_{IL}(Z) = 0.8\text{ V}$) ($V_{IH} = 2.7\text{ V}$, $V_{IL}(Z) = 0.8\text{ V}$)	$I_{OL}(Z)$	— —	— —	± 100 ± 100	μA
Output Leakage Current — Power OFF ($V_{OH} = 6.0\text{ V}$, $V_{CC} = 0\text{ V}$) ($V_{OL} = -0.25\text{ V}$, $V_{CC} = 0\text{ V}$)	$I_{OL(off)}$	— —	— —	+100 -100	μA
Output Offset Voltage Difference (Note 2)	$V_{OS} - \bar{V}_{OS}$	—	—	± 0.4	V
Output Differential Voltage (Note 2)	V_{OD}	2.0	—	—	V
Output Differential Voltage Difference (Note 2)	$ \Delta V_{OD} $	—	—	± 0.4	V
Power Supply Current (Control Pins = Gnd, Note 3) (Control Pins = 2.0 V)	I_{CCX} I_{CC}	— —	— —	105 85	mA

Notes: 1. Only one output may be shorted at a time.
2. See EIA Specification EIA-422 for exact test conditions.
3. Circuit in three-state condition.

SWITCHING CHARACTERISTICS

($V_{CC} = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Times High to Low Output Low to High Output	t_{PHL} t_{PLH}	— —	— —	20 20	ns
Output Transition Times — Differential High to Low Output Low to High Output	t_{THL} t_{TLH}	— —	— —	20 20	ns
Propagation Delay — Control to Output ($R_L = 200\ \Omega$, $C_L = 50\text{ pF}$) ($R_L = 200\ \Omega$, $C_L = 50\text{ pF}$) ($R_L = \infty$, $C_L = 50\text{ pF}$) ($R_L = 200\ \Omega$, $C_L = 50\text{ pF}$)	$t_{PHZ(E)}$ $t_{PLZ(E)}$ $t_{PZH(E)}$ $t_{PZL(E)}$	— — — —	— — — —	25 25 30 30	ns

FIGURE 1 – THREE-STATE ENABLE TEST CIRCUIT AND WAVEFORMS

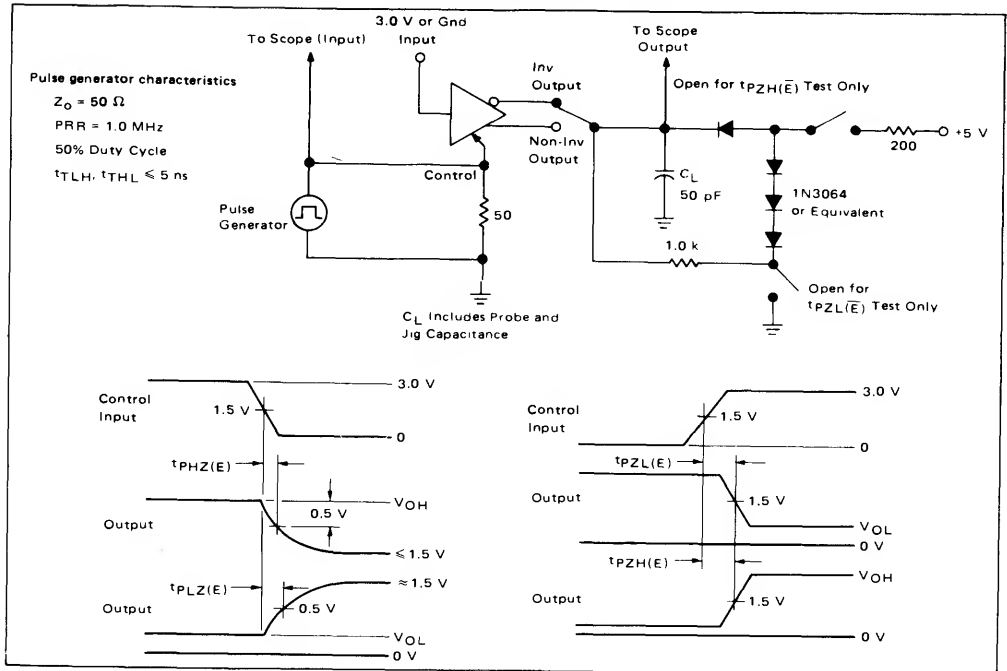
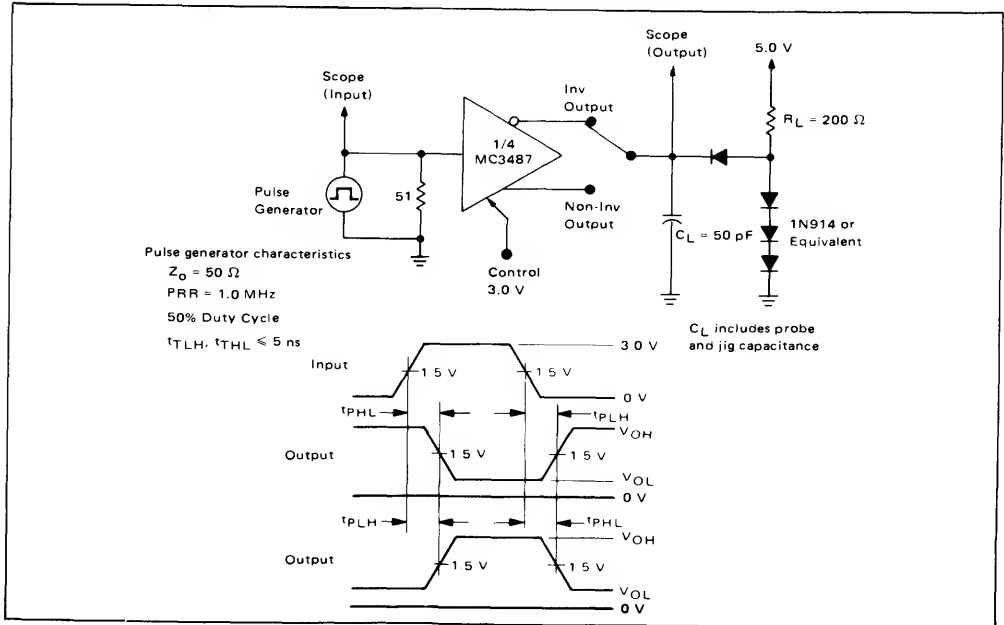


FIGURE 2 – PROPAGATION DELAY TIMES INPUT TO OUTPUT WAVEFORMS AND TEST CIRCUIT



MC3487

FIGURE 3 – OUTPUT TRANSITION TIMES TEST CIRCUIT AND WAVEFORMS

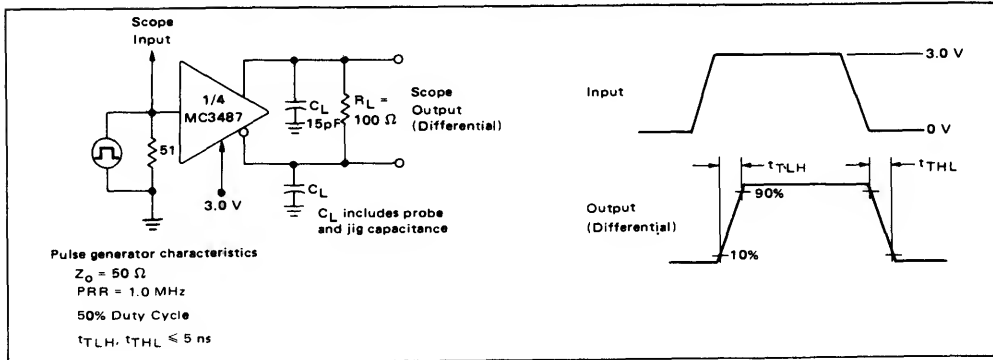


FIGURE 4 – OUTPUT CURRENT versus OUTPUT VOLTAGE

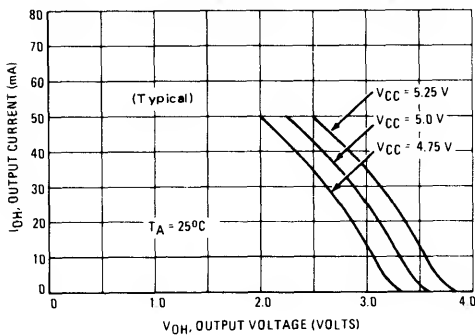
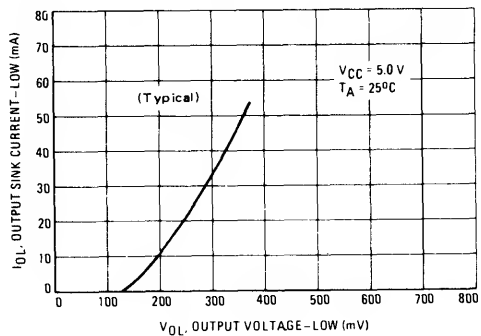


FIGURE 5 – OUTPUT SINK CURRENT versus OUTPUT VOLTAGE



MC3488A

DUAL
EIA-423/EIA-232D
DRIVER

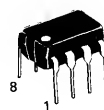
SILICON MONOLITHIC
INTEGRATED CIRCUIT

DUAL EIA-423/EIA-232D LINE DRIVER

The MC3488A dual single-ended line driver has been designed to satisfy the requirements of EIA standards EIA-423 and EIA-232D, as well as CCITT X.26, X.28 and Federal Standard FIDS1030. It is suitable for use where signal wave shaping is desired and the output load resistance is greater than 450 ohms. Output slew rates are adjustable from 1.0 μ s to 100 μ s by a single external resistor. Output level and slew rate are insensitive to power supply variations. Input undershoot diodes limit transients below ground and output current limiting is provided in both output states.

The MC3488A has a standard 1.5 V input logic threshold for TTL or NMOS compatibility.

- PNP Buffered Inputs to Minimize Input Loading
- Short Circuit Protection
- Adjustable Slew Rate Limiting
- MC3488A Equivalent to 9636A
- Output Levels and Slew Rates are Insensitive to Power Supply Voltages
- No External Blocking Diode Required for V_{EE} Supply
- Second Source μ A9636A

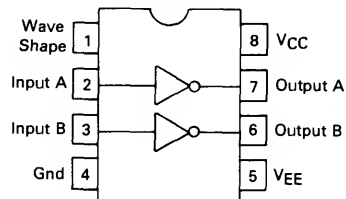


P1 SUFFIX
PLASTIC PACKAGE
CASE 626

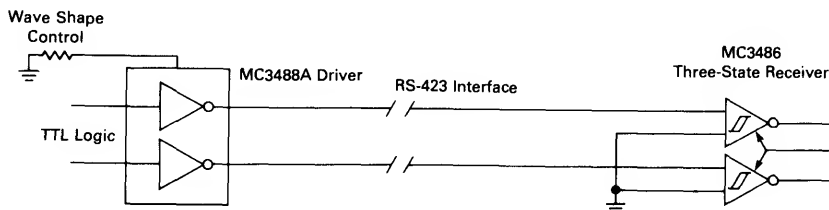
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)



PIN CONNECTIONS



TYPICAL APPLICATION



MC3488A

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltages	V _{CC} V _{EE}	+15 -15	V
Output Current Source Sink	I _{O+} I _{O-}	+150 -150	mA
Operating Ambient Temperature	T _A	0 to +70	°C
Junction Temperature Range Ceramic Package Plastic Package	T _J	175 150	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltages	V _{CC} V _{EE}	10.8 -13.2	12 -12	13.2 -10.8	V
Operating Temperature Range	T _A	0	25	70	°C
Wave Shaping Resistor	R _{WS}	10	—	1000	kΩ

TARGET ELECTRICAL CHARACTERISTICS (Unless otherwise noted specifications apply over recommended operating conditions)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage — Low Logic State	V _{IL}	—	—	0.8	V
Input Voltage — High Logic State	V _{IH}	2.0	—	—	V
Input Current — Low Logic State (V _{IL} = 0.4 V)	I _{IL}	-80	—	—	μA
Input Current — High Logic State (V _{IH} = 2.4 V) (V _{IH} = 5.5 V)	I _{IH1} I _{IH2}	— —	— —	10 100	μA
Input Clamp Diode Voltage (I _{IK} = -15 mA)	V _{IK}	-1.5	—	—	V
Output Voltage — Low Logic State (R _L = ∞) EIA-423 (R _L = 3.0 kΩ) EIA-232D (R _L = 450 Ω) EIA-423	V _{OL}	-6.0 -6.0 -6.0	— — —	-5.0 -5.0 -4.0	V
Output Voltage — High Logic State (R _L = ∞) EIA-423 (R _L = 3.0 kΩ) EIA-232D (R _L = 450 Ω) EIA-423	V _{OH}	5.0 5.0 4.0	— — —	6.0 6.0 6.0	V
Output Resistance (R _L ≥ 450 Ω)	R _O	—	25	50	Ω
Output Short-Circuit Current (Note 2) (V _{in} = V _{out} = 0 V) (V _{in} = V _{IH} (Min), V _{out} = 0 V)	I _{OSH} I _{OSL}	-150 +15	— —	-15 +150	mA
Output Leakage Current (Note 3) (V _{CC} = V _{EE} = 0 V, -6.0 V ≤ V _O ≤ 6.0 V)	I _{ox}	-100	—	100	μA
Power Supply Currents (R _W = 100 kΩ, R _L = ∞, V _{IL} ≤ V _{in} ≤ V _{IH})	I _{CC} I _{EE}	— -18	— —	+18 —	mA

Note 1: Devices should not be operated at these values. The "Electrical Characteristics" provide conditions for actual device operation.

2: One output shorted at a time.

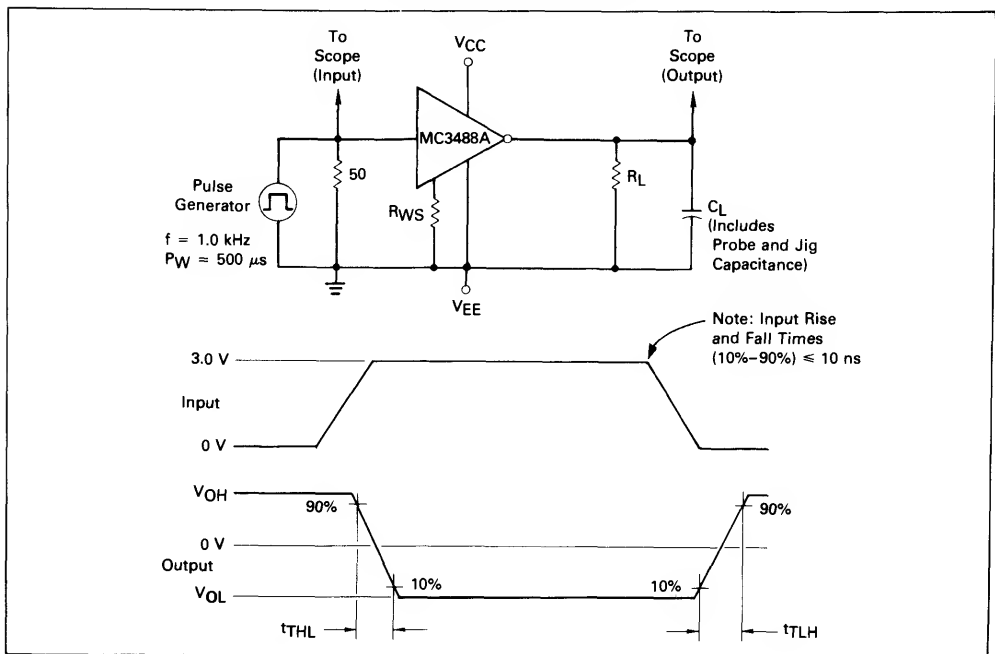
3: No V_{EE} diode required.

MC3488A

TRANSITION TIMES (Unless otherwise noted, $C_L = 30$ pF, $f = 1.0$ kHz, $V_{CC} = -V_{EE} = 12.0$ V $\pm 10\%$, $T_A = 25^\circ\text{C}$, $R_L = 450$ Ω . Transition times measured 10% to 90% and 90% to 10%)

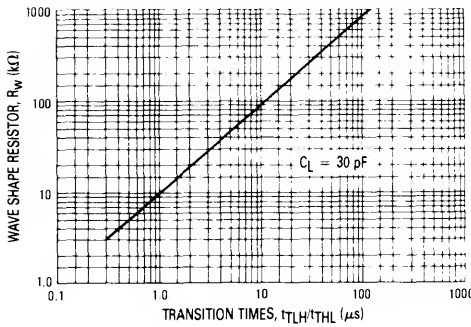
Characteristic	Symbol	Min	Typ	Max	Unit
Transition Time, Low-to-High State Output ($R_W = 10$ k Ω) ($R_W = 100$ k Ω) ($R_W = 500$ k Ω) ($R_W = 1000$ k Ω)	t_{TLH}	0.8 8.0 40 80	— — — —	1.4 14 70 140	μs
Transition Time, High-to-Low State Output ($R_W = 10$ k Ω) ($R_W = 100$ k Ω) ($R_W = 500$ k Ω) ($R_W = 1000$ k Ω)	t_{THL}	0.8 8.0 40 80	— — — —	1.4 14 70 140	μs

FIGURE 1 — TEST CIRCUIT AND WAVEFORMS FOR TRANSITION TIMES



MC3488A

**FIGURE 2 — OUTPUT TRANSITION TIMES
versus WAVE SHAPE RESISTOR VALUE**



**FIGURE 3 — INPUT/OUTPUT CHARACTERISTICS
versus TEMPERATURE**

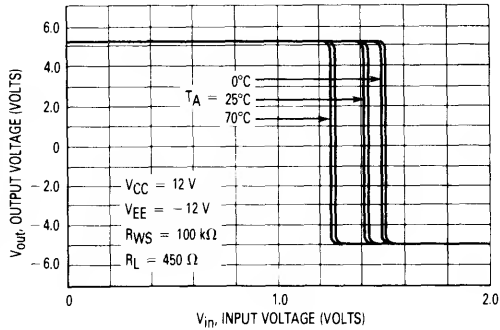
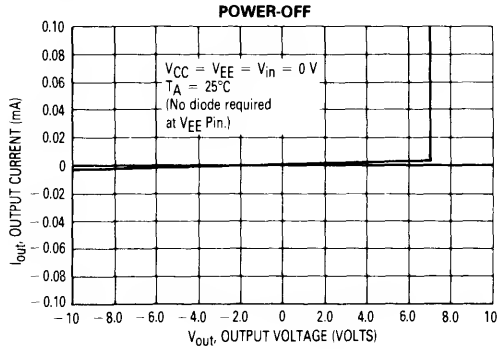
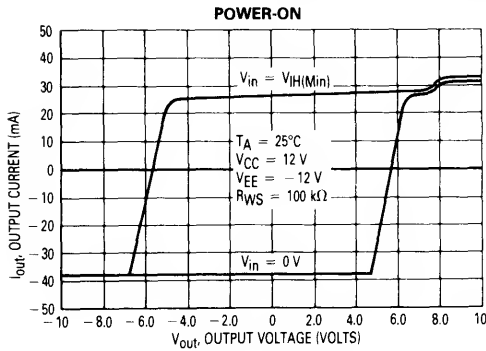


FIGURE 4 — OUTPUT CURRENT versus OUTPUT VOLTAGE



**FIGURE 5 — SUPPLY CURRENT versus
TEMPERATURE**

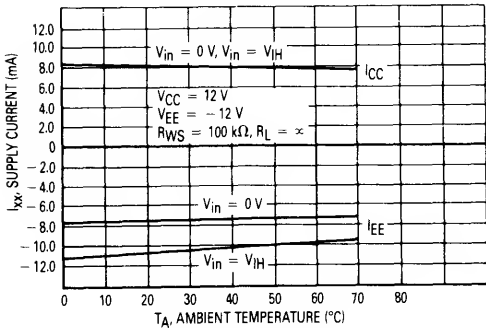
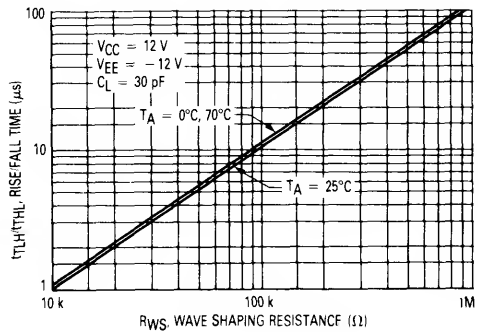


FIGURE 6 — RISE/FALL TIME versus R_{WS}



M6800 CLOCK GENERATOR

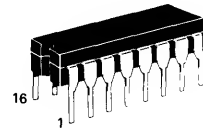
Intended to supply the non-overlapping $\phi 1$ and $\phi 2$ clock signals required by the microprocessor, this clock generator is compatible with 1.0, 1.5, and 2.0 MHz versions of the MC6800. Both the oscillator and high capacitance driver elements are included along with numerous other logic accessory functions for easy system expansion.

Schottky technology is employed for high speed and PNP-buffered inputs are employed for NMOS compatibility. A single +5 V power supply, and a crystal or RC network for frequency determination are required.

MC6875 MC6875A

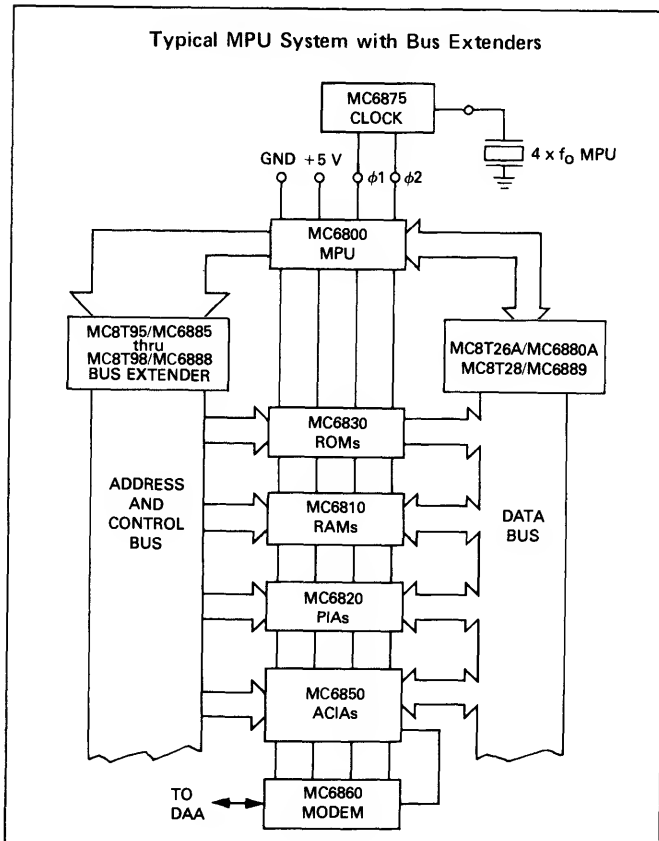
M6800 TWO-PHASE CLOCK GENERATOR/DRIVER

SCHOTTKY MONOLITHIC INTEGRATED CIRCUIT

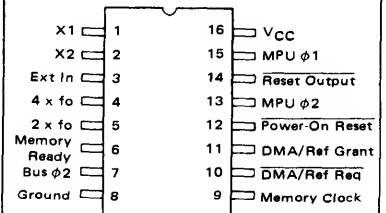


L SUFFIX
CERAMIC PACKAGE
CASE 620

Typical MPU System with Bus Extenders



PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
MC6875L	0 to +70°C	Ceramic DIP
MC6875AL	-55 to +125°C	

MC6875, MC6875A

MAXIMUM RATINGS (Unless otherwise noted $T_A = 25^{\circ}\text{C}$.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+7.0	Vdc
Input Voltage	V_I	+5.5	Vdc
Operating Ambient Temperature Range MC6875L MC6875AL	T_A	0 to +70 -55 to +125	$^{\circ}\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^{\circ}\text{C}$
Operating Junction Temperature	T_J	175	$^{\circ}\text{C}$

NOTE:

Operation of the MC6875AL over the full military temperature range (to maximum T_A) will result in excessive operating junction temperature.

The use of a clip on 16 pin heat sink similar to AAVID Engineering, Inc., Model 5007 ($R_{\theta CA} = 18^{\circ}\text{C/W}$) is recommended above $T_A = 95^{\circ}\text{C}$.

Contact AAVID Engineering, Inc.
30 Cook Court
Laconia, New Hampshire 03246
Tel. (603) 524-4443

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+4.75 to +5.25	Vdc

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted specifications apply over recommended power supply and temperature ranges. Typical values measured at $V_{CC} = 5.0\text{ V}$ and $T_A = 25^{\circ}\text{C}$.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage — High Logic State MPU $\phi 1$ and $\phi 2$ Outputs ($V_{CC} = 4.75\text{ V}$, $I_{OHM} = -200\text{ }\mu\text{A}$) ($V_{CC} = 5.25\text{ V}$, $I_{OHMK} = +5.0\text{ mA}$)	V_{OHM} V_{OHMK}	$V_{CC} - 0.6$ —	— —	— $V_{CC} + 1.0$	V
Bus $\phi 2$ Output ($V_{CC} = 4.75\text{ V}$, $I_{OHB} = -10\text{ mA}$) ($V_{CC} = 5.25\text{ V}$, $I_{OHBK} = +5.0\text{ mA}$)	V_{OHB} V_{OHBK}	2.4 —	— —	— $V_{CC} + 1.0$	V
4 x $\phi 0$ Output ($V_{CC} = 4.75\text{ V}$, $V_{IH} = 2.0\text{ V}$, $I_{OH4X} = -500\text{ }\mu\text{A}$)	V_{OH4X}	2.4	—	—	V
2 x $\phi 0$, DMA/Refresh Grant and Memory Clock Outputs ($V_{CC} = 4.75\text{ V}$, $I_{OH} = -500\text{ }\mu\text{A}$)	V_{OH}	2.4	—	—	V
Reset Output ($V_{CC} = 4.75\text{ V}$, $V_{IH} = 3.3\text{ V}$, $I_{OHR} = -100\text{ }\mu\text{A}$)	V_{OHR}	2.4	—	—	V
Output Voltage — Low Logic State MPU $\phi 1$ and $\phi 2$ Outputs ($V_{CC} = 4.75\text{ V}$, $I_{OLM} = +200\text{ }\mu\text{A}$) ($V_{CC} = 4.75\text{ V}$, $I_{OLMK} = -5.0\text{ mA}$)	V_{OLM} V_{OLMK}	— —	— —	0.4 -1.0	V
Bus $\phi 2$ Output ($V_{CC} = 4.75\text{ V}$, $I_{OLB} = +48\text{ mA}$) ($V_{CC} = 4.75\text{ V}$, $I_{OLBK} = -5.0\text{ mA}$)	V_{OLB} V_{OLBK}	— —	— —	0.5 -1.0	V
4 x $\phi 0$ Output ($V_{CC} = 4.75\text{ V}$, $V_{IL} = 0.8\text{ V}$, $I_{OL4X} = 16\text{ mA}$)	V_{OL4X}	—	—	0.5	V
2 x $\phi 0$, DMA/Refresh Grant and Memory Clock Outputs ($V_{CC} = 4.75\text{ V}$, $I_{OL} = 16\text{ mA}$)	V_{OL}	—	—	0.5	V
Reset Output ($V_{CC} = 4.75\text{ V}$, $V_{IL} = 0.8\text{ V}$, $I_{OLR} = 3.2\text{ mA}$)	V_{OLR}	—	—	0.5	V
Input Voltage — High Logic State Ext. In, Memory Ready and DMA/Refresh Request Inputs	V_{IH}	2.0	—	—	V
Input Voltage — Low Logic State Ext. In, Memory Ready and DMA/Refresh Request Inputs	V_{IL}	—	—	0.8	V
Input Thresholds — Power-On Reset Input (See Figure 2) Output Low to High Output High to Low	V_{ILH} V_{IHL}	— 0.8	2.8 1.4	3.6 —	V
Input Clamp Voltage ($V_{CC} = 4.75\text{ V}$, $I_{IC} = -5.0\text{ mA}$)	V_{IK}	— —	— —	-1.0 -1.5	V
Input Current — High Logic State Ext. In, Memory Ready and DMA/Refresh Request Inputs ($V_{CC} = 4.75\text{ V}$, $V_{IH} = 5.0\text{ V}$) Power-On Reset ($V_{CC} = 5.0\text{ V}$, $V_{IHR} = 5.0\text{ V}$)	I_{IH} I_{IHR}	— —	— —	25 50	μA
Input Current — Low Logic State Ext. In, Memory Ready and DMA/Refresh Request Inputs ($V_{CC} = 5.25\text{ V}$, $V_{IL} = 0.5\text{ V}$) Power-On Reset Input ¹ ($V_{CC} = 5.25\text{ V}$, $V_{IL} = 0.5\text{ V}$)	I_{IL} I_{ILR}	— —	— —	-250 -250	μA

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OPERATING DYNAMIC POWER SUPPLY CURRENT

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Currents ($V_{CC} = 5.25\text{ V}$, $f_{osc} = 8.0\text{ MHz}$, $V_{IL} = 0\text{ V}$, $V_{IH} = 3.0\text{ V}$)					
Normal Operation (Memory Ready and DMA/Refresh Request Inputs at High Logic State)	I_{CCN}	—	—	150	mA
Memory Ready Stretch Operation (Memory Ready Input at Low Logic State; DMA/Refresh Request Input at High Logic State)	I_{CCMR}	—	—	135	mA
DMA/Refresh Request Stretch Operation (Memory Ready Input at High Logic State; DMA/Refresh Request Input at Low Logic State)	I_{CCDR}	—	—	135	mA

SWITCHING CHARACTERISTICS

(These specifications apply whether the Internal Oscillator (see Figure 9) or an External Oscillator is used (see Figure 10). Typical values measured at $V_{CC} = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$, $f_o = 1.0\text{ MHz}$ (see Figure 8).

Characteristic	Symbol	Min	Typ	Max	Unit
MPU $\phi 1$ AND $\phi 2$ CHARACTERISTICS					
Output Period (Figure 3)	t_o	500	—	—	ns
Pulse Width (Figure 3) ($f_o = 1.0\text{ MHz}$) ($f_o = 1.5\text{ MHz}$) ($f_o = 2.0\text{ MHz}$)	t_{PWM}	400 230 180	— — —	— — —	ns
Total Up Time (Figure 3) ($f_o = 1.0\text{ MHz}$) ($f_o = 1.5\text{ MHz}$) ($f_o = 2.0\text{ MHz}$)	t_{UPM}	900 600 440	— — —	— — —	ns
Delay Time Referenced to Output Complement (Figure 3) Output High to Low State (Clock Overlap at 1.0 V)	t_{PLHM}	0	—	—	ns
Delay Times Referenced to $2 \times f_o$ (Figure 4 MPU $\phi 2$ only) Output Low to High Logic State Output High to Low Logic State	t_{PLHM2X} t_{PHLM2X}	— —	— —	85 70	ns ns
Transition Times (Figure 3) Output Low to High Logic State Output High to Low Logic State	t_{TLHM} t_{THLM}	— —	— —	25 25	ns ns
BUS $\phi 2$ CHARACTERISTICS					
Pulse Width — Low Logic State (Figure 4) ($f_o = 1.0\text{ MHz}$) ($f_o = 1.5\text{ MHz}$) ($f_o = 2.0\text{ MHz}$)	t_{PWLb}	430 280 210	— — —	— — —	ns
Pulse Width — High Logic State ($f_o = 1.0\text{ MHz}$) ($f_o = 1.5\text{ MHz}$) ($f_o = 2.0\text{ MHz}$)	t_{PWHb}	450 295 235	— — —	— — —	ns
Delay Times — (Referenced to MPU $\phi 1$) (Figure 4) Output Low to High Logic State ($f_o = 1.0\text{ MHz}$) ($f_o = 1.5\text{ MHz}$) ($f_o = 2.0\text{ MHz}$) Output High to Low Logic State ($C_L = 300\text{ pF}$) ($C_L = 100\text{ pF}$)	t_{PLHbM1} t_{PHLbM1}	480 320 240 — —	— — — — —	— — — 25 20	ns
Delay Times (Referenced to MPU $\phi 2$) (Figure 4) Output Low to High Logic State Output High to Low Logic State	t_{PLHbM2} t_{PHLbM2}	-30 0	— —	+25 +40	ns ns
Transition Times (Figure 4) Output Low to High Logic State Output High to Low Logic State	t_{TLHb} t_{THLb}	— —	— —	20 20	ns ns

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SWITCHING CHARACTERISTICS (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
MEMORY CLOCK CHARACTERISTICS					
Delay Times (Referenced to MPU $\phi 2$) (Figure 4)					
Output Low to High Logic State	t_{PLHCM}	-50	—	+25	ns
Output High to Low Logic State	t_{PHLCM}	0	—	+40	ns
Delay Times (Referenced to $2 \times f_0$) (Figure 4)					
Output Low to High Logic State	t_{PLHC2X}	—	—	65	ns
Output High to Low Logic State	t_{PHLC2X}	—	—	85	ns
Transition Times (Figure 4)					
Output Low to High State	t_{TLHC}	—	—	25	ns
Output High to Low State	t_{THLC}	—	—	25	ns
$2 \times f_0$ CHARACTERISTICS					
Delay Times (Referenced to $4 \times f_0$) (Figure 4)					
Output Low to High Logic State	t_{PLH2X}	—	—	50	ns
Output High to Low Logic State	t_{PHL2X}	—	—	65	ns
Delay Time (Referenced to MPU $\phi 1$) (Figure 4)					
Output High to Low Logic State	$t_{PHL2XM1}$	365	—	—	ns
($f_0 = 1.0$ MHz)		220	—	—	
($f_0 = 1.5$ MHz)					
Transition Times (Figure 4)					
Output Low to High Logic State	t_{TLH2X}	—	—	25	ns
Output High to Low Logic State	t_{THL2X}	—	—	25	ns
$4 \times f_0$ CHARACTERISTICS					
Delay Times (Referenced to Ext. In) (Figure 4)					
Output Low to High Logic State	t_{PLH4X}	—	—	50	ns
Output High to Low Logic State	t_{PHL4X}	—	—	30	ns
Transition Time (Figure 4)					
Output Low to High Logic State	t_{TLH4X}	—	—	25	ns
Output High to Low Logic State	t_{THL4X}	—	—	25	ns
MEMORY READY CHARACTERISTICS					
Set-Up Times (Figure 5)					
Low Input Logic State	t_{SMRL}	55	—	—	ns
High Input Logic State	t_{SMRH}	75	—	—	ns
Hold Time (Figure 5)					
Low Input Logic State	t_{HMRL}	10	—	—	ns
DMA/REFRESH REQUEST CHARACTERISTICS					
Set-Up Times (Figure 6)					
Low Input Logic State	t_{SDRL}	65	—	—	ns
High Input Logic State	t_{SDRH}	75	—	—	ns
Hold Time (Figure 6)					
Low Input Logic State	t_{HDRL}	10	—	—	ns
DMA/REFRESH GRANT CHARACTERISTICS					
Delay Time Referenced to Memory Clock (Figure 6)					
Output Low to High Logic State	t_{PLHG}	-15	—	+25	ns
Output High to Low Logic State	t_{PHLG}	-25	—	+15	ns
Transition Times (Figure 6)					
Output Low to High Logic State	t_{TLHG}	—	—	25	ns
Output High to Low Logic State	t_{THLG}	—	—	25	ns
RESET CHARACTERISTICS					
Delay Time Referenced to Power-On Reset (Figure 7)					
Output Low to High Logic State	t_{PLHR}	—	—	1000	ns
Output High to Low Logic State	t_{PHLR}	—	—	250	ns
Transition Times (Figure 7)					
Output Low to High Logic State	t_{TLHR}	—	—	100	ns
Output High to Low Logic State	t_{THLR}	—	—	50	ns

DESCRIPTION OF PIN FUNCTIONS

- $4 \times f_0$ — A free running oscillator at four times the MPU clock rate useful for a system sync signal.
- $2 \times f_0$ — A free running oscillator at two times the MPU clock rate.
- DMA/REF REQ — An asynchronous input used to freeze the MPU clocks in the $\phi 1$ high, $\phi 2$ low state for dynamic memory refresh or cycle steal DMA (Direct Memory Access).
- REF GRANT — A synchronous output used to synchronize the refresh or DMA operation to the MPU.
- MEMORY READY — An asynchronous input used to freeze the MPU clocks in the $\phi 1$ low, $\phi 2$ high state for slow memory interface.
- MPU $\phi 1$ — Capable of driving the $\phi 1$ and $\phi 2$ inputs on two MC6800s.
- MPU $\phi 2$
- BUS $\phi 2$ — An output nominally in phase with MPU $\phi 2$ having MC8T26A type drive capability.
- MEMORY CLOCK — An output nominally in phase with MPU $\phi 2$ which free runs during a refresh request cycle.
- POWER-ON RESET — A Schmitt trigger input which controls Reset. A capacitor to ground is required to set the desired time constant. Internal 50 k resistor to V_{CC} . See General Design Suggestions for Manual Reset Operation.
- RESET — An output to the MPU and I/O devices.
- X1, X2 — Provision to attach a series resonant crystal or RC network.
- EXT IN — Allows driving by an external TTL signal to synchronous the MPU to an external system.

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FIGURE 1 — BLOCK DIAGRAM

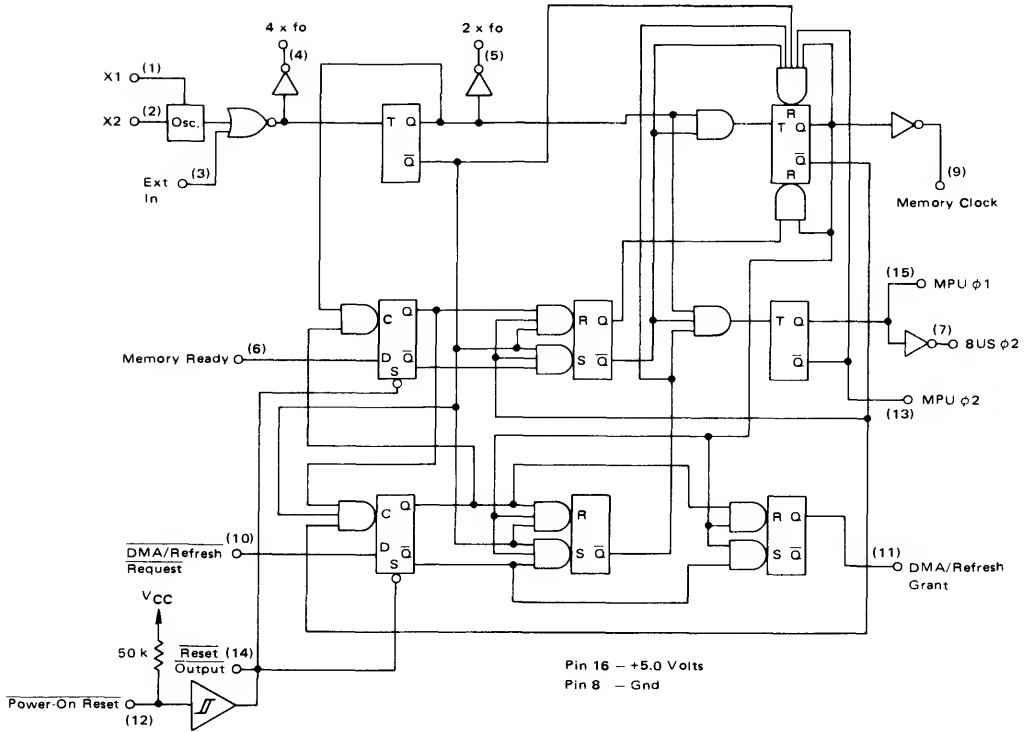


FIGURE 2 — TYPICAL HYSTERESIS CHARACTERISTIC OF RESET FUNCTION

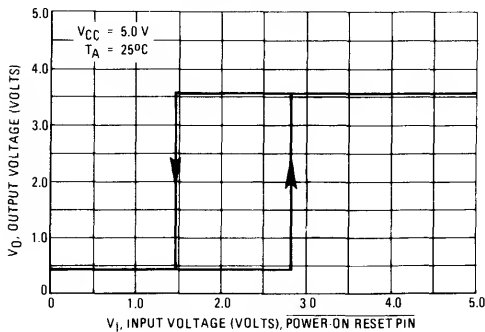
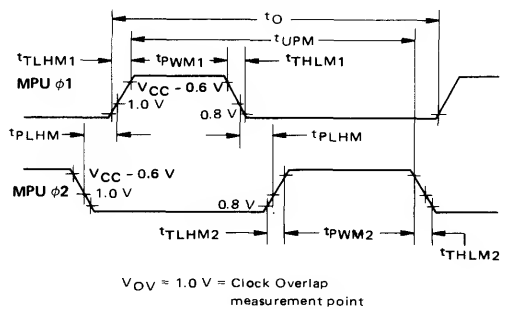


FIGURE 3 — TIMING DIAGRAM FOR MPU φ1 AND φ2

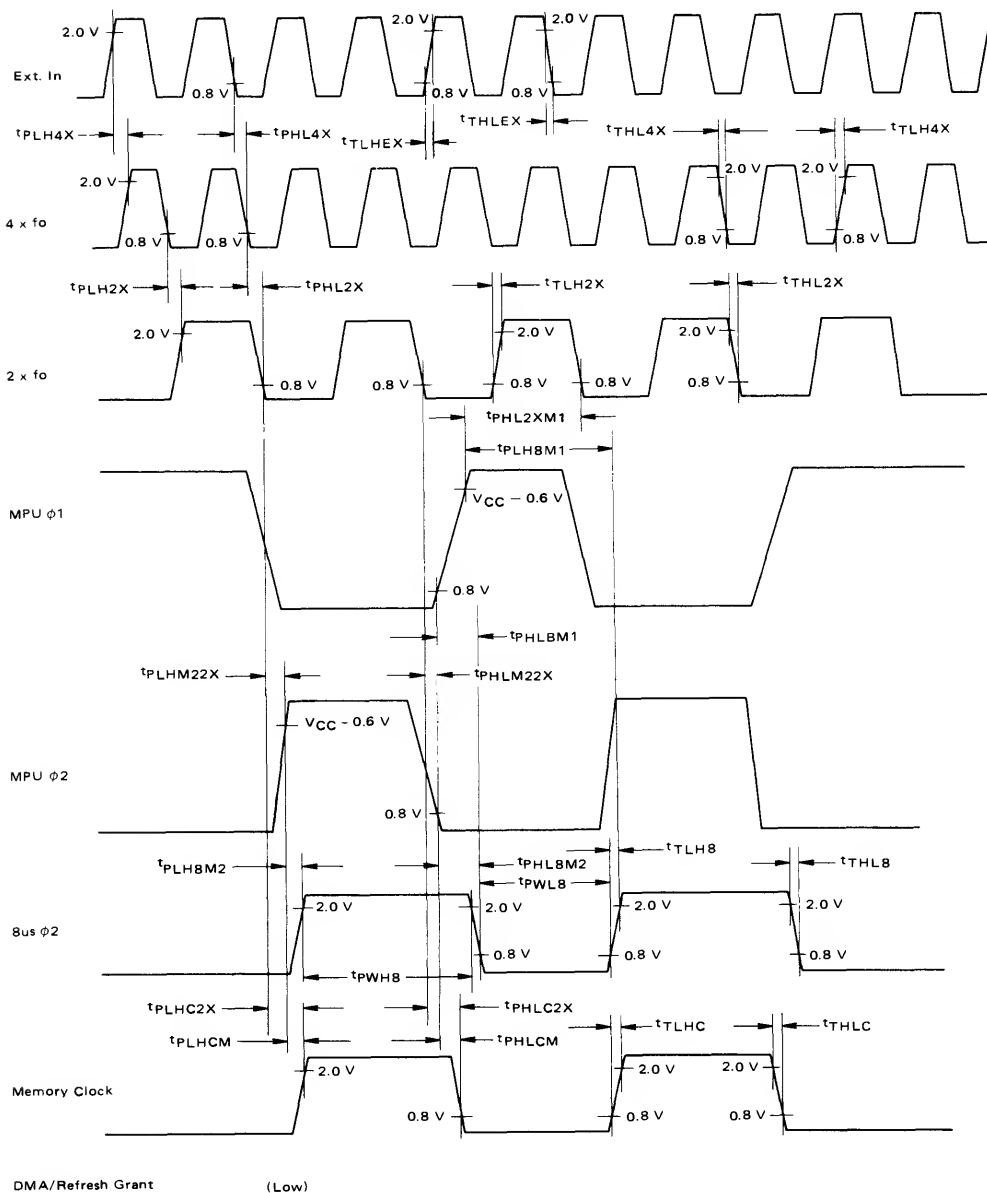


MC6875, MC6875A

FIGURE 4 – TIMING DIAGRAM FOR NON-STRETCHED OPERATION

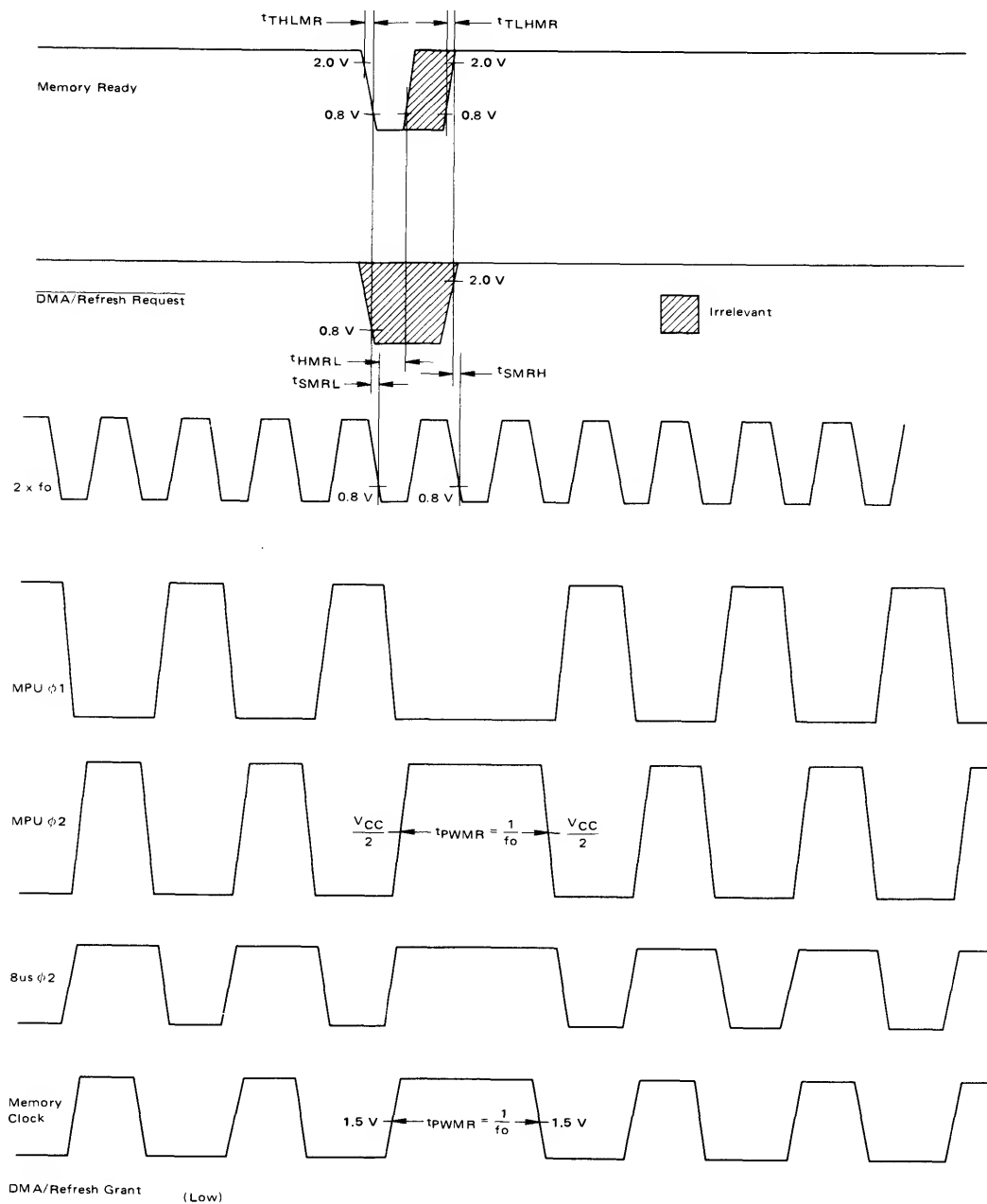
(Memory Ready and DMA/Refresh Request held high continuously)

Ext. In Input Voltage: 0 V to 3.0 V, $f = 8.0$ MHz, Duty Cycle = 50%, $t_{TLHEX} = t_{THLEX} = 5.0$ ns



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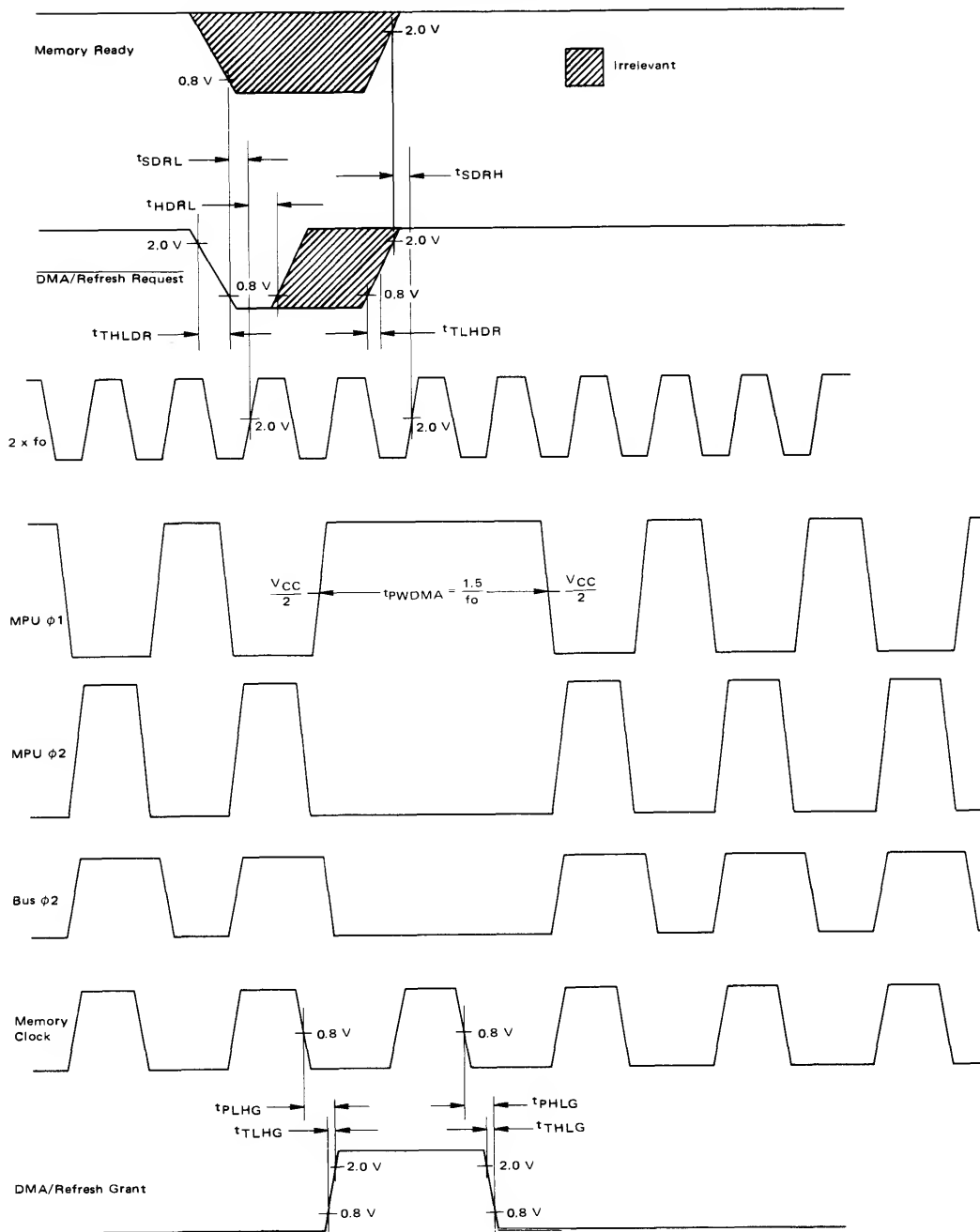
Input Voltage: 3.0 to 0 V, $t_{THLMB} \approx t_{TLHMB} = 5.0$ ns



MC6875, MC6875A

FIGURE 6 — TIMING DIAGRAM FOR DMA/REFRESH REQUEST STRETCH OPERATION
(Minimum Stretch Shown)

Input Voltage: 3.0 to 0 V, $t_{THLDR} = t_{TLHDR} = 5.0 \text{ ns}$



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FIGURE 7 — POWER ON RESET

Input Voltage: 0 to 5.0 V, $f = 100 \text{ kHz}$ — Pulse Width $\approx 1.0 \mu\text{s}$, $t_{\text{TLH}} = t_{\text{THL}} \approx 25 \text{ ns}$

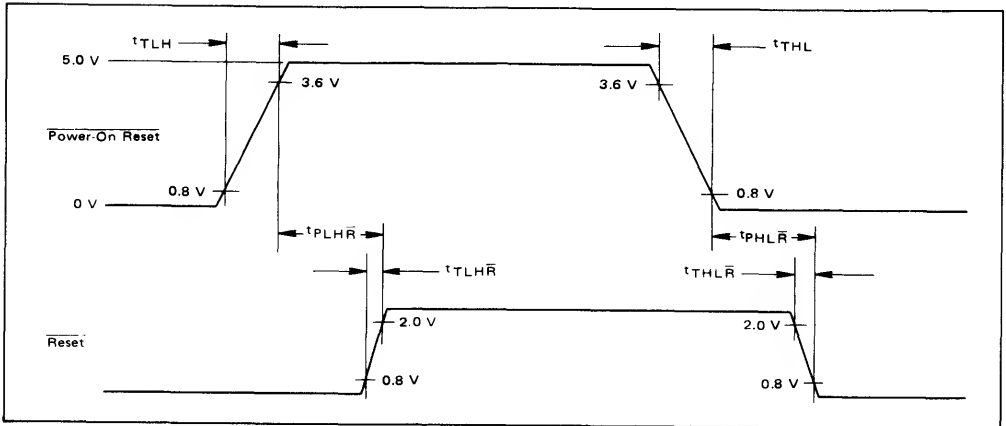
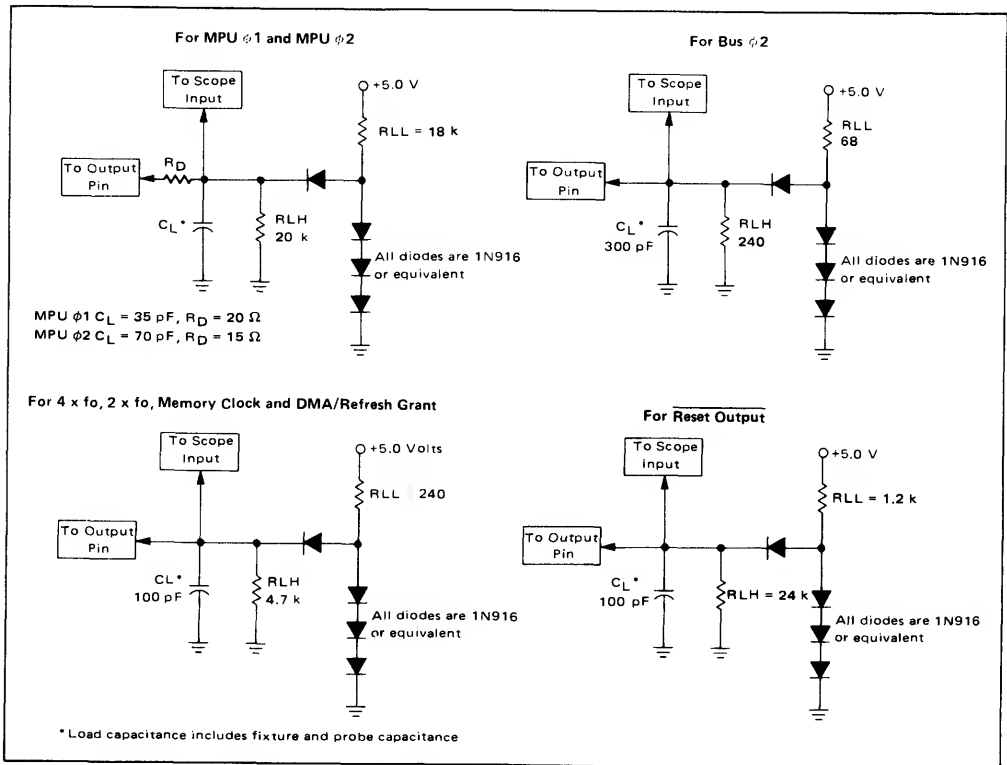


FIGURE 8 — LOAD CIRCUITS



MC6875, MC6875A

APPLICATIONS INFORMATION

FIGURE 9 — TYPICAL RC FREQUENCY versus VOLTAGE

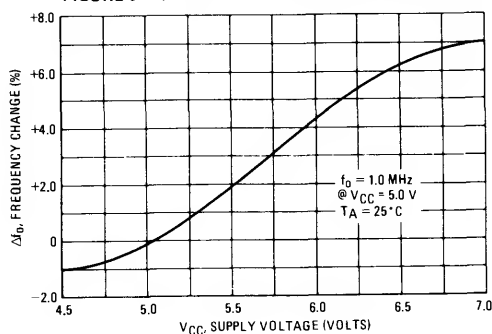


FIGURE 10 — TYPICAL RC FREQUENCY versus TEMPERATURE

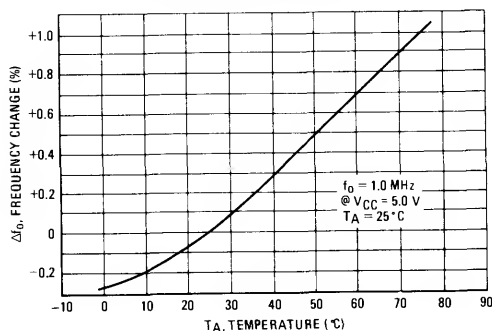
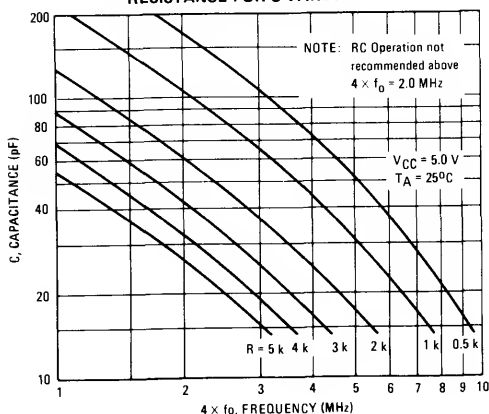


FIGURE 11 — TYPICAL FREQUENCY versus RESISTANCE FOR C VARIABLE



GENERAL

The MC6875 Clock Generator/Driver should be located on the same board and within two inches of the MC6800 MPU. Series damping resistors of 10-30 ohms may be utilized between the MC6875 and the MC6800 on the $\phi 1$ and $\phi 2$ clocks to suppress overshoot and reflections.

The V_{CC} pin (pin 16) of the MC6875 should be bypassed to the ground pin (pin 8) at the package with a $0.1 \mu F$ capacitor. Because of the high peak currents associated with driving highly capacitive loads, an adequately large ground strip to pin 8 should be used on the MC6875. Grounds should be carefully routed to minimize coupling of noise to the sensitive oscillator inputs. Unnecessary grounds or ground planes should be avoided near pin 2 or the frequency determining components. These components should be located as near as possible to the respective pins of the MC6875. Stray capacitance near pin 2 or the crystal, can affect the frequency. The can of the crystal should not be grounded. The ground side of the crystal or the C of the R-C oscillator should be connected as directly as possible to pin 8.

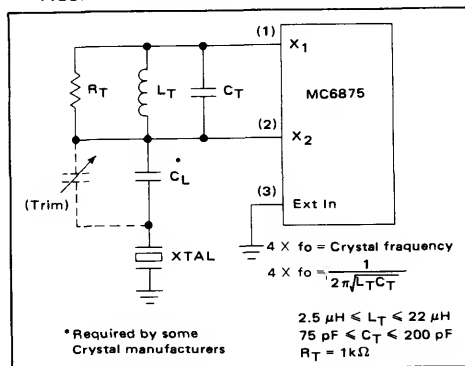
Unused inputs should be connected to V_{CC} or ground. Memory Ready, DMA/Refresh Request and Power-On Reset should be connected to V_{CC} when not used. The External Input should be connected to ground when not used.

OSCILLATOR

A tank circuit tuned to the desired crystal frequency connected between terminals X_1 and X_2 as shown in Figure 12, is recommended to prevent the oscillator from starting at other than the desired frequency. The $1k\Omega$ resistor reduces the Q sufficiently to maintain stable crystal control. Crystal manufacturers may recommend a capacitance (C_L) to be used in series with the crystal for optimum performance at series resonance.

See Figures 9 and 10 for typical oscillator temperature and V_{CC} supply dependence for R-C operation.

FIGURE 12 — OSCILLATOR-CRYSTAL OPERATION



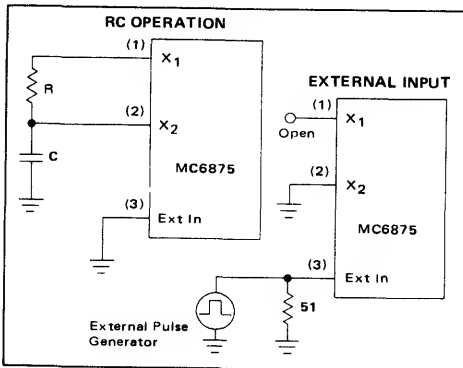
MC6875, MC6875A

TABLE 1 — OSCILLATOR COMPONENTS

TANK CIRCUIT PARAMETERS		APPROXIMATE CRYSTAL PARAMETERS				CTS KNIGHTS 400 REIMANN AVE. SANDWICH, IL 60548 (815) 786-8411	McCOY ELECT. CO. WATTS & CHESTNUTS STS. MT. HOLLY SPRING, PA 17065 (717) 486-3411	TYCO CRYSTAL PRODUCTS 3940 W. MONTECITO PHOENIX, AZ 85019 (602) 272-7945
L _T μH	C _T pF	R _S Ohms	C ₀ pF	C ₁ mpF	f ₀ MHz			
10	150	15-75	3-6	12	4.0	MP-04A * 390 pF	113-31	150-3260
4.7	82	8-45	4-7	23	8.0	MP-080 * 47 pF	113-32	150-3270

Inductors may be obtained from: Coilcraft, Cary, IL 60013 (312) 639-2361

FIGURE 13



To precisely time a crystal to desired frequency, a variable trimmer capacitor in the range of 7 to 40 pF would typically be used. Note it is not a recommended practice to tune the crystal with a parallel load capacitance.

The table above shows typical values for C_T and L_T, typical crystal characteristics, and manufacturers' part numbers for 4.0 and 8.0 megahertz operation.

The MC6875 will function as an R-C oscillator when connected as shown in Figure 13. The desired output frequency (Mφ1) is approximately:

$$\text{Formula} \quad 4 \times f_0 \approx \frac{320}{C(R + .27) + 23}$$

C in picofarads
R in K ohms

(See Figure 11) $4 \times f_0$ in Megahertz

It would be desirable to select a capacitor greater than 15 pF to minimize the effects of stray capacitance. It is also desirable to keep the resistor in the 1 to 5 k Ω range. There is a nominal 270 Ω resistor internally at X₁ which is in series with the external R. By keeping the external R as large as possible, the effects due to process variations of the internal resistor on the frequency will be reduced. There will, however, still be some variation in frequency in a production lot both from the resistance variations, external and internal, and process variations of the input switching thresholds. Therefore, in a production system, it is recommended a potentiometer be placed in series with a fixed R between X₁ and X₂.

POWER-ON RESET

As the power to the MC6875 comes up, the Reset Output will be in a high impedance state and will not give

a solid V_{OL} output level until V_{CC} has reached 3.5 to 4.0 V. During this time transients may appear on the clock outputs as the oscillator begins to start. This happens at approximately V_{CC} = 3 V. At some V_{CC} level above that, where Reset Output goes low, all the clock outputs will begin functioning normally. This phenomenon of the start-up sequence should not cause any problems except possibly in systems with battery back-up memory. The transients on the clock lines during the time the Reset Output is high impedance could initiate the system in some unknown mode and possibly write into the backup memory system. Therefore in battery backup systems, more elaborate reset circuitry will be required.

Please note that the Power-On Reset input pin of the MC6875 is not suitable for use with a manual MPU reset switch if the DMA/Ref Req or Memory Ready inputs are going to be used. The power on reset circuitry is used to initialize the internal control logic and whenever the input is switched low, the MC6875 is irresponsive to the DMA/Ref Req or Memory Ready inputs. This may result in the loss of dynamic memory and/or possibly a byte of slow static memory. The circuit of Figure 14 is recommended for applications which do not utilize the DMA/Ref Req or Memory Ready inputs. The circuit of Figure 15 is recommended for those applications that do.

FIGURE 14 — MANUAL RESET FOR APPLICATIONS NOT USING DMA/REFRESH REQUEST OR MEMORY READY INPUTS

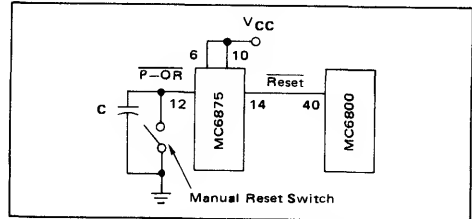
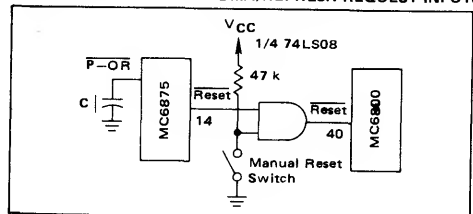


FIGURE 15 — MANUAL RESET FOR SYSTEMS USING DYNAMIC RAM OR SLOW STATIC RAM IN CONJUNCTION WITH MEMORY READY OR DMA/REFRESH REQUEST INPUTS



MC34050 MC34051

DUAL EIA-422/423 TRANSCEIVER

The MC34050/51 are dual transceivers which comply with EIA Standards EIA-422 (Balanced line) and EIA-423 (Unbalanced line). Each device contains two drivers and two receivers.

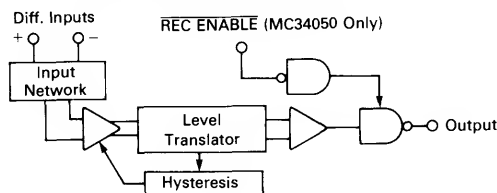
The MC34050 has a DRIVER ENABLE (for both drivers) and a RECEIVER ENABLE (for both receivers). Connecting the two ENABLES together provides Driver-to-Receiver switching from a single line.

The MC34051 has a DRIVER ENABLE for each driver. The two receivers are permanently enabled.

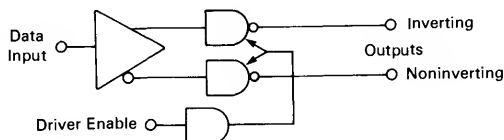
The Driver inputs, Receiver outputs, and Enable inputs are 74LS TTL compatible.

- Two Independent Drivers and Receivers Per Package
- 3-State Outputs
- Single 5 Volt Supply
- Internal Hysteresis (50 mV Typical) on Receivers
- Receivers Provide Fail-Safe Function. Output Stays High if Inputs are Open, Shorted (floating), or Terminated (floating)
- Receivers May Be Used in EIA-422 or 423 Systems
- Drivers Meet Full EIA-422 Standards
- Drivers' Outputs are Short Circuit Current Limited

RECEIVER BLOCK DIAGRAM



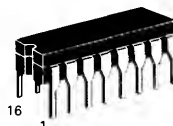
DRIVER BLOCK DIAGRAM



Driver				Receiver		
Data	EN	Inv. Out	Noninv. Out	Input	EN	Output
L	H	H	L	$> +0.2$ V Diff.	L	H
H	H	L	H	< -0.2 V Diff.	L	L
X	L	Z	Z	X	H	Z

DUAL EIA-422/423 TRANSCEIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT

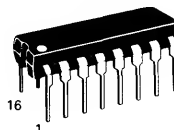


L SUFFIX
CERAMIC PACKAGE
CASE 620

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO-16)

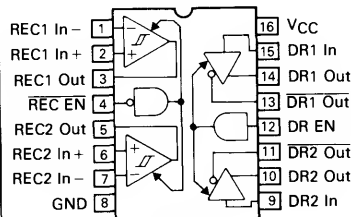


(MC34050 Only)

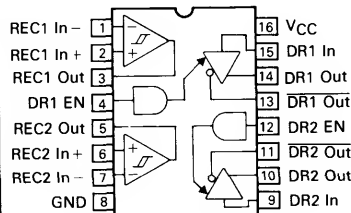


P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS



MC34050



MC34051

MC34050, MC34051

MAXIMUM RATINGS

Parameter	Value	Units
Power Supply Voltage (V_{CC})	7.0	Vdc
Input Common Mode Voltage (Receivers)	± 25	Vdc
Input Differential Voltage (Receivers)	± 25	Vdc
Output Sink Current (Receivers)	50	mA
Enable Input Voltage (Drivers and Receivers)	5.5	Vdc
Input Voltage (Drivers)	5.5	Vdc
Applied Output Voltage (3-State mode) — Receivers	-1.0 to +7.0	Vdc
Applied Output Voltage (3-State mode) — Drivers	-1.0 to +7.0	Vdc
Junction Temperature	-65 to +150	°C
Storage Temperature	-65 to +150	°C

Devices should not be operated at these values.

The "Recommended Operating Limits" provide for actual device operation.

RECOMMENDED OPERATING LIMITS

Parameter	Min	Typ	Max	Units
Power Supply Voltage	+4.75	+5.0	+5.25	Vdc
Input Common Mode Voltage (Receivers)	-7.0	—	+7.0	Vdc
Input Differential Voltage (Receivers)	-6.0	—	+6.0	Vdc
Enable Input Voltage (Drivers and Receivers)	0	—	+5.25	Vdc
Input Voltage (Drivers)	0	—	+5.25	Vdc
Ambient Temperature Range	0	—	+70	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted specifications apply for $4.75 < V_{CC} < 5.25$ volts, and $0^\circ < T_A < 70^\circ\text{C}$).

Parameter	Symbol	Min	Typ	Max	Units
DRIVERS					
Input Voltage — Low	V_{ILD}	—	—	0.8	Vdc
Input Voltage — High	V_{IHD}	2.0	—	—	Vdc
Input Current ($\alpha V_{IL} = 0.4$ V)	I_{ILD}	-360	—	—	μA
Input Current ($\alpha V_{IH} = 2.7$ V $V_{IH} = 5.25$ V)	I_{IHD}	—	—	+20 +100	μA
Input Clamp Voltage ($I_{IK} = -18$ mA)	V_{IKD}	-1.5	—	—	Vdc
Output Voltage — Low ($I_{OL} = 20$ mA)	V_{OLD}	—	—	0.5	Vdc
Output Voltage — High ($I_{OH} = -20$ mA)	V_{OHD}	2.5	—	—	Vdc
Output Offset Voltage Difference (Note 1)	V_{OSD}	-0.4	—	+0.4	Vdc
Output Differential Voltage (Note 1)	V_T	2.0	—	—	Vdc
Output Differential Voltage Difference (Note 1)	V_{TD}	-0.4	—	+0.4	Vdc
Short Circuit Current ($V_{CC} = 5.25$ V) (From High Output, Note 2)	I_{OSD}	-150	—	-30	mA
Output Leakage Current — Hi-Z State ($V_{out} = 0.5$ V, DR EN = 0.8 V) ($V_{out} = 2.7$ V, DR EN = 0.8 V)	I_{OZD}	-100 -100	— —	+100 +100	μA
Output Leakage — Power Off ($V_{out} = -0.25$ V, $V_{CC} = 0$ V) ($V_{out} = 6.0$ V, $V_{CC} = 0$ V)	$I_{O(off)}$	-100 —	— —	— +100	μA

Notes: 1) See EIA Standard EIA-422 and Figure 1 for exact test conditions.

2) Only one output in a package should be shorted at a time, for no longer than 1 second.

MC34050, MC34051

ELECTRICAL CHARACTERISTICS (Unless otherwise noted specifications apply for $4.75 < V_{CC} < 5.25$ volts, and $0^\circ < T_A < 70^\circ\text{C}$).

Parameter	Symbol	Min	Typ	Max	Units
RECEIVERS					
Differential Input Threshold Voltage (Note 3) ($-7.0 \text{ V} < V_{ICM} < +7.0 \text{ V}$, $V_{out} \geq 2.7 \text{ V}$) ($-7.0 \text{ V} < V_{ICM} < +7.0 \text{ V}$, $V_{out} \leq 0.45 \text{ V}$)	V_{THR}	— -0.2	—	+0.2 —	Vdc
Input Bias Current ($0 \leq V_{CC} \leq 5.25 \text{ V}$, $V_{in} = +15 \text{ V}$) ($0 \leq V_{CC} \leq 5.25 \text{ V}$, $V_{in} = -15 \text{ V}$)	I_{IBR}	— -2.8	—	+2.3 —	mA
Input Balance and Output Level ($-7.0 \leq V_{ICM} \leq +7.0 \text{ V}$) ($V_{ID} = +0.4 \text{ V}$, $I_O = -400 \mu\text{A}$) ($V_{ID} = -0.4 \text{ V}$, $I_O = 8.0 \text{ mA}$)	V_{OHR} V_{OLR}	2.7 —	— —	— 0.45	Vdc
Output Leakage Current — 3-State (Pin 4 = 2.0 V, MC34050 only) ($V_{ID} = +3.0 \text{ V}$, $V_O = 0.4 \text{ V}$) ($V_{ID} = -3.0 \text{ V}$, $V_O = 2.4 \text{ V}$)	I_{OZR}	-100 -100	— —	+100 +100	μA
Output Short Circuit Current (Note 2, $V_{CC} = 5.25 \text{ V}$) ($V_{ID} = +3.0 \text{ V}$, MC34050 Pin 4 = 0.4 V, $V_O = 0 \text{ V}$)	I_{OSR}	-85	—	-15	mA

ENABLES

Input Voltage — Low	V_{ILE}	—	—	0.8	Vdc
Input Voltage — High	V_{IHE}	2.0	—	—	Vdc
Input Current ($\alpha V_{IL} = 0.4 \text{ V}$ (Receiver EN) (Driver EN)	I_{ILER} I_{ILED}	-100 -360	— —	— —	μA
Input Current ($\alpha V_{IH} = 2.7 \text{ V}$ $V_{IH} = 5.25 \text{ V}$)	I_{IHE}	— —	— —	+20 +100	μA
Input Clamp Voltage ($I_{IK} = -18 \text{ mA}$)	V_{IKE}	-1.5	—	—	Vdc

POWER SUPPLY

Power Supply Current ($\alpha V_{CC} = 5.25 \text{ V}$)	I_{CC}	—	55	80	mA
---	----------	---	----	----	----

Notes: 1) See EIA Standard EIA-422 and Figure 1 for exact test conditions.

2) Only one output in a package should be shorted at a time, for no longer than 1 second.

3) Differential input threshold voltage and guaranteed output levels are done simultaneously for worst case.

4) All currents into a device pin are positive, those out of a pin are negative. Voltages are referenced to ground. Algebraic convention rather than magnitude is used to define limits.

DRIVER SWITCHING CHARACTERISTICS ($V_{CC} = 5.0 \text{ V}$, $T_A = 25^\circ\text{C}$, See Figure 2)

Parameter	Symbol	Min	Typ	Max	Units
Propagation Delay					ns
Data Input to Output High-to-Low	t_{PHLD}	—	—	20	
Data Input to Output Low-to-High	t_{PLHD}	—	—	20	
Output Skew ($ t_{pHL} - t_{pLH} $ each driver)	t_{SKD}	—	—	8	
Enable Input to Output					
$C_L = 10 \text{ pF}$, $R_L = 75 \Omega$ to Gnd	t_{PHZD}	—	—	30	
$C_L = 10 \text{ pF}$, $R_L = 180 \Omega$ to V_{CC}	t_{PLZD}	—	—	35	
$C_L = 30 \text{ pF}$, $R_L = 75 \Omega$ to Gnd	t_{PZHD}	—	—	40	
$C_L = 30 \text{ pF}$, $R_L = 180 \Omega$ to V_{CC}	t_{PZLD}	—	—	45	
Maximum Data Input Transition Time (10–90%)	t_{TRD}	—	50	—	ns

RECEIVER SWITCHING CHARACTERISTICS ($V_{CC} = 5.0 \text{ V}$, $T_A = 25^\circ\text{C}$, Figure 3)

Parameter	Symbol	Min	Typ	Max	Units
Propagation Delay					ns
Differential Input to Output — High-to-Low	t_{PHLR}	—	—	30	
Differential Input to Output — Low-to-High	t_{PLHR}	—	—	30	
Enable Input — Output Low to 3-State*	t_{PLZR}	—	—	35	
Enable Input — Output High to 3-State*	t_{PHZR}	—	—	35	
Enable Input — Output 3-State to High*	t_{PZHR}	—	—	30	
Enable Input — Output 3-State to Low*	t_{PZLR}	—	—	30	

*MC34050 Only.

MC34050, MC34051

FIGURE 1 — DRIVER OUTPUT TEST CIRCUIT

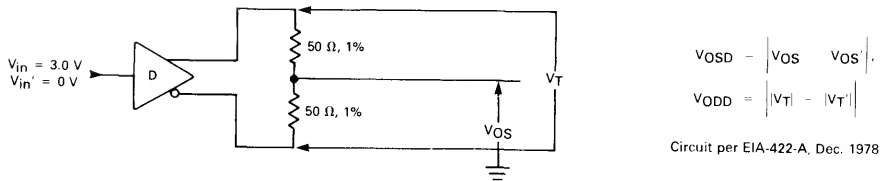
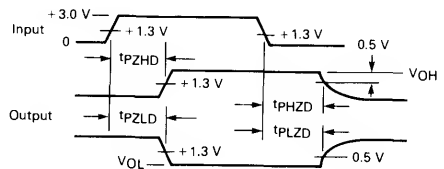
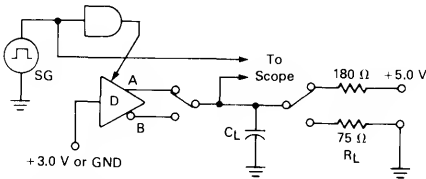
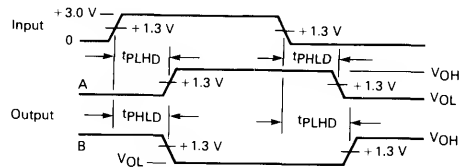
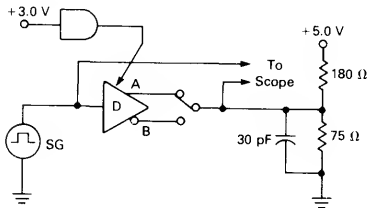
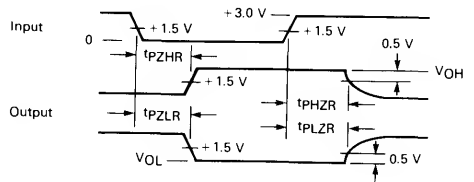
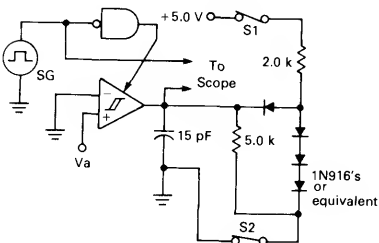
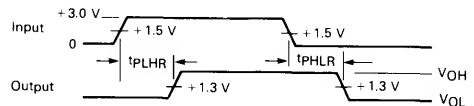
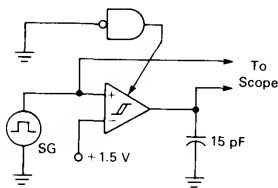


FIGURE 2 — DRIVER SWITCHING TEST CIRCUITS



SG: 1.0 MHz, 50% duty cycle, t_r , $t_f = 6.0 \text{ ns}$ (10–90%)
 $R_L = 75 \Omega$ to GND for t_{PZHD} and t_{PHZD} , 180Ω to V_{CC} for t_{PLZD} and t_{PHZD} .
 $C_L = 10 \text{ pF}$ for t_{PZHD} and t_{PLZD} , 30 pF for t_{PHZD} and t_{PHZD} .

FIGURE 3 — RECEIVER SWITCHING TEST CIRCUITS



MC34050 Only

SG: 1.0 MHz, 50% duty cycle, t_r , $t_f = 6.0 \text{ ns}$ (10–90%)
 $V_a = +1.5 \text{ V}$ for t_{PHZ} , t_{PZH} ; $V_a = -1.5 \text{ V}$ for t_{PLZ} , t_{PLH} .
 S1, S2 closed for t_{PHZ} , t_{PLZ} ; S1 open, S2 closed for t_{PZH} ; S1 closed, S2 open for t_{PLH} .

MC34050, MC34051

FIGURE 4 — DRIVER INPUT CHARACTERISTICS

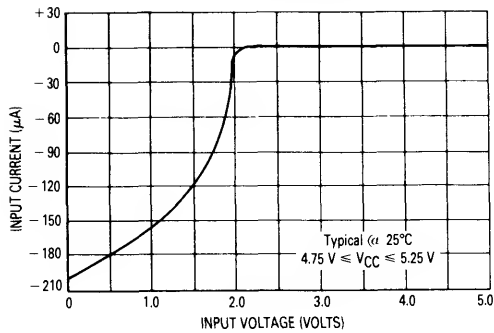


FIGURE 5 — DRIVER DIFFERENTIAL OUTPUT CHARACTERISTICS

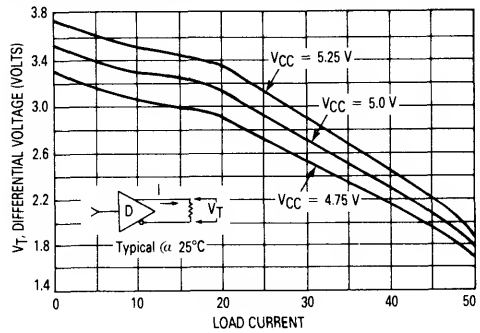


FIGURE 6 — DRIVER OUTPUT VOLTAGE

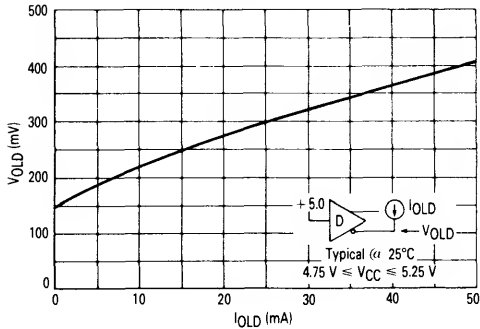


FIGURE 7 — DRIVER OUTPUT VOLTAGE

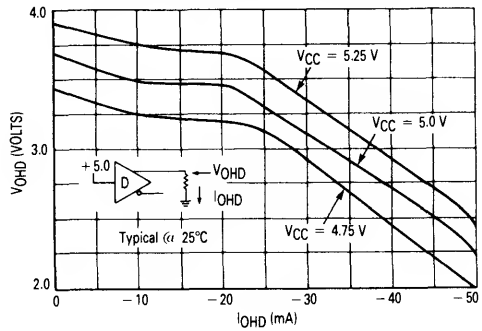


FIGURE 8 — RECEIVER OUTPUT VOLTAGE

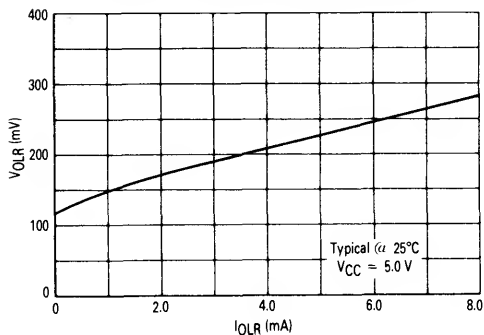
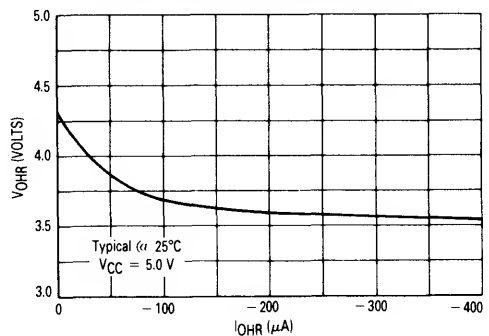


FIGURE 9 — RECEIVER OUTPUT VOLTAGE



MC34050, MC34051

FIGURE 10 — RECEIVER INPUT CHARACTERISTICS

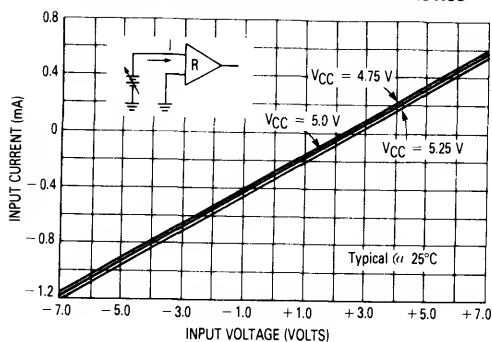


FIGURE 11 — ENABLE INPUT CHARACTERISTICS

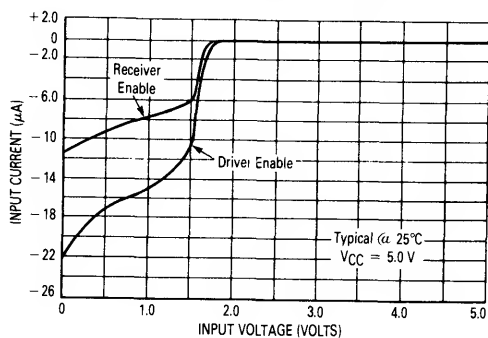


FIGURE 12 — RECEIVER INPUT CHARACTERISTICS

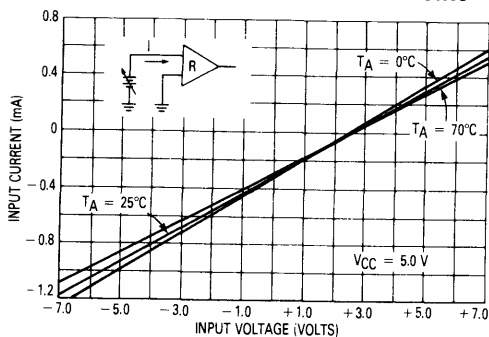


FIGURE 13 — RECEIVER OUTPUT LEAKAGE

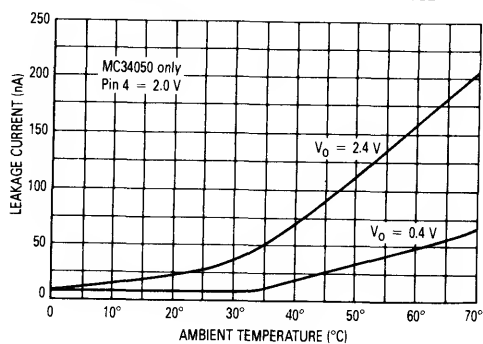


FIGURE 14 — DRIVER OUTPUT VOLTAGE

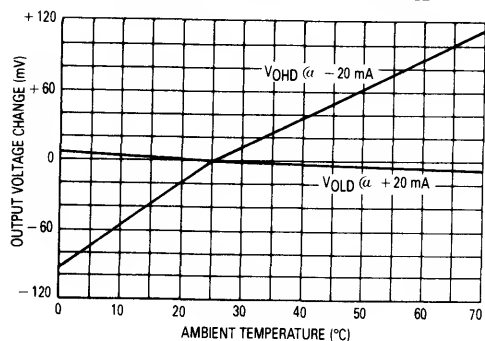
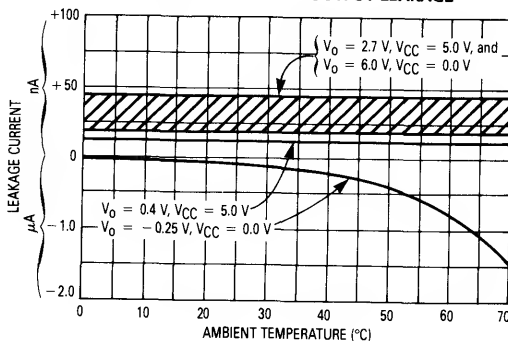


FIGURE 15 — DRIVER OUTPUT LEAKAGE



MC34050, MC34051

FIGURE 16 — EIA-422 APPLICATION

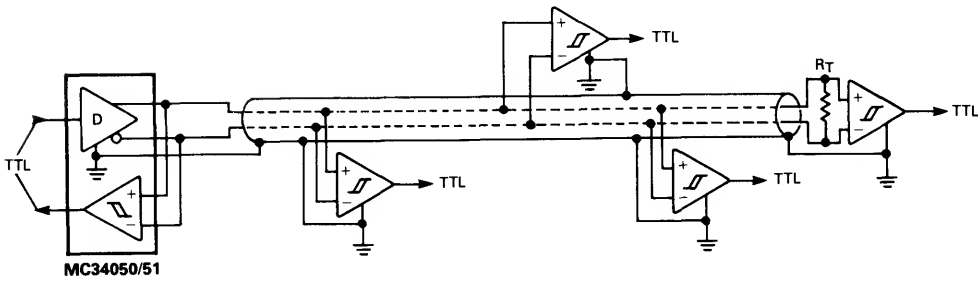
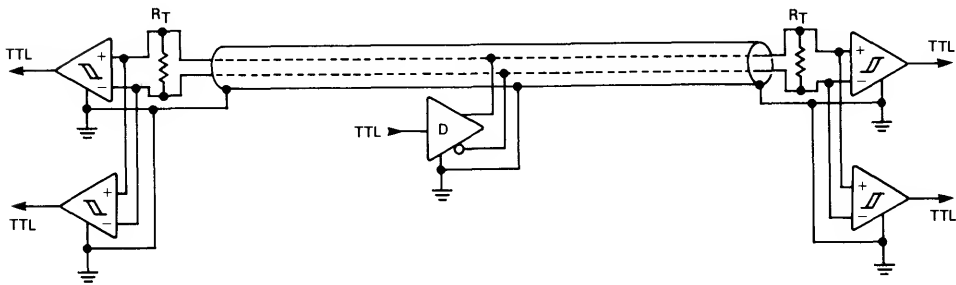


FIGURE 17 — EIA-422 APPLICATION



- Notes: 1) R_T must equal characteristic impedance of the cable.
 2) Individual receivers may be MC34050, MC34051, MC3486, or AM26LS32.
 3) System ground may be made through cable shield as shown, or through chassis ground. Common mode differences and signal quality must be considered when choosing a ground path.

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

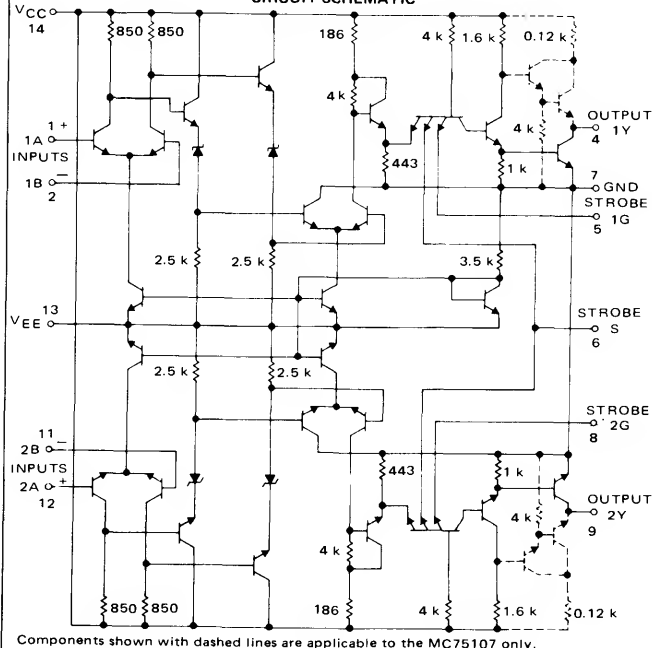
DUAL LINE RECEIVERS

The MC75107 and MC75108 are MTTL compatible dual line receivers featuring independent channels with common voltage supply and ground terminals. The MC75107 circuit features an active pull-up (totem-pole) output. The MC75108 circuit features an open-collector output configuration that permits the Wired-OR logic connection with similar outputs (such as the MC5401/MC7401 MTTL gate or additional MC75108 receivers). Thus a level of logic is implemented without extra delay.

The MC75107 and MC75108 circuits are designed to detect input signals of greater than 25 millivolts amplitude and convert the polarity of the signal into appropriate MTTL compatible output logic levels.

- High Common-Mode Rejection Ratio
- High Input Impedance
- High Input Sensitivity
- Differential Input Common-Mode Voltage Range of ± 3.0 V
- Differential Input Common-Mode Voltage of More Than ± 15 V Using External Attenuator
- Strobe Inputs for Receiver Selection
- Gate Inputs for Logic Versatility
- MTTL or MDTL Drive Capability
- High DC Noise Margins
- MC55107 Available as JM38510/10401

CIRCUIT SCHEMATIC



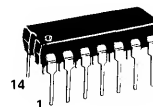
MC75107 MC75108

DUAL LINE RECEIVERS

SILICON MONOLITHIC INTEGRATED CIRCUITS

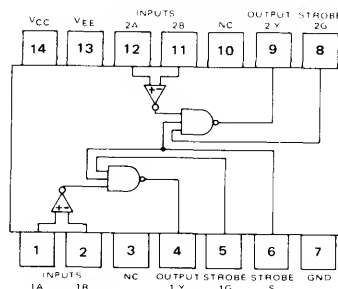


L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

PIN CONNECTIONS



TRUTH TABLE

Differential Inputs A-B	Strobes		Output Y
	G	S	
$V_{ID} \geq 25$ mV	L or H	L or H	H
-25 mV $< V_{ID} < 25$ mV	L or H	L	H
	L	L or H	H
$V_{ID} \leq -25$ mV	H	H	Indeterminate
	L or H	L	H
	L	L or H	H
	H	H	L

MC75107, MC75108

MAXIMUM RATINGS ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC} V_{EE}	+7.0 -7.0	Vdc
Differential-Mode Input Signal Voltage Range	V_{ID}	± 6.0	Vdc
Common-Mode Input Voltage Range	V_{ICR}	± 5.0	Vdc
Strobe Input Voltage	$V_{I(S)}$	5.5	Vdc
Power Dissipation (Package Limitation) Plastic and Ceramic Dual-In-Line Packages Derate above $T_A = +25^\circ\text{C}$	P_D	625 3.85	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to $+70$	°C
Storage Temperature Range	T_{stg}	-65 to $+150$	°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltages	V_{CC} V_{EE}	+4.75 -4.75	+5.0 -5.0	+5.25 -5.25	Vdc
Output Sink Current	I_{OS}	—	—	-16	mA
Differential-Mode Input Voltage Range	V_{IDR}	-5.0	—	+5.0	Vdc
Common-Mode Input Voltage Range	V_{ICR}	-3.0	—	+3.0	Vdc
Input Voltage Range, any differential input to ground	V_{IR}	-5.0	—	+3.0	Vdc
Operating Temperature Range	T_A	0	—	$+70$	°C

DEFINITIONS OF INPUT LOGIC LEVELS

Characteristic	Symbol	Test Fig.	Min	Max	Unit
High-Level Input Voltage (between differential inputs)	V_{IDH}	1	0.025	5.0	Vdc
Low-Level Input Voltage (between differential inputs)	V_{IDL}	1	-5.0†	-0.025	Vdc
High-Level Input Voltage (at strobe inputs)	$V_{IH(S)}$	3	2.0	5.5	Vdc
Low-Level Input Voltage (at strobe inputs)	$V_{IL(S)}$	3	0	0.8	Vdc

†The algebraic convention, where the most positive limit is designated maximum, is used with Low-Level Input Voltage Level (V_{IDL}).

ELECTRICAL CHARACTERISTICS ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Fig.	Min	Typ #	Max	Unit
High-Level Input Current to 1A or 2A Input ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$, $V_{ID} = 0.5\text{ V}$, $V_{IC} = -3.0\text{ V}$ to $+3.0\text{ V}$) (1)	I_{IH}	2	—	30	75	μA
Low-Level Input Current to 1A or 2A Input ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$, $V_{ID} = -2.0\text{ V}$, $V_{IC} = -3.0\text{ V}$ to $+3.0\text{ V}$) (1)	I_{IL}	2	—	—	-10	μA
High-Level Input Current to 1G or 2G Input ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$, $V_{IH(S)} = 2.4\text{ V}$) (1) ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$, $V_{IH(S)} = V_{CC} \text{ Max}$) (1)	I_{IH}	4	— —	— —	40 1.0	μA mA
Low-Level Input Current to 1G or 2G Input ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$, $V_{IL(S)} = 0.4\text{ V}$) (1)	I_{IL}	4	—	—	-1.6	mA
High-Level Input Current to S Input ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$, $V_{IH(S)} = 2.4\text{ V}$) (1) ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$, $V_{IH(S)} = V_{CC} \text{ Max}$) (1)	I_{IH}	4	— —	— —	80 2.0	μA mA
Low-Level Input Current to S Input ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$, $V_{IL(S)} = 0.4\text{ V}$) (1)	I_{IL}	4	—	—	-3.2	mA
High-Level Output Voltage ($V_{CC} = \text{Min}$, $V_{EE} = \text{Min}$, $I_{load} = -400\text{ }\mu\text{A}$, $V_{IC} = -3.0\text{ V}$ to $+3.0\text{ V}$) (1)	V_{OH}	3	—	—	—	V
Low-Level Output Voltage ($V_{CC} = \text{Min}$, $V_{EE} = \text{Min}$, $I_{sink} = 16\text{ mA}$, $V_{IC} = -3.0\text{ V}$ to $+3.0\text{ V}$) (1)	V_{OL}	3	—	—	0.4	V
High-Level Leakage Current ($V_{CC} = \text{Min}$, $V_{EE} = \text{Min}$, $V_{OH} = V_{CC} \text{ Max}$) (1)	I_{CEX}	3	—	—	250	μA
Short-Circuit Output Current (3) ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$) (1)	I_{OSC}	5	—	—	—	mA
High Logic Level Supply Current from V_{CC} ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$, $V_{ID} = 25\text{ mV}$, $T_A = +25^\circ\text{C}$) (1)	I_{CCH+}	6	—	18	30	mA
High Logic Level Supply Current from V_{EE} ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$, $V_{ID} = 25\text{ mV}$, $T_A = +25^\circ\text{C}$) (1)	I_{CCH-}	6	0	8.4	-15	mA

NOTES:

- For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable device type.
- All typical values are at $V_{CC} = +5.0\text{ V}$, $V_{EE} = -5.0\text{ V}$, $T_A = -25^\circ\text{C}$.
- Not more than one output should be shorted at a time.

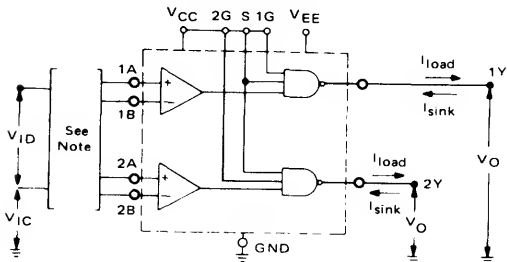
MC75107, MC75108

SWITCHING CHARACTERISTICS (V_{CC} = +5.0 V, V_{EE} = -5.0 V, T_A = +25°C)

Characteristic	Symbol	Test Fig.	Min	Typ	Max	Unit
Propagation Delay Time, low-to-high level from differential inputs A and B to output (R _L = 390 Ω, C _L = 50 pF) (R _L = 390 Ω, C _L = 15 pF)	t _{PLH} (D)	7	—	—	—	ns
Propagation Delay Time, high-to-low level from differential inputs A and B to output (R _L = 390 Ω, C _L = 50 pF) (R _L = 390 Ω, C _L = 15 pF)	t _{PHL} (D)	7	—	—	—	ns
Propagation Delay Time, low-to-high level, from strobe input G or S to output (R _L = 390 Ω, C _L = 50 pF) (R _L = 390 Ω, C _L = 15 pF)	t _{PLH} (S)	7	—	—	—	ns
Propagation Delay Time, high-to-low level, from strobe input G or S to output (R _L = 390 Ω, C _L = 50 pF) (R _L = 390 Ω, C _L = 15 pF)	t _{PHL} (S)	7	—	—	—	ns

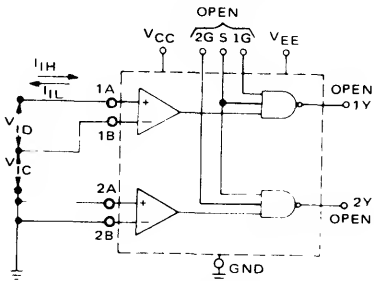
TEST CIRCUITS

FIGURE 1 – V_{IDH} and V_{IDL}



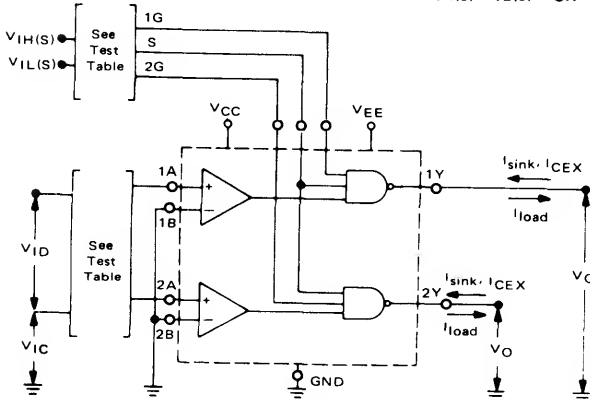
NOTE: When testing one channel, the inputs of the other channel are grounded.

FIGURE 2 – I_{IH} and I_{IL}



NOTE: Each pair of differential inputs is tested separately. The inputs of the other pair are grounded.

FIGURE 3 – V_{IH}(S), V_{IL}(S), V_{OH}, V_{OL}, and I_{QH}



TEST TABLE

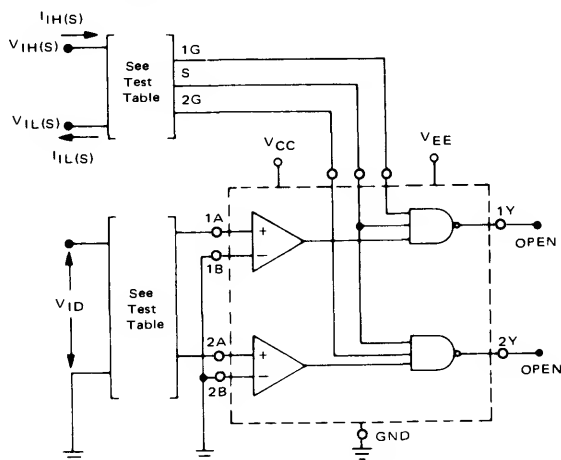
MC75107	MC75108	V _{ID}	STROBE 1G or 2G	STROBE S
TEST		APPLY		
V _{OH}	I _{CEX}	+25 mV	V _{IH} (S)	V _{IH} (S)
V _{OH}	I _{CEX}	-25 mV	V _{IL} (S)	V _{IL} (S)
V _{OH}	I _{CEX}	-25 mV	V _{IH} (S)	V _{IL} (S)
V _{OL}	V _{OL}	-25 mV	V _{IH} (S)	V _{IH} (S)

NOTES 1 V_{IC} = -3.0 V to +3.0 V
2 When testing one channel, the inputs of the other channel should be grounded

MC75107, MC75108

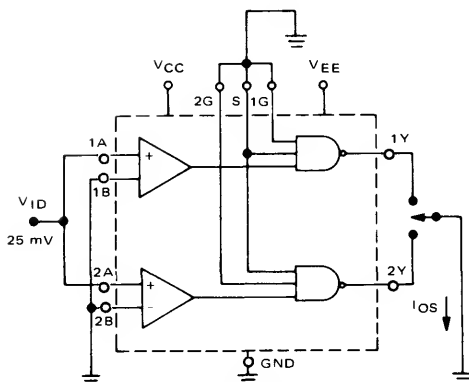
TEST CIRCUITS (continued)

FIGURE 4 – $I_{IH}(G)$, $I_{IL}(G)$, $I_{IH}(S)$, and $I_{IL}(S)$



TEST	INPUT 1A	INPUT 2A	STROBE 1G	STROBE S	STROBE 2G
I_{IH} at Strobe 1G	+25 mV	Gnd	$V_{IH}(S)$	Gnd	Gnd
I_{IH} at Strobe 2G	Gnd	+25 mV	Gnd	Gnd	$V_{IH}(S)$
I_{IH} at Strobe S	+25 mV	+25 mV	Gnd	$V_{IH}(S)$	Gnd
I_{IL} at Strobe 1G	-25 mV	Gnd	$V_{IL}(S)$	4.5 V	Gnd
I_{IL} at Strobe 2G	Gnd	-25 mV	Gnd	4.5 V	$V_{IL}(S)$
I_{IL} at Strobe S	-25 mV	-25 mV	4.5 V	$V_{IL}(S)$	4.5 V

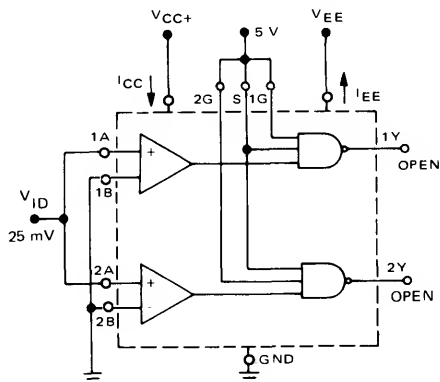
FIGURE 5 – I_{OS}



NOTES: 1. Each channel is tested separately.

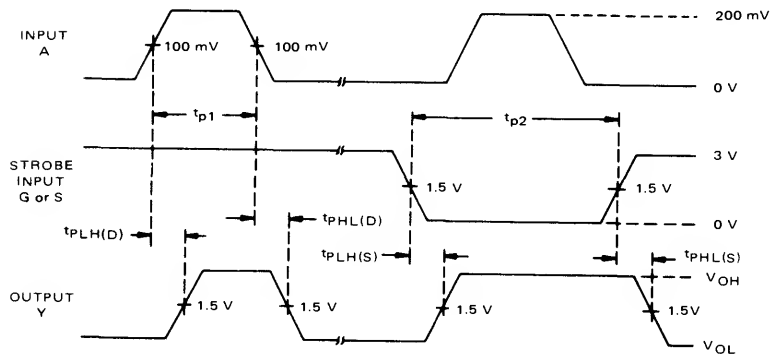
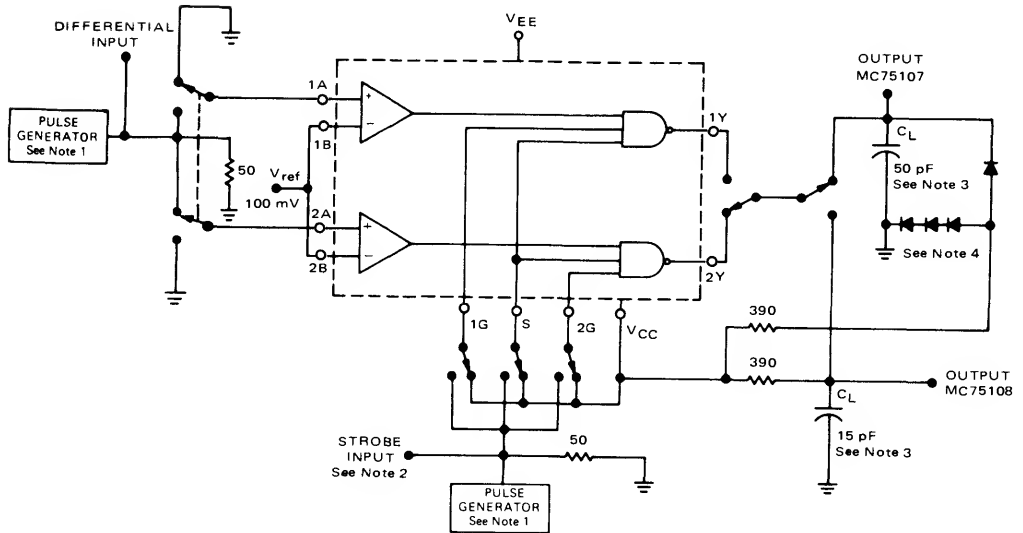
2. Not more than one output should be tested at one time.

FIGURE 6 – I_{CC} and I_{EE}



MC75107, MC75108

TEST CIRCUITS (continued)
FIGURE 7 — PROPAGATION DELAY TIME TEST CIRCUIT
AND WAVEFORMS



- NOTES: 1. The pulse generators have the following characteristics: $z_o = 50 \Omega$, $t_r = t_f = 10 \pm 5$ ns, $t_{p1} = 500$ ns, $PRR = 1$ MHz, $t_{p2} = 1 \mu s$, $PRR = 500$ kHz.
2. Strobe input pulse is applied to Strobe 1G when Inputs 1A-1B are being tested, to Strobe S when Inputs 1A-1B or 2A-2B are being tested, and to Strobe 2G when Inputs 2A-2B are being tested.
3. C_L includes probe and jig capacitance.
4. All diodes are 1N916 or equivalent.

MC75S110

MONOLITHIC DUAL LINE DRIVERS

The MC75S110 dual line driver features independent channels with common voltage supply and ground terminals. Each driver circuit provides a constant output current that switches to either of two output terminals subject to the appropriate logic levels at the input terminals. Output current can be switched "off" (inhibited) by appropriate logic levels at the inhibit inputs. Output current is nominally twelve milliamperes.

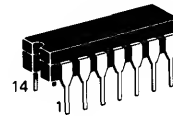
The inhibit feature permits use in party-line or data-bus applications. A strobe or inhibitor, common to both drivers, is included to increase driver-logic versatility. With output current in the inhibited mode, $I_{O(off)}$ is specified so that minimum line loading occurs when the driver is used in a party-line system with other drivers. Output impedance of the driver in inhibited mode is very high (the output impedance of a transistor biased to cutoff).

All driver outputs have a common-mode voltage range of -3.0 volts to $+3.0$ volts, allowing common-mode voltage on the line without affecting driver performance.

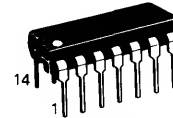
- Insensitive to Supply Variations Over the Entire Operating Range
- M TTL Input Compatibility
- Current-Mode Output (12 mA Typical)
- High Output Impedance
- Common-Mode Output Voltage Range (-3.0 V to $+3.0$ V)
- Inhibitor Available for Driver Selection

DUAL LINE DRIVERS

SILICON MONOLITHIC INTEGRATED CIRCUIT



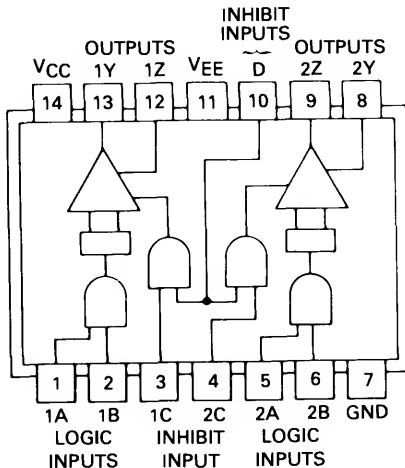
L SUFFIX
 CERAMIC PACKAGE
 CASE 632



P SUFFIX
 PLASTIC PACKAGE
 CASE 646

7

PIN CONNECTIONS



TRUTH TABLE

LOGIC INPUTS		INHIBITOR INPUTS		OUTPUTS	
A	B	C	D	Y	Z
L or H	L or H	L	L or H	H	H
L or H	L or H	L or H	L	H	H
L	L or H	H	H	L	H
L or H	L	H	H	L	H
H	H	H	H	H	L

Low output represents the "on" state.
 High output represents the "off" state.

MC75S110

MAXIMUM RATINGS (T_A = 0 to +70°C unless otherwise noted.)

Ratings	Symbol	Value	Unit
Power Supply Voltages (See Note 1)	V _{CC} V _{EE}	+7.0 -7.0	Volts
Logic and Inhibitor Input Voltages (See Note 1)	V _{in}	5.5	Volts
Common-Mode Output Voltage Range (See Note 1)	V _{OCR}	-5.0 to +7.0	Volts
Power Dissipation (Package Limitation) Plastic and Ceramic Dual In-Line Packages Derate above T _A = +25°C	P _D	1000 3.85	mW mW/°C
Operating Temperature Range	T _A	0 to +70	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

NOTE 1. These voltage values are with respect to the ground terminal.

RECOMMENDED OPERATING CONDITIONS (See Notes 1 and 2.)

Characteristic	Symbol	Min	Nom	Max	Unit
Power Supply Voltages	V _{CC} V _{EE}	+4.75 -4.75	+5.0 -5.0	+5.25 -5.25	Volts
Common-Mode Output Voltage Range	V _{OCR}	-3.0	—	+3.0	Volts

NOTE 2. When using only one channel of the line drivers, the other channel should be inhibited and/or its outputs grounded.

DEFINITIONS OF INPUT LOGIC LEVELS*

Characteristic	Symbol	Test Figure	Min	Max	Unit
High-Level Input Voltage (at any input)	V _{IH}	1,2	2.0	5.25	Volts
Low-Level Input Voltage (at any input)	V _{IL}	1,2	0	0.8	Volts

* The algebraic convention, where the most positive limit is designated maximum, is used with Logic Level Input Voltage Levels only.

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_D(T_A) = \frac{T_J(\max) - T_A}{R_{\theta JA}(T_{yp})}$$

Where: P_D(T_A) = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply volt-

ages and supply currents at the worst case operating condition.

T_J(max) = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

R_{θJA}(T_{yp}) = Typical Thermal Resistance Junction to Ambient

MC75S110

ELECTRICAL CHARACTERISTICS ($T_A = 0$ to $+70^\circ\text{C}$ unless otherwise noted.)

Characteristic**	Symbol	Test Figure	Min	Typ*	Max	Unit
High-Level Input Current to 1A, 1B, 2A or 2B ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$, $V_{IH_L} = 2.4 \text{ V}$)* ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$, $V_{IH_L} = V_{CC} \text{ Max}$)	I_{IH_L}	1	— —	— —	40 1.0	μA mA
Low-Level Input Current to 1A, 1B, 2A or 2B ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$, $V_{IL_L} = 0.4 \text{ V}$)	I_{IL_L}	1	—	—	-3.0	mA
High-Level Input Current into 1C or 2C ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$, $V_{IH_I} = 2.4 \text{ V}$) ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$, $V_{IH_I} = V_{CC} \text{ Max}$)	I_{IH_I}	1	— —	— —	40 1.0	μA mA
Low-Level Input Current into 1C or 2C ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$, $V_{IL_I} = 0.4 \text{ V}$)	I_{IL_I}	1	—	—	-3.0	mA
High-Level Input Current into D ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$, $V_{IH_I} = 2.4 \text{ V}$) ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$, $V_{IH_I} = V_{CC} \text{ Max}$)	I_{IH_I}	1	— —	— —	80 2.0	μA mA
Low-Level Input Current into D ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$, $V_{IL_I} = 0.4 \text{ V}$)	I_{IL_I}	1	—	—	-6.0	mA
Output Current ("on" state) ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$) ($V_{CC} = \text{Min}$, $V_{EE} = \text{Min}$)	$I_{O(\text{on})}$	2	— 6.5	12 —	15 —	mA
Output Current ("off" state) ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$) ($V_{CC} = \text{Min}$, $V_{EE} = \text{Min}$)	$I_{O(\text{off})}$	2	— —	— —	100 100	μA
Supply Current from V_{CC} (with driver enabled) ($V_{IL_L} = 0.4 \text{ V}$, $V_{IH_I} = 2.0 \text{ V}$)	$I_{CC(\text{on})}$	3	—	—	35	mA
Supply Current from V_{EE} (with driver enabled) ($V_{IL_L} = 0.4 \text{ V}$, $V_{IH_I} = 2.0 \text{ V}$)	$I_{EE(\text{on})}$	3	—	—	-50	mA
Supply Current from V_{CC} (with driver inhibited) ($V_{IL_L} = 0.4 \text{ V}$, $V_{IL_I} = 0.4 \text{ V}$)	$I_{CC(\text{off})}$	3	—	—	35	mA
Supply Current from V_{EE} (with driver inhibited) ($V_{IL_L} = 0.4 \text{ V}$, $V_{IL_I} = 0.4 \text{ V}$)	$I_{EE(\text{off})}$	3	—	—	-50	mA

*All typical values are at $V_{CC} = +5.0 \text{ V}$, $V_{EE} = -5.0 \text{ V}$.

**For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.

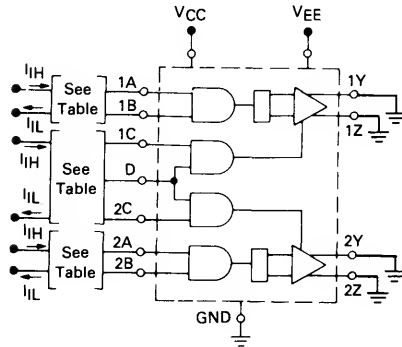
SWITCHING CHARACTERISTICS ($V_{CC} = +5.0 \text{ V}$, $V_{EE} = -5.0 \text{ V}$, $T_A = +25^\circ\text{C}$.)

Characteristic	Symbol	Test Figure	Min	Typ	Max	Unit
Propagation Delay Time from Logic Input A or B to Output Y or Z ($R_L = 50 \text{ ohms}$, $C_L = 40 \text{ pF}$)	t_{PLH_L} t_{PHL_L}	4	— —	9.0 9.0	15 15	ns
Propagation Delay Time from Inhibitor Input C or D to Output Y or Z ($R_L = 50 \text{ ohms}$, $C_L = 40 \text{ pF}$)	t_{PLH_I} t_{PHL_I}	4	— —	16 13	25 25	ns

MC75S110

TEST CIRCUITS

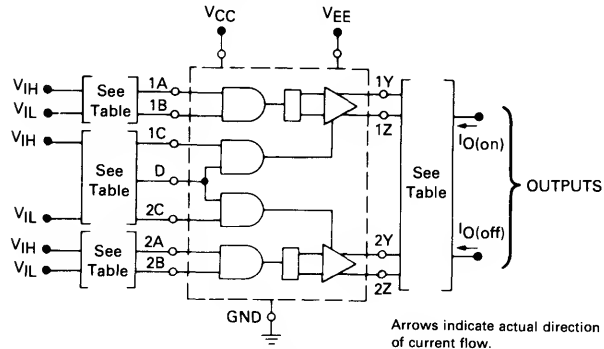
FIGURE 1 — I_{IH} , I_{IL}



TEST TABLE

TEST AT ANY INPUT	ADJACENT INPUTS NOT UNDER TEST
I_{IH}	GND
I_{IL}	4.5 V

FIGURE 2 — $I_{O(on)}$ and $I_{O(off)}$



Arrows indicate actual direction of current flow.

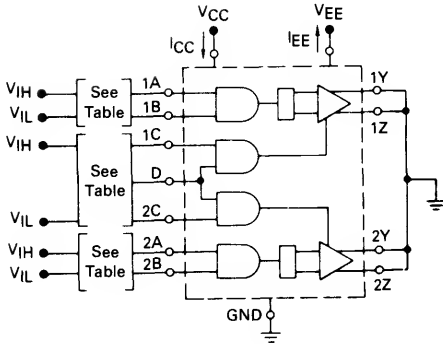
TEST TABLE

TEST Ground all output pins not under test.		LOGIC INPUTS		INHIBITOR INPUTS	
		1A or 2A	1B or 2B	1C or 2C	D
$I_{O(on)}$	at output 1Y or 2Y	V_{IL}	V_{IL}	V_{IH}	V_{IH}
		V_{IL}	V_{IH}		
		V_{IH}	V_{IL}		
$I_{O(on)}$	at output 1Z or 2Z	V_{IH}	V_{IH}	V_{IH}	V_{IH}
$I_{O(off)}$	at output 1Y or 2Y	V_{IH}	V_{IH}	V_{IH}	V_{IH}
		V_{IL}	V_{IL}		
		V_{IL}	V_{IH}		
$I_{O(off)}$	at output 1Z or 2Z	V_{IH}	V_{IL}	V_{IH}	V_{IH}
		Either state	Either state		
		Either state	Either state		

MC75S110

TEST CIRCUITS (continued)

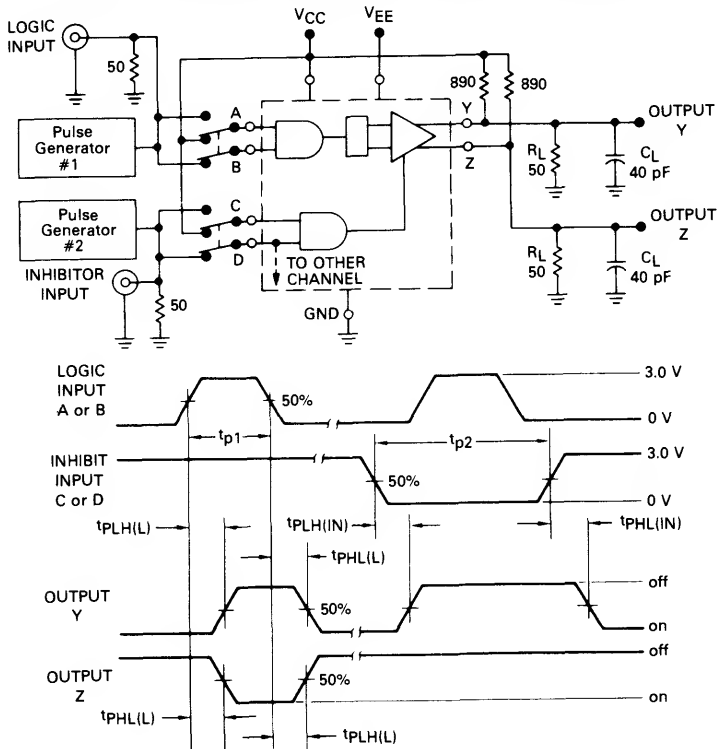
FIGURE 3 — I_{CC} and I_{EE}



TEST TABLE

TEST	ALL LOGIC INPUTS	ALL INHIBITOR INPUTS
$I_{CC}(\text{on})$ Driver enabled	V_{IL}	V_{IH}
$I_{EE}(\text{on})$ Driver enabled	V_{IL}	V_{IH}
$I_{CC}(\text{off})$ Driver inhibited	V_{IL}	V_{IL}
$I_{EE}(\text{off})$ Driver inhibited	V_{IL}	V_{IL}

FIGURE 4 — PROPAGATION DELAY TIMES TEST CIRCUIT AND WAVEFORMS



- NOTES: 1. The pulse generators have the following characteristics: $z_0 = 50 \Omega$, $t_r = t_f = 10 \pm 5.0 \text{ ns}$, $t_{p1} = 500 \text{ ns}$, $\text{PRR} = 1.0 \text{ MHz}$, $t_{p2} = 1.0 \text{ ms}$, $\text{PRR} = 500 \text{ kHz}$.
2. C_L includes probe and jig capacitance.
3. For simplicity, only one channel and the inhibitor connections are shown.

MC75125
MC75127

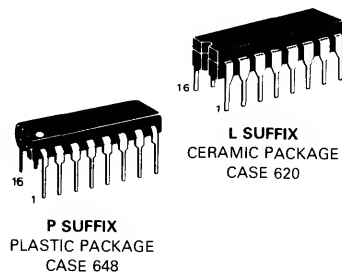
SEVEN CHANNEL
LINE RECEIVERS

SEVEN CHANNEL LINE RECEIVERS

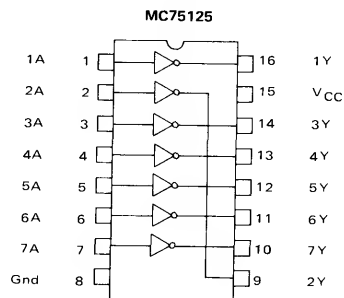
The MC75125 and MC75127 are seven-channel line receivers designed to satisfy the requirements of the input/output interface specification for IBM 360/370.

Special low-power design and Schottky-diode-clamped transistors allow low supply-current requirements while maintaining fast switching speeds and high-current TTL outputs. The MC75125 and MC75127 are characterized for operation from 0 to 70°C.

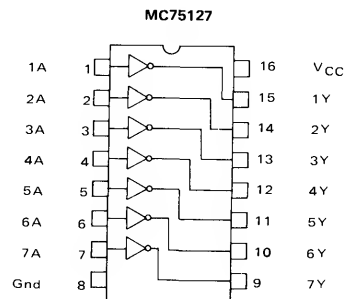
- Meets IBM 360/370 I/O Specification
- Input Resistance $\sim 7\text{ k}\Omega$ to $20\text{ k}\Omega$
- Output Compatible with DTL or TTL
- Schottky-Clamped Transistors
- Operates from a Single 5 Volt Supply
- High-Speed — Low Propagation Delay
- Ratio Specification — t_{PLH}/t_{PHL}
- Seven Channels in One 16-Pin Package
- Standard V_{CC} and Ground Positioning on MC75127



PIN CONNECTIONS

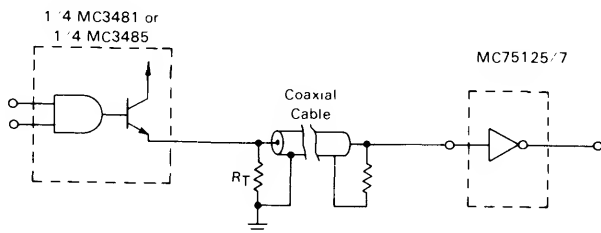


Logic: $Y = \bar{A}$



Logic: $Y = \bar{A}$

TYPICAL APPLICATIONS



MC75125, MC75127

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V _{CC}	+7.0	V
Input Voltage	V _I	-2.0 to +7.0	V
Power Dissipation (Package Limitation)			
Ceramic Package	P _D	1150	mW
Plastic Package		960	
Derate Above T _A = 25°C	1/R _{θJA}	7.7	mW/°C
Operating Ambient Temperature Range	T _A	0 to +70	°C
Junction Temperature	T _J		°C
Ceramic Package		+175	
Plastic Package		+150	
Storage Temperature Range	T _{stg}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V _{CC}	4.5	5.0	5.5	V _{dc}
High Level Output Current	I _{OH}	—	—	-0.4	mA
Low Level Output Current	I _{OL}	—	—	16	mA
Operating Ambient Temperature Range	T _A	0	—	+70	°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, these specifications apply over recommended power supply and temperature ratings. Typical values measured at T_A = 25°C and V_{CC} = +5.0 V)

Characteristic	Symbol	Min	Typ	Max	Unit
High-Level Input Voltage	V _{IH}	1.7	—	—	V
Low-Level Input Voltage	V _{IL}	—	—	0.7	V
High-Level Output Voltage (V _{CC} = 4.5 V, V _{IL} = 0.7 V, I _{OH} = -0.4 mA)	V _{OH}	2.4	3.1	—	V
Low-Level Output Voltage (V _{CC} = 4.5 V, V _{IH} = 1.7 V, I _{OL} = 16 mA)	V _{OL}	—	0.4	0.5	V
High-Level Input Current (V _{CC} = 5.5 V, V _I = 3.11 V)	I _{IH}	0.2	0.3	0.42	mA
Low-Level Input Current (V _{CC} = 5.5 V, V _I = 0.15 V)	I _{IL}	—	—	-0.24	mA
Short Circuit Output Current* (V _{CC} = 5.5 V, V _O = 0)	I _{OS}	-18	—	-60	mA
Input Resistance (V _{CC} = 4.5 V, 0 V, or Open, ΔV _I = 0.15 V to 4.15 V)	r _i	7.4	—	20	kΩ
Power Supply Current Outputs High-Logic State (V _{CC} = 5.5 V, I _{OH} = -0.4 mA, all inputs at 0.7 V)	I _{CCH}	—	15	25	mA
Power Supply Current Outputs Low-Logic State (V _{CC} = 5.5 V, I _{OL} = 16 mA, all inputs at 4.0 V)	I _{CCL}	—	28	47	mA

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C, R_L = 400 Ω, C_L = 50 pF, unless otherwise noted. See Figure 1)

Characteristic	Symbol	MC75125			MC75127			Unit
		Min	Typ	Max	Min	Typ	Max	
Propagation Delay Time								ns
Low-to-High-Level Output	t _{PLH}	7.0	14	25	7.0	14	25	
High-to-Low-Level Output	t _{PHL}	10	18	30	10	18	30	
Ratio of Propagation Delay Times	t _{PLH} /t _{PHL}	0.5	0.8	1.3	0.5	0.8	1.3	
Transition Time, Low-to-High-Level Output	t _{TLH}	1.0	7.0	12	1.0	7.0	12	ns
Transition Time, High-to-Low Level Output	t _{THL}	1.0	3.0	12	1.0	3.0	12	ns

* No more than one output should be shorted at a time.

MC75125, MC75127

FIGURE 1 — PARAMETER MEASUREMENT INFORMATION

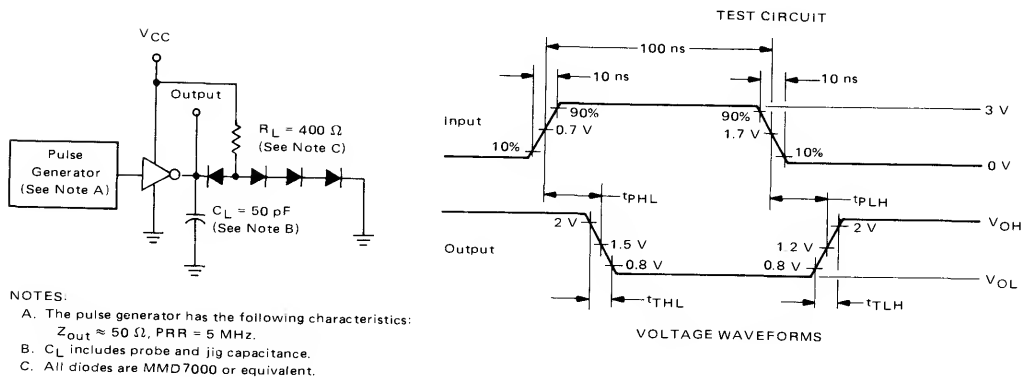
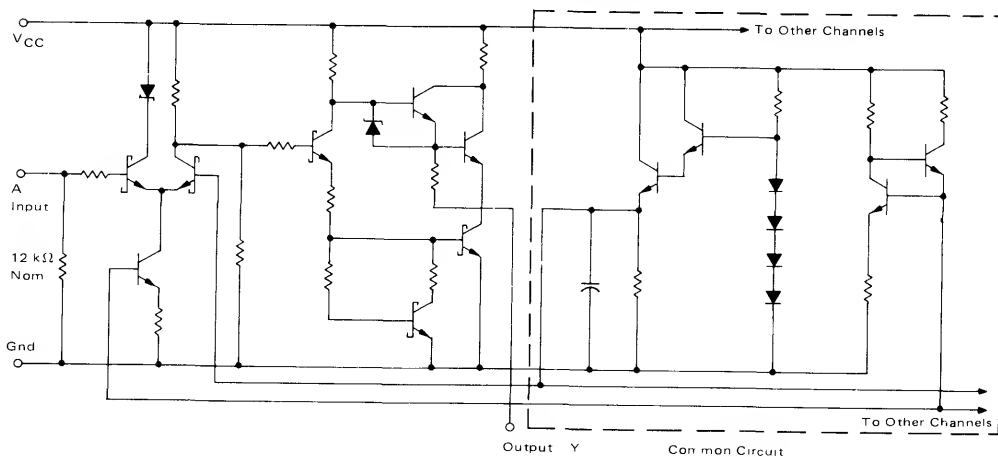


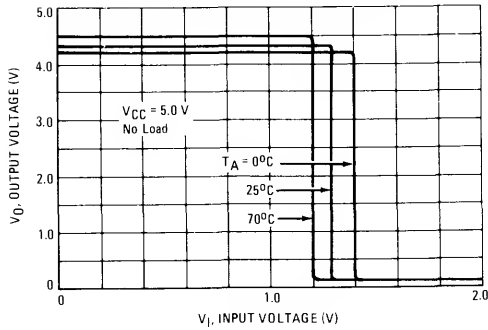
FIGURE 2 — SCHEMATIC (EACH RECEIVER)



MC75125, MC75127

TYPICAL CHARACTERISTICS

**FIGURE 3 – VOLTAGE TRANSFER CHARACTERISTICS
versus AMBIENT TEMPERATURE**



**FIGURE 4 – VOLTAGE TRANSFER CHARACTERISTIC
versus SUPPLY VOLTAGE**

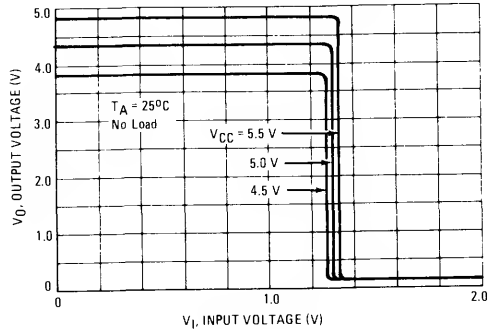
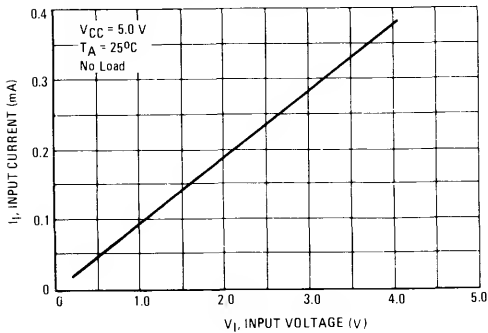


FIGURE 5 – INPUT CURRENT versus INPUT VOLTAGE



**FIGURE 6 – LOW-LEVEL OUTPUT VOLTAGE
versus OUTPUT CURRENT**

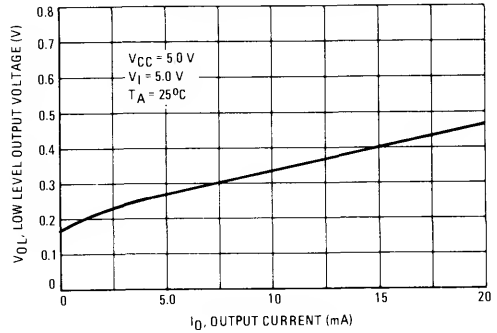
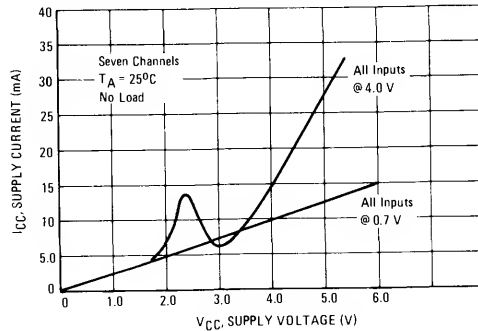


FIGURE 7 – SUPPLY CURRENT versus SUPPLY VOLTAGE



MC75128
MC75129

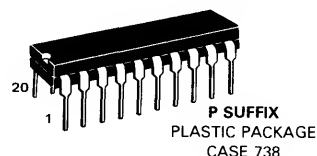
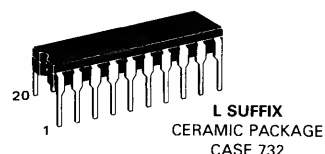
**EIGHT-CHANNEL
 LINE RECEIVERS**

EIGHT-CHANNEL LINE RECEIVERS

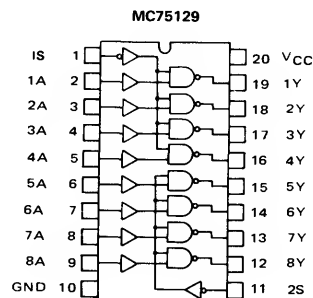
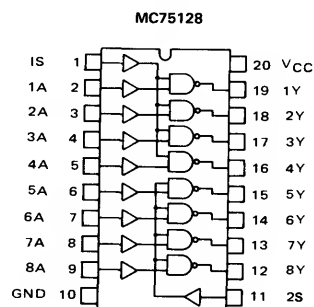
The MC75128 and MC75129 are eight-channel line receivers designed to satisfy the requirements of the input/output interface specification for IBM 360/370. Both devices feature common strobes for each group of four receivers. The MC75128 has an active high strobe; the MC75129 has an active low strobe.

Special low-power design and Schottky-diode-clamped transistors allow low supply current requirements while maintaining fast switching speeds and high-current TTL outputs. Both devices are characterized for operation from 0 to 70°C.

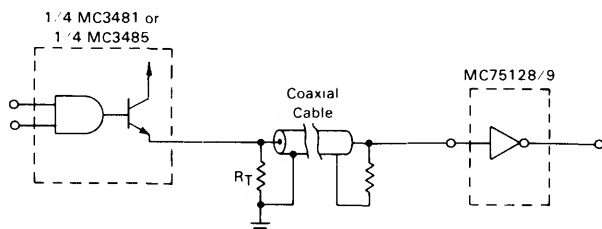
- Meets IBM 360/370 I/O Specification
- Input Resistance — 7 k Ω to 20 k Ω
- Output Compatible with DTL or TTL
- Schottky-Clamped Transistors
- Operates from a Single 5 Volt Supply
- High-Speed — Low Propagation Delay
- Ratio Specification — t_{PLH}/t_{PHL}
- Common Strobe for Each Group of Four Receivers
- MC75128 Strobe — Active-High
 MC75129 Strobe — Active-Low



PIN CONNECTIONS



TYPICAL APPLICATION



MC75128, MC75129

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V _{CC}	+7.0	V
A Input Voltage	V _{IA}	-0.15 to +7.0	V
Strobe Input Voltage	V _{IS}	+7.0	V
Power Dissipation (Package Limitation)	P _D	1150	mW
Ceramic Package		960	
Plastic Package		-7.7	mW/°C
Derate Above T _A = 25°C	1/R _{θJA}		
Operating Ambient Temperature Range	T _A	0 to +70	°C
Junction Temperature	T _J	+175	°C
Ceramic Package		+150	
Plastic Package			
Storage Temperature Range	T _{stg}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V _{CC}	4.5	5.0	5.5	Vdc
High Level Output Current	I _{OH}	—	—	-0.4	mA
Low Level Output Current	I _{OL}	—	—	16	mA
Operating Ambient Temperature Range	T _A	0	—	+70	°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, these specifications apply over recommended power supply and temperature ratings. Typical values measured at T_A = 25°C and V_{CC} = +5.0 V)

Characteristic	Symbol	Min	Typ	Max	Unit
High-Level Input Voltage	V _{IH}	1.7	—	—	V
A Inputs		2.0	—	—	
S Inputs		—	—	—	
Low-Level Input Voltage	V _{IL}	—	—	0.7	V
A Inputs		—	—	0.7	
S Inputs		—	—	—	
High-Level Output Voltage (V _{CC} = 4.5 V, V _{IL} = 0.7 V, I _{OH} = -0.4 mA)	V _{OH}	2.4	3.1	—	V
Low-Level Output Voltage (V _{CC} = 4.5 V, V _{IH} = 1.7 V, I _{OL} = 16 mA)	V _{OL}	—	0.4	0.5	V
Input Clamp Voltage (V _{CC} = 4.5 V, I _I = -18 mA, S Inputs)	V _{IK}	—	—	-1.5	V
High-Level Input Current (V _{CC} = 5.5 V, V _I = 3.11 V, A Inputs)	I _{IH}	—	0.3	0.42	mA
(V _{CC} = 5.5 V, V _I = 2.7 V, S Inputs)		—	—	20	μA
Low-Level Input Current (V _{CC} = 5.5 V, V _I = 0.15 V, A Inputs)	I _{IL}	—	—	-0.24	mA
(V _{CC} = 5.5 V, V _I = 0.4 V, S Inputs)		—	—	-0.4	
Short Circuit Output Current * (V _{CC} = 5.5 V, V _O = 0)	I _{OS}	-18	—	-60	mA
Input Resistance (V _{CC} = 4.5 V, 0 V, or Open, ΔV _I = 0.15 V to 4.15 V)	r _i	7.0	—	20	kΩ
Power Supply Current — Outputs High-Logic State, all inputs at 0.7 V	I _{CCH}	—	19	31	mA
(V _{CC} = 5.5 V, Strobe at 2.4 V — MC75128)		—	19	31	
(V _{CC} = 5.5 V, Strobe at 0.4 V — MC75129)		—	—	—	
Power Supply Current — Outputs Low-Logic State, all inputs at 4.0 V	I _{CCL}	—	32	53	mA
(V _{CC} = 5.5 V, Strobe at 2.4 V — MC75128)		—	32	53	
(V _{CC} = 5.5 V, Strobe at 0.4 V — MC75129)		—	—	—	

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C, R_L = 400 Ω, C_L = 50 pF, unless otherwise noted, See Figures 1 and 2)

Characteristic	Symbol	MC75128			MC75129			Unit
		Min	Typ	Max	Min	Typ	Max	
Propagation Delay Time — From A Inputs								
Low-to-High-Level Output	t _{PLH} (A)	7.0	14	25	7.0	14	25	ns
High-to-Low-Level Output	t _{PHL} (A)	10	18	30	10	18	30	
Propagation Delay Time — From S Inputs								
Low-to-High-Level Output	t _{PLH} (S)	—	26	40	—	20	35	ns
High-to-Low-Level Output	t _{PHL} (S)	—	22	35	—	16	30	
Ratio of Propagation Delay Times — A Inputs	t _{PLH} (A)/t _{PHL} (A)	0.5	0.8	1.3	0.5	0.8	1.3	
Transition Time, Low-to-High-Level Output	t _{TLH}	1.0	7.0	12	1.0	7.0	12	ns
Transition Time, High-to-Low-Level Output	t _{THL}	1.0	3.0	12	1.0	3.0	12	ns

*No more than one output should be shorted at a time.

MC75128, MC75129

FIGURE 1 – PARAMETER MEASUREMENT INFORMATION

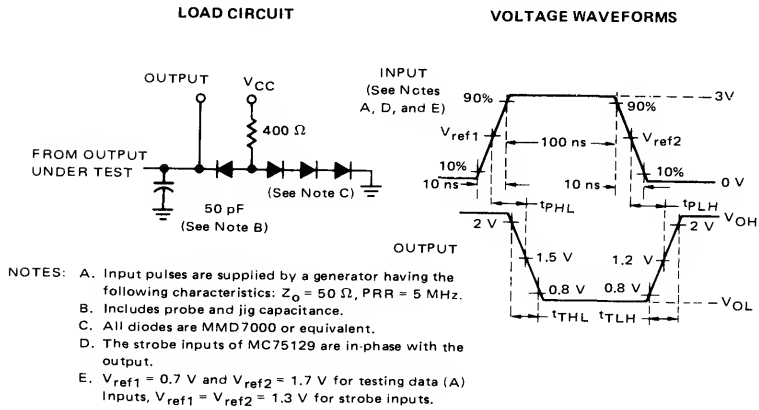
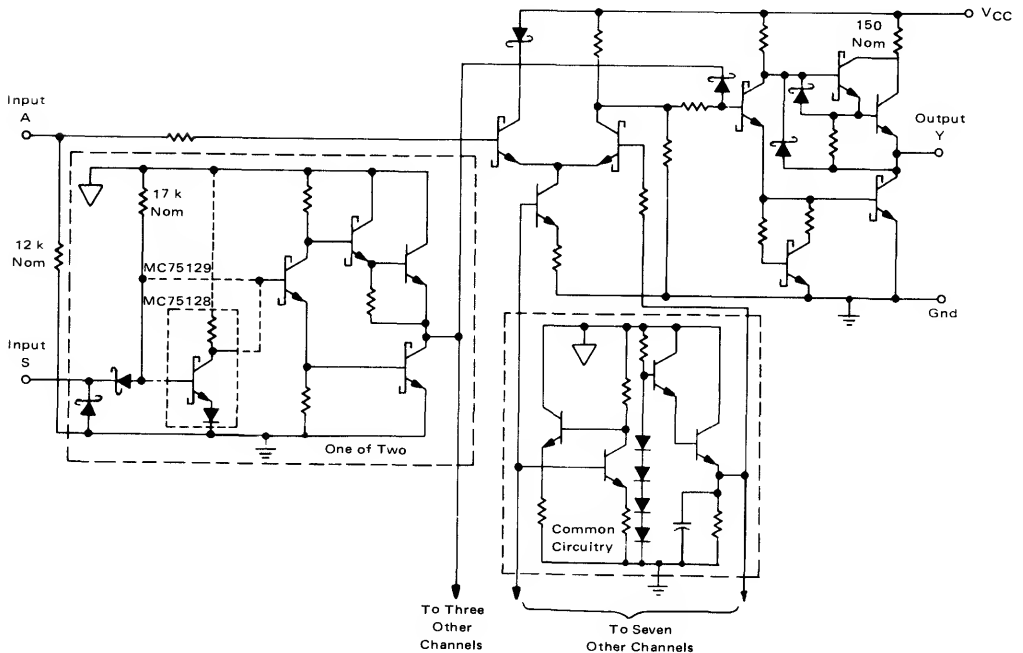


FIGURE 2 – SCHEMATIC (EACH RECEIVER)



MC75128, MC75129

TYPICAL CHARACTERISTICS

FIGURE 3 — VOLTAGE TRANSFER CHARACTERISTICS
versus AMBIENT TEMPERATURE

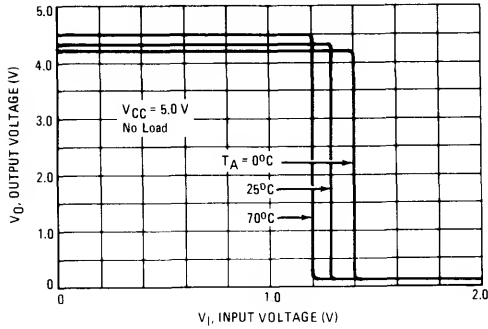


FIGURE 4 — VOLTAGE TRANSFER CHARACTERISTIC
versus SUPPLY VOLTAGE

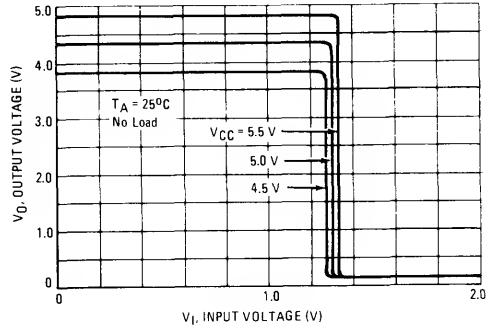


FIGURE 5 — INPUT CURRENT versus INPUT VOLTAGE

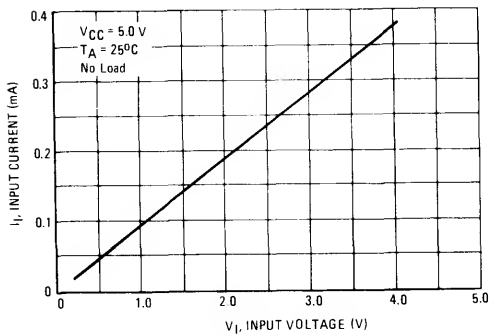
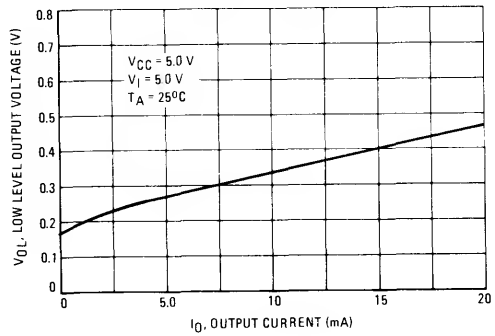


FIGURE 6 — LOW-LEVEL OUTPUT VOLTAGE
versus OUTPUT CURRENT



7

SN75172
SN75174

Product Preview

**QUAD LINE DRIVERS WITH NAND ENABLED
THREE-STATE OUTPUTS**

The Motorola SN75172/174 are monolithic quad differential line drivers with three-state outputs. They are designed specifically to meet the requirements of EIA-485, EIA-422A Standards and CCITT recommendations V.11 and X.27.

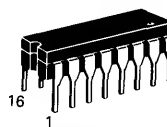
The device is optimized for balanced multipoint bus transmission at rates up to 4 megabits per second. Each driver features wide positive and negative common-mode output voltage ranges making it suitable for party-line applications in noisy environments.

The SN75172/174 provides positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. Shutdown occurs at a junction temperature of approximately 150°C. These devices offer optimum performance when used with the SN75173 or SN75175 quadruple differential line receivers.

- Meets EIA-485 Standard for Party-Line Operation
- Meets EIA Standard EIA-422A and CCITT Recommendations V.11 and X.27
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Common Mode Output Voltage Range . . . -7.0 V to 12 V
- Active High and Active Low Enables
- Thermal Shutdown Protection
- Positive and Negative Current Limiting
- Operates from Single 5.0 Volt Supply
- Low Power Requirements
- Functionally Interchangeable With AM26LS31 (SN75172) MC3487 (SN75174)

**QUAD EIA-485 LINE DRIVERS
WITH THREE-STATE OUTPUTS**

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**

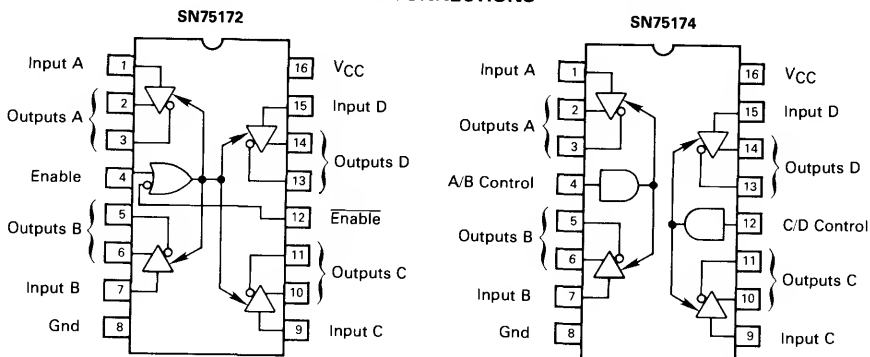


J SUFFIX
CERAMIC PACKAGE
CASE 620



N SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS



This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

SN75172, SN75174

SN75172

TRUTH TABLE			
Input	Control Inputs (E/ \bar{E})	Noninverting Output	Inverting Output
H	H/L	H	L
L	H/L	L	H
X	L/H	Z	Z
L = Low Logic State H = High Logic State X = Irrelevant Z = Third-State (High Impedance)			

SN75174

TRUTH TABLE			
Input	Control Input	Noninverting Output	Inverting Output
H	H	H	L
L	H	L	H
X	L	Z	Z
L = Low Logic State H = High Logic State X = Irrelevant Z = Third-State (High Impedance)			

SN75173
SN75175

QUAD EIA-485 LINE RECEIVERS

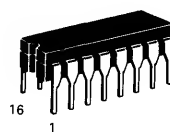
The Motorola SN75173/175 are monolithic quad differential line receivers with three-state outputs. They are designed specifically to meet the requirements of EIA-485, EIA-422A/23A Standards and CCITT recommendations.

The devices are optimized for balanced multipoint bus transmission at rates up to 10 megabits per second. They also feature high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ± 200 millivolts over a common mode input voltage range of -12 volts to 12 volts. The SN75173/175 are designed for optimum performance when used with the SN75172 or SN75174 quad differential line drivers.

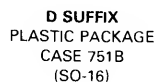
- Meets EIA Standards EIA-422A and EIA-423A, EIA-485
- Meets CCITT Recommendations V.10, V.11, X.26, and X.27
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Common-Mode Input Voltage Range . . . -12 V to 12 V
- Input Sensitivity . . . ± 200 mV
- Input Hysteresis . . . 50 mV Typ
- High Input Impedance . . . 1 EIA-485 Unit Load
- Operates from Single 5.0 V Supply
- Low Power Requirements
- Plug-In Replacement for MC3486 (SN75175)
 AM26LS32 (SN75173)

QUAD EIA-485
LINE RECEIVERS WITH
THREE-STATE OUTPUTS

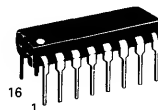
SILICON MONOLITHIC
INTEGRATED CIRCUITS



J SUFFIX
 CERAMIC PACKAGE
 CASE 620

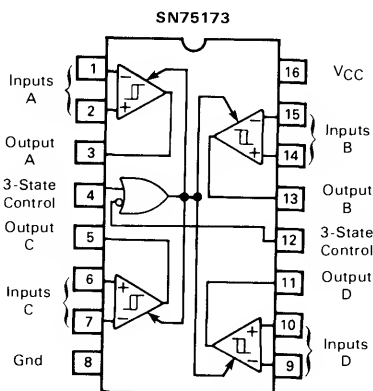


D SUFFIX
 PLASTIC PACKAGE
 CASE 751B
 (SO-16)

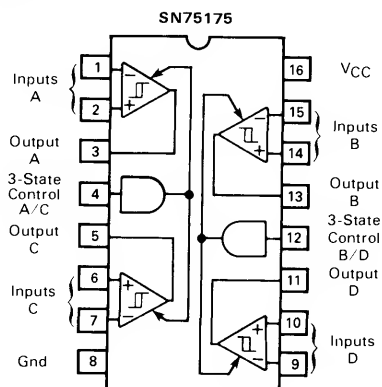


N SUFFIX
 PLASTIC PACKAGE
 CASE 648

PIN CONNECTIONS



ORDERING INFORMATION		
Device	Temperature	Package
SN75173J	0 to $+70^{\circ}\text{C}$	Ceramic DIP
SN75173N	0 to $+70^{\circ}\text{C}$	Plastic DIP



ORDERING INFORMATION		
Device	Temperature	Package
SN75175J	0 to $+70^{\circ}\text{C}$	Ceramic DIP
SN75175N	0 to $+70^{\circ}\text{C}$	Plastic DIP

SN75173, SN75175

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Input Common Mode Voltage	V_{ICM}	± 25	Vdc
Input Differential Voltage	V_{ID}	± 25	Vdc
Three-State Control Input Voltage	V_I	7.0	Vdc
Output Sink Current	I_O	50	mA
Storage Temperature	T_{stg}	-65 to +150	$^{\circ}\text{C}$
Operating Junction Temperature — Ceramic Package — Plastic Package	T_J	+175 +150	$^{\circ}\text{C}$

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	4.75 to 5.25	Vdc
Operating Ambient Temperature	T_A	0 to +70	$^{\circ}\text{C}$
Input Common Mode Voltage Range	V_{ICM}	-12 to +12	Vdc
Input Differential Voltage Range	V_{IDR}	-12 to +12	Vdc

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, minimum and maximum limits apply over recommended temperature and power supply voltage ranges. Typical values are for $T_A = 25^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V}$ and $V_{ICM} = 0\text{ V}$) (Note 1)

Characteristic	Symbol	Min	Typ	Max	Unit
Differential Input Threshold Voltage (Note 2) ($-12\text{ V} \leq V_{ICM} \leq 12\text{ V}$, $V_{IH} = 2.0\text{ V}$) ($I_O = -0.4\text{ mA}$, $V_{OH} \geq 2.7\text{ V}$) ($I_O = 16\text{ mA}$, $V_{OL} \leq 0.5\text{ V}$)	$V_{TH(D)}$	—	—	0.2 -0.2	V
Input Hysteresis	$V_{T+} - V_{T-}$	—	50	—	mV
Input Line Current (Differential Inputs) (Unmeasured Input at 0 V — Note 3) ($V_I = +12\text{ V}$) ($V_I = -7.0\text{ V}$)	I_I	—	—	1.0 -0.8	mA
Input Resistance (Note 4)	r_i	1 Unit Load	—	—	
Input Balance and Output Level (Note 3) ($-12\text{ V} \leq V_{ICM} \leq 12\text{ V}$, $V_{IH} = 2.0\text{ V}$) ($I_O = -0.4\text{ mA}$, $V_{ID} = 0.2\text{ V}$) ($I_O = 8.0\text{ mA}$, $V_{ID} = -0.2\text{ V}$) ($I_O = 16\text{ mA}$, $V_{ID} = -0.2\text{ V}$)	V_{OH} V_{OL} V_{OL}	2.7 — —	— — —	— 0.45 0.5	V
Input Voltage — High Logic State (Three-State Control)	V_{IH}	2.0	—	—	V
Input Voltage — Low Logic State (Three-State Control)	V_{IL}	—	—	0.8	V
Input Current — High Logic State (Three-State Control) ($V_{IH} = 2.7\text{ V}$) ($V_{IH} = 5.5\text{ V}$)	I_{IH}	— —	— —	20 100	μA
Input Current — Low Logic State (Three-State Control) ($V_{IL} = 0.4\text{ V}$)	I_{IL}	—	—	-100	μA
Input Clamp Diode Voltage (Three-State Control) ($I_{IK} = -18\text{ mA}$)	V_{IK}	—	—	-1.5	V
Output Third State Leakage Current ($V_{I(D)} = 3.0\text{ V}$, $V_{IL} = 0.8\text{ V}$, $V_O = 0.4\text{ V}$) ($V_{I(D)} = -3.0\text{ V}$, $V_{IL} = 0.8\text{ V}$, $V_O = 2.4\text{ V}$)	I_{OZ}	— —	— —	-20 20	μA
Output Short-Circuit Current (Note 5) ($V_{I(D)} = 3.0\text{ V}$, $V_{IH} = 2.0\text{ V}$, $V_O = 0\text{ V}$)	I_{OS}	-15	—	-85	mA
Power Supply Current ($V_{IL} = 0\text{ V}$) (All Inputs Grounded)	I_{CC}	—	—	70	mA

NOTES:

1. All currents into device pins are shown as positive, out of device pins are negative. All voltages referenced to ground unless otherwise noted.
2. Differential input threshold voltage and guaranteed output levels are done simultaneously for worst case.
3. Refer to EIA-485 for exact conditions. Input balance and guaranteed output levels are done simultaneously for worst case.

4. Input resistance should be derived from input line current specifications and is shown for reference only. See EIA-485 and input line current specifications for more specific input resistance information.
5. Only one output at a time should be shorted.

SN75173, SN75175

SWITCHING CHARACTERISTICS (Unless otherwise noted, $V_{CC} = 5.0\text{ V}$ and $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	SN75173			SN75175			Unit
		Min	Typ	Max	Min	Typ	Max	
Propagation Delay Time — Differential Inputs to Output (Output High to Low) (Output Low to High)	$t_{PHL(D)}$	—	25	35	—	25	35	ns
	$t_{PLH(D)}$	—	25	35	—	25	35	
Propagation Delay Time — Three-State Control to Output (Output Low to Third State) (Output High to Third State) (Output Third State to High) (Output Third State to Low)	t_{PLZ}	—	20	40	—	16	35	ns
	t_{PHZ}	—	20	30	—	19	35	
	t_{PZH}	—	16	22	—	11	30	
	t_{PZL}	—	16	25	—	11	30	

SN75173

FUNCTION TABLE (EACH RECEIVER)

Differential Inputs	3-State Control		Output Y
	4	12	
$V_{ID} \geq 0.2\text{ V}$	H	X	H
	X	L	H
$-0.2\text{ V} < V_{ID} < 0.2\text{ V}$	H	X	?
	X	L	?
$V_{ID} \leq -0.2\text{ V}$	H	X	L
	X	L	L
X	L	H	Z

SN75175

FUNCTION TABLE (EACH RECEIVER)

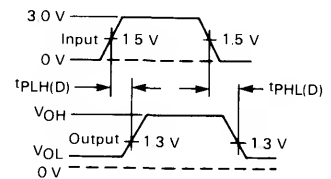
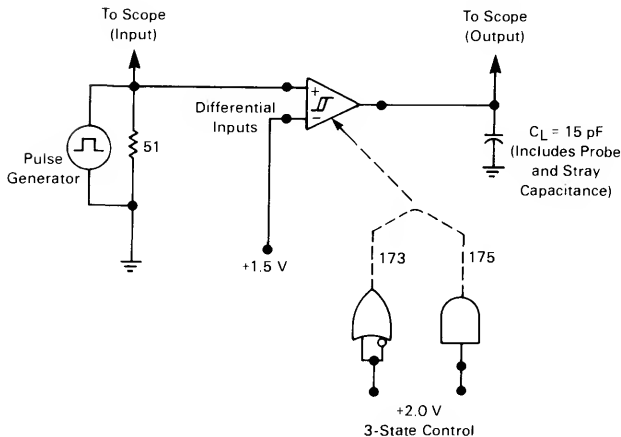
Differential Inputs	3-State Control	Output Y
$V_{ID} \geq 0.2\text{ V}$	H	H
$-0.2\text{ V} < V_{ID} < 0.2\text{ V}$	H	?
$V_{ID} \leq -0.2\text{ V}$	H	L
X	L	Z

H = high level
L = low level
X = irrelevant

? = indeterminate
Z = high-impedance (off)

SWITCHING TEST CIRCUIT AND WAVEFORMS

FIGURE 1 — PROPAGATION DELAY, DIFFERENTIAL INPUT TO OUTPUT



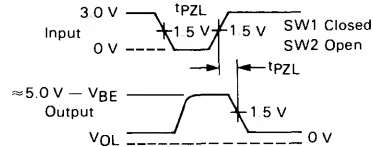
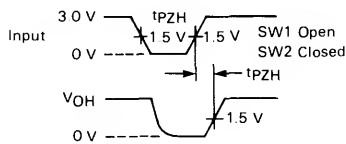
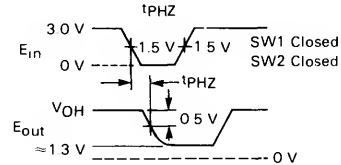
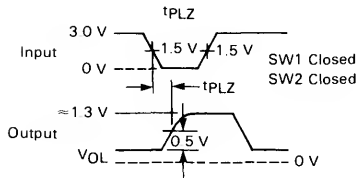
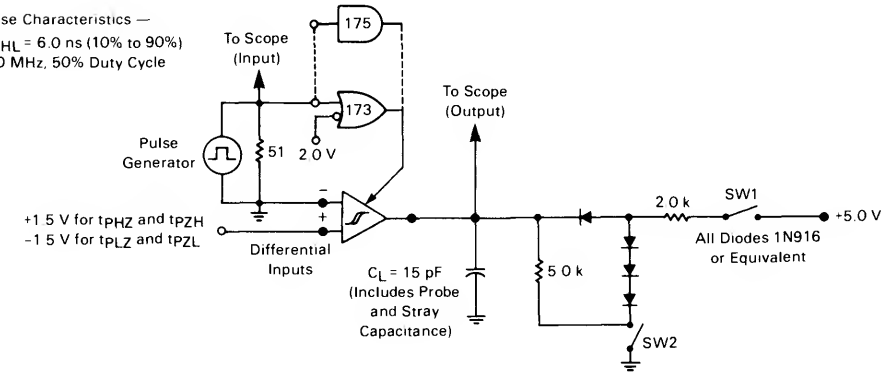
Input Pulse Characteristics —
 $t_{TLH} = t_{THL} = 6.0\text{ ns}$ (10% to 90%)
PRR = 1.0 MHz, 50% Duty Cycle

SN75173, SN75175

SWITCHING TEST CIRCUIT AND WAVEFORMS (continued)

FIGURE 2 — PROPAGATION DELAY, THREE-STATE CONTROL INPUT TO OUTPUT

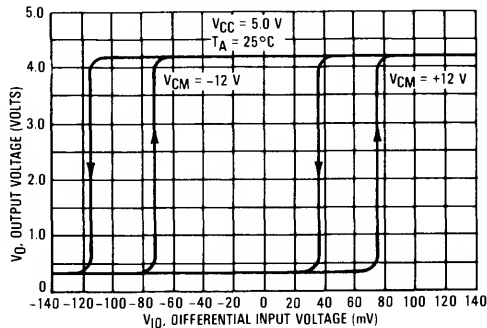
Input Pulse Characteristics —
 $t_{TLH} = t_{THL} = 6.0 \text{ ns}$ (10% to 90%)
 $\text{PRR} = 1.0 \text{ MHz}$, 50% Duty Cycle



TYPICAL CHARACTERISTICS

(Both Device Types, Unless Otherwise Noted)

FIGURE 3 — OUTPUT VOLTAGE versus DIFFERENTIAL INPUT VOLTAGE



TYPICAL CHARACTERISTICS (continued)

FIGURE 4 — OUTPUT VOLTAGE versus 3-STATE CONTROL VOLTAGE

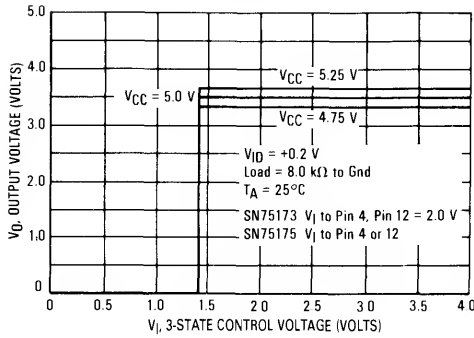


FIGURE 5 — OUTPUT VOLTAGE versus (INVERTED) 3-STATE CONTROL VOLTAGE — SN75173

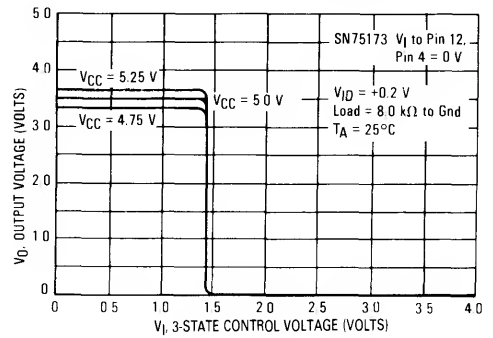


FIGURE 6 — HIGH LEVEL OUTPUT VOLTAGE versus OUTPUT CURRENT

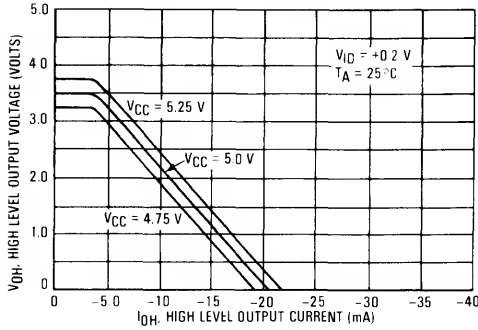


FIGURE 7 — LOW LEVEL OUTPUT VOLTAGE versus OUTPUT CURRENT

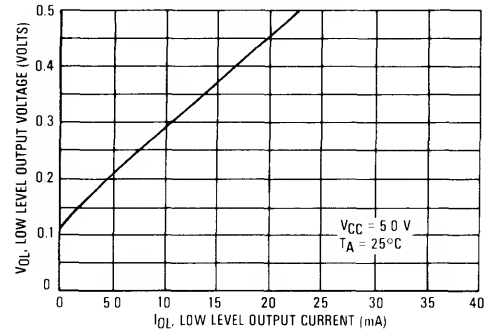


FIGURE 8 — HIGH LEVEL OUTPUT VOLTAGE versus TEMPERATURE

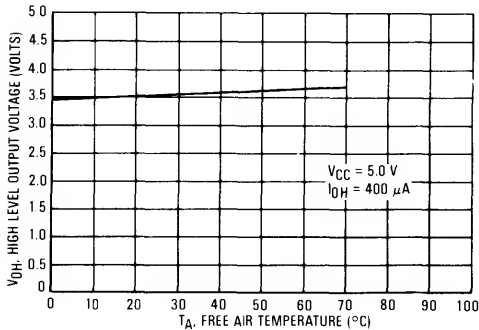
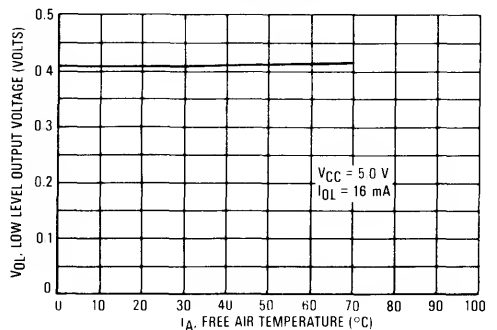


FIGURE 9 — LOW LEVEL OUTPUT VOLTAGE versus TEMPERATURE



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

QUAD 1.5 A SINKING HIGH CURRENT SWITCH

The ULN2068B is a high-voltage, high-current quad Darlington switch array designed for high current loads, both resistive and reactive, up to 300 watts.

It is intended for interfacing between low level (TTL, DTL, LS and 5.0 V CMOS) logic families and peripheral loads such as relays, solenoids, dc and stepping motors, multiplexer LED and incandescent displays, heaters, or other high voltage, high current loads.

The Motorola ULN2068B is specified with minimum guaranteed breakdown of 50 V and is 100% tested for safe area using an inductive load. It includes integral transient suppression diodes. Use of a predriver stage reduces input current while still allowing the device to switch 1.5 Amps.

It is supplied in an improved 16-Pin plastic DIP package with heat sink contact tabs (Pins 4, 5 and 12, 13). A copper alloy lead frame allows maximum power dissipation using standard cooling techniques. The use of the contact tab lead frame facilitates attachment of a DIP heat sink while permitting the use of standard layout and mounting practices.

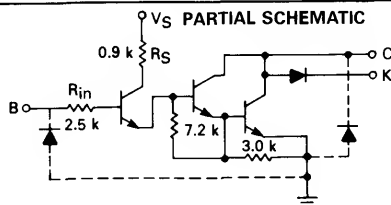
- TTL, DTL, LS, CMOS Compatible Inputs
- 1.5 Amp Maximum Output Current
- Low Input Current
- Internal Freewheeling Clamp Diodes
- 100% Inductive Load Tested
- Heat Tab Copper Alloy Lead Frame for Increased Dissipation

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ and ratings apply to any one device in the package unless otherwise noted)

Rating	Symbol	Value	Unit
Output Voltage	V_O	50	V
Input Voltage (Note 1)	V_I	15	V
Supply Voltage	V_S	10	V
Collector Current (Note 2)	I_C	1.75	A
Input Current (Note 3)	I_I	25	mA
Operating Ambient Temperature Range	T_A	0 to +70	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-55 to +150	$^\circ\text{C}$
Junction Temperature	T_J	150	$^\circ\text{C}$

Notes:

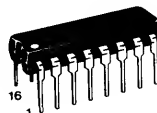
1. Input voltage referenced to ground.
2. Allowable output conditions shown in Figures 11 and 12.
3. May be limited by max input voltage.



ULN2068B

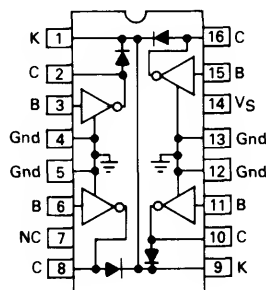
QUAD 1.5 A DARLINGTON SWITCH

SILICON MONOLITHIC INTEGRATED CIRCUIT



B SUFFIX
PLASTIC PACKAGE
CASE 648C

PIN CONNECTIONS



ORDERING INFORMATION*

Device	Temperature Range	Package
ULN2068B	0 $^\circ\text{C}$ to +70 $^\circ\text{C}$	Plastic DIP

*Other options of this ULN2060/2070 series are available for volume applications. Contact your local Motorola Sales Representative.

ULN2068B

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Fig.	Symbol	Min	Typ	Max	Unit
Output Leakage Current ($V_{CE} = 50\text{ V}$) ($V_{CE} = 50\text{ V}$, $T_A = 70^\circ\text{C}$)	1	I_{CEX}	— —	— —	100 500	μA
Collector-Emitter Saturation Voltage ($I_C = 500\text{ mA}$) ($I_C = 750\text{ mA}$) ($I_C = 1.0\text{ A}$) ($I_C = 1.25\text{ A}$) $V_{in} = 2.4\text{ V}$	2	$V_{CE(sat)}$	— — — —	— — — —	1.13 1.25 1.40 1.60	V
Input Current — On Condition ($V_I = 2.4\text{ V}$) ($V_I = 3.75\text{ V}$)	4	$I_{I(on)}$	— —	— —	0.25 1.0	mA
Input Voltage — On Condition ($V_{CE} = 2.0\text{ V}$, $I_C = 1.5\text{ A}$)	5	$V_{I(on)}$	—	—	2.4	V
Inductive Load Test ($V_S = 5.5\text{ V}$, $V_{CC} = 24.5\text{ V}$, $tp_W = 4.0\text{ ms}$)	3	ΔV_{out}	—	—	100	mV
Supply Current ($I_C = 500\text{ mA}$, $V_{in} = 2.4\text{ V}$, $V_S = 5.5\text{ V}$)	8	I_S	—	—	6.0	mA
Turn-On Delay Time (50% E_I to 50% E_O)	—	t_{PHL}	—	—	1.0	μs
Turn-Off Delay Time (50% E_I to 50% E_O)	—	t_{PLH}	—	—	4.0	μs
Clamp Diode Leakage Current ($V_R = 50\text{ V}$) ($V_R = 50\text{ V}$, $T_A = 70^\circ\text{C}$)	6	I_R	— —	— —	50 100	μA
Clamp Diode Forward Voltage ($I_F = 1.0\text{ A}$) ($I_F = 1.5\text{ A}$)	7	V_F	— —	— —	1.75 2.0	V

TEST FIGURES

FIGURE 1

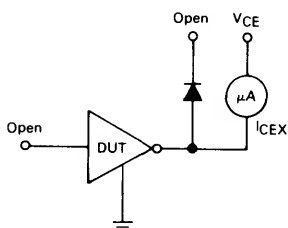


FIGURE 2

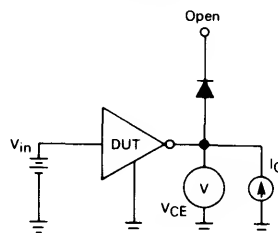


FIGURE 3

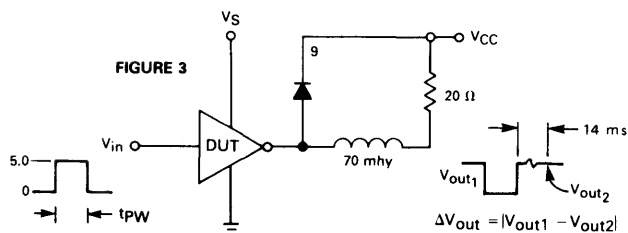
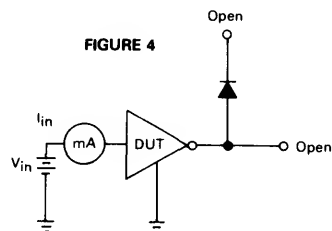


FIGURE 4



ULN2068B

TEST FIGURES (CONTINUED)

FIGURE 5

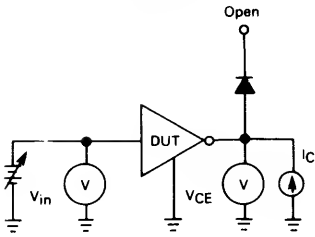


FIGURE 7

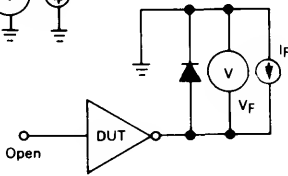


FIGURE 6

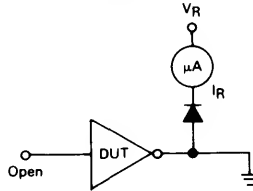
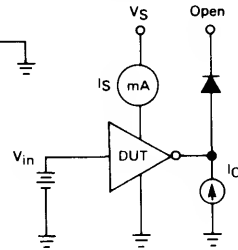


FIGURE 8



TYPICAL CHARACTERISTIC CURVES — $T_A = 25^\circ\text{C}$

FIGURE 9 — INPUT CURRENT versus INPUT VOLTAGE

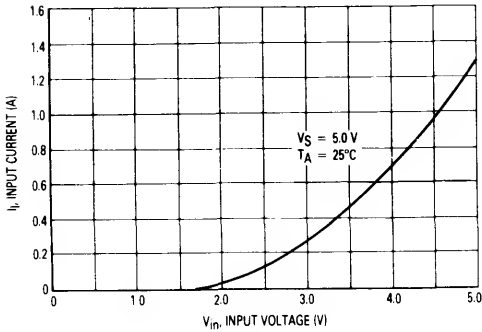


FIGURE 10 — COLLECTOR CURRENT versus INPUT CURRENT

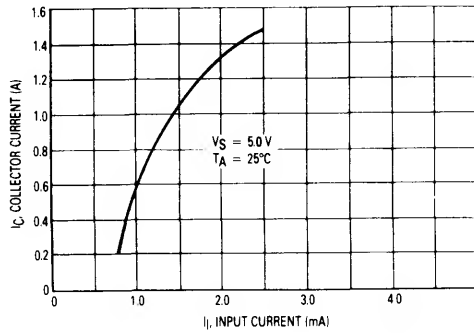


FIGURE 11 — $T_A = 70^\circ\text{C}$ w/o HEAT SINK

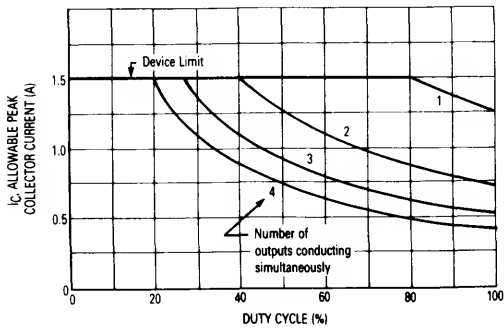


FIGURE 12 — $T_A = 70^\circ\text{C}$ w/STAVER V-8 HEAT SINK (37.5 $^\circ\text{C}/\text{W}$)

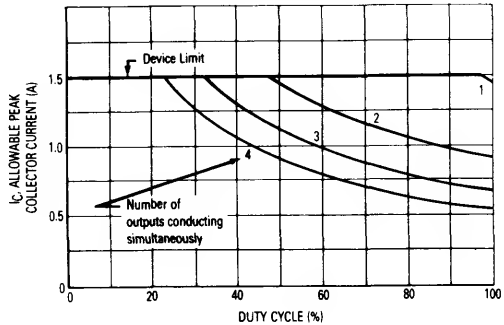


FIGURE 13 — $T_A = 70^\circ\text{C}$ w/STAVR V-7
HEAT SINK (27.5 $^\circ\text{C/W}$)

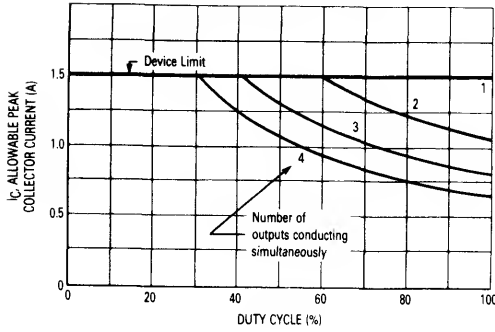


FIGURE 14 — $T_A = 50^\circ\text{C}$ w/o HEAT SINK

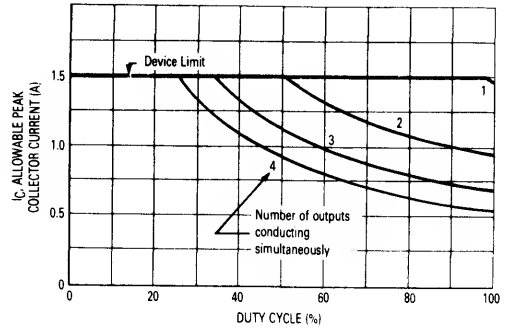


FIGURE 15 — $T_A = 50^\circ\text{C}$ w/STAVR V-8
HEAT SINK (37.5 $^\circ\text{C/W}$)

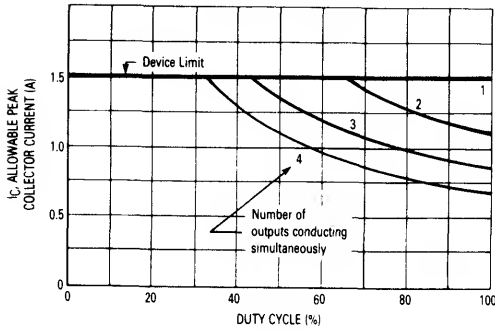
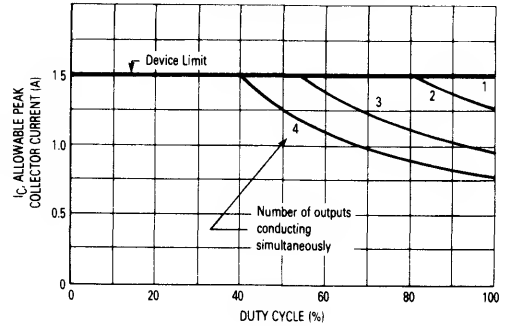


FIGURE 16 — $T_A = 50^\circ\text{C}$ w/STAVR V-7
HEAT SINK (27.5 $^\circ\text{C/W}$)



QUAD 1.5 A SINKING HIGH CURRENT SWITCH

The ULN2074B is a high voltage, high current quad Darlington switch array designed for high current loads, both resistive and reactive, up to 300 watts.

It is intended for interfacing between low level (TTL, DTL, LS and 5.0 V CMOS) logic families and peripheral loads such as relays, solenoids, dc and stepping motors, multiplexer LED and incandescent displays, heaters, or other high-voltage, high current loads.

The Motorola ULN2074B is specified with minimum guaranteed breakdown of 50 V and is 100% tested for safe area using an inductive load.

It is supplied in an improved 16-Pin plastic DIP package with heat sink contact tabs (Pins 4, 5 and 12, 13). A copper alloy lead frame allows maximum power dissipation using standard cooling techniques. The use of the contact tab lead frame facilitates attachment of a DIP heat sink while permitting the use of standard layout and mounting practices.

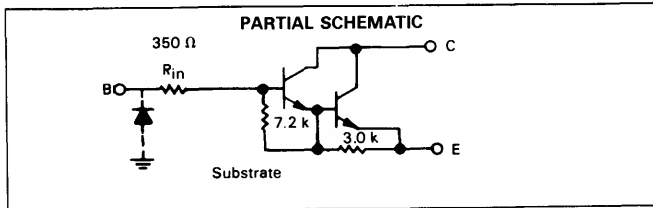
- TTL, DTL, LS, CMOS Compatible Inputs
- 1.5 Amp maximum Output Current
- Low Input Current
- 100% Inductive Load Tested
- Heat Tab Copper Alloy Lead Frame for Increased Dissipation

MAXIMUM RATINGS ($T_A = 25^{\circ}\text{C}$ and ratings apply to any one device in the package unless otherwise noted).

Rating	Symbol	Value	Unit
Output Voltage	V_O	50	V
Input Voltage (Note 1)	V_I	30	V
Collector Current (Note 2)	I_C	1.75	A
Input Current (Note 3)	I_I	25	mA
Operating Ambient Temperature Range	T_A	0 to +70	$^{\circ}\text{C}$
Storage Temperature Range	T_{stg}	-55 to +150	$^{\circ}\text{C}$
Junction Temperature	T_J	150	$^{\circ}\text{C}$

Notes:

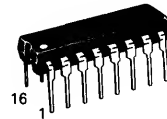
1. Input voltage referenced to ground (substrate).
2. Allowable output conditions shown in Figures 8 and 9.
3. May be limited by max input voltage.



ULN2074B

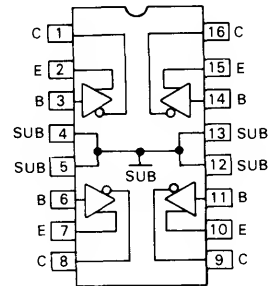
QUAD 1.5 A DARLINGTON SWITCH

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**



B SUFFIX
PLASTIC PACKAGE
CASE 648C

PIN CONNECTIONS



ORDERING INFORMATION*

Device	Temperature Range	Package
ULN2074B	0°C to +70°C	Plastic DIP

*Other options of this ULN2060 2070 series are available for volume applications. Contact your local Motorola Sales Representative.

ULN2074B

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Fig.	Symbol	Min	Typ	Max	Unit
Output Leakage Current ($V_{CE} = 50\text{ V}$) ($V_{CE} = 50\text{ V}$, $T_A = 70^\circ\text{C}$)	1	I_{CEX}	— —	— —	100 500	μA
Collector-Emitter Saturation Voltage ($I_C = 500\text{ mA}$, $I_I = 625\text{ }\mu\text{A}$) ($I_C = 750\text{ mA}$, $I_I = 935\text{ }\mu\text{A}$) ($I_C = 1.0\text{ A}$, $I_I = 1.25\text{ mA}$) ($I_C = 1.25\text{ A}$, $I_I = 2.0\text{ mA}$)	2	$V_{CE(sat)}$	— — — —	— — — —	1.13 1.25 1.40 1.60	V
Input Current — On Condition ($V_I = 2.4\text{ V}$) ($V_I = 3.75\text{ V}$)	4	$I_{I(on)}$	2.0 4.5	— —	4.3 9.6	mA
Input Voltage — On Condition ($V_{CE} = 2.0\text{ V}$, $I_C = 1.0\text{ A}$) ($V_{CE} = 2.0\text{ V}$, $I_C = 1.5\text{ A}$)	5	$V_{I(on)}$	— —	— —	2.0 2.5	V
Inductive Load Test ($V_{CC} = 24.5\text{ V}$, $t_{PW} = 4.0\text{ }\mu\text{s}$)	3	ΔV_{out}	—	—	100	mV
Turn-On Delay Time (50% E_I to 50% E_O)	—	t_{PHL}	—	—	1.0	μs
Turn-Off Delay Time (50% E_I to 50% E_O)	—	t_{PLH}	—	—	1.5	μs

TEST FIGURES

FIGURE 1

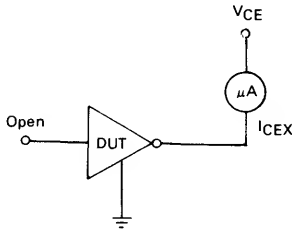


FIGURE 2

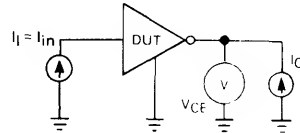


FIGURE 3

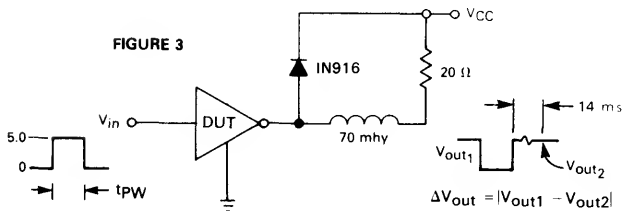


FIGURE 4

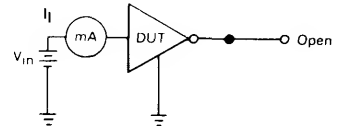
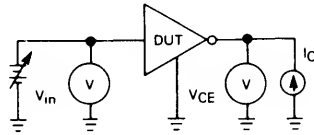


FIGURE 5



TYPICAL CHARACTERISTIC CURVES

FIGURE 6 — INPUT CURRENT versus INPUT VOLTAGE

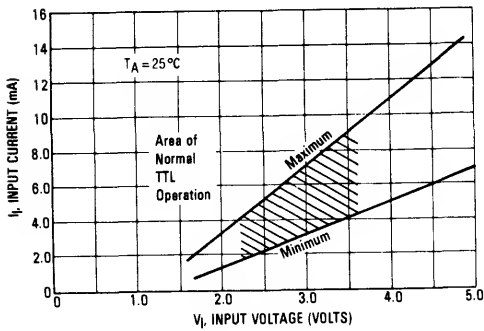


FIGURE 7 — COLLECTOR CURRENT versus INPUT CURRENT

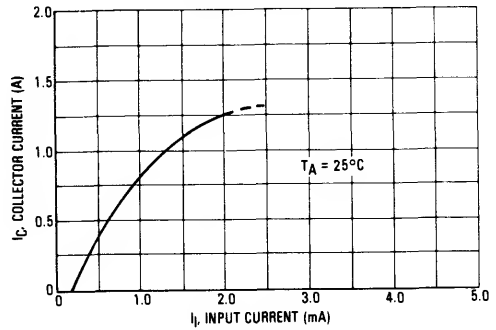


FIGURE 8 — $T_A = 70^\circ\text{C}$ w/o HEAT SINK

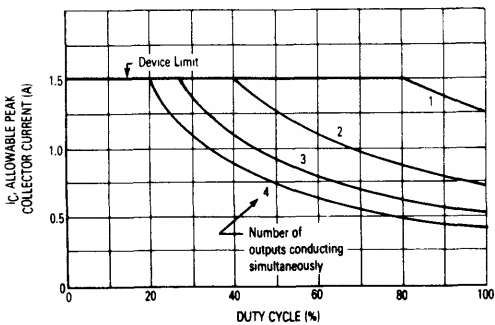


FIGURE 9 — $T_A = 70^\circ\text{C}$ w/ STAVER V-8 HEAT SINK (37.5 $^\circ\text{C/W}$)

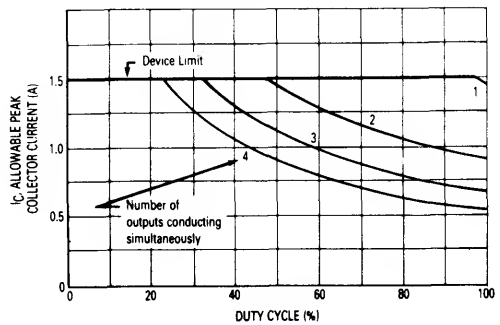


FIGURE 10 — $T_A = 70^\circ\text{C}$ w/STAVER V-7
HEAT SINK (27.5°C/W)

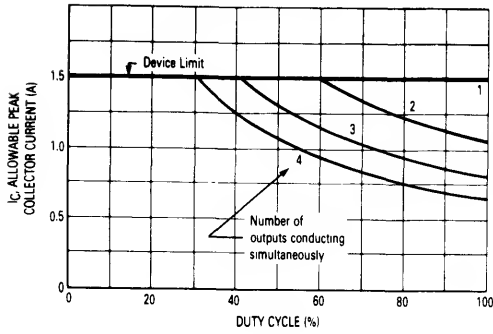


FIGURE 11 — $T_A = 50^\circ\text{C}$ w/o HEAT SINK

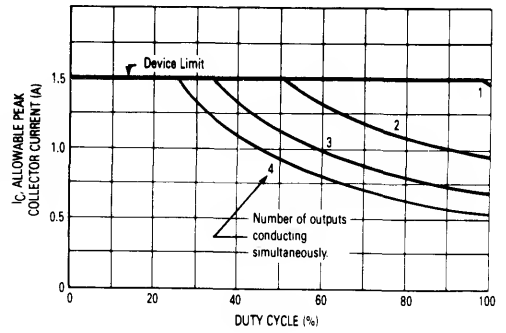


FIGURE 12 — $T_A = 50^\circ\text{C}$ w/STAVER V-8
HEAT SINK (37.5°C/W)

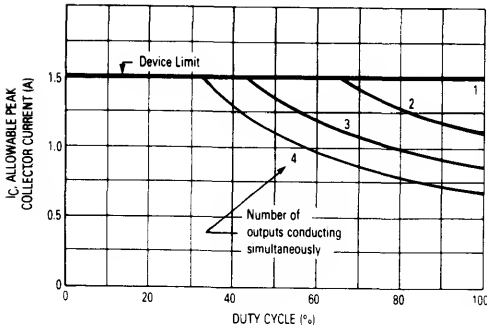
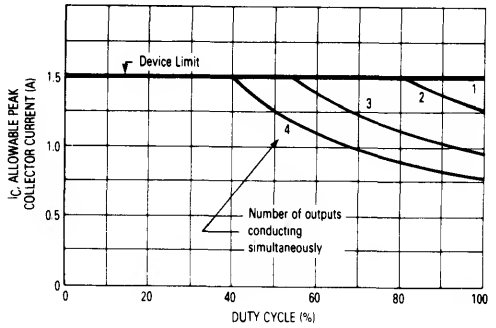


FIGURE 13 — $T_A = 50^\circ\text{C}$ w/STAVER V-7
HEAT SINK (27.5°C/W)



OCTAL HIGH VOLTAGE, HIGH CURRENT DARLINGTON TRANSISTOR ARRAYS

The eight NPN Darlington connected transistors in this family of arrays are ideally suited for interfacing between low logic level digital circuitry (such as TTL, CMOS or PMOS/NMOS) and the higher current/voltage requirements of lamps, relays, printer hammers or other similar loads for a broad range of computer, industrial, and consumer applications. All devices feature open-collector outputs and free wheeling clamp diodes for transient suppression.

The ULN2801 is a general purpose device for use with CMOS, PMOS or TTL logic. The ULN2802 contains a zener diode and resistor in series with the input to limit input currents and assure compatibility with 14 to 25 volt PMOS logic. The ULN2803 is designed to be compatible with standard TTL families while the ULN2804 is optimized for 6 to 15 volt high level CMOS or PMOS.

MAXIMUM RATINGS ($T_A = 25^{\circ}\text{C}$ and rating apply to any one device in the package unless otherwise noted.)

Rating	Symbol	Value	Unit
Output Voltage	V_O	50	V
Input Voltage (Except ULN2801)	V_I	30	V
Collector Current — Continuous	I_C	500	mA
Base Current — Continuous	I_B	25	mA
Operating Ambient Temperature Range	T_A	0 to +70	$^{\circ}\text{C}$
Storage Temperature Range	T_{stg}	-55 to +150	$^{\circ}\text{C}$
Junction Temperature	T_J	125	$^{\circ}\text{C}$

$R_{\theta JA} = 55^{\circ}\text{C/W}$
Do not exceed maximum current limit per driver.

ORDERING INFORMATION

Device	Characteristics		
	Input Compatibility	$V_{CE}(\text{Max})/I_C(\text{Max})$	T_A
ULN2801A	General Purpose CMOS, PMOS	50 V/500 mA	0 to +70 $^{\circ}\text{C}$
ULN2802A	14-25 Volt PMOS		
ULN2803A	TTL, 5.0 V CMOS		
ULN2804A	6-15 V CMOS, PMOS		

ULN2801

ULN2802

ULN2803

ULN2804

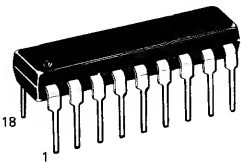
OCTAL

PERIPHERAL

DRIVER ARRAYS

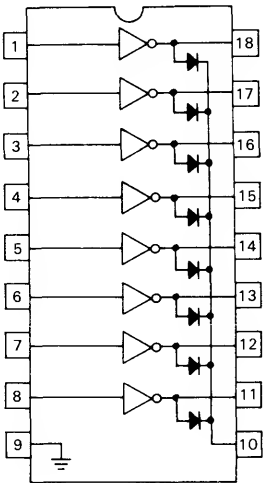
SILICON MONOLITHIC

INTEGRATED CIRCUITS



A SUFFIX
PLASTIC PACKAGE
CASE 707

PIN CONNECTIONS



ULN2801, ULN2802, ULN2803, ULN2804

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic		Fig.	Symbol	Min	Typ	Max	Unit
Output Leakage Current ($V_O = 50\text{ V}$, $T_A = +70^\circ\text{C}$) ($V_O = 50\text{ V}$, $T_A = +25^\circ\text{C}$) ($V_O = 50\text{ V}$, $T_A = +70^\circ\text{C}$, $V_I = 6.0\text{ V}$) ($V_O = 50\text{ V}$, $T_A = +70^\circ\text{C}$, $V_I = 1.0\text{ V}$)	All Types All Types ULN2802 ULN2804	1	I_{CEX}	— — — —	— — — —	100 50 500 500	μA
Collector-Emitter Saturation Voltage ($I_C = 350\text{ mA}$, $I_B = 500\text{ }\mu\text{A}$) ($I_C = 200\text{ mA}$, $I_B = 350\text{ }\mu\text{A}$) ($I_C = 100\text{ mA}$, $I_B = 250\text{ }\mu\text{A}$)	All Types All Types All Types	2	$V_{CE(sat)}$	— — —	1.1 0.95 0.85	1.6 1.3 1.1	V
Input Current — On Condition ($V_I = 17\text{ V}$) ($V_I = 3.85\text{ V}$) ($V_I = 5.0\text{ V}$) ($V_I = 12\text{ V}$)	ULN2802 ULN2803 ULN2804 ULN2804	4	$I_{I(on)}$	— — — —	0.82 0.93 0.35 1.0	1.25 1.35 0.5 1.45	mA
Input Voltage — On Condition ($V_{CE} = 2.0\text{ V}$, $I_C = 300\text{ mA}$) ($V_{CE} = 2.0\text{ V}$, $I_C = 200\text{ mA}$) ($V_{CE} = 2.0\text{ V}$, $I_C = 250\text{ mA}$) ($V_{CE} = 2.0\text{ V}$, $I_C = 300\text{ mA}$) ($V_{CE} = 2.0\text{ V}$, $I_C = 125\text{ mA}$) ($V_{CE} = 2.0\text{ V}$, $I_C = 200\text{ mA}$) ($V_{CE} = 2.0\text{ V}$, $I_C = 275\text{ mA}$) ($V_{CE} = 2.0\text{ V}$, $I_C = 350\text{ mA}$)	ULN2802 ULN2803 ULN2803 ULN2803 ULN2804 ULN2804 ULN2804 ULN2804	5	$V_{I(on)}$	— — — — — — — —	— — — — — — — —	13 2.4 2.7 3.0 5.0 6.0 7.0 8.0	V
Input Current — Off Condition ($I_C = 500\text{ }\mu\text{A}$, $T_A = +70^\circ\text{C}$)	All Types	3	$I_{I(off)}$	50	100	—	μA
DC Current Gain ($V_{CE} = 2.0\text{ V}$, $I_C = 350\text{ mA}$)	ULN2801	2	h_{FE}	1000	—	—	—
Input Capacitance			C_I	—	15	25	pF
Turn-On Delay Time (50% E_I to 50% E_O)			t_{on}	—	0.25	1.0	μs
Turn-Off Delay Time (50% E_I to 50% E_O)			t_{off}	—	0.25	1.0	μs
Clamp Diode Leakage Current ($V_R = 50\text{ V}$)	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	6	I_R	—	—	50 100	μA
Clamp Diode Forward Voltage ($I_F = 350\text{ mA}$)		7	V_F	—	1.5	2.0	V

ULN2801, ULN2802, ULN2803, ULN2804

TEST FIGURES

(SEE FIGURE NUMBERS IN ELECTRICAL CHARACTERISTICS TABLES)

FIGURE 1

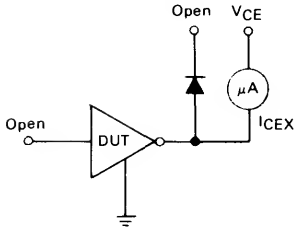


FIGURE 2

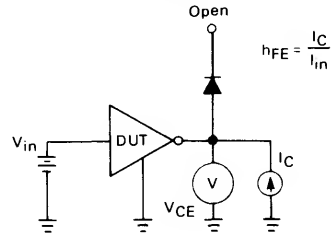


FIGURE 3

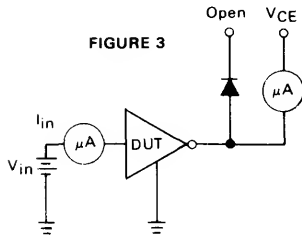


FIGURE 4

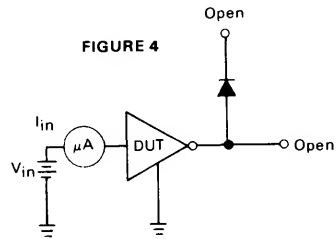


FIGURE 5

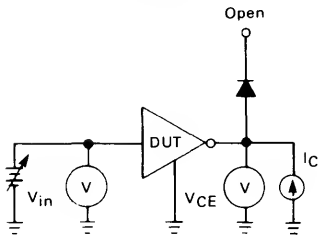


FIGURE 7

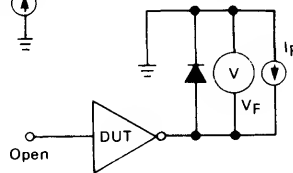
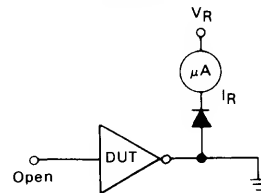


FIGURE 6



ULN2801, ULN2802, ULN2803, ULN2804

TYPICAL CHARACTERISTIC CURVES — $T_A = 25^\circ\text{C}$ (unless otherwise noted)

OUTPUT CHARACTERISTICS

FIGURE 8 — OUTPUT CURRENT versus SATURATION VOLTAGE

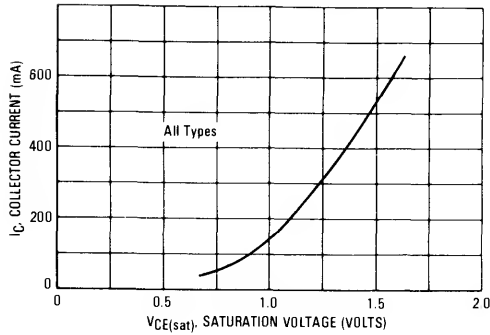
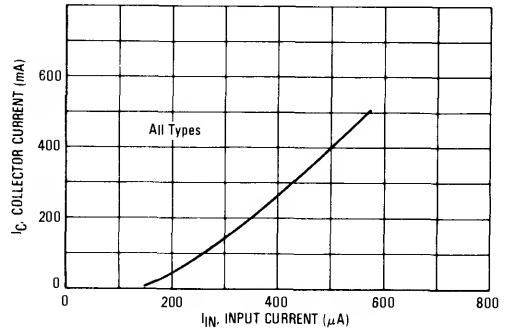


FIGURE 9 — OUTPUT CURRENT versus INPUT CURRENT



INPUT CHARACTERISTICS

FIGURE 10 — ULN2802 INPUT CURRENT versus INPUT VOLTAGE

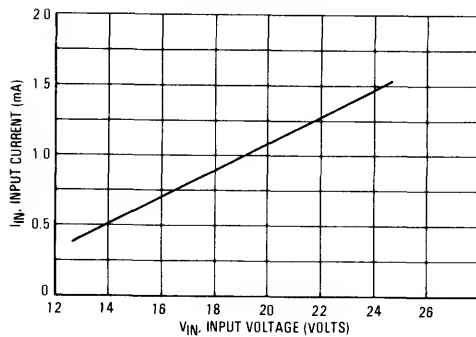


FIGURE 11 — ULN2803 INPUT CURRENT versus INPUT VOLTAGE

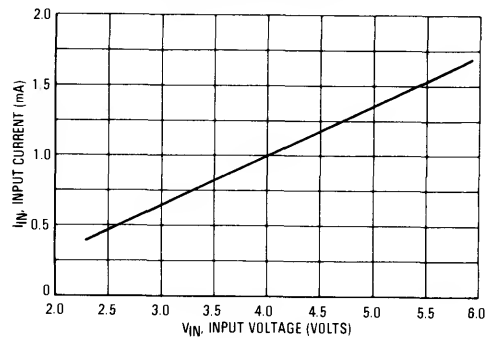
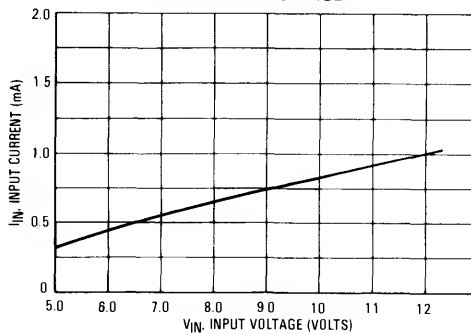
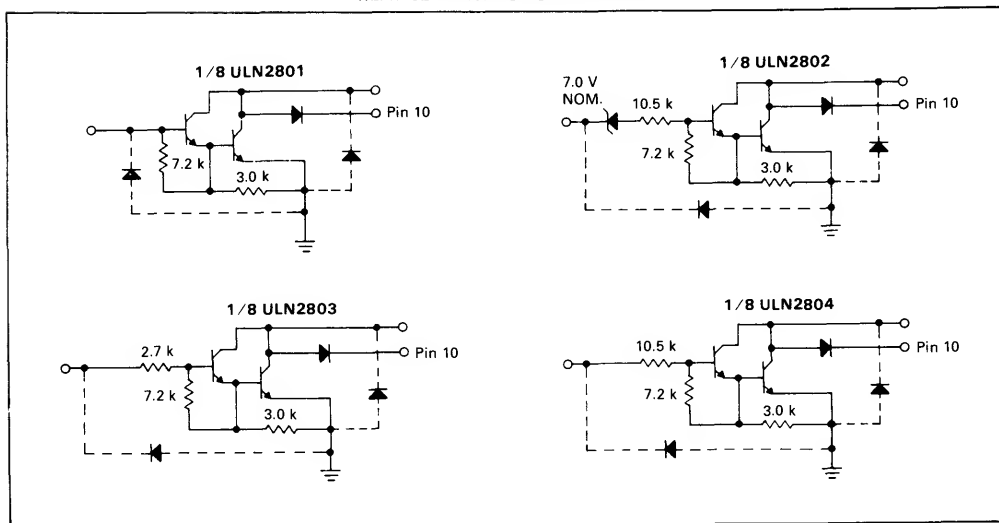


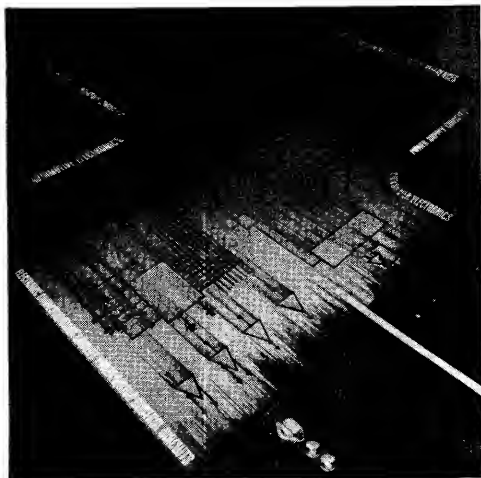
FIGURE 12 — ULN2804 INPUT CURRENT versus INPUT VOLTAGE



ULN2801, ULN2802, ULN2803, ULN2804

REPRESENTATIVE CIRCUIT SCHEMATICS





In Brief . . .

RF

Radio communication has greatly expanded its scope in the past several years. Once dominated by public safety radio, the 30 to 1000 MHz spectrum is now packed with personal and low cost business radio systems. The vast majority of this equipment uses FM or FSK modulation and is targeted at short range applications. From mobile phones and VHF marine radios to garage door openers and radio controlled toys, these new systems have become a part of our lifestyle. Motorola linear products have focused on this technology adding a wide array of new products including complete receivers processed in our exclusive 3 GHz MOSAIC 1.5 process. New surface mount packages, for high density assembly, are available for all of these products, as is a growing family of supporting applications notes and development kits.

Telephone & Voice/Data

Traditionally, an office environment has utilized two distinctly separate wired communications systems — Telecommunications and Datacommunications. Each had its individual hardware components complement and each required its own independent transmission line system: twisted wire pairs for Telecom and relatively high priced coax cable for Datacom. But times have changed. Today, Telecom and Datacom coexist comfortably on inexpensive twisted wire pairs and utilize a significant number of components in common. This has led to the development and enhancement of PBX (Private Branch Exchanges) to the point where the long heralded "office of the future," with simultaneous voice and data communications capability at each station, is no longer of the future at all. The capability is here today!

Motorola semiconductor components serve a wide range of requirements for the voice/data marketplace. They encompass both CMOS and linear technologies, each to its best advantage, and upgrade the conventional analog voice systems and establish new capabilities in digital communications. Early products, such as the solid-state single-chip crosspoint switch, the more recent monolithic Subscriber-Loop-Interface Circuit (SLIC), a single-chip Codec/Filter (Monocircuit) the latest Universal Digital Loop Transceivers (UDLT), and single-chip telephone circuits are just a few examples of Motorola leadership in the voice/data area.

Selector Guide

RF Communications	8-2
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Alphanumeric Listing	8-11
Related Application Notes	8-12
Data Sheets	8-13

Communication Circuits

Communication Circuits

RF Communications

Narrowband Dual Conversion Receivers — FM/FSK — VHF

Type	V _{CC}	I _{CC}	Sensitivity	RF Input (Max)	IF1 (Max)	IF2 (limiter in)	Mute	RSSI	Data Rate	Notes	Package	Suffix
MC3362	2–7 V	3 mA	<1 μ V	180 MHz	10.7 MHz	455 kHz	—	✓	>4.8 kb	Includes buffered VCO output	24 Pin DIP, SOIC	P/724 DW/751E
MC3363	2–7 V	4 mA	<0.5	180 MHz	10.7 MHz	455 kHz	✓	✓	>4.8 kb	Includes RF amp, mute	28 Pin SOIC	DW/751F
MC3335	2–7 V	4 mA	<0.1	180 MHz	10.7 MHz	455 kHz	✓	✓	>4.8 kb	Low cost version	20 Pin SOIC	P/738 DW/751D

Wideband Data (FM/FSK) Receiver — VHF

Type	V _{CC}	I _{CC}	Sensitivity	IF1 (Max)	IF2 (limiter in)	Mute	RSSI	Max Data Rate	Notes	Package	Suffix
MC3356	3–9 V	25 mA	30 μ V	200 MHz	10.7 MHz	✓	✓	500 Kb	Includes front end mixer/L.O.	20 Pin DIP/PLCC	P/738 FN/775

Narrowband IFs — Wideband (FM/FSK) IF

MC3357	4–8 V	5 mA	5 μ V	45 MHz	455 kHz	✓	—	—		16 Pin DIP	P/648
MC3359	4–9 V	7 mA	2 μ V	45 MHz	455 kHz	✓	—	—		18/20 Pin DIP/SOIC	P/707 DW/751D
MC3361A	2–8 V	6 mA	2 μ V	60 MHz	455 kHz	✓	—	—		16 Pin DIP/SOIC	P/648 D/751B
MC3367	1–5 V	1 mA	<1 μ V	75 MHz	455 kHz	✓	—	1.2 Kb	1 Cell Operation	28 Pin SOIC	DW/751F
MC3371	2–8 V	6 mA	2 μ V	60 MHz	455 kHz	✓	✓	—	(4Q89 Intro)	16 Pin DIP/SOIC	P/648 D/751B
MC13055	3–12 V	25 mA	20 μ V	—	40 MHz	✓	✓	2 Mb	Wideband Data IF	16 Pin DIP/SOIC	P/648 D/751B

Transmitters — FM/FSK

Type	V _{CC}	I _{CC}	P _{out}	Max RF Freq. Out	Battery Check	Tone OSC	Max Mod. Freq.	Notes	Package	Suffix
MC2831A	3–8 Vdc	5 mA	–30 dBm	50 MHz	✓	✓	50 kHz (xtal Ctl)	Includes low battery checker, tone osc.	16 Pin DIP/SOIC	P/648 D/751B
MC2833	3–8 Vdc	3 mA	–30 dBm to +10 dBm	150 MHz	—	—	50 kHz (xtal ctl)	Includes two frequency multiplier/amplifier transistors	16 Pin DIP/SOIC	P/648 D/751B

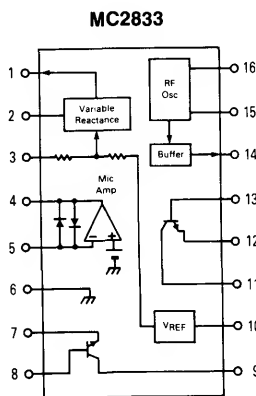
Balanced Modulator/Demodulator

Type	V _{CC}	I _{CC}	Function	Package	Case Suffix
MC1596	5-30 V	10 mA	Carrier Balance >50 dB General purpose balanced modulator/ demodulator for AM, SSB, FM Detection	10 Pin Metal	G/603
MC1496	5-30 V	10 mA		14 Pin Ceramic DIL, DIP, SOIC	L/632 P/646 D/751A

Low Power FM Transmitter System

MC2833 — $T_A = -30^\circ$ to $+75^\circ\text{C}$, Case 648, 751B

- Complete VHF FM Transmitter/Exciter
- Mike Preamp with Limiting
- Tone Generator for CTSS or AFSK
- Crystal or L-C VCO Operation
- Buffer/Multiplier Output Stage
- Two Multiplier/Amplifier Stages
- Operates to 150+ MHz



Low Voltage FM Narrowband Receiver

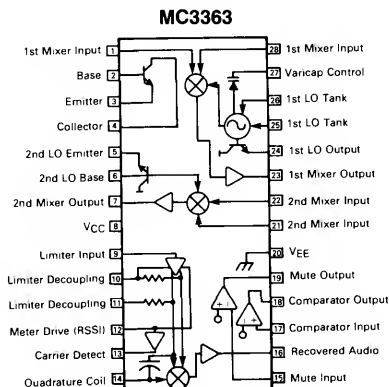
MC3367 — $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, Case 751F

- Single Cell Operation to 0.9 V_{CC}
- Single Conversion Operation to 75 MHz
- Current Drain of 1 mA
- Split I.F. Amplifier for Single or Dual Filters
- Analog and Data Outputs
- Sensitivity of 0.7 μ V Typ for 20 dB Quieting
- Low Battery Voltage Indicator

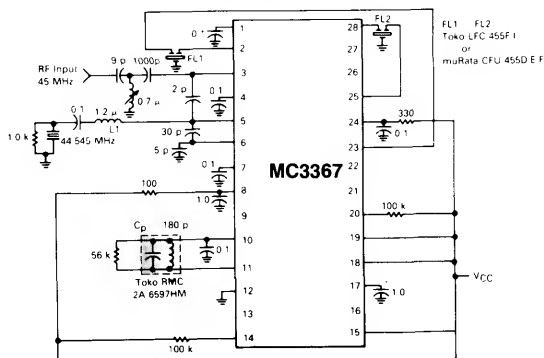
MOSAIC® 1.5 VHF Narrowband Dual-Conversion Receiver

MC3363 — $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, Case 751F

- Operation to 180 MHz
- 2–8 Vdc Supply
- <0.5 μ V for 20 dB Quieting Sensitivity
- Analog and Data Modulation Recovery
- >60 dB Dynamic Range RSSI
- Crystal or VCO First L.O. Operation
- On-Chip RF Amp/MC3363



(All capacitors in μF unless otherwise stated. Resistors in ohms. Inductors in Henries.)



TELECOMMUNICATIONS

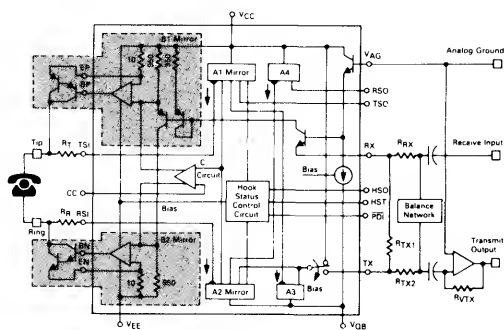
Subscriber Loop Interface Circuit (SLIC)

MC3419-1L — $T_A = 0^\circ$ to $+70^\circ\text{C}$, Case 726

The replacement of two-to-four wire conversion hybrid transformers in Central Office, PBX, and Subscriber Carrier equipment with the SLIC has resulted in major improvement in telephone equipment. The SLIC family performs this task, along with most other BORSHT functions required by signal

transmission. These include the provision of dc power to the telephone (Battery); Overvoltage protection; Ring trip detection; Supervisory features such as hook status and dial pulsing; 2-to-4 wire conversion, suppression of longitudinal signals (Hybrid).

- All Key Parameters Externally Programmable
- Current Sensing Outputs Monitor Status of Both Tip and Ring Leads
- On-Hook Power Below 5.0 mW
- Digital Hook Status Output
- Power Down Input
- Ground Fault Protection
- Size and Weight Reduction Over Conventional Approaches
- The sale of this product is licensed under patent No. 4,004,109. All royalties related to this patent are included in the unit price.



MC33120 — $T_A = -40^\circ$ to $+85^\circ\text{C}$, Case 738, 751D

With a guaranteed minimum longitudinal balance of 58 dB, the MC33120 is ideally suited for central office applications, as well as PBXs, and other related equipment. Protection and sensing components on the 2 wire side can be non-precision while achieving required system performance. Most BORSHT functions are provided while maintaining low power consumption, and a cost effective design. Size and weight reduction over conventional transformer designs permit a higher density system.

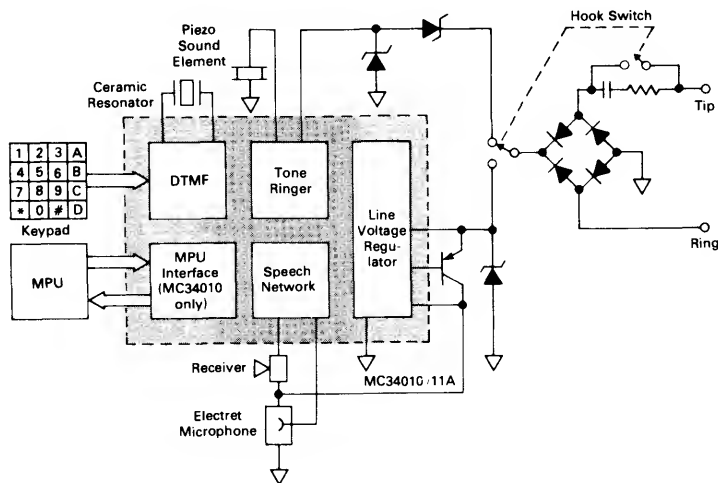
- All key parameters externally programmable with resistors:
 - Transmit and receive gains
 - Transhybrid loss

- Return loss
- DC loop current limit and battery feed resistance
- Longitudinal Impedance
- Single and double fault sensing and protection
- Minimum 58 dB longitudinal balance (2 wire and 4 wire) guaranteed
- Digital Hook Status and Fault outputs
- Power Down input
- Loop Start or ground start operation
- Size and weight reduction over conventional approaches
- Available in 20 pin DIP and SOIC packages

Electronic Telephone

The Complete Electronic Telephone Circuit

MC34010/11A — $T_A = -20^\circ$ to $+60^\circ\text{C}$, Case 711, 777



The conventional transformer-driven telephone handset is undergoing major innovations. The bulky transformer is disappearing. So are many of its discrete components, including the familiar telephone bell. They are being replaced with integrated circuits that perform all the major handset functions simply, reliably and inexpensively . . . functions such as 2-to-4 wire conversion, DTMF dialing, tone ringing, and a variety of related activities.

The culmination of these capabilities is the Electronic Telephone Circuit, the MC34010/11A. These IC's place all of the above mentioned functions on a single monolithic chip.

These telephone circuits utilize advanced bipolar linear (i^2L) technology and provide all the necessary elements of a modern tone-dialing telephone. The MC34010 even incorporates an MPU interface circuit for the inclusion of automatic dialing in the final system.

Features

- Provides All Basic Telephone Functions, Including DTMF Dialer, Tone Ringer, Speech Network and Line Voltage Regulator
- DTMF Generator Uses Low-Cost Ceramic Resonator with Accurate Frequency Synthesis Technique
- Tone Ringer Drives Piezoelectric Transducer and Satisfies EIA-470 Requirements
- Speech Network Provides Two-Four Wire Conversion with Adjustable Sidetone Utilizing an Electret Transmitter
- On-Chip Regulator Insures Stable Operation Over Wide Range of Loop Lengths
- i^2L Technology Provides Low 1.4 Volt Operation and High Static Discharge Immunity
- MC34010P Provides Microprocessor Interface Port for Automatic Dialing Features

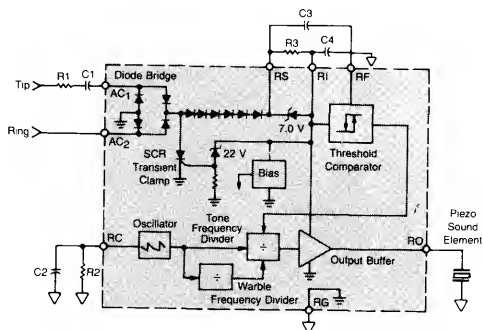
Tone Ringers

The MC34012, MC34017, and MC34117 Tone Ringers are designed to replace the bulky bell assembly of a telephone, while providing the same function and performance under a variety of conditions. The operational requirements spelled out by the FCC and EIA-470, simply stated, are that a ringer

circuit MUST function when a ringing signal is provided, and MUST NOT ring when other signals (speech, dialing, noise) are on the line. The tone ringers described below were designed to meet those requirements with a minimum of external components.

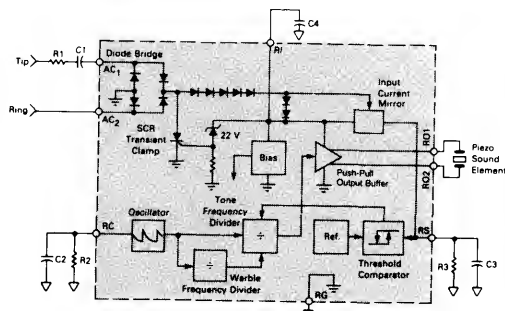
MC34012 — $T_A = -20^\circ$ to $+60^\circ\text{C}$, Case 626, 751

- Complete Telephone Bell Replacement
- On-Chip Diode Bridge and Transient Protection
- Single-Ended Output to Piezo Transducer
- Input Impedance Signature Meets Bell and EIA Standards
- Rejects Rotary Dial and Hook Switch Transients
- Adjustable Base Frequencies
- Output Frequency to Warble Ratio — MC34012-1: 80
MC34012-2: 160
MC34012-3: 40



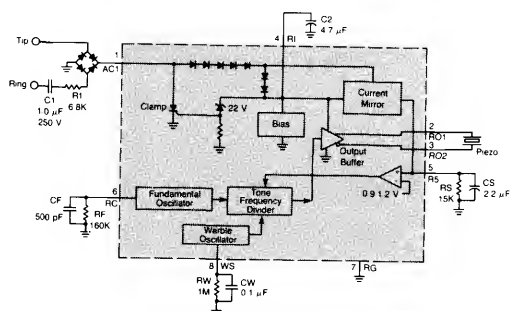
MC34017 — $T_A = -20^\circ$ to $+60^\circ\text{C}$, Case 626, 751

- Complete Telephone Bell Replacement
- On-Chip Diode Bridge and Transient Protection
- Differential Output to Piezo Transducer for Louder Sound
- Input Impedance Signature Meets Bell and EIA Standards
- Rejects Rotary Dial and Hook Switch Transients
- Output Frequency to Warble Ratio — MC34017-1: 80
MC34017-2: 160
MC34017-3: 40



MC34117 — $T_A = -20^\circ\text{C}$ to $+60^\circ\text{C}$, Case 626, 751

- Complete Telephone Bell Replacement
- External Diode Bridge
- Internal Transient Protection
- Differential Output to Piezo Transducer for Louder Sound
- Input Impedance Signature Meets Bell and EIA Standards
- Rejects Rotary Dial and Hook Switch Transients
- Base Frequency and Warble Frequencies are Independently Adjustable

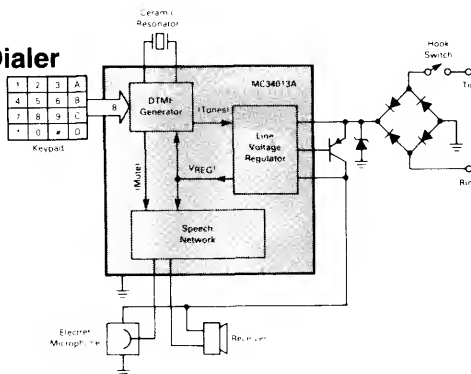


Speech Networks

Telephone Speech Network and Tone Dialer

MC34013A — $T_A = -20^\circ$ to $+60^\circ\text{C}$, Case 710, 776

- Linear/ $i2L$ Technology Provides Low 1.4 Volt Operation in Both Speech and Dialing Modes
- Speech Network Provides 2-4 Wire Conversion with Adjustable Sidetone Utilizing an Electret Microphone
- DTMF Generator Uses Low-Cost Ceramic Resonator with Accurate Frequency Synthesis Technique
- On-Chip Regulator Insures Stable Operation Over Wide Range of Loop Lengths
- Dialer Mutes Speech Network with Internal Delay for Click Suppression on DTMF Key Release

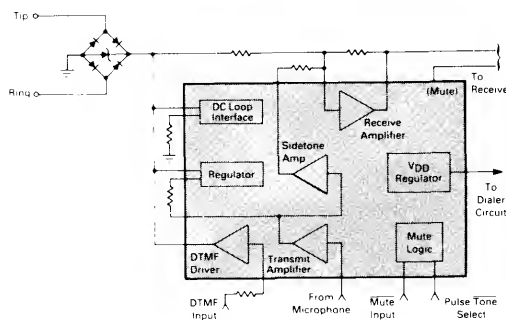


Speech Network with Dialer Interface

MC34014 — $T_A = -20^\circ$ to $+60^\circ\text{C}$, Case 707, 775

The MC34014 is a Telephone Speech Network integrated circuit which incorporates adjustable transmit, receive, and sidetone functions, line interface circuit, dialer interface, and a regulated output voltage for a dialer circuit. It includes an equalization circuit to compensate for various line lengths and the conversion from 2-to-4 wire is accomplished with supply voltages as low as 1.5 volts.

- Transmit, Receive, and Sidetone Gains Set By External Resistors
- Loop Length Equalization for Transmit, Receive, and Sidetone Functions
- Operates Down to 1.5 Volts (V_+) in Speech Mode
- Provides Regulated Voltage for CMOS Dialer
- Speech Amplifiers Muted During Pulse and Tone Dialing
- DTMF Output Level Adjustable with a Single Resistor
- Compatible with 2-Terminal Electret Microphones
- Compatible with Receiver Impedances of 150 Ω and Higher

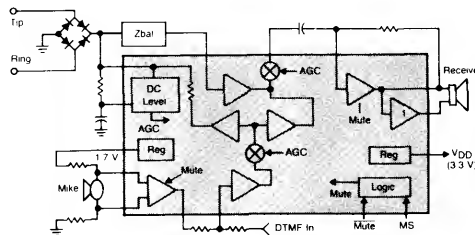


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Telephone Speech Network with Dialer Interface

MC34114, MC34214 — $T_A = -20^\circ$ to $+70^\circ\text{C}$, Case 707, 751D

- Operation Down to 1.2 Volts
- Adjustable Transmit, Receive, and Sidetone Gains by External Resistors
- Differential Microphone Amplifier Input Minimizes RFI
- Transmit, Receive, and Sidetone Equalization on both Voice and DTMF Signals
- Regulated 1.7 Volts Output for Biasing Microphone
- Regulated 3.3 Volts Output for Powering External Dialer
- Microphone and Receive Amplifiers Muted During Dialing
- Differential Receive Amplifier Output Eliminates Coupling Capacitor
- Operates with Receiver Impedances of 150 Ω and Higher

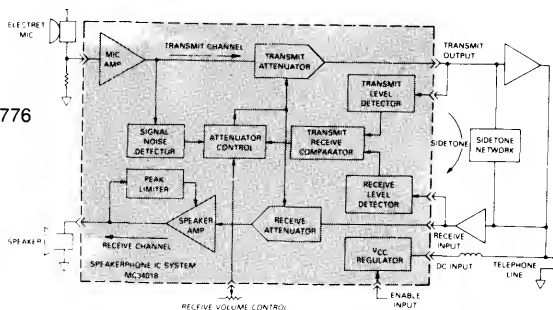


Speakerphone

Voice Switched Speakerphone Circuit

MC34018 — $T_A = -20^\circ$ to $+60^\circ\text{C}$, Case 710, 776

The MC34018 Speakerphone integrated circuit incorporates the necessary amplifiers, attenuators, and control functions to produce a high quality hands-free speakerphone system. Included are a microphone amplifier, a power audio amplifier for the speaker, transmit and receive attenuators, a monitoring system for background sound level, and an attenuation control system which responds to the relative transmit and receive levels as well as the background level. Also included are all necessary regulated voltages for both internal and external circuitry, allowing line-powered operation (no additional power supplies required). A Chip Select pin allows the chip to be powered down when not in use. A volume control function may be implemented with an external potentiometer. MC34018 applications include speakerphones for household and business use, intercom systems, automotive telephones, and others.



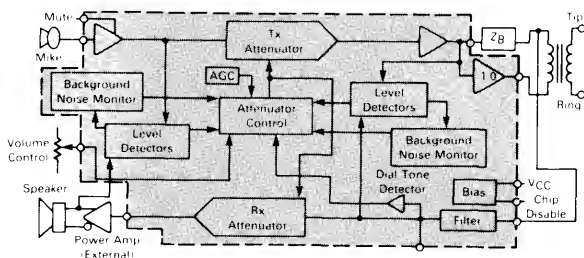
- All Necessary Level Detection and Attenuation Controls for a Hands-Free Telephone in a Single Integrated Circuit
- Background Noise Level Monitoring with Long Time Constant
- Wide Operating Dynamic Range Through Signal Compression
- On-chip Supply and Reference Voltage Regulation
- Typical 100 mW Output Power (into 25 Ω) with Peak Limiting to Minimize Distortion
- Chip Select Pin for Active/Standby Operation
- Linear Volume Control Function

Voice Switched Speakerphone Circuit

MC34118 — $T_A = -20^\circ$ to $+60^\circ\text{C}$, Case 710, 751F

The MC34118 Voice Switched Speakerphone Circuit incorporates the necessary amplifiers, attenuators, level detectors, and control algorithm to form the heart of a high quality hands-free speakerphone system. Included are a microphone amplifier with adjustable gain and MUTE control, Transmit and Receive attenuators which operate in a complementary manner, level detectors at both input and output of both attenuators, and background noise monitors for both the transmit and receive channels. A Dial Tone Detector prevents the dial tone from being attenuated by the Receive background noise monitor circuit. Also included are two line driver amplifiers which can be used to form a hybrid network in conjunction with an external coupling transformer. A high-pass filter can be used to filter out 60 Hz noise in the receive channel, or for other filtering functions. A Chip Disable pin permits powering down the entire circuit to conserve power on long loops where loop current is at a minimum.

The MC34118 may be operated from a power supply, or it can be powered from the telephone line, requiring typically 5.0 mA. The MC34118 can be interfaced directly to Tip and Ring (through a coupling transformer) for stand-alone operation, or it can be used in conjunction with a handset speech network and/or other features of a featurephone.



- Improved Attenuator Gain Range: 52 dB Between Transmit and Receive
- Low Voltage Operation for Line-Powered Applications (3.0–6.5 V)
- 4-Point Signal Sensing for Improved Sensitivity
- Background Noise Monitors for Both Transmit and Receive Paths
- Microphone Amplifier Gain Set by External Resistors — Mute Function Included
- Chip Disable for Active/Standby Operation
- On Board Filter Pinned-Out for User Defined Function
- Dial Tone Detector to Inhibit Receive Idle Mode During Dial Tone Presence
- Compatible with MC34119 Speaker Amplifier

Continuously Variable Slope Delta (CVSD) Modulator/Demodulator

Provides the A/D-D/A function of voice communications by digital transmission.

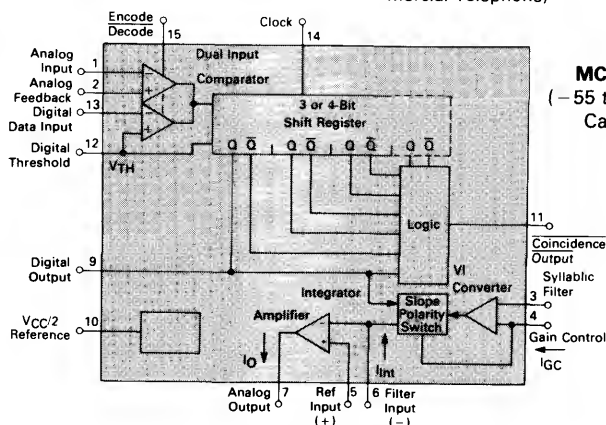
The MC3517/18 series of CVSDs is designed for military secure communications and commercial telephone applications. A single IC provides both encoding and decoding functions in 16-pin package.

- Encode and Decode functions on the Same Chip with a Digital Input for Selection
- CMOS Compatible Digital Output
- Digital Input Threshold Selectable ($V_{CC}/2$ reference provided on chip)
- MC3417/MC3517/MC34115 has a 3-Bit Algorithm (General Communications)
- MC3418/MC3518 has a 4-Bit Algorithm (Commercial Telephone)

MC3417/18
(0 to 70°C)
Case 620

MC34115
(0 to 70°C)
Case 648

MC3517/18
(-55 to +125°C)
Case 620



COMMUNICATION CIRCUITS

RF Communications

Device	Function	Page
MC1496	Balanced Modulator/Demodulator	8-13
MC1596	Balanced Modulator/Demodulator	8-13
MC2830	Voice Activated Switch	8-23
MC2831A	Low Power FM Transmitter System	8-27
MC2833	Low Power FM Transmitter System	8-30
MC3335	Low Power Dual Conversion FM Receiver	8-36
MC3356	Wideband FSK Receiver	8-40
MC3357	Low Power FM IF	8-46
MC3359	Low Power Narrowband FM IF	8-50
MC3361B	Low Voltage Narrowband FM IF	8-56
MC3362	Low Power Dual Conversion FM Receiver	8-58
MC3363	Low Power Dual Conversion FM Receiver	8-65
MC3367	Low Voltage FM Narrowband Receiver	8-73
MC13041	AM Receiver Subsystem.....	See Chapter 9
MC13055	Wideband FSK Receiver	8-82

Telecommunications

Device	Function	Page
MC3417	Continuously Variable Slope Delta Modulator/Demodulator	*
MC3418	Continuously Variable Slope Delta Modulator/Demodulator	*
MC3419-1L	Telephone Line-Feed Circuit	*
MC3517	Continuously Variable Slope Delta Modulator/Demodulator	*
MC3518	Continuously Variable Slope Delta Modulator/Demodulator	*
MC33120	Subscriber Loop Interface Circuit	*
MC33129	High Performance Current Mode Controller	See Chapter 3, *
MC34010	Electronic Telephone Circuit	*
MC34011A	Electronic Telephone Circuit	*
MC34012-1,-2,-3	Telephone Tone Ringer	*
MC34013A	Speech Network and Tone Ringer	*
MC34014	Telephone Speech Network with Dialer Interface	*
MC34017	Telephone Tone Ringer	*
MC34018	Voice Switched Speakerphone Circuit	*
MC34114	Telephone Speech Network with Dialer Interface	*
MC34115	Continuously Variable Slope Delta Modulator/Demodulator	*
MC34117	Telephone Tone Ringer	*
MC34118	Voice Switched Speakerphone Circuit	*
MC34119	Low Power Audio Amplifier.....	See Chapter 9
MC34129	High Performance Current Mode Controller	See Chapter 3, *

*See Telecommunications Device Data (DL136)

RELATED APPLICATION NOTES

Application Note	Title	Related Device
AN531	MC1596 Balanced Modulator	MC1596
AN933	A Variety of Uses for the MC34012/MC34017 Tone Ringers	MC34012-1,-2,-3, MC34017
AN937	A Telephone Ringer which Complies with FCC and EIA Impedance Standards	MC34012, MC34017
AN957	Interfacing the Speakerphone to the MC34010/11/13 Speech Networks	MC34010, MC34011A, MC34013A
AN958	Transmit Gain Adjustments for the MC34014 Speech Network	MC34014
AN959	A Speakerphone with Receive Idle Mode	MC34018
AN960	Equalization of DTMF Signals Using the MC34014	MC34014
AN976	A New High Performance Current Mode Controller Teams Up with Current Sensing Power MOSFETs	MC34129
AN980	Low Power FM Dual Conversion Receivers	MC3362, MC3363
AN1002	A Handsfree Featurephone Design Using the MC34114 Speech Network and the MC34018 Speakerphone ICs	MC34018 MC34114
AN1003	A Featurephone Design, with Tone Ringer and Dialer, Using the MC34118 Speakerphone IC	MC34118, MC34017, MC145412, MC34119
AN1004	A Handsfree Featurephone Design Using the MC34114 Speech Network and the MC34118 Speakerphone ICs	MC34114, MC34118, MC34119, MC3417, MC145412
AN1006	Linearize the Volume Control of the MC34118 Speakerphone	MC34118
AN1077	Adding Digital Volume Control to Speakerphone Circuits ...	MC34018, MC34118
AN1081	Minimize the "Pop" in the MC34119 Power Audio Amplifiers	MC34119
ANHK07	A High Performance, Manual-Tuned AM Stereo Receiver for Automotive Application Using Motorola ICs: MC13021, MC13020 & MC13041	MC13041
SG98R4	Linear Telecom Cross Reference	

BALANCED MODULATOR/ DEMODULATOR

... designed for use where the output voltage is a product of an input voltage (signal) and a switching function (carrier). Typical applications include suppressed carrier and amplitude modulation, synchronous detection, FM detection, phase detection, and chopper applications. See Motorola Application Note AN-531 for additional design information.

- Excellent Carrier Suppression — 65 dB typ @ 0.5 MHz
 — 50 dB typ @ 10 MHz
- Adjustable Gain and Signal Handling
- Balanced Inputs and Outputs
- High Common Mode Rejection — 85 dB typ

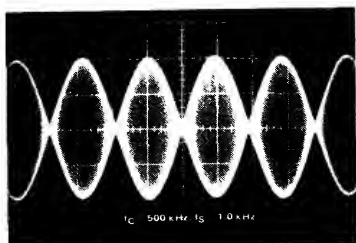


FIGURE 1 —
 SUPPRESSED CARRIER
 OUTPUT WAVEFORM

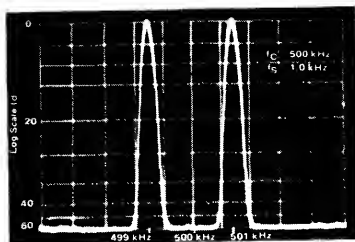


FIGURE 2 —
 SUPPRESSED CARRIER
 SPECTRUM

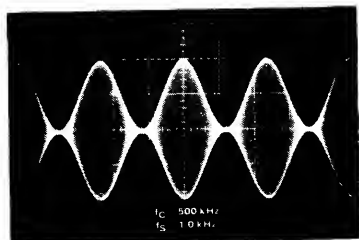
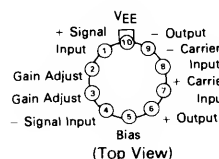
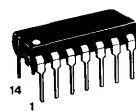


FIGURE 3 —
 AMPLITUDE MODULATION
 OUTPUT WAVEFORM

MC1496
MC1596

BALANCED MODULATOR/DEMODULATOR

G SUFFIX
 METAL PACKAGE
 CASE 603

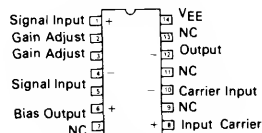


L SUFFIX
 CERAMIC PACKAGE
 CASE 632

D SUFFIX
 PLASTIC PACKAGE
 CASE 751A
 (SO-14)

P SUFFIX
 PLASTIC PACKAGE
 CASE 646

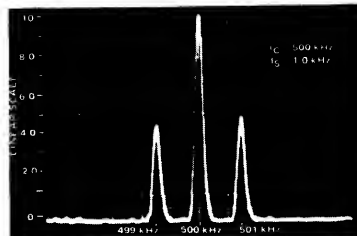
PIN ASSIGNMENTS



ORDERING INFORMATION

Device	Temperature Range	Package
MC1496D	0°C to +70°C	SO-14
MC1496G		Metal Can
MC1496L		Ceramic DIP
MC1496P		Plastic DIP
MC1596G	55°C to +125°C	Metal Can
MC1596L		Ceramic DIP

FIGURE 4 — AMPLITUDE-MODULATION SPECTRUM



MC1496, MC1596

MAXIMUM RATINGS* (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Applied Voltage (V ₆ - V ₇ , V ₈ - V ₁ , V ₉ - V ₇ , V ₉ - V ₈ , V ₇ - V ₄ , V ₇ - V ₁ , V ₈ - V ₄ , V ₆ - V ₈ , V ₂ - V ₅ , V ₃ - V ₅)	ΔV	30	Vdc
Differential Input Signal	V ₇ - V ₈ V ₄ - V ₁	+5.0 ± (5 + I ₅ R _e)	Vdc
Maximum Bias Current	I ₅	10	mA
Thermal Resistance, Junction to Air Ceramic Dual In-Line Package Plastic Dual In-Line Package Metal Package	R _{θJA}	100 100 160	°C/W
Operating Temperature Range MC1496 MC1596	T _A	0 to +70 -55 to +125	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS* (V_{CC} = +12 Vdc, V_{EE} = -8.0 Vdc, I₅ = 1.0 mAdc, R_L = 3.9 kΩ, R_e = 1.0 kΩ, T_A = +25°C, all input and output characteristics are single-ended, unless otherwise noted.)

Characteristic	Fig.	Note	Symbol	MC1596			MC1496			Unit
				Min	Typ	Max	Min	Typ	Max	
Carrier Feedthrough V _C = 60 mV(rms) sine wave and offset adjusted to zero V _C = 300 mVp-p square wave: offset adjusted to zero offset not adjusted	5	1	V _{CFT}	—	40 140	—	—	40 140	—	μV(rms) mV(rms)
Carrier Suppression f _S = 10 kHz, 300 mV(rms) f _C = 500 kHz, 60 mV(rms) sine wave f _C = 10 MHz, 60 mV(rms) sine wave	5	2	V _{CS}	—	—	—	—	—	—	dB
Transmittance Bandwidth (Magnitude) (R _L = 50 ohms) Carrier Input Port, V _C = 60 mV(rms) sine wave f _S = 1.0 kHz, 300 mV(rms) sine wave Signal Input Port, V _S = 300 mV(rms) sine wave V _C = 0.5 Vdc	8	8	BW _{3dB}	—	300	—	—	300	—	MHz
Signal Gain V _S = 100 mV(rms), f = 1.0 kHz; V _C = 0.5 Vdc	10	3	A _{VS}	2.5	3.5	—	2.5	3.5	—	V/V
Single-Ended Input Impedance, Signal Port, f = 5.0 MHz Parallel Input Resistance Parallel Input Capacitance	6	—	r _{ip} c _{ip}	—	200 2.0	—	—	200 2.0	—	kΩ pF
Single-Ended Output Impedance, f = 10 MHz Parallel Output Resistance Parallel Output Capacitance	6	—	r _{op} c _{oo}	—	40 5.0	—	—	40 5.0	—	kΩ pF
Input Bias Current I _{bS} = $\frac{I_1 + I_4}{2}$; I _{bC} = $\frac{I_7 + I_8}{2}$	7	—	I _{bS} I _{bC}	—	12 12	25 25	—	12 12	30 30	μA
Input Offset Current I _{ioS} = I ₁ - I ₄ ; I _{ioC} = I ₇ - I ₈	7	—	I _{ioS} I _{ioC}	—	0.7 0.7	5.0 5.0	—	0.7 0.7	7.0 7.0	μA
Average Temperature Coefficient of Input Offset Current (T _A = -55°C to +125°C)	7	—	TC _{Iio}	—	2.0	—	—	2.0	—	nA/°C
Output Offset Current (I ₆ - I ₉)	7	—	I _{oo}	—	14	50	—	14	80	μA
Average Temperature Coefficient of Output Offset Current (T _A = -55°C to +125°C)	7	—	TC _{Ioo}	—	90	—	—	90	—	nA/°C
Common-Mode Input Swing, Signal Port, f _S = 1.0 kHz	9	4	CMV	—	5.0	—	—	5.0	—	Vp-p
Common-Mode Gain, Signal Port, f _S = 1.0 kHz, V _C = 0.5 Vdc	9	—	ACM	—	-85	—	—	-85	—	dB
Common-Mode Quiescent Output Voltage (Pin 6 or Pin 9)	10	—	V _{out}	—	8.0	—	—	8.0	—	Vp-p
Differential Output Voltage Swing Capability	10	—	V _{out}	—	8.0	—	—	8.0	—	Vp-p
Power Supply Current I ₆ + I ₉ I ₁₀	7	6	I _{CC} I _{EE}	—	2.0 3.0	3.0 4.0	—	2.0 3.0	4.0 5.0	mAdc
DC Power Dissipation	7	5	P _D	—	33	—	—	33	—	mW

* Pin number references pertain to this device when packaged in a metal can.
To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

MC1496, MC1596

GENERAL OPERATING INFORMATION *

Carrier Feedthrough

Carrier feedthrough is defined as the output voltage at carrier frequency with only the carrier applied (signal voltage = 0).

Carrier null is achieved by balancing the currents in the differential amplifier by means of a bias trim potentiometer (R_1 of Figure 5).

Carrier Suppression

Carrier suppression is defined as the ratio of each sideband output to carrier output for the carrier and signal voltage levels specified.

Carrier suppression is very dependent on carrier input level, as shown in Figure 22. A low value of the carrier does not fully switch the upper switching devices, and results in lower signal gain, hence lower carrier suppression. A higher than optimum carrier level results in unnecessary device and circuit carrier feedthrough, which again degenerates the suppression figure. The MC1596 has been characterized with a 60 mV(rms) sinewave carrier input signal. This level provides optimum carrier suppression at carrier frequencies in the vicinity of 500 kHz, and is generally recommended for balanced modulator applications.

Carrier feedthrough is independent of signal level, V_S . Thus carrier suppression can be maximized by operating with large signal levels. However, a linear operating mode must be maintained in the signal-input transistor pair — or harmonics of the modulating signal will be generated and appear in the device output as spurious sidebands of the suppressed carrier. This requirement places an upper limit on input-signal amplitude (see Figure 20). Note also that an optimum carrier level is recommended in Figure 22 for good carrier suppression and minimum spurious sideband generation.

At higher frequencies circuit layout is very important in order to minimize carrier feedthrough. Shielding may be necessary in order to prevent capacitive coupling between the carrier input leads and the output leads.

Signal Gain and Maximum Input Level

Signal gain (single-ended) at low frequencies is defined as the voltage gain,

$$A_{VS} = \frac{V_O}{V_S} = \frac{R_L}{R_E + 2r_e} \text{ where } r_e = \frac{26 \text{ mV}}{I_5 \text{ (mA)}}$$

A constant dc potential is applied to the carrier input terminals to fully switch two of the upper transistors "on" and two transistors "off" ($V_C = 0.5 \text{ Vdc}$). This in effect forms a cascode differential amplifier.

Linear operation requires that the signal input be below a critical value determined by R_E and the bias current I_5 .

$$V_S \leq I_5 R_E \text{ (Volts peak)}$$

Note that in the test circuit of Figure 10, V_S corresponds to a maximum value of 1 volt peak.

Common Mode Swing

The common-mode swing is the voltage which may be applied to both bases of the signal differential amplifier, without saturating the current sources or without saturating the differential amplifier itself by swinging it into the upper switching devices. This swing is variable depending on the particular circuit and biasing conditions chosen.

Power Dissipation

Power dissipation, P_D , within the integrated circuit package should be calculated as the summation of the voltage-current products at each port, i.e. assuming $V_g = V_6$, $I_5 = I_6 = I_9$ and ignoring base current, $P_D = 2 I_5 (V_6 - V_{10}) + I_5 (V_5 - V_{10})$ where subscripts refer to pin numbers.

Design Equations

The following is a partial list of design equations needed to operate the circuit with other supply voltages and input conditions.

A. Operating Current

The internal bias currents are set by the conditions at pin 5. Assume:

$$I_5 = I_6 = I_9$$

$$I_B \ll I_C \text{ for all transistors}$$

then:

$$R_5 = \frac{V - \phi}{I_5} - 500 \Omega \quad \text{where: } R_5 \text{ is the resistor between pin 5 and ground}$$

$$\phi = 0.75 \text{ V at } T_A = +25^\circ\text{C}$$

The MC1596 has been characterized for the condition $I_5 = 1.0 \text{ mA}$ and is the generally recommended value.

B. Common-Mode Quiescent Output Voltage

$$V_6 = V_9 = V^+ - I_5 R_L$$

Biasing

The MC1596 requires three dc bias voltage levels which must be set externally. Guidelines for setting up these three levels include maintaining at least 2 volts collector-base bias on all transistors while not exceeding the voltages given in the absolute maximum rating table;

$$30 \text{ Vdc} \geq [(V_6, V_9) - (V_7, V_8)] \geq 2 \text{ Vdc}$$

$$30 \text{ Vdc} \geq [(V_7, V_8) - (V_1, V_4)] \geq 2.7 \text{ Vdc}$$

$$30 \text{ Vdc} \geq [(V_1, V_4) - (V_5)] \geq 2.7 \text{ Vdc}$$

The foregoing conditions are based on the following approximations:

$$V_6 = V_9, V_7 = V_8, V_1 = V_4$$

Bias currents flowing into pins 1, 4, 7, and 8 are transistor base currents and can normally be neglected if external bias dividers are designed to carry 1.0 mA or more.

Transadmittance Bandwidth

Carrier transadmittance bandwidth is the 3 dB bandwidth of the device forward transadmittance as defined by:

$$\gamma_{21C} = \frac{i_o \text{ (each sideband)}}{v_s \text{ (signal)}} \Big|_{V_O = 0}$$

Signal transadmittance bandwidth is the 3 dB bandwidth of the device forward transadmittance as defined by:

$$\gamma_{21S} = \frac{i_o \text{ (signal)}}{v_s \text{ (signal)}} \Big|_{V_C = 0.5 \text{ Vdc}, V_O = 0}$$

*Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

MC1496, MC1596

Coupling and Bypass Capacitors C_1 and C_2

Capacitors C_1 and C_2 (Figure 5) should be selected for a reactance of less than 5.0 ohms at the carrier frequency.

Output Signal, V_o

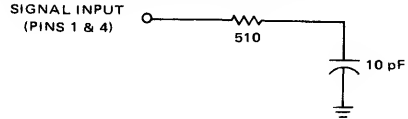
The output signal is taken from pins 6 and 9, either balanced or single-ended. Figure 12 shows the output levels of each of the two output sidebands resulting from variations in both the carrier and modulating signal inputs with a single-ended output connection.

Negative Supply, V_{EE}

V_{EE} should be dc only. The insertion of an RF choke in series with V_{EE} can enhance the stability of the internal current sources.

Signal Port Stability

Under certain values of driving source impedance, oscillation may occur. In this event, an RC suppression network should be connected directly to each input using short leads. This will reduce the Q of the source-tuned circuits that cause the oscillation.



An alternate method for low-frequency applications is to insert a 1 kOhm resistor in series with the inputs, pins 1 and 4. In this case input current drift may cause serious degradation of carrier suppression.

TEST CIRCUITS*

*Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

FIGURE 5 – CARRIER REJECTION AND SUPPRESSION

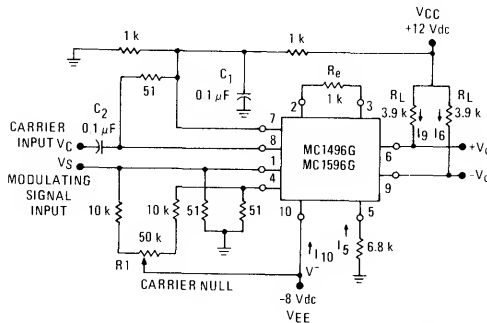
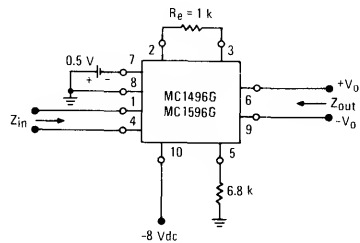


FIGURE 6 – INPUT-OUTPUT IMPEDANCE



NOTE: Shielding of input and output leads may be needed to properly perform these tests.

FIGURE 7 – BIAS AND OFFSET CURRENTS

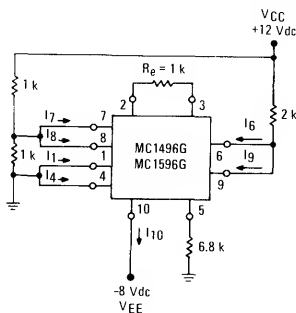
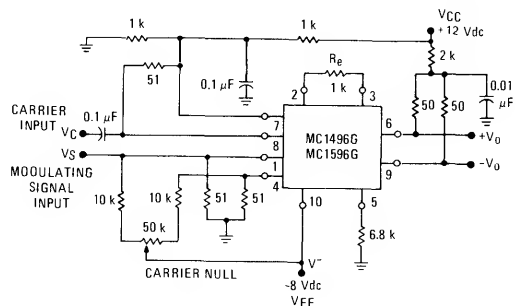


FIGURE 8 – TRANSCONDUCTANCE BANDWIDTH



MC1496, MC1596

TEST CIRCUITS (continued)

FIGURE 9 – COMMON MODE GAIN

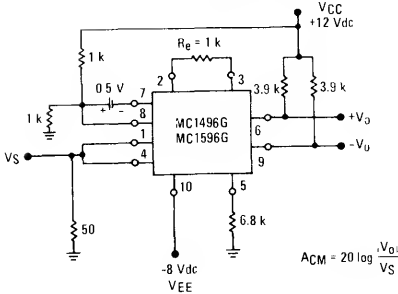
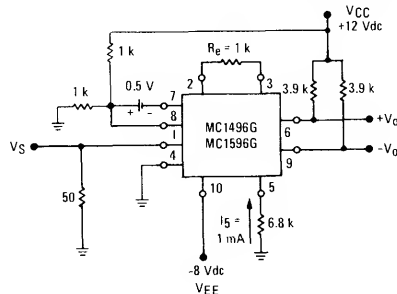


FIGURE 10 – SIGNAL GAIN AND OUTPUT SWING



TYPICAL CHARACTERISTICS

Typical characteristics were obtained with circuit shown in Figure 5, $f_C = 500 \text{ kHz}$ (sine wave), $V_C = 60 \text{ mV(rms)}$, $f_S = 1 \text{ kHz}$, $V_S = 300 \text{ mV(rms)}$, $T_A = +25^\circ\text{C}$ unless otherwise noted.

FIGURE 11 – SIDEBAND OUTPUT versus CARRIER LEVELS

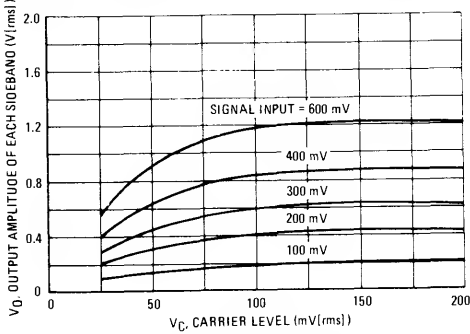


FIGURE 12 – SIGNAL-PORT PARALLEL-EQUIVALENT INPUT RESISTANCE versus FREQUENCY

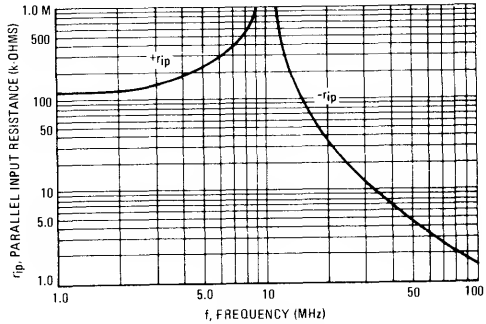


FIGURE 13 – SIGNAL-PORT PARALLEL-EQUIVALENT INPUT CAPACITANCE versus FREQUENCY

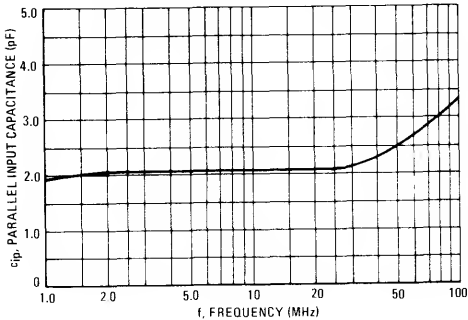
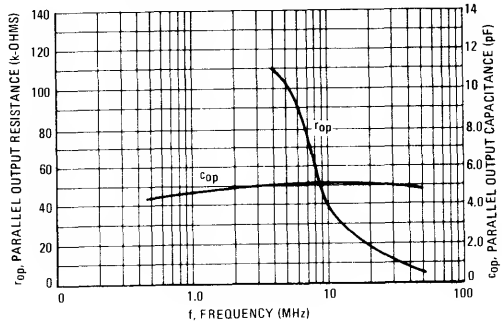


FIGURE 14 – SINGLE-ENDED OUTPUT IMPEDANCE versus FREQUENCY



TYPICAL CHARACTERISTICS (continued)

Typical characteristics were obtained with circuit shown in Figure 5, $f_C = 500$ kHz (sine wave),
 $V_C = 60$ mV(rms), $f_S = 1$ kHz, $V_S = 300$ mV(rms), $T_A = +25^\circ\text{C}$ unless otherwise noted.

FIGURE 15 — SIDE BAND AND SIGNAL PORT TRANSADMITTANCES versus FREQUENCY

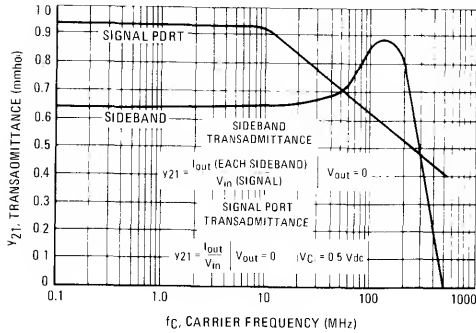


FIGURE 16 — CARRIER SUPPRESSION versus TEMPERATURE

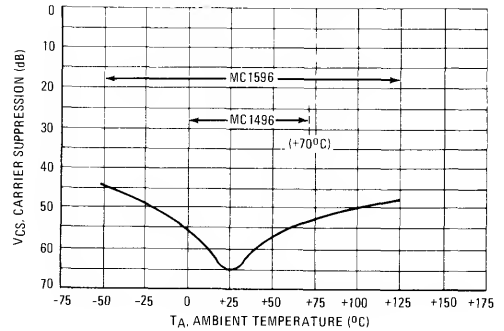


FIGURE 17 — SIGNAL-PORT FREQUENCY RESPONSE

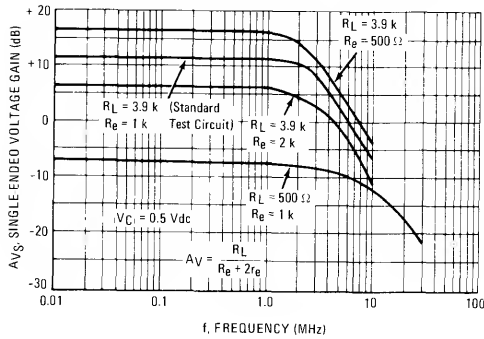


FIGURE 18 — CARRIER SUPPRESSION versus FREQUENCY

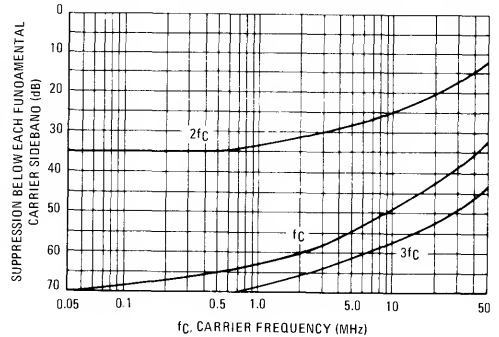


FIGURE 19 — CARRIER FEEDTHROUGH versus FREQUENCY

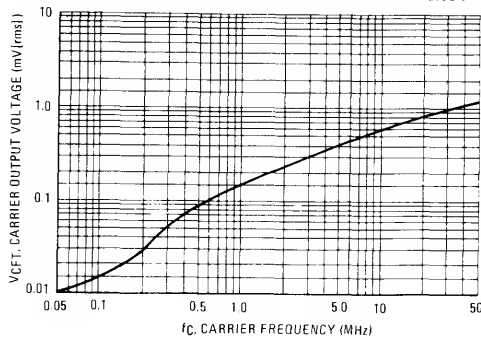
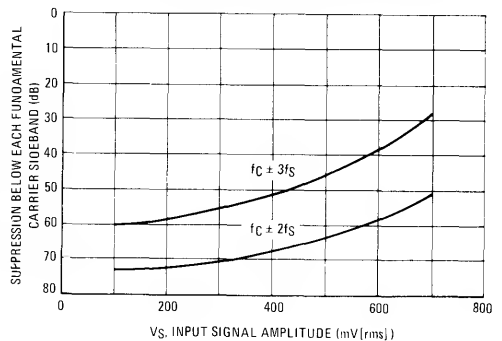


FIGURE 20 — SIDE BAND HARMONIC SUPPRESSION versus INPUT SIGNAL LEVEL



MC1496, MC1596

TYPICAL CHARACTERISTICS (continued)

FIGURE 21 – SUPPRESSION OF CARRIER HARMONIC SIDEBANDS versus CARRIER FREQUENCY

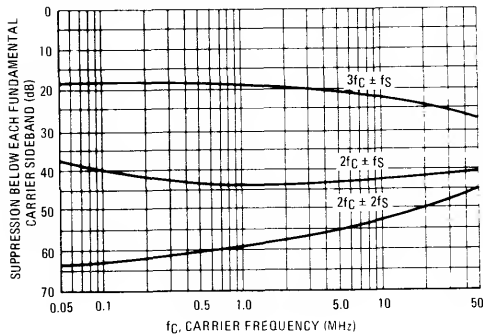
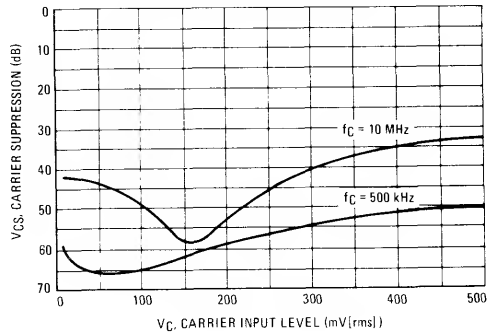


FIGURE 22 – CARRIER SUPPRESSION versus CARRIER INPUT LEVEL



OPERATIONS INFORMATION

The MC1596/MC1496, a monolithic balanced modulator circuit, is shown in Figure 23.

This circuit consists of an upper quad differential amplifier driven by a standard differential amplifier with dual current sources. The output collectors are cross-coupled so that full-wave balanced multiplication of the two input voltages occurs. That is, the output signal is a constant times the product of the two input signals.

Mathematical analysis of linear ac signal multiplication indicates that the output spectrum will consist of only the sum and difference of the two input frequencies. Thus, the device may be used as a balanced modulator, doubly balanced mixer, product detector, frequency doubler, and other applications requiring these particular output signal characteristics.

The lower differential amplifier has its emitters connected to the package pins so that an external emitter resistance may be used. Also, external load resistors are employed at the device output.

Signal Levels

The upper quad differential amplifier may be operated either in a linear or a saturated mode. The lower differential amplifier is operated in a linear mode for most applications.

For low-level operation at both input ports, the output signal will contain sum and difference frequency components and have an amplitude which is a function of the product of the input signal amplitudes.

For high-level operation at the carrier input port and linear operation at the modulating signal port, the output signal will contain sum and difference frequency components of the modulating signal frequency and the fundamental and odd harmonics of the carrier frequency. The output amplitude will be a constant times the modulating signal amplitude. Any amplitude variations in the carrier signal will not appear in the output.

FIGURE 23 – CIRCUIT SCHEMATIC*

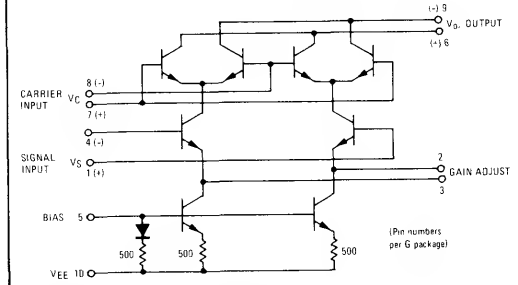
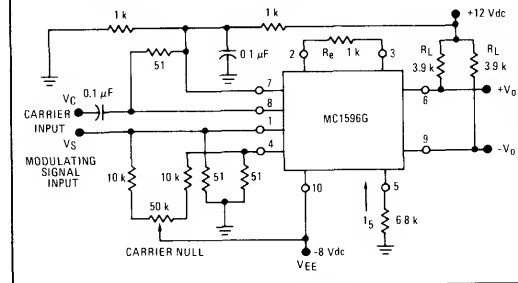


FIGURE 24 – TYPICAL MODULATOR CIRCUIT*



*Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

OPERATIONS INFORMATION (continued)

The linear signal handling capabilities of a differential amplifier are well defined. With no emitter degeneration, the maximum input voltage for linear operation is approximately 25 mV peak. Since the upper differential amplifier has its emitters internally connected, this voltage applies to the carrier input port for all conditions.

Since the lower differential amplifier has provisions for an external emitter resistance, its linear signal handling range may be adjusted by the user. The maximum input voltage for linear operation may be approximated from the following expression:

$$V = (I_5)(R_E) \text{ volts peak.}$$

This expression may be used to compute the minimum value of R_E for a given input voltage amplitude.

FIGURE 25 — TABLE 1
VOLTAGE GAIN AND OUTPUT FREQUENCIES

Carrier Input Signal (V_C)	Approximate Voltage Gain	Output Signal Frequency(s)
Low-level dc	$\frac{R_L V_C}{2(R_E + 2r_e)(\frac{KT}{q})}$	f_M
High-level dc	$\frac{R_L}{R_E + 2r_e}$	f_M
Low-level ac	$\frac{R_L V_C(\text{rms})}{2\sqrt{2}(\frac{KT}{q})(R_E + 2r_e)}$	$f_C \pm f_M$
High-level ac	$\frac{0.637 R_L}{R_E + 2r_e}$	$f_C \pm f_M, 3f_C \pm f_M, 5f_C \pm f_M, \dots$

The gain from the modulating signal input port to the output is the MC1596/MC1496 gain parameter which is most often of interest to the designer. This gain has significance only when the lower differential amplifier is operated in a linear mode, but this includes most applications of the device.

As previously mentioned, the upper quad differential amplifier may be operated either in a linear or a saturated mode. Approximate gain expressions have been developed for the MC1596/MC1496 for a low-level modulating signal input and the following carrier input conditions:

- 1) Low-level dc
- 2) High-level dc
- 3) Low-level ac
- 4) High-level ac

These gains are summarized in Table 1, along with the frequency components contained in the output signal.

NOTES:

1. Low-level Modulating Signal, V_M , assumed in all cases. V_C is Carrier Input Voltage.
2. When the output signal contains multiple frequencies, the gain expression given is for the output amplitude of each of the two desired outputs, $f_C + f_M$ and $f_C - f_M$.
3. All gain expressions are for a single-ended output. For a differential output connection, multiply each expression by two.
4. R_L = Load resistance.
5. R_E = Emitter resistance between pins 2 and 3.
6. r_e = Transistor dynamic emitter resistance, at $+25^\circ\text{C}$;

$$r_e \approx \frac{26 \text{ mV}}{I_5 (\text{mA})}$$

7. K = Boltzmann's Constant, T = temperature in degrees Kelvin, q = the charge on an electron.

$$\frac{KT}{q} \approx 26 \text{ mV at room temperature}$$

APPLICATIONS INFORMATION

Double sideband suppressed carrier modulation is the basic application of the MC1596/MC1496. The suggested circuit for this application is shown on the front page of this data sheet.

In some applications, it may be necessary to operate the MC1596/MC1496 with a single dc supply voltage instead of dual supplies. Figure 26 shows a balanced modulator designed for operation with a single +12 Vdc supply. Performance of this circuit is similar to that of the dual supply modulator.

AM Modulator

The circuit shown in Figure 27 may be used as an amplitude modulator with a minor modification.

All that is required to shift from suppressed carrier to AM operation is to adjust the carrier null potentiometer for the proper amount of carrier insertion in the output signal.

However, the suppressed carrier null circuitry as shown in Figure 27 does not have sufficient adjustment range. Therefore, the modulator may be modified for AM operation by changing two resistor values in the null circuit as shown in Figure 28.

Product Detector

The MC1596/MC1496 makes an excellent SSB product detector (see Figure 29).

This product detector has a sensitivity of 3.0 microvolts and a dynamic range of 90 dB when operating at an intermediate frequency of 9 MHz.

The detector is broadband for the entire high frequency range. For operation at very low intermediate frequencies down to 50 kHz the 0.1 μF capacitors on pins 7 and 8 should be increased to 1.0 μF . Also, the output filter at pin 9 can be tailored to a specific intermediate frequency and audio amplifier input impedance.

As in all applications of the MC1596/MC1496, the emitter resistance between pins 2 and 3 may be increased or decreased to adjust circuit gain, sensitivity, and dynamic range.

This circuit may also be used as an AM detector by introducing carrier signal at the carrier input and an AM signal at the SSB input.

The carrier signal may be derived from the intermediate frequency signal or generated locally. The carrier signal may be introduced with or without modulation, provided its level is sufficiently high to saturate the upper quad differential amplifier. If the carrier signal is modulated, a 300 mV(rms) input level is recommended.

MC1496, MC1596

APPLICATIONS INFORMATION (continued)

Doubly Balanced Mixer

The MC1596/MC1496 may be used as a doubly balanced mixer with either broadband or tuned narrow band input and output networks.

The local oscillator signal is introduced at the carrier input port with a recommended amplitude of 100 mV(rms).

Figure 30 shows a mixer with a broadband input and a tuned output.

Frequency Doubler

The MC1596/MC1496 will operate as a frequency doubler by introducing the same frequency at both input ports.

Figures 31 and 32 show a broadband frequency doubler and a tuned output very high frequency (VHF) doubler, respectively.

Phase Detection and FM Detection

The MC1596/MC1496 will function as a phase detector. High-level input signals are introduced at both inputs. When both inputs are at the same frequency the MC1596/MC1496 will deliver an output which is a function of the phase difference between the two input signals.

An FM detector may be constructed by using the phase detector principle. A tuned circuit is added at one of the inputs to cause the two input signals to vary in phase as a function of frequency. The MC1596/MC1496 will then provide an output which is a function of the input signal frequency.

TYPICAL APPLICATIONS

Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

FIGURE 26 – BALANCED MODULATOR
(+12 Vdc SINGLE SUPPLY)

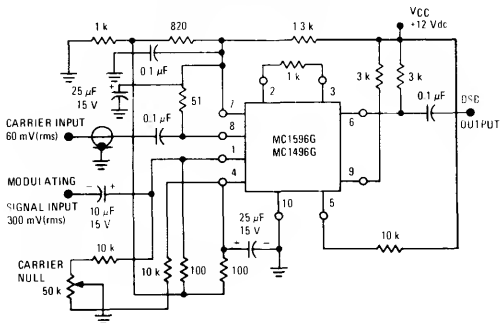


FIGURE 27 – BALANCED MODULATOR-DEMODULATOR

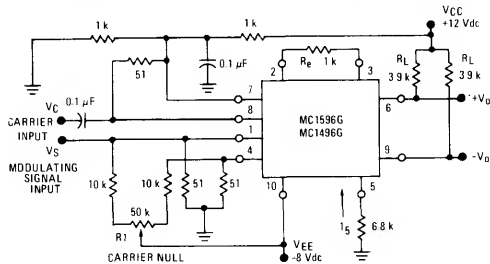


FIGURE 28 – AM MODULATOR CIRCUIT

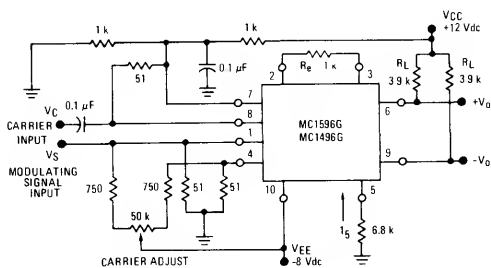
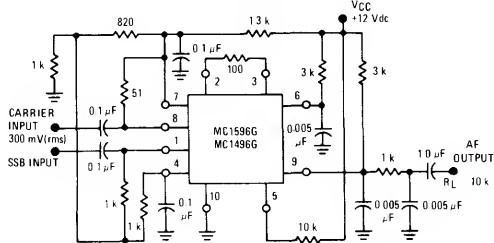


FIGURE 29 – PRODUCT DETECTOR
(+12 Vdc SINGLE SUPPLY)



MC1496, MC1596

TYPICAL APPLICATIONS (continued)

Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

FIGURE 30 — DOUBLY BALANCED MIXER
(BROADBAND INPUTS, 9.0 MHz TUNED OUTPUT)

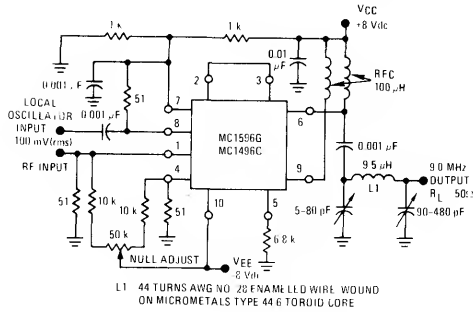


FIGURE 31 — LOW-FREQUENCY DOUBLER

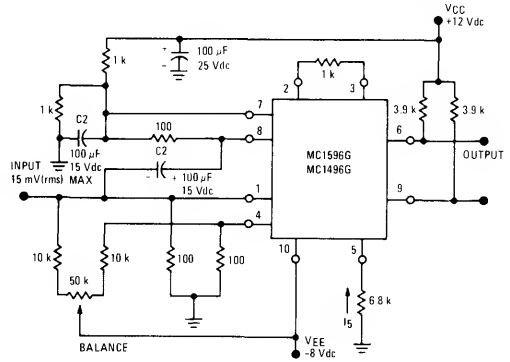
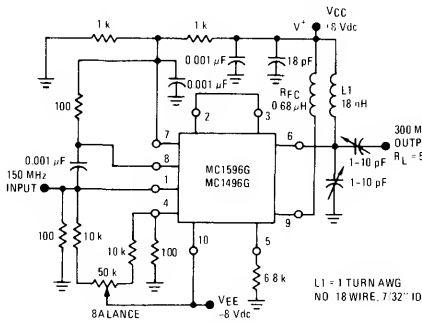
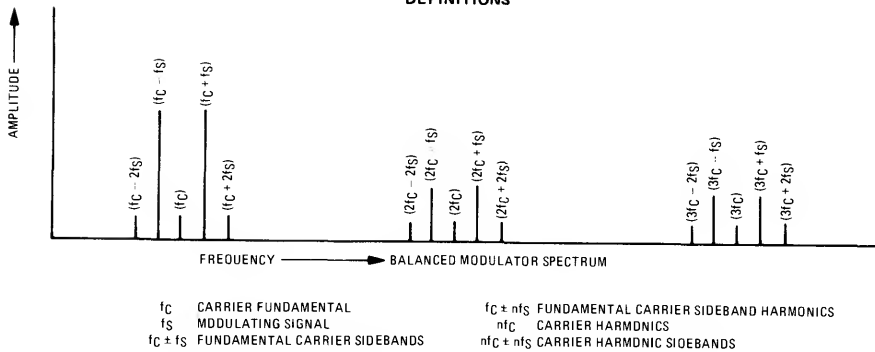


FIGURE 32 — 150 to 300 MHz DOUBLER



DEFINITIONS

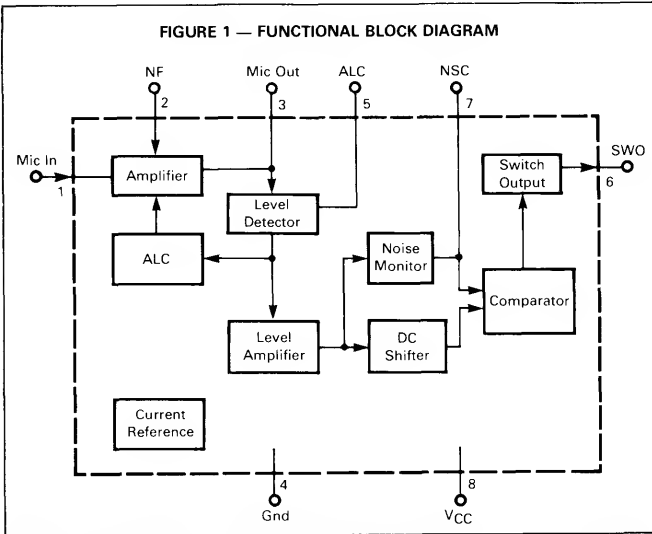


Product Preview

VOICE ACTIVATED SWITCH

The MC2830 circuit incorporates a microphone amplifier (MIC AMP), automatic level control (ALC) and a voice activated switch. The voice activated switch circuit has the ability to distinguish a voice from the background noise and trigger the switch output circuit by the voice signal. Therefore, the switching operation is highly reliable in noisy environments. The ALC range of the microphone amplifier is over 50 dB and can be adjusted by an external resistor. This device is particularly suitable for applications such as radio transceivers, car radios, message storage recorders, and voice controlled toys.

- Microphone Amplifier with External Feedback
- External Resistor Adjust ALC Over 50 dB
- Voice Activated Switch with Externally Controlled Sensitivity
- Low Voltage Operation from 1.8 to 8.0 V

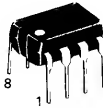


This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice

MC2830

VOICE ACTIVATED SWITCH

SILICON MONOLITHIC INTEGRATED CIRCUIT

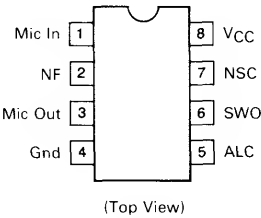


P SUFFIX
PLASTIC PACKAGE
CASE 626



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
MC2830D	0 to +70°C	SO-8
MC2830P		Plastic DIP

MC2830

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	10	V
Operation Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Loading Current: Pin 3	I_O	200	μA
Pin 6	I_{SWO}	2.0	mA

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0$ V, Input Frequency = 1.0 kHz, Loading Resistor = 50 kOhm, $T_A = 25$ °C)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Supply Voltage	8	V_{CC}	1.8	—	8.0	V
Quiescent Current	8	I_D	—	—	2.0	mA
MIC AMP Open Loop Gain		A_{VOL}	—	80	—	dB
Total Harmonic Distortion of MIC AMP ($V_O = 0.1$ Vrms)	3	THD	—	1.0	—	%
Maximum MIC AMP Output Swing	3	V_O	—	0.16	—	Vrms
ALC Range (-6.0 dB, $R_1 = 33$ k, $V_{in} = 1.0$ V)	3	ALC	40	50	—	dB
Ripple Rejection	3	RR	—	55	—	dB
Voice Trigger Level Above Noise		$V_{s,n}$	—	3.0	—	dB
Switch Output Current	6	I_{SWO}	—	—	2.0	mA
Switch Output Voltage ($I_{SWO} = 2.0$ mA) High Low	6	V_{SWO}	4.6 —	— —	— 0.4	V

PIN FUNCTION DESCRIPTION

Pin No.	Function	Description
1	MIC IN	Input of the microphone amplifier. The gain of the amplifier is set by the external components of the R_f , R_2 , and C_2 (See formula 2).
2	NF	This is the negative feedback input pin of the microphone amplifier.
3	MIC OUT	Output of the microphone amplifier. It is designed to drive a maximum load current of 200 μA .
4	GND	The ground pin.
5	ALC	This pin is for the ALC level detector filter. An RC is connected to this pin.
6	SWO	This is the output pin of the voice activated switch. A resistor at this pin sets the voice trigger level above the noise level. The current drain of this pin is around 20 μA typical with a switch "off" state. The maximum output voltage level is $V_{CC} - V_{CES}$ with a maximum output current of 2.0 mA. As shown in Figure 3, this output is used to connect a switch time delay circuit to unify the "on" time. In Figure 3, C_5 is the time delay capacitor which controls the "on" time of TR_1 .
7	NSC	The Noise Storing Capacitor at this pin sets the rise time and decay time. The rise time is determined by the constant of the R_5C_4 .
8	V_{CC}	This pin has a low voltage operation from 1.8 to 8.0 Volts.

MC2830

FIGURE 2 — TEST CIRCUIT

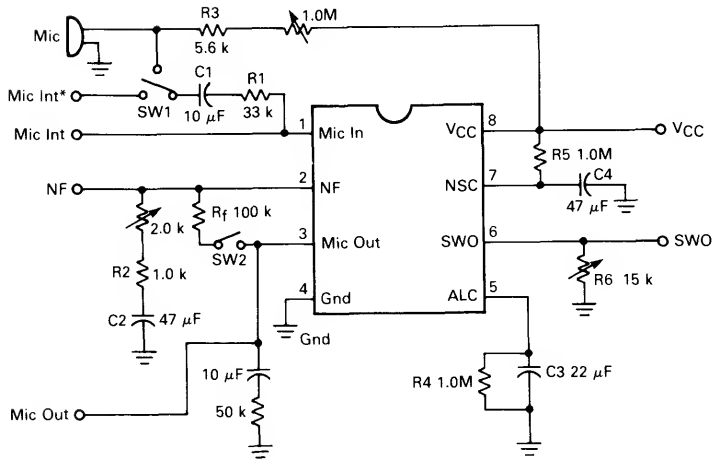
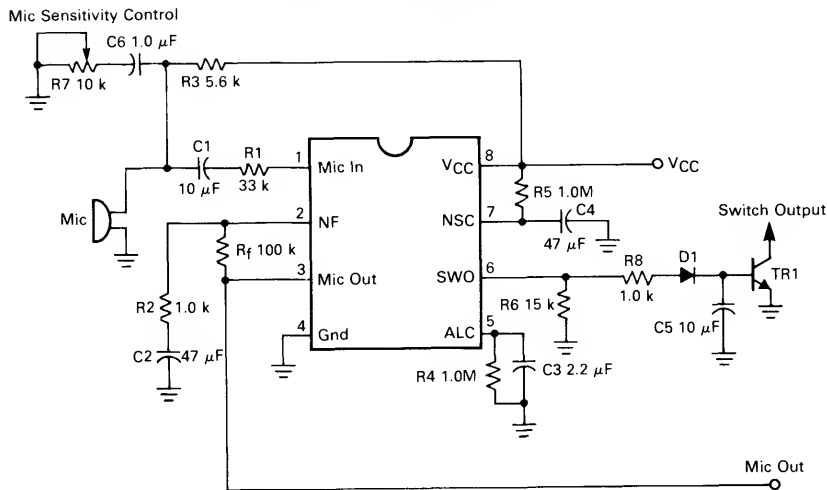


FIGURE 3 — TYPICAL APPLICATION CIRCUIT



FUNCTIONAL DESCRIPTION

As shown in the block diagram, the features provided by the MC2830 are the microphone amplifier with ALC and voice switch circuit. The detailed functional circuitry is described below.

Microphone Amplifier

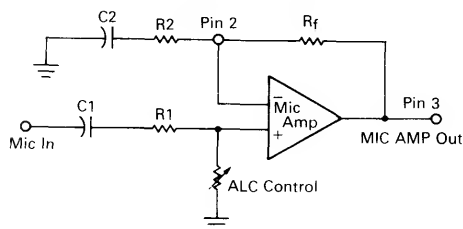
The MIC AMP is a noninverting amplifier as shown in Figure 4. An ALC controlled resistance is connected to the input pin of the MIC AMP to accomplish ALC function. The voltage gain and ALC attenuation ratio are given in formulas (1) and (2):

$$\text{Voltage Gain} = 1 + \frac{R_f}{R_2 = 1/\omega C_2} \quad (1)$$

$$\text{ALC} = 20 \log \left(\frac{R_1 + R_{alc}}{R_{alc}} \right) \quad (2)$$

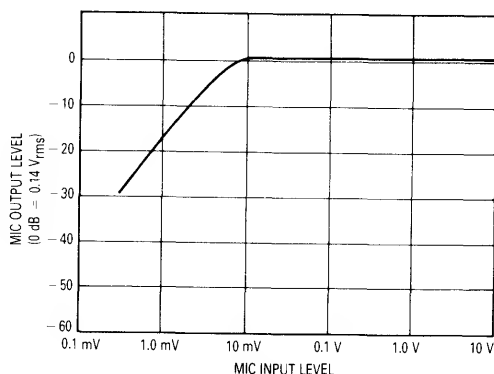
Replacing R_f by a Z_f network can be formed as a band pass, low pass or high pass network for various applications.

FIGURE 4 — MIC AMPLIFIER WITH ALC



A typical application circuit is shown in Figure 3, the ALC performance of the microphone amplifier is shown in Figure 5.

FIGURE 5 — ALC CHARACTERISTICS

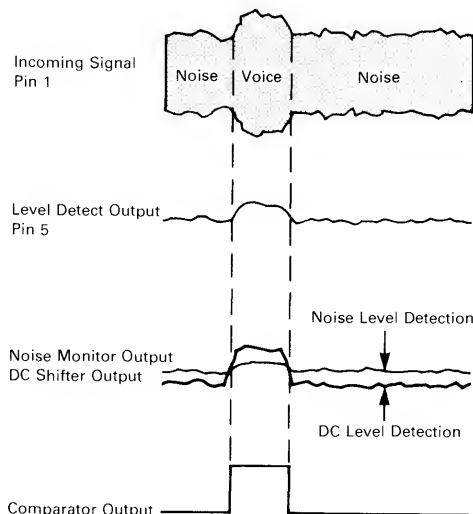


Voice Detection and Switching

A traditional voice activated circuit design is unable to distinguish between voice and noise in the incoming signal. In a noisy environment, the switch is often mis-triggered by noise, or the activation sensitivity must be reduced. The MC2830 voice activated circuit has overcome this weakness in traditional designs. The switch is activated by voice level above the noise and is not affected by the background noise level. This is accomplished by utilizing the differences in voice and noise waveforms. Voice waveforms generally have a wide range of variation in amplitude, whereas noise waveforms are more stable. With this in mind, the NOISE MONITOR in Figure 1 was designed to have an output characteristic which has a slow attack time but a fast decay time. When the envelope of incoming signal, which consists of voice and noise, is passing through it, the voice will not be stable during the long time constant of RC (approx. 45 seconds) and it is therefore degraded. Whereas the noise content of incoming signal is delayed at the rising edge of its envelope, as in Figure 6. Meanwhile, the envelope of the incoming signal is passing through the DC SHIFTER path, which does not introduce any time constant or amplification, but gives the incoming signal envelope a dc offset set by resistor R6.

By comparing the two signals from the output of the DC SHIFTER and the NOISE MONITOR, as in Figure 6, the voice is distinguished from the incoming signal and activates the switch circuit. The sensitivity of voice activation depends on the value of R6. The voice activation sensitivity is reduced from 3.0 dB to 8.0 dB above the noise if R6 changes from 14 k to 7.0 k.

FIGURE 6 — WAVEFORMS OF VOICE DETECTION AND SWITCHING



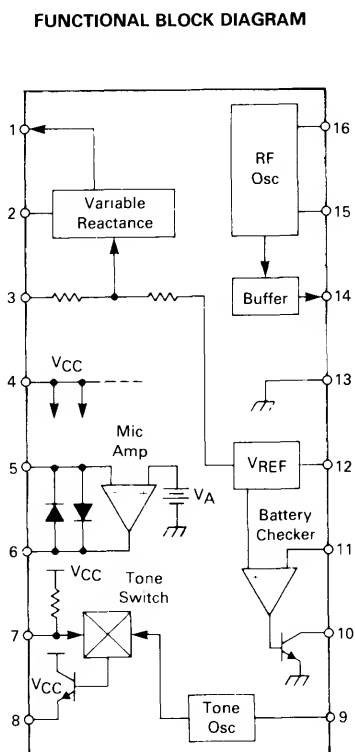
MC2831A

LOW POWER FM TRANSMITTER SYSTEM

SILICON MONOLITHIC INTEGRATED CIRCUIT

-

PIN ASSIGNMENTS



Variable	Pin	Variable	Pin
Reactance	1	RF	16
Output	2	Osc	15
Decoupling	2	RF	14
Modulator	3	Output	13
Input	3	Gnd	12
VCC2	4	VCC1	11
Mic Amp	5	Battery	10
Input	5	Checker	9
Output	6	LED	8
Tone	7	Osc	7
Switch	7	Coil	6
Tone	8		
Output	8		

Device	Temperature Range	Package
MC2831AD	- 30°C to + 75°C	SO-16
MC2831AP		Plastic DIP

MC2831A

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	10	Vdc
Operating Supply Voltage Range	V_{CC}	3.0 to 8.0	Vdc
Battery Checker Output Sink Current	I_{LED}	25	mA
Junction Temperature	T_J	+150	$^\circ\text{C}$
Operating Ambient Temperature Range	T_A	-30 to +75	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($V_{CC1} = 4.0\text{ Vdc}$, $V_{CC2} = 4.0\text{ Vdc}$, $T_A = 25^\circ\text{C}$, unless otherwise noted)

Characteristic	Symbol	Pin	Min	Typ	Max	Unit
Drain Current	I_{CC1}	12	150	290	420	μA
Drain Current	I_{CC2}	4	2.2	3.6	6.5	mA

BATTERY CHECKER

Threshold Voltage (LED Off \rightarrow On)	V_{TB}	11	1.0	1.2	1.4	Vdc
Output Saturation Voltage (Pin 11 = 0 V, Pin 10 Sink Current = 5.0 mA)	V_{OSAT}	10	—	0.15	0.5	Vdc

MIC AMPLIFIER

Voltage Gain, Closed Loop ($V_{in} = 1.0\text{ mV}_{rms}$, $f_{in} = 1.0\text{ kHz}$)	A_V	5, 6	27	30	33	dB
Output DC Voltage	V_{Odc}	6	1.1	1.4	1.7	Vdc
Output Swing ($V_{in} = 30\text{ mV}_{rms}$, $f_{in} = 1.0\text{ kHz}$)	V_{OP-p}	6	0.8	1.2	1.6	Vp-p
Total Harmonic Distortion ($V_O = 31\text{ mV}_{rms}$, $f_{in} = 1.0\text{ kHz}$)	THD	6	—	0.7	—	%

PILOT TONE OSCILLATOR (250 Ω LOADING)

Output AF Voltage ($f_O = 5.0\text{ kHz}$)	V_{AFO}	8	—	50	—	mV_{rms}
Output DC Voltage	V_{Odc}	8	—	1.4	—	Vdc
Total Harmonic Distortion ($f_O = 5.0\text{ kHz}$, $V_{AF} = 150\text{ mV}_{rms}$)	THD	8	—	1.8	5.0	%
Tone Switch Threshold	—	7	1.1	1.4	1.7	Vdc

FM MODULATOR (120 Ω LOADING)

Output RF Voltage ($f_O = 16.6\text{ MHz}$)	V_{RFO}	14	—	40	—	mV_{rms}
Output DC Voltage	V_{Odc}	14	—	1.3	—	Vdc
Modulation Sensitivity (Note 1) ($V_{in} = 1.0\text{ V} \pm 0.2\text{ V}$)	SEN	3, 14	6.0	10	18	Hz mVdc
Maximum Deviation (Note 1) ($V_{in} = 0\text{ V to } +2.0\text{ V}$)	F_{dev}	3, 14	± 2.5	± 5.0	± 12.5	kHz
RF Frequency Range	—	14	—	—	60	MHz

Note 1. Modulation sensitivity and maximum deviation are measured at 49.815 MHz, which is the third harmonic of the crystal frequency.

MC2831A

FIGURE 1 — TEST CIRCUIT

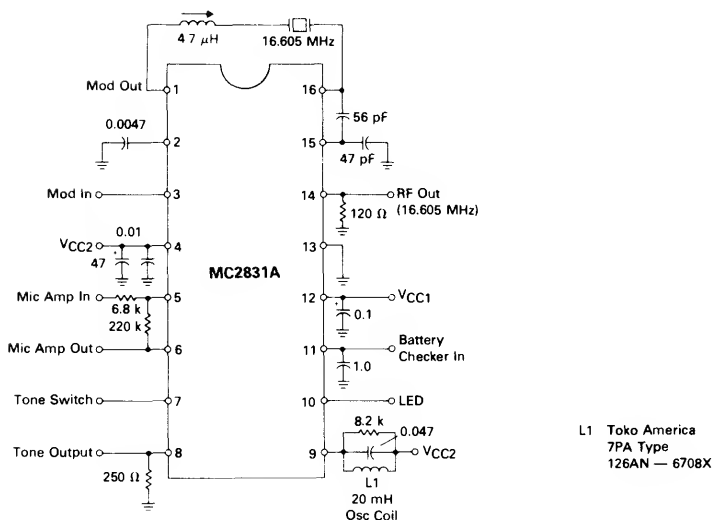
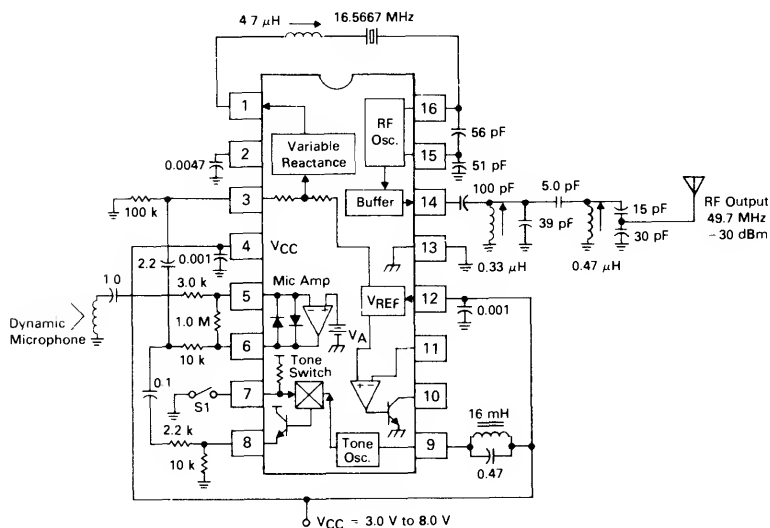


FIGURE 2 — SINGLE CHIP FM VHF TRANSMITTER AT 49.7 MHz



NOTES:

S1 is a normally closed push button type switch.

The crystal used is fundamental mode, calibrated for parallel resonance with a 32 pF load. The 49.7 MHz output is generated in the output buffer, which generates useful harmonics to 60 MHz.

The network on the output at Pin 14 provides output tuning and impedance matching to 50 Ω at 49.7 MHz. Harmonics are suppressed by more than 25 dB.

Battery checker circuit (Pins 10, 11) is not used in this application.

All capacitors in microfarads, inductors in Henries and resistors in Ohms, unless otherwise specified.

Advance Information

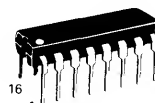
LOW POWER FM TRANSMITTER SYSTEM

MC2833 is a one-chip FM transmitter subsystem designed for cordless telephone and FM communication equipment. It includes a microphone amplifier, voltage controlled oscillator and two auxiliary transistors.

- Wide Range of Operating Supply Voltage (2.8–9.0 V)
- Low Drain Current ($I_{CC} = 2.9 \text{ mA Typ}$)
- Low Number of External Parts Required
- –30 dBm Power Output to 60 MHz Using Direct RF Output
- +10 dBm Power Output Attainable Using On-Chip Transistor Amplifiers

MC2833

LOW POWER FM TRANSMITTER SYSTEM



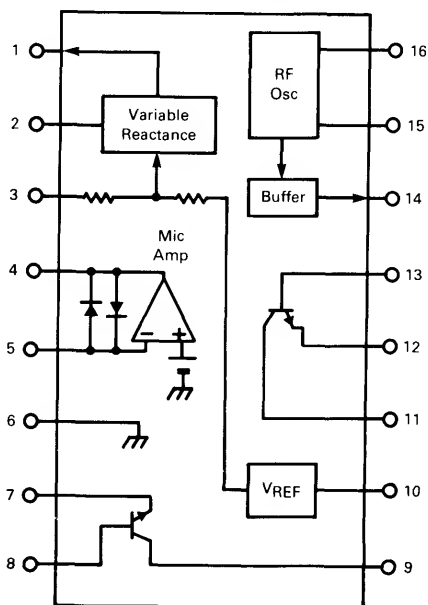
P SUFFIX
PLASTIC PACKAGE
CASE 648



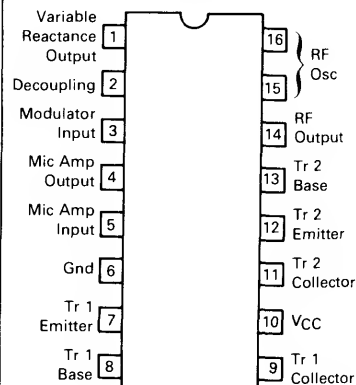
D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO-16)

8

FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENTS



This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS

Ratings	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	10 (max)	V
Operating Supply Voltage Range	V_{CC}	2.8–9.0	V
Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_A	–30 to +75	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS ($V_{CC} = 4.0$ V, $T_A = 25^\circ\text{C}$, unless otherwise noted)

Characteristics	Symbol	Pin	Min	Typ	Max	Unit
Drain Current (No input signal)	I_{CC}	10	1.7	2.9	4.3	mA

FM MODULATOR

Output RF Voltage ($f_o = 16.6$ MHz)	$V_{out\ RF}$	14	60	90	130	mVrms
Output DC Voltage (No input signal)	V_{dc}	14	2.2	2.5	2.8	V
Modulation Sensitivity ($f_o = 16.6$ MHz) ($V_{in} = 0.8$ V to 1.2 V)	SEN	3.0 14	7.0 —	10 —	15 —	Hz/mVdc
Maximum Deviation ($f_o = 16.6$ MHz) ($V_{in} = 0$ V to 2.0 V)	Fdev	3.0 14	3.0 —	5.0 —	10 —	kHz

MIC AMPLIFIER

Closed Loop Voltage Gain ($V_{in} = 3.0$ mVrms) ($f_{in} = 1.0$ kHz)	A_v	4.0 5.0	27 —	30 —	33 —	dB
Output DC Voltage (No input signal)	$V_{out\ dc}$	4.0	1.1	1.4	1.7	V
Output Swing Voltage ($V_{in} = 30$ mVrms) ($f_{in} = 1.0$ kHz)	$V_{out\ P-P}$	4.0	0.8	1.2	1.6	Vp-p
Total Harmonic Distortion ($V_{in} = 3.0$ mVrms) ($f_{in} = 1.0$ kHz)	THD	4.0	—	0.15	2.0	%

AUXILIARY TRANSISTOR STATIC CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
Collector Base Breakdown Voltage ($I_C = 5.0$ μA)	$V_{(BR)CBO}$	15	45	—	V
Collector Emitter Breakdown Voltage ($I_C = 200$ μA)	$V_{(BR)CEO}$	10	15	—	V
Collector Substrate Breakdown Voltage ($I_C = 50$ μA)	$V_{(BR)CSO}$	—	70	—	V
Emitter Base Breakdown Voltage ($I_E = 50$ μA)	$V_{(BR)EBO}$	—	6.2	—	V
Collector Base Cut Off Current ($V_{CB} = 10$ V) ($I_E = 0$)	I_{CBO}	—	—	200	nA
DC Current Gain ($I_C = 3.0$ mA) ($V_{CE} = 3.0$ V)	h_{FE}	40	150	—	—

AUXILIARY TRANSISTOR DYNAMIC CHARACTERISTICS

Current Gain Bandwidth Product ($V_{CE} = 3.0$ V) ($I_C = 3.0$ mA)	f_T	—	500	—	MHz
Collector Base Capacitance ($V_{CE} = 3.0$ V) ($I_C = 0$)	C_{CB}	—	2.0	—	pF
Collector Substrate Capacitance ($V_{CS} = 3.0$ V) ($I_C = 0$)	C_{CS}	—	3.3	—	pF

MC2833

FIGURE 1 — TEST CIRCUIT

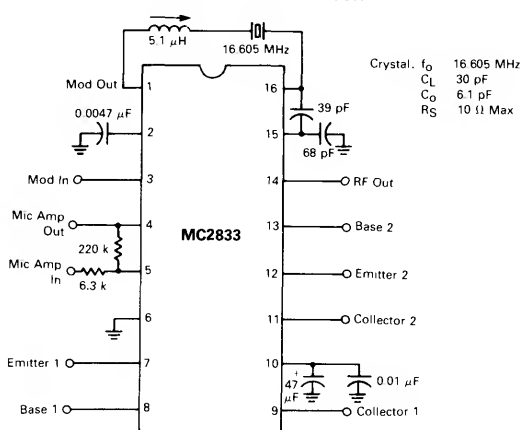
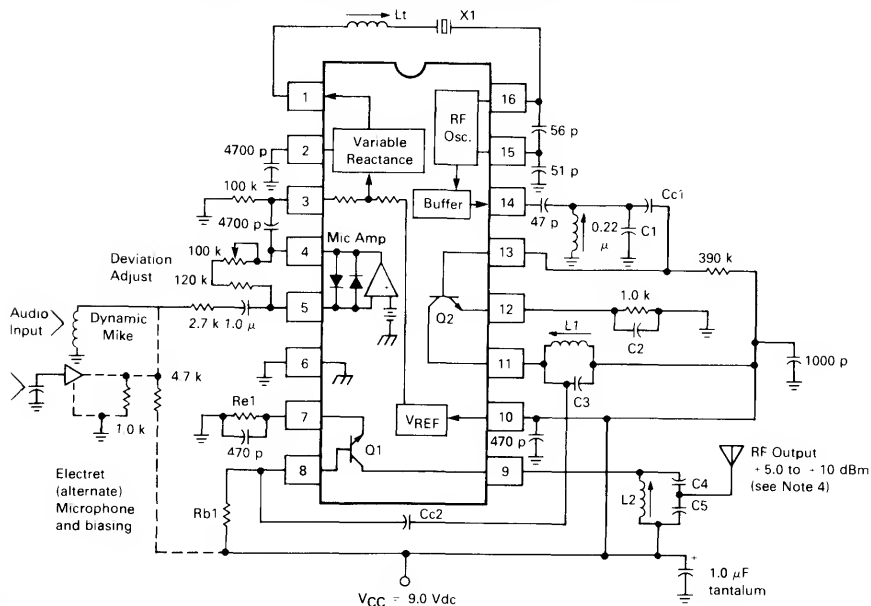


FIGURE 2 — SINGLE CHIP VHF NARROWBAND FM TRANSMITTER



NOTES:

1. Components versus output frequency:

Output RF	X1 (MHz)	Lt (μH)	L1 (μH)	L2 (μH)	Re1	Rb1	Cc1	Cc2	C1	C2	C3	C4	C5
49.7 MHz	16.5667	3.3-4.7	0.22	0.22	330	390 k	33 p	33 p	33 p	470 p	33 p	47 p	220 p
76 MHz	12.6	5.1	0.22	0.22	150	300 k	68 p	10 p	68 p	470 p	12 p	20 p	120 p
144.6 MHz	12.05	5.6	0.15	0.10	150	220 k	47 p	10 p	68 p	1000 p	18 p	12 p	33 p

2. Crystal X1 is fundamental mode, calibrated for parallel resonance with a 32 pF load. The final output frequency is generated by frequency multiplication within the MC2833 IC. The RF output buffer (Pin 14) and Q2 transistor are used as a frequency tripler and doubler, respectively, in all three transmitters. The Q1 output transistor is a linear amplifier in the 49.7 MHz and 76 MHz transmitters, and a frequency doubler in the 144 MHz transmitter.

3. All coils used are 7 mm tunable shielded inductors, Toko B199SN-T10XXZ, B199KN-T10XXZ or equivalent.

4. Power output is $\approx +10$ dBm for 49.7 MHz and 76 MHz transmitters, and $\approx +5.0$ dBm for the 144 MHz transmitter at $V_{CC} = 8.0$ V. Power output drops with lower V_{CC} .

5. All capacitors in microfarads, inductors in Henries and resistors in Ohms unless otherwise specified.

FIGURE 3 — BUFFER/MULTIPLIER (X3, PIN 14)

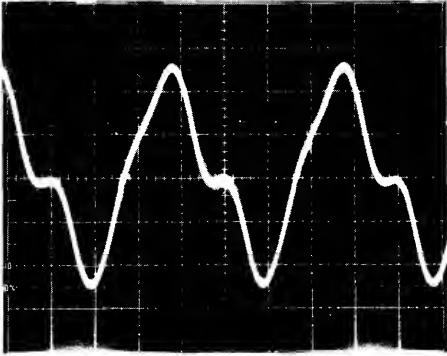


FIGURE 4 — INPUT TO DOUBLER (PIN 13)

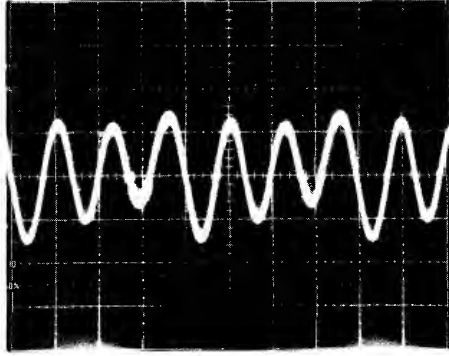


FIGURE 5 — DOUBLER OUTPUT 76 MHz (PIN 11)

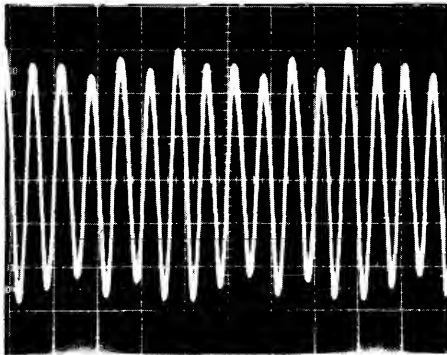


FIGURE 6 — SPECTRUM

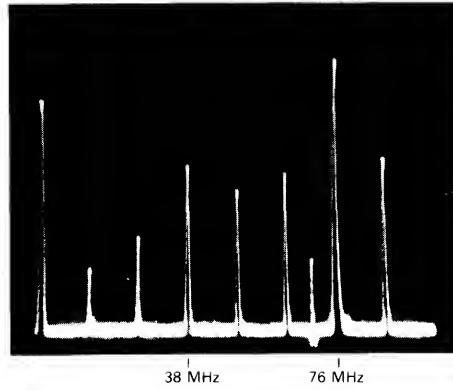
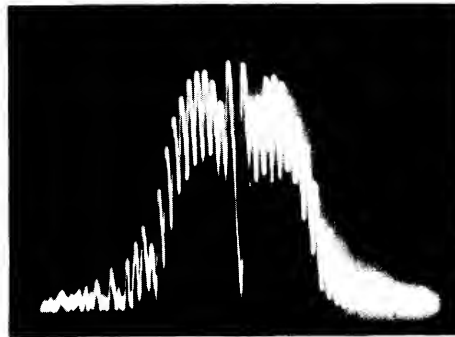


FIGURE 7 — OUTPUT SPECTRUM (49 MHz)



FIGURE 8 — MODULATION SPECTRUM

-43 dB



MC2833

FIGURE 9 — 144 MHz/X12 MULTIPLIER

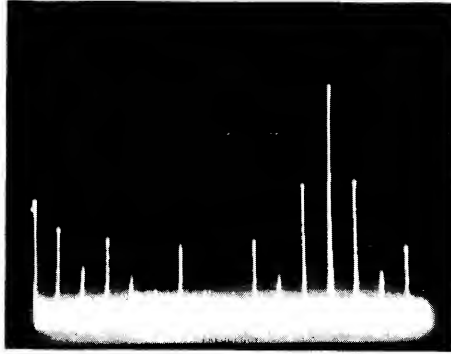


FIGURE 10 — CIRCUIT SIDE VIEW

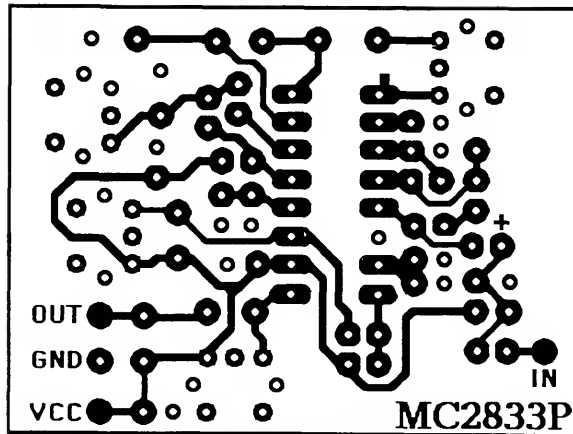
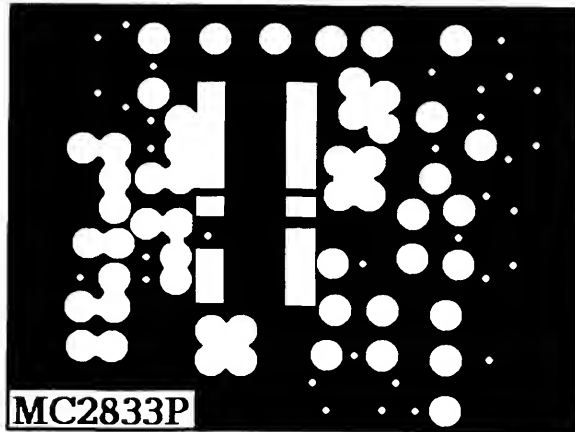
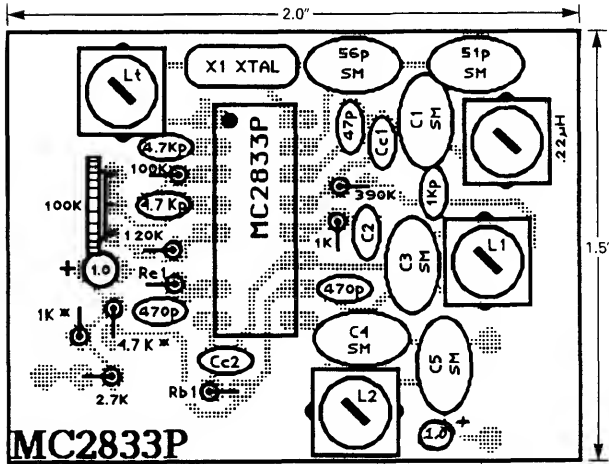


FIGURE 11 — GROUND PLANE ON COMPONENT SIDE



MC2833

FIGURE 12 — COMPONENT VIEW



NOTES:

- Positive artwork provided
- Drawing is 2X each dimension (final board size 1.5" x 2.0").
- Drill holes must be plated to ensure making all ground (V_{EE}) connections!
- Resistors labelled * are used for biasing of electret microphone if used.
- Capacitors labelled "SM" are silver mica.

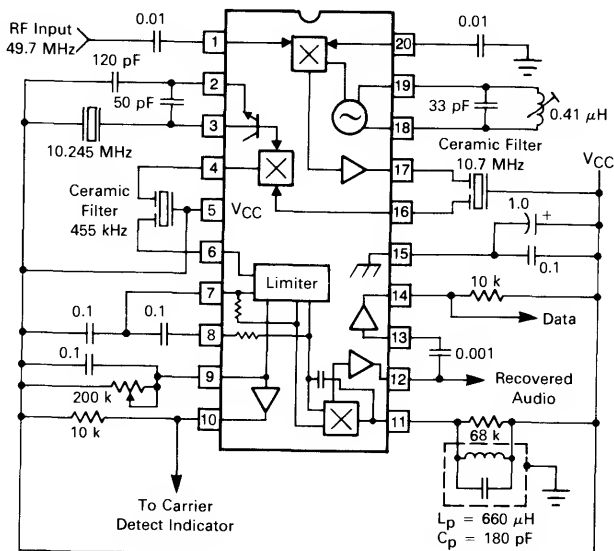
Advance Information

LOW POWER NARROWBAND FM RECEIVER

... includes dual FM conversion with Oscillators, Mixers, Quadrature Discriminator, and Meter Drive/Carrier Detect Circuitry. The MC3335 also has a comparator circuit for FSK detection.

- Complete Dual Conversion Circuitry
- Low Voltage: $V_{CC} = 2.0$ to 6.0 Vdc
- Low Drain Current (Typical 3.6 mA with $V_{CC} = 3.0$ Vdc)
- Excellent Sensitivity: -3.0 dB Input Limiting = 0.7 μ V
- Externally Adjustable Carrier Detect Function
- Separate Data Shaping Output Circuitry
- Data Rate of 2000 to 35000 Baud Detectable
- 60 dB RSSI Range
- Low Number of External Parts Required
- Manufactured in Motorola's MOSAIC Process Technology

TYPICAL APPLICATION AS A FIXED RECEIVER

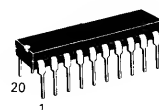


This document contains information on a new product. Specifications and information herein are subject to change without notice.
 MOSAIC is a trademark of Motorola, Inc.

MC3335

LOW POWER DUAL CONVERSION FM RECEIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT

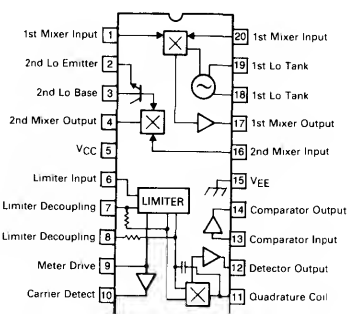


P SUFFIX
 PLASTIC PACKAGE
 CASE 738



DW SUFFIX
 PLASTIC PACKAGE
 CASE 751D
 (SO-20L)

PIN CONNECTION AND FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Device	Temperature Range	Package
MC3335DW	-40° to +85°C	SO-20
MC3335P		Plastic DIP

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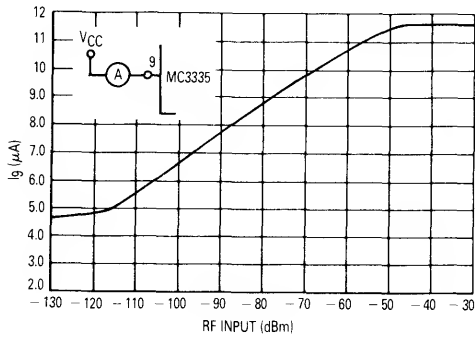
FIGURE 2 — I_{meter} versus INPUT

FIGURE 3 — DRAIN CURRENT, RECOVERED AUDIO versus SUPPLY

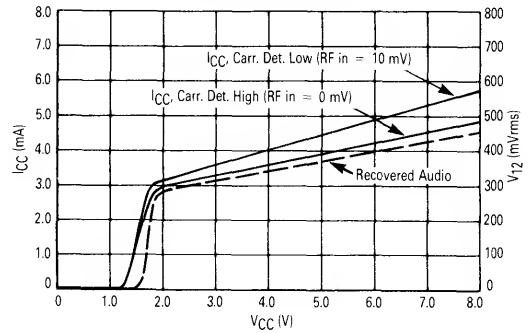
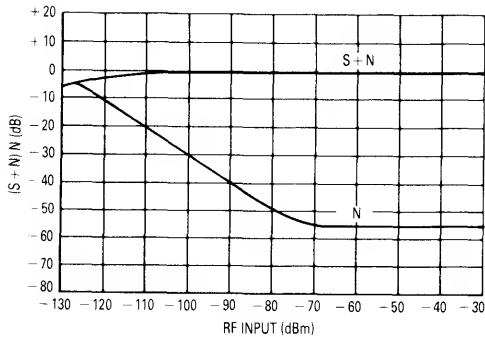
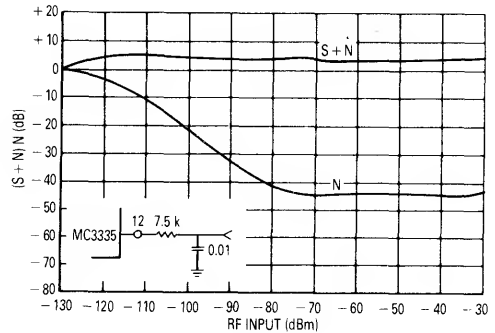
FIGURE 4 — $(S+N)$, N OF 2ND MIXERFIGURE 5 — $(S+N)/N$ versus INPUT

FIGURE 6 — 1ST MIXER 3RD ORDER INTERMODULATION

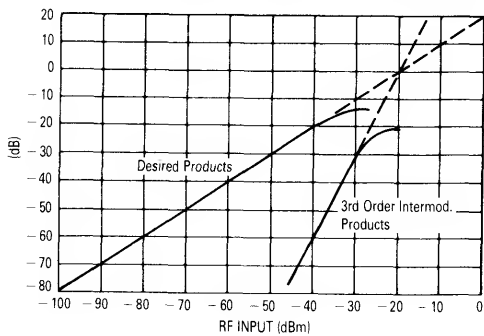
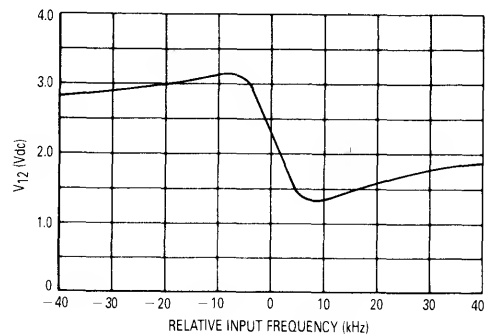


FIGURE 7 — DETECTOR OUTPUT versus FREQUENCY



CIRCUIT DESCRIPTION

The MC3335 is a complete FM narrowband receiver from antenna input to audio preamp output. The low voltage dual conversion design yields low power drain, excellent sensitivity and good image rejection in narrowband voice and data link applications.

In the typical application diagram, the first mixer amplifies the signal and converts the RF input to 10.7 MHz. This IF signal is filtered externally and fed into the second mixer, which further amplifies the signal and converts it to a 455 kHz IF signal. After external band-pass filtering, the low IF is fed into the limiting amplifier and detection circuitry. The audio is recovered using a conventional quadrature detector. Twice-IF filtering is provided internally.

The input signal level is monitored by meter drive circuitry which detects the amount of limiting in the limiting amplifier. The voltage at the meter drive pin determines the state of the carrier detect output which is active low.

APPLICATION

The first local oscillator can be run using a free running LC tank, as a VCO using PLL synthesis, or driven from an external crystal oscillator. At higher V_{CC} values (6.0–7.0 V), it has been run to 170 MHz. The second local oscillator is a common base Colpitts type which is typically run at 10.245 MHz under crystal control.

The mixers are doubly balanced to reduce spurious responses. The first and second mixers have conversion gains of 18 dB and 22 dB (typical), respectively. Mixer gain is stable with respect to supply voltage. For both conversions, the mixer impedances and pin layout are designed to allow the user to employ low cost, readily available ceramic filters. Overall sensitivity is shown in Figure 5. The input level for 20 dB (S+N)/N is 1.3 μ V using the two-pole post-detection filter is demonstrated.

Following the first mixer, a 10.7 MHz ceramic band-pass filter is recommended. The 10.7 MHz filtered signal is then fed into one second mixer input pin, the other input pin being connected to V_{CC} . Pin 5 (V_{CC}) is treated as a common point for emitter-driven signals.

The 455 kHz IF is typically filtered using a ceramic bandpass filter, then fed into the limiter input pin. The limiter has 10 μ V sensitivity for –3.0 dB limiting, flat to 1.0 MHz.

The output of the limiter is internally connected to the quadrature detector, including a quadrature capacitor. A parallel LC tank is needed externally from Pin 11 to V_{CC} . A 68 k Ω shunt resistance is included which determines the peak separation of the quadrature detector; a smaller value will increase the spacing and linearity but decrease recovered audio and sensitivity.

A data shaping circuit is available and can be coupled to the recovered audio output of Pin 12. The circuit is a comparator which is designed to detect zero crossings of FSK modulation. Data rates of 2000 to 35000 baud are detectable using the typical application. Hysteresis is available by connecting a high-valued resistor from Pin 13 to Pin 14. Values below 120 k Ω are not recommended as the input signal cannot overcome the hysteresis.

The meter drive circuitry detects input signal level by monitoring the limiting of the limiting amplifier stages. Figure 2 shows the unloaded current at Pin 9 versus input power. The meter drive current can be used directly (RSSI) or can be used to trip the carrier detect circuit at a specified input power. To do this, pick an RF trip level in dBm. Read the corresponding current from Figure 2 and pick a resistor such that:

$$R10 = 0.64 V_{dc} / I10$$

Hysteresis is available by connecting a high-valued resistor RH between Pin 9 and 10. The formula is:

$$\text{Hysteresis} = V_{CC} / (RH \times 10^{-7}) \text{ dB}$$

MC3356

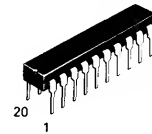
WIDEBAND FSK RECEIVER

... includes Oscillator, Mixer, Limiting IF Amplifier, Quadrature Detector, Audio Buffer, Squelch, Meter Drive, Squelch Status output, and Data Shaper comparator. The MC3356 is designed for use in digital data communications equipment.

- Data Rates up to 500 kilobaud
- Excellent Sensitivity: -3 dB Limiting Sensitivity
 $30 \mu\text{Vrms}$ @ 100 MHz
- Highly versatile, full function device, yet few external parts are required

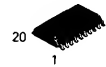
WIDEBAND FSK RECEIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 738

DW SUFFIX
PLASTIC PACKAGE
CASE 751D
(SO-20L)



8

FIGURE 1 — FUNCTIONAL BLOCK DIAGRAM

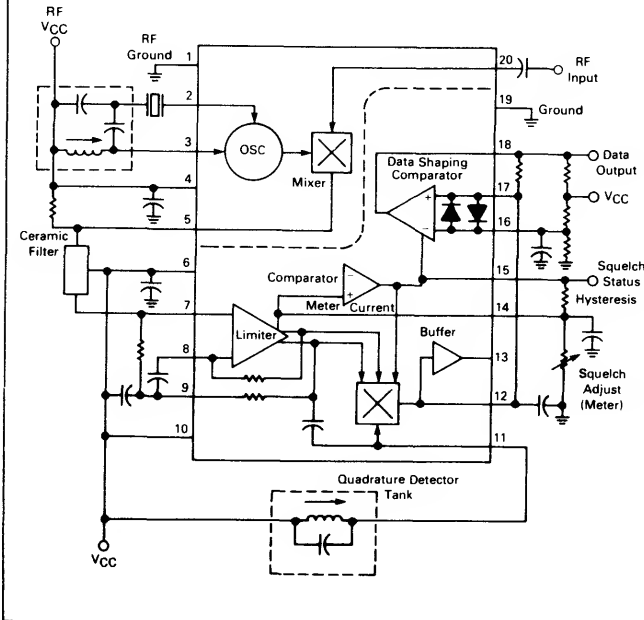
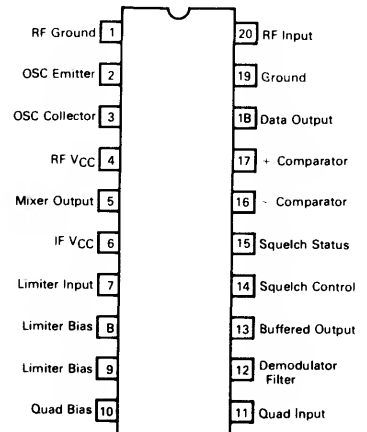


FIGURE 2 — PIN CONNECTIONS



MC3356

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC(max)}$	15	Vdc
Operating Power Supply Voltage Range (Pins 6, 10)	V_{CC}	3.0 to 9.0	Vdc
Operating RF Supply Voltage Range (Pin 4)	RF V_{CC}	3.0 to 12.0	Vdc
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Power Dissipation, Package Rating	P_D	1.25	W

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0$ Vdc, $f_o = 100$ MHz, $f_{osc} = 110.7$ MHz, $\Delta f = \pm 75$ kHz, $f_{mod} = 1.0$ kHz, 50Ω source, $T_A = 25^\circ\text{C}$, test circuit of Figure 3, unless otherwise noted.)

Characteristics	Min	Typ	Max	Unit
Drain Current Total, RF V_{CC} and V_{CC}	—	20	25	mAdc
Input for -3 dB limiting	—	30	—	μVrms
Input for 50 dB quieting $\left(\frac{S+N}{N}\right)$	—	60	—	μVrms
Mixer Voltage Gain, Pin 20 to Pin 5	2.5	—	—	
Mixer Input Resistance, 100 MHz	—	260	—	Ω
Mixer Input Capacitance, 100 MHz	—	5.0	—	pF
Mixer/Oscillator Frequency Range (Note 1)	—	0.2 to 150	—	MHz
IF/Quadrature Detector Frequency Range (Note 1)	—	0.2 to 50	—	MHz
AM Rejection (30% AM, RF $V_{in} = 1.0$ mVrms)	—	50	—	dB
Demodulator Output, Pin 13	—	0.5	—	Vrms
Meter Drive	—	7.0	—	$\mu\text{A/dB}$
Squelch Threshold	—	0.8	—	Vdc

Note 1: Not taken in Test Circuit of Figure 3; new component values required.

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FIGURE 3 — TEST CIRCUIT

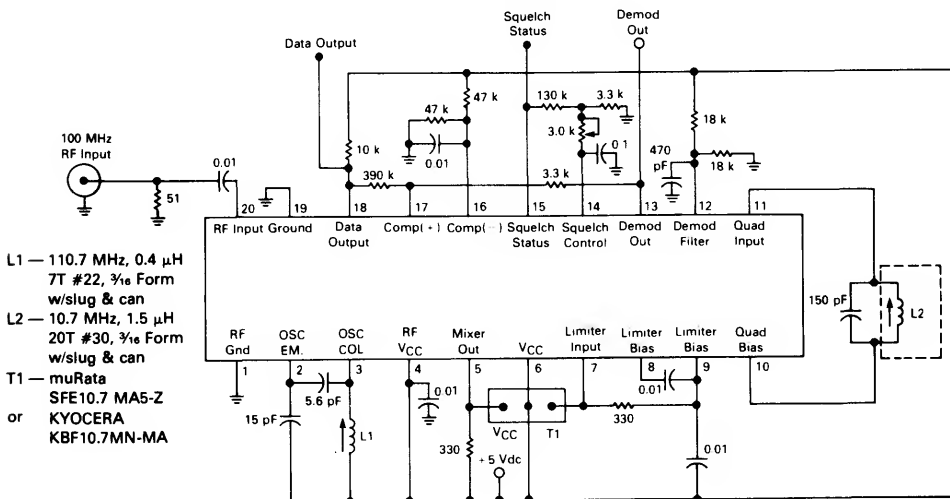


FIGURE 4 — OUTPUT COMPONENTS OF SIGNAL, NOISE, AND DISTORTION

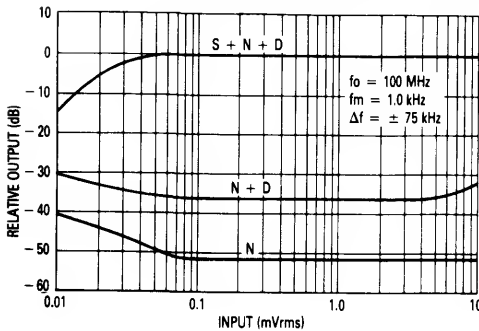
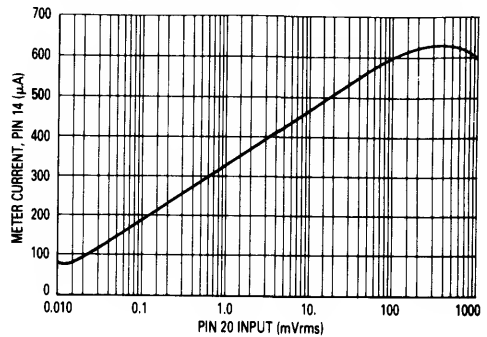


FIGURE 5 — METER CURRENT versus SIGNAL INPUT



GENERAL DESCRIPTION

This device is intended for single and double conversion VHF receiver systems, primarily for FSK data transmission up to 500 K baud (250 kHz). It contains an oscillator, mixer, limiting IF, quadrature detector, signal strength meter drive, and data shaping amplifier.

The oscillator is a common base Colpitts type which can be crystal controlled, as shown in Figure 1, or L-C controlled as shown in the other figures. At higher V_{CC} , it has been operated as high as 200 MHz. A mixer/oscillator voltage gain of 2 up to approximately 150 MHz, is readily achievable.

The mixer functions well from an input signal of 10 μVrms , below which the squelch is unpredictable, up to about 10 mVrms, before any evidence of overload. Operation up to 1.0 Vrms input is permitted, but non-linearity of the meter output is incurred, and some oscillator pulling is suspected. The AM rejection above 10 mVrms is degraded.

The limiting IF is a high frequency type, capable of being operated up to 50 MHz. It is expected to be used at 10.7 MHz in most cases, due to the availability of standard ceramic resonators. The quadrature detector is internally coupled to the IF, and a 5.0 pF quadrature capacitor is internally provided. The -3dB limiting sensitivity of the IF itself is approximately 50 μV (at Pin 7), and the IF can accept signals up to 1.0 Vrms without distortion or change of detector quiescent dc level.

The IF is unusual in that each of the last 5 stages of the 6 state limiter contains a signal strength sensitive, current sinking device. These are parallel connected and buffered to produce a signal strength meter drive which is fairly linear for IF input signals of 10 μV to 100 mVrms. (See Figure 5.)

A simple squelch arrangement is provided whereby the meter current flowing through the meter load resistance flips a comparator at about 0.8 Vdc above ground. The signal strength at which this occurs can be adjusted by changing the meter load resistor. The comparator (+) input and output are available to permit con-

trol of hysteresis. Good positive action can be obtained for IF input signals of above 30 μVrms . The 130 k Ω resistor shown in the test circuit provides a small amount of hysteresis. Its connection between the 3.3 k resistor to ground and the 3.0 k pot, permits adjustment of squelch level without changing the amount of hysteresis.

The squelch is internally connected to both the quadrature detector and the data shaper. The quadrature detector output, when squelched, goes to a dc level approximately equal to the zero signal level, unsquelched. The squelch causes the data shaper to produce a high (V_{CC}) output.

The data shaper is a complete "floating" comparator, with back to back diodes across its inputs. The output of the quadrature detector can be fed directly to either input of this amplifier to produce an output that is either at V_{CC} or V_{EE} , depending upon the received frequency. The impedance of the biasing can be varied to produce an amplifier which "follows" frequency detuning to some degree, to prevent data pulse width changes.

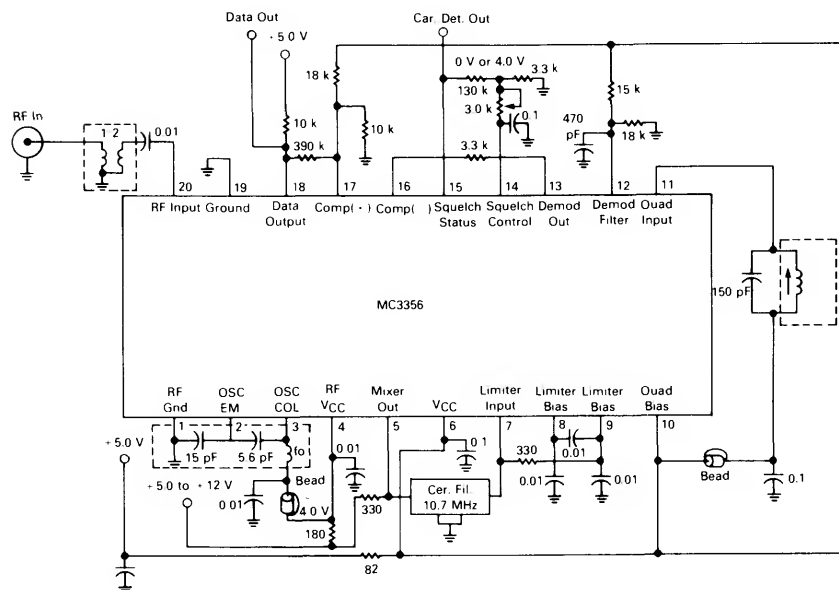
When the data shaper is driven directly from the demodulator output, Pin 13, there may be distortion at Pin 13 due to the diodes, but this is not important in the data application. A useful note in relating high/low input frequency to logic state: low IF frequency corresponds to low demodulator output. If the oscillator is above the incoming RF frequency, then high RF frequency will produce a logic low. (Input to (+) input of Data Shaper as shown in figures 1 and 3.)

APPLICATION NOTES

The MC3356 is a high frequency/high gain receiver that requires following certain layout techniques in designing a stable circuit configuration. The objective is to minimize or eliminate, if possible, any unwanted feedback.

MC3356

FIGURE 6 — APPLICATION WITH FIXED BIAS ON DATA SHAPER



APPLICATION NOTES (continued)

Shielding, which includes the placement of input and output components, is important in minimizing electrostatic or electromagnetic coupling. The MC3356 has its pin connections such that the circuit designer can place the critical input and output circuits on opposite ends of the chip. Shielding is normally required for inductors in tuned circuits.

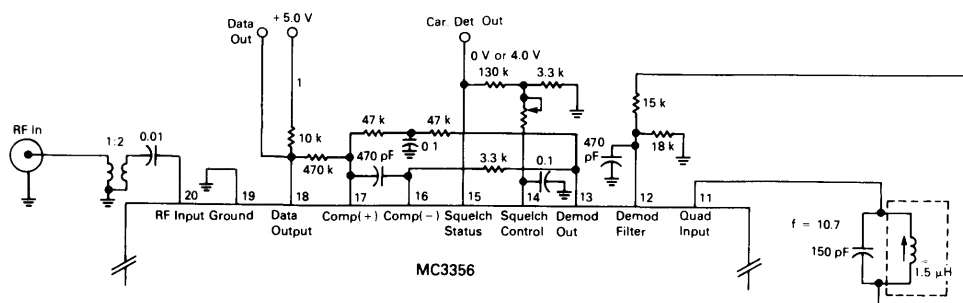
The MC3356 has a separate V_{CC} and ground for the RF and IF sections which allows good external circuit isolation by minimizing common ground paths.

Note that the circuits of Figures 1 and 3 have RF, Oscillator, and IF circuits predominantly referenced to the plus supply rails. Figure 6, on the other hand, shows a suitable means of ground referencing. The two methods produce identical results when carefully executed. It is important to treat Pin 19 as a ground node for either approach. The RF input should be "grounded" to Pin 1 and then the input and the mixer/oscillator grounds (or RF V_{CC} bypasses) should be connected by a low inductance path to Pin 19. IF and detector sections should also

have their bypasses returned by a *separate* path to Pin 19. V_{CC} and RF V_{CC} can be decoupled to minimize feedback, although the configuration of Figure 3 shows a successful implementation on a common 5.0 V supply. Once again, the message is: define a supply node and a ground node and return each section to those nodes by separate, low impedance paths.

The test circuit of Figure 3 has a 3 db limiting level of 30 μ V which can be lowered 6 db by a 1:2 untuned transformer at the input as shown in figures 6 and 7. For applications that require additional sensitivity, an RF amplifier can be added, but with no greater than 20 db gain. This will give a 2.0 to 2.5 μ V sensitivity and any additional gain will reduce receiver dynamic range without improving its sensitivity. Although the test circuit operates at +5.0 V, the mixer/oscillator optimum performance is at +8.0 V to 12 V. A minimum of +8.0 V is recommended in high frequency applications (above 150 MHz), or in PLL applications where the oscillator drives a prescaler.

FIGURE 7 — APPLICATION WITH SELF-ADJUSTING BIAS ON DATA SHAPER

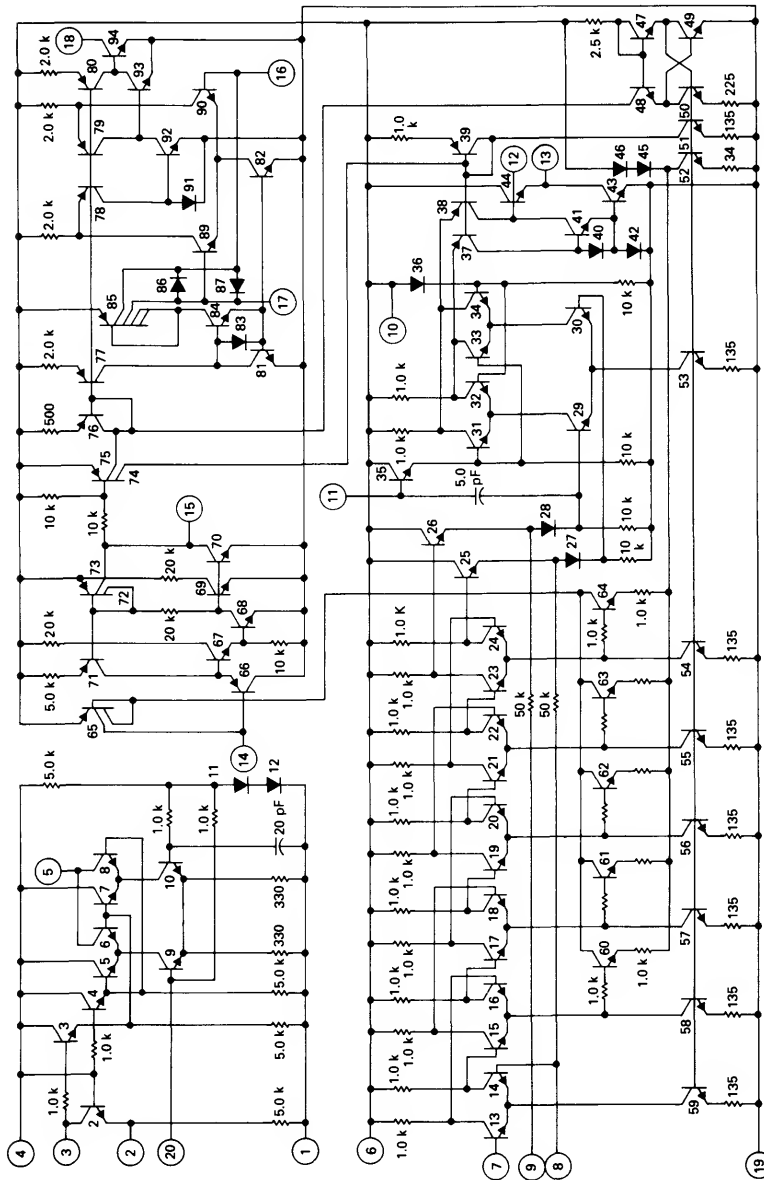
**APPLICATION NOTES (continued)**

Depending on the external circuit, inverted or non-inverted data is available at Pin 18. Inverted data makes the higher frequency in the FSK signal a 'one' when the local oscillator is above the incoming RF. Figure 6 schematic shows the comparator with hysteresis. In this circuit the dc reference voltage at Pin 17 is about the same as the demodulated output voltage (Pin 13) when no signal is present. This type circuit is preferred for systems where the data rates can drop to zero. Some systems have a low frequency limit on the data rate, such as systems using the MC3850 ACIA that has a start or stop bit. This defines the low frequency limit that can appear in the data stream. Figure 6 circuit can then be

changed to a circuit configuration as shown in Figure 7. In Figure 7 the reference voltage for the comparator is derived from the demodulator output through a low pass circuit where τ is much lower than the lowest frequency data rate. This and similar circuits will compensate for small tuning changes (or drift) in the quadrature detector.

Squelch status (Pin 15) goes high (squelch off) when the input signal becomes greater than some preset level set by the resistance between Pin 14 and ground. Hysteresis is added to the circuit externally by the resistance from Pin 14 to Pin 15.

FIGURE 8 — INTERNAL SCHEMATIC



MC3357

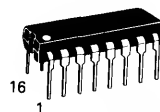
LOW POWER NARROWBAND FM IF

...includes Oscillator, Mixer, Limiting Amplifier, Quadrature Discriminator, Active Filter, Squelch, Scan Control, and Mute Switch. The MC3357 is designed for use in FM dual conversion communications equipment.

- Low Drain Current (3.0 mA (Typ) @ $V_{CC} = 6.0$ Vdc)
- Excellent Sensitivity: Input Limiting Voltage – (-3.0 dB) = $5.0 \mu V$ (Typ)
- Low Number of External Parts Required

**LOW POWER
FM IF**

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**

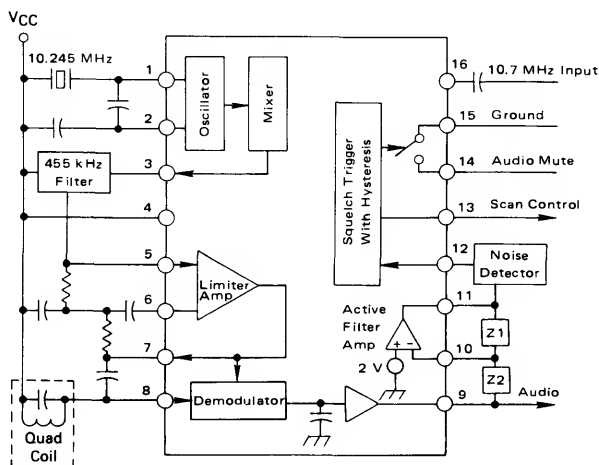


P SUFFIX
PLASTIC PACKAGE
CASE 648

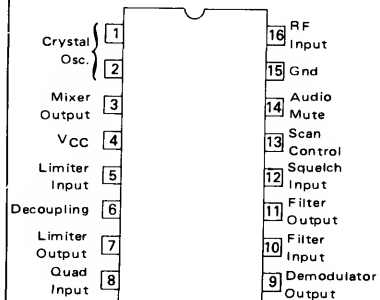


D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO-16)

FIGURE 1 — FUNCTIONAL BLOCK DIAGRAM



PIN CONNECTIONS



MC3357

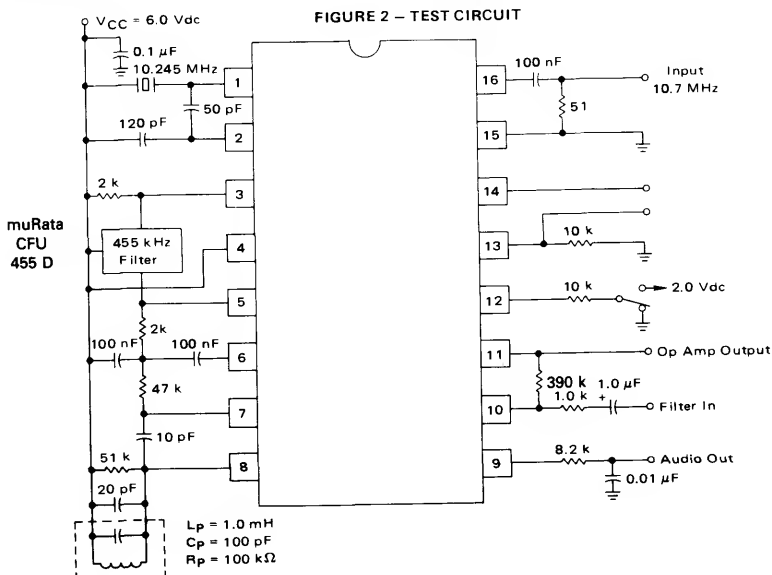
MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4	V _{CC(max)}	12	Vdc
Operating Supply Voltage Range	4	V _{CC}	4 to 8	Vdc
Detector Input Voltage	8	—	1.0	V _{p-p}
Input Voltage (V _{CC} ≥ 6.0 Volts)	16	V _{I6}	1.0	V _{RMS}
Mute Function	14	V _{I4}	-0.5 to 5.0	V _{pk}
Junction Temperature	—	T _J	150	°C
Operating Ambient Temperature Range	—	T _A	-30 to +70	°C
Storage Temperature Range	—	T _{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 6.0 Vdc, f_o = 10.7 MHz, Δf = ± 3.0 kHz, f_{mod} = 1.0 kHz, T_A = 25°C unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
Drain Current	4	—	2.0	—	mA
Squelch Off	—	—	3.0	5.0	—
Squelch On	—	—	—	—	—
Input Limiting Voltage (-3 dB Limiting)	16	—	5.0	10	μV
Detector Output Voltage	9	—	3.0	—	Vdc
Detector Output Impedance	—	—	400	—	Ω
Recovered Audio Output Voltage (V _{in} = 10 mV)	9	200	350	—	mVrms
Filter Gain (10 kHz) (V _{in} = 5 mV)	—	40	46	—	dB
Filter Output Voltage	11	1.8	2.0	2.5	Vdc
Trigger Hysteresis	—	—	100	—	mV
Mute Function Low	14	—	15	50	Ω
Mute Function High	14	1.0	10	—	MΩ
Scan Function Low (Mute Off) (V _{I2} = 2 Vdc)	13	—	0	0.5	Vdc
Scan Function High (Mute On) (V _{I2} = Gnd)	13	5.0	—	—	Vdc
Mixer Conversion Gain	3	—	20	—	dB
Mixer Input Resistance	16	—	3.3	—	kΩ
Mixer Input Capacitance	16	—	2.2	—	pF

8



CIRCUIT DESCRIPTION

The MC3357 is a low power FM IF circuit designed primarily for use in voice communication scanning receivers.

The mixer-oscillator combination converts the input frequency (e.g., 10.7 MHz) down to 455 kHz, where, after external bandpass filtering, most of the amplification is done. The audio is recovered using a conventional quadrature FM detector. The absence of an input signal is indicated by the presence of noise above the desired audio frequencies. This "noise band" is monitored by an active filter and a detector. A squelch trigger circuit indicates the presence of noise (or a tone) by an output which can be used to control scanning. At the same time, an internal switch is operated which can be used to mute the audio.

The oscillator is an internally-biased Colpitts type with the collector, base, and emitter connections at Pins 4, 1, and 2 respectively. A crystal can be used in place of the usual coil.

The mixer is doubly-balanced to reduce spurious responses. The input impedance at Pin 16 is set by a 3.0 k Ω internal biasing resistor and has low capacitance, allowing the circuit to be preceded by a crystal filter. The collector output at Pin 3 must be dc connected to B+, below which it can swing 0.5 V.

After suitable bandpass filtering (ceramic or LC) the signal goes to the input of a five-stage limiter at Pin 5. The output of the limiter at Pin 7 drives a multiplier,

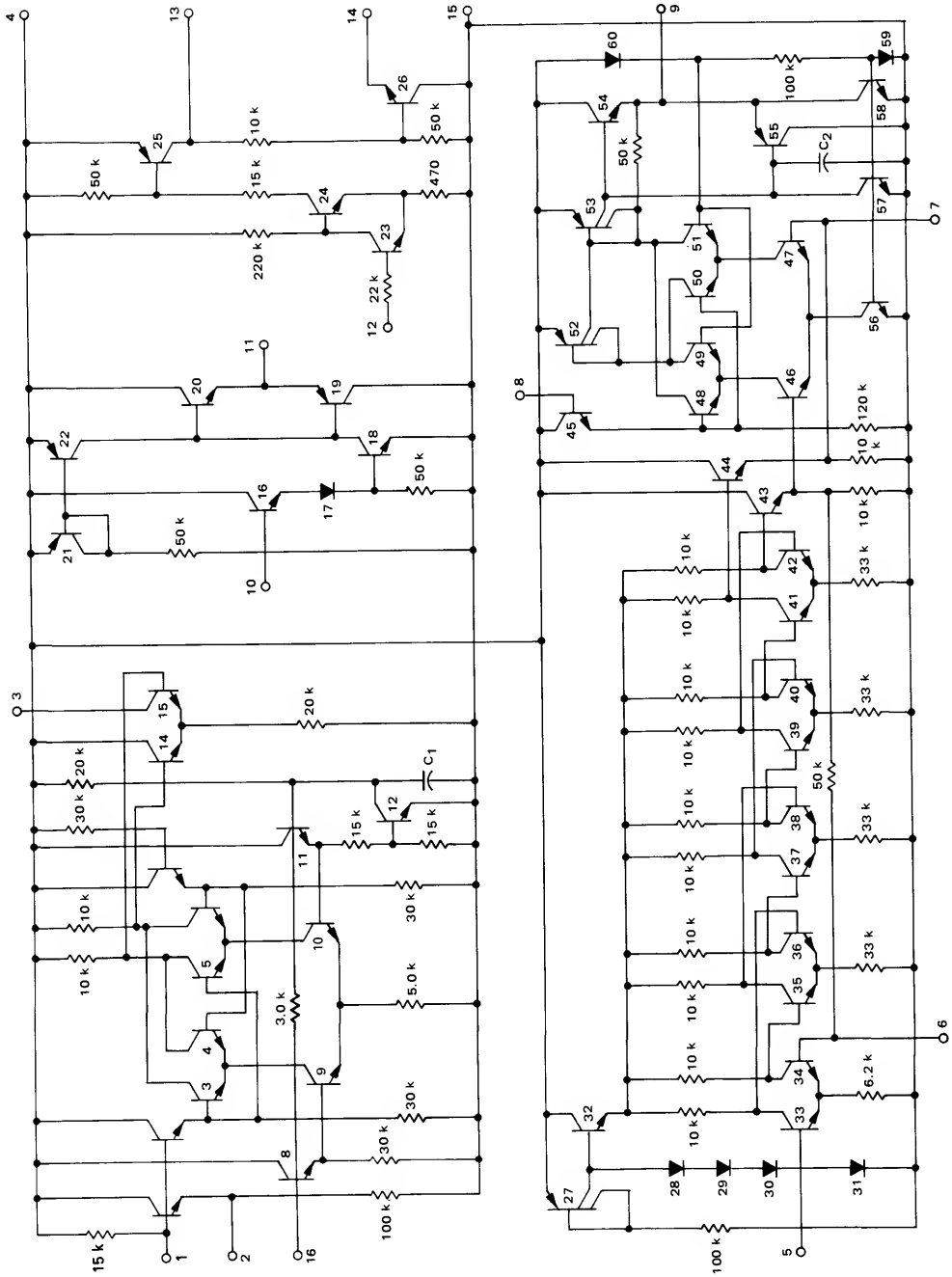
both internally directly, and externally through a quadrature coil, to detect the FM. The output at Pin 7 is also used to supply dc feedback to Pin 5. The other side of the first limiter stage is decoupled at Pin 6.

The recovered audio is partially filtered, then buffered giving an impedance of around 400 Ω at Pin 9. The signal still requires de-emphasis, volume control and further amplification before driving a loudspeaker.

A simple inverting op amp is provided with an output at Pin 11 providing dc bias (externally) to the input at Pin 10 which is referred internally to 2.0 V. A filter can be made with external impedance elements to discriminate between frequencies. With an external AM detector the filtered audio signal can be checked for the presence of noise above the normal audio band, or a tone signal. This information is applied to Pin 12.

An external positive bias to Pin 12 sets up the squelch trigger circuit such that Pin 13 is low at an impedance level of around 60 k Ω , and the audio mute (Pin 14) is open circuit. If Pin 12 is pulled down to 0.7 V by the noise or tone detector, Pin 13 will rise to approximately 0.5 Vdc below supply where it can support a load current of around 500 μ A and Pin 14 is internally short-circuited to ground. There is 100 mV of hysteresis at Pin 12 to prevent jitter. Audio muting is accomplished by connecting Pin 14 to a high-impedance ground-reference point in the audio path between Pin 9 and the audio amplifier.

FIGURE 3 - CIRCUIT SCHEMATIC



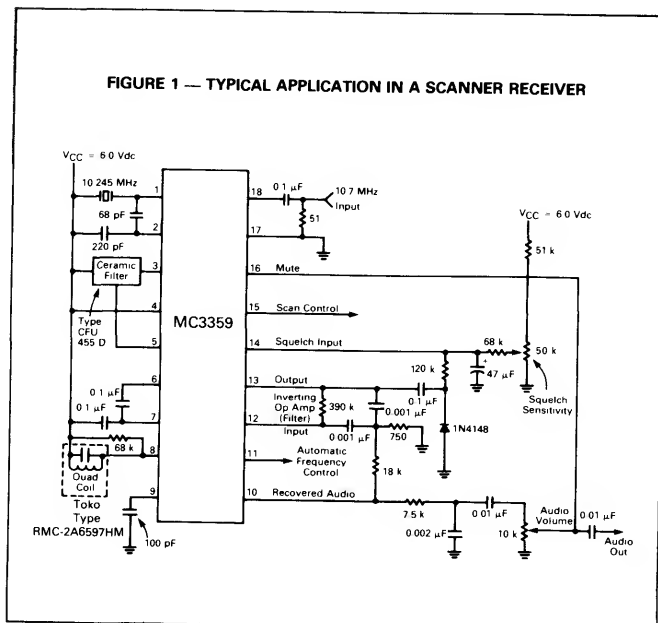
MOTOROLA SEMICONDUCTOR TECHNICAL DATA

LOW POWER NARROWBAND FM IF

... includes oscillator, mixer, limiting amplifier, AFC, quadrature discriminator, op/amp, squelch, scan control, and mute switch. The MC3359 is designed to detect narrowband FM signals using a 455 kHz ceramic filter for use in FM dual conversion communications equipment. The MC3359 is similar to the MC3357 except that the MC3359 has an additional limiting IF stage, an AFC output, and an opposite polarity Broadcast Detector. The MC3359 also requires fewer external parts. For low cost applications requiring V_{CC} below 6.0 V, the MC3361BP, BD are recommended. For applications requiring a fixed, tuned, ceramic quadrature resonator, use the MC3357. For applications requiring dual conversion and RSSI, refer to these devices; MC3335, MC3362 and MC3363.

- Low Drain Current: 3.6 mA (Typ) (α $V_{CC} = 6.0$ Vdc)
- Excellent Sensitivity: Input Limiting Voltage —
—3.0 dB = 2.0 μ V (Typ)
- Low Number of External Parts Required

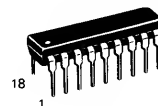
FIGURE 1 — TYPICAL APPLICATION IN A SCANNER RECEIVER



MC3359

HIGH GAIN LOW POWER FM IF

SILICON MONOLITHIC INTEGRATED CIRCUIT

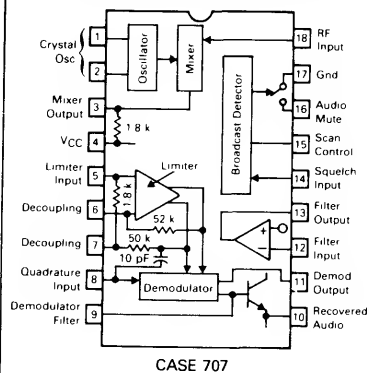


P SUFFIX
PLASTIC PACKAGE
CASE 707

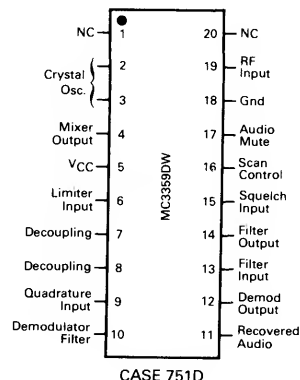
DW SUFFIX
PLASTIC PACKAGE
CASE 751D
(SO-20L)



FIGURE 2 — PIN CONNECTIONS AND
FUNCTIONAL BLOCK DIAGRAM



CASE 707



CASE 751D

MC3359

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4	$V_{CC}(\text{max})$	12	Vdc
Operating Supply Voltage Range	4	V_{CC}	6 to 9	Vdc
Input Voltage ($V_{CC} \geq 6.0$ Volts)	18	V_{18}	1.0	V_{rms}
Mute Function	16	V_{16}	-0.7 to 12	V_{pk}
Junction Temperature	—	T_J	150	$^\circ\text{C}$
Operating Ambient Temperature Range	—	T_A	-30 to +70	$^\circ\text{C}$
Storage Temperature Range	—	T_{stg}	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($V_{CC} = 6.0$ Vdc, $f_o = 10.7$ MHz, $\Delta f = \pm 3.0$ kHz, $f_{\text{mod}} = 1.0$ kHz, 50 Ω source, $T_A = 25^\circ\text{C}$ test circuit of Figure 3, unless otherwise noted)

Characteristics		Min	Typ	Max	Units
Drain Current (Pins 4 and 8)	Squelch Off	—	3.6	6.0	mA
	Squelch On	—	5.4	7.0	
Input for 20 dB Quieting		—	8.0	—	μVrms
Input for -3.0 dB Limiting		—	2.0	—	μVrms
Mixer Voltage Gain (Pin 18 to Pin 3, Open)		—	46	—	
Mixer Third Order Intercept, 50 Ω Input		—	-1.0	—	dBm
Mixer Input Resistance		—	3.6	—	$k\Omega$
Mixer Input Capacitance		—	2.2	—	pF
Recovered Audio, Pin 10 (Input Signal 1.0 mVrms)		450	700	—	mVrms
Detector Center Frequency Slope, Pin 10		—	0.3	—	V/kHz
AFC Center Slope, Pin 11, Unloaded		—	12	—	V/kHz
Filter Gain (test circuit of Figure 3)		40	51	—	dB
Squelch Threshold, Through 10K to Pin 14		—	0.62	—	Vdc
Scan Control Current, Pin 15	Pin 14 — High	—	0.01	1.0	μA
	— Low	2.0	2.4	—	mA
Mute Switch Impedance	Pin 14 — High	—	5.0	10	Ω
	— Low	—	1.5	—	$M\Omega$

8

FIGURE 3 — TEST CIRCUIT

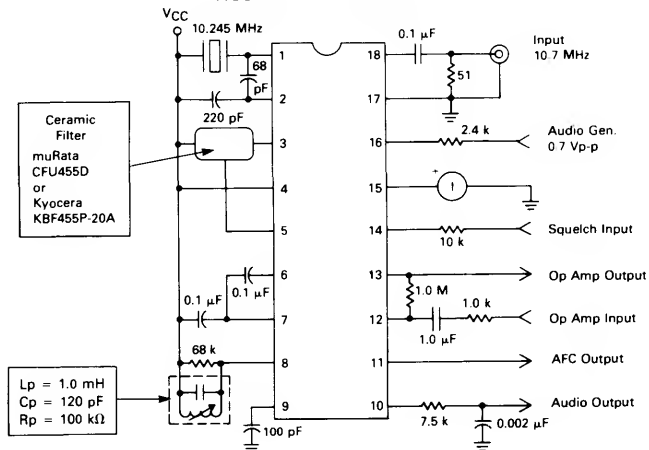


FIGURE 4 — MIXER VOLTAGE GAIN

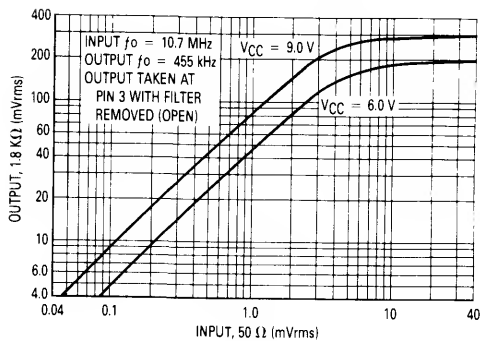


FIGURE 5 — LIMITING I.F. FREQUENCY RESPONSE

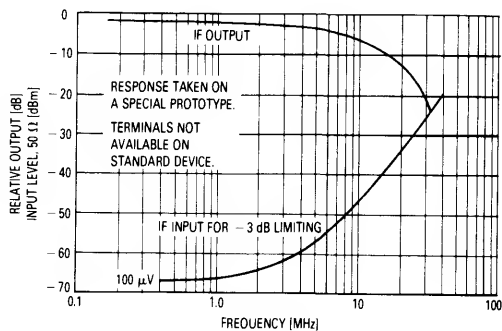


FIGURE 6 — MIXER THIRD ORDER INTERMODULATION PERFORMANCE

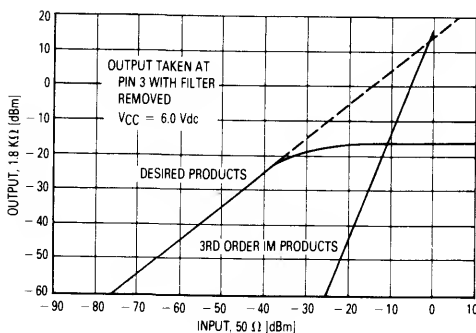


FIGURE 7 — DETECTOR AND AFC RESPONSES

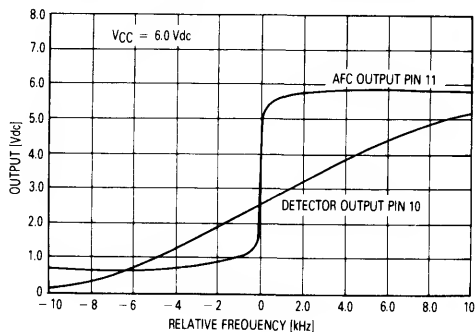


FIGURE 8 — RELATIVE MIXER GAIN

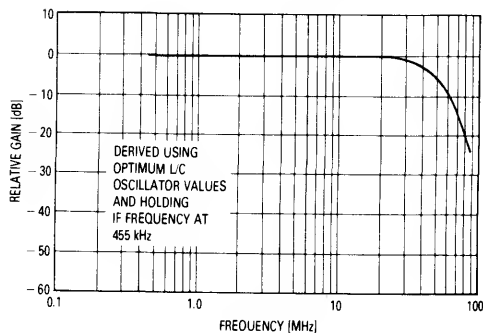


FIGURE 9 — OVERALL GAIN, NOISE, AND A.M. REJECTION

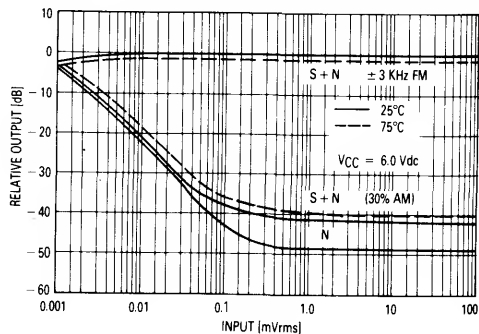


FIGURE 10 — OUTPUT COMPONENTS OF SIGNAL, NOISE, AND DISTORTION

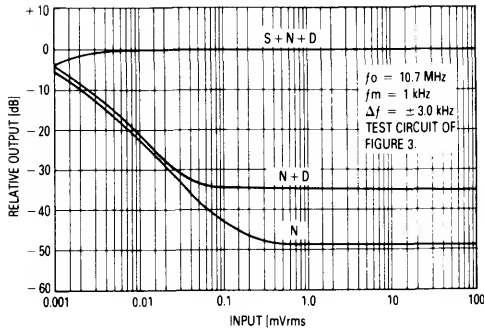


FIGURE 11 — AUDIO OUTPUT AND TOTAL CURRENT DRAIN versus SUPPLY VOLTAGE

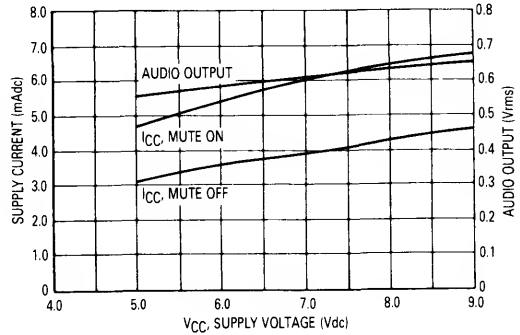


FIGURE 12 — L/C OSCILLATOR, TEMPERATURE AND POWER SUPPLY SENSITIVITY

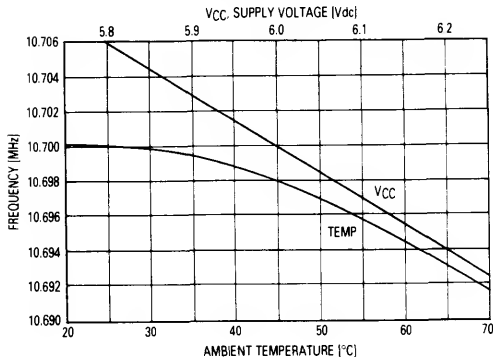


FIGURE 13 — OP AMP GAIN AND PHASE RESPONSE

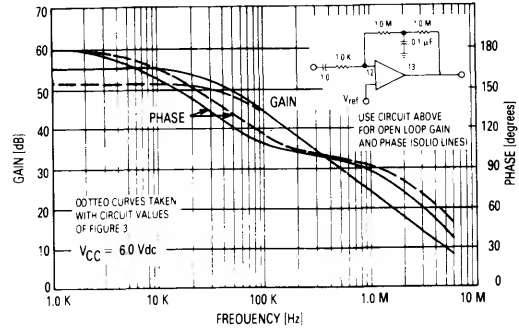


FIGURE 14 — L/C OSCILLATOR RECOMMENDED COMPONENT VALUES

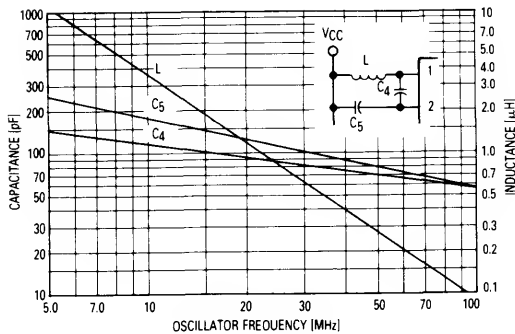
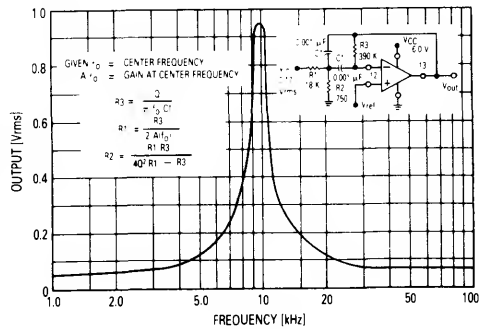


FIGURE 15 — THE OP AMP AS A BANDPASS FILTER





CIRCUIT DESCRIPTION

The MC3359 is a low-power FM IF circuit designed primarily for use in voice-communication scanning receivers. It is also finding a place in narrowband data links.

In the typical application (Figure 1), the mixer-oscillator combination converts the input frequency (10.7 MHz) down to 455 kHz, where, after external bandpass filtering, most of the amplification is done. The audio is recovered using a conventional quadrature FM detector. The absence of an input signal is indicated by the presence of noise above the desired audio frequencies. This "noise band" is monitored by an active filter and a detector. A squelch-trigger circuit indicates the presence of noise (or a tone) by an output which can be used to control scanning. At the same time, an internal switch is operated which can be used to mute the audio.

APPLICATION

The oscillator is an internally biased Colpitts type with the collector, base, and emitter connections at Pin 4, 1, and 2, respectively. The crystal is used in fundamental mode, calibrated for parallel resonance at 32 pF load capacitance. In theory this means that the two capacitors in series should be 32 pF, but in fact much larger values do not significantly affect the oscillator frequency, and provide higher oscillator output.

The oscillator can also be used in the conventional L/C Colpitts configuration without loss of mixer conversion gain. This oscillator is, of course, much more sensitive to voltage and temperature as shown in Figure 12. Guidelines for choosing L and C values are given in Figure 14.

The mixer is doubly balanced to reduce spurious responses. The mixer measurements of Figure 4 and 6 were made using an external 50 Ω source and the internal 1.8 k at Pin 3. Voltage gain curves at several V_{CC} voltages are shown in Figure 4. The Third Order Intercept curves of Figure 6 are shown using the conventional dBm scales. Measured power gain (with the 50 Ω input) is approximately 18 dB but the useful gain is much higher because the mixer input impedance is over 3 k Ω . Most applications will use a 330 Ω 10.7 MHz crystal filter ahead of the mixer. For higher frequencies, the relative mixer gain is given in Figure 8.

Following the mixer, a ceramic bandpass filter is recommended. The 455 kHz types come in bandwidths from ± 2 kHz to ± 15 kHz and have input and output impedances of 1.5 k to 2.0 k. For this reason, the Pin 5 input to the 6 stage limiting IF

has an internal 1.8 k resistor. The IF has a 3 dB limiting sensitivity of approximately 100 μ V at Pin 5 and a useful frequency range of about 5 MHz as shown in Figure 5. The frequency limitation is due to the high resistance values in the IF, which were necessary to meet the low power requirement. The output of the limiter is internally connected to the quadrature detector, including the 10 pF quadrature capacitor. Only a parallel L/C is needed externally from Pin 8 to V_{CC} . A shunt resistance can be added to widen the peak separation of the quadrature detector.

The detector output is amplified and buffered to the audio output, Pin 10, which has an output impedance of approximately 300 Ω . Pin 9 provides a high impedance (50 k) point in the output amplifier for application of a filter or de-emphasis capacitor. Pin 11 is the AFC output, with high gain and high output impedance (1 M). If not needed, it should be grounded, or it can be connected to Pin 9 to double the recovered audio. The detector and AFC responses are shown in Figure 7.

Overall performance of the MC3359 from mixer input to audio output is shown in Figure 9 and 10. The MC3359 can also be operated in "single conversion" equipment; i.e., the mixer can be used as a 455 kHz amplifier. The oscillator is disabled by connecting Pin 1 to Pin 2. In this mode the overall performance is identical to the 10.7 MHz results of Figure 9.

A simple inverting op amp is provided with an output at Pin 13 providing dc bias (externally) to the input at Pin 12, which is referred internally to 2.0 V. A filter can be made with external impedance elements to discriminate between frequencies. With an external AM detector, the filtered audio signal can be checked for the presence of either noise above the normal audio, or a tone signal.

The open loop response of this op amp is given in Figure 13. Bandpass filter design information is provided in Figure 15.

A low bias to Pin 14 sets up the squelch-trigger circuit such that Pin 15 is high, a source of at least 2.0 mA, and the audio mute (Pin 16) is open-circuit. If Pin 14 is raised to 0.7 V by the noise or tone detector, Pin 15 becomes open circuit and Pin 16 is internally short circuited to ground. There is no hysteresis. Audio muting is accomplished by connecting Pin 16 to a high-impedance ground-reference point in the audio path between Pin 10 and the audio amplifier. No dc voltage is needed, in fact it is not desirable because audio "thump" would result during the muting function. Signal swing greater than 0.7 V below ground on Pin 16 should be avoided.

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Advance Information

LOW POWER NARROWBAND FM IF

... includes Oscillator, Mixer, Limiting Amplifier, Quadrature Discriminator, Active Filter, Squelch, Scan Control, and Mute Switch. The MC3361B is designed for use in FM dual conversion communications equipment.

- Operates from 2.0 V to 8.0 V
- Low Drain Current 3.9 mA Typ @ $V_{CC} = 4.0$ Vdc
- Excellent Sensitivity: Input Limiting Voltage —
-3.0 dB = 2.6 μ V Typ
- Low Number of External Parts Required

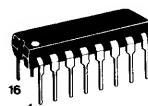
MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4	$V_{CC(max)}$	10	Vdc
Operating Supply Voltage Range	4	V_{CC}	2.0 to 8.0	Vdc
Detector Input Voltage	8	—	1.0	Vp-p
Input Voltage ($V_{CC} \geq 4.0$ Volts)	16	V_{I1}	1.0	V_{rms}
Mute Function	14	V_{I4}	-0.5 to 5.0	V_{pk}
Junction Temperature	—	T_J	150	$^\circ\text{C}$
Operating Ambient Temperature Range	—	T_A	-30 to +70	$^\circ\text{C}$
Storage Temperature Range	—	T_{stg}	-65 to +150	$^\circ\text{C}$

MC3361B

LOW POWER FM IF

SILICON MONOLITHIC INTEGRATED CIRCUIT

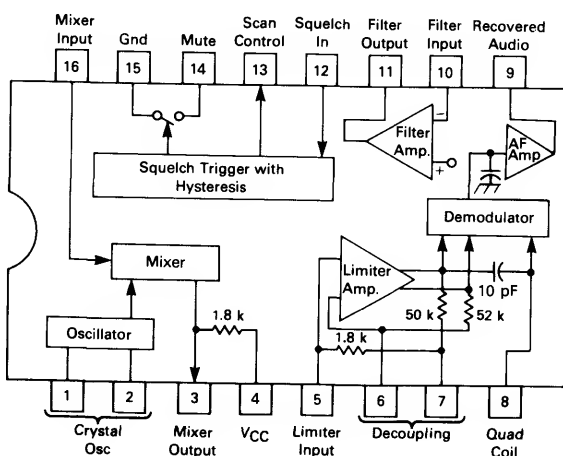


P SUFFIX
PLASTIC PACKAGE
CASE 648

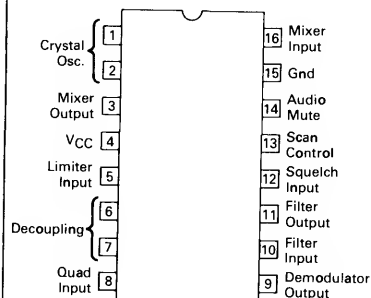


D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO-16)

FIGURE 1 — FUNCTIONAL BLOCK DIAGRAM



PIN CONNECTIONS



This document contains information on a new product. Specifications and information herein are subject to change without notice.

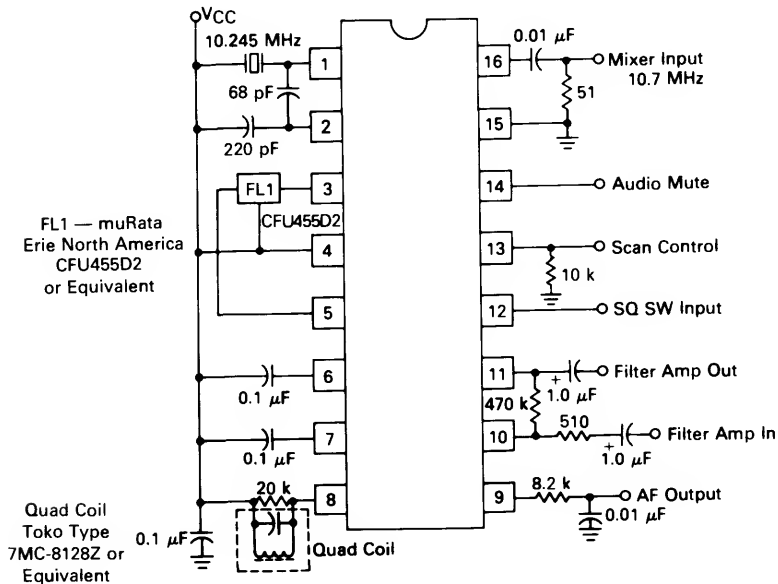
MC3361B

ELECTRICAL CHARACTERISTICS ($V_{CC} = 4.0$ Vdc, $f_o = 10.7$ MHz, $\Delta f = \pm 3.0$ kHz, $f_{mod} = 1.0$ kHz, $T_A = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Units
Drain Current (No Signal) Squelch Off Squelch On	4	2.9 4.4	3.9 5.4	4.9 6.4	mA
Input Limiting Voltage (-3.0 dB Limiting)	16	—	2.6	6.0	μV
Recovered Output Voltage (No Input Signal)	9	60	120	250	mVrms
Detector Output Impedance	—	—	450	—	Ω
Total Harmonic Distortion	9	—	0.86	—	%
Drop Voltage AF Gain Loss	9	-3.0	-0.6	—	dB
Recovered Audio Output Voltage ($V_{in} = 10$ mV)	9	130	160	200	mVrms
Filter Gain (10 kHz) ($V_{in} = 0.3$ mV)	—	40	50	—	dB
Filter Output Voltage	11	1.0	1.3	1.6	Vdc
Trigger Hysteresis	—	—	45	100	mV
Mute Function Low	14	—	30	50	Ω
Mute Function High	14	1.0	11	—	M Ω
Scan Function Low (Mute Off) ($V_{12} = 1.0$ Vdc)	13	—	0	0.4	Vdc
Scan Function High (Mute On) ($V_{12} = \text{Gnd}$)	13	3.0	3.6	—	Vdc
Mixer Conversion Gain	3	—	28	—	dB
Mixer Input Resistance	16	—	3.3	—	k Ω
Mixer Input Capacitance	16	—	2.2	—	pF

8

FIGURE 2 — TEST CIRCUIT



LOW-POWER DUAL CONVERSION FM RECEIVER

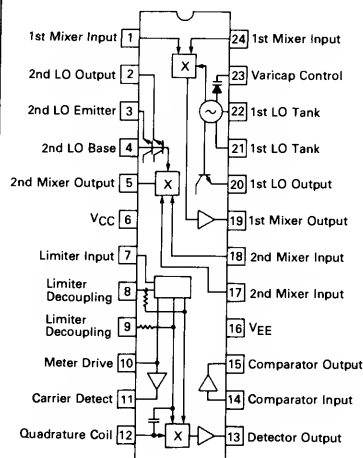
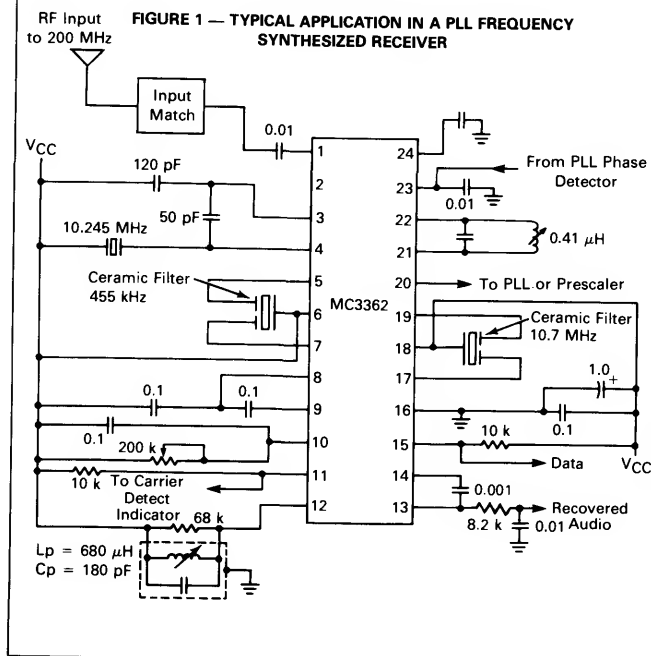
SILICON MONOLITHIC INTEGRATED CIRCUIT

P SUFFIX
PLASTIC PACKAGE
CASE 724

- DW SUFFIX**
PLASTIC PACKAGE
CASE 751E
(SO-24L)

8

FIGURE 2 — PIN CONNECTIONS AND FUNCTIONAL BLOCK DIAGRAM



8

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage (See Diagram)	6	V _{CC(max)}	7.0	Vdc
Operating Supply Voltage Range (Recommended)	6	V _{CC}	2.0 to 6.0	Vdc
Input Voltage (V _{CC} ≥ 5.0 Vdc)	1, 24	V ₁₋₂₄	1.0	Vrms
Junction Temperature	—	T _J	150	°C
Operating Ambient Temperature Range	—	T _A	− 40 to + 85	°C
Storage Temperature Range	—	T _{stg}	− 65 to + 150	°C

Characteristic	Pin	Min	Typ	Max	Units
Drain Current (Carrier Detect Low — See Figure 5)	6	—	4.5	7.0	mA
Input for –3.0 dB Limiting	—	—	0.7	2.0	μVrms
Recovered Audio (RF signal level = 10 mV)	13	—	350	—	mVrms
Noise Output (RF signal level = 0 mV)	13	—	250	—	mVrms
Carrier Detect Threshold (below V_{CC})	10	—	0.64	—	Vdc
Meter Drive Slope	10	—	100	—	nA/dB
Input for 20 dB (S + N)/N (See Figure 7)	—	—	0.7	—	μVrms
First Mixer 3rd Order Intercept (Input)	—	—	–22	—	dBm
First Mixer Input Resistance (Rp)	—	—	690	—	Ω
First Mixer Input Capacitance (Cp)	—	—	7.2	—	pF
First Mixer Conversion Voltage Gain	—	—	18	—	dB
Second Mixer Conversion Voltage Gain	—	—	21	—	dB
Detector Output Resistance	13	—	1.4	—	k Ω

MC3362

FIGURE 4 — I_Q METER versus INPUT

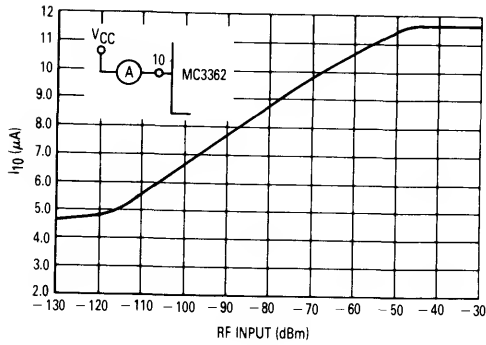


FIGURE 5 — DRAIN CURRENT, RECOVERED AUDIO versus SUPPLY

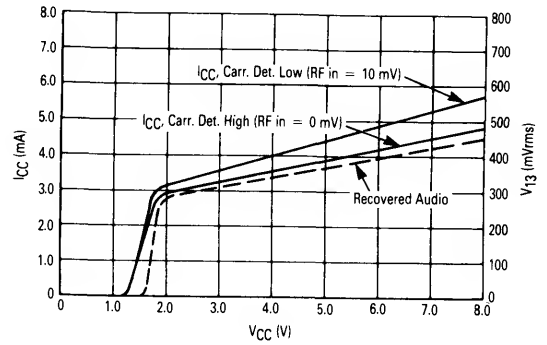


FIGURE 6 — SIGNAL LEVELS

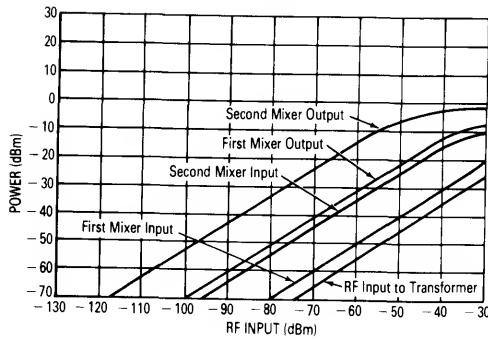


FIGURE 7 — $S+N$, N , AMR versus INPUT

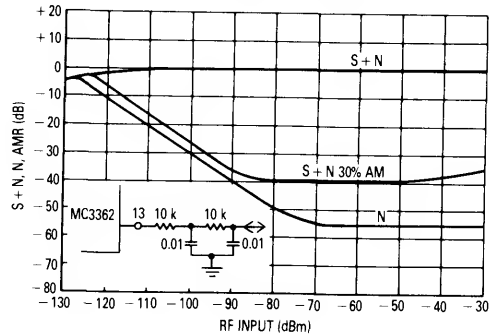


FIGURE 8 — 1ST MIXER 3RD ORDER INTERMODULATION

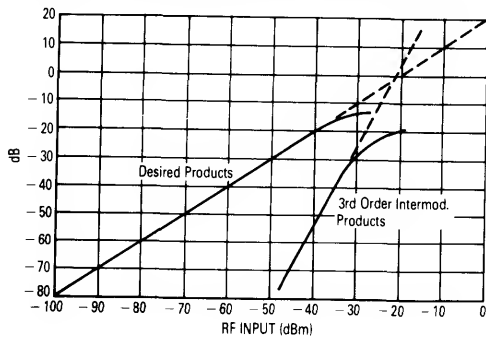
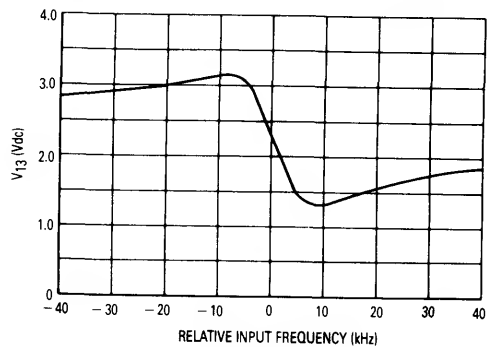


FIGURE 9 — DETECTOR OUTPUT versus FREQUENCY



MC3362

FIGURE 10 — PC BOARD TEST CIRCUIT

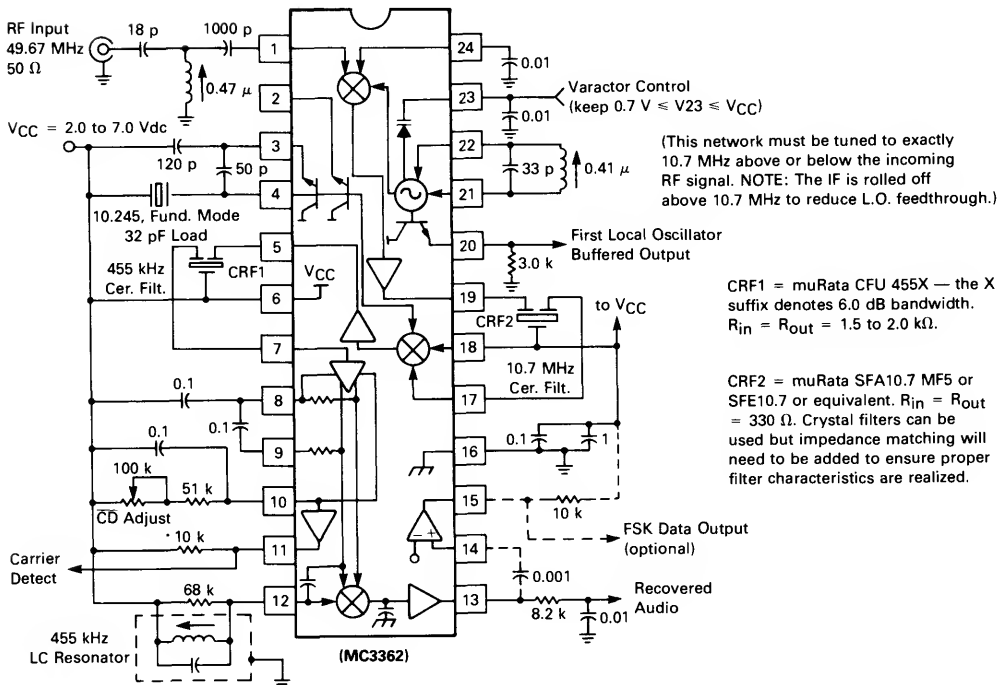
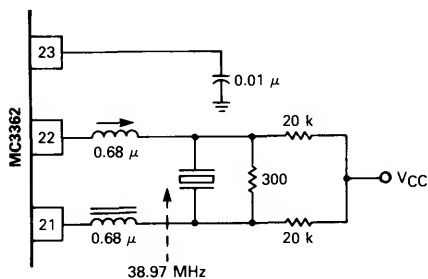
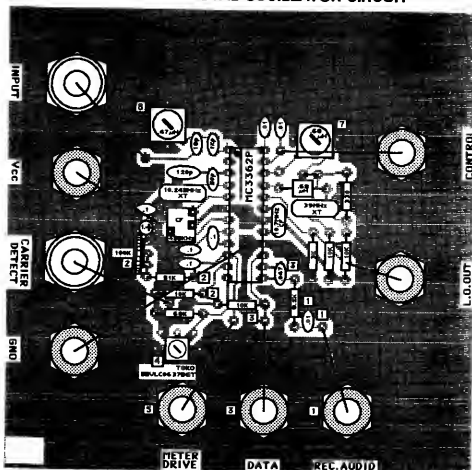


FIGURE 10A — CRYSTAL OSCILLATOR CONFIGURATION FOR SINGLE CHANNEL APPLICATION



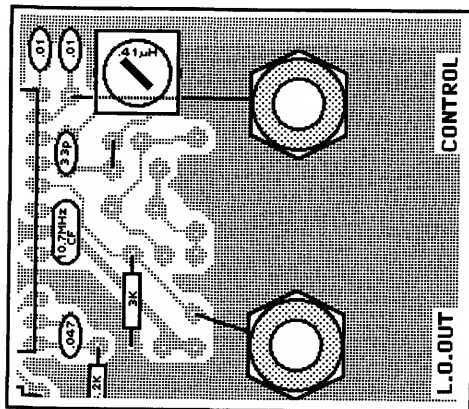
Crystal used is series mode resonant (no load capacity specified), 3rd overtone. This method has not proven adequate for fundamental mode, 5th or 7th overtone crystals. The inductor and capacitor will need to be changed for other frequency crystals. See AN980 for further information.

FIGURE 11 — COMPONENT PLACEMENT VIEW
SHOWING CRYSTAL OSCILLATOR CIRCUIT

NOTES:

1. Recovered Audio components may be deleted when using data output.
2. Carrier Detect components must be deleted in order to obtain linear Meter Drive output. With these components in place the Meter Drive outputs serve only to trip the Carrier Detect indicator.
3. Data Output components should be deleted in applications where only audio modulation is used. For combined audio/data applications, the 0.047 μ F coupling capacitor will add distortion to the audio, so a pull-down resistor at pin 13 may be required.
4. Toko 5SVLC0637BGT 5mm quadrature coil for miniaturization. Use Toko RMC2A6597HM high quality 10mm coil for maximum recovered signal at pin 13.

FIGURE 11A — LC OSCILLATOR COMPONENT VIEW



5. Meter Drive cannot be used simultaneously with Carrier Detect output. For analog meter drive, remove components labelled "2" and measure meter current (4–12 μ A) through ammeter to VCC.
6. Either type of oscillator circuit may be used with any output circuit configuration.
7. LC Oscillator Coil: Coilcraft UNI 10/42 10.9 turns, 0.41 μ H Crystal Oscillator circuit: trim coil, 0.68 μ H, Toko B199SNT1051Z
8. 0.47 μ H, Toko B199SNT1050Z. Input LC network used to match first mixer input impedance to 50 Ω .

8

CIRCUIT DESCRIPTION

The MC3362 is a complete FM narrowband receiver from antenna input to audio preamp output. The low voltage dual conversion design yields low power drain, excellent sensitivity and good image rejection in narrowband voice and data link applications.

In the typical application (Figure 1), the first mixer amplifies the signal and converts the RF input to 10.7 MHz. This IF signal is filtered externally and fed into the second mixer, which further amplifies the signal and converts it to a 455 kHz IF signal. After external band-pass filtering, the low IF is fed into the limiting amplifier and detection circuitry. The audio is recovered using a conventional quadrature detector. Twice-IF filtering is provided internally.

The input signal level is monitored by meter drive circuitry which detects the amount of limiting in the limiting amplifier. The voltage at the meter drive pin determines the state of the carrier detect output, which is active low.

APPLICATION

The first local oscillator can be run using a free-running LC tank, as a VCO using PLL synthesis, or driven from an external crystal oscillator. It has been run to 190 MHz.* A buffered output is available at Pin 20. The second local oscillator is a common base Colpitts type which is typically run at 10.245 MHz under crystal control. A buffered output is available at Pin 2. Pins 2 and 3 are interchangeable.

The mixers are doubly balanced to reduce spurious responses. The first and second mixers have conversion gains of 18 dB and 22 dB (typical), respectively, as seen in Figure 6. Mixer gain is stable with respect to supply voltage. For both conversions, the mixer impedances and pin layout are designed to allow the user to employ low cost, readily available ceramic filters. Overall sensitivity and AM rejection are shown in Figure 7. The input level for 20 dB (S+N)/N is 0.7 μ V using the two-pole post-detection filter pictured.

*If the first local oscillator (Pins 21 and/or 22) is driven from a strong external source (100 mVrms), the mixer can be used to over 450 MHz.

MC3362

Following the first mixer, a 10.7 MHz ceramic bandpass filter is recommended. The 10.7 MHz filtered signal is then fed into one second mixer input pin, the other input pin being connected to V_{CC} . Pin 6 (V_{CC}) is treated as a common point for emitter-driven signals.

The 455 kHz IF is typically filtered using a ceramic bandpass filter then fed into the limiter input pin. The limiter has $10 \mu V$ sensitivity for -3.0 dB limiting, flat to 1.0 MHz.

The output of the limiter is internally connected to the quadrature detector, including a quadrature capacitor. A parallel LC tank is needed externally from Pin 12 to V_{CC} . A 68 k Ω shunt resistance is included which determines the peak separation of the quadrature detector; a smaller value will increase the spacing and linearity but decrease recovered audio and sensitivity.

A data shaping circuit is available and can be coupled to the recovered audio output of Pin 13. The circuit is a comparator which is designed to detect zero

crossings of FSK modulation. Data rates are typically limited to 1200 baud to ensure data integrity and avoid adjacent channel "splatter." Hysteresis is available by connecting a high valued resistor from Pin 15 to Pin 14. Values below 120 k Ω are not recommended as the input signal cannot overcome the hysteresis.

The meter drive circuitry detects input signal level by monitoring the limiting amplifier stages. Figure 4 shows the unloaded current at Pin 10 versus input power. The meter drive current can be used directly (RSSI) or can be used to trip the carrier detect circuit at a specified input power. To do this, pick an RF trip level in dBm. Read the corresponding current from Figure 4 and pick a resistor such that:

$$R_{10} = 0.64 V_{dc} / I_{10}$$

Hysteresis is available by connecting a high valued resistor R_H between Pins 10 and 11. The formula is:

$$\text{Hysteresis} = V_{CC} / (R_H \times 10^{-7}) \text{ dB}$$

FIGURE 12 — CIRCUIT SIDE VIEW

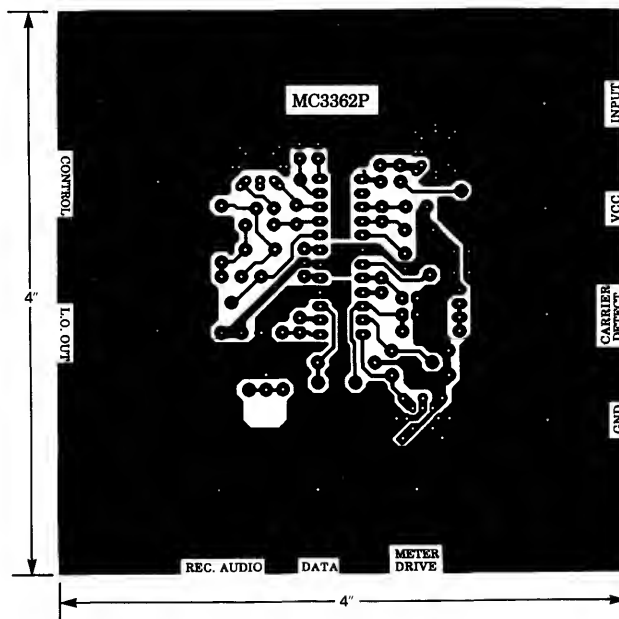
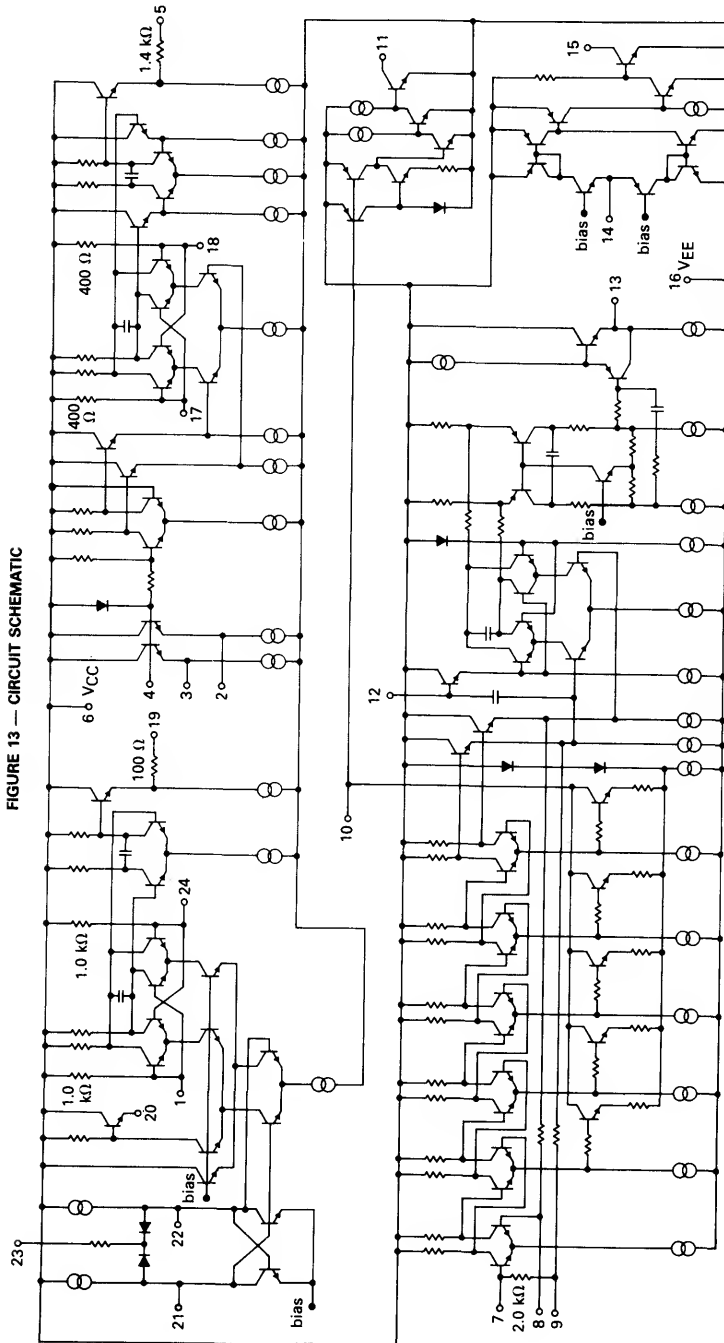


FIGURE 13 — CIRCUIT SCHEMATIC



MC3363

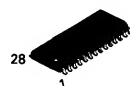
LOW POWER DUAL CONVERSION FM RECEIVER

The MC3363 is a single chip narrowband VHF FM radio receiver. It is a dual conversion receiver with RF amplifier transistor, oscillators, mixers, quadrature detector, meter drive/carrier detect and mute circuitry. The MC3363 also has a buffered first local oscillator output for use with frequency synthesizers, and a data slicing comparator for FSK detection.

- Wide Input Bandwidth — 200 MHz Using Internal Local Oscillator
 — 450 MHz Using External Local Oscillator
- RF Amplifier Transistor
- Muting Operational Amplifier
- Complete Dual Conversion
- Low Voltage: $V_{CC} = 2.0$ V to 6.0 Vdc
- Low Drain Current: $I_{CC} = 3.6$ mA (Typ) at $V_{CC} = 3.0$ V, Excluding RF Amplifier Transistor
- Excellent Sensitivity: Input $0.3 \mu\text{V}$ (Typ) for 12 dB SINAD Using Internal RF Amplifier Transistor
- Data Shaping Comparator
- Received Signal Strength Indicator (RSSI) with 60 dB Dynamic Range
- Low Number of External Parts Required
- Manufactured in Motorola's MOSAIC Process Technology

LOW POWER DUAL CONVERSION FM RECEIVER

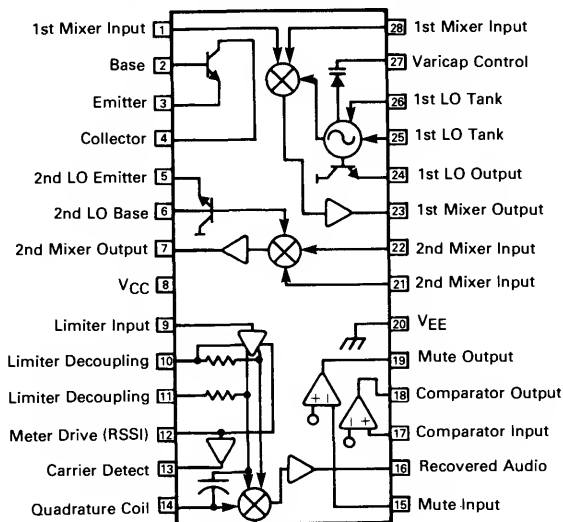
**SILICON MONOLITHIC
 INTEGRATED CIRCUIT**



DW SUFFIX
 PLASTIC PACKAGE
 CASE 751F
 (SO-28L)

8

**FIGURE 1 — PIN CONNECTIONS AND FUNCTIONAL
 BLOCK DIAGRAM**



MC3363

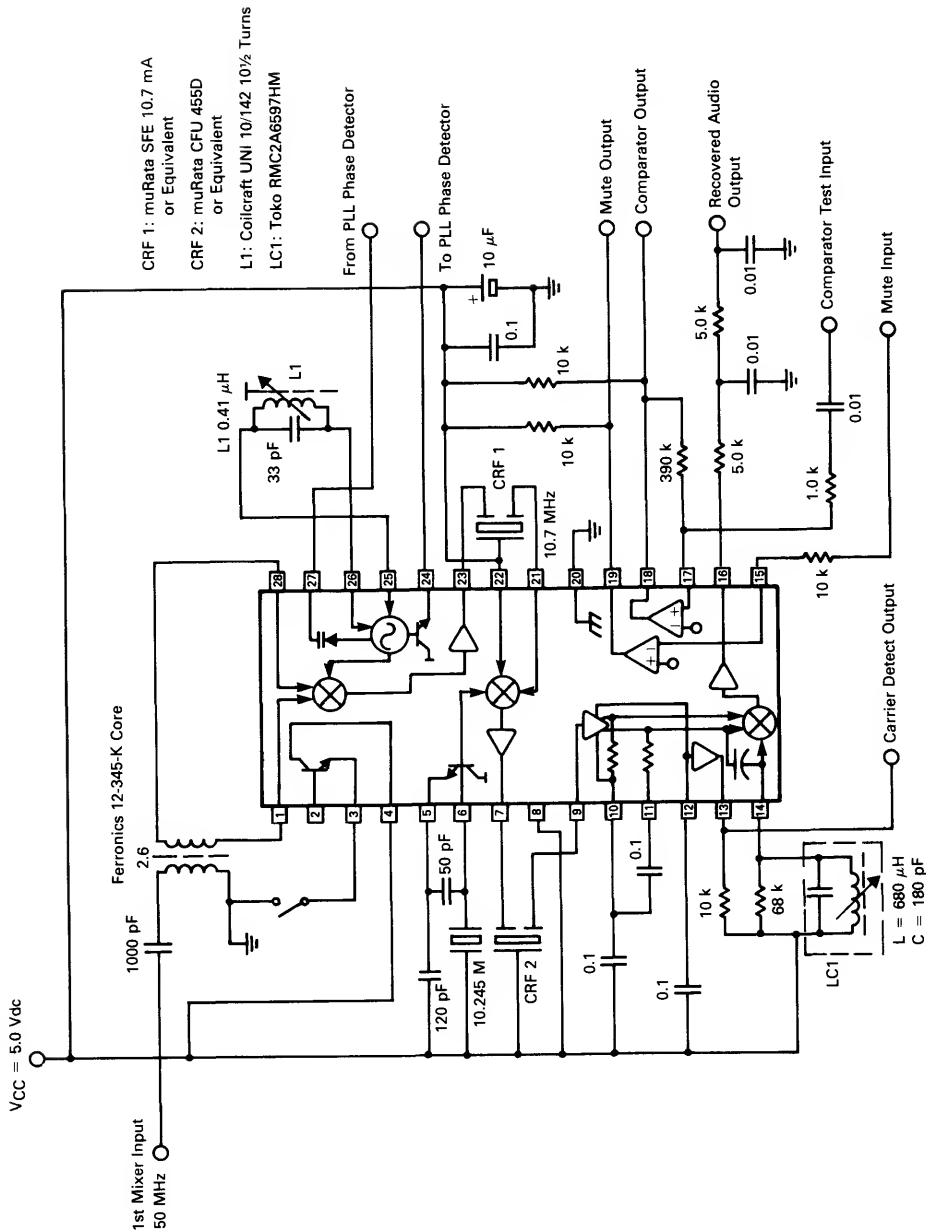
MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	8	$V_{CC(max)}$	7.0	Vdc
Operating Supply Voltage Range (Recommended)	8	V_{CC}	2.0 to 6.0	Vdc
Input Voltage ($V_{CC} = 5.0$ Vdc)	1, 28	V_{1-28}	1.0	Vrms
Mute Output Voltage	19	V_{19}	-0.7 to 8.0	Vpk
Junction Temperature	—	T_J	150	$^\circ\text{C}$
Operating Ambient Temperature Range	—	T_A	-40 to +85	$^\circ\text{C}$
Storage Temperature Range	—	T_{stg}	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0$ Vdc, $f_o = 49.7$ MHz, Deviation = ± 3.0 kHz, $T_A = 25^\circ\text{C}$, Mod 1.0 kHz, test circuit of Figure 2 unless otherwise noted)

Characteristic	Pin	Min	Typ	Max	Unit
Drain Current (Carrier Detect Low)	8	—	4.5	8.0	mA
-3.0 dB Limiting Sensitivity (RF Amplifier Not Used)	—	—	0.7	2.0	μVrms
20 dB S/N Sensitivity (RF Amplifier Not Used)	—	—	1.0	—	μVrms
1st Mixer Input Resistance (Parallel — R_p)	1, 28	—	690	—	Ohm
1st Mixer Input Capacitance (Parallel — C_p)	1, 28	—	7.2	—	pF
1st Mixer Conversion Voltage Gain (A_{VC1} , Open Circuit)	—	—	18	—	dB
2nd Mixer Conversion Voltage Gain (A_{VC2} , Open Circuit)	—	—	21	—	dB
2nd Mixer Input Sensitivity (20 dB S/N) (10.7 MHz i/p)	21	—	10	—	μVrms
Limiter Input Sensitivity (20 dB S/N) (455 kHz i/p)	9	—	100	—	μVrms
RF Transistor DC Current Drain	4	1.0	1.5	2.5	mA _{dc}
Recovered Audio (RF Signal Level = 1.0 mV)	16	120	200	—	mVrms
Noise Output Level (RF Signal = 0 mV)	16	—	70	—	mVrms
THD of Recovered Audio (RF Signal = 1.0 mV)	16	—	2%	—	%
Detector Output Impedance	16	—	400	—	Ohm
Data (Comparator) Output Voltage — High	18	—	—	V_{CC}	Vdc
— Low	18	0.1	0.1	—	Vdc
Data (Comparator) Threshold Voltage Difference	17	70	110	150	mV
Meter Drive Slope	12	70	100	135	nA/dB
Carrier Detect Threshold (Below V_{CC})	12	0.53	0.64	0.77	Vdc
Mute Output Impedance — High	19	—	10	—	Mohm
— Low	19	—	25	—	Ohm

FIGURE 2 — TEST CIRCUIT



CIRCUIT DESCRIPTION

The MC3363 is a complete FM narrowband receiver from RF amplifier to audio preamp output. The low voltage dual conversion design yields low power drain, excellent sensitivity and good image rejection in narrowband voice and data link applications.

In the typical application, the input RF signal is amplified by the RF transistor and then the first mixer amplifies the signal and converts the RF input to 10.7 MHz. This IF signal is filtered externally and fed into the second mixer, which further amplifies the signal and converts it to a 455 kHz IF signal. After external bandpass filtering, the low IF is fed into the limiting amplifier and detection circuitry. The audio is recovered using a conventional quadrature detector. Twice-IF filtering is provided internally.

The input signal level is monitored by meter drive circuitry which detects the amount of limiting in the limiting amplifier. The voltage at the meter drive pin determines the state of the carrier detect output, which is active low.

APPLICATION

The first local oscillator is designed to serve as the VCO in a PLL frequency synthesized receiver. The MC3363 can operate together with the MC145166/7 to provide a two-chip ten channel frequency synthesized receiver in the 46/49 cordless telephone band. The MC3363 can also be used with the MC14515X series of CMOS PLL synthesizers and MC120XX series of ECL prescalers in VHF frequency synthesized applications to 200 MHz.

For single channel applications the first local oscillator can be crystal controlled. The circuit of Figure 4 has been used successfully up to 60 MHz. For higher frequencies an external oscillator signal can be injected into Pins 25 and/or 26 — a level of approximately 100 mVrms is recommended. The first mixer's transfer characteristic is essentially flat to 450 MHz when this approach is used (keeping a constant 10.7 MHz IF frequency). The second local oscillator is a Colpitts type which is typically run at 10.245 MHz under crystal control.

The mixers are doubly balanced to reduce spurious responses. The first and second mixers have conversion gains of 18 dB and 21 dB (typical), respectively. Mixer gain is stable with respect to supply voltage. For both conversions, the mixer impedances and pin layout are designed to allow the user to employ low cost, readily available ceramic filters.

Following the first mixer, a 10.7 MHz ceramic bandpass filter is recommended. The 10.7 MHz filtered signal is then fed into the second mixer input Pin 21, the other input Pin 22 being connected to VCC.

The 455 kHz IF is filtered by a ceramic narrow bandpass filter then fed into the limiter input Pin 9. The limiter has 10 μ V sensitivity for -3.0 dB limiting, flat to 1.0 MHz.

The output of the limiter is internally connected to the quadrature detector, including a quadrature capacitor. A parallel LC tank is needed externally from Pin 14 to VCC. A 68 kOhm shunt resistance is included which determines the peak separation of the quadrature detector; a smaller value will lower the Q and expand the deviation range and linearity, but decrease recovered audio and sensitivity.

A data shaping circuit is available and can be coupled to the recovered audio output of Pin 16. The circuit is a comparator which is designed to detect zero crossings of FSK modulation. Data rates of 2000 to 35000 baud are detectable using the comparator. Best sensitivity is obtained when data rates are limited to 1200 baud maximum. Hysteresis is available by connecting a high-valued resistor from Pin 17 to Pin 18. Values below 120 kOhm are not recommended as the input signal cannot overcome the hysteresis.

The meter drive circuitry detects input signal level by monitoring the limiting of the limiting amplifier stages. Figure 5 shows the unloaded current at Pin 12 versus input power. The meter drive current can be used directly (RSSI) or can be used to trip the carrier detect circuit at a specified input power.

A muting op amp is provided and can be triggered by the carrier detect output (Pin 13). This provides a carrier level triggered squelch circuit which is activated when the RF input at the desired input frequency falls below a preset level. The level at which this occurs is determined by the resistor placed between the meter drive output (Pin 12) and VCC. Values between 80-130 kOhms are recommended. This type of squelch is pictured in Figures 3 and 4.

Hysteresis is available by connecting a high-valued resistor Rh between Pins 12 and 13. The formula is:

$$\text{Hyst} = V_{CC} / (R_h \times 10^{-7}) \text{ dB}$$

The meter drive can also be used directly to drive a meter or to provide AGC. A current to voltage converter or other linear buffer will be needed for this application.

A second possible application of the op amp would be in a noise triggered squelch circuit, similar to that used with the MC3357/MC3359/MC3361B FM IFs. In this case the op amp would serve as an active noise filter, the output of which would be rectified and compared to a reference on a squelch gate. The MC3363 does not have a dedicated squelch gate, but the NPN RF input stage or data shaping comparator might be used to provide this function if available. The op amp is a basic type with the inverting input and the output available. This application frees the meter drive to allow it to be used as a linear signal strength monitor.

The circuit of Figure 4 is a complete 50 MHz receiver from antenna input to audio preamp output. It uses few components and has good performance. The receiver operates on a single channel and has input sensitivity of <0.3 μ V for 12 dB SINAD.

NOTE: For further application and design information, refer to AN980.

FIGURE 3 — TYPICAL APPLICATION IN A PLL FREQUENCY SYNTHESIZED RECEIVER

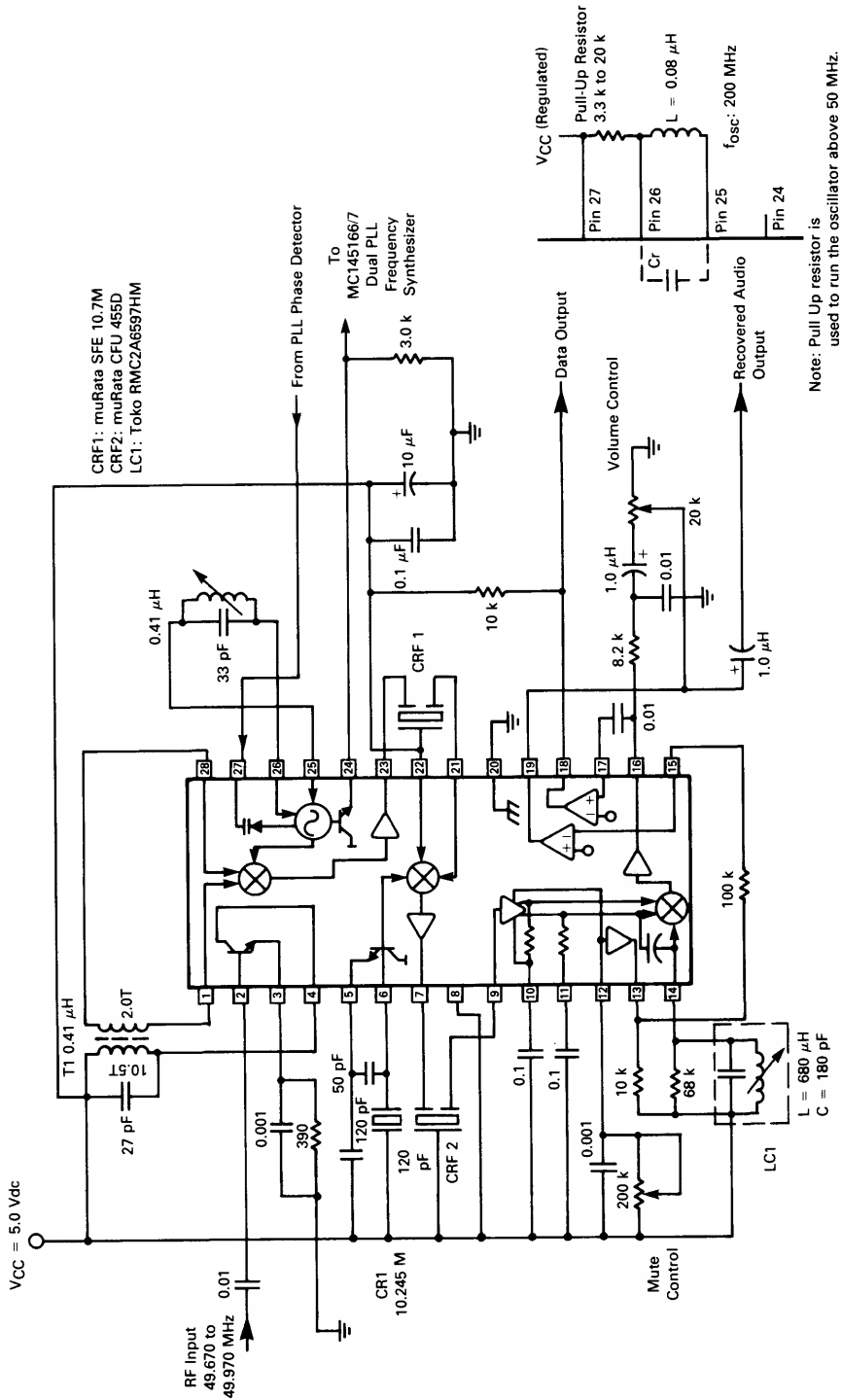


FIGURE 4 — SINGLE CHANNEL NARROWBAND FM RECEIVER AT 49.67 MHz

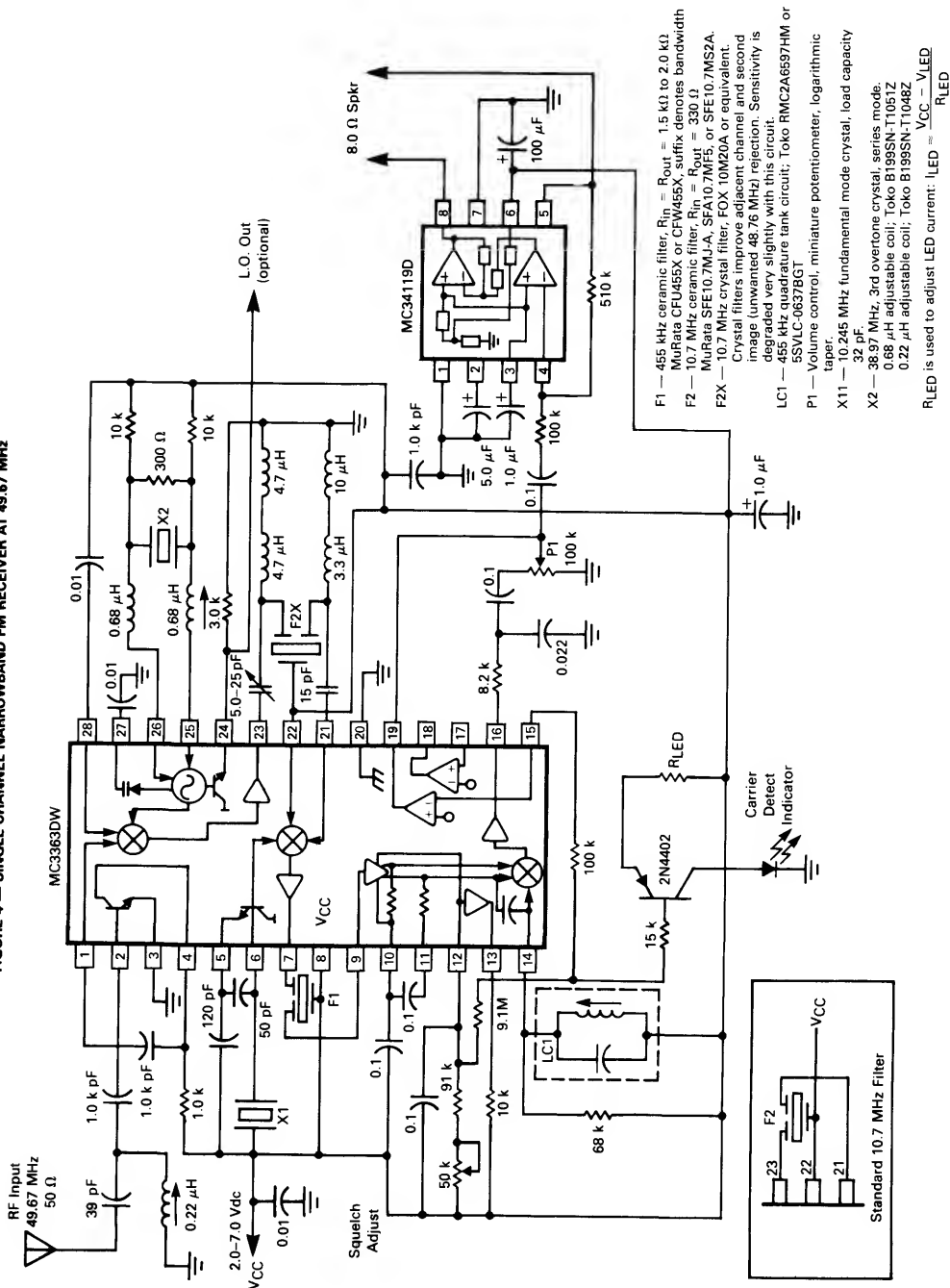


FIGURE 5 — CIRCUIT SCHEMATIC

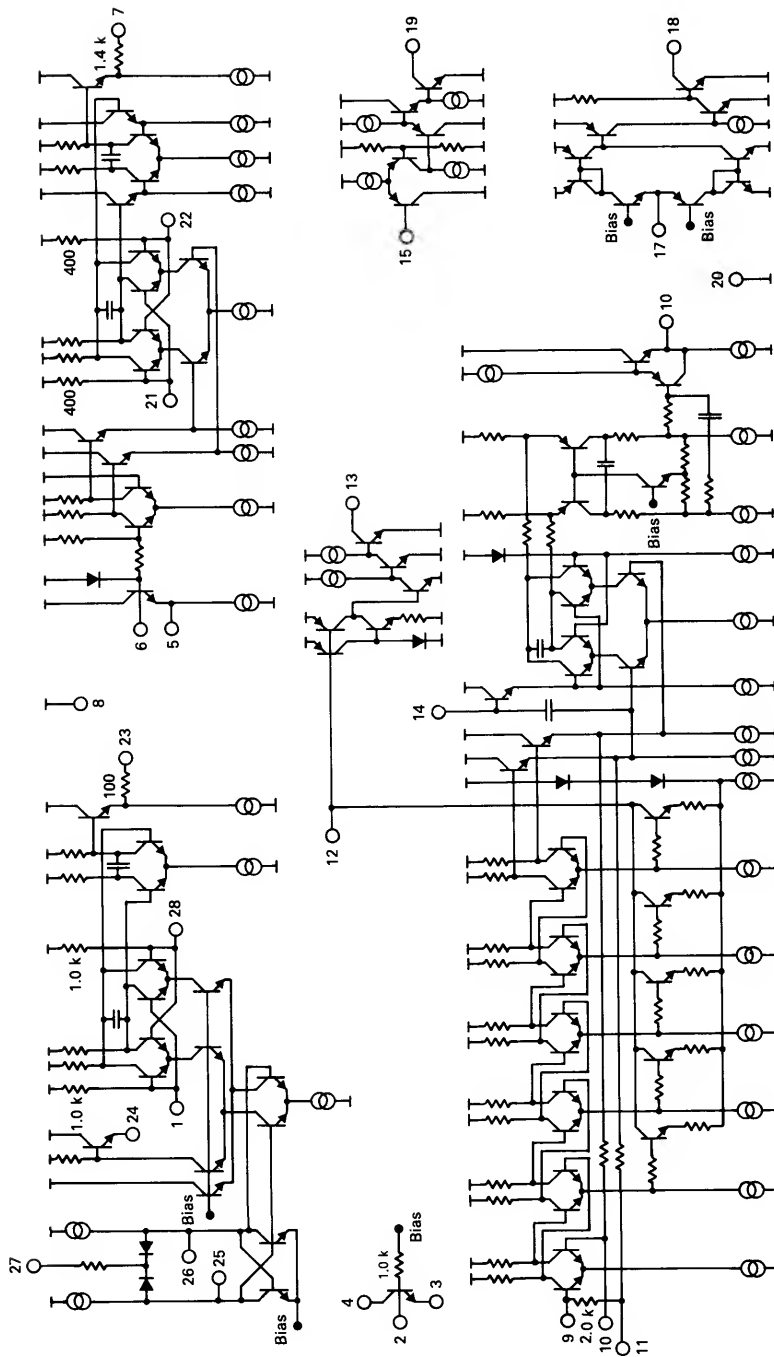


FIGURE 6 — PC BOARD COMPONENT VIEW
WITH HIGH PERFORMANCE CRYSTAL FILTER

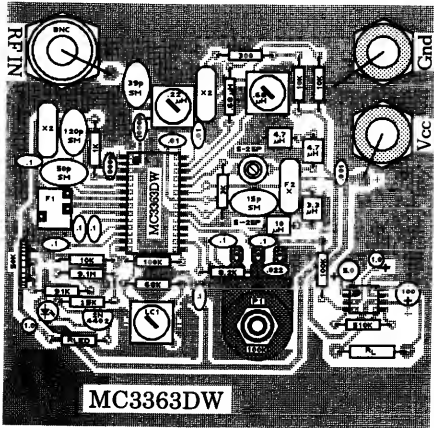


FIGURE 7 — PC BOARD CIRCUIT SIDE VIEW

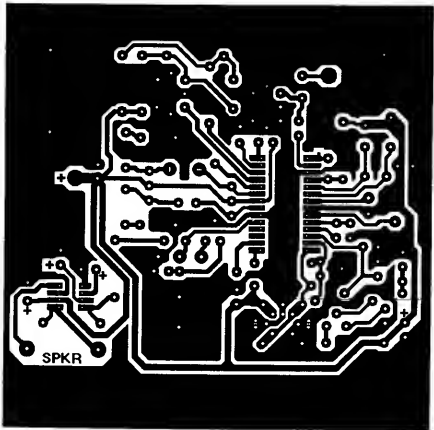
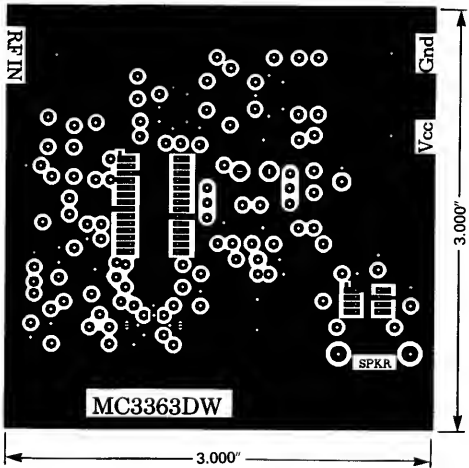


FIGURE 8 — PC BOARD COMPONENT SIDE GROUND PLANE

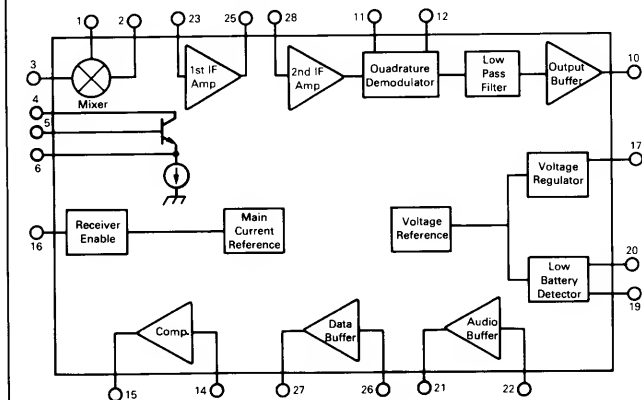


LOW VOLTAGE FM NARROWBAND RECEIVER

... with single conversion circuitry including oscillator, mixer, IF amplifiers, limiting IF circuitry, and quadrature discriminator. The MC3367 is perfect for narrowband audio and data applications up to 75 MHz which require extremely low power consumption. Battery powered applications down to $V_{CC} = 1.1$ V are possible. The MC3367 also includes an on-board voltage regulator, low battery detection circuitry, a receiver enable allowing a power down "sleep mode," two undedicated buffer amplifiers to allow simultaneous audio and data reception, and a comparator for enhancing FSK (Frequency Shift Keyed) data reception to 1200 baud.

- Low Supply Voltage: $V_{CC} = 1.1$ to 3.0 Vdc
- Low Power Consumption: $P_D = 1.5$ to 5.0 mW
- Input Bandwidth 75 MHz
- Excellent Sensitivity: Input Limiting Voltage for 12 dB $Sinad = 0.5 \mu V_{rms}$ from Conjugated Matched Source
- Voltage Regulator Available (Source Capability 3.0 mA)
- Receiver Enable to Allow Active/Standby Operation
- Low Battery Detection Circuitry
- Self Biasing Audio Buffer with Nominal Gain $A_V = 4.0$
- Data Buffer with Nominal Gain $A_V = 3.2$
- FSK Data Shaping Comparator Included
- Standard 28-Lead Surface Mount (SOIC) Package

FIGURE 1 — BLOCK DIAGRAM



MC3367

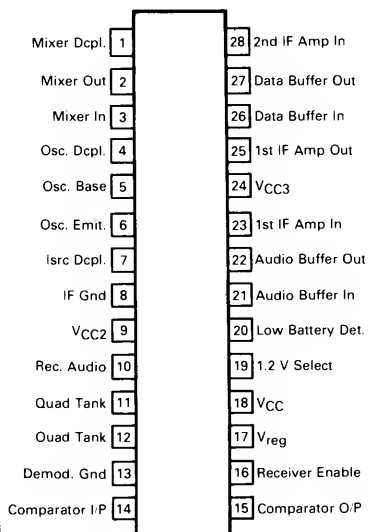
LOW VOLTAGE SINGLE CONVERSION FM RECEIVER

SILICON MONOLITHIC
INTEGRATED CIRCUIT



DW SUFFIX
PLASTIC PACKAGE
CASE 751F
(SO-28L)

PIN CONNECTIONS



MC3367

MAXIMUM RATINGS (Voltages with respect to Pins 8 and 13; $T_A = 25^\circ\text{C}$)

Rating	Pin	Value	Unit
Supply Voltage	18	5.0	Vdc
RF Input Signal	3	1.0	Vrms
Audio Buffer Input	21	1.0	Vrms
Data Buffer Input	26	1.0	Vrms
Comparator Input	14	1.0	Vrms
Junction Temperature	—	150	$^\circ\text{C}$
Storage Temperature	—	-65 to +150	$^\circ\text{C}$

Devices should not be operated at or outside these values. The "Recommended Operating Limits" provide for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Parameter	Pin	Value	Unit
Supply Voltage	18	1.1 to 3.0	Vdc
Receiver Enable Voltage	16	0 or V_{CC}	Vdc
1.2 V Select Voltage	19	Open or V_{CC}	Vdc
RF Input Signal Level	3	0.001 to 100	mVrms
RF Input Frequency	3	0 to 75	MHz
Intermediate Frequency (IF)	—	455	kHz
Audio Buffer Input	21	0 to 75	mVrms
Data Buffer Input	26	0 to 75	mVrms
Comparator Input	14	10 to 300	mVrms
Ambient Temperature	—	0 to 70	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($V_{CC} = 1.3\text{ V}$, $f_0 = 10.7\text{ MHz}$, $f_{\text{mod}} = 1.0\text{ kHz}$, Deviation = 3.0 kHz , $T_A = 25^\circ\text{C}$, Test Circuit of Figure 2 unless otherwise noted)

Characteristic	Pin	Min	Typ	Max	Units
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OVERALL MC3367 PERFORMANCE

Drain Current — Pin 15 = V_{CC}	—	—	1.4	3.0	mA
— Pin 15 = 0 Vdc	—	—	0.5	—	μA
Recovered Audio (RF Input = 10 mV)	10	—	13	—	mVrms
Noise Output (RF Input = 0 mV)	10	—	4.5	—	mVrms
Input for -3.0 dB Limiting	3	—	0.2	—	μVrms

MIXER

Mixer Input Resistance (R_p)	3	—	3.0	—	$\text{k}\Omega$
Mixer Input Capacitance (C_p)	3	—	9.0	—	pF

FIRST IF AMPLIFIER

First IF Amp Voltage Gain	—	—	25	—	dB
---------------------------	---	---	----	---	----

AUDIO BUFFER

Voltage Gain	—	—	4.0	—	V/V
Input Resistance	21	—	125	—	$\text{k}\Omega$
Maximum Input for Undistorted Output	21	—	70	—	mVrms
Maximum Output Swing	22	—	800	—	mVpp
Output Resistance	22	—	680	—	Ω

DATA BUFFER

Voltage Gain	—	—	3.2	—	V/V
Input Resistance	26	—	8.0	—	$\text{M}\Omega$
Maximum Input for Undistorted Output (< 3% THD)	26	—	70	—	mVrms
Maximum Output Swing	27	—	600	—	mVpp
Output Resistance	27	—	1.5	—	$\text{k}\Omega$

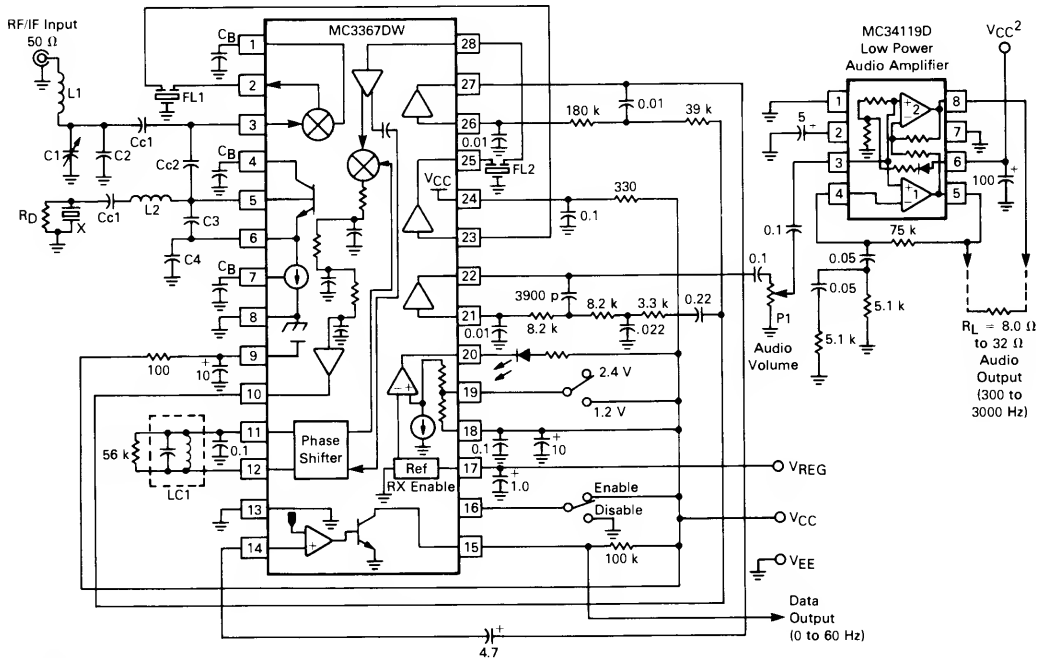
(continued)

MC3367

ELECTRICAL CHARACTERISTICS — continued ($V_{CC} = 1.3 \text{ V}$, $f_o = 10.7 \text{ MHz}$, $f_{\text{mod}} = 1.0 \text{ kHz}$, Deviation = 3.0 kHz , $T_A = 25^\circ\text{C}$, Test Circuit of Figure 2 unless otherwise noted)

Characteristic	Pin	Min	Typ	Max	Units
COMPARATOR					
Minimum Input for Triggering	14	—	7.0	—	mVrms
Maximum Input Frequency ($R_L = 100 \text{ k}\Omega$)	14	—	25	—	kHz
Rise Time (10–90%; $R_L = 100 \text{ k}\Omega$)	15	—	5.0	—	μs
Fall Time (90–10%; $R_L = 100 \text{ k}\Omega$)	15	—	0.4	—	μs
LOW BATTERY DETECTOR					
Low Battery Trip Point	18	—	1.09	—	Vdc
Low Battery Output — $V_{CC} = 0.9 \text{ V}$	20	—	0.2	—	Vdc
— $V_{CC} = 1.3 \text{ V}$	20	—	V_{CC}	—	Vdc
VOLTAGE REGULATOR					
Regulated Output (see Figure 6)	17	—	0.95	—	Vdc
Source Capability	17	—	—	3.0	mA

FIGURE 2 — EVALUATION CIRCUIT



NOTES:

- FL1 and FL2 are 455 kHz ceramic bandpass filters, which should have input and output impedances of 1.5 k Ω to 2.0 k Ω . Suggested part numbers are muRata CFU455X or CFW455X—the "X" suffix denotes bandwidth.
- LC1 is a 455 kHz LC resonator. Recommended part numbers are Toko America RMC2A6597HM or 5SVLC-0637BGT (smaller). The evaluation board layout shown provides for use of either resonator. **Ceramic discriminator elements cannot be used with the MC3367 due to their low input impedance.** The damping resistor value can be raised to increase the recovered audio or lowered to increase the quadrature detector's bandwidth and linearity — practical limits are approximately 27 k Ω to 75 k Ω . Typically the quadrature detector's bandwidth should match the low IF filter's bandwidth.
- The data buffer is set up as a low-pass filter with a corner frequency of approximately 200 Hz. The audio buffer is a bandpass filter with corner frequencies of 300 Hz and 3.0 kHz. The audio amplifier provides bass suppression.
- Cc1 and Cc3 are RF coupling capacitors and should have $\leq 20 \Omega$ impedance at the desired input and oscillator frequencies.
- Cc2 provides "light coupling" of the oscillator signal into the mixer, and should have a $\approx 3.0 \text{ k}\Omega$ to $5.0 \text{ k}\Omega$ impedance at the desired local oscillator frequency.
- Capacitors labelled C_B are bypass capacitors and should have $\leq 20 \Omega$ impedance at the desired RF and local oscillator frequencies.
- The network of L1, C1 and C2 provides impedance matching of the mixer input (nominally $3.0 \text{ k}\Omega$ shunted by 9.0 pF) to 50 Ω at the desired RF/IF input frequency. This will allow for bench testing of the receiver from typical RF signal generators or radio service monitors, but additional or different matching will be required to maximize receiver sensitivity when used in conjunction with an antenna, RF preamplifier or mixer.

FIGURE 3 — RECOVERED AUDIO versus SUPPLY

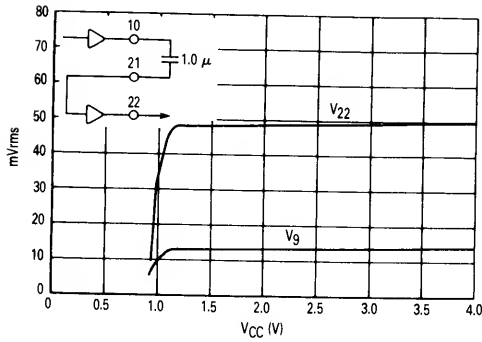


FIGURE 4 — DRAIN versus SUPPLY

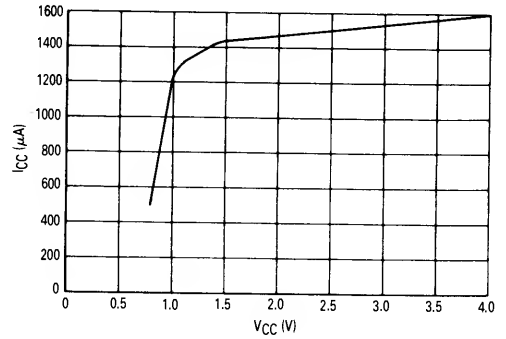


FIGURE 5 — S + N, N versus INPUT

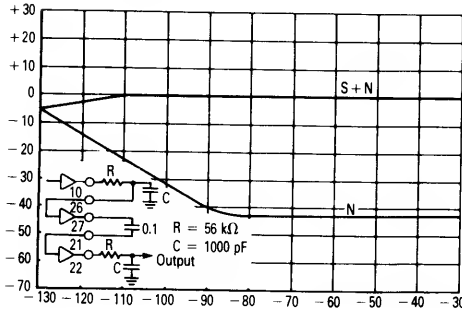


FIGURE 6 — VREG versus SUPPLY

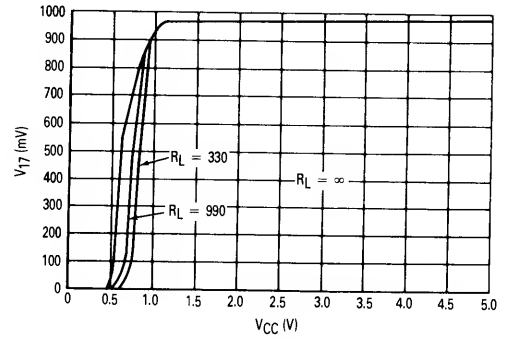


FIGURE 7 — REGULATED OUTPUT AND RECOVERED AUDIO versus TEMPERATURE

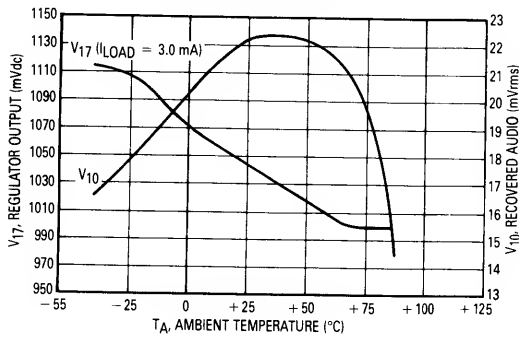
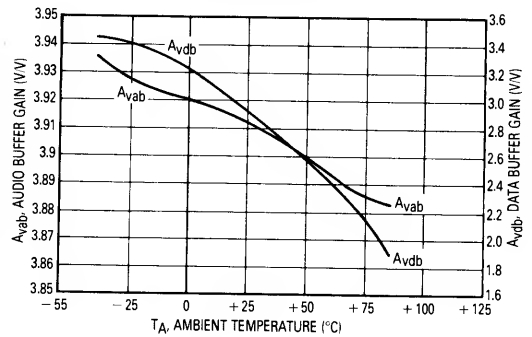


FIGURE 8 — BUFFER AMPLIFIER GAINS versus TEMPERATURE



MC3367

FIGURE 9 — CURRENT DRAIN versus TEMPERATURE

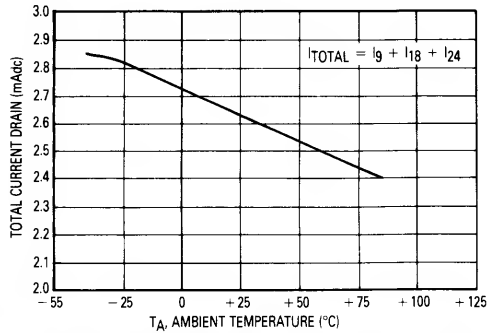
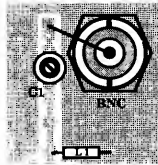
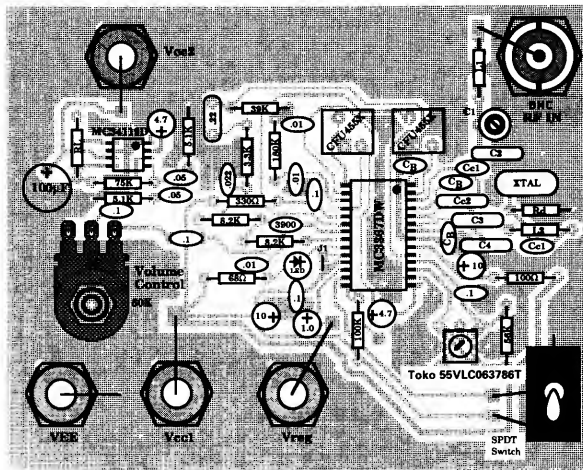


FIGURE 10 — MC3367DW DEMONSTRATION RECEIVER



**Alternate input circuit
for 72 MHz receiver.**

In. Freq.	L1	L2	C1	C2	C3	C4	Cc1	Cc2	Cg	R _D
10.7 MHz	6.8 μH	Short	2-82 pF	10 pF	120 pF	50 pF	1.0 k pF	5.0 pF	0.1 μF	Open
45 MHz	0.68 μH	1.2 μH	5-25 pF	Open	30 pF	5.0 pF	1.0 k pF	1.0 pF	1.0 k pF	1.0 k
72 MHz	0.22 μH	0.22 μH	5-25 pF	Open	18 pF	3.0 pF	470 pF	1.0 pF	470 pF	1.0 k

Volume Control: CRL B12503SL

V_{CC1}: 1.1 V to 3.0 V

V_{CC2}: 2.0 V to 16 V

Speaker: 8.0 Ω to 32 Ω

J1: Jumper — install for 1.2 V operation. Leave open for 2.4 V operation.

ICs mount on circuit side (back) of PC board.

C3, C4 must be 5% silver mica

MC3367

FIGURE 11 — BOTTOM (CIRCUIT) SIDE

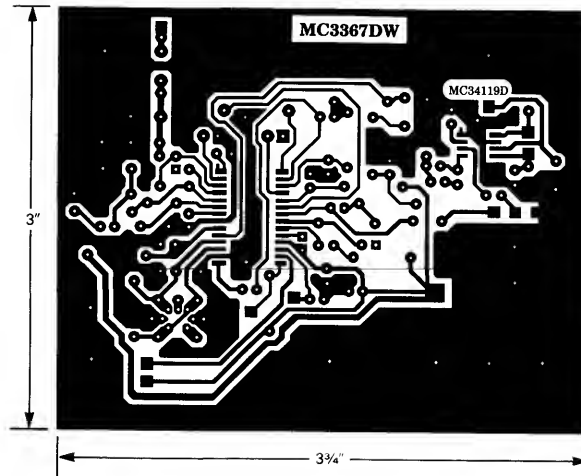


FIGURE 12 — TOP (COMPONENT/GROUND PLANE) SIDE

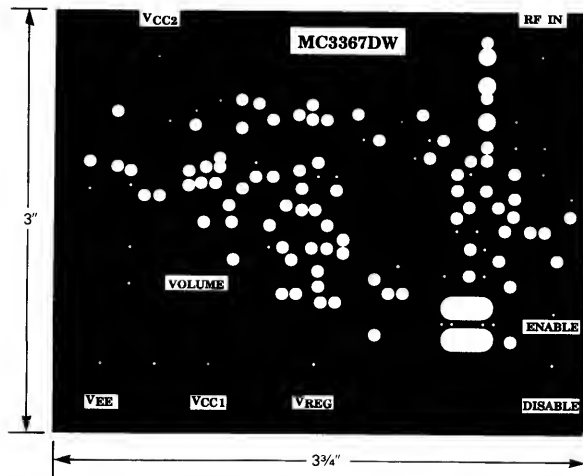
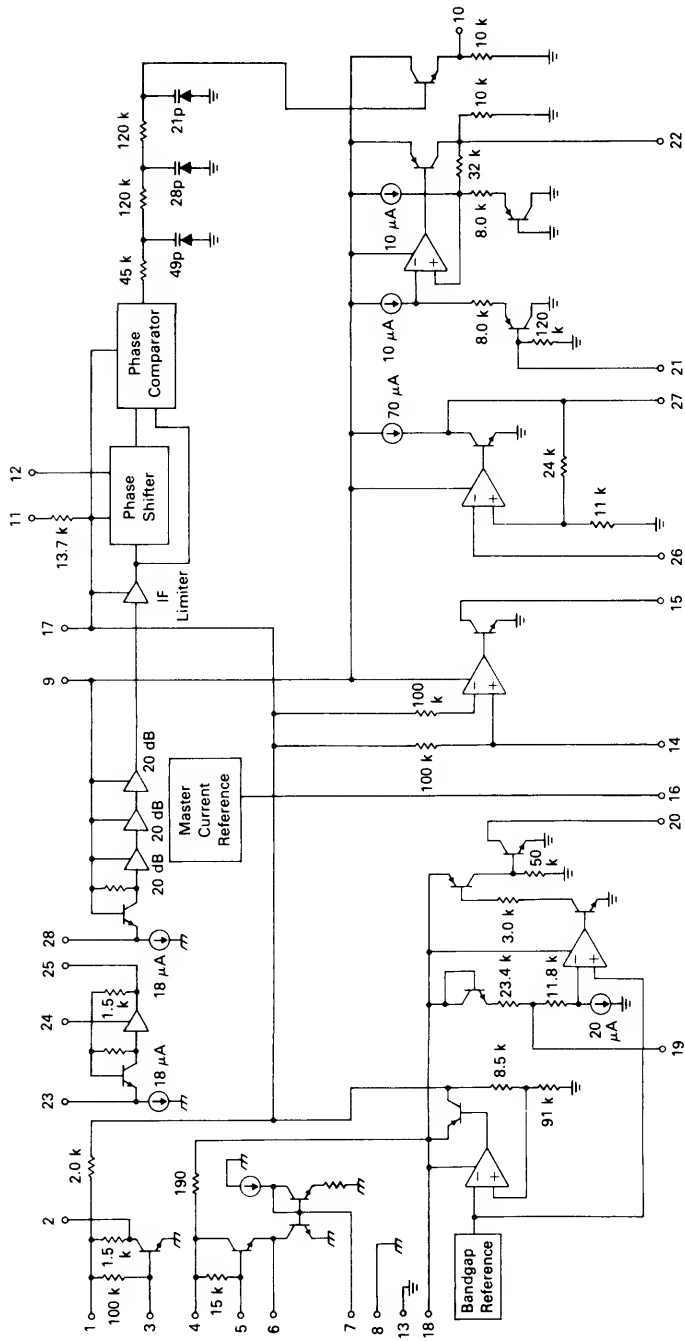


FIGURE 13 — CIRCUIT SCHEMATIC



CIRCUIT DESCRIPTION

The MC3367 is an FM narrowband receiver capable of operation to 75 MHz. The low voltage design yields low power drain and excellent sensitivity in narrowband voice and data link applications. In the typical application the mixer amplifies the incoming RF or IF signal and converts this frequency to 455 kHz. The signal is then filtered by a 455 kHz ceramic filter and applied to the first intermediate frequency (IF) amplifier input, before passing through a second ceramic filter. The modulated IF signal is then applied to the limiting IF amplifier and detector circuitry. Modulation is recovered by a conventional quadrature detector. The typical modulation bandwidth available is 3.0 to 5.0 kHz.

Features available include buffers for audio/data amplification and active filtering, on board voltage regulator, low battery detection circuitry with programmable level, and receiver disable circuitry. The MC3367 is an FM utility receiver to be used for voice and/or narrowband data reception. It is especially suitable where extremely low power consumption and high design flexibility are required.

APPLICATION

The MC3367 can be used as a high performance FM IF for use in low power dual conversion receivers. Because of the MC3367's extremely good sensitivity (0.6 μ V for 20 dB (S+N)/N, see Figure 5), it can also be used as a stand alone single conversion narrowband receiver to 75 MHz for applications not sensitive to image frequency interference. An RF preamplifier will likely be needed to overcome preselector losses.

The oscillator is a Colpitts type which must be run under crystal control. For fundamental mode crystals choose resonators, parallel resonant, for a 32 pF load. For higher frequencies, use a 3rd overtone series mode type. The coil (L2) and R_D resistor are needed to ensure proper operation.

The best adjacent channel and sensitivity response occur when two 455 kHz ceramic filters are used, as shown in Figure 2. Either can be replaced by a 0.1 μ F coupling capacitor to reduce cost, but some degradation in sensitivity and/or stability is suspected.

The detector is a quadrature type, with the connection from the limiter output to the detector input provided internally as with the MC3359 and the MC3361. A 455 kHz LC tank circuit must be provided externally. One of the tank pins (Pin 11) must be decoupled using a 0.1 μ F capacitor. The 56 k Ω damping resistor (see Figure 2), determines the peak separation of the detector (and thus its bandwidth). Smaller values will increase the separation and bandwidth but decrease recovered audio and sensitivity.

The data buffer is a noninverting amplifier with a nominal voltage gain of 3.2 V/V. This buffer needs its dc bias (approx. 250 mV) provided externally or else debiasing will occur. A single-pole RC filter, as shown in Figure 5, connecting the recovered audio output to the data buffer input provides the necessary dc bias and some post detection filtering. The buffer can also be used as an active filter.

The audio buffer is a noninverting amplifier with a nominal voltage gain of 4.0 V/V. This buffer is self-biasing so its input should be ac coupled. The two buffers, when applied as active filters, can be used together to allow simultaneous audio and very low speed data reception. Another possible configuration is to receive audio only and include a noise-triggered squelch.

The comparator is a noninverting type with an open collector output. Typically, the pull-up resistor used between Pin 15 and V_{CC} is 100 k Ω . With R_L = 100 k Ω the comparator is capable of operation up to 25 kHz. This circuit is self-biasing, so its input should be ac coupled.

The regulator is a 0.95 V reference capable of sourcing 3.0 mA. This pin (Pin 17) needs to be decoupled using a 1.0–10 μ F capacitor to maintain stability of the MC3367.

All three V_{CC}s on the MC3367 (V_{CC}, V_{CC2}, V_{CC3}) run on the same supply voltage. V_{CC} is typically decoupled using capacitors only. V_{CC2} and V_{CC3} should be bypassed using the RC bypasses shown in Figure 2. Eliminating the resistors on the V_{CC2} and V_{CC3} bypasses may be possible in some applications, but a reduction in sensitivity and quieting will likely occur.

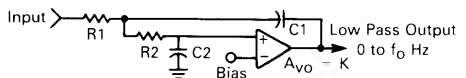
The low battery detection circuit gives an NPN open collector output at Pin 20 which drops low when the MC3367 supply voltage drops below 1.1 V. Typically it would be pulled up via a 100 k Ω resistor to supply.

The 1.2 V Select pin, when connected to the MC3367 supply, programs the low battery detector to trip at V_{CC} < 1.1 V. Leaving this pin open raises the trip voltage on the low battery detector.

Pin 16 is a receiver enable which is connected to V_{CC} for normal operation. Connecting this pin to ground shuts off receiver and reduces current drain to I_{CC} < 0.5 μ A.

APPENDIX

Design of 2nd Order Sallen-Key Low Pass Filters



The audio and data buffers can easily be configured as active low pass filters using the circuit configuration shown above. The circuit has a center frequency (f_0) and quality factor (Q) given by the following:

$$f_0 = \frac{1}{2\pi \sqrt{R_1 R_2 C_1 C_2}}$$

$$Q = \frac{1}{\sqrt{\frac{R_2 C_2}{R_1 C_1}} + \sqrt{\frac{R_1 C_2}{R_2 C_1}} + (1-K) \sqrt{\frac{R_1 C_1}{R_2 C_2}}}$$

If possible, let R₁ = R₂ or C₁ = C₂ to simplify the above equations. Be sure to avoid a negative Q value to prevent instability. Setting Q = 1/√2 = 0.707 yields a maximally flat filter response.

Data Buffer Design

The data buffer is designed as follows:

$$f_o = 200 \text{ Hz}$$

$$C1 = C2 = 0.01 \mu\text{F}$$

$$Q = 0.707 \text{ (target)}$$

$$K = 3.2 \text{ (data buffer open loop voltage gain)}$$

Setting $C1 = C2$ yields:

$$f_o = \frac{1}{2\pi C1 \sqrt{R1 R2}}$$

$$Q = \frac{1}{\sqrt{\frac{R2}{R1} + (2-K) \sqrt{\frac{R1}{R2}}}}$$

Iteration yields $R2 = 4.2 (R1)$ to make $Q = 0.707$.

Substitution into the equation for f_o yields:

$$R1 = 38 \text{ k}\Omega \text{ (use } 39 \text{ k}\Omega)$$

$$R2 = 4.2 (R1) = 180 \text{ k}\Omega$$

$$C1 = C2 = 0.01 \mu\text{F}$$

Audio Buffer Design

The audio buffer is designed as follows:

$$f_o = 3000 \text{ Hz}$$

$$R1 = R2 = 8.2 \text{ k}\Omega$$

$$Q = 0.707 \text{ (target)}$$

$$K = 4.0 \text{ (audio buffer open loop voltage gain)}$$

Setting $R1 = R2$ yields:

$$f_o = \frac{1}{2\pi R1 \sqrt{C1 C2}}$$

$$Q = \frac{1}{2 \sqrt{\frac{C2}{C1} + (1-K) \sqrt{\frac{C1}{C2}}}}$$

Iteration yields $C2 = 2.65 (C1)$ to make $Q = 0.707$.

Substitution into the equation for f_o yields:

$$C1 = 3900 \text{ pF}$$

$$C2 = 2.65 (C1) = 0.01 \mu\text{F}$$

$$R1 = R2 = 8.2 \text{ k}\Omega$$

MC13055

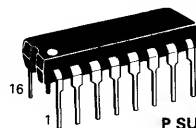
WIDEBAND FSK RECEIVER

The MC13055 is intended for RF data link systems using carrier frequencies up to 40 MHz and FSK (frequency shift keying) data rates up to 2.0M Baud (1.0 MHz). This design is similar to the MC3356, except that it does not include the oscillator/mixer. The IF bandwidth has been increased and the detector output has been revised to a balanced configuration. The received signal strength metering circuit has been retained, as has the versatile data slicer/comparator.

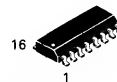
- Input Sensitivity 20 μV @ 40 MHz
- Signal Strength Indicator Linear Over 3 Decades
- Available in Surface Mount Package
- Easy Application, Few Peripheral Components

WIDEBAND FSK RECEIVER

MONOLITHIC SILICON INTEGRATED CIRCUIT

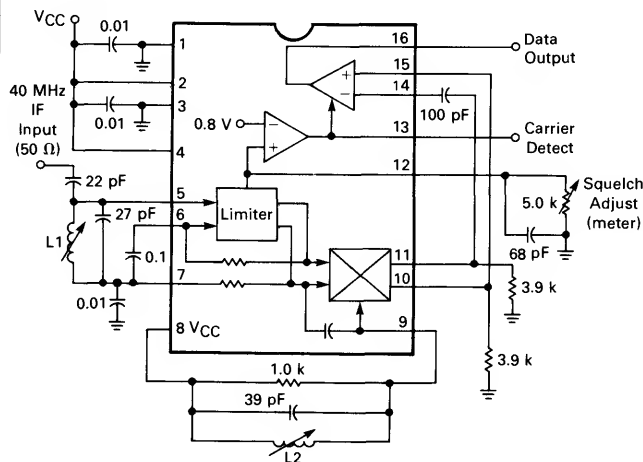


P SUFFIX
 PLASTIC PACKAGE
 CASE 648



D SUFFIX
 PLASTIC PACKAGE
 CASE 751B
 (SO-16)

FIGURE 1 — BLOCK DIAGRAM AND APPLICATION CIRCUIT



PIN CONNECTIONS

Comparator Ground	1	16	Data Out
Comparator VCC	2	15	+ Comparator
IF Ground	3	14	- Comparator
IF VCC	4	13	Carrier Detect
Limiter Input	5	12	Meter Drive
Limiter Bias	6	11	Detector Out
Limiter Bias	7	10	Detector Out
Quad Bias	8	9	Quad Input

MC13055

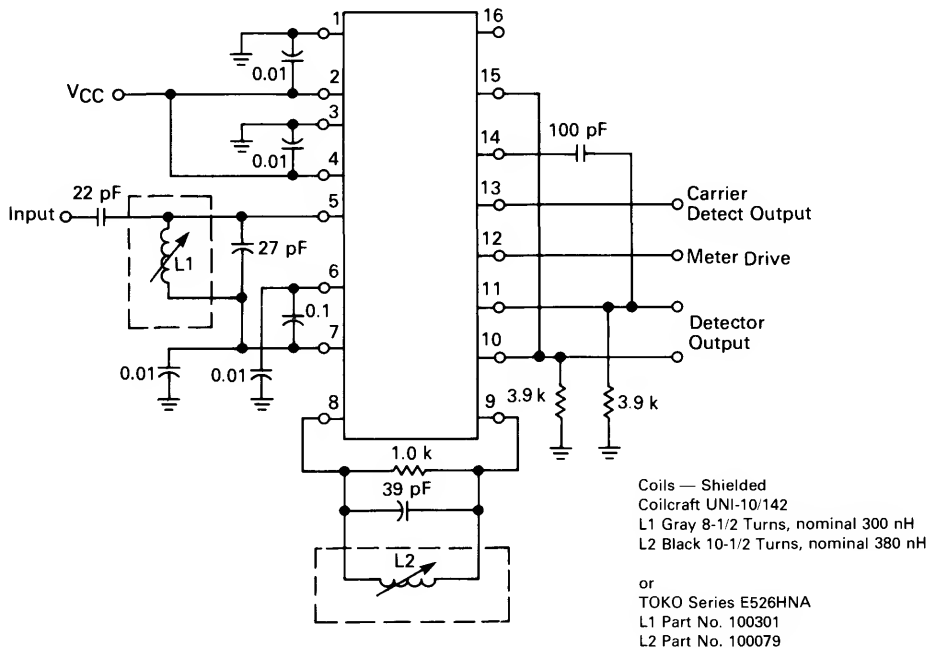
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC(max)}$	15	Vdc
Operating Supply Voltage Range	V2, V4	3.0 to 12	Vdc
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Power Dissipation, Package Rating	P_D	1.25	W

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0$ Vdc, $f_o = 40$ MHz, $f_{mod} = 1.0$ MHz, $\Delta f = \pm 1.0$ MHz, $T_A = 25^\circ\text{C}$, test circuit of Figure 2)

Characteristics	Measure	Min	Typ	Max	Unit
Total Drain Current	I2 + I4	—	20	25	mA
Data Comparator Pull-Down Current	I16	—	10	—	mA
Meter Drive Slope versus Input	I12	4.5	7.0	9.0	$\mu\text{A/dB}$
Carrier Detect Pull-Down Current	I13	—	1.3	—	mA
Carrier Detect Pull-Up Current	I13	—	500	—	μA
Carrier Detect Threshold Voltage	V12	700	800	900	mV
DC Output Current	I10, I11	—	430	—	μA
Recovered Signal	V10 - V11	—	350	—	mVrms
Sensitivity for 20 dB S + N/N, BW = 5.0 MHz	VIN	—	20	—	μVrms
S + N/N at $V_{in} = 50$ μV	V10 - V11	—	30	—	dB
Input Impedance @ 40 MHz	R_{in} C_{in}	Pin 5, Ground	— —	4.2 4.5	k Ω pF
Quadrature Coil Loading	R_{in} C_{in}	Pin 9 to 8	— —	7.6 5.2	k Ω pF

FIGURE 2 — TEST CIRCUIT



MC13055

All curves taken with test conditions of ELECTRICAL CHARACTERISTICS, unless otherwise noted

FIGURE 3 — OVERALL GAIN, NOISE, AM REJECTION

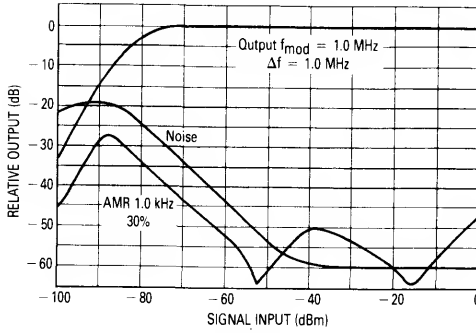


FIGURE 4 — METER CURRENT versus SIGNAL

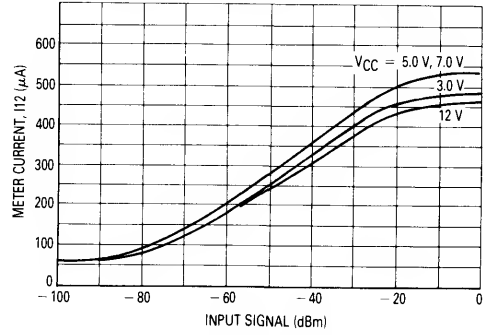


FIGURE 5 — UNTUNED INPUT: LIMITING SENSITIVITY versus FREQUENCY

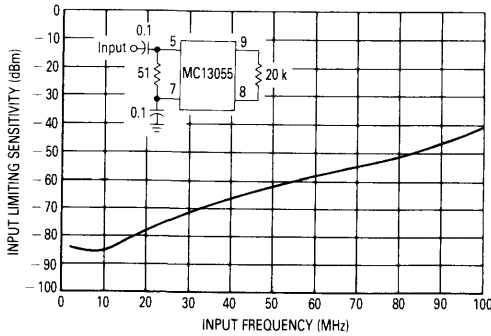


FIGURE 6 — UNTUNED INPUT: METER CURRENT versus FREQUENCY

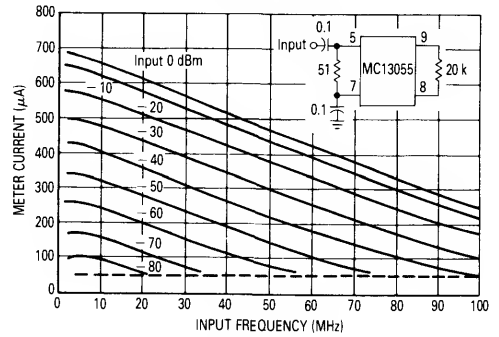


FIGURE 7 — LIMITING SENSITIVITY AND DETUNING versus SUPPLY

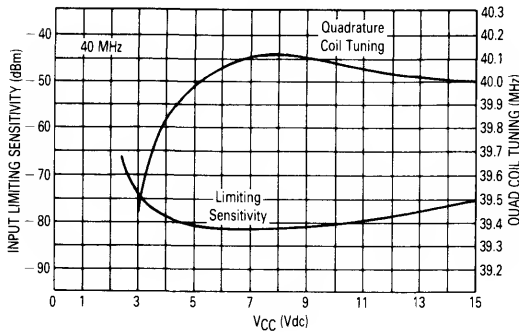
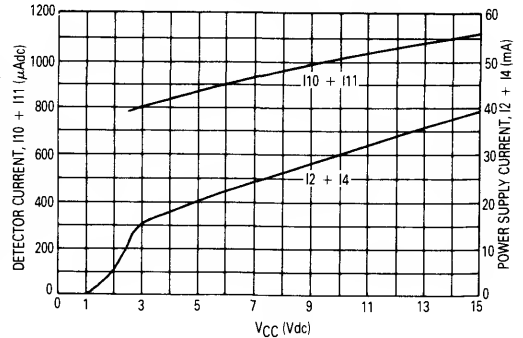


FIGURE 8 — DETECTOR CURRENT AND POWER SUPPLY CURRENT versus SUPPLY VOLTAGE



8

**FIGURE 10 — CARRIER DETECT THRESHOLD
versus TEMPERATURE**

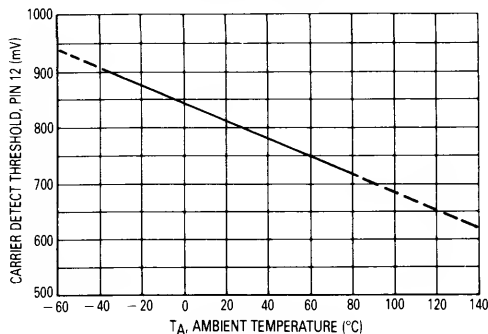
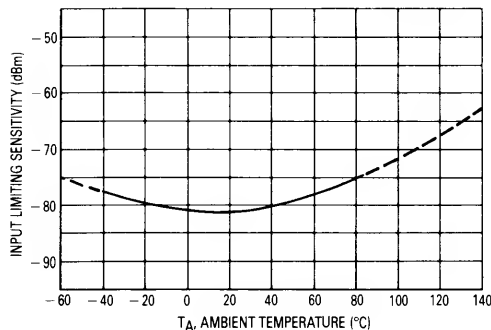


FIGURE 12 — INPUT LIMITING versus TEMPERATURE



0.25 inch

40 MHz Input (BNC)

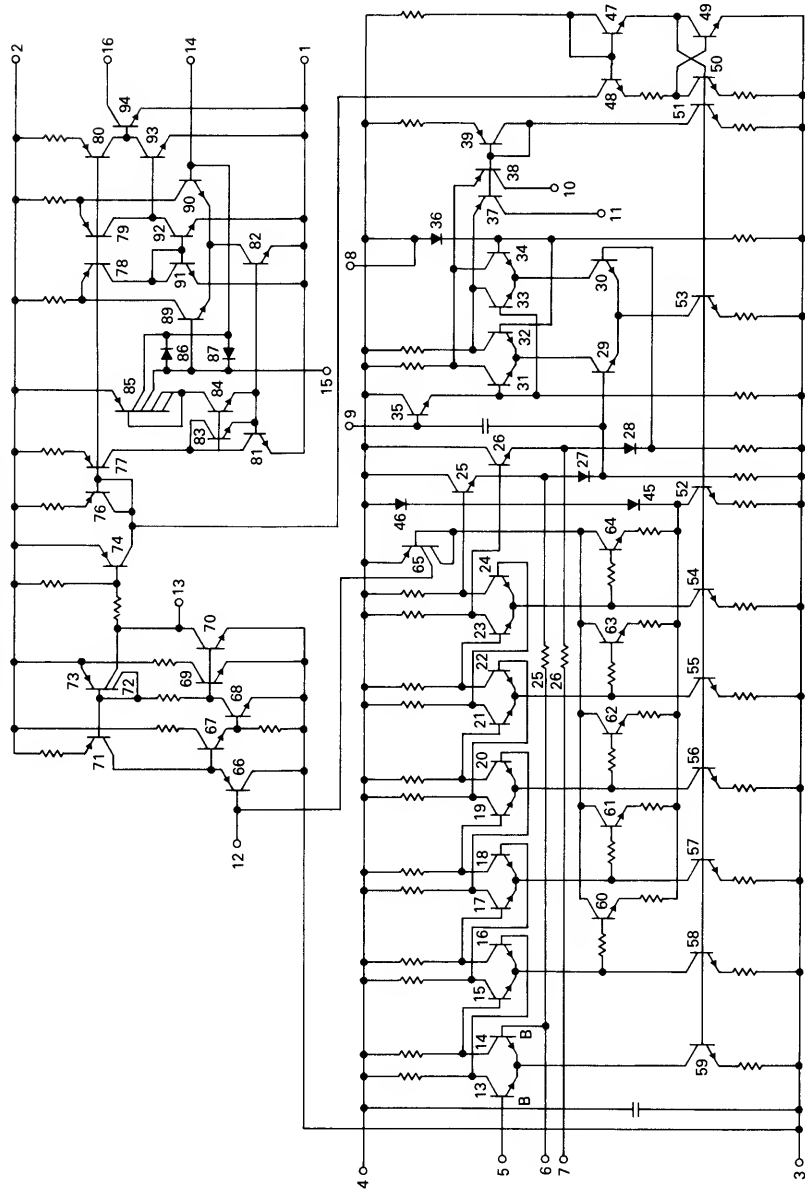
Squelch Adjust or Meter Drive

Data Output

Carrier Detect

VCC

FIGURE 14 — INTERNAL SCHEMATIC



GENERAL DESCRIPTION

The MC13055 is an extended frequency range FM IF, quadrature detector, signal strength detector and data shaper. It is intended primarily for FSK data systems. The design is very similar to MC3356 except that the oscillator/mixer has been removed, and the frequency capability of the IF has been raised about 2:1. The detector output configuration has been changed to a balanced, open-collector type to permit symmetrical drive of the data shaper (comparator). Meter drive and squelch features have been retained.

The limiting IF is a high frequency type, capable of being operated up to 100 MHz. It is expected to be used at 40 MHz in most cases. The quadrature detector is internally coupled to the IF, and a 2.0 pF quadrature capacitor is internally provided. The 20 dB quieting sensitivity is approximately 20 μ V, tuned input, and the IF can accept signals up to 220 mVrms without distortion or change of detector quiescent dc level.

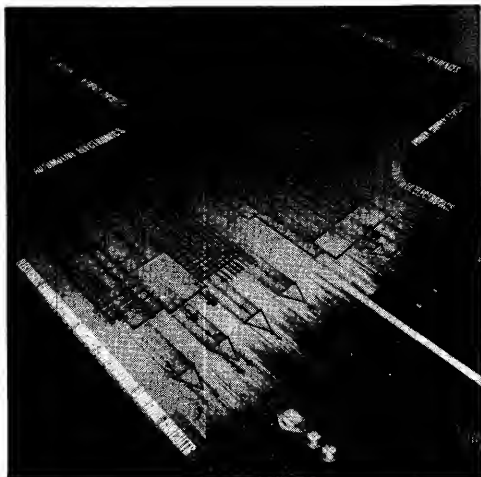
The IF is unusual in that each of the last 5 stages of the 6 stage limiter contains a signal strength sensitive, current sinking device. These are parallel connected and buffered to produce a signal strength meter drive which

is fairly linear for IF input signals of 20 μ V to 20 mVrms. (See Figure 4.)

A simple squelch arrangement is provided whereby the meter current flowing through the meter load resistance flips a comparator at about 0.8 Vdc above ground. The signal strength at which this occurs can be adjusted by changing the meter load resistor. The comparator(+) input and output are available to permit control of hysteresis. Good positive action can be obtained for IF input signals of above 20 μ Vrms. A resistor R from Pin 13 to Pin 12 will provide V_{CC}/R of feedback current. This current can be correlated to an amount of signal strength hysteresis by using Figure 4.

The squelch is internally connected to the data shaper. Squelch causes the data shaper to produce a high (V_{CC}) output.

The data shaper is a complete "floating" comparator, with diodes across its inputs. The outputs of the quadrature detector can be fed directly to either or preferably both inputs of the comparator to produce a squared output swinging from V_{CC} to ground in inverted or non-inverted form.



In Brief . . .

. . . reflecting Motorola's continuing commitment to semiconductor products necessary for consumer system designs. This tabulation is arranged to simplify first-order selection of consumer integrated circuit devices that satisfy the primary functions for home entertainment products, including Television, Hi-Fi Audio and AM/FM Radio.

Consumer Electronic Circuits

Selector Guide

Entertainment Radio Receiver Circuits.	9-2
Video Circuits	9-3
Remote Control Circuits.	9-6
Alphanumeric Index.	9-7
Related Application Notes	9-8
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Consumer Electronic Circuits

Entertainment Radio Receiver Circuits

C-QUAM® AM Stereo Decoders

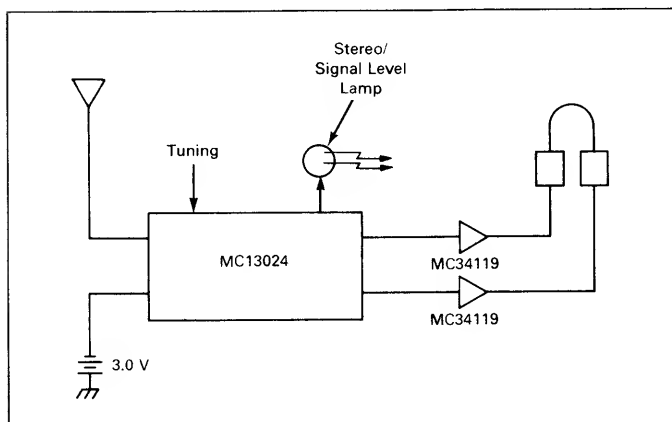
Function	Features	Package Suffix	Device
Basic AM Stereo Decoder	Monaural/Stereo AM Detector, Indicator, 6–10 V Operation	P/738	MC13020
Advanced AM Stereo Decoder	Medium Voltage 2–8 V, Decoder and IF Amp	DW/751F	MC13022
AM Front End	Tuning Stabilizer for MC13022	P/738	MC13023
AM Stereo Personal Radio	Complete Low Voltage AM Stereo Receiver	P/724	MC13024

Audio Amplifiers

Function	P _O Watts	V _{CC} Vdc Max	V _{in} @ rated P _O mV Typ	I _D mA Typ	R _L Ohms	Package Suffix	Device
Mini Watt SOIC Audio Amp	1.0 W	35	80	11	16	D/751	MC13060
Low Power Audio Amp	400 mW	16	—	2.5 mA	8–100	D/751 P/626	MC34119

Audio Attenuators/Controls

Function	V _{CC} Range Vdc	THD %	Tone Control Range dB Typ	Attenuation Range dB Typ	Package Suffix	Device
Electronic Attenuator	8–18	0.6 Typ	± 13	80	P/626	MC3340
Stereo, Volume, Bass, Treble, Balance	3–18	0.5 Max	± 15	80	P/707	TDA1524



C-QUAM Portable Receiver

When AM stereo broadcasting was sanctioned by the F.C.C. in 1982, there were five different systems vying for user approval. Since then C-QUAM® has become the defacto standard in the U.S.A., with over 700 stations "on the air" as the market and broadcasters recognize its performance advantages. It is the legal standard in Canada, Australia and Brazil where A.M. is the dominant radio medium. C-QUAM is available from nearly 50 automobile radio makers and a dozen home receiver builders.

Based on the field-proven C-Quam performance, Motorola has developed a low-cost, high performance C-Quam AM Stereo Decoder chip, with fully compatible, no-compromise mono performance, as the basis for both broadcast and receiving equipment. Additional IC components from Motorola's inventory offer a single supply source for state-of-the-art radio receiver designs. New products cover virtually every type of receiver — home, auto, and personal portable.

Radio Circuits (See Communications Section)

Video Circuits

9

Modulators

Function	Features	Package Suffix	Device
Color TV Video Modulator	RF Oscillator and Modulator	P/626	MC1373
TV Modulator (High Quality)	RF Oscillator Modulator, and FM Sound Oscillator/Modulator	P/646	MC1374
Video RGB to PAL/NTSC Encoder	RGB and Sync Inputs, Composite Video Out — PAL/NTSC Switch Selectable	P/738	MC1377
Video Synchronizer	Complete Color TV Video Overlay Synchronizer	P/711	MC1378

Demodulators

Color Processor	PAL NTSC Input, RGB Output, also RGB Inputs, Plus Fast Blanking Input. Ideal for Text, Graphics, Overlays	P 711	TDA3301B TDA3303
Color Processor	PAL NTSC Input, RGB Outputs, On-Chip Hue Control	P/724	TDA3330
Color Processor	PAL NTSC Input, Color Difference Outputs On-Chip Hue Control	P/707	TDA3333
Chroma 4 Multi-Standard Decoder	Full PAL SECAM NTSC Capability, Dual Composite or S-VHS Inputs, RGB Outputs, Digital Control of all On-Chip Functions	P 711	MC44000*

*To be introduced

VIDEO CIRCUITS (continued)

Tuning System

Function	Features	Package Suffix	Device
Remote Control Amplifier	Infrared Diode Signal Amplifier Shaper	P/626	MC3373
PLL-Tuning Circuit	TV Tuning System — Prescaler — M-Bus Control	DW/751C	MC44802
Remote Control Receiver	Infrared Preamplifier	P/626	MC44520*

Deflection

Horizontal Processor	Linear Balanced Phase Detector, Oscillator and Predriver, Adjustable dc Loop Gain, Adjustable Duty Cycle	P/626	MC1391
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Sound

Sound IF Detector	Interchangeable with ULN2111A	P/646	MC1357
Sound IF, Low Pass Filter, Detector, dc Volume Control, Preamplifier	Complete TV Sound System; 100 μ V, 3 dB Limiting Sensitivity; 4 Watts Output; $V_{CC} = 24$ V; $R_L = 16 \Omega$	P/648C	TDA3190

Transistor Arrays

Function	$I_{C(max)}$ mA	V_{CEO} Volts Max	V_{CBO} Volts Max	V_{EBO} Volts Max	Package Suffix	Device
One Differentially Connected Pair and Three Isolated Transistors	50	15	20	5.0	P/646 D/751A	MC3346
Dual Independent Differential Amplifiers with Associated Constant Current Transistors	50	15	20	5.0	P/646	CA3054
General Purpose H/V Array	50	30	40	5.0	D/751A	CA3146

Television Subsystems

Function	Features	Package Suffix	Device
MONOMAX — 1-Chip Black and White TV Subsystem	Video IF, Detector, AGC, Video Amplifier, Horizontal Processor, Vertical Processor, and Sync For 525 Line Systems	P/710	MC13001X
	Same as Above Except For 625 Line Systems	P/710	MC13002X
Sound IF, Low Pass Filter, Detector, dc Volume Control, Preamplifier, Power Amplifier	Complete TV Sound System; 100 μ V, 3 dB Limiting Sensitivity; 4 Watts Output; $V_{CC} = 24$ V; $R_L = 16 \Omega$	P/648C	TDA3190

Video IF Amplifiers

Function	Features	Package Suffix	Device
1st and 2nd Video IF Amplifier	IF Gain (α 45 MHz = 50 dB typ, AGC Range = 60 dB min	P/626	MC1350
3rd IF, Video Detector, Video Buffer, and AFC Buffer	Low Level Detection, Low Harmonic Generation	P/626	MC1330A
SAW Preamp, IF Amplifier, Detector, AGC, AFC	Complete Video IF or Parallel Sound IF System Complete AFT System with Simple Quadrature Detector	P/707	MC13010
Advanced Video IF	Complete Video/Audio IF System for High Performance Analog TV Receivers	DW/751F	MC44301
Video Switch	5 RGB & Video Inputs and 5 Video Outputs	P/724	MC44900*

Color Graphics DACs

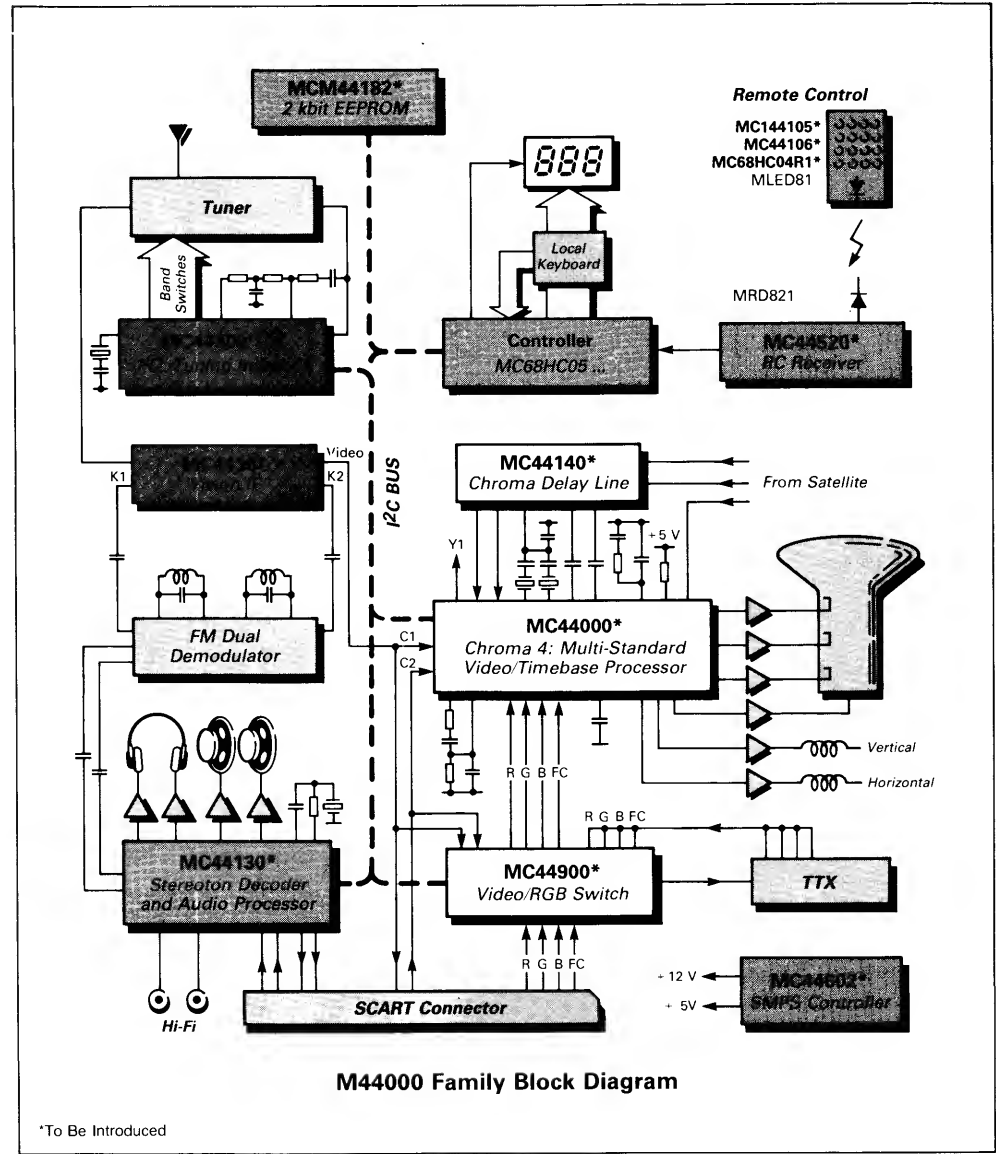
Resolution (Bits)	Device	Suffix	Accuracy (α 25°C (Max)	Max Settling Time ($\pm 1/2$ LSB)	Supplies (V)	Temperature Range	Package	Comments
4 x 3	MC10320	L	$\pm 1/4$ LSB	3.0 ns	+5.0, or ± 5.0	0°C to +70°C	733	125 MHz Color Graphics Triple DAC
	MC10320-1							90 MHz Color

*To be introduced

VIDEO CIRCUITS (continued)

Monitor Systems

Function	Features	Package Suffix	Device
Multisync TTL to Analog Interface	Converts TTL Inputs from CGA or EGA to Analog RGB Outputs	P/724 DW/751E	MC1382
Multimode Monitor Processor	Auto Frequency Tracking, Vertical Output Pulse and 50 MHz Video System	P/711	MC1383
Multimode Monitor Processor with Vertical Timebase	Auto Frequency Tracking, Vertical Time Base and 50 MHz Video System	P/711	MC1384



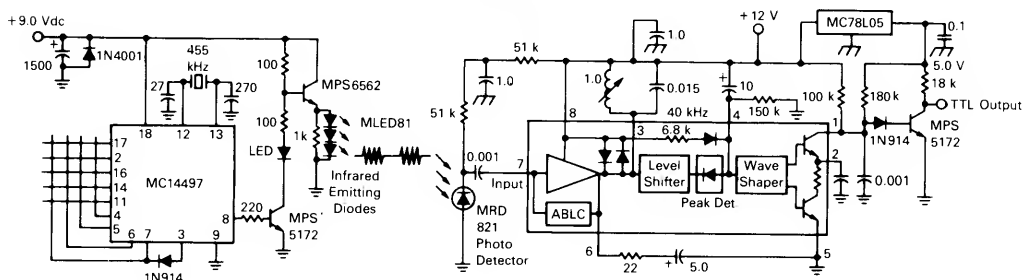
Remote Control Circuits

MC3373P Amplifier/Detector (Bipolar), Case 626 MC14497 Transmitter (CMOS), Case 707

The MC3373 remote receiver is specifically designed for infra-red link systems where high sensitivity and good noise immunity are critical. The MC3373 incorporates a high gain detector diode preamp driving an envelope detector and data wave shaper for accurate data recovery. Provision is also made to use an external L-C tank circuit at the carrier frequency, normally 30 to 60 kHz, for extended range low noise systems. Applications

include TV remote control, short range data links (up to several hundred feet), door openers and security systems. The MC144997 is an ideal companion transmitter, where a simple D.T.M.F. like key-pad control is desired. The Motorola discrete opto division also has several high sensitivity detectors and emitters which match up well to the MC3373 system.

FIGURE 1 — REMOTE CONTROL APPLICATION
40 kHz CARRIER



CONSUMER ELECTRONIC PRODUCTS

ENTERTAINMENT RADIO RECEIVER CIRCUITS

Device	Function	Page
MC3340P	Electronic Attenuator	9-67
MC13020P	C-QUAM* AM Stereo Decoder	9-108
MC13022	Advanced Medium Voltage AM Stereo Decoder	9-113
MC13023	C-QUAM* AM Receiver Front End and Tuner Stabilizer	9-117
MC13024	Low Voltage Motorola C-QUAM* AM Stereo Receiver	9-123
MC13041	AM Receiver Subsystem	9-128
MC13060	Mini-Watt Audio Output	9-134
MC34119	Low Power Audio Amplifier	9-138
TDA1524A	Stereo Tone Control System	9-161

VIDEO CIRCUITS

Device	Function	Page
CA3054	Dual Differential Amplifier	9-9
CA3146	General Purpose Transistor Array	9-11
MC1330AP	Low Level Video Detector	9-13
MC1350	IF Amplifier	9-19
MC1357	IF Amplifier and Quadrature Detector	9-23
MC1373	TV Video Modulator Circuit	9-29
MC1374	TV Modulator Circuit	9-32
MC1377	Color Television RGB to PAL/NTSC Encoder	9-40
MC1378	Complete Color TV Video Overlay Synchronizer	9-44
MC1382	Multi-Sync Monitor TTL to Analog Inputs Interface	9-48
MC1383	Multimode Monitor Processor	9-53
MC1384	Multimode Monitor Processor with Vertical Timebase	9-58
MC1391P	TV Horizontal Processor	9-63
MC1733,C	Differential Audio Amplifier	See Chapter 2
MC3346	General Purpose Transistor Array	9-70
MC3373	Remote Control Wideband Amplifier-Detector	9-73
MC10320	Triple 4-Bit Color Palette Video DAC	9-77
MC10320-1	Triple 4-Bit Color Palette Video DAC	9-77
MC13001XP	Monomax Black and White TV Subsystem	9-94
MC13002XP	Monomax Black and White TV Subsystem	9-94
MC13010P	TV Parallel Sound IF and AFT	9-103
MC44301	System 4 High Performance Color TV IF	9-147
MC44602	Current Mode Controller	See Chapter 3
MC44802	PLL Tuning Circuit with 1.3 GHz Prescaler	9-153
NE592	Video Amplifier	See Chapter 2
SE592	Video Amplifier	See Chapter 2
TDA3190P	TV Sound System	9-166
TDA3301B	TV Color Processor	9-169
TDA3303	TV Color Processor	9-169
TDA3330	TV Color Processor	9-183

REMOTE CONTROL CIRCUIT

Device	Function	Page
MC3373	Remote Control Wideband Amplifier-Detector	9-73

RELATED APPLICATION NOTES

Application Note	Title	Related Device
AN545A	Television Video IF Amplifier Using Integrated Circuits	MC1350
AN829	Application of the MC1374 TV Modulator	MC1374
AN879	Monomax-Application of the MC13001 Monochrome TV IC	MC13001
AN932	Application of the MC1377 Color Encoder	MC1377
AN1016	Infrared Sensing and Data Transmission Fundamentals	MC3373
AN1019	NTSC Decoding Using the TDA3330, with Emphasis on Cable In/Cable Out Option	TDA3330
AN1044	The MC1378 — A Monolithic Composite Video Synchronizer	MC1378
ANHK07	A High Performance, Manual-Tuned AM Stereo Receiver for Automotive Application Using Motorola ICs: MC13020, MC13021 and MC13041	MC13020,21 MC1378, MC3373, TDA3330

CA3054

DUAL INDEPENDENT DIFFERENTIAL AMPLIFIER

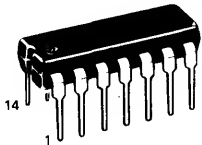
**DUAL DIFFERENTIAL
AMPLIFIER**

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**

The CA3054 consists of two independent differential amplifiers with associated constant-current transistors on a common monolithic substrate. The six NPN transistors which comprise the amplifiers are general purpose devices useful from dc to 120 MHz.

The monolithic construction of the CA3054 provides close electrical and thermal matching of the amplifiers which makes this device particularly useful in dual channel applications where matched performance of the two channels is required.

- Two Differential Amplifiers on a Common Substrate
- Independently Accessible Inputs and Outputs
- Maximum Input Offset Voltage — ± 5.0 mV



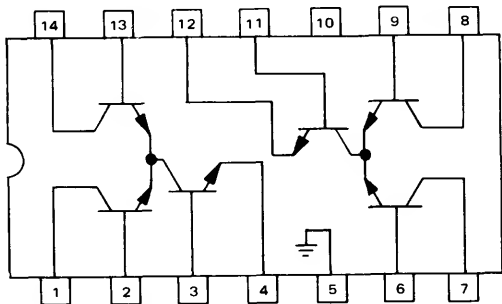
P SUFFIX
PLASTIC PACKAGE
CASE 646

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CE0}	15	Vdc
Collector-Base Voltage	V_{CB0}	20	Vdc
Emitter-Base Voltage	V_{EB0}	5.0	Vdc
Collector-Substrate Voltage	V_{C10}	20	Vdc
Collector Current — Continuous	I_C	50	mA dc
Junction Temperature	T_J	150	°C
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

9

PIN CONNECTIONS



Pin 5 is connected to substrate and must remain at the lowest circuit potential

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
STATIC CHARACTERISTICS FOR EACH DIFFERENTIAL AMPLIFIER					
Input Offset Voltage ($V_{CB} = 3.0\text{ Vdc}$)	V_{IO}	—	—	5.0	mV
Input Offset Current ($V_{CB} = 3.0\text{ Vdc}$)	I_{IO}	—	—	2.0	μA
Input Bias Current ($V_{CB} = 3.0\text{ Vdc}$)	I_{IB}	—	—	24	μA

STATIC CHARACTERISTICS FOR EACH TRANSISTOR

Base-Emitter Voltage ($V_{CB} = 3.0\text{ Vdc}$, $I_C = 50\text{ }\mu\text{A}$) ($V_{CB} = 3.0\text{ Vdc}$, $I_C = 1.0\text{ mA}$) ($V_{CB} = 3.0\text{ Vdc}$, $I_C = 3.0\text{ mA}$) ($V_{CB} = 3.0\text{ Vdc}$, $I_C = 10\text{ mA}$)	V_{BE}	— — — —	— — — —	0.70 0.80 0.85 0.90	Vdc
Collector Cutoff Current ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$)	I_{CBO}	—	—	100	nA
Collector-Emitter Breakdown Voltage ($I_C = 1.0\text{ mA}$)	$V_{(BR)CEO}$	15	—	—	Vdc
Collector-Base Breakdown Voltage ($I_C = 10\text{ }\mu\text{A}$)	$V_{(BR)CBO}$	20	—	—	Vdc
Collector-Substrate Breakdown Voltage ($I_C = 10\text{ }\mu\text{A}$)	$V_{(BR)CIO}$	20	—	—	Vdc
Emitter-Base Breakdown Voltage ($I_E = 10\text{ }\mu\text{A}$)	$V_{(BR)EBO}$	5.0	—	—	Vdc

CA3146

GENERAL PURPOSE TRANSISTOR ARRAY

ONE DIFFERENTIALLY CONNECTED PAIR AND THREE ISOLATED TRANSISTOR ARRAYS

The CA3146 is designed for general purpose, low power applications in the DC through VHF range.

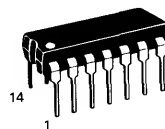
- Guaranteed Base-Emitter Voltage Matching
- Operating Current Range Specified — 10 μ A to 10 mA
- Five General Purpose Transistors in One Package

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CE0}	30	Vdc
Collector-Base Voltage	V_{CBO}	20	Vdc
Collector-Substrate Voltage	V_{CIO}	20	Vdc
Emitter-Base Voltage	V_{EBO}	5.0	Vdc
Collector Current	I_C	50	mA dc
Operating Temperature Range	T_A	-40 to +85	$^{\circ}$ C
Storage Temperature Range	T_{stg}	-65 to +150	$^{\circ}$ C

GENERAL PURPOSE TRANSISTOR ARRAY

SILICON MONOLITHIC INTEGRATED CIRCUITS



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CASE 646



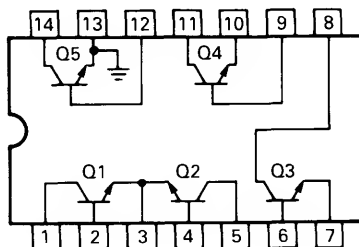
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CASE 751A
(SO-14)

ORDERING INFORMATION

Device	Temperature Range	Package
CA3146D	-40 $^{\circ}$ C to +85 $^{\circ}$ C	SO-14
CA3146P		Plastic DIP

9

PIN CONNECTIONS



Pin 13 is connected to substrate and must remain at the lowest circuit potential.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
STATIC CHARACTERISTICS					
Collector-Base Breakdown Voltage ($I_C = 10 \mu\text{A}$)	$V_{(BR)CBO}$	40	89	—	Vdc
Collector-Emitter Breakdown Voltage ($I_C = 1.0 \text{ mA}$)	$V_{(BR)CEO}$	35	45	—	Vdc
Collector-Substrate Breakdown Voltage ($I_{C1} = 10 \mu\text{A}$)	$V_{(BR)CIO}$	40	85	—	Vdc
Emitter-Base Breakdown Voltage ($I_E = 10 \mu\text{A}$)	$V_{(BR)EBO}$	5.0	—	—	Vdc
Collector-Base Cutoff Current ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$)	I_{CBO}	—	0.68	40	nA
DC Current Gain ($I_C = 10 \text{ mA}$, $V_{CE} = 5.0 \text{ Vdc}$) ($I_C = 1.0 \text{ mA}$, $V_{CE} = 5.0 \text{ Vdc}$)	h_{FE}	— —	171 188	— —	—
Base-Emitter Voltage ($V_{CE} = 5.0 \text{ Vdc}$, $I_E = 1.0 \text{ mA}$)	V_{BE}	—	0.7	—	Vdc
Collector-Emitter Saturation Voltage ($I_C = 10 \text{ mA}$, $I_B = 0.4 \text{ mA}$)	$V_{CE(sat)}$	—	0.28	0.5	Vdc
Magnitude of Input Offset Current $ I_{O1} - I_{O2} $ ($V_{CE} = 5.0 \text{ Vdc}$, $I_{C1} = I_{C2} = 1.0 \text{ mA}$)	I_{IO}	—	0.03	2.0	μA
Magnitude of Input Offset Voltage $ V_{BE1} - V_{BE2} $ ($V_{CE} = 5.0 \text{ Vdc}$, $I_E = 1.0 \text{ mA}$)	$ V_{IO} $	—	0.13	2.0	mVdc
DYNAMIC CHARACTERISTICS					
Low Frequency Noise Figure ($V_{CE} = 5.0 \text{ Vdc}$, $I_C = 100 \mu\text{A}$, $R_S = 1.0 \text{ k}\Omega$, $f = 1.0 \text{ kHz}$)	NF	—	3.25	—	dB
Forward Current Transfer Ratio ($V_{CE} = 5.0 \text{ Vdc}$, $I_C = 1.0 \text{ mA}$, $f = 1.0 \text{ kHz}$)	h_{fe}	—	201.5	—	—
Short Circuit Input Impedance ($V_{CE} = 5.0 \text{ Vdc}$, $I_C = 1.0 \text{ mA}$, $f = 1.0 \text{ kHz}$)	h_{ie}	—	6.7	—	kohm
Open Circuit Output Impedance ($V_{CE} = 5.0 \text{ Vdc}$, $I_C = 1.0 \text{ mA}$, $f = 1.0 \text{ kHz}$)	h_{oe}	—	15.6	—	μmho
Reverse Voltage Transfer Ratio ($V_{CE} = 5.0 \text{ Vdc}$, $I_C = 1.0 \text{ mA}$, $f = 1.0 \text{ kHz}$)	h_{re}	—	3.5	—	$\times 10^{-4}$
Input Admittance ($V_{CE} = 5.0 \text{ Vdc}$, $I_C = 1.0 \text{ mA}$, $f = 1.0 \text{ MHz}$)	Y_{ie}	—	$0.14 + j0.16$	—	mho
Forward Transfer Admittance ($V_{CE} = 5.0 \text{ Vdc}$, $I_C = 1.0 \text{ mA}$, $f = 1.0 \text{ MHz}$)	Y_{fe}	—	$34.6 - j0.63$	—	mho
Reverse Transfer Admittance ($V_{CE} = 5.0 \text{ Vdc}$, $I_C = 1.0 \text{ mA}$, $f = 1.0 \text{ MHz}$)	Y_{re}	—	$62.0 - j59.4$	—	μmho
Output Admittance ($V_{CE} = 5.0 \text{ Vdc}$, $I_C = 1.0 \text{ mA}$, $f = 1.0 \text{ MHz}$)	Y_{oe}	—	$0.16 + j0.14$	—	mho
Current Gain — Bandwidth Product ($V_{CE} = 5.0 \text{ Vdc}$, $I_C = 3.0 \text{ mA}$)	f_T	300	500	—	MHz
Emitter-Base Capacitance ($V_{EB} = 5.0 \text{ Vdc}$, $I_E = 0 \text{ mA}$)	C_{EB}	—	1.17	—	pF
Collector-Base Capacitance ($V_{CB} = 5.0 \text{ Vdc}$, $I_E = 0 \text{ mA}$)	C_{CB}	—	0.68	—	pF
Collector-Substrate Capacitance ($V_{CS} = 5.0 \text{ Vdc}$, $I_C = 0 \text{ mA}$)	C_{CI}	—	1.92	—	pF

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

MC1330AP

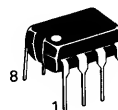
LOW-LEVEL VIDEO DETECTOR

... an integrated circuit featuring very linear video characteristics and wide bandwidth. Designed for color and monochrome television receivers, replacing the third IF, detector, video buffer and AFC buffer.

- Conversion Gain — 33 dB (Typ)
- Excellent Differential Phase and Gain
- High Rejection of IF Carrier Feedthrough
- High Video Output — 8.0 V(p-p)
- Fully Balanced Detector
- Output Temperature Compensated
- Improved Version of the MC1330P

LOW-LEVEL VIDEO DETECTOR

SILICON MONOLITHIC
INTEGRATED CIRCUIT

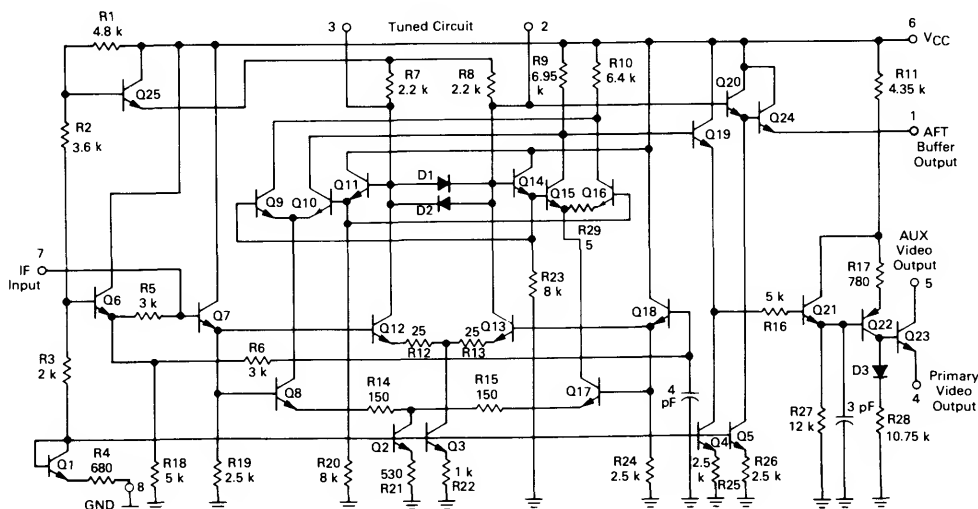


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PLASTIC PACKAGE
CASE 626

MAXIMUM RATINGS

Rating	Value	Unit
Power Supply Voltage	24	Vdc
DC Video Output Current	5.0	mAdc
DC AFT Output Current	2.0	mAdc
Junction Temperature	150	°C
Operating Ambient Temperature Range	0 to 75	°C
Storage Temperature Range	- 65 to +150	°C

FIGURE 1 — CIRCUIT SCHEMATIC



MC1330AP

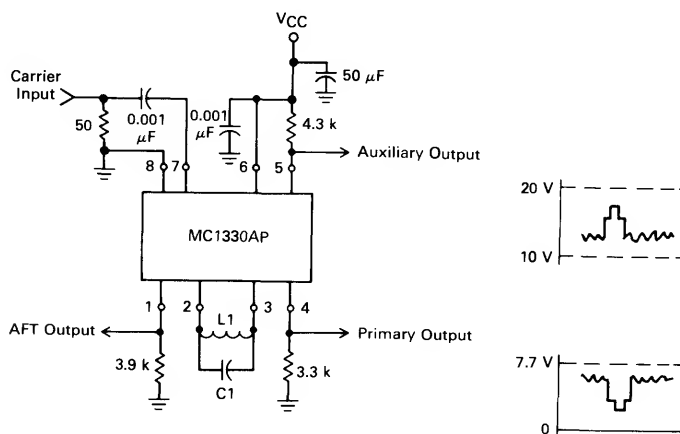
ELECTRICAL CHARACTERISTICS ($V_{CC} = +20$ Vdc, $Q = 40$, $f_c = 45.75$ MHz, $T_A = +25^\circ\text{C}$ unless otherwise noted)

Characteristic	Pin	Min	Typ	Max	Unit
Zero Signal dc Output Voltage	4	7.0	—	8.7	Vdc
Supply Current	5, 6	11	17.5	24	mA
Maximum Signal dc Output Voltage	4	—	0	0.5	Vdc
Conversion Gain for 1.0 Vp-p Output (30% Modulation)	7	25	36	65	mVrms
AFT Buffer Output at Carrier Frequency	1	300	475	650	mVp-p

DESIGN CHARACTERISTICS ($V_{CC} = +20$ Vdc, $Q = 40$, $f_c = 45.75$ MHz, $T_A = +25^\circ\text{C}$ unless otherwise noted)

Characteristic		Pin	Typ	Unit
Input Resistance		7	4.9	kΩ
Input Capacitance		7	1.5	pF
Internal Resistance (Across Tuned Circuit)		2, 3	4.4	kΩ
Internal Capacitance (Across Tuned Circuit)		2, 3	1.0	pF
Negative Video Output Bandwidth (Figure 10)		4	10.8	MHz
Positive Video Output Bandwidth (Figure 10)		5	2.2	MHz
Differential Phase @ 3.58 MHz, 100% Modulated Staircase, 3.0 Vp-p Detected Video Pin 5 Tied to Pin 6		4	7.0	Degrees
Differential Gain @ 3.58 MHz, 100% Modulated Staircase, 3.0 Vp-p Detected Video Pin 5 Tied to Pin 6		4	4.0	%
Differential Phase @ 3.58 MHz, 100% Modulated Staircase, 3.0 Vp-p Detected Video, R Pin 5 = 4.3 kΩ		4	8.0	Degrees
Differential Gain @ 3.58 MHz, 100% Modulated Staircase, 3.0 Vp-p Detected Video, R Pin 5 = 4.3 kΩ		4	6.0	%
920 kHz Beat Output (dB Below 100% Modulated Video, See Figure 11) 45.75 MHz = Reference 42.17 MHz = -6.0 dB 41.25 MHz = -20 dB		4	-38	dB
Video Output Resistance @ 1.0 MHz, 2.0 mA		4	94	Ω
Input Overload (Carrier Level at Input to Pin 4, Primary Output to go Positive 0.1 Vdc from Ground.) VCC = 12 Vdc VCC = 15 Vdc VCC = 20 Vdc VCC = 24 Vdc		7	2.0 2.6 3.6 4.6	Volts
Power Supply Voltage Range		5	10 to 24	Volts

FIGURE 2 — TEST FIXTURE CIRCUIT



L1, C1: See General Information Number 3, page 5 of this specification.

MC1330AP

FIGURE 3 — INPUT ADMITTANCE

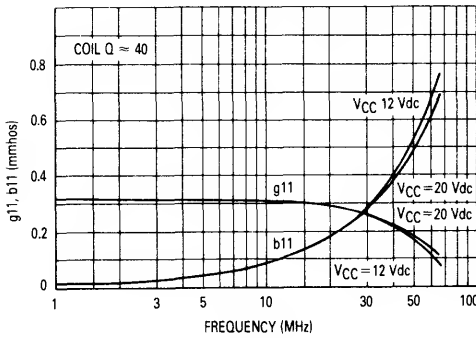
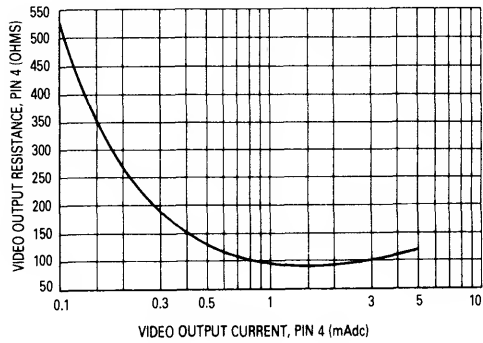


FIGURE 4 — VIDEO DETECTOR OUTPUT RESISTANCE



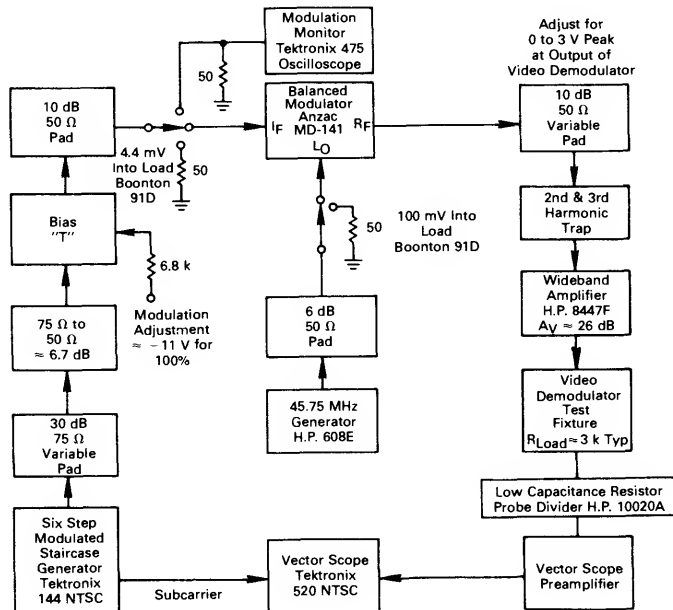
CIRCUIT DESCRIPTION

The MC1330AP video detector is a fully balanced multiplier detector circuit that has linear amplitude and phase characteristics. The signal is divided into two channels, one a linear amplifier and the other a limiting amplifier that provides the switching carrier for the detector.

The switching carrier has a buffered output for use in providing the AFT function.

The video amplifier output is an improved design that reduces the differential gain and phase distortion associated with previous video output systems. The output is wide band, > 8.0 MHz, with normal negative polarity. A separate narrow bandwidth, positive video output is also provided.

FIGURE 5 — DIFFERENTIAL PHASE AND GAIN TEST SET UP



TYPICAL CHARACTERISTICS

($V_{CC} = +20$ Vdc, $T_A = +25^\circ\text{C}$ Unless Otherwise Noted)

FIGURE 6 — OUTPUT VOLTAGE TRANSFER FUNCTION

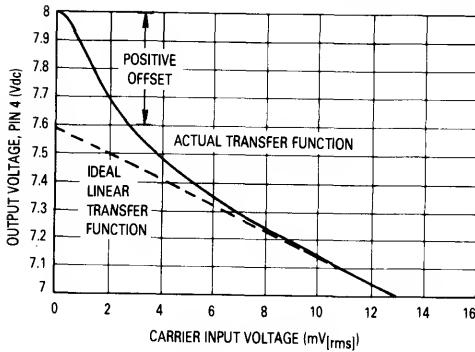


FIGURE 7 — OUTPUT VOLTAGE TRANSFER FUNCTION

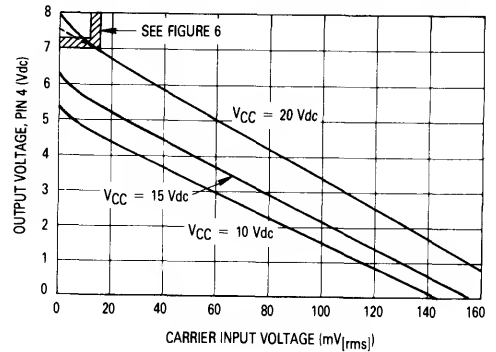


FIGURE 8 — OUTPUT VOLTAGE, SUPPLY CURRENT

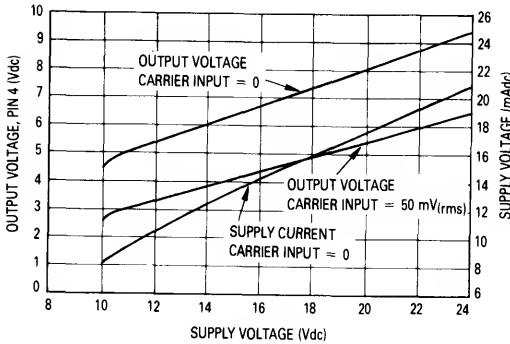


FIGURE 9 — AFT LIMITING

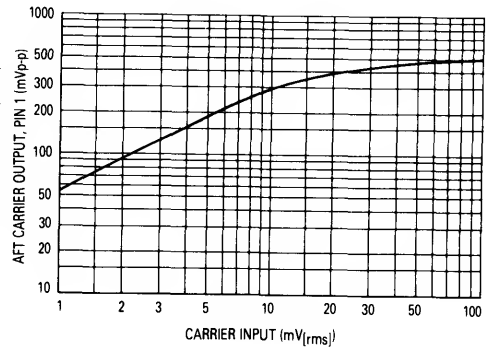


FIGURE 10 — VIDEO OUTPUT RESPONSE

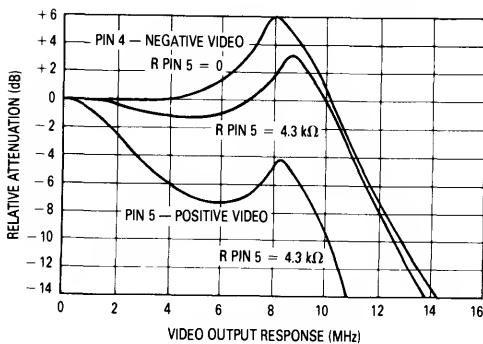
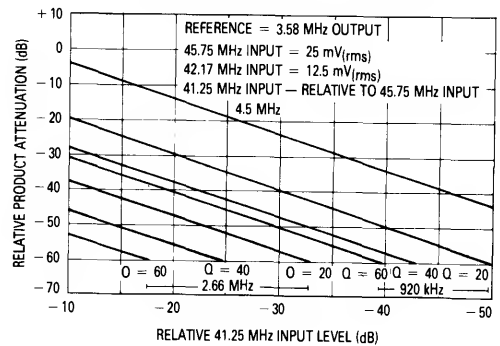


FIGURE 11 — VIDEO OUTPUT PRODUCTS



TV-IF Amplifier Information

A very compact high performance IF amplifier constructed as shown in Figure 14 minimizes the number of overall components and alignment adjustments. It can be readily combined with normal tuners and input tuning-trapping circuitry to provide the performance demanded of high quality receivers. This configuration will provide approximately 93 dB voltage gain and can accommodate the usual low impedance input network or, if desired, can take advantage of an impedance step-up from tuner to MC1350P input.

The burden of selectivity, formerly found between the third IF and detector, must now be placed at the interstage. The nominal 3.0 volt peak-to-peak output can be varied from 0 to 7.0 V with excellent linearity and freedom from spurious output products.

Alignment is most easily accomplished with an AM generator, set at a carrier frequency of 45.75 MHz, modulated with a video frequency sweep. This provides the proper realistic conditions necessary to operate to low-level detector (LLD). The detector tank is first adjusted for maximum detected dc (with a CW input). Next, the video sweep modulation is applied and the interstage and input circuits aligned, step by step, as in a standard IF amplifier.

Note: A normal IF sweep generator, essentially an FM generator, will not serve properly without modification. The LLD tank attempts to "follow" the sweep input frequency, and results in variations of switching amplitude in the detector. Hence, the apparent overall response becomes modified by the response of the LLD tank, which a real signal doesn't do.

This effect can be prevented by resistively adding a 45.75 MHz CW signal to the output of the sweep generator approximately 3.0 dB greater than the sweep amplitude. See Figures 12 and 13 below. For a more detailed description of the MC1330AP see application note AN545A.

General Information

The MC1330AP offers the designer a new approach to an old problem. Now linear detection can be per-

formed at much lower power signal levels than possible with a detector diode.

Offering a number of distinct advantages, its easy implementation should meet with ready acceptance for television designs. Some specific features and information on systems design with this device are given below:

1. The device provides excellent linearity of output versus input, as shown in Figures 6 and 7. These graphs also show that video peak-to-peak amplitude (ac) does not change with supply voltage variation. (Slopes are parallel. Visualize a given variation of input CW and use the figure as a transfer function.)
2. The dc output level does change linearly with supply voltage shown in Figure 8. This can be accommodated by regulating the supply or by referencing the subsequent video amplifier to the same power supply.
3. The choice of Q for the tuned circuit of Pin 2 and 3 is not critical. The higher the Q, the better the rejection of 920 kHz products but the more critical the tuning accuracy required. See Figure 11. Values of Q from 20 to 50 are recommended. (Note the internal resistance.)
4. A video output with positive-going sync is available at Pin 5 if required. This signal has a higher output impedance than Pin 4 so it must be handled with greater care. If not used, Pin 5 may be connected directly to the supply voltage (Pin 6). The video response will be altered somewhat. See Figure 10.
5. An AFT output (Pin 1) provides 460 mV of IF carrier output, sufficient voltage to drive an AFT ratio detector, with only one additional stage.
6. AGC lockout can occur if the input signal presented in the MC1330AP is greater than that shown in the input overload section of the design characteristics shown on Page 3. If these values are exceeded, the turns ratio between the primary and secondary of T_1 should be increased. Another solution to the problem is to use an input clamp diode D_1 shown in Figure 14.
7. The total I.F. noise figure at high gain reductions can be improved by reflecting ≈ 1.0 k source impedance to the input of the MC1330AP. This will cause some loss in overall IF voltage gain.

FIGURE 12 — BYPASS DISPLAYED BY CONVENTIONAL SWEEP

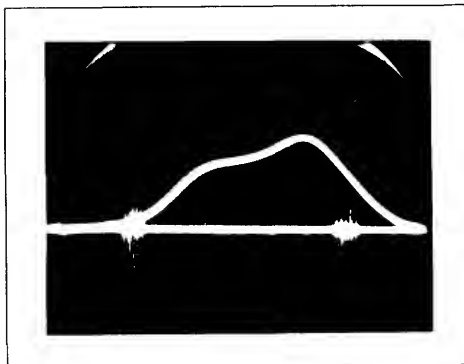
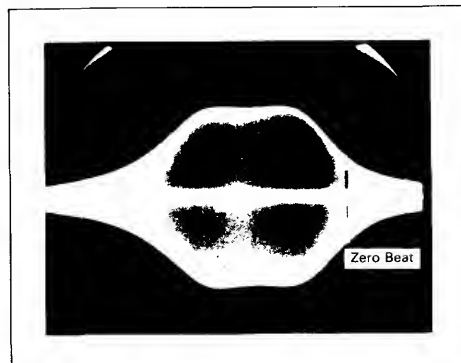


FIGURE 13 — BYPASS DISPLAY WITH THE ADDITION OF CARRIER INJECTION



9

[illegible]

L1 wound with #26 AWG tinned nylon acetate wire tuned by distorting winding.

The schematic diagram illustrates the internal circuitry of the MC1350P integrated circuit. Key components include:

- Resistors:** R1, R2, R3, R4, R5, R6, R7.
- Capacitors:** C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14.
- Transistor:** T1.
- Inductor:** L1.
- External Connections:** INPUT, AGC, VIDEO, AFT, and a +Vdc supply.

The circuit shows a complex arrangement of these components, including a feedback loop with R1 and C1, a variable gain stage with R2, C2, and C3, and a video output stage with R4, C4, and C5. The AFT (Automatic Frequency Tuning) section includes R6, C14, and L1. The +Vdc supply is connected to the circuit through R7 and C12.

MC1350

MONOLITHIC IF AMPLIFIER

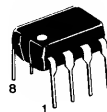
... an integrated circuit featuring wide range AGC for use as an IF amplifier in radio and TV over the temperature range 0 to +75°C.

- Power Gain — 50 dB Typ at 45 MHz
 — 48 dB Typ at 58 MHz
- AGC Range — 60 dB Min, dc to 45 MHz
- Nearly Constant Input and Output Admittance Over the Entire AGC Range
- y_{21} Constant (–3.0 dB) to 90 MHz
- Low Reverse Transfer Admittance — $<< 1.0 \mu\text{mho}$ Typ
- 12 Volt Operation, Single-Polarity Power Supply

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+	+18	Vdc
Output Supply Voltage	V_1, V_8	+18	Vdc
AGC Supply Voltage	V_{AGC}	V^+	Vdc
Differential Input Voltage	V_{in}	5.0	Vdc
Power Dissipation (Package Limitation)	P_D	625	mW
Plastic Package Derate above 25°C		5.0	mW/°C
Operating Temperature Range	T_A	0 to +75	°C

IF AMPLIFIER SILICON MONOLITHIC INTEGRATED CIRCUIT

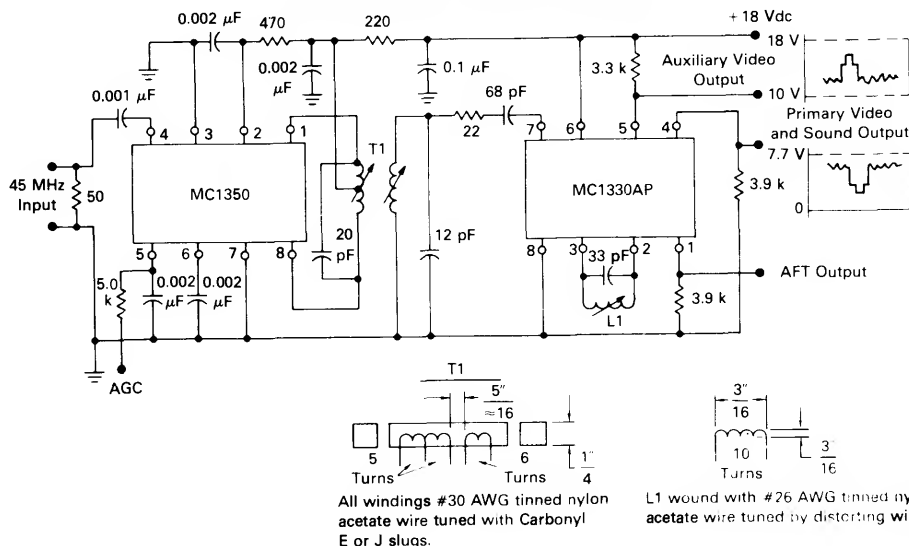


P SUFFIX
 PLASTIC PACKAGE
 CASE 626



D SUFFIX
 PLASTIC PACKAGE
 CASE 751
 (SO-8)

**FIGURE 1 — TYPICAL MC1350 VIDEO IF AMPLIFIER
 AND MC1330 LOW-LEVEL VIDEO DETECTOR CIRCUIT**



MC1350

ELECTRICAL CHARACTERISTICS ($V^+ = +12\text{ Vdc}$; $T_A = +25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
AGC Range, 45 MHz (5.0 V to 7.0 V) (Figure 1)		60	68	—	dB
Power Gain (Pin 5 grounded via a 5.1 k Ω resistor) $f = 58\text{ MHz}$, BW = 4.5 MHz See Figure 6(a) $f = 45\text{ MHz}$, BW = 4.5 MHz See Figure 6(a),(b) $f = 10.7\text{ MHz}$, BW = 350 kHz See Figure 7 $f = 455\text{ kHz}$, BW = 20 kHz	A_p	— 46 — —	48 50 58 62	— — — —	dB
Maximum Differential Voltage Swing 0 dB AGC -30 dB AGC	V_o	— —	20 8.0	— —	V_{p-p}
Output Stage Current (Pins 1 and 8)	$I_1 + I_8$	—	5.6	—	mA
Total Supply Current (Pins 1, 2 and 8)	I_S	—	14	17	mA _{dc}
Power Dissipation	P_D	—	168	204	mW

DESIGN PARAMETERS, Typical Values ($V^+ = +12\text{ Vdc}$, $T_A = +25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Frequency				Unit
		455 kHz	10.7 MHz	45 MHz	58 MHz	
Single-Ended Input Admittance	g_{11} b_{11}	0.31 0.022	0.36 0.50	0.39 2.30	0.5 2.75	mmho
Input Admittance Variations with AGC (0 to 60 dB)	Δg_{11} Δb_{11}	— —	— —	60 0	— —	μmho
Differential Output Admittance	g_{22} b_{22}	4.0 3.0	4.4 110	30 390	60 510	μmho
Output Admittance Variations with AGC (0 to 60 dB)	Δg_{22} Δb_{22}	— —	— —	4.0 90	— —	μmho
Reverse Transfer Admittance (Magnitude)	$ Y_{12} $	$\ll 1.0$	$\ll 1.0$	$\ll 1.0$	$\ll 1.0$	μmho
Forward Transfer Admittance Magnitude Angle (0 dB AGC) Angle (-30 dB AGC)	$ Y_{21} $ $\angle Y_{21}$ $\angle Y_{21}$	160 -5.0 -3.0	160 -20 -18	200 -80 -69	180 -105 -90	mmho degrees degrees
Single-Ended Input Capacitance	C_{in}	7.2	7.2	7.4	7.6	pF
Differential Output Capacitance	C_o	1.2	1.2	1.3	1.6	pF

FIGURE 2 — TYPICAL GAIN REDUCTION
(Figures 6 and 7)

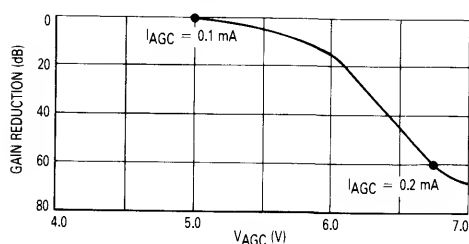
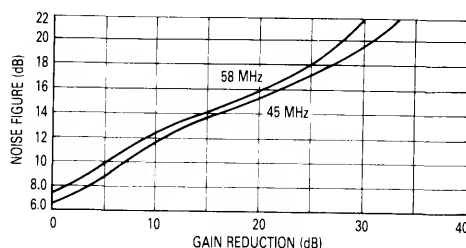


FIGURE 3 — NOISE FIGURE
(Figure 6)

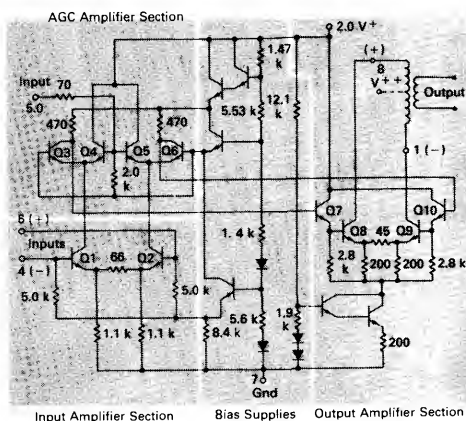


MC1350

GENERAL OPERATING INFORMATION

The input amplifiers (Q1 and Q2) operate at constant emitter currents so that input impedance remains independent of AGC action. Input signals may be applied single-ended or differentially (for ac) with identical results. Terminals 4 and 6 may be driven from a transformer, but a dc path from either terminal to ground is not permitted.

FIGURE 4 — CIRCUIT SCHEMATIC



AGC action occurs as a result of an increasing voltage on the base of Q4 and Q5 causing these transistors to conduct more heavily thereby shunting signal current from the interstage amplifiers Q3 and Q6. The output amplifiers are supplied from an active current source to maintain constant quiescent bias thereby holding output admittance nearly constant. Collector voltage for the output amplifier must be supplied through a center-tapped tuning coil to Pins 1 and 8. The 12-volt supply (V+) at Pin 2 may be used for this purpose, but output admittance remains more nearly constant if a separate 15-volt supply (V++) is used, because the base voltage on the output amplifier varies with AGC bias.

FIGURE 5 — TEST CIRCUIT RESPONSE CURVE (45 and 58 MHz)

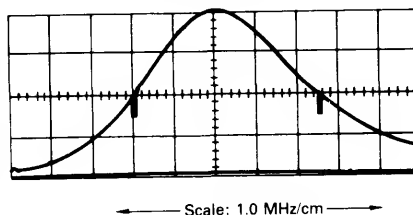
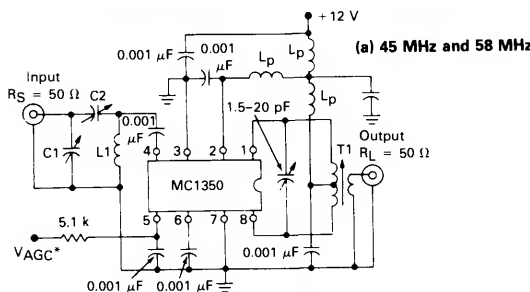


FIGURE 6 — POWER GAIN, AGC AND NOISE FIGURE TEST CIRCUITS



*Connect to ground for maximum power gain test.
All power-supply chokes (L_p), are self-resonant at input frequency. $L_p \approx 20$ k Ω
See Figure 5 for frequency response curve.

L1 @ 45 MHz = 7 1/4 Turns on a 1/4" coil form.

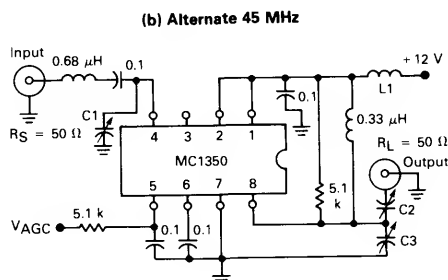
@ 58 MHz = 6 Turns on a 1/4" coil form

T1 Primary Winding = 18 Turns on a 1/4" coil form, center-tapped, #26 AWG

Secondary Winding = 2 Turns centered over Primary Winding @ 45 MHz

= 1 Turn @ 58 MHz

Slug = Carbonyl E or J



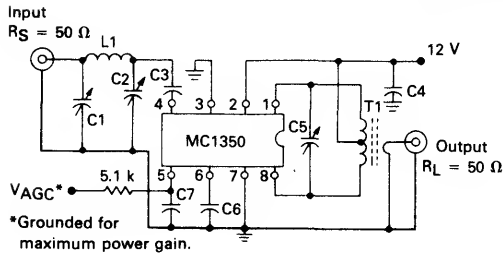
Ferrite Core	
L1	14 Turns 28 S.W.G
C1	5-25 pF
C2	5-25 pF
C3	5-25 pF

	45 MHz		58 MHz	
L1	0.4 μ H	$Q \geq 100$	0.3 μ H	$Q \geq 100$
T1	1.3-3.4 μ H	$Q \geq 100$ @ 2.0 μ H	1.2-3.8 μ H	$Q \geq 100$ @ 2.0 μ H
C1	50-160 pF		8-60 pF	
C2	8-60 pF		3-35 pF	

MC1350

GENERAL OPERATING INFORMATION (continued)

FIGURE 7 — POWER GAIN AND AGC TEST CIRCUIT
(455 kHz and 10.7 MHz)



Component	Frequency	
	455 kHz	10.7 MHz
C1	—	80–450 pF
C2	—	5.0–80 pF
C3	0.05 μ F	0.001 μ F
C4	0.05 μ F	0.05 μ F
C5	0.001 μ F	36 pF
C6	0.05 μ F	0.05 μ F
C7	0.05 μ F	0.05 μ F
L1	—	4.6 μ H
T1	Note 1	Note 2

Note 1. Primary: 120 μ H (center-tapped)

$Q_U = 140$ at 455 kHz

Primary: Secondary turns ratio ≈ 13

Note 2. Primary: 6.0 μ H

Primary winding = 24 turns #36 AWG
(close-wound on 1/4" dia. form)

Core = Carbonyl E or J

Secondary winding = 1-1/2 turns #36 AWG, 1/4" dia.
(wound over center-tap)

TYPICAL CHARACTERISTICS

($V^+ = 12$ V, $T_A = +25^\circ$ C)

FIGURE 8 — SINGLE-ENDED INPUT ADMITTANCE

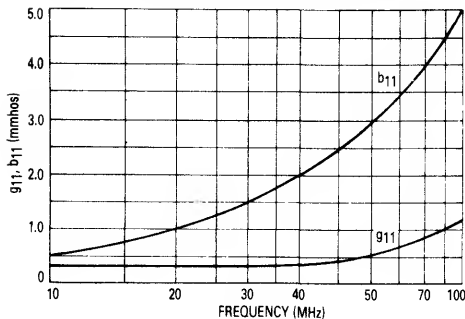


FIGURE 9 — FORWARD TRANSFER ADMITTANCE

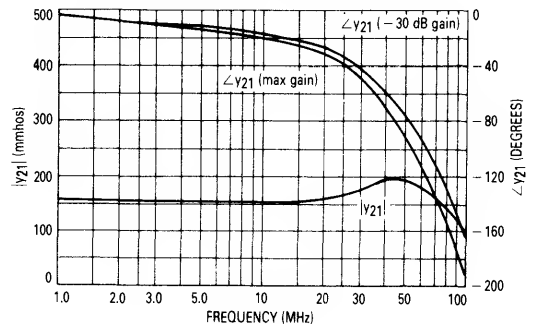


FIGURE 10 — DIFFERENTIAL OUTPUT ADMITTANCE

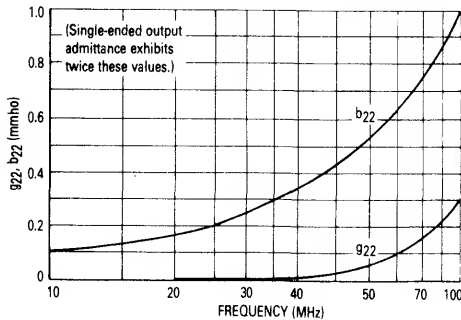
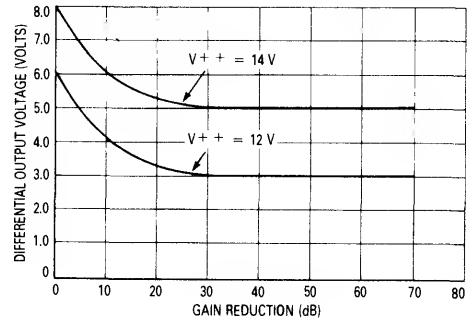


FIGURE 11 — DIFFERENTIAL OUTPUT VOLTAGE



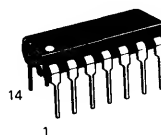
MC1357

**TV SOUND IF OR FM IF AMPLIFIER
 WITH QUADRATURE DETECTOR**

**IF AMPLIFIER
 WITH QUADRATURE
 DETECTOR**

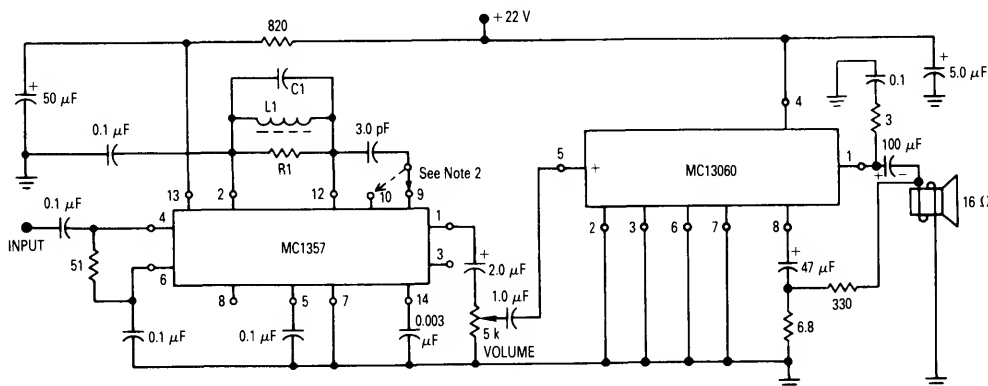
**SILICON MONOLITHIC
 INTEGRATED CIRCUIT**

- A Direct Replacement for the ULN2111A
- Greatly Simplified FM Demodulator Alignment
- Excellent Performance at $V_{CC} = 8.0 \text{ Vdc}$



P SUFFIX
 PLASTIC PACKAGE
 CASE 646

FIGURE 1 — TV TYPICAL APPLICATION CIRCUIT



Typical Performance
 2 Watts Output
 2% Distortion
 250 μV Sensitivity (3 dB Lim.)

$C1 = 120 \text{ pF}$
 $L1 = 14 \mu\text{H}$
 $R1 = 20 \text{ k}\Omega$
 $Q = 30$

MC1357

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Value	Unit
Power Supply Voltage	16	Vdc
Input Voltage (Pin 4)	3.5	V _p
Power Dissipation (Package Limitation) Plastic Packages Derate above T _A = +25°C	625 5.0	mW mW/°C
Operating Temperature Range (Ambient)	0 to +70	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
Drain Current V _{CC} = 8.0 V V _{CC} = 12 V	13	10 —	12 15	19 21	mA
Amplifier Input Reference Voltage	6	—	1.45	—	Vdc
Detector Input Reference Voltage	2	—	3.65	—	Vdc
Amplifier High Level Output Voltage	10	1.25	1.45	1.65	Vdc
Amplifier Low Level Output Voltage	9	—	0.145	0.2	Vdc
Detector Output Voltage V _{CC} = 8.0 V V _{CC} = 12 V	1	— —	3.7 5.4	— —	Vdc
Amplifier Input Resistance	4	—	5.0	—	kΩ
Amplifier Input Capacitance	4	—	11	—	pF
Detector Input Resistance	12	—	70	—	kΩ
Detector Input Capacitance	12	—	2.7	—	pF
Amplifier Output Resistance	10	—	60	—	ohm
Detector Output Resistance	1	—	200	—	ohm
De-Emphasis Resistance	14	—	8.8	—	kΩ

DYNAMIC CHARACTERISTICS FM Modulation Freq. = 1.0 kHz, Source Resistance = 50 ohms, T_A = +25°C for all tests. (V_{CC} = 12 Vdc, f_o = 4.5 MHz, Δf = ±25 kHz, Peak Separation = 150 kHz)

Characteristic	Pin	Min	Typ	Max	Unit
Amplifier Voltage Gain (V _{in} ≤ 50 μV[rms])	10	—	60	—	dB
AM Rejection* (V _{in} = 10 mV[rms])	1	—	36	—	dB
Input Limiting Threshold Voltage	4	—	250	—	μV(rms)
Recovered Audio Output Voltage (V _{in} = 10 mV[rms])	1	—	0.72	—	V(rms)
Output Distortion (V _{in} = 10 mV[rms])	1	—	3.0	—	%

(V_{CC} = 12 Vdc, f_o = 5.5 MHz, Δf = ±50 kHz, Peak Separation = 260 kHz)

Amplifier Voltage Gain (V _{in} ≤ 50 μV[rms])	10	—	60	—	dB
AM Rejection* (V _{in} = 10 mV[rms])	1	—	40	—	dB
Input Limiting Threshold Voltage	4	—	250	—	μV(rms)
Recovered Audio Output Voltage (V _{in} = 10 mV[rms])	1	—	1.2	—	V(rms)
Output Distortion (V _{in} = 10 mV[rms])	1	—	5.0	—	%

(V_{CC} = 8.0 Vdc, f_o = 10.7 MHz, Δf = ±75 kHz, Peak Separation = 550 kHz)

Amplifier Voltage Gain (V _{in} ≤ 50 μV[rms])	10	—	53	—	dB
AM Rejection* (V _{in} = 10 mV[rms])	1	—	37	—	dB
Input Limiting Threshold Voltage	4	—	600	—	μV(rms)
Recovered Audio Output Voltage (V _{in} = 10 mV[rms])	1	—	0.3	—	V(rms)
Output Distortion (V _{in} = 10 mV[rms])	1	—	1.4	—	%

(V_{CC} = 12 Vdc, f_o = 10.7 MHz, Δf = ±75 kHz, Peak Separation = 550 kHz)

Amplifier Voltage Gain (V _{in} ≤ 50 μV[rms])	10	—	53	—	dB
AM Rejection* (V _{in} = 10 mV[rms])	1	—	45	—	dB
Input Limiting Threshold Voltage	4	—	600	—	μV(rms)
Recovered Audio Output Voltage (V _{in} = 10 mV[rms])	1	—	0.48	—	V(rms)
Output Distortion (V _{in} = 10 mV[rms])	1	—	1.4	—	%

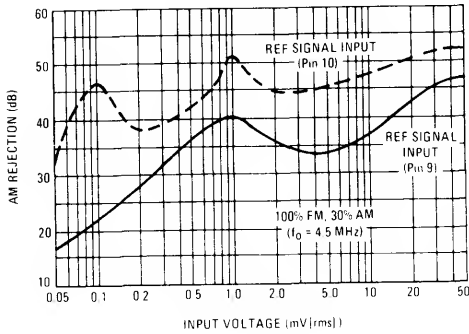
*100% FM, 30% AM Modulation

MC1357

TYPICAL CHARACTERISTICS
($V_{CC} = 12\text{ V}$, $T_A = +25^\circ\text{C}$ unless otherwise noted)
(Use Test Circuit of Figure 13)

($f_0 = 4.5\text{ MHz}$)

FIGURE 2 – AM REJECTION



($f_0 = 5.5\text{ MHz}$)

FIGURE 3 – AM REJECTION

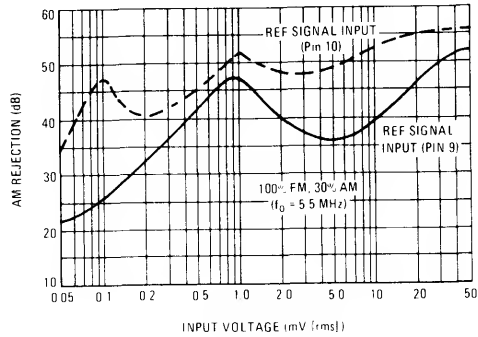


FIGURE 4 – DETECTED AUDIO OUTPUT

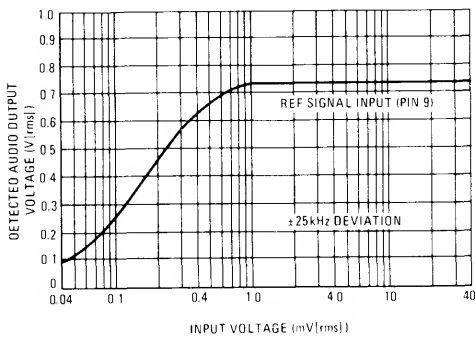


FIGURE 5 – DETECTED AUDIO OUTPUT

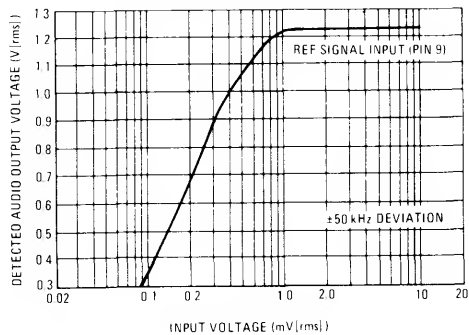


FIGURE 6 – DETECTOR TRANSFER CHARACTERISTIC

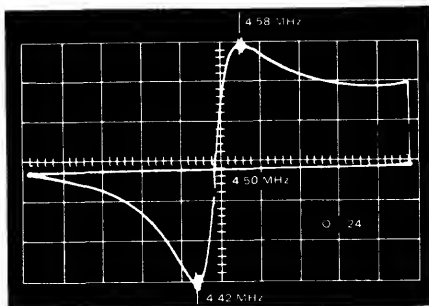
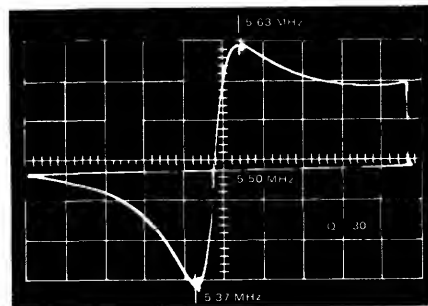


FIGURE 7 – DETECTOR TRANSFER CHARACTERISTIC



TYPICAL CHARACTERISTICS (continued)
 $(f_o = 10.7 \text{ MHz}, T_A = +25^\circ\text{C} \text{ unless otherwise noted.})$
 (Use Test Circuit of Figure 13)

FIGURE 8 — AM REJECTION

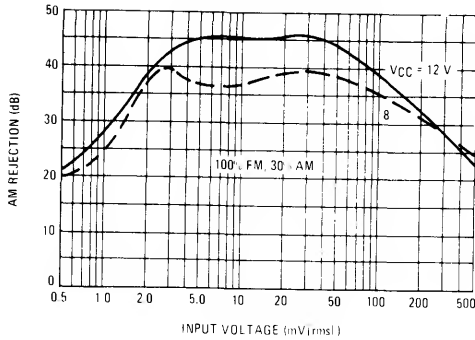
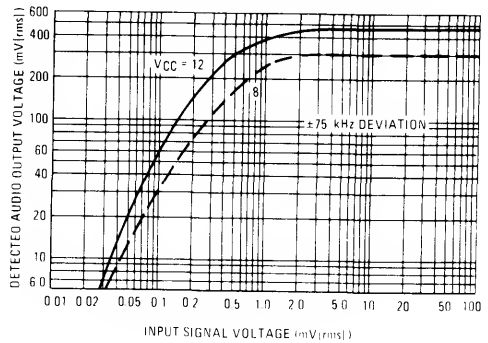
FIGURE 9 — AFC VOLTAGE DRIFT
(1.0 mV INPUT CARRIER @ 10.7 MHz)

FIGURE 10 — LIMITING

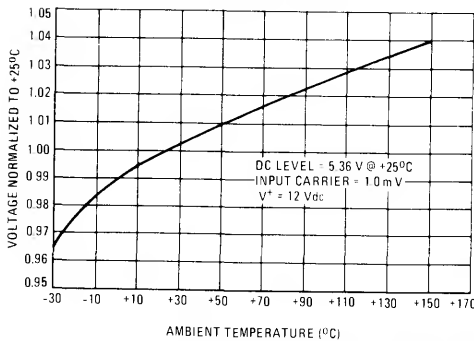


FIGURE 11 — SIGNAL-TO-NOISE RATIO

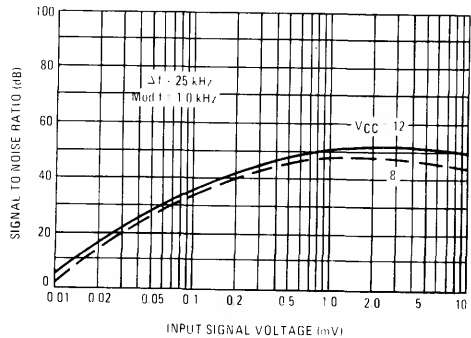


FIGURE 12 — DETECTOR TRANSFER CHARACTERISTIC

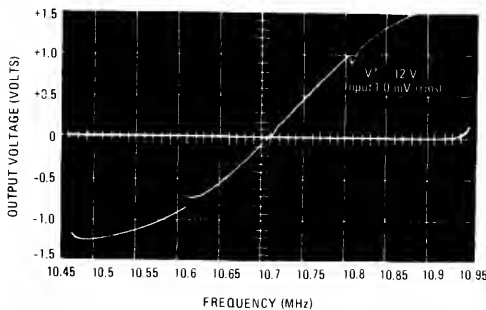


FIGURE 13 — TEST CIRCUIT

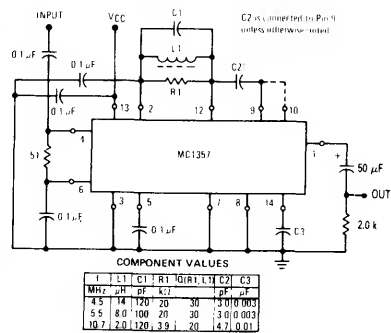
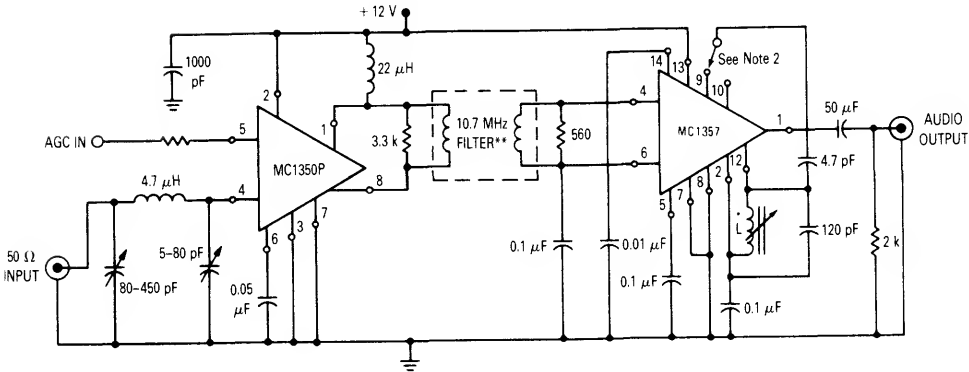


FIGURE 14 – FM RADIO TYPICAL APPLICATION CIRCUIT



Note 1:

Information shown in Figures 15, 16, and 17 was obtained using the circuit of Figure 14.

Note 2:

Optional input to the quadrature coil may be from either pin 9 or pin 10 in the applications shown. Pin 9 has commonly been used on this type of part to avoid overload with various tuning techniques. For this reason, pin 9 is used in tests on the preceding pages (except as noted). However, a significant improvement of limiting sensitivity can be obtained using pin 10, see Figure 17, and no overload problems have been incurred with this tuned circuit configuration.

FIGURE 15 – OUTPUT DISTORTION

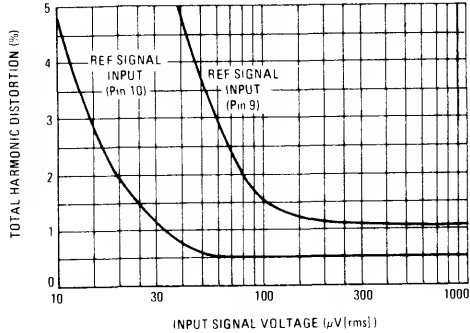


FIGURE 16 – SIGNAL-TO-NOISE RATIO

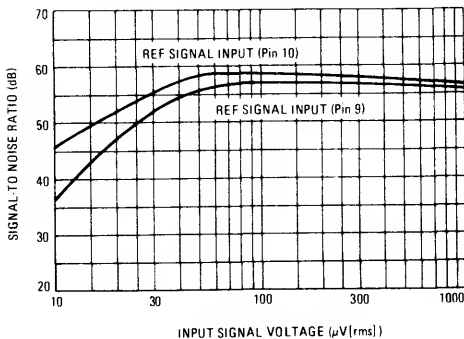
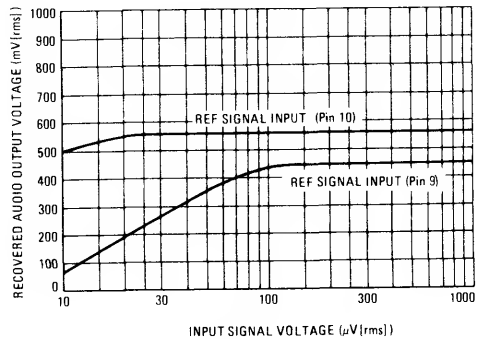
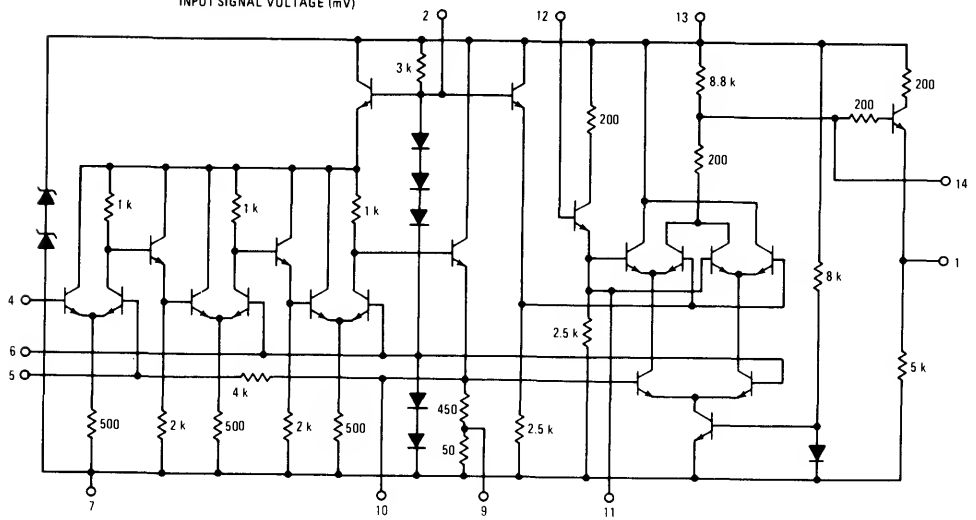


FIGURE 17 – RECOVERED AUDIO OUTPUT



INPUT SIGNAL VOLTAGE (mV)



MC1373

TV VIDEO MODULATOR

... an RF oscillator and dual-input modulator to generate a TV signal from baseband video inputs.

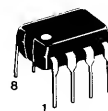
Applications include video games, home computer display, video tape recorders, and test equipment.

The very low level of intermodulation products, compact package and small external component count make this device superior to simple discrete circuits.

- Single 5.0 Vdc Supply
- Channel 3 or 4 Operation
- Excellent Oscillator Stability to 100 MHz
- Color and Sound Compatibility
- Dual Input Modulator for Ease of Signal Handling
- Low Intermodulation (- 50 dB 920 kHz Beat)
- Overmodulation Protection

TV VIDEO MODULATOR CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
 PLASTIC PACKAGE
 CASE 626

PIN CONNECTIONS

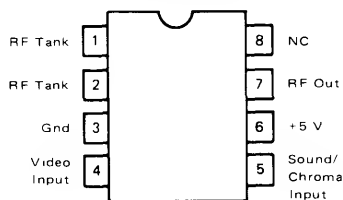
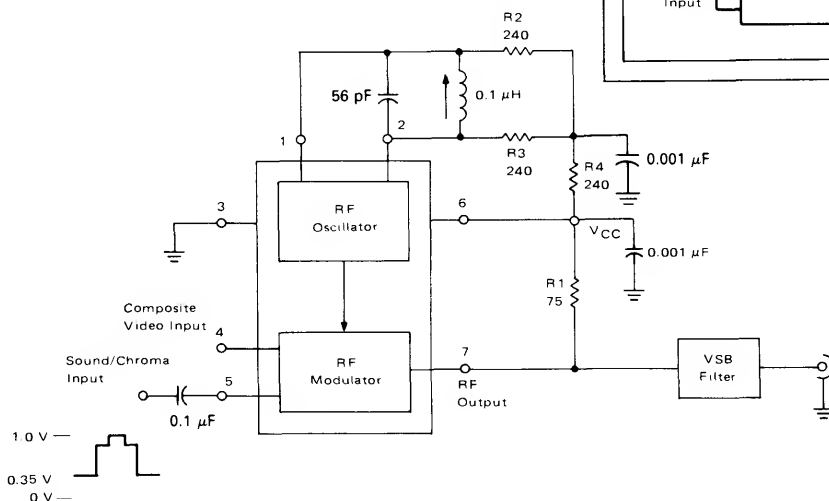
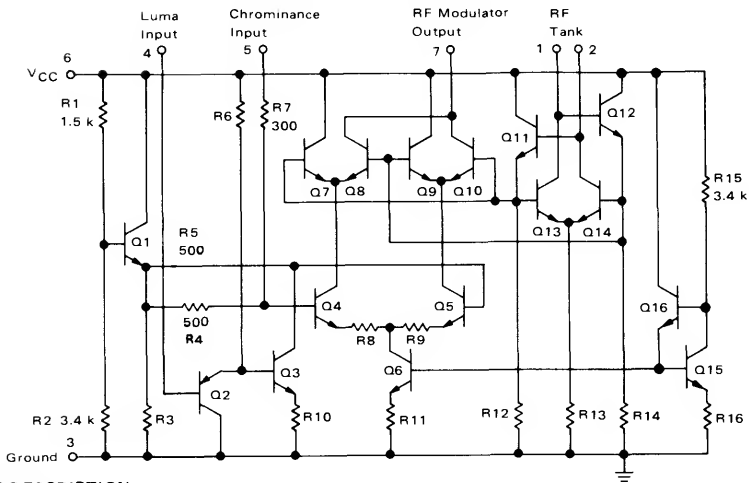


FIGURE 1 - BLOCK DIAGRAM AND APPLICATION CIRCUIT



MC1373

FIGURE 4 – SCHEMATIC DIAGRAM



SCHEMATIC DESCRIPTION

The RF oscillator consists of differential amplifier Q13 and Q14 cross-coupled through emitter followers Q11 and Q12. The oscillator will operate at the parallel resonant frequency of the network connected between pins 1 and 2. The oscillator output is used to switch the doubly balanced RF modulator, Q4 through Q10. Transistors Q2 and Q3 provide level shifting and a high input impedance to the luminance input pin 4. The bases of transistors Q4 and Q5 are both biased through resistors R4 and R5, respectively, to the same dc reference voltage at Q1 emitter. The base voltage at Q5 may only be offset in a negative direction by luminance signal current source Q3. This design insures that overmodulation due to the luminance signal will never occur. The chrominance signal is externally ac coupled to pin 5 where it is reduced by resistor dividers R7 and R4, and added to the luminance signal in Q4. The resultant differential composite video currents are switched at the appropriate RF frequency in Q7 through Q10. The output signal current is presented at pin 7.

Transistors Q15, Q16 and resistors R15, R16 provide a highly stable voltage reference for biasing the current source Q6.

OPERATIONAL DESCRIPTION

Pins 1 and 2 — RF Tank. A tuned circuit connected between these pins determines the RF oscillator frequency. The tuned circuit must provide a low dc resistance shunt. Applying a dc offset voltage between these pins results in baseband composite video at the RF Modulator Output.

Pin 3 – Ground.

Pin 4 – Luminance Input. Input to RF modulator. This pin accepts a dc coupled luminance and sync signal. The amplitude of the RF signal output increases with positive voltage applied to the pin, and ground potential results in zero output (i.e., 100% modulation). A signal with positive-going sync should be used.

Pin 5 – Chrominance/Sound Input. Input to the RF modulator. This pin accepts an ac coupled chrominance signal. The signal is reduced by an internal resistor divider

before being applied to the RF modulator. The resistor divider consists of a 300 ohm series resistor and a 500 ohm shunt resistor. A 4.5 MHz FM audio signal may be added to the input by selecting an appropriate series input resistor to provide the correct Luminance:Sound ratio.

Pin 6 – V_{CC}. Positive supply voltage.

Pin 7 – RF Modulator Output. Common collector of output modulator stage. Output impedance and stage gain may be selected by choice of resistor connected between this pin and dc supply.

Pin 8 – No Connection.

APPLICATIONS INFORMATION (Refer to Figure 1)

RF Modulator and Oscillator

The coil and capacitor connected between pins 1 and 2 should be selected to have a parallel resonance at the carrier frequency of the desired TV channel. The values of 56 pF and 0.1 μ H shown in Figure 1 were chosen for a Channel 4 carrier frequency of 67.25 MHz. For Channel 3 operation, the resonant frequency should be 61.25 MHz ($C = 75$ pF, $L = 0.1$ μ H). Resistors R2 and R3 are chosen to provide an adequate amplitude of switching voltage, whereas R4 is used to lower the maximum dc level of switching voltage below V_{CC} , thus preventing saturation within the IC.

Composite Luminance and Sync should be dc coupled to Luminance Input, pin 4. This signal must be within the Luma Input Dynamic Range to insure linearity. Since an increase in dc voltage applied to pin 4 results in an increase in RF output, the input signal should have positive-going sync to generate an NTSC compatible signal. As long as the input signal is positive, overmodulation is prevented by the integrated circuit.

Chrominance information should be ac coupled to Chrominance Input, pin 5. This pin is internally connected to a resistor divider consisting of a series 300 ohms and a shunt 500 ohms resistor. The input impedance is thus 800 ohms, and a coupling capacitor should be appropriately chosen.

MC1374

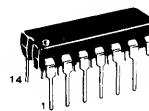
TV MODULATOR CIRCUIT

The MC1374 includes an FM audio modulator, sound carrier oscillator, RF oscillator, and RF dual input modulator. It is designed to generate a TV signal from audio and video inputs. The MC1374's wide dynamic range and low distortion audio make it particularly well suited for applications such as video tape recorders, video disc players, T.V. games and subscription decoders.

- Single Supply, 5 V to 12 V
- Channel 3 or 4 Operation
- Variable Gain RF Modulator
- Wide Dynamic Range
- Low Intermodulation Distortion
- Positive or Negative Sync
- Low Audio Distortion
- Few External Components

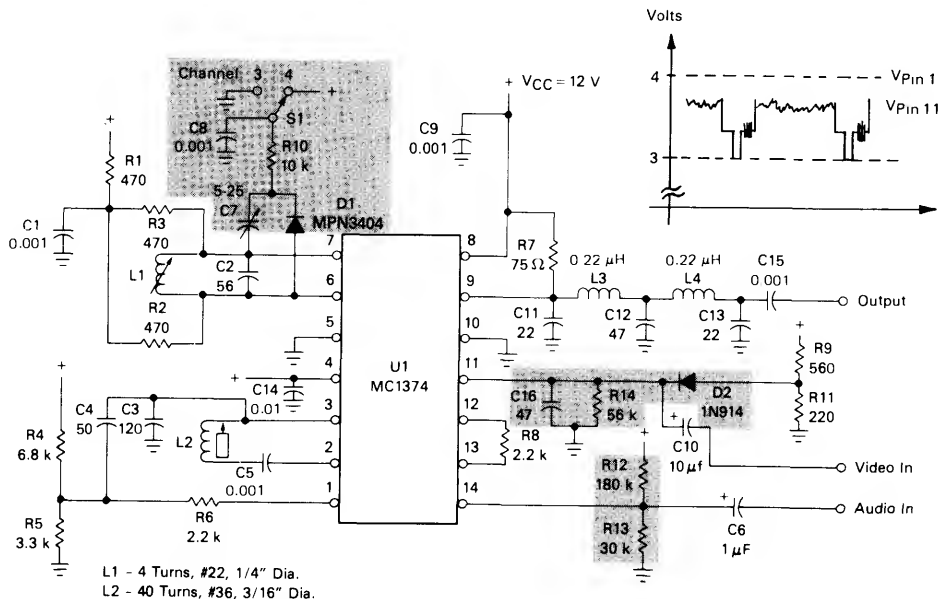
TV MODULATOR CIRCUIT

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**



P SUFFIX
PLASTIC PACKAGE
CASE 646

FIGURE 1 — TYPICAL APPLICATION



L1 - 4 Turns, #22, 1/4" Dia.
L2 - 40 Turns, #36, 3/16" Dia.

Shaded Parts Optional

MC1374

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Value	Unit
Supply Voltage	14	Vdc
Operating Ambient Temperature Range	0 to +70	°C
Storage Temperature Range	-65 to +150	°C
Junction Temperature	150	°C
Power Dissipation, Package Derate above 25°C	1.25 10 mW/°C	Watts

AM OSCILLATOR/MODULATOR

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 Vdc, T_A = 25°C, f_c = 67.25 MHz, Figure 4 circuit, unless otherwise noted)

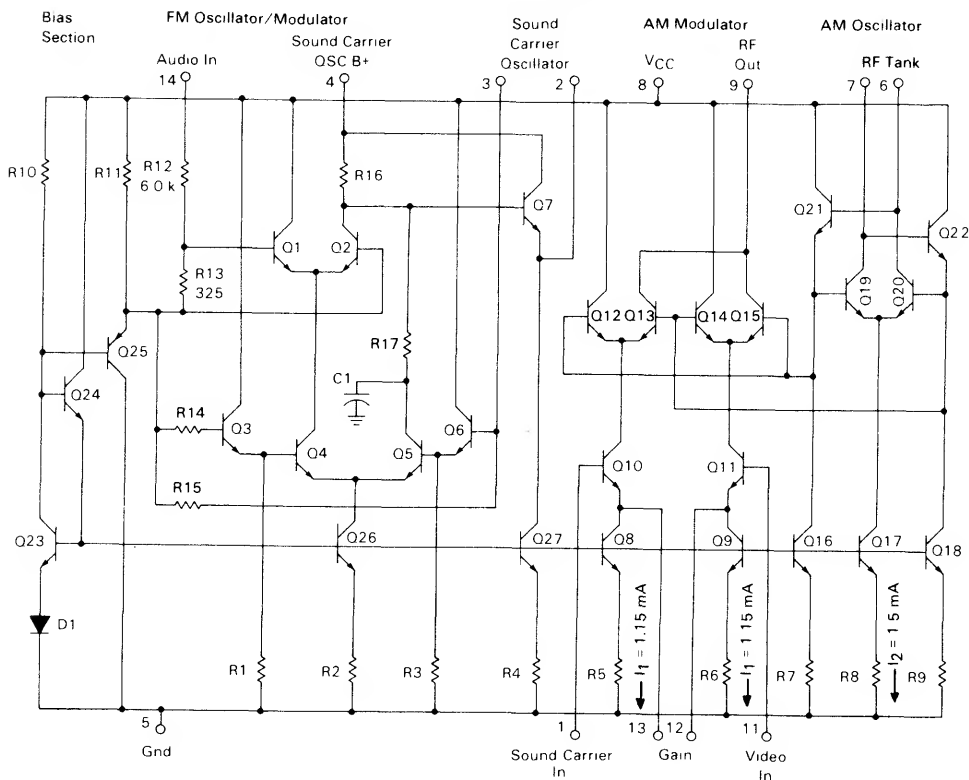
Characteristic	Min	Typ	Max	Unit
Operating Supply Voltage	5.0	12	12	V
Supply Current (Figure 1)	—	13	—	mA
Video Input Dynamic Range (Sync Amplitude)	0.25	1.0	1.0	V Pk
RF Output (Pin 9, R7 = 75 Ω, No External Load)	—	170	—	mV pp
Carrier Suppression	36	40	—	dB
Linearity (75% to 12.5% Carrier, 15 kHz to 3.58 MHz)	—	—	2.0	%
Differential Gain Distortion (IRE Test Signal)	5.0	7.0	10	%
Differential Phase Distortion (3.58 MHz IRE Test Signal)	—	1.5	2.0	Degrees
920 kHz Beat (3.58 MHz @ 30%, 4.5 MHz @ 25%)	—	-57	—	dB
Video Bandwidth (75 Ω Input Source)	30	—	—	MHz
Oscillator Frequency Range	—	105	—	MHz
Internal Resistance across Tank (Pin 6 to Pin 7)	—	18	—	kΩ
Internal Capacitance across Tank (Pin 6 to Pin 7)	—	4.0	—	pF

FM OSCILLATOR/MODULATOR

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 12 Vdc, 4.5 MHz, Test circuit of Figure 11, unless otherwise noted)

Characteristic	Min	Typ	Max	Unit
Frequency Range of Modulator	1.4	4.5	14	MHz
Frequency Shift versus Temperature (Pin 14 open)	—	0.2	0.3	kHz/°C
Frequency Shift versus V _{CC} (Pin 14 open)	—	—	4.0	kHz/V
Output Amplitude (Pin 3 not loaded)	—	900	—	mVp-p
Output Harmonics, Unmodulated	—	—	-40	dB
Modulation Sensitivity 1.7 MHz	—	0.20	—	MHz/V
4.5 MHz	—	0.24	—	MHz/V
10.7 MHz	—	0.80	—	MHz/V
Audio Distortion (±25 kHz Deviation, Optimized Bias Pin 14)	—	0.6	1.0	%
Audio Distortion (±25 kHz Deviation, Pin 14 self biased)	—	1.4	—	
Incidental AM (±25 kHz FM)	—	2.0	—	
Audio Input Resistance (Pin 14 to ground)	—	6.0	—	kΩ
Audio Input Capacitance (Pin 14 to ground)	—	5.0	—	pF
Stray Tuning Capacitance (Pin 3 to ground)	—	5.0	—	pF
Effective Oscillator Source Impedance (Pin 3 to load)	—	2.0	—	kΩ

FIGURE 2 — TV MODULATOR



GENERAL DESCRIPTION

The MC1374 contains an RF oscillator, RF modulator, and a phase-shift type FM modulator, arranged to permit good printed circuit layout of a complete T.V. modulation system. The RF oscillator is similar to the one used in MC1373, and is coupled internally in the same way. Its frequency is controlled by an external tank on Pins 6 and 7, or by a crystal circuit, and will operate to approximately 105 MHz. The video modulator is a balanced type as used in the well known MC1496. Modulated sound carrier and composite video information can be put in separately on pins 1 and 11 to minimize unwanted crosstalk. A single resistor on Pins 12 and 13 is selected to set the modulator gain. The RF output at Pin 9 is a current source which drives a load connected from Pin 9 to V_{CC} .

The FM system was designed specifically for the T.V. intercarrier function. For circuit economy, one phase shift circuit was built into the chip. Still, it will operate from 1.4 MHz to 14 MHz, low enough to be used in a

cordless telephone base station (1.76 MHz), and high enough to be used as an FM IF test signal source (10.7 MHz). At 4.5 MHz, a deviation of ± 25 kHz can be achieved with 0.6% distortion (typical).

In the circuit above devices Q1 through Q7 are active in the oscillator function. Differential amplifier Q3, Q4, Q5, and Q6 acts as a gain stage, sinking current from input section Q1, Q2 and the phase shift network R17, C1. Input amplifier Q1, Q2 can vary the amount of "in phase" Q4 current to be combined with phase shifter current in load resistor R16. The R16 voltage is applied to emitter follower Q7 which drives an external L-C circuit. Feedback from the center of the L-C circuit back to the base of Q6 closes the loop. As audio input is applied which would off-set the stable oscillatory phase, the frequency changes to counteract. The input to Pin 14 can include a dc feedback current for AFC over a limited range.

The modulated FM signal from Pin 3 is coupled to Pin 1 of the RF modulator and is then modulated onto the AM carrier.

THE AM SECTION

The AM modulator transfer function in Figure 3 shows that the video input can be of either polarity (and can be applied at either input). When the voltages on Pin 1 and Pin 11 are equal, the RF output is theoretically zero. As the difference between $V_{Pin\ 11}$ and $V_{Pin\ 1}$ increases, the RF output increases linearly until all of the current from both I_1 current sources (Q8 and Q9) is flowing in one side of the modulator. This occurs when $\pm(V_{Pin\ 11} - V_{Pin\ 1}) = I_1 R_G$, where I_1 is typically 1.15 mA. The peak-to-peak RF output is then $2I_1 R_L$. Usually the value of R_L is chosen to be 75Ω to ease the design of the output filter and match into T.V. distribution systems. The theoretical range of input voltage and R_G is quite wide, but noise and available sound level limit the useful video (sync tip) amplitude to between 0.25 and 1.0 Vpk. It is recommended that the value of R_G be chosen so that only about half of the dynamic range will be used at sync tip level.

The operating window of Figure 5 shows a cross-hatched area where Pin 1 and Pin 11 voltages must always be in order to avoid saturation in any part of the modulator. (The letter ϕ represents one diode drop, or about 0.75 V.) The oscillator Pins 6 and 7 must be biased to a level of $V_{CC} - \phi - 2I_1 R_L$ (or lower) and the input Pins 1 and 11 must always be at least 2ϕ below that. It is permissible to operate down to 1.6 V, saturating the current sources, but whenever possible, the minimum should be 3ϕ above ground.

The oscillator will operate dependably up to about 105 MHz with a broad range of tank circuit components values. It is desirable to use a small L and a large C to minimize the dependence on I.C. internal capacitance. An operating Q between 10 and 20 is recommended. The values of R_1 , R_2 and R_3 are chosen to produce the desired Q and to set the Pin 6 and 7 d.c. voltage as discussed above. Unbalanced operation; i.e., Pin 6 or 7 bypassed to ground, is not recommended. Although the oscillator will still run, and the modulator will produce a useable signal, this mode causes substantial base-band video feedthrough. Bandswitching, as Figure 1 shows, can still be accomplished economically without using the unbalanced method.

The oscillator frequency with respect to temperature in the test circuit shows less than ± 20 kHz total shift from 0°C to 50°C as shown in Figure 7. At higher temperatures the slope approaches $2.0\text{ kHz}/^\circ\text{C}$. Improvement in this region would require a temperature compensating tuning capacitor of the N75 family.

Crystal control is feasible using the circuit shown in Figure 21. The crystal is a 3rd overtone series type, used in series resonance. The L_1 , C_2 resonance is adjusted well below the crystal frequency and is sufficiently tolerant to permit fixed values. A frequency shift versus temperature of less than $1.0\text{ Hz}/^\circ\text{C}$ can be expected from this approach. The resistors R_a and R_b are to suppress parasitic resonances.

Coupling of output RF to wiring and components on Pins 1 and 11 can cause as much as 300 kHz shift in carrier (at 67 MHz) over the video input range. A careful layout can keep this shift below 10 kHz. Oscillator may also be inadvertently coupled to the RF output, with the undesired effect of preventing a good null when $V_{11} = V_1$. Reasonable care will yield carrier rejection ratios of 36 to 40 dB below sync tip level carrier.

In television, one of the most serious concerns is the prevention of the intermodulation of color (3.58 MHz) and sound (4.5 MHz) frequencies, which causes a 920 kHz signal to appear in the spectrum. Very little (3rd order) non-linearity is needed to cause this problem. The results in Figure 6 are unsatisfactory, and demonstrate that too much of the available dynamic range of the MC1374 has been used. Figures 8 and 10 show that by either reducing standard signal level, or reducing gain, acceptable results may be obtained.

At VHF frequencies, small imbalances within the device introduce substantial amounts of 2nd harmonic in the RF output. At 67 MHz, the 2nd harmonic is only 6 to 8 dB below the maximum fundamental. For this reason a double pi low pass filter is shown in the test circuit of Figure 3 and works well for channel 3 and 4 lab work. For a fully commercial application, a vestigial sideband filter will be required. The general form and approximate values are shown in Figure 19. It must be exactly aligned to the particular channel.

FIGURE 3 — AM MODULATOR TRANSFER FUNCTION

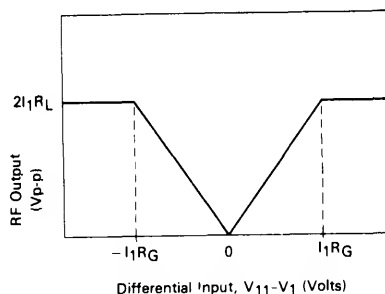


FIGURE 4 — AM TEST CIRCUIT

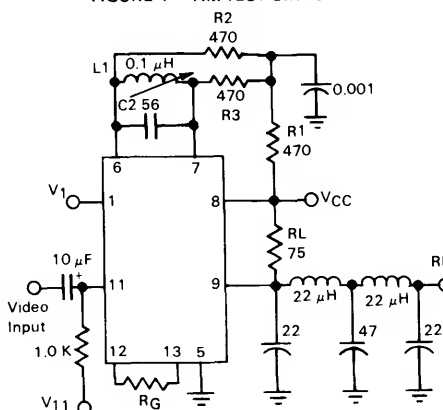


FIGURE 5 — THE OPERATING WINDOW

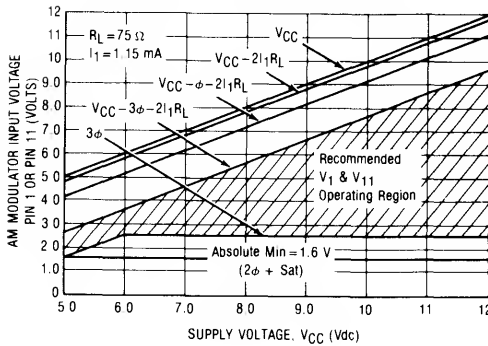


FIGURE 6 — 920 kHz BEAT

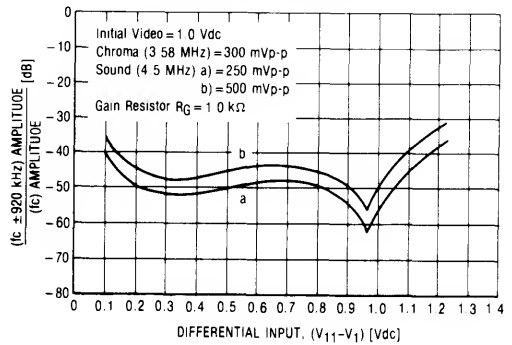


FIGURE 7 — RF OSCILLATOR FREQUENCY versus TEMPERATURE

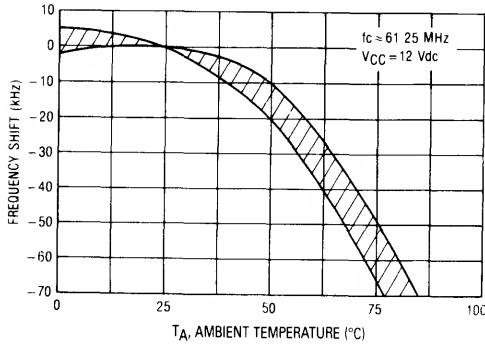


FIGURE 8 — 920 kHz BEAT

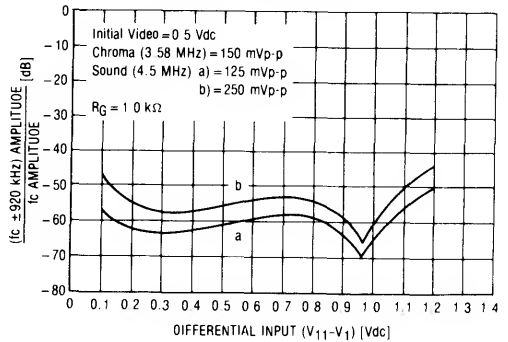


FIGURE 9 — RF OSCILLATOR FREQUENCY versus SUPPLY VOLTAGE

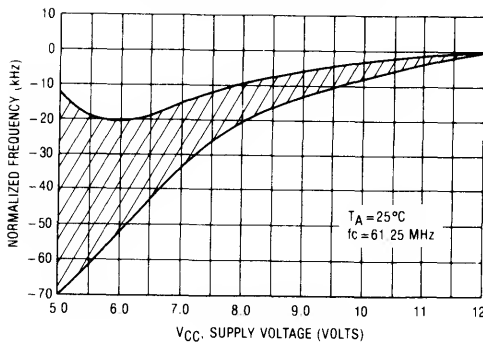
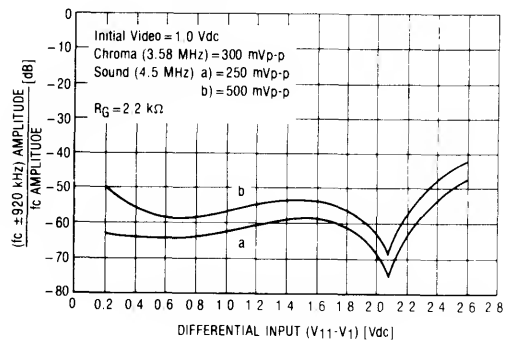


FIGURE 10 — 920 kHz BEAT



FM SECTION

The oscillator center frequency is approximately the resonance of the inductor L_2 from Pin 2 to Pin 3 and the effective capacitance C_3 from Pin 3 to ground. For overall oscillator stability, it is best to keep X_L in the range of 300 Ω to 1.0 k Ω .

The modulator transfer characteristic at 4.5 MHz is shown in Figure 15. Transfer curves at other frequencies have a very similar shape, but differ in deviation per input volt, as shown in Figures 13 and 17.

Most applications will not require dc connection to the audio input, Pin 14. However, some improvements can be achieved by the addition of biasing circuitry. The unaided device will establish its own Pin 14 bias at 4 θ , or about 3.0 V. This bias is a little too high for optimum modulation linearity. Figure 14 shows better than 2-to-1 improvement in distortion between the unaided device and pulling Pin 14 down to 2.6 to 2.7 V. This can be accomplished by a simple divider, if the supply voltage is relatively constant.

The impedance of the divider has a bearing on the frequency versus temperature stability of the FM system. A divider of 180 k Ω and 30 k Ω (for $V_{CC} = 12$ V) will give good temperature stabilization results. However, as Figure 18 shows, a divider is not a good method if the supply voltage varies. The designer must make the decisions here, based on considerations of economy, distortion and temperature requirements and power supply capability. If the distortion requirements are not stringent, then no bias components are needed. If, in this case, the temperature compensation needs to be improved in the high ambient area, the tuning capacitor from Pin 3 to ground can be selected from N75 or N150 temperature compensation types.

Another reason for dc input to Pin 14 is the possibility of automatic frequency control. Where high accuracy of intercarrier frequency is required, it may be desirable to feed back the dc output of an AFC or phase detector for nominal carrier frequency control. Only limited control range could be used without adversely affecting the distortion performance, but very little frequency compensation will be needed.

One added convenience in the FM section is the separate Pin "oscillator B+" which permits disabling of the sound system during alignment of the AM section. Usually it can be hard wired to the V_{CC} source without decoupling.

Standard practice in television is to provide pre-emphasis of higher audio frequencies at the transmitter and a matching de-emphasis in the T.V. receiver audio amplifier. The purpose of this is to counteract the fact that less energy is usually present in the higher frequencies, and also that fewer modulation sidebands are within the deviation window. Both factors degrade signal to noise ratio. Pre-emphasis of 75 μ s is standard practice. For cases where it has not been provided, a suitable pre-emphasis network is covered in Figure 20.

It would seem natural to take the FM system output from Pin 2, the emitter follower output, but this output is high in harmonic content. Taking the output from Pin 3 sacrifices somewhat in source impedance but results in a clean output fundamental, with all harmonics more than 40 dB down. This choice removes the need for additional filtering

components. The source impedance of Pin 3 is approximately 2.0 k Ω , and the open circuit amplitude is about 900 mV p-p for the test circuit shown in Figure 11.

The application circuit of Figure 1 shows the recommended approach to coupling the FM output from Pin 3 to the AM modulator input, Pin 1. The input impedance at Pin 1 is very high, so the intercarrier level is determined by the source impedance of Pin 3 driving through C_4 into the videobias circuit impedance of R_4 and R_5 , about 2.2 K. This provides an intercarrier level of 500 mV p-p, which is correct for the 1.0 V peak video level chosen in this design. Resistor R_6 and the input capacitance of Pin 1 provide some decoupling of stray pickup of RF oscillator or AM output which may be coupled to the sound circuitry.

FIGURE 11 — FM TEST CIRCUIT

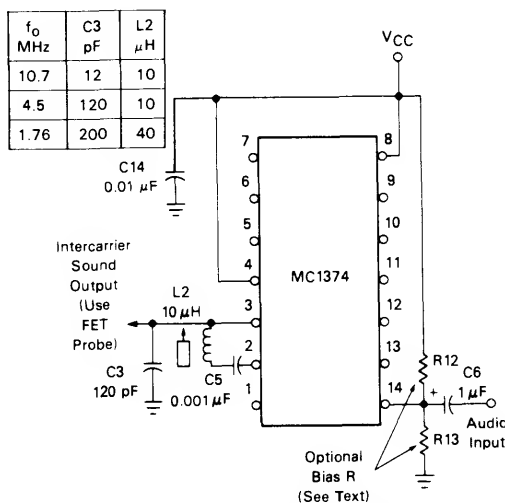


FIGURE 12 — MODULATOR SENSITIVITY

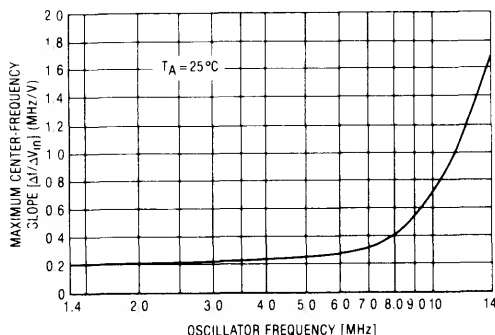


FIGURE 13 — MODULATOR TRANSFER FUNCTION (1.76 MHz)

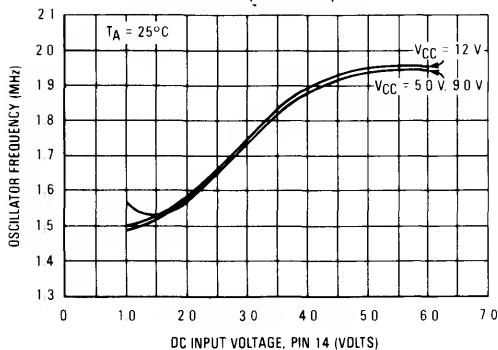


FIGURE 14 — DISTORTION versus MODULATION DEPTH

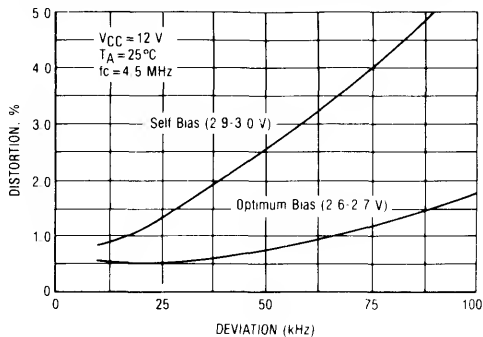


FIGURE 15 — MODULATOR TRANSFER FUNCTION (4.5 MHz)

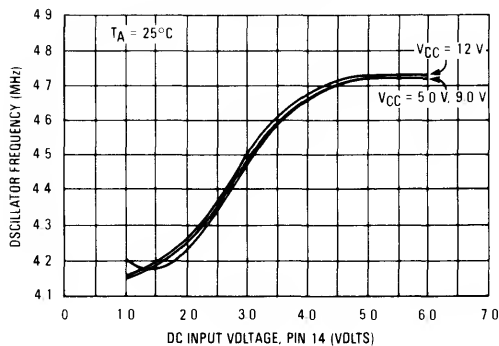


FIGURE 16 — FM SYSTEM FREQUENCY versus TEMPERATURE

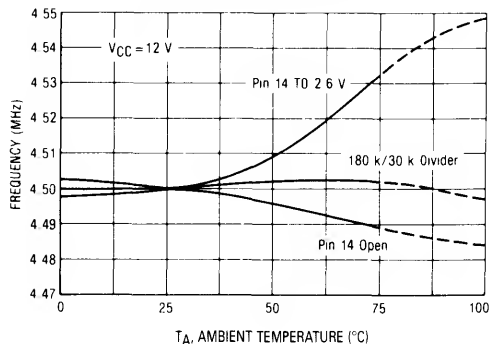


FIGURE 17 — MODULATOR TRANSFER FUNCTION (10.7 MHz)

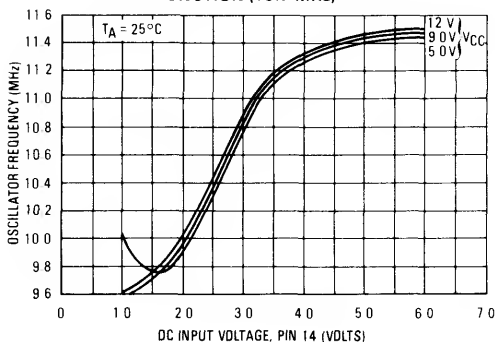
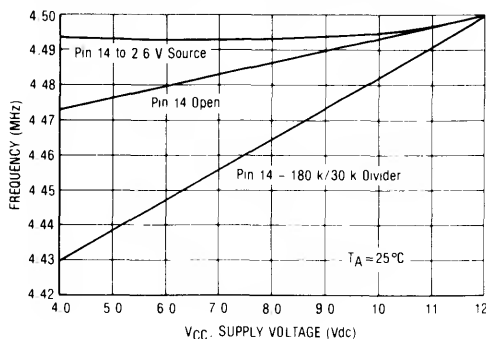
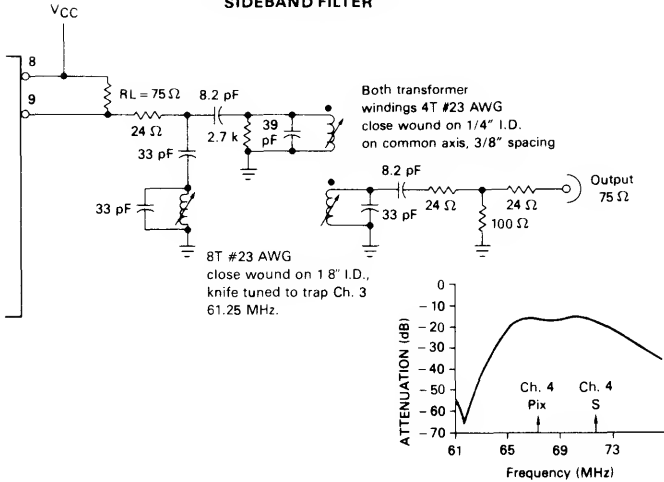


FIGURE 18 — FM SYSTEM FREQUENCY versus VCC



MC1374

**FIGURE 19 — A CHANNEL 4 VESTIGIAL
SIDE BAND FILTER**



**FIGURE 21 — CRYSTAL CONTROLLED RF OSCILLATOR
FOR CHANNEL 3, 61.25 MHz**

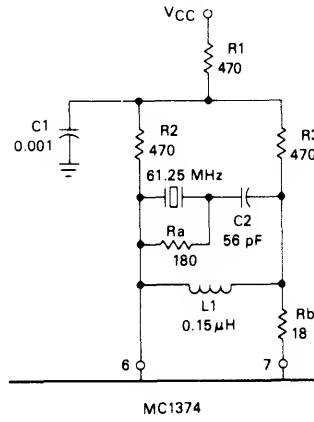
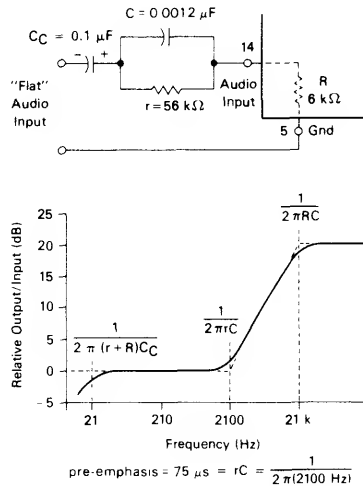


FIGURE 20 — AUDIO PRE-EMPHASIS CIRCUIT



See Application Note AN829 for further information.

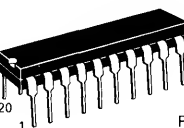
MC1377

Advance Information

COLOR TELEVISION RGB to PAL/NTSC ENCODER

... an integrated circuit used to generate a composite TV signal from baseband red, blue, green and sync inputs. The MC1377 has color subcarrier oscillator, voltage controlled 90° phase shifter, two DSB suppressed carrier chroma modulators, RGB input matrices and blanking level clamps. It can be operated with very few external parts, but has the pinouts for a fully implemented, top quality composite signal. It is ideal for encoding signals from color cameras and graphics generators.

- Reference Oscillator Self-Contained Or Externally Driven
- Nominal 90° ±3.0° Axes Are Optionally Trimmable
- Simple PAL/NTSC Switch
- Luminance And Chroma Channels Can Accept Delay Line/ Bandpass Elements Or Direct Connection
- Provides DC Reference To Permit Direct Drive To RF Modulator



P SUFFIX
 PLASTIC PACKAGE
 CASE 738

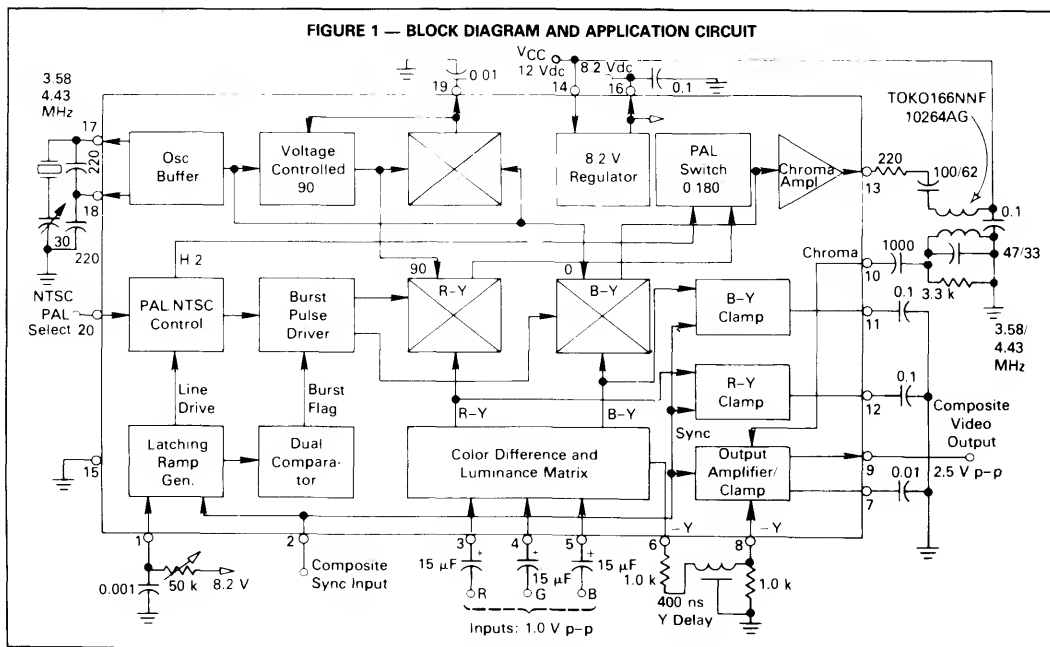
DW SUFFIX
 PLASTIC PACKAGE
 CASE 751D
 (SO-20L)



ORDERING INFORMATION

Device	Temperature Range	Package
MC1377DW	0-70°C	SO-20L
MC1377P		Plastic DIP

FIGURE 1 — BLOCK DIAGRAM AND APPLICATION CIRCUIT



This document contains information on a new product. Specifications and information herein are subject to change without notice.

MC1377

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	15	Vdc
8.2 Vdc Regulator Output Current	I_{REG}	10	mAdc
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	-65 to +150	°C
Junction Temperature	$T_{J(max)}$	150	°C
Power Dissipation, package	P_D	1.25	W
Derate above 25°C		10	mW/°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage	12 ± 1.2	Vdc
Sync Tip Level	-0.5 to +1.0	Vdc
Sync, Blanking Level	+1.7 to +8.2	
Red, Green, Blue Inputs (Saturated)	1.0	V_{p-p}

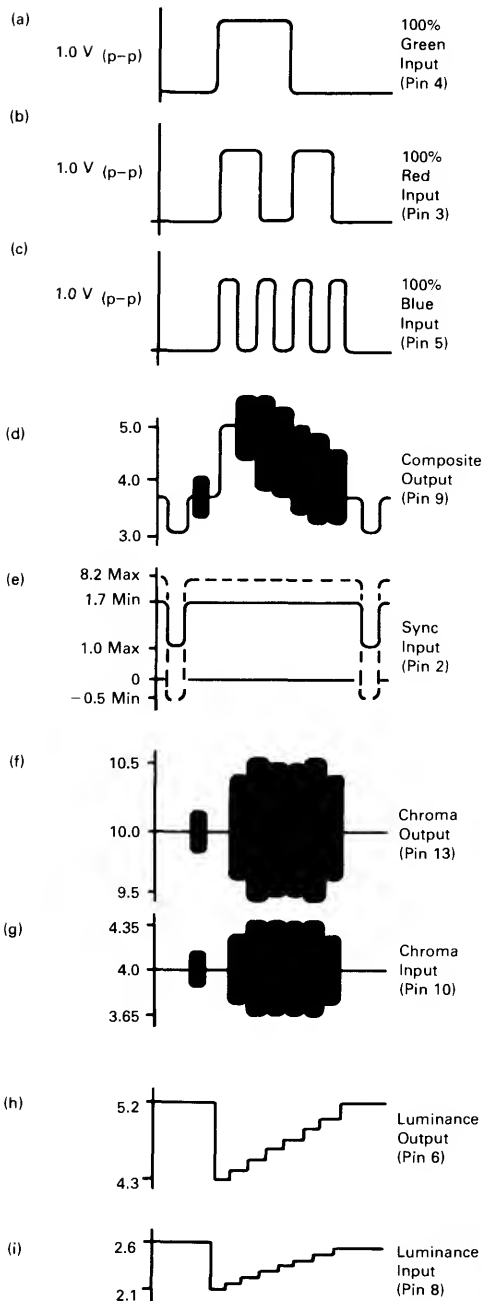
ELECTRICAL CHARACTERISTICS ($V_{CC} = 12$ Vdc, $T_A = 25^\circ\text{C}$, Circuit Of Figure 1 Unless Otherwise Noted.)

Characteristic	Pin No.	Min	Typ	Max	Unit
Supply Current	14	20	32	40	mAdc
Oscillator Amplitude	18	—	0.5	—	$V_{(p-p)}$
External Subcarrier Input (Oscillator Components Removed)	17	—	0.25	—	V_{RMS}
Subcarrier Input: Resistance	17	—	5.0	—	k Ω
Capacitance		—	2.0	—	pF
Modulation Angle (R-Y) to (B-Y)	—	85	90	95	Degrees
(R-Y) Angle Adjustment	19	—	0.25	—	Deg/ μA
R, G, B Input For 100% Color Saturation	3, 4, 5	—	1.0	—	$V_{(p-p)}$
R, G, B Input: Resistance	3, 4, 5	—	10	—	k Ω
Capacitance		—	2.0	—	pF
Sync Threshold (See Figure 2e)	2	—	1.7	—	V
Sync Input Resistance (Input > 1.7 V)	2	—	10	—	k Ω
Chroma Output Level At 100% Saturation	13	—	1.0	—	$V_{(p-p)}$
Chroma Output Resistance	13	—	50	—	Ω
Chroma Input Level For 100% Saturation	10	—	0.7	—	$V_{(p-p)}$
Chroma Input: Resistance	10	—	10	—	k Ω
Capacitance		—	2.0	—	pF
Composite Output, 100% Saturation (See Figure 2d)	9	—	0.6	—	$V_{(p-p)}$
Sync		—	1.4	—	
Luminance		—	1.7	—	
Chroma Burst		—	0.6	—	
Output Impedance (See Note 1)	9	—	50	—	Ω
Luminance Bandwidth (3 dB), Less Delay Line	9	—	8.0	—	MHz
Subcarrier Leakage In Output	9	—	20	—	mV $_{(p-p)}$

Note 1: Output Impedance can be reduced to less than 10 Ω by using a 150 Ω output load from Pin 9 to ground. Power supply current will increase to about 60 mA.

See Application Note AN932 for further information.

FIGURE 2 — SIGNAL VOLTAGES
(CIRCUIT VALUES OF FIGURE 1)



APPLICATION NOTES

R.G.B. Inputs should be set up to be 1.0 V p-p for fully saturated levels. This is not arbitrary, since sync and burst levels are internally fixed. The large (15 μ F) input capacitors of Figure 1 are needed for the 50/60 Hz vertical component.

Subcarrier Oscillator. The internal common-collector Colpitts can be free run or it can easily be pulled in by a lightly coupled signal from a "master" into Pin 17. Also, it can be disabled entirely and a 0.25 V_{RMS} signal driven into Pin 17.

Modulator Phase Angles are quite accurately established internally. Taking (B-Y) as 0°, burst is at 180°, and the angle of (R-Y) is 90° \pm 3.0°. The (R-Y) angle can be "tweaked." For example, 470 k Ω from Pin 19 to ground will increase the (R-Y) to (B-Y) angle about 3.0°. Pulling Pin 19 up will decrease the angle.

Composite Output is dc referenced and can be direct coupled to an RF modulator as shown in Figure 3. In this case, the 8.2 V regulator output of the MC1377 is divided down to 5.8 V to provide the zero carrier reference to Pin 1 of the MC1374.

Burst Generation is provided by a sync triggered ramp on Pin 1 and two internal level sensors. Since the early part of this ramp is used, it is quite accurate. Fixed R-C values are feasible, as shown in Figure 3.

Sync Input can be varied over a wide latitude but nevertheless must be applied correctly. The typical ac coupled sync signal has very little positive value and will require a pull-up resistor to 8.2 Vdc at the input. The sync input is a 10 k Ω /10 k Ω divider in the base of a common emitter stage. For PAL operation, the correctly serrated vertical sync interval must be used, in order to continuously trigger the PAL flip-flop. "Block" vertical sync can be used for NTSC.

(R-Y)(B-Y)(-Y) signals are generated to NTSC values (\pm 5.0%) in the input matrices. They are dc clamped at black level by a sync driven clamp. Burst amplitude is internally fixed to correspond to sync level, allowing for 3.0 dB loss in the chroma bandpass filter. If the filter is not used, as shown in Figure 3, a resistor divider should be inserted between Pin 13 and Pin 10 to provide the proper chroma level. When the chroma bandpass is not used, the (-Y) delay line should also be removed, but the 1.0 k/1.0 k divider from Pin 6 to Pin 8 should be retained.

MC1377

FIGURE 3 — COUPLING THE MC1377 TO THE MC1374 RF MODULATOR

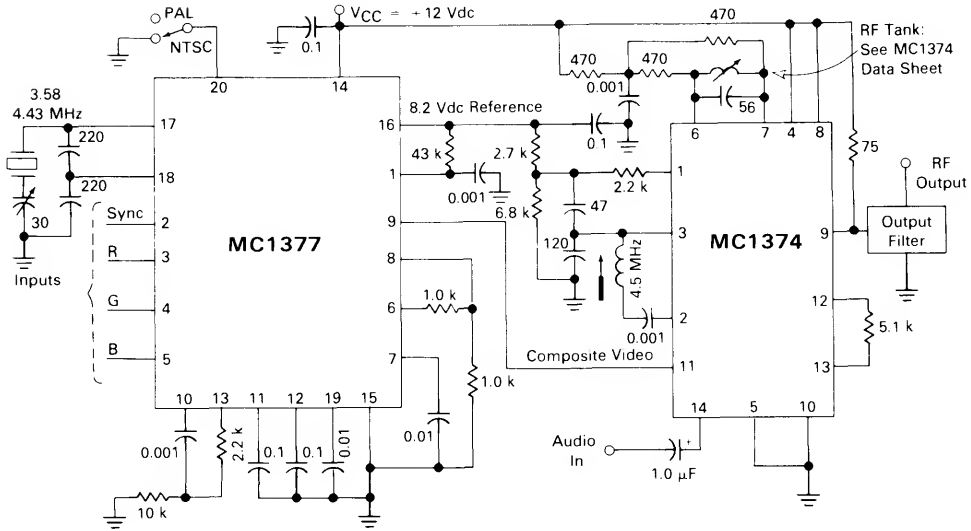


FIGURE 4 — VECTORSCOPE DISPLAY OF 100% SATURATED NTSC COLOR BARS

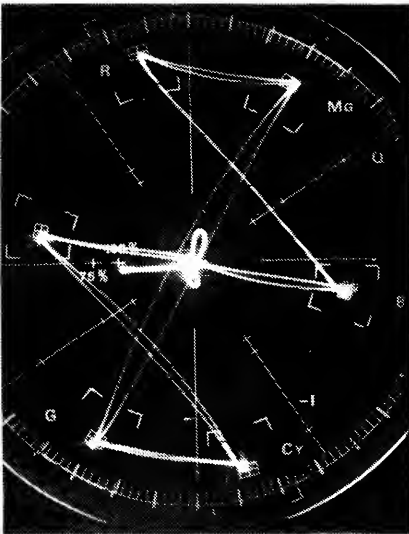
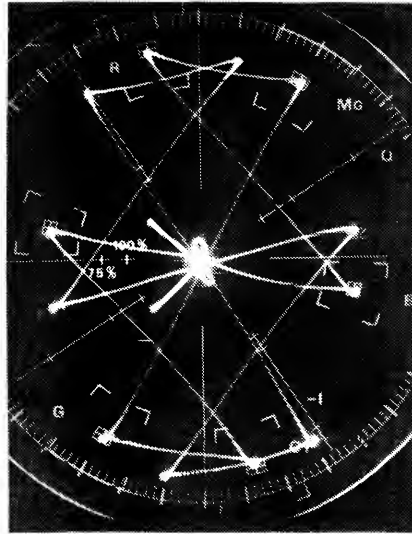


FIGURE 5 — 100% SATURATED PAL COLOR BARS ON NTSC VECTORSCOPE



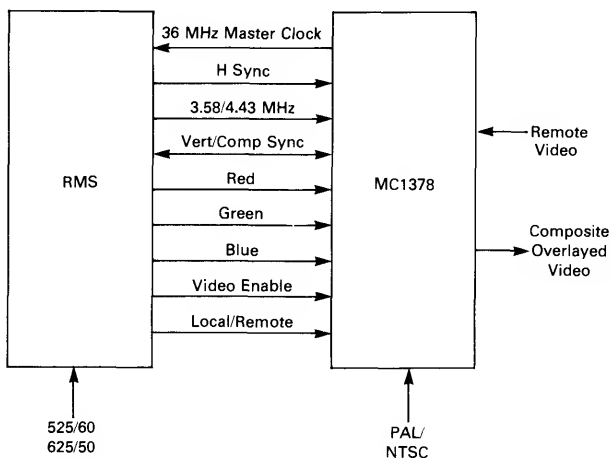
Advance Information

COLOR TELEVISION COMPOSITE VIDEO OVERLAY SYNCHRONIZER

... a bipolar composite video overlay encoder and microcomputer synchronizer. The MC1378 contains the complete encoder function of the MC1377, i.e. quadrature color modulators, RGB matrix, and blanking level clamps, plus a complete complement of synchronizers to lock a microcomputer-based video source to any remote video source. The MC1378 is especially tailored to work with the Motorola RMS (Raster Memory System), but it can be applied to other controllable video sources. It can be used as a local system timing and encoding source, but it is most valuable when used to lock the microcomputer source to a remotely originated video signal.

- Contains All Needed Reference Oscillators
- Can Be Operated in PAL or NTSC Mode, 625 or 525 Line
- Wideband, Full-Fidelity Color Encoding
- Local or Remote Modes of Operation
- Minimal External Components
- Designed to Operate from 5.0 V Supply
- Will Work with Non-standard Video

FIGURE 1 — BLOCK DIAGRAM TYPICAL APPLICATION

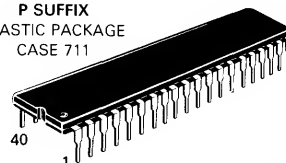


MC1378

COLOR TELEVISION COMPOSITE VIDEO OVERLAY SYNCHRONIZER

SILICON MONOLITHIC INTEGRATED CIRCUIT

P SUFFIX
PLASTIC PACKAGE
CASE 711



FN SUFFIX
PLASTIC PACKAGE
CASE 777
(PLCC-44)



ORDERING INFORMATION

Device	Temperature Range	Package
MC1378P	0–70°C	Plastic DIP
MC1378FN		PLCC-44

PIN ASSIGNMENTS

Local/Rem.	1 (1)	(44) 40	H. Sync In
H. PLL Filter	2 (2)	(43) 39	Comp. Sync Out
H. VCO	3 (3)	(42) 38	V. Out/Sync In
	4 (4)	(41) 37	Clock PLL Filter
Burst Gate Out	5 (5)	(40) 36	Clock VCC
PAL/NTSC Mode	6 (7)	(38) 35	Clock Output
Ground	7 (8)	(37) 34	Clock Ground
3.58/4.43 In	8 (9)	(36) 33	Clock
Chroma PLL Filter	9 (10)	(35) 32	VCO
Chroma VCO	10 (11)	(34) 31	Killer Filter
	11 (12)	(33) 30	Quad. Loop Filter
R-Y Clamp	12 (13)	(32) 29	PAL Ident. Cap
B-Y Clamp	13 (14)	(31) 28	VCC
R Input	14 (15)	(30) 27	Comp. Vid. Out
G Input	15 (16)	(29) 26	Ground
B Input	16 (18)	(27) 25	Overlay Enable
-Y Output	17 (19)	(26) 24	Rem. Vid. In
Chroma Out	18 (20)	(25) 23	ACC Filter
Loc. Vid. Clamp	19 (21)	(24) 22	-Y Input
Chroma In	20 (22)	(23) 21	Rem. Vid. Clamp

* () PLCC Pin Assignments

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MC1378

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V _{CC}	6.0	Vdc
Operating Temperature	T _A	0 to +70	°C
Storage Temperature	T _{stg}	-65 to +150	°C
Junction Temperature	T _{J(max)}	150	°C
Power Dissipation (Package) Derate above 25°C	P _D	1.25 10	W mW/°C

RECOMMENDED OPERATING CONDITIONS

Condition	Pin No.	Value	Unit
Supply Voltage	28, 36	5.0 ± 0.25	Vdc
RGB Input for 100% Saturation	14, 15, 16	1.0	V _{p-p}
Color Oscillator Input Level	8	0.5	V _{p-p}
Video Input, Positive	24	1.0	V _{p-p}

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C Circuit of Figure 4 or 5)

Characteristic	Pin No.	Min	Typ	Max	Unit
Supply Current	28, 36	—	100	—	mAdc
Video Output, Open Circuit, Positive	27	—	2.0	9.4	V _{p-p}
Modulation Angle (R - Y) to (B - Y)	—	87	90	93	Degrees
RGB Input Impedance	14, 15, 16	—	10	—	kΩ
Local/Remote Switch (TTL)	High Low	1	—	Remote Local	—
Horizontal Sync Input, Negative Going (TTL)	40	—	4.3	—	V _{p-p}
Vertical Sync Output, Negative Going, Remote Mode (TTL)	38	—	4.3	—	V _{p-p}
Composite Sync Output, Negative Going (TTL)	39	—	4.3	—	V _{p-p}
Burst Gate Output, Positive Going (TTL)	5	—	4.3	—	V _{p-p}

DESCRIPTION OF OPERATION — Refer to Figures 3, 4

REMOTE MODE	LOCAL MODE
<p>The incoming remote video signal (Pin 24) supplies all synchronizing information. A discussion of the function of the phase detectors helps to clarify the lockup method:</p> <p>PD1 — locks the internally counted-down 4 MHz horizontal VCO to the incoming horizontal sync. It is fast acting, to follow VCR source fluctuations.</p> <p>PD2 — locks the 36 MHz clock VCO, which is divided down by the RMS, to the divided down horizontal VCO.</p> <p>PD3 — is a gated phase detector which locks the 14 MHz crystal oscillator, divided by 4, to the incoming color burst.</p> <p>PD4 — controls an internal phase shifter to assure that the outgoing color burst is the same phase as incoming burst at PD3.</p> <p>PD5 — not used in REMOTE MODE</p> <p>Vertical lock is obtained by continuously resetting the sync generator in the RMS with separated vertical sync from the MC1378, Pin 38. This signal is TTL level vertical block sync, negative going. The horizontal sync from the RMS to Pin 40 is also TTL level with sync negative going. The local/remote switch, Pin 1, is in local mode when grounded, remote mode when taken to 5.0 V. The overlay control, Pin 25, has an analog characteristic, centered about 1.0 V, which allows fading from local to remote.</p>	<p>The MC1378 and RMS combine to provide a fully synchronized standard signal source. In this case, composite sync must be supplied by the RMS or other time base system. In the MC1378 the phase detectors operate as follows:</p> <p>PD1 — locks the internally counted-down 4 MHz horizontal VCO to a Horizontal Sync signal (at Pin 40) from the RMS (counted down from 36 MHz).</p> <p>PD2 — not used in LOCAL MODE.</p> <p>PD3 — not used in LOCAL MODE.</p> <p>PD4 — active, but providing an arbitrary phase shift setting between the color oscillator and the output burst phase.</p> <p>PD5 — locks the 36 MHz clock VCO (which is divided down by the RMS) to the 14 MHz (crystal) color oscillator. The 14 MHz is, therefore, the system standard in LOCAL MODE, and it is not dc controlled.</p> <p>COMPOSITE VIDEO GENERATION</p> <p>The color encoding at the RGB signals is done exactly as in the MC1377. Composite chroma is looped out at Pins 18 and 20 to allow the designer to choose band shaping. Luminance is similarly brought out (Pins 17 and 22) to permit installation of the appropriate delay.</p> <p>Composite sync output, Pin 39, and burst gate output, Pin 5, are provided for convenience only.</p>

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MC1378

FIGURE 3 — REMOTE MODE

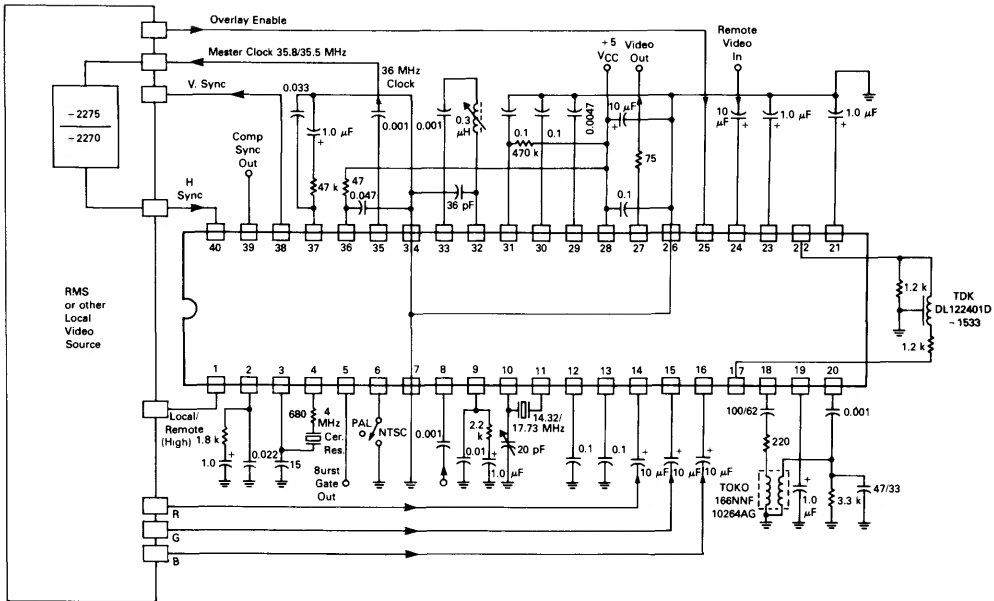
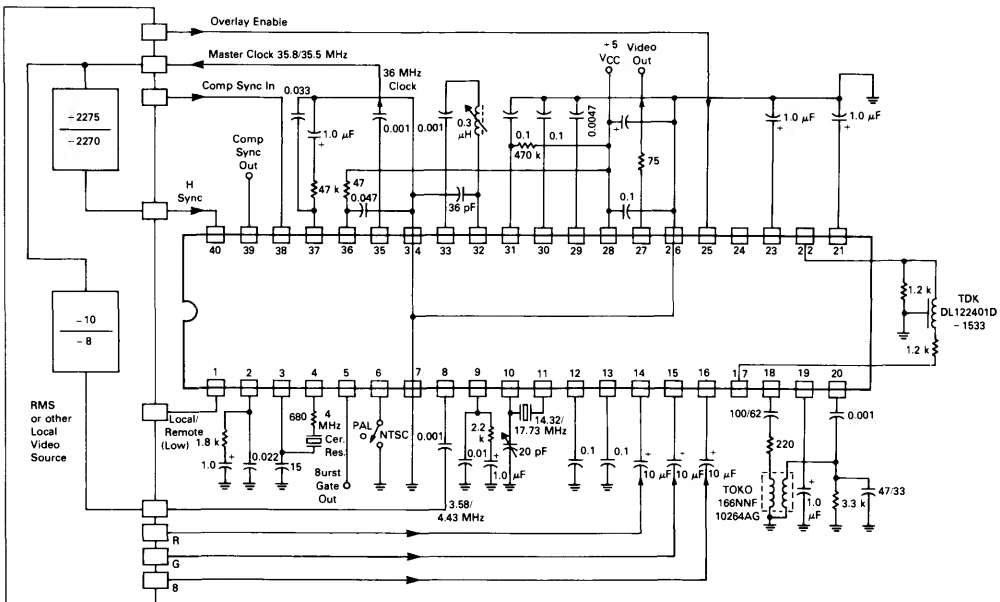


FIGURE 4 — LOCAL MODE



MC1382

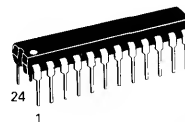
Advance Information

MULTISYNC MONITOR TTL TO ANALOG INPUTS INTERFACE

The MC1382 is a companion chip of the MC1381/3/4 series for multisync monitor applications. It performs the conversion of TTL inputs from either non-IBM PC or standard IBM CGA or EGA color graphic boards to analog R.G.B. outputs for direct interfacing with the MC1381 series. It also performs the necessary signal switching for IBM CGA/EGA color mode selection and 7 text colors selection.

MULTISYNC MONITOR TTL TO ANALOG INPUT INTERFACE

SILICON MONOLITHIC
INTEGRATED CIRCUIT

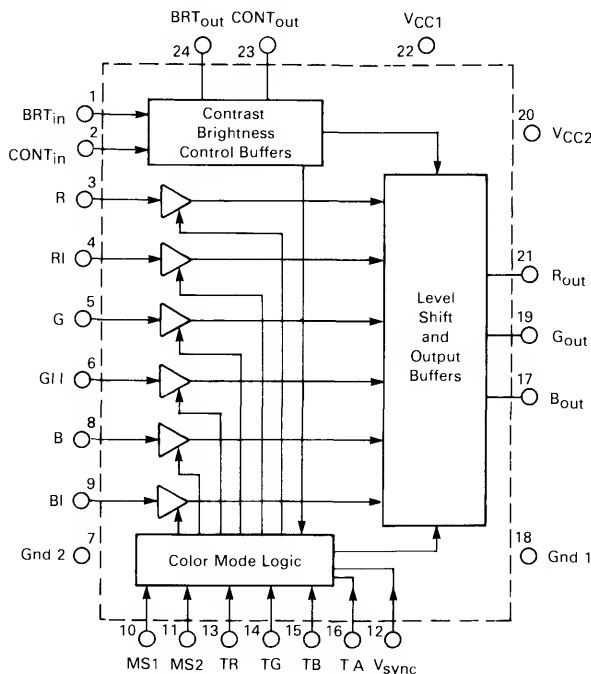


P SUFFIX
 PLASTIC PACKAGE
 CASE 724

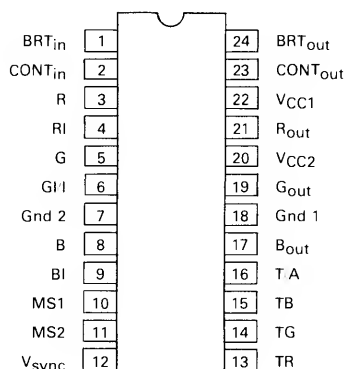


DW SUFFIX
 PLASTIC PACKAGE
 CASE 751E
 (SO-24L)

BLOCK DIAGRAM



PIN ASSIGNMENTS



(Top View)

ORDERING INFORMATION

MC1382DW	SO-24L
MC1382P	Plastic DIP

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MC1382

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC1}, V_{CC2}	6.5	V
Power Dissipation	P_D	550	mW
Input Voltage Range	V_I	$V_{CC} + 0.7$	V
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-60 to +150	°C
Operating Junction Temperature	T_J	+150	°C

NORMAL OPERATION ($V_{CC} = 5.0$ V, Output Loading 75 Ohms)

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC1}, V_{CC2}	4.5	5.0	5.5	V
R, B, G, Gl/I, Bl, Rl Input Voltage	V_{in}	0.7 V_{CC}	—	—	V
		—	—	0.5	
R, B, G, Gl/I, Bl, Rl Input Impedance	R_{in}	—	10	—	k Ω
R, B, G, Gl/I, Bl, Rl Input Capacitance	C_{in}	—	—	4.0	pF
$R_{out}, G_{out}, B_{out}$ Voltage	V_o	1.0	1.2	—	Vp-p
Bandwidth	BW	20	—	—	MHz
MS1, MS2, TR, TG, TB, T.A, V_{sync} Input		3.5	—	—	V
		—	—	0.5	
MS1, MS2, TR, TG, TB, T.A Input Impedance	R_{in2}	—	15	—	k Ω
Brightness Output BRT_{out} IBM-TTL Mode ($T_A = "1"$)	V_{BRT}	—	2.5	—	V
Analog Mode or Non-IBM-TTL Mode ($T_A = "0"$ or MS1/MS2 = "11")		0.3	—	4.7	
Brightness Output BRT_{out}	V_{BRT}	0.3	2.5	4.7	V
Contrast Output $CONT_{out}$	V_{CONT}	0.3	—	4.7	V
Contrast Control Range		—	16	20	dB
Quiescent Current (All R, B, G, Gl/I, Bl, Rl Inputs at low and put on EGA mode)	I_{CC1} I_{CC2}	— —	40 30	— —	mA
$BRT_{in}, CONT_{in}$ Input Control Range		0.2	—	4.0	V

MC1382

PIN FUNCTION DESCRIPTION

Pin No.	Function	Description
1	BRT _{in}	Brightness control input.
2	CONT _{in}	Contrast control input.
3	R	TTL input for primary Red.
4	RI	TTL input for secondary Red.
5	G	TTL input for primary Green.
6	GI/I	TTL input for secondary Green or Intensity.
7	GND2	Ground pin for the TTL inputs.
8	B	TTL input for primary Blue.
9	BI	TTL input for secondary Blue.
10, 11	MS1, MS2	Logic combination of these 2 pins selects the mode of operation, either IBM or (8/64) non-IBM colors.
12	V _{sync}	Connect to MC1381 Sync-Polarity output.
13, 14, 15	TR, TG, TB	Logic combination of these 3 pins determines one of seven colors displayed for the text.
16	T/A	TTL/ANALOG input format select. "1" for TTL and "0" for ANALOG.
17	B _{out}	Analog output for Blue.
18	GND1	Quiet ground for the circuit.
19	G _{out}	Analog output for Green.
20	V _{CC2}	Positive power supply for the analog output circuit. Maximum input is 5.0 volts.
21	R _{out}	Analog output for Red.
22	V _{CC1}	Clean power supply for the chip. 5.0 Volts maximum.
23	CONT _{out}	Contrast control output.
24	BRT _{out}	Brightness control output.

MC1382

FEATURES:

Accepts IBM-TTL (CGA, EGA) and non-IBM 8/64 TTL color inputs of R, B, G, I or R, G, B, RI, BI, GI.

Logic combination of pins MS1, MS2 selects the desired mode of IBM or non-IBM (8/64) operation.

COLOR MODE	MS1	MS2
8	L	L
8	L	H
64	H	L
IBM	H	H

IBM-TTL Mode

The chip automatically adjusts itself to generate 16 color (CGA) or 64 color (EGA) based on the polarity of vertical sync. Only R, B, G, I inputs will be decoded if the vertical sync is positive. On the other hand, R, G, B, RI, GI and BI will be decoded if negative vertical sync is detected. The vertical sync polarity indication is generated from the sync polarity detector in the time base portion of the MC1381, and the input to "V sync" on the MC1382. If the voltage is higher than 3.0 V, it indicates CGA mode. If lower than 3.0 V, this signifies EGA mode.

The colors will follow the IBM standard as shown in the color chart below.

Text Mode Selection

Seven colors can be selected by TR, TG, TB inputs or set by software program from the graphic board. The truth table is as follows:

TEXT COLOR	TR	TG	TB
RED	H	L	L
GREEN	L	H	L
BLUE	L	L	H
YELLOW	H	H	L
CYAN	L	H	H
MAGENTA	H	L	H
WHITE	H	H	H
# NORMAL	L	L	L

Text color is set by a software program from the color graphics board.

Converts TTL inputs to RGB analog outputs with 75 ohm loading capability.

The T/A pin is used to select the input sources of TTL or Analog formats. If T/A goes to the high state, TTL input format is selected, and the TTL to Analog conversion circuit is enabled. It then converts either R, G, B, I or R, G, B, RI, GI, BI TTL inputs into R, G, B Analog outputs of 1.2 V at 75 ohm external loading.

If the T/A pin is pulled low, the TTL to Analog conversion circuit is disabled, and the outputs of the conversion circuit go to high impedance. Analog signals are fed directly to the MC1381, and the brightness and contrast controls will be processed by the MC1381.

TABLE 1 — IBM COLOR CHART

COLOR	CGA				EGA					
	I	R	G	B	RI	GI	BI	R	G	B
Black	0	0	0	0	0	0	0	0	0	0
Blue	0	0	0	1	0	0	0	0	0	1
Green	0	0	1	0	0	0	0	0	1	0
Cyan	0	0	1	1	0	0	0	0	1	1
Red	0	1	0	0	0	0	0	1	0	0
Magenta	0	1	0	1	0	0	0	1	0	1
Brown	0	1	1	0	0	1	0	1	0	0
White	0	1	1	1	0	0	0	1	1	1
Black (CGA)/Dark Gray (EGA)	1	0	0	0	1	1	1	0	0	0
Light Blue	1	0	0	1	1	1	1	0	0	1
Light Green	1	0	1	0	1	1	1	0	1	0
Light Cyan	1	0	1	1	1	1	1	0	1	1
Light Red	1	1	0	0	1	1	1	1	0	0
Light Magenta	1	1	0	1	1	1	1	1	0	1
Yellow	1	1	1	0	1	1	1	1	1	0
Intensified White	1	1	1	1	1	1	1	1	1	1

Contrast and Brightness Controls

In IBM-TTL mode, the contrast control complies with the IBM standard. It controls the gain of nonintensified colors in CGA mode or intensified colors in EGA mode.

The brightness control is not performed in the MC1382 but in the MC1381 companion chip. The TTL brightness input is provided at $CONT_{out}$ for connection to the MC1381 for control of the R, B, G gain.

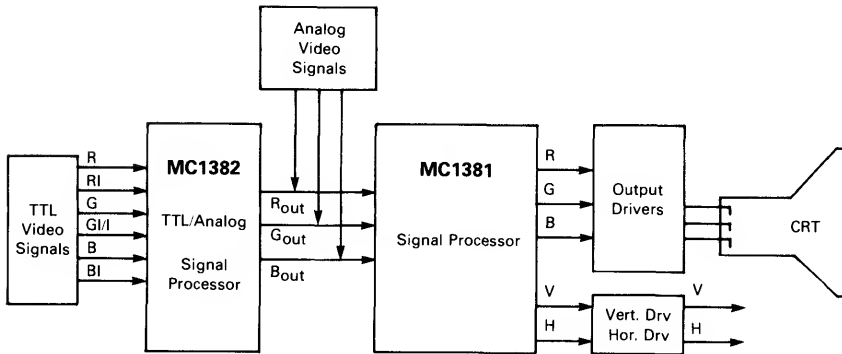
Analog or Non-IBM-TTL Mode

The contrast and brightness controls are performed in the MC1381 companion device. The BRT_{in} and $CONT_{in}$ directly output to BRT_{out} and $CONT_{out}$ respectively without any signal processing within MC1382.

TABLE 2 — CONTROL MODES — PIN ROUTING FOR IBM AND NON-IBM MODES

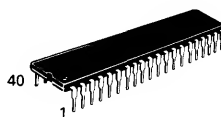
IBM TTL Mode T/A = "1"	Analog Mode or non-IBM-TTL Mode T/A = "0" or MS1/MS2 \neq "11"
$CONT_{in} \rightarrow$ Internal Contrast Control Circuit	$CONT_{in} \rightarrow CONT_{out}$
$BRT_{in} \rightarrow CONT_{out}$	$BRT_{in} \rightarrow BRT_{out}$
$BRT_{out} \rightarrow 2.5$ Volts	

FIGURE 1 — SIMPLIFIED "MULTISCAN" MONITOR SYSTEM



MULTIMODE MONITOR PROCESSOR

- Automatic horizontal frequency tracking of all commonly used personal computer and broadcast standards, infinitely variable from 15.5 to 40 kHz.
- The positive vertical output pulse is automatically polarity corrected.
- The 50 MHz video system includes contrast and brightness controls with automatic beam limiter. The video drivers can be used as the lower device in a cascode output stage.



P SUFFIX
PLASTIC PACKAGE
CASE 711

MOTOROLA LINEAR/INTERFACE DEVICES

MC1383

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V _{CC}	10	V
Operating Temperature Range	T _A	-10 to +60	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C
Junction Temperature	T _J	+150	°C

NORMAL OPERATION (T_A = 25°C, V_{CC} = 8.0 V, using application circuit)

Characteristic	Condition	Min	Typ	Max	Unit
Supply Voltage Pins 31, 40		7.6	8.0	8.4	Volts
Supply Current Pins 31, 40	Excluding current at Pins 23, 26, 29	—	40	—	mA
Internal Regulator Pin 5		0.57	0.625	0.68	XV _{CC}
Horizontal Frequency Range		15.5	—	40	kHz
Short Term Horizontal Pull-In Range	Time = < 5.0 ms	—	± 5.0	—	%FH
Long Term Horizontal Pull-In Range	Time = > 500 ms	15.5	—	40	kHz
Horizontal Picture Position Adjustment Range	V ₃₆ = 0–8.0 V	-20	—	+20	%TH
Horizontal Output Duty Cycle Adjustment	V ₃₅ = 0–8.0 V	2:1	—	1:2	
X-Ray Horizontal Shutdown Threshold		0.4	0.6	0.9	V
Vertical and Horizontal TTL Input Threshold		1.5	2.0	2.5	V
Comp. Video Sync. Sep. Input Level	Blanking to sync tip	0.1	—	2.0	V
Comp. Video Sync. Sep. Drive Impedance		—	—	1.0 k	Ohms
Horizontal Oscillator Free Run Temperature Drift	Pin 7 open circuit	—	—	300	ppm/°C
Source Current for 15.5 kHz FH	I _{source} Pin 8	—	120	—	μA
Source Current for 40 kHz FH	I _{source} Pin 8	—	320	—	μA
Horizontal Drive Output Current	V ₃₄ low	—	—	40	mA
Horizontal Drive Output Voltage	I ₃₄ = 40 mA	—	—	0.3	V
Source Current for Pins 11, 13		—	0.5	—	XIPin8
Voltage Threshold at Pins 11, 13		—	0.625	—	XV _{CC}
Hysteresis Voltage of Threshold Pins 11, 13		—	120	—	mV
Voltage Pins 10, 12	I _{pins 10, 12} < 10 μA	—	—	12	V
Pins 10, 12	I _{pins 10, 12} = 10 mA	—	—	0.3	
Vertical Output Pulse Amplitude Pin 39		—	4.0	—	V
Video Source Impedance Pins 15, 16, 17		—	—	100	Ohms
Video Input Level Pins 15, 16, 17		0.5	0.7	1.2	Vp-p
Video Output Current Pins 23, 26, 29	Peak white with nominal black level	—	—	60	mA
Video Bandwidth -3.0 dB Pins 15–28, 16–25, 17–22	AV = 4.5	50	—	—	MHz
Brightness Control Range	V ₁₉ = 0–5.0 V (Measured at Pins 22, 25, 28)	—	± 0.5	—	V

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Characteristic	Condition	Min	Typ	Max	Unit
Contrast Control Range	V ₁₈ = 0–5.0 V	—	26	—	dB
Nominal Video Voltage Gain Pins 15–28, 16–25, 17–22	V ₁₈ = 5.0 V	—	4.5	—	
Video Clamp Reference Voltage Pin 30		—	2.5	—	V
Video Output Clamp Voltage	V ₁₉ = 2.5 V	—	2.5	—	V

9



SIMPLIFIED BLOCK DIAGRAM DESCRIPTION

5.0 Volt Regulator — The regulator reference is derived from the V_{CC} . This is buffered and used as an internal voltage source for many functions within the device.

Sync Input Control — In this block the polarity of the TTL sync inputs is monitored and corrected automatically. In the absence of horizontal or composite TTL sync the default input becomes the composite sync separator. The integrator that forms part of the vertical polarity correction has an external capacitor, the voltage at which can be used to determine the polarity of the vertical TTL sync and therefore the mode of certain PC graphics standards. The MC1382 uses this pin for mode control.

V_{sync} Buffer — This stage is used to drive an external vertical timebase with a positive V_{sync} pulse.

32H Oscillator — A current controlled oscillator running at 32 times horizontal rate is locked to the external horizontal sync using a PLL.

Divide by 32 and Clamp Pulse Decoder — The 32H oscillator frequency is divided down to H frequency and a pulse decoded for back porch clamping of the video.

Dual Current Source, I_{fix} I_{var} — The fixed and variable current sources control the 32H oscillator as part of the phase-locked loop. The variable source is used elsewhere in the device for various horizontal frequency dependent functions.

Primary Phase Detector and Unity Gain Buffer — The H_{sync} and H signals are phase compared and used to drive a unity gain buffer the output of which is used to control I_{var} , thus completing the PLL.

Horizontal Lock Control — This block provides frequency agility to the horizontal PLL.

FH Switches — Two comparators compare the internal 5.0 V reference with the voltage developed across external resistors by one-half of I_{var} provide programmable frequency dependent TMOS driver levels for horizontal output stage control.

H_{ramp1} and Comparator 1 — The picture position is controlled by slicing the output of H_{ramp1} .

H_{ramp2} , Comparator 2 and Comparator 3 — These blocks control the duty cycle and position of the horizontal drive pulse.

Secondary Phase Detector — Horizontal flyback is compared with Comparator 2 output to provide automatic compensation for horizontal output stage turn-off delay.

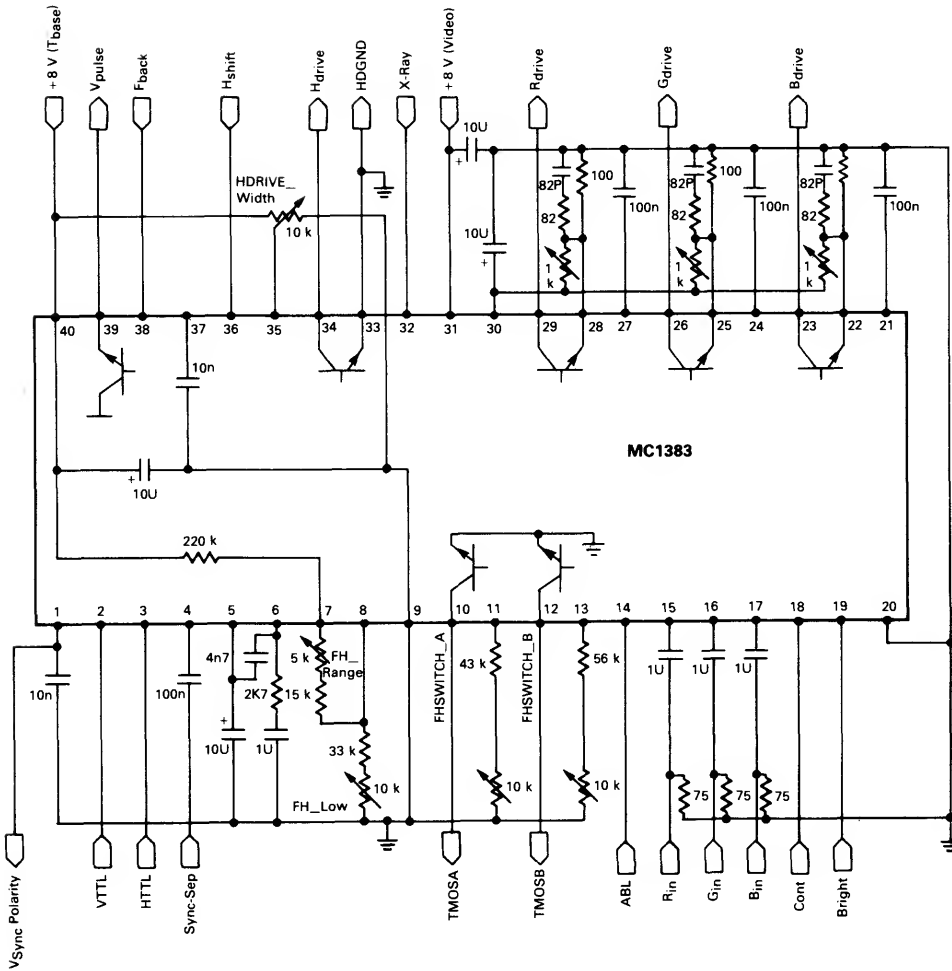
X-Ray Latch and Horizontal Drive — If the threshold of the latch is exceeded the horizontal drive is permanently on until the V_{CC} is removed.

Brightness and Contrast Processor — The dc video controls are distributed to the video stages and a clamp reference voltage is developed for the output stages.

Video Input and Video Drivers — The video signals are processed clamped and amplified to provide either an emitter follower or lower stage of a cascode amplifier to drive the high voltage output stage.

MC1383

APPLICATION CIRCUIT DIAGRAM



MC1384

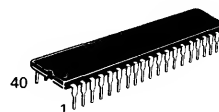
Advance Information

**MULTIMODE MONITOR
HORIZONTAL, VERTICAL, AND VIDEO
COMBINATION PROCESSOR
WITH VERTICAL TIMEBASE**

The MC1384 includes all the signal processing functions for a resistor programmable fixed frequency and multiple sync source RGB monitor and includes the following functions:

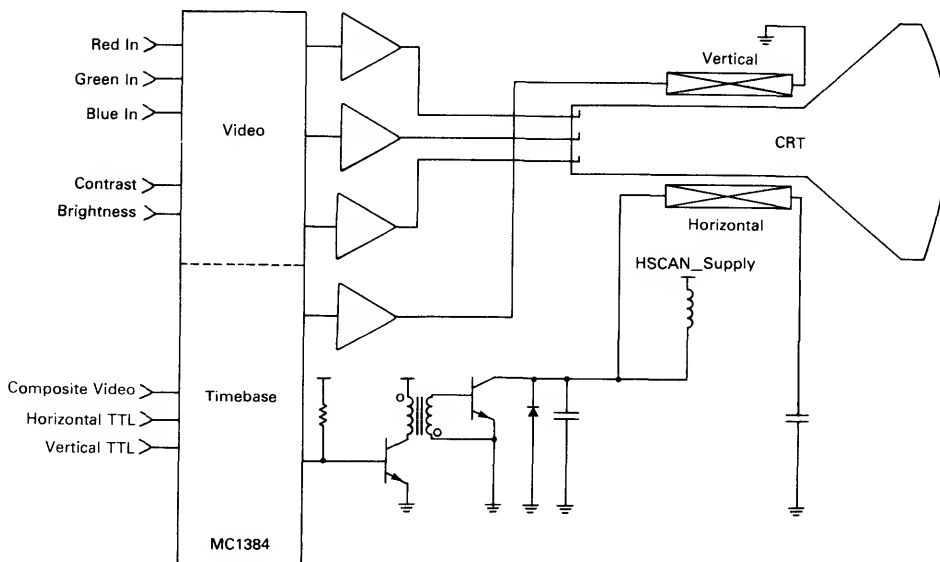
- Automatic horizontal frequency tracking of all commonly used personal computer and broadcast standards, resistor programmable from 15.5 to 40 kHz.
- The vertical timebase operates from 45 to 80 Hz.
- The 50 MHz video system includes contrast and brightness controls with automatic beam limiter. The video drivers can be used as the lower device in a cascode output stage.

**MULTIMODE MONITOR
PROCESSOR
WITH VERTICAL TIMEBASE**



P SUFFIX
PLASTIC PACKAGE
CASE 711

APPLICATION BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

MC1384

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	10	V
Operating Temperature Range	T_A	-10 to +60	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Junction Temperature	T_J	+150	°C

NORMAL OPERATION ($T_A = 25^\circ\text{C}$, $V_{CC} = 8.0\text{ V}$, using application circuit)

Characteristic	Condition	Min	Typ	Max	Unit
Supply Voltage Pins 31, 20		7.6	8.0	8.4	Volts
Supply Current Pins 31, 20	Excluding current at Pins 12, 15, 18	—	40	—	mA
Internal Regulator Pin 38		0.57	0.625	0.68	XV_{CC}
Horizontal Frequency Range	(With components shown, $F_H = 31.5\text{ kHz}$)	15.5	—	40	kHz
Horizontal Pull-In Range		—	± 5.0	—	%FH
Horizontal Picture Position Adjustment Range	$V_{25} = 0-8.0\text{ V}$	-20	—	+20	%TH
Horizontal Output Duty Cycle Adjustment	$V_{24} = 0-8.0\text{ V}$	2:1	—	1:2	
X-Ray Horizontal Shutdown Threshold		0.4	0.6	0.9	V
Vertical and Horizontal TTL Input Threshold		1.5	2.0	2.5	V
Comp. Video Sync. Sep. Input Level	Blanking to sync tip	0.1	—	2.0	V
Comp. Video Sync. Sep. Drive Impedance		—	—	1.0 k	Ohms
Horizontal Oscillator Free Run Temperature Drift	Pin 2 open circuit	—	—	300	ppm/°C
Source Current for 15.5 kHz FH	I_{source} Pin 1	—	120	—	μA
Source Current for 40 kHz FH	I_{source} Pin 1	—	320	—	μA
Horizontal Drive Output Current	V_{23} low	—	—	40	mA
Horizontal Drive Output Voltage	$I_{23} = 40\text{ mA}$	—	—	0.3	V
Vertical Synchronization Range	$FV_{\text{nom}} = 60\text{ Hz}$	—	12	—	Hz
Vertical Ramp Amplitude		—	—	3.0	V_{p-p}
Vertical Ramp Output Current		—	—	2.0	mA_{p-p}
Vertical Ramp Nonlinearity		—	—	1.0	%
Vertical Ramp Frequency Range		45	—	80	Hz
Vertical Free Run Temperature Drift	$FV = 60\text{ Hz}$	—	0.01	—	$\text{Hz}/^\circ\text{C}$
Vertical Free Run Drift with V_{CC}	$FV = 60\text{ Hz}$	—	0.5	—	Hz/V
Video Source Impedance Pins 4, 5, 6		—	—	100	Ohms
Video Input Level Pins 4, 5, 6		0.5	0.7	1.2	V_{p-p}
Video Output Current Pins 12, 15, 18	Peak white with nominal black level	—	—	60	mA

9

Characteristic	Condition	Min	Typ	Max	Unit
Video Bandwidth -3.0 dB Pins 4-17, 5-14, 6-11	AV = 4.5	50	—	—	MHz
Brightness Control Range	V ₈ = 0-5.0 V (Measured at Pins 11, 14, 17)	—	± 0.5	—	V
Contrast Control Range	V ₇ = 0-5.0 V	—	26	—	dB
Nominal Video Voltage Gain Pins 4-17, 5-14, 6-11	V ₇ = 5.0 V	—	4.5	—	
Video Clamp Reference Voltage Pin 19		—	2.5	—	V
Video Output Clamp Voltage	V ₈ = 2.5 V	—	2.5	—	V

The diagram illustrates the internal architecture of the MC1384 video processor. Key components and their connections include:

- Power and Reference:** A 5V Regulator (pin 38) provides +5V_{ref} (pin 39). T_{base} GND (pin 40) is connected to ground. Video GND (pin 9) is the common ground for video signals.
- Control and Timing:** The Sync Input Control (pins 37-34) receives T_{base} VCC (pin 31) and V_{sync} (pin 32). It outputs H_{sync} (pin 33) to the Primary Phase Detector. The Vertical Oscillator (pins 33-32) and Vertical Ramp (pins 30-28) generate vertical timing signals.
- Phase Detection and Locking:** The Primary Phase Detector (pins 40, 2, 1) outputs Up (pin 37), Down (pin 36), and H (pin 35) signals. The Horizontal Lock Control (pins 35, 34, 33, 32, 31, 30, 29, 28) receives these signals and outputs H_{ramp1} (pin 25) and H_{ramp2} (pin 26). The Horizontal Drive (pins 23, 22, 21) receives H_{ramp1} and H_{ramp2} and outputs H_{sync} (pin 33), H_{up} (pin 37), and H_{down} (pin 36).
- Video Processing:** The Brightness and Contrast Processor (pins 7, 8) receives ABL (pin 3) and Video Reference (pin 19). It outputs Red (pin 13), Green (pin 15), and Blue (pin 10) signals to the Video Input Red (pin 13), Video Input Green (pin 15), and Video Input Blue (pin 10) blocks. These blocks output to the Video Driver Red (pin 13), Video Driver Green (pin 15), and Video Driver Blue (pin 10) blocks. The Video Driver Red (pin 13) also outputs to the Video Driver Green (pin 15) and Video Driver Blue (pin 10).
- Other Features:** The Dual Current Source (pins 2, 1) outputs IF (pin 3) and IV (pin 4) signals. The 32H Oscillator (pin 3) outputs 32H (pin 4) to the Divide by 32 + Clamp Pulse Decode (pin 4) block, which outputs a Clamp Pulse (pin 4) to the Video Input Red (pin 13), Video Input Green (pin 15), and Video Input Blue (pin 10) blocks. The X-Ray Latch (pin 23) is controlled by H_{sync} (pin 33) and outputs to the Horizontal Drive (pin 23).

SIMPLIFIED BLOCK DIAGRAM DESCRIPTION

5.0 Volt Regulator — The regulator reference is derived from the V_{CC} . This is buffered and used as an internal voltage source for many functions within the device.

Sync Input Control — In this block the polarity of the TTL sync inputs is monitored and corrected automatically. In the absence of horizontal or composite TTL sync the default input becomes the composite sync separator. The integrator that forms part of the vertical polarity correction has an external capacitor, the voltage at which can be used to determine the polarity of the vertical TTL sync and therefore the mode of certain PC graphics standards. The MC1382 uses this pin for mode control.

Vertical Oscillator — This oscillator is injection-locked by the signal from the sync input control and provides a drive for the vertical ramp generator.

Vertical Ramp Generator — An adjustable linearity and amplitude vertical rate ramp is generated-locked to the vertical oscillator.

32H Oscillator — A current controlled oscillator running at 32 times horizontal rate is locked to the external horizontal sync using a PLL.

Divide by 32 and Clamp Pulse Decoder — The 32H oscillator frequency is divided down to H frequency and a pulse decoded for back porch clamping of the video.

Dual Current Source, I_{fix} I_{var} — The fixed and variable current sources control the 32H oscillator as part of the phase-locked loop. The variable source is used elsewhere in the device for various horizontal frequency dependent functions.

Primary Phase Detector and Unity Gain Buffer — The H_{sync} and H signals are phase compared and used to drive a unity gain buffer the output of which is used to control I_{var} , thus completing the PLL.

Horizontal Lock Control — This block provides frequency agility to the horizontal PLL.

Hramp1 and Comparator 1 — The picture position is controlled by slicing the output of Hramp1.

Hramp2, Comparator 2 and Comparator 3 — These blocks control the duty cycle and position of the horizontal drive pulse.

Secondary Phase Detector — Horizontal flyback is compared with Comparator 2 output to provide automatic compensation for horizontal output stage turn-off delay.

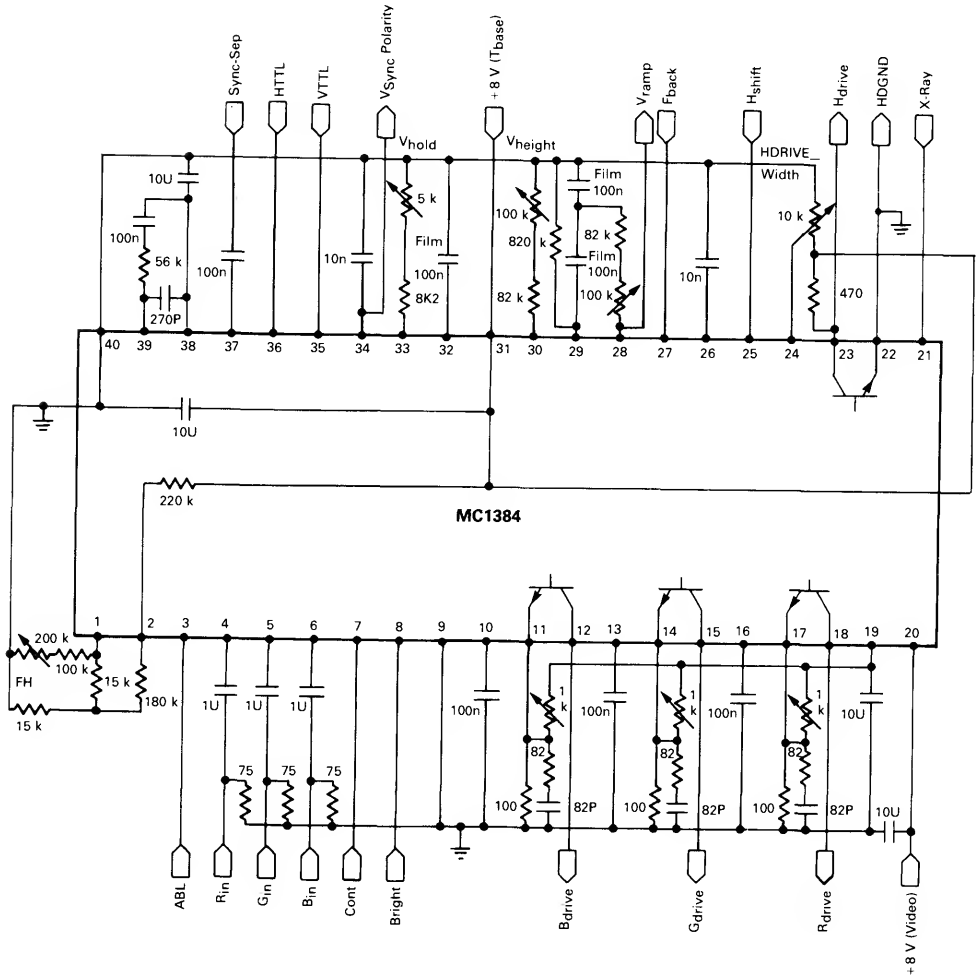
X-Ray Latch and Horizontal Drive — If the threshold of the latch is exceeded the horizontal drive is permanently on until the V_{CC} is removed.

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MC1384

APPLICATION CIRCUIT DIAGRAM



MC1391P

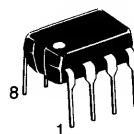
TV HORIZONTAL PROCESSOR

... low-level horizontal sections including phase detector, oscillator and pre-driver — a device designed for use in all types of television receivers.

- Internal Shunt Regulator
- Preset Hold Control Capability
- ± 300 Hz Typical Pull-In
- Linear Balanced Phase Detector
- Variable Output Duty Cycle for Driving Tube or Transistor
- Low Thermal Frequency Drift
- Small Static Phase Error
- Adjustable dc Loop Gain
- Positive Flyback Inputs

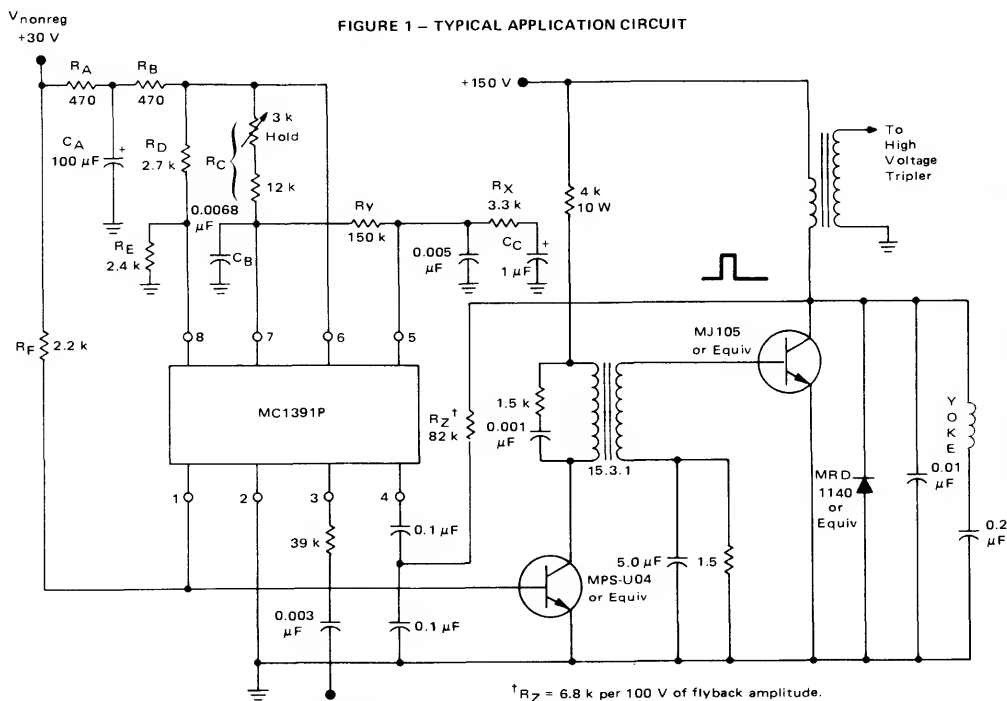
TV HORIZONTAL PROCESSOR

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**



P SUFFIX
PLASTIC PACKAGE
CASE 626

FIGURE 1 — TYPICAL APPLICATION CIRCUIT



This circuit has an oscillator pull-in range of ± 300 Hz, a noise bandwidth of 320 Hz, and a damping factor of 0.8.

MC1391P

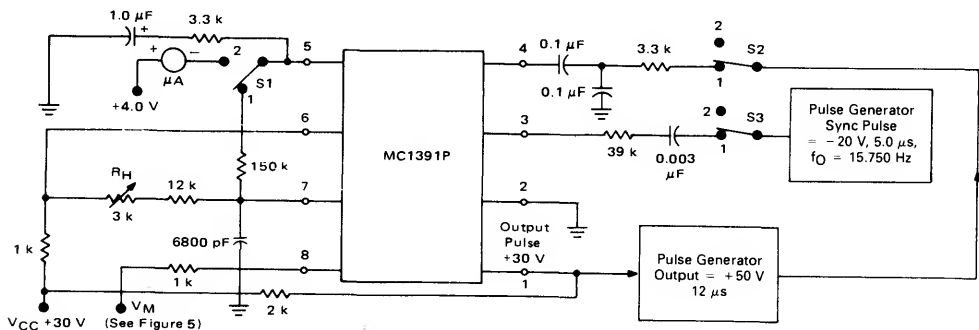
MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted.)

Rating	Value	Unit
Supply Current	40	mAdc
Output Voltage	40	Vdc
Output Current	30	mAdc
Sync Input Voltage (Pin 3)	5.0	V(p-p)
Flyback Input Voltage (Pin 4)	5.0	V(p-p)
Power Dissipation (Package Limitation)		
Plastic Package	625	mW
Derate above $T_A = +25^\circ\text{C}$	5.0	mW/ $^\circ\text{C}$
Operating Temperature Range (Ambient)	0 to +70	$^\circ\text{C}$
Storage Temperature Range	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted.) (See Test Circuit of Figure 2, all switches in position 1.)

Characteristic	Min	Typ	Max	Unit
Regulated Voltage (Pin 6)	8.0	8.6	9.4	Vdc
Supply Current (Pin 6)	—	20	—	mAdc
Collector-Emitter Saturation Voltage (Output Transistor Q1 in Figure 6)				Vdc
$I_C = 20 \text{ mA}$, Pin 1) Vdc	—	0.15	0.25	
Voltage (Pin 4)	—	2.0	—	Vdc
Oscillator Pull-in Range (Adjust R_H in Figure 2)	—	± 300	—	Hz
Oscillator Hold-in Range (Adjust R_H in Figure 2)	—	± 900	—	Hz
Static Phase Error ($\Delta f = 300 \text{ Hz}$)	—	0.5	—	$^\circ$
Free-running Frequency Supply Dependence (S1 in position 2)	—	± 3.0	—	Hz/Vdc
Phase Detector Leakage (Pin 5)	—	—	± 1.0	μA
Sync Input Voltage (Pin 3)	2.0	—	5.0	V(p-p)
Sawtooth Input Voltage (Pin 4)	1.0	—	3.0	V(p-p)

FIGURE 2 – TEST CIRCUIT



MC1391P

TYPICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 3 – FREQUENCY versus TEMPERATURE

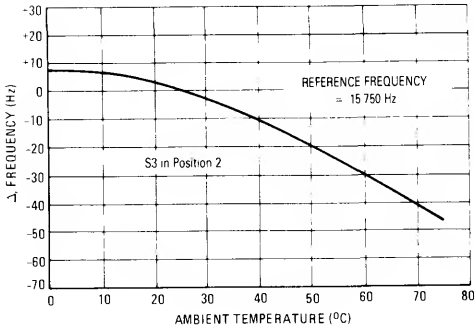


FIGURE 4 – FREQUENCY DRIFT versus WARM-UP TIME

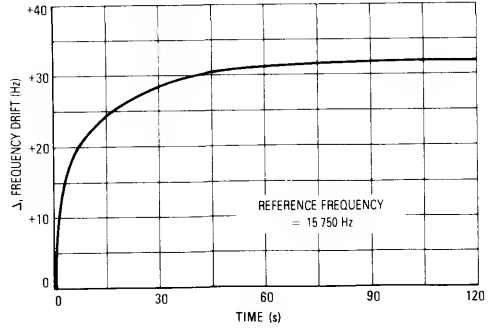


FIGURE 5 – MARK SPACE RATIO

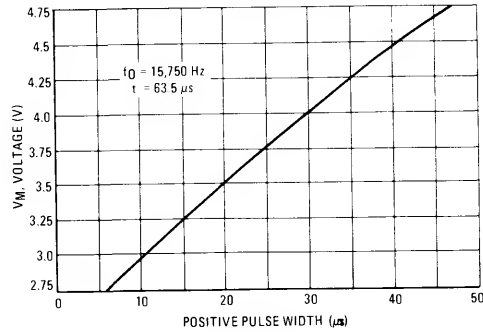
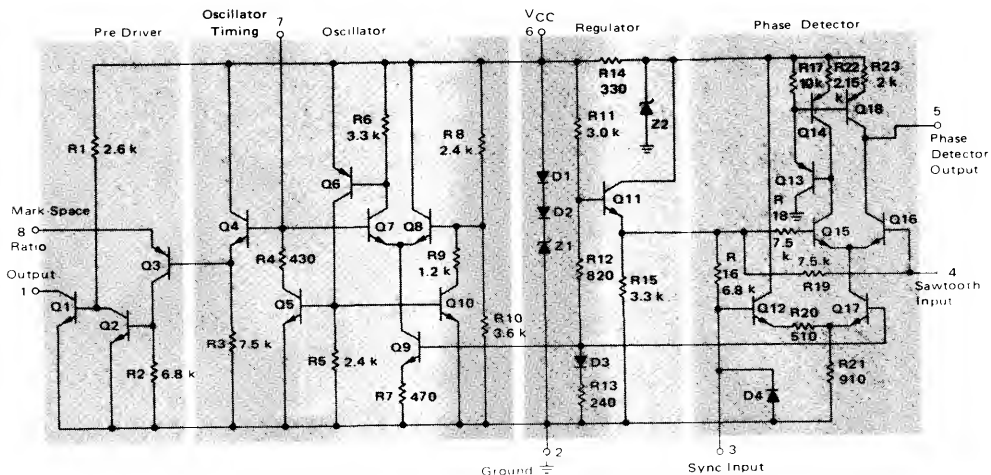


FIGURE 6 – CIRCUIT SCHEMATIC



MC1391P

CIRCUIT OPERATION

The MC1391P contains the oscillator, phase detector and predriver sections needed for a television horizontal APC loop.

The oscillator is an RC type with one pin (Pin 7) used to control the timing. The basic operation can be explained easily. If it is assumed that Q7 is initially off, then the capacitor connected from Pin 7 to ground will be charged by an external resistor (R_C) connected to Pin 6. As soon as the voltage at Pin 7 exceeds the potential set at the base of Q8 by resistors R8 and R10, Q7 will turn on and Q6 will supply base current to Q5 and Q10. Transistor Q10 will set a new, lower potential at the base of Q8 determined by R8, R9 and R10. Then, transistor Q5 will discharge the capacitor through R4 until the base bias of Q7 falls below that of Q8, at which time Q7 will turn off and the cycle repeats.

The sawtooth generated at the base of Q4 will appear across R3 and turn off Q3 whenever it exceeds the bias set on Pin 8. By adjusting the potential at Pin 8, the duty cycle (MSR) at the predriver output pin (Pin 1) can be changed to accommodate

either tube or transistor horizontal output stages.

The phase detector is isolated from the remainder of the circuit by R14 and Z2. The phase detector consists of the comparator Q15, Q16 and the gated current source Q17. Negative going sync pulses at Pin 3 turn off Q12 and the current division between Q15 and Q16 will be determined by the phase relationship of the sync and the sawtooth waveform at Pin 4, which is derived from the horizontal flyback pulse. If there is no phase difference between the sync and sawtooth, equal currents will flow in the collectors of Q15 and Q16 each for half the sync pulse period. The current in Q15 is turned around by Q18 so that there is no net output current at Pin 5 for balanced conditions. When a phase offset occurs, current will flow either in or out of Pin 5. This pin is connected via an external low-pass filter to Pin 7, thus controlling the oscillator.

Shunt regulation for the circuit is obtained with a zero temperature coefficient from the series combination of D1, D2 and Z1.

APPLICATION INFORMATION

Although it is an integrated circuit, the MC1391P has all the flexibility of a conventional discrete component horizontal APC loop.

The internal temperature compensated voltage regulator allows a wide supply voltage variation to be tolerated, enabling operation from nonregulated power supplies. A minimum value for supply current into Pin 6 to maintain zener regulation is about 18 mA. Allowing 2 mA for the external dividers

$$R_A + R_B = \frac{V_{\text{nonreg(min)}} - 8.8}{20 \times 10^{-3}}$$

Components R_A , R_B and C_A are used for ripple rejection. If the supply voltage ripple is expected to be less than 100 mV (for a 30 Volt supply) then R_A and R_B can be combined and C_A omitted.

The output pulse width can be varied from 6 μ s to 48 μ s by changing the voltage at Pin 8 (see Figure 5). However, care should be taken to keep the lead lengths to Pin 8 as short as possible to prevent ringing which can result in erroneous output pulses at Pin 1. The parallel impedance of R_D and R_E should be close to 1 k Ω to ensure stable pulse widths.

For 15 mA drive at saturation

$$R_F = \frac{V_{\text{nonreg}} - 0.3}{15 \times 10^{-3}}$$

The oscillator free-running frequency is set by R_C and C_B connected to Pin 7. For values of $R_C \gg R_{\text{discharge}}$ (R4 in Figure 6), a useful approximation for the free-running frequency is

$$f_O = \frac{1}{0.6 R_C C_B}$$

Proper choice of R_C and C_B will give a wide range of oscillator frequencies — operation at 31.5 kHz for count-down circuits is possible for example. As long as the product $R_C C_B = 10^{-4}$ many combinations of values of R_C and C_B will satisfy the free-running frequency requirement of 15.734 kHz. However, the sensitivity of the oscillator (β) to control-current from the phase detector is directly dependent on the magnitude of R_C , and this provides a convenient method of adjusting the dc loop gain (f_c).

For a given phase detector sensitivity (μ) = 1.60×10^{-4} A rad

$$f_c = \mu \beta \text{ and } \beta = 3.15 \times R_C \text{ Hz/mA}$$

Increasing R_C will raise the dc loop gain and reduce the static phase error (S.P.E.) for a given frequency offset. Secondary effects are to increase the natural resonant frequency of the loop (ω_n) and give a wider pull-in range from an out-of-lock condition. The loop will also tend to be underdamped with fast pull-in times, producing good airplane flutter performance. However, as the loop becomes more underdamped impulse noise can cause shock excitation of the loop. Unlimited increase in the dc loop gain will also raise the noise bandwidth excessively causing horizontal jitter with thermal noise. Once the dc loop gain has been selected for adequate S.P.E. performance, the loop filter can be used to produce the balance between other desirable characteristics. Damping of the loop is achieved most directly by changing the resistor R_X with respect to R_Y which modifies the ac/dc gain ratio (m) of the loop. Lowering this ratio will reduce the pull-in range and noise bandwidth (f_{nn}). (Note: very large values of R_Y will limit the control capability of the phase detector with a corresponding reduction in hold-in range.)

Static phasing can be adjusted simply by adding a small resistor between the flyback pulse integrating capacitor and ground. The sync coupling capacitor should not be too small or it can charge during the vertical pulse and this may result in picture bends at the top of the CRT.

NOTE:

In adjusting the loop parameters, the following equations may prove useful:

$$f_{nn} = \frac{1 \times \chi^2 T \omega_c}{4 \chi T}$$

$$\omega_n = \sqrt{\frac{\omega_c}{(1 + \chi) T}}$$

$$K = \frac{\chi^2 T \omega_c}{4}$$

$$\chi = \frac{R_X}{R_Y}$$

$$\omega_c = 2 \pi f_c$$

$$T = R_Y C_C$$

where:

K = loop damping coefficient

MC3340P

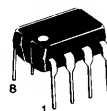
ELECTRONIC ATTENUATOR

The MC3340P is a simple but very effective electronic attenuator. This device offers up to 80 dB of attenuation control for frequencies to 1.0 MHz. THD (distortion) is less than 1 percent — up to 15 dB attenuation and less than three percent — up to 40 dB. Typical uses include instrumentation control, remote control audio amplifiers, electronic games, and CATV (cable TV) set-top converter audio control.

- Designed for use in:
 DC Operated Volume Control
 Compression and Expansion Amplifier Applications
- Controlled by DC Voltage or External Variable Resistor
- Economical 8-Pin Dual-In-Line Package

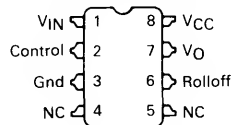
ELECTRONIC ATTENUATOR

**SILICON MONOLITHIC
 INTEGRATED CIRCUIT**



P SUFFIX
 PLASTIC PACKAGE
 CASE 626

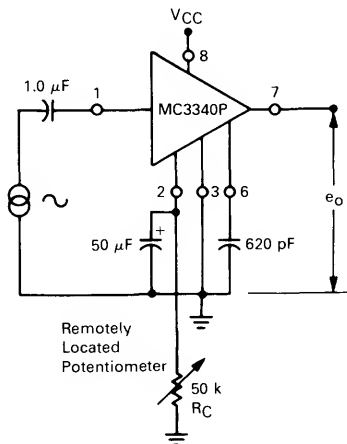
PIN ASSIGNMENTS



MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	20	Vdc
Power Dissipation ($T_A = 25^\circ\text{C}$ Derate above $T_A = 25^\circ\text{C}$)	P_D	1.2 10	Watts mW/ $^\circ\text{C}$
Operating Ambient Temperature Range	T_A	0 to +75	$^\circ\text{C}$

FIGURE 1 — TYPICAL DC "REMOTE" VOLUME CONTROL



MC3340P

ELECTRICAL CHARACTERISTICS ($e_{in} = 100 \text{ mV (RMS)}$, $f = 1.0 \text{ kHz}$, $V_{CC} = 16 \text{ Vdc}$, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

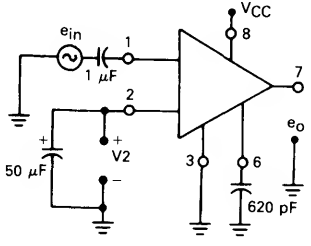
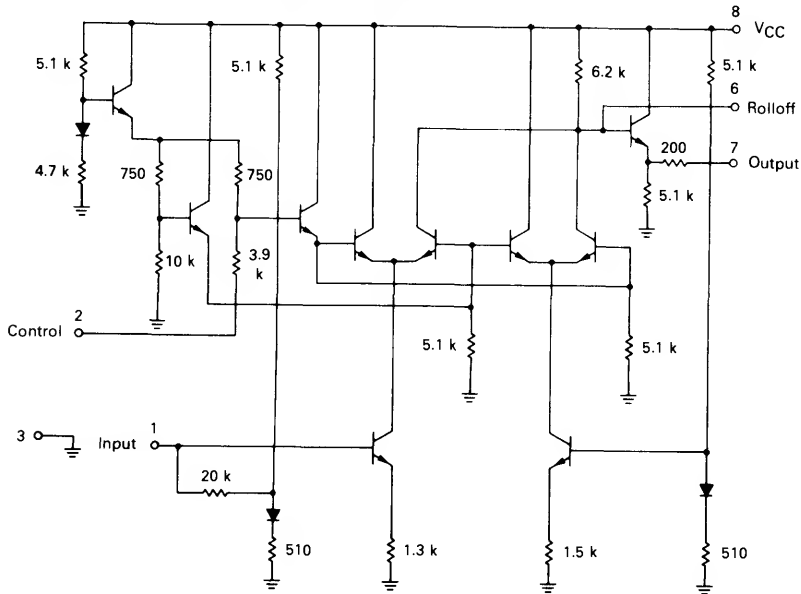
Circuit	Characteristic	Min	Typ	Max	Unit
	Operating Power Supply Voltage	8.0	—	18	Vdc
	Control Terminal Sink Current, Pin 2 ($e_{in} = 0$)	—	—	2.0	mAdc
	Maximum Input Voltage	—	—	0.5	V(RMS)
	Voltage Gain	11	13	—	dB
	Attenuation Range from Max Gain ($V_2 = 6.5 \text{ Vdc}$)	70	80	—	dB
	Total Harmonic Distortion (Pin 2 Gnd) ($e_{in} = 100 \text{ mV (RMS)}$, $e_o = A_v \times e_{in}$)	—	0.6	1.0	%

FIGURE 2 — CIRCUIT SCHEMATIC

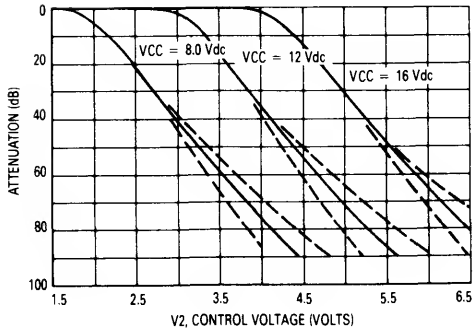


MC3340P

TYPICAL ELECTRICAL CHARACTERISTICS

($V_{CC} = 16 \text{ Vdc}$, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

**FIGURE 3 – ATTENUATION
versus DC CONTROL VOLTAGE**



**FIGURE 4 – ATTENUATION
versus CONTROL RESISTOR**

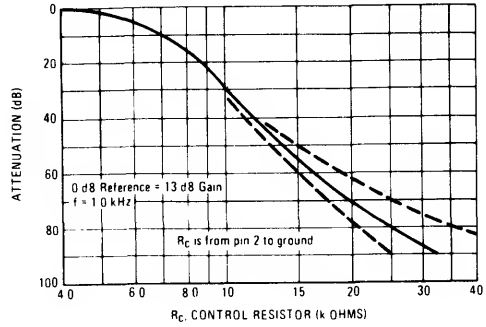


FIGURE 5 – FREQUENCY RESPONSE

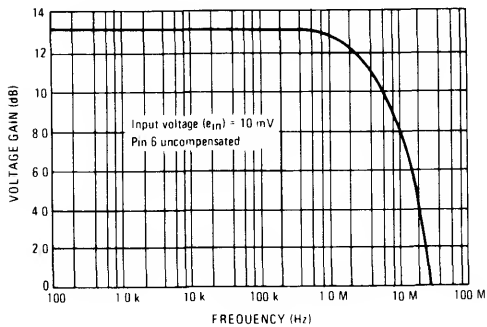


FIGURE 6 – OUTPUT VOLTAGE SWING

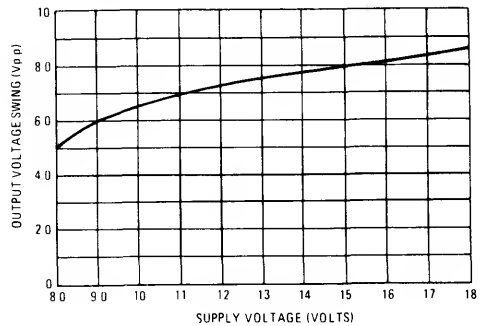
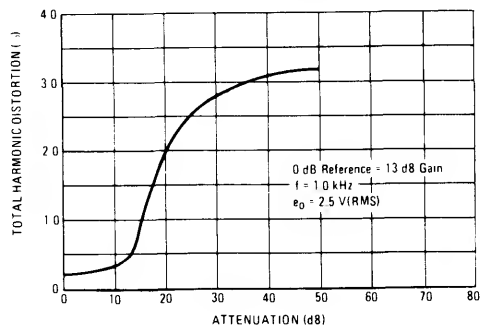


FIGURE 7 – TOTAL HARMONIC DISTORTION



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

MC3346

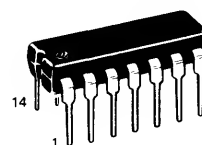
ONE DIFFERENTIALLY CONNECTED PAIR AND THREE ISOLATED TRANSISTOR ARRAY

The MC3346 is designed for general purpose, low power applications for consumer and industrial designs.

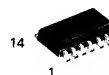
- Guaranteed Base-Emitter Voltage Matching
- Operating Current Range Specified – $10 \mu\text{A}$ to 10 mA
- Five General-Purpose Transistors in One Package

GENERAL PURPOSE TRANSISTOR ARRAY

SILICON MONOLITHIC
INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 646



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

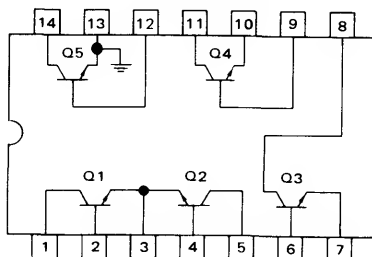
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	15	Vdc
Collector-Base Voltage	V_{CBO}	20	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector-Substrate Voltage	V_{CIO}	20	Vdc
Collector Current – Continuous	I_C	50	mA dc
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C Derate Each Transistor @ 25°C	P_D	1.2 10 300	Watts mW/ $^\circ\text{C}$ mW/ $^\circ\text{C}$
Operating Temperature Range	T_A	-40 to $+85$	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to $+150$	$^\circ\text{C}$

ORDERING INFORMATION

Device	Temperature Range	Package
MC3346D	-40°C to $+85^\circ\text{C}$	SO-14
MC3346P		Plastic DIP

PIN CONNECTIONS



Pin 13 is connected to substrate and must remain at the lowest circuit potential.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
STATIC CHARACTERISTICS					
Collector-Base Breakdown Voltage ($I_C = 10 \mu\text{Adc}$)	$V_{(BR)CBO}$	20	60	—	Vdc
Collector-Emitter Breakdown Voltage ($I_C = 1.0 \text{ mAdc}$)	$V_{(BR)CEO}$	15	—	—	Vdc
Collector-Substrate Breakdown Voltage ($I_C = 10 \mu\text{A}$)	$V_{(BR)CIO}$	20	60	—	Vdc
Emitter-Base Breakdown Voltage ($I_E = 10 \mu\text{Adc}$)	$V_{(BR)EBO}$	5.0	7.0	—	Vdc
Collector-Base Cutoff Current ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$)	I_{CBO}	—	—	40	nAdc
DC Current Gain ($I_C = 10 \text{ mAdc}$, $V_{CE} = 3.0 \text{ Vdc}$) ($I_C = 1.0 \text{ mAdc}$, $V_{CE} = 3.0 \text{ Vdc}$) ($I_C = 10 \mu\text{Adc}$, $V_{CE} = 3.0 \text{ Vdc}$)	h_{FE}	— 40 —	140 130 60	— — —	—
Base-Emitter Voltage ($V_{CE} = 3.0 \text{ Vdc}$, $I_E = 1.0 \text{ mAdc}$) ($V_{CE} = 3.0 \text{ Vdc}$, $I_E = 10 \text{ mAdc}$)	V_{BE}	— —	0.72 0.8	— —	Vdc
Input Offset Current for Matched Pair Q1 and Q2 ($V_{CE} = 3.0 \text{ Vdc}$, $I_C = 1.0 \text{ mAdc}$)	$ I_{IO1} - I_{IO2} $	—	0.3	2.0	μAdc
Magnitude of Input Offset Voltage ($V_{CE} = 3.0 \text{ Vdc}$, $I_C = 1.0 \text{ mAdc}$)	—	—	0.5	5.0	mVdc
Temperature Coefficient of Base-Emitter Voltage ($V_{CE} = 3.0 \text{ Vdc}$, $I_C = 1.0 \text{ mAdc}$)	$\frac{\Delta V_{BE}}{\Delta T}$	—	-1.9	—	mV/°C
Temperature Coefficient	$\frac{ \Delta V_{IO} }{\Delta T}$	—	1.0	—	$\mu\text{V}/^\circ\text{C}$
Collector-Emitter Cutoff Current ($V_{CE} = 10 \text{ Vdc}$, $I_B = 0$)	I_{CEO}	—	—	0.5	μAdc
DYNAMIC CHARACTERISTICS					
Low Frequency Noise Figure ($V_{CE} = 3.0 \text{ Vdc}$, $I_C = 100 \mu\text{Adc}$, $R_S = 1.0 \text{ k}\Omega$, $f = 1.0 \text{ kHz}$)	NF	—	3.25	—	dB
Forward Current Transfer Ratio ($V_{CE} = 3.0 \text{ Vdc}$, $I_C = 1.0 \text{ mAdc}$, $f = 1.0 \text{ kHz}$)	h_{FE}	—	110	—	—
Short-Circuit Input Impedance ($V_{CE} = 3.0 \text{ Vdc}$, $I_C = 1.0 \text{ mAdc}$)	h_{ie}	—	3.5	—	k Ω
Open-Circuit Output Impedance ($V_{CE} = 3.0 \text{ Vdc}$, $I_C = 1.0 \text{ mAdc}$)	h_{oe}	—	15.6	—	μmhos
Reverse Voltage Transfer Ratio ($V_{CE} = 3.0 \text{ Vdc}$, $I_C = 1.0 \text{ mAdc}$)	h_{re}	—	1.8	—	$\times 10^{-4}$
Forward Transfer Admittance ($V_{CE} = 3.0 \text{ Vdc}$, $I_C = 1.0 \text{ mAdc}$, $f = 1.0 \text{ MHz}$)	Y_{fe}	—	31 - j1.5	—	—
Input Admittance ($V_{CE} = 3.0 \text{ Vdc}$, $I_C = 1.0 \text{ mAdc}$, $f = 1.0 \text{ MHz}$)	Y_{ie}	—	0.3 + j0.04	—	—
Output Admittance ($V_{CE} = 3.0 \text{ Vdc}$, $I_C = 1.0 \text{ mAdc}$, $f = 1.0 \text{ MHz}$)	Y_{oe}	—	0.001 + j0.03	—	—
Current-Gain — Bandwidth Product ($V_{CE} = 3.0 \text{ Vdc}$, $I_C = 3.0 \text{ mAdc}$)	f_T	300	550	—	MHz
Emitter-Base Capacitance ($V_{EB} = 3.0 \text{ Vdc}$, $I_E = 0$)	C_{eb}	—	0.6	—	pF
Collector-Base Capacitance ($V_{CB} = 3.0 \text{ Vdc}$, $I_C = 0$)	C_{cb}	—	0.58	—	pF
Collector-Substrate Capacitance ($V_{CS} = 3.0 \text{ Vdc}$, $I_C = 0$)	C_{CI}	—	2.8	—	pF

TYPICAL CHARACTERISTICS

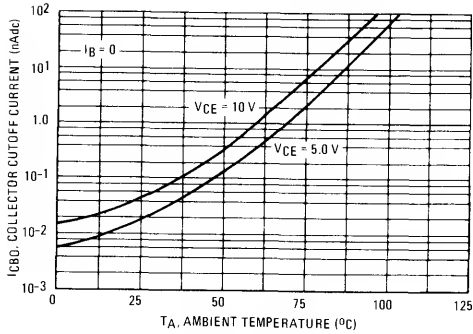
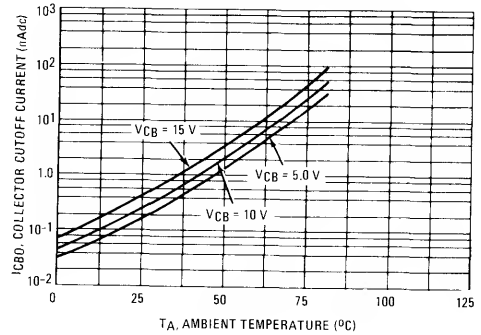
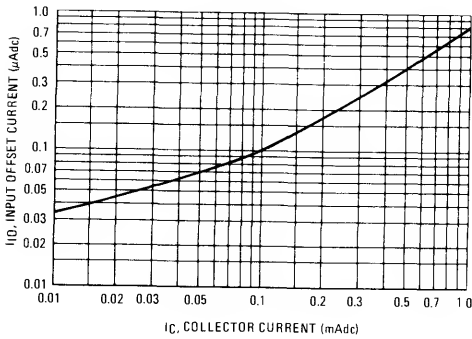
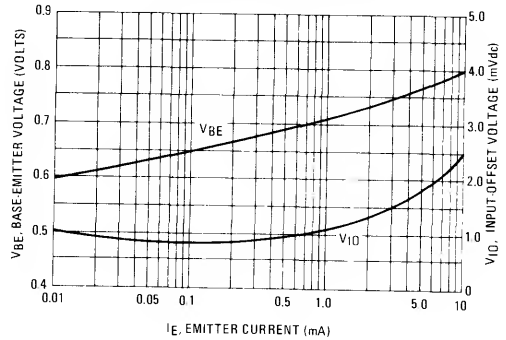
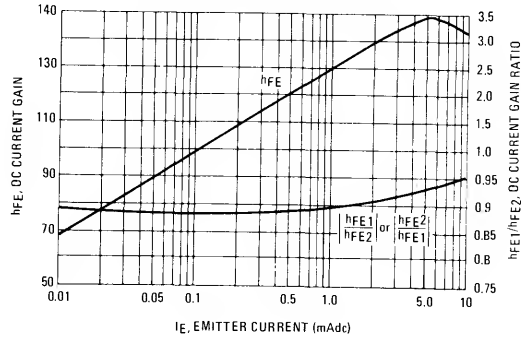
FIGURE 1 – COLLECTOR CUTOFF CURRENT
versus TEMPERATURE (Each Transistor)FIGURE 2 – COLLECTOR CUTOFF CURRENT
versus TEMPERATURE (Each Transistor)FIGURE 3 – INPUT OFFSET CHARACTERISTICS FOR
Q1 and Q2FIGURE 4 – BASE-EMITTER AND INPUT OFFSET
VOLTAGE CHARACTERISTICS

FIGURE 5 – DC CURRENT GAIN



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

REMOTE CONTROL AMPLIFIER-DETECTOR

The MC3373 is intended for application in infrared remote controls. It provides the high gain and pulse shaping needed to couple the signal from an IR receiver diode to the tuning control system logic.

- High Gain Pre-Amp
- Envelope Detector for PCM Demodulation
- Simple Interface to Microcomputer Remote Control Decoder
- May Be Used with Tuned Circuit for Narrow Bandwidth, Lower Noise Operation
- Small Package Size
- Minimum External Components
- Wide Operating Supply Voltage Range
- Low Current Drain
- Improved Retrofit for NEC Part No. μ PC1373
- See AN1016 for IR System Information
- MC14497 Recommended IR Transmitter
- MLED81 Complementary Emitter
- MRD821 Complementary Detector Diode

MAXIMUM RATINGS

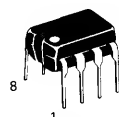
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	15	Vdc
Operating Temperature Range	T_A	0 to 75	$^{\circ}\text{C}$
Storage Temperature Range	T_{stg}	-55 to +125	$^{\circ}\text{C}$
Junction Temperature	T_J	150	$^{\circ}\text{C}$
Power Dissipation, Package Rating Derate above 25 $^{\circ}\text{C}$	P_D $1/\theta_{JA}$	1.25 10	Watts $\text{mW}/^{\circ}\text{C}$

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage (25 $^{\circ}\text{C}$)	V_{CC}	4.75	—	15	Vdc
Power Supply Voltage (0 $^{\circ}\text{C}$)	V_{CC}	5.0	—	15	Vdc
Input Frequency	f_{in}	30	40	80	kHz

MC3373

REMOTE CONTROL WIDEBAND AMPLIFIER WITH DETECTOR



P SUFFIX
PLASTIC PACKAGE
CASE 626



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

PIN CONNECTIONS

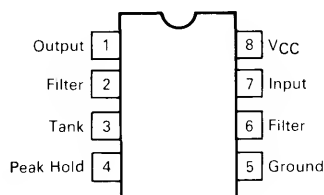
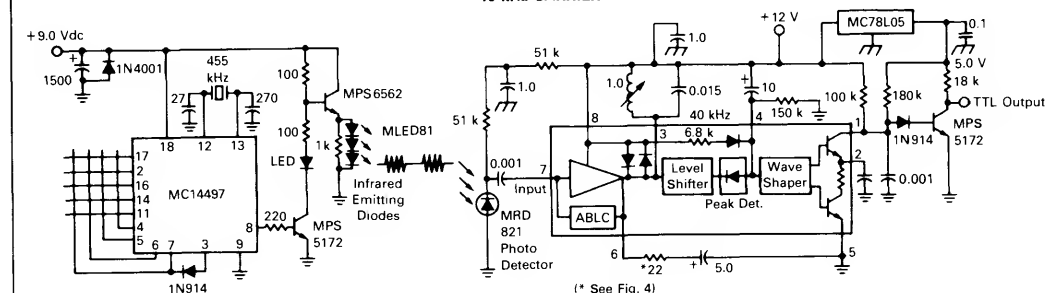


FIGURE 1 — REMOTE CONTROL APPLICATION
40 kHz CARRIER



MC3373

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$, $f_{in} = 40\text{ kHz}$, Test circuit of Figure 2)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Current	I_{CC}	1.5	2.5	3.5	mAdc
Input Terminal Voltage	$V(\text{Pin } 7)$	2.4	2.8	3.0	Vdc
Input Voltage Threshold	V_{in}	—	50	100	$\mu\text{Vp-p}$
Input Amplifier Voltage Gain ($V(\text{Pin } 3) = 500\text{ mVp-p}$)	A_V	—	60	—	dB
Input Impedance	r_{in}	40	60	80	$k\Omega$
Output Voltage, $V_{in} = 1.0\text{ mVp-p}$	V_{OL}	—	—	0.5	V
Output Leakage, $V_{CC} = V_{OH} = 15\text{ Vdc}$	I_{OH}	—	—	2.0	μA
Output Voltage, Input Open	V_{OH}	—	—	5.0	Vdc

**FIGURE 2 — TEST CIRCUIT
(BOTTOM VIEW)**

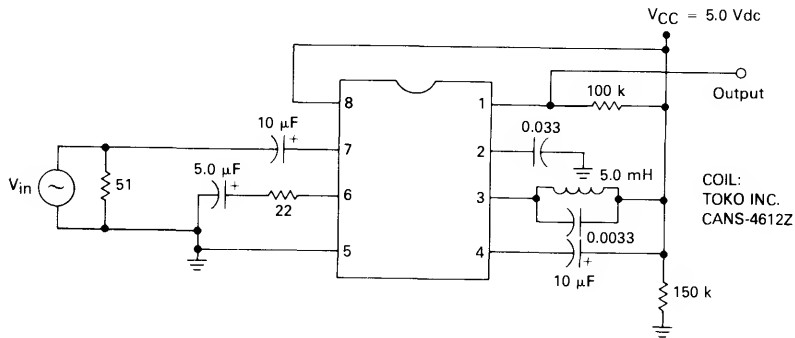


FIGURE 3 — BLOCK DIAGRAM

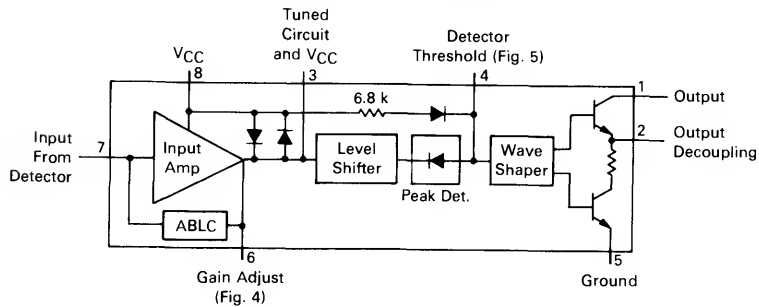


FIGURE 4 — INPUT AMPLIFIER GAIN

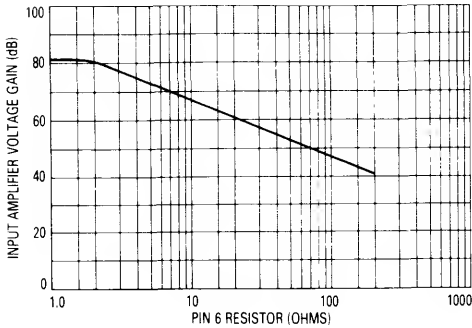


FIGURE 5 — DETECTOR THRESHOLD

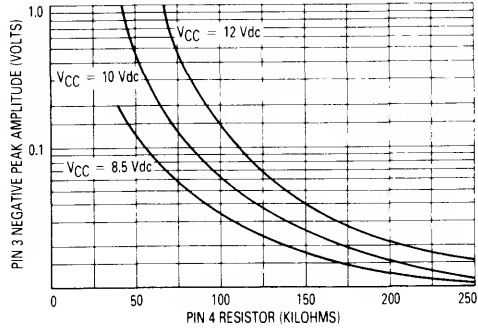
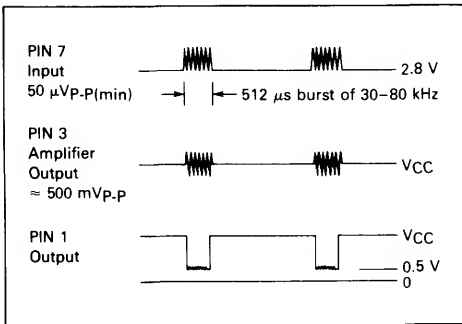


FIGURE 6 — TYPICAL SIGNAL WAVEFORMS



APPLICATIONS INFORMATION

The MC3373 is a specialized high gain amplifier/signal processor bipolar analog IC designed to be the core of infrared carrier signaling systems. The amplifier section has an automatic bias level control (ABLC) for simplified direct connection to an IR detector diode. Generally, it is operated AC coupled, utilizing an input high-pass filter to eliminate power line related noise, particularly that from fluorescent and gas vapor lamps. The use of a high frequency carrier is strongly recommended as opposed to simply detecting "DC" bursts of IR energy. In the carrier mode setup the MC3373 acts like an AM receiver subsystem, amplifying the incoming signal, demodulating it, and providing some basic wave shaping of the demodulated envelope. The tuned circuit at Pin 3 provides the main system selectivity reducing random noise interference and permitting multichannel operation in the same physical area without falsing. In the multichannel case the carriers must not be harmonically related. The bandwidth is determined primarily by the "Q" of the coil. Bandwidth may be increased by loading, shunting, the coil with a resistor.

Since this is a very high gain system operating at relatively high frequencies, care **must** be taken in the circuit layout and construction. Do not use wire wrap or non-ground plane protoboard. A simple single sided PCB with ground fill or a two-sided board with a solid groundplane and top side point-to-point will provide consistent high performance. There is a wide array of IR emitters/detectors available. The Motorola MLED81 and MRD821 are an excellent low cost combination to use with the MC3373. Multiple emitters are recommended for extended range. Application note AN1016 is must reading as it covers basic IR systems and specific applications.

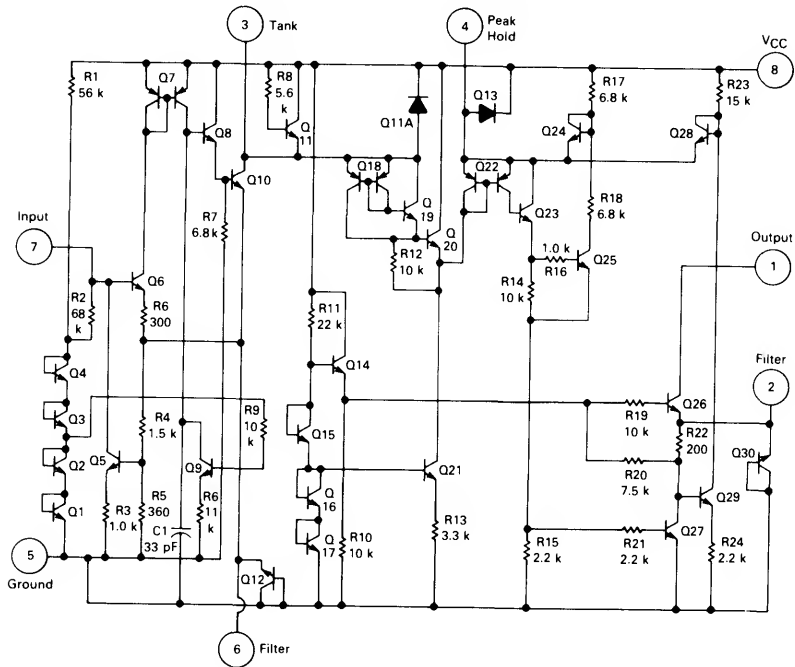
The input amplifier gain is approximately equal to the load impedance at Pin 3, divided by the resistor from Pin 6 to ground. Again, the low frequency gain can be reduced by using a small coupling capacitor in series with the Pin 6 resistor.

The load may be resistive, as shown in the application circuit, or tuned, as in the test circuit. The amplifier output is limited by back-to-back clamping diodes, level shifted, buffered and fed to a negative peak detector. The detector threshold is set by the external resistor on Pin 4, and an internal 6.8 kΩ resistor and diode to VCC. The capacitor from VCC to Pin 4 quickly charges during the negative peaks and then settles toward the set-up voltage between signal bursts at a rate roughly determined by the value of the capacitor and the 6.8 k resistor. The external capacitor at Pin 2 filters the ultrasonic carrier from the pulses.

Circuit Description (Refer to Figure 7)

Q1–Q4 set the bias on the amplifier input at approximately 2.8 V. Q6–Q10 form the input amplifier, which has a gain of about 80 dB when R(Pin 6) = 0. Q5 sinks input current from the photo diode and keeps the amplifier properly biased. Q18–Q20 level shift and buffer the signal to the negative peak detector, Q22 and Q23. Output devices Q26 and Q27 conduct during peaks and pull the output, Pin 1, low. The capacitor on Pin 2 filters out the carrier.

FIGURE 7 — INTERNAL SCHEMATIC



TRIPLE 4-BIT COLOR PALETTE VIDEO DAC

The MC10320 integrates a triple 4-bit digital-to-analog converter and a 16 x 12 color look-up table into a single 28 pin IC for use in a high resolution color graphics display system. The outputs are EIA-343-A compatible red, blue, and green video signals capable of driving single or doubly terminated 50 ohm or 75 ohm cables directly. Complementary outputs are provided for custom displays.

Control inputs include $\overline{\text{BLANK}}$ and $\overline{\text{SYNC}}$ to produce the levels required for vertical and horizontal retrace.

The color look-up table allows up to 16 color combinations (out of a palette of 4096 possible colors) on the screen at any one time. The table can be updated as often as required.

The lower speed digital inputs ($\overline{\text{WRITE}}$, $\overline{\text{DATA}}$, and $\overline{\text{SYNC}}$) are TTL compatible, whereas the high speed inputs ($\overline{\text{ADDRESS}}$, $\overline{\text{PIXEL}}$ $\overline{\text{CLOCK}}$, and $\overline{\text{BLANK}}$) can be user programmed to either ECL or TTL compatibility. The address and blank signals are latched into input registers, facilitating the timing requirements for those signals. Additional registers frame the data as it is presented to the three DACs, ensuring low glitch area and matched response.

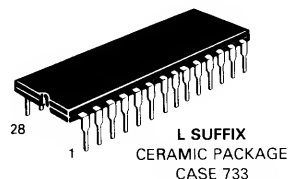
Innovative level translators permit the MC10320 series to be used in single or dual supply systems, permitting compatibility with most any system configuration. The MC10320 series is fabricated with Motorola's MOSAIC process, which provides both low power consumption and high speed.

- Triple 4-Bit Video DAC with 16 x 12 Color Look-Up Table
- 125 MHz Max Pixel Rate (MC10320), 90 MHz Max (MC10320-1)
- User Selectable TTL or ECL Compatibility on High Speed Inputs
- Single/Dual Supply Operation (Inputs and/or Outputs May Be Above/Below Ground)
- Supply Sensitivity Typically - 34 dB
- EIA-343-A Compatible Output Levels
- Directly Drives 50 or 75 Ohm Cables
- Low Power Dissipation — 684 mW Typical
- Internal Bandgap Reference
- $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ Control Inputs

MC10320 MC10320-1

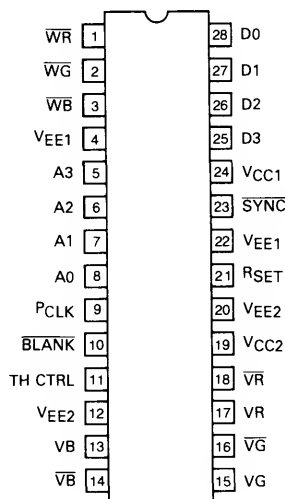
TRIPLE 4-BIT COLOR PALETTE VIDEO DAC

SILICON MONOLITHIC
INTEGRATED CIRCUIT



PIN CONNECTIONS

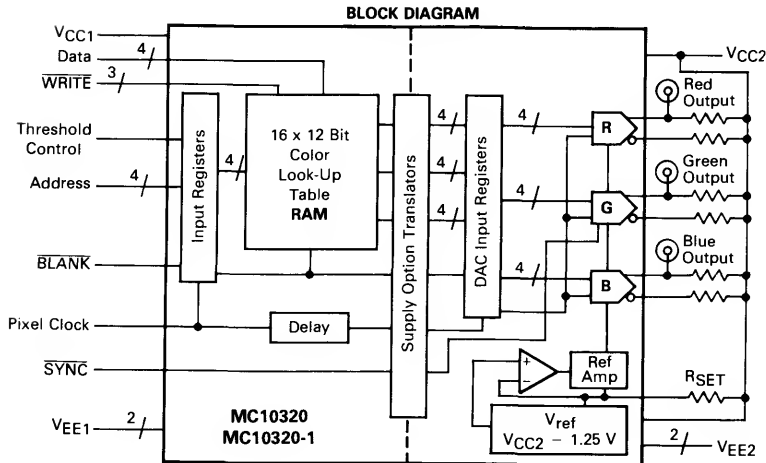
(Top View)



ORDERING INFORMATION

Maximum Pixel Rate	Device
125 MHz	MC10320L
90 MHz	MC10320L-1

MC10320, MC10320-1



ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Units
Supply Voltages		Vdc
VCC1 (Measured to VEE1)	-0.5, +7.0	
VCC2 (Measured to VEE2)	-0.5, +7.0	
VEE1 (Measured to VEE2)	-0.5, +7.0	
VCC2 (Measured to VEE1)	-0.5, +7.0	
Input Voltages (Address, Data, WR, WG, WB, SYNC, BLANK, PCLK, and Threshold Control)	VEE1 - 0.5, VCC1 + 0.5	Vdc
RSET (Pin 21)	VEE2 - 0.5, VCC2	Vdc
RSET External Resistor	0, 3.0 k	Ω
Outputs (VR, VR, VG, VG, VB, VB Measured to VEE2)	+2.5, +8.0	Vdc
Junction Temperature	-55, +150	°C

"Maximum Ratings" are not meant to imply that the device should be operated at these limits.
The "Recommended Operating Limits" provide for actual device operation.

RECOMMENDED OPERATING LIMITS

Parameter	Min	Typ	Max	Units
Single Supply — VCC1, VCC2 VEE1, VEE2	4.5	5.0	5.5	Vdc
or VCC1, VCC2 VEE1, VEE2	—	0	—	
Dual Supply — VCC1	—	0	—	
VCC2	-4.5	-5.0	-5.72	
VEE1	4.5	5.0	5.5	
VEE2	—	0	—	
RSET (Between VCC2 and Pin 21)	—	0	—	
ISET (Determined by RSET)	500	1.0 k	2.0 k	Ω
RL (Load Resistance at Each Output)	0.55	1.25	2.8	mA
	0	—	75	Ω
Input Voltages — Threshold Control (Pin 11, See Text)	VEE1	—	VCC1	Vdc
TTL High (Pins 1-3, 5-10, 23, 25-28,	VEE1 + 2.0	—	VCC1	
TTL Low Pin 11 connected to VEE1)	VEE1	—	VEE1 + 0.8	
ECL High (Pins 5-10 only, Pin 11	VCC1 - 1.13	—	VCC1	
ECL Low connected to VCC1)	VEE1	—	VCC1 - 1.48	
Output Compliance (Measured to VCC2)	-2.0	0	+2.0	Vdc
Ambient Temperature	0	—	+70	°C

MC10320, MC10320-1

ELECTRICAL CHARACTERISTICS (See Figure 1, $T_A = 25^\circ\text{C}$)

Parameter	Symbol	Min	Typ	Max	Units
Resolution (Each DAC)	Res	4.0	4.0	4.0	Bits
Palette Colors (Active) (Total Available)	—	—	—	16 4096	Colors Colors
Integral Nonlinearity	INL	-1.4	0	+1/4	LSB
Differential Nonlinearity	DNL	-1.4	0	+1/4	LSB
Monotonicity	—	Guaranteed (Note 1)			
Output Levels (α VR, VG, VB, relative to V_{CC2} unless otherwise noted. Ref. White Offset (DAC Input = 1111) BLANK, SYNC = 1	I_{OW} V_{OW}	— -15	50 -1.9	400 —	μA mV
Ref. Black (DAC Input = 0000) Relative to Ref. White, BLANK, SYNC = 1	I_{OB} V_{OB}	16.1 -682	17.2 -645	18.2 -604	mA mV
Blank Level Relative to Ref. Black BLANK = 0, SYNC = 1	I_{OBK} V_{OBK}	1.17 -56.2	1.33 -50	1.5 -43.9	mA mV
Sync Level — VG Only, Relative to Blank SYNC, BLANK = 0	I_{OSY} V_{OSY}	6.71 -320	7.63 -286	8.54 -251	mA mV
Total Error (Each DAC, Ref. White to Ref. Black)	GER	-6.0	0	+6.0	%
Gain Tracking Error (Any two DACs α Ref. Black)	GTR	-3.0	0	+3.0	%
Output Impedance α VR, VG, VB	Z_O	10	100	—	k Ω
Reference Voltage ($V_{CC2} - V_{RSET}$, $R_{SET} = 1.0\text{ k}\Omega$) Pin 21 Output DC Resistance (0 mA < I_{REF} < 3.0 mA)	V_{REF} —	-1.4 —	-1.25 3.0	-1.1 —	Vdc Ω
Input Voltage High (Data, \overline{WR} , \overline{WG} , \overline{WB} , SYNC) Low (Data, \overline{WR} , \overline{WG} , \overline{WB} , SYNC)	V_{IHA} V_{ILA}	$V_{EE1} + 2.0$ V_{EE1}	— —	V_{CC1} $V_{EE1} + 0.8$	Vdc
Input Voltage High (Address, P_{CLK} , \overline{BLANK}) (Threshold Control α V_{EE1} [TTL Mode]) (Threshold Control α V_{CC1} [ECL Mode])	V_{IHB} V_{IHC}	$V_{EE1} + 2.0$ $V_{CC1} - 1.13$	— —	V_{CC1} V_{CC1}	
Input Voltage Low (Address, P_{CLK} , \overline{BLANK}) (Threshold Control α V_{EE1} [TTL Mode]) (Threshold Control α V_{CC1} [ECL Mode])	V_{ILB} V_{ILC}	V_{EE1} V_{EE1}	— —	$V_{EE1} + 0.8$ $V_{CC1} - 1.48$	
Input Current (α 2.4 V (TTL Mode) (All Input Pins α 0.4 V (TTL Mode) Except Pin 11)	I_{IHA} I_{ILA}	— —	50 10	150 100	μA
Input Current α $V_{CC1} - 0.8\text{ V}$ (ECL Mode) α $V_{CC1} - 1.8\text{ V}$ (ECL Mode)	I_{IHB} I_{ILB}	— —	100 70	250 200	
Input Current α Pin 11 (Pin 11 = V_{CC1}) α Pin 11 (Pin 11 = V_{EE1})	I_{ITH} I_{ITL}	-5.0 -1.0	0 -0.4	— —	mA
Signal Feedthrough to Outputs Due to Pixel Clock (α 125 MHz for MC10320, BLANK 90 MHz MC10320-1) Data	SRR	— — —	-50 -50 -60	— — —	dB
Power Supply Rejection Ratio (All DACs) V_{CC1} α 1.0 kHz V_{CC1} α 1.0 MHz V_{CC1} α 50 MHz V_{EE2} α 1.0 kHz V_{EE2} α 1.0 MHz V_{EE2} α 50 MHz	PSRR	— — — — — —	60 45 30 50 33 12	— — — — — —	dB
Power Supply Sensitivity (Note 2)	—	—	0.02	0.12	%/%
Power Supply Requirements (See Figure 1) V_{CC1} Current ($V_{CC1} - V_{EE1} = 5.0\text{ V}$) V_{EE1} Current ($V_{CC1} - V_{EE1} = 5.0\text{ V}$) V_{CC2} Current ($V_{CC2} - V_{EE2} = 5.0\text{ V}$) V_{EE2} Current ($V_{CC2} - V_{EE2} = 5.0\text{ V}$, Includes output currents)	I_{CC1} I_{EE1} I_{CC2} I_{EE}	— — — —	50 -50 28 -92	70 -70 45 -120	mA
Power Dissipation (α 5.0 volt supplies)	P_D	—	684	894	mW

NOTES:

- Guaranteed by linearity tests.
- ($V_{CC1} - V_{EE1}$) and ($V_{CC2} - V_{EE2}$) are each varied from 4.5 to 5.72 volts, but not simultaneously.

MC10320, MC10320-1

TIMING CHARACTERISTICS (See Timing Diagram — Figure 2)

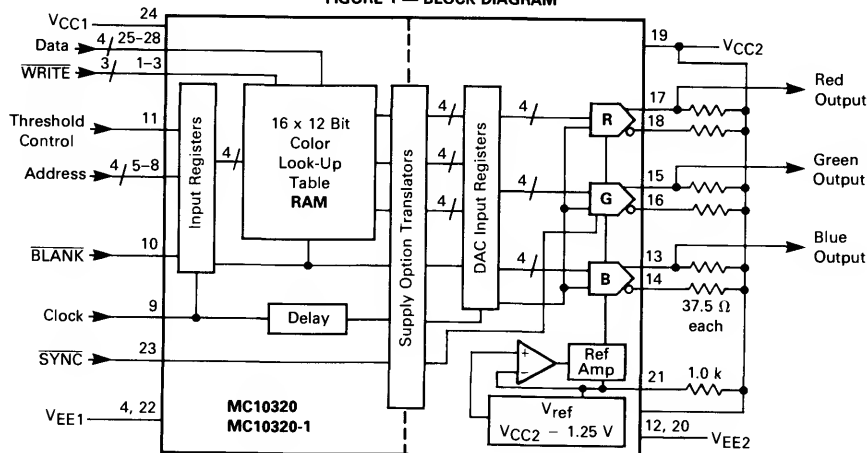
Parameter	Symbol	Min	Typ	Max	Units
READ Cycle (Display Mode)					
Address, BLANK Setup Time	t_{RSA}	—	1.5	—	ns
Address, BLANK Hold Time	t_{RHA}	—	1.5	—	ns
Clock Pulse Width — High	t_{PWH}	—	3.0	—	ns
Clock Pulse Width — Low	t_{PWL}	—	3.0	—	ns
Pipeline Delay	t_{PIPE}	1.0	1.0	1.0	clk cycle
DAC Prop Delay (P_{CLK} to 50% Point)	t_{DPD}	—	9.0	—	ns
DAC Prop Delay Difference (DAC to DAC)	$t_{DPD\Delta}$	—	0.5	—	ns
SYNC Prop Delay	t_{SPD}	—	6.0	—	ns
Output Settling Time ($\pm 1/2$ LSB to $\pm 1/2$ LSB)	t_{DS}	—	3.0	—	ns
Output Slew Rate	SR	—	300	—	V/ μ s
Glitch Area	AG	—	20	—	pV-S
WRITE Cycle (RAM Update Mode)					ns
Address Setup Time	t_{WSA}	—	1.5	—	
Address Hold Time	t_{WHA}	—	1.5	—	
Clock Setup Time	t_{WSC}	—	5.0	—	
Clock Hold Time	t_{WHC}	—	10	—	
Data Setup Time	t_{WSD}	—	90	—	
Data Hold Time	t_{WHD}	—	10	—	
Write Pulse Width	t_{WPW}	—	90	—	

TEMPERATURE CHARACTERISTICS

Parameter	Typ	Units
Offset (at Ref. White)	± 20	ppm GS/ $^{\circ}$ C
DAC Gain	± 100	ppm GS/ $^{\circ}$ C
Gain Tracking (any 2 DACs @ Ref. Black)	± 50	ppm GS/ $^{\circ}$ C
Linearity	± 100	ppm GS/ $^{\circ}$ C

(0 $^{\circ}$ C to +70 $^{\circ}$ C, ppm GS/ $^{\circ}$ C = Parts Per Million of Gray Scale/ $^{\circ}$ C.)

FIGURE 1 — BLOCK DIAGRAM



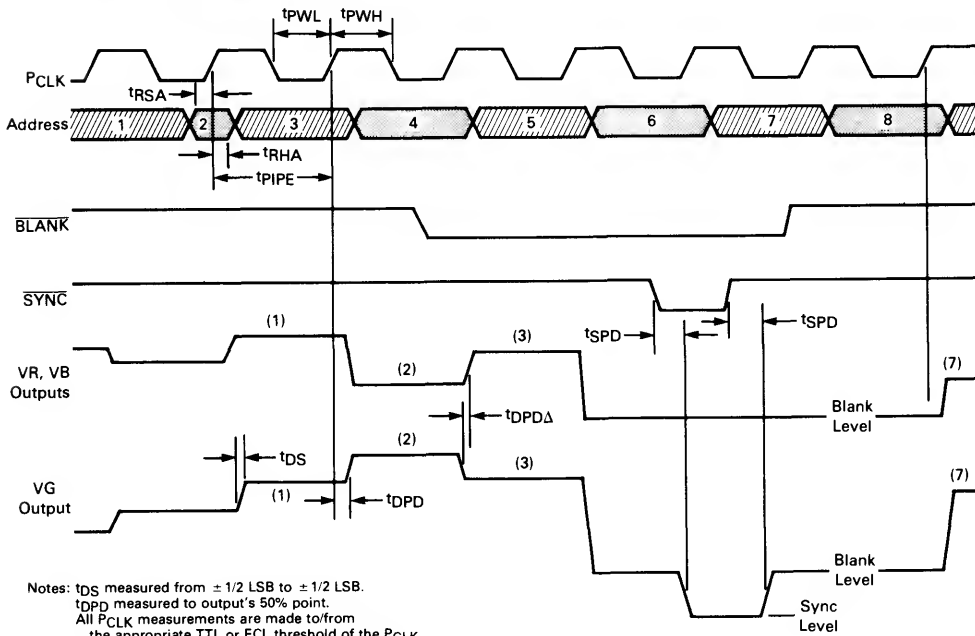
Note:

Electrical Characteristics are tested with both single and dual supply configurations at the typical supply voltages listed in the "Recommended Operating Limits." Input levels are TTL or ECL, as appropriate. Threshold control input is set at VCC1, or VEE1, as appropriate. Exceptions to these conditions are noted in the Characteristics.

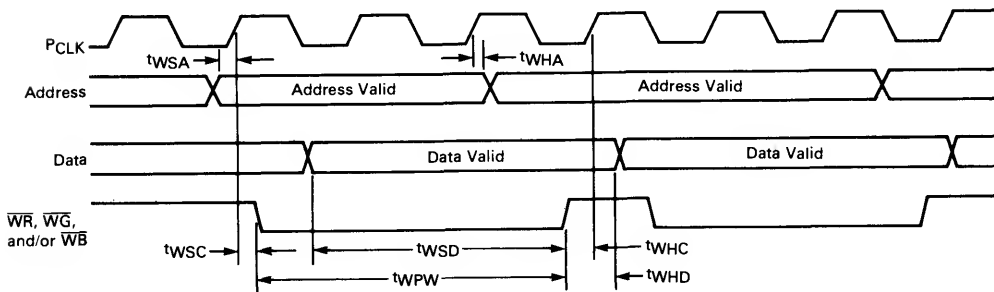
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FIGURE 2 — TIMING DIAGRAM

READ CYCLE (PIXEL DISPLAY MODE)



WRITE CYCLE (RAM UPDATE MODE)



PIN DESCRIPTIONS

Symbol	Pin	Description
WR	1	Write Enable (Red) — Taking this pin low enables the data (Pins 25–28) to be written into the selected address location for the RED look-up table. The data is latched in the RAM when the pin is high.
WG	2	Write Enable (Green) — Same as Pin 1, except for the GREEN table.
WB	3	Write Enable (Blue) — Same as Pin 1, except for the BLUE table.
VEE1	4	Power supply pin for all circuitry prior to the supply option translators (See Block Diagram). This is the reference for VCC1, and is typically 5.0 volts below it. Internally it is connected to Pin 22. This pin and Pin 22 must be connected externally for proper operation.
A0–A3	5–8	Address lines — They are used to select one of sixteen 12-bit words in the color look-up table for both reading and writing. The address is latched on the PCLK rising edge, and presented to the DACs on the following rising edge. Pin 5 is A3 (MSB), and Pin 8 is A0 (LSB).
PCLK	9	Pixel clock — Address and BLANK signals are latched on the rising edge of this clock. The following rising edge presents the data in the look-up table (of the selected address) to the DACs. SYNC is independent from PCLK.
BLANK	10	Blanking — A logic low overrides the color look-up table, and forces the three DACs to the blanking level. The BLANK input is latched, the same as the address lines.
ThCntrl	11	Threshold Control — When tied to VCC1, the PCLK, A0–A3, and BLANK inputs are at ECL levels with respect to VCC1. When tied to VEE1 (Pin 4 or 22), the same inputs are at TTL levels with respect to VEE1.
VEE2	12	Power supply pin for the circuitry to the right of the supply option translators (See Block Diagram). This is the reference for VCC2, and is typically 5.0 volts below it. It is internally connected to Pin 20. This pin and Pin 20 must be connected externally.
VB	13	The output of the BLUE 4-bit DAC. Output compliance is ± 2.0 volts with respect to VCC2, and output impedance is typically 100 k Ω . Designed for a typical load of 37.5 Ω , the load may be between 0 and 75 Ω . The output is a current sink.
VB	14	The complementary output of the BLUE DAC. This output may be used in conjunction with Pin 13 for twisted pair signal transmission or for custom interface schemes. If unused, it must be tied to VCC2.

PIN DESCRIPTIONS

Symbol	Pin	Description
VG	15	Same as Pin 13, except for the GREEN DAC. The SYNC signal appears at this output. Waveform polarity is "sync down."
VG	16	Same as Pin 14, except for the GREEN DAC. The SYNC signal appears at this output. Waveform polarity is "sync up."
VR	17	Same as Pin 13, except for the RED DAC.
VR	18	Same as Pin 14, except for the RED DAC.
VCC2	19	Power supply pin for the circuitry to the right of the supply option translators (See Block Diagram). Its reference is VEE2, and is nominally 5.0 volts more positive than VEE2.
VEE2	20	Power supply pin for the circuitry to the right of the supply option translators (See Block Diagram). This is the reference for VCC2, and is typically 5.0 volts below it. It is internally connected to Pin 12. This pin and Pin 12 must be connected externally.
RSET	21	Current setting resistor — A user supplied low inductance resistor is to be connected between VCC2 and this pin to set the DAC's full scale current. An RSET of 1.0 k Ω , combined with load resistors of 37.5 Ω (at Pins 13, 15, 17) provides output signals consistent with EIA-343-A. The RSET resistor is to be between 500 Ω to 2.0 k Ω . The voltage at this pin is 1.25 volts below VCC2.
VEE1	22	Power supply pin for all circuitry prior to the supply option translators (See Block Diagram). This is the reference for VCC1, and is typically 5.0 volts below it. Internally it is connected to Pin 4. This pin and Pin 4 must be connected externally for proper operation.
SYNC	23	A logic low on this input forces the GREEN DAC to increase its output current by 7.6 mA ($R_{SET} = 1.0$ k Ω), providing the sync level of 286 mV ($R_L = 37.5$ Ω) below blanking. The BLANK input must have been asserted previously. SYNC is independent of PCLK.
VCC1	24	Power supply pin for the circuitry to the left of the supply option translators (See Block Diagram). Its reference is VEE1, and is nominally 5.0 volts more positive than VEE1.
D0–D3	25–28	Data inputs — Information on these pins is written into the color look-up table, at the locations specified by the address lines, by taking the appropriate Write pin low. Pin 28 is D0 (LSB), and Pin 25 is D3 (MSB).

FUNCTIONAL DESCRIPTION

GENERAL

The MC10320 is a triple video DAC, with a 16 location color palette RAM, designed for high resolution graphics systems. The maximum pixel speed capability is 125 MHz for the MC10320, and 90 MHz for the MC10320-1. The input configurations are compatible with TTL or ECL systems, and the outputs are directly compatible with monitors having 50 Ω or 75 Ω RGB inputs. Using the external components recommended in this data sheet, the outputs will conform to EIA-343-A levels. The output levels are adjustable by means of the R_{SET} resistor.

The MC10320 contains three 4-bit DACs whose inputs are fed from a color palette RAM (data is loaded by the user). The RAM contains 16 locations (each 12 bits wide). Each 4-bit nibble of each RAM address can be individually loaded, so that every address location can have any one of a possible 4096 codes. The DAC output levels are determined by the contents of the selected RAM address (by means of the address inputs).

The MC10320 contains an input register to accept the address and Blanking information, and a second register located between the RAM and the DAC inputs. This arrangement ensures that the RAM data is presented to the 3 DACs simultaneously, which ensures the DAC outputs will transition simultaneously. The registers are toggled by the P_{CLK} input's rising edge.

The \overline{BLANK} input overrides the RAM data to the DACs, and forces the outputs to the Blanking level. The \overline{SYNC} input goes directly to the Green DAC, bypassing the RAM and the latches, forcing the green DAC output to shift. The combination of \overline{BLANK} and \overline{SYNC} produce the video sync level.

Referring to the Block Diagram, the input stage (circuitry to the left of the Supply Option Translators) and the output stage (to the right of the Translators) can be operated at different supply voltages. The only restriction is that the output stage cannot be more positive than the input stage.

INPUTS

Address, P_{CLK} , \overline{BLANK}

The Address, P_{CLK} (pixel clock), and \overline{BLANK} inputs are the "high speed" inputs capable of the maximum pixel clock rates mentioned above. The Address and \overline{BLANK} are latched into the input register on the rising edge of the P_{CLK} , as long as the required setup and hold times are adhered to. The data at that RAM address (or the \overline{BLANK} signal) is then presented to the DAC inputs on the next P_{CLK} rising edge.

The \overline{BLANK} input, when taken to a Logic "0" and clocked in as described above, will override the RAM data presented to the DACs, and force the 3 DAC outputs to the Blanking level (see Figure 2).

These 6 input pins can accept either TTL or ECL signals. With the Threshold Control pin (Pin 11) connected to V_{EE1} , the inputs are TTL compatible with respect to V_{EE1} , having a nominal threshold of 1.5 volts above

V_{EE1} , independent of V_{CC1} . With Pin 11 connected to V_{CC1} , the inputs are fully compatible with the 10 kH family of ECL devices, having a nominal threshold of 1.3 volts below V_{CC1} , independent of V_{EE1} .

Figure 3 depicts a typical input stage configuration, and Figure 4 indicates the typical input current. Figure 4 applies to both ECL and TTL modes of operation. The inputs should be kept within the range of V_{EE1} to V_{CC1} . If an input is taken more than 0.3 volts below V_{EE1} , or more than 0.5 volts above V_{CC1} , excessive currents will flow through that input, and the DAC output waveforms will be distorted.

SYNC

The \overline{SYNC} input goes directly to the green DAC, independent of the clock. When taken to a Logic "0", the output current at VG is forced to increase by $6.1 \times I_{SET}$. For a standard EIA-343-A system, the shift is 7.63 mA, resulting in a 286 mV change in the output voltage. The \overline{SYNC} input does **not** override the RAM data, requiring that the \overline{BLANK} input have been asserted (Logic "0") previously in order to obtain a proper video sync level. The \overline{SYNC} input does not affect the red or blue DACs.

The \overline{SYNC} input is always TTL compatible, with a nominal threshold of 1.5 volts above V_{EE1} , independent of V_{CC1} .

Figure 3 depicts the input stage configuration, and Figure 4 indicates the typical input current. The input should be kept within the range of V_{EE1} to V_{CC1} . If the input is taken more than 0.3 volts below V_{EE1} , or more than 0.5 volts above V_{CC1} , excessive currents will flow through the input, and the DAC output waveforms will be distorted.

DATA (1-4), \overline{WR} , \overline{WB} , \overline{WG}

The data (D0, D1, D2, D3), and \overline{WRITE} inputs are the "low speed" inputs, as they do not have to operate at the same high speed as the above mentioned inputs. These inputs are independent of the P_{CLK} , although they are normally used in conjunction with the clock.

Pins 25-28 are the data inputs to the color palette RAM, and are used for updating the RAM information. The information is written into the RAM at the address which was previously clocked into the input register, while the appropriate \overline{WRITE} input is low, and then latched in when the \overline{WRITE} input is taken high. The required data setup and hold times (mentioned in the Timing Characteristics) are with respect to the rising edge of the \overline{WRITE} input. If the same data is to be loaded into different nibbles (color sections) of the same address, the appropriate \overline{WRITE} inputs may be taken low simultaneously, or sequentially. \overline{WR} , \overline{WB} , and \overline{WG} control the loading of data into the red, blue and green nibbles respectively.

The data and \overline{WRITE} inputs are always TTL compatible, with a nominal threshold of 1.5 volts above V_{EE1} , independent of V_{CC1} .

In most applications, it will be advantageous to set the Blanking level while updating the RAM. If Blanking is not set, the DAC outputs will change unpredictably while new data is being written into the RAM.

Figure 3 depicts a typical input stage configuration, and Figure 4 indicates the typical input current. The inputs should be kept within the range of V_{EE1} to V_{CC1} . If an input is taken more than 0.3 volts below V_{EE1} , or more than 0.5 volts above V_{CC1} , excessive currents will flow through the input, and the DAC output waveforms will be distorted.

FIGURE 3 — TYPICAL INPUT STAGE

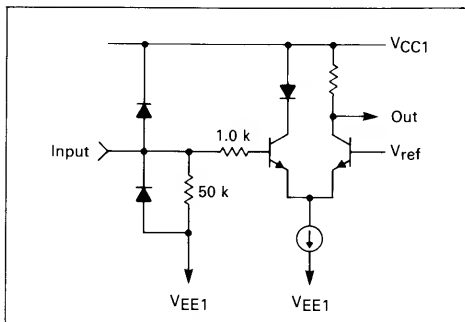
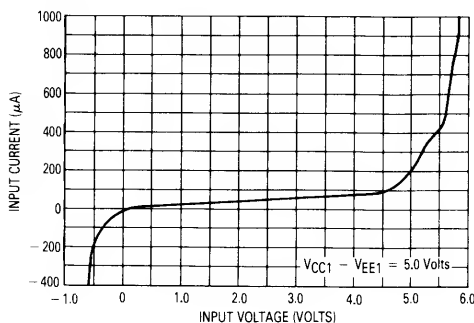


FIGURE 4 — INPUT CURRENT AT PINS 1-3, 5-10, 23, 25-28



THRESHOLD CONTROL

The Threshold Control input (Pin 11) is to be connected directly to V_{CC1} to set Pins 5-10 to ECL compatibility, or directly to V_{EE1} to set the pins to TTL compatibility. A series resistor should not be used with this input, and it should not be connected to any other voltage as an incorrect threshold will result at Pins 5-10. Bias current at Pin 11 is approximately 400 μ A out of the pin when at V_{EE1} , and 0 μ A when at V_{CC1} . If the pin is taken more than 0.3 volts below V_{EE1} , excessive currents will flow through this input, and the DAC output waveforms will be distorted.

OUTPUTS

The six DAC outputs (\overline{VB} , \overline{VB} , \overline{VG} , \overline{VG} , \overline{VR} , \overline{VR}) at Pins 13-18 are high impedance current sink outputs, with the current flow **into** the pins, never out. \overline{VG} , \overline{VB} , and \overline{VR} provide the conventional video polarity (sync down), while the complementary outputs provide a "sync up" waveform. The output loads must be connected from the outputs to V_{CC2} , or to a pullup voltage, such that the output voltages are within ± 2.0 volts of V_{CC2} . Unused outputs **must** be connected to V_{CC2} , and not left open.

The output current (for the gray scale) at Pins 13, 15, and 17 is related to the digital inputs (of the DACs) and the reference current (I_{SET} at Pin 21, equal to 1.25 V/ R_{SET}) by the following equation:

$$I_{OUT(GS)} = \frac{(15-A) \times I_{SET} \times 14.63}{16} \quad (\text{nominal value})$$

where A = binary value of the digital input (0-15). A digital input of 1111 (15) produces no output current, and therefore the most positive output voltage, referred to as "Reference White." An input code of 0000 (0) results in the maximum current, and therefore the Gray Scale's most negative output voltage, referred to as "Reference Black."

After the \overline{BLANK} input is asserted and clocked in as described above, the RAM data to the DACs is overridden, and the output current is set at:

$$I_{OUT(BLANK)} = I_{SET} \times 14.864 \quad (\text{nominal value})$$

When the \overline{SYNC} input is asserted, the output current at \overline{VG} is increased by:

$$\Delta I_{OUT(SYNC)} = I_{SET} \times 6.1 \quad (\text{nominal value})$$

The four outputs of the red and blue DACs are not affected by \overline{SYNC} . The current increase at \overline{VG} results regardless of the digital input to the Green DAC. To obtain the correct (EIA-343-A) sync level, the \overline{BLANK} output level must have previously been set. Otherwise the green output will simply shift by the above amount from the Gray Scale level in effect at the time the \overline{SYNC} input was asserted. If both \overline{BLANK} and \overline{SYNC} are asserted, the output current at \overline{VG} is:

$$I_{OUT(SYNC)} = I_{SET} \times 20.97 \quad (\text{nominal value})$$

The sum of the currents into each pair of outputs is a constant equal to $[20.93 \times I_{SET}]$ for the $\overline{VG}/\overline{VG}$ pair, and $[14.824 \times I_{SET}]$ for the $\overline{VR}/\overline{VR}$ and $\overline{VB}/\overline{VB}$ pairs. Table 1 summarizes the above information.

The voltage levels generated at the outputs depend on the value of I_{SET} and the load impedance. An R_{SET} of 1.0 k Ω ($I_{SET} = 1.25$ mA), and a load of 37.5 Ω (doubly terminated 75 Ω system) at each output will generate the standard EIA-343-A levels. The output voltages must be kept within the range of $+2.0$ to -2.0 volts **with respect to V_{CC2}** . If any part of the output's waveform is outside this range, its linearity will be affected.

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TABLE 1

Video Level	Output Current (mA) at:			
	VR, VB	VG	VR, VB	VG
Gray Scale	$\left(\frac{(15-A) \times I_{SET}}{1.09} \right)$	Same as VB, VR	$\left(\frac{(A) \times I_{SET}}{1.09} + 1.06 I_{SET} \right)$	$\left(\frac{(A) \times I_{SET}}{1.09} + 7.17 I_{SET} \right)$
Blank	$I_{SET} \times 14.824$	Same as VB, VR	0 mA	$I_{SET} \times 6.1$
Sync + Blank	$I_{SET} \times 14.824$	$I_{SET} \times 20.93$	0 mA	0 mA

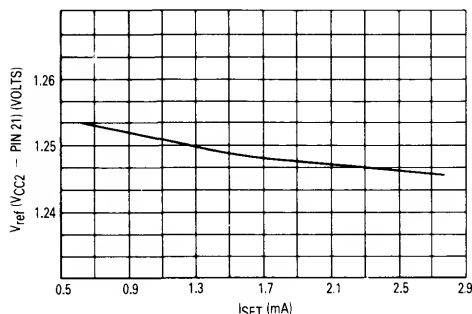
A = DAC digital input (binary value), I_{SET} is the current into Pin 21.

REFERENCE VOLTAGE (R_{SET})

The reference current for the DACs is supplied from an internal band-gap reference with a typical TC of $\approx \pm 50$ ppm/°C. The voltage at R_{SET} (Pin 21) is a constant 1.25 volts below V_{CC2} , and an external resistor R_{SET} is to be connected from V_{CC2} to Pin 21. The current I_{SET} is therefore equal to $1.25 V/R_{SET}$. Internally, equal reference currents are supplied to the three DACs such that their outputs are matched within $\pm 3.0\%$.

R_{SET} should normally be between 500 Ω and 2.0 k Ω . With values less than 500 Ω , the current at Pin 21 approaches an upper limit, resulting in a nonlinear relationship for the MC10320. With values greater than 2.0 k Ω , instability and oscillations of the reference amplifier will result. For this reason, current to Pin 21 should not be supplied from a current source. Additionally, the resistor should be noninductive (non-wirewound). Metal film resistors, available with low TCs, are recommended. The resistor should be physically adjacent to the MC10320 to avoid the inductive effects of long PC board tracks. Figure 5 indicates the voltage/current characteristics at Pin 21.

FIGURE 5 — V_{ref} versus I_{SET}



POWER SUPPLIES

The MC10320 may be used in a single or dual supply system, depending on the system logic levels, and/or the output requirements (See the Applications Section). Table 2 indicates permissible configurations. The only restriction is that the output stage (V_{CC2}/V_{EE2}) cannot be more positive than the input stage. The positive supplies may range from +4.5 to +5.5 volts, and negative supplies may range from -4.5 to -5.72 volts.

TABLE 2

System	VCC1	VEE1	VCC2	VEE2
Single Supply	+5.0 V	Gnd	+5.0 V	Gnd
Single Supply	Gnd	-5.0 V	Gnd	-5.0 V
Dual Supply	+5.0 V	Gnd	Gnd	-5.0 V

The current requirement for the input stage (I_{CC1}) is typically 50 mA, and the majority of that current (+0, -4.0 mA) flows out of V_{EE1} . The current requirement for the output stage (I_{CC2}) is typically 28 mA. Out of V_{EE2} flows that current, plus the current due to the outputs and I_{SET} . In a typical application the output currents total ≈ 63 mA, and I_{SET} is ≈ 1.25 mA, giving a total I_{EE2} of ≈ 92 mA.

The minimum voltage at V_{CC1} for memory retention is ≈ 1.5 volts.

Proper bypassing of the supplies at the IC is critical due to the high frequencies involved. Further information can be found in the Applications section.

TIMING

Timing diagrams for the Read (display) mode and the Write (RAM update) mode are shown in Figure 2.

In the READ mode, the clock may be any frequency up to 125 MHz for the MC10320, and up to 90 MHz for the MC10320-1. Duty cycle is not important as long as the minimum low and high times are observed. On each clock's rising edge, a new address is clocked in, and the previous address' information is supplied to the DACs from the look-up table. If the \overline{BLANK} line is taken to a Logic "0", it will override the information to the DACs on the next clock rising edge, and the 3 DACs will be taken to the blanking level. The SYNC input, when taken to a Logic "0", drives the Green DAC directly with only a small internal propagation delay. The output of the Green DAC will then change with respect to the last address input. For this reason, the SYNC input should normally be used only after asserting the \overline{BLANK} input.

In the WRITE mode, the clock is used only to enter the address where the new data is to be written. The P_{CLK} input may continue to toggle if the address inputs are stable during the write period, or the clock may be stopped while writing. Data is then entered into each of 3 color sections of that address by taking low the appropriate WRITE lines (\overline{WR} , \overline{WG} , \overline{WB}). If the same four bits are to be stored in different color locations of the same address, the appropriate WRITE lines may be taken low simultaneously. If the \overline{BLANK} input is held low during the Write operation, the DAC outputs will be held in a known state.

APPLICATIONS INFORMATION

POWER SUPPLIES, GROUNDING

The PC board layout, and the quality of the power supplies and the ground system **at the IC** are very important in order to obtain proper operation. Noise, from any source, coming into the device can result in an incorrect output due to interaction with the analog portion of the circuit. At the same time, noise generated within the MC10320 can cause incorrect operation if that noise does not have a clear path to ac ground.

The power supply pins at both the input and output sections of the MC10320 must be decoupled to ground **at the IC** (within 1" max) with a 10 μ F tantalum and a 0.1 μ F ceramic. Tantalum capacitors are recommended since electrolytic capacitors simply have too much inductance at the frequencies of interest. The quality of the V_{CC} and V_{EE} supplies should then be checked at the IC with a high frequency scope. Noise spikes (always present among digital circuits) can easily exceed 400 mV peak, and if they get into the analog portion of the IC, the output waveforms can be disrupted. Noise can be reduced by inserting resistors and/or inductors between the supplies and the IC.

If switching power supplies are used, there will usually be spikes of 0.5 volts or greater at frequencies of 50–200 kHz. These spikes are generally more difficult to reduce because of their greater energy content. In extreme cases, 3-terminal regulators (MC78L05ACP, MC7805CT), with appropriate high frequency filtering, should be used and dedicated to the MC10320.

The ripple content of the supplies should not allow their magnitude to exceed the values in the Recommended Operating Limits.

The PC board tracks supplying V_{CC} and V_{EE} to the MC10320 should preferably not be at the tail end of the bus distribution, after passing through a maze of digital circuitry. The MC10320 should be close to the power supply, or the connector where the supply voltages enter the board. If the V_{CC} and V_{EE} lines are supplying considerable current to other parts of the board, then it is preferable to have dedicated lines from the supply or connector directly to the MC10320.

The two V_{EE1} pins (4 and 22) **must** be connected directly together. Likewise, the two V_{EE2} pins (12 and 20) **must** be connected directly together. Any long path between them can cause stability problems due to the inductance (ω 125 MHz) of the PC tracks. The ground return for the analog signals must be noise free.

PC Board Layout

Due to the high frequencies involved, and in particular, the fast edges of the various digital signals, proper PC board layout is imperative. A solid ground plane is necessary in order to have known transmission characteristics, and also to minimize coupling of the digital signals into the analog section. **Use of wire wrapped boards should definitely be avoided.**

Each PC track should be considered a transmission line, and if they are of any considerable length (more

than a few inches), they should be terminated according to transmission line theory. Otherwise reflections back to the signal sources can occur, disrupting their operation. Additionally, the overshoots and undershoots which will occur at the MC10320's input pins can cause its operation to be disrupted, resulting in an incorrect output.

Additional information regarding the transmission characteristics of PC board tracks can be found in Motorola's MECL System Design Handbook (HB205R1).

Input Configurations

The unique configuration of the MC10320's power supply system permits its use in an all TTL, or all ECL, or mixed TTL/ECL environments, with the secondary capability of having the output levels be above or below ground. For standard TTL inputs refer to Figure 7. For systems using "above ground ECL" (ECL circuitry operated between ground and +5.0 volts, rather than -5.2 volts), refer to Figure 8. The MC10H350 translators will change the above ground ECL levels to the TTL levels required by the SYNC, Data and WRITE inputs, while the Threshold Control will set the thresholds of the Address, Clock and BLANK inputs to the ECL levels. For standard (below ground) ECL levels, refer to Figure 9. Since V_{CC2} cannot be more positive than V_{CC1} , they are both connected to ground level in this case.

In the case where all inputs are above ground, but the low speed inputs (Data, WRITE, and SYNC) are connected to TTL circuits, while the high speed inputs are connected to above ground ECL circuits, refer to Figure 10. In the case where the low speed inputs are connected to standard TTL, and the high speed inputs are connected to standard (below ground) ECL, refer to Figure 11.

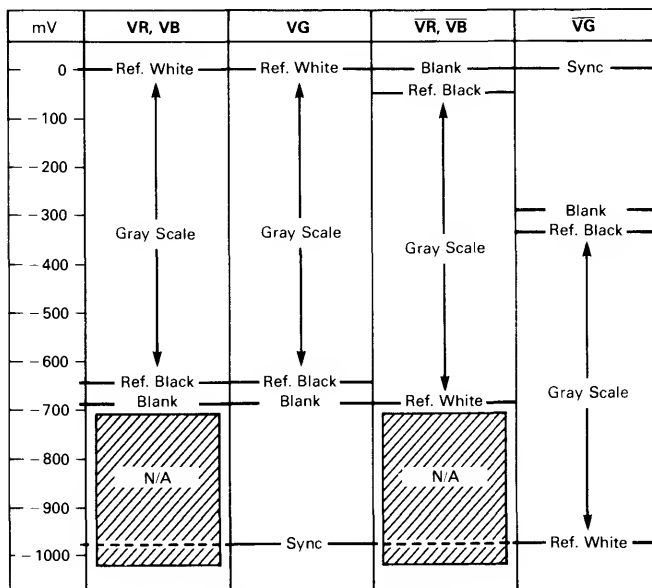
Output Configurations

The output waveforms may be above or below ground, depending on the choice of supply voltages for V_{CC2} and V_{EE2} , but the output voltages are always referenced to V_{CC2} . In Figure 12, the outputs are referenced to +5.0 V, and produce a 1.0 volt p-p waveform when used with a doubly terminated 75 Ω load, and an R_{SET} of 1.0 k Ω . The +5.0 volt supply is the "ac ground" in this case. If the outputs must be referenced to system ground rather than the +5.0 volt supply, the circuit of Figure 13 will provide the required level shifting. Figure 14 provides ground referenced outputs with a range of 0 to -1.0 volt. In Figure 15, the outputs are pulled up to a voltage different from V_{CC2} , providing an offset (+1.0 volt offset in the figure). In Figure 15 the complementary outputs should be connected to the +1.0 volt pullup voltage. The voltage at VR, VG, and VB (and the complementary outputs) must always lie within the range of ± 2.0 volts with respect to V_{CC2} .

Figure 6 illustrates the output voltage range, with respect to V_{CC2} or a pullup voltage, of the six outputs ($R_L = 37.5 \Omega$, $R_{SET} = 1.0 k\Omega$):

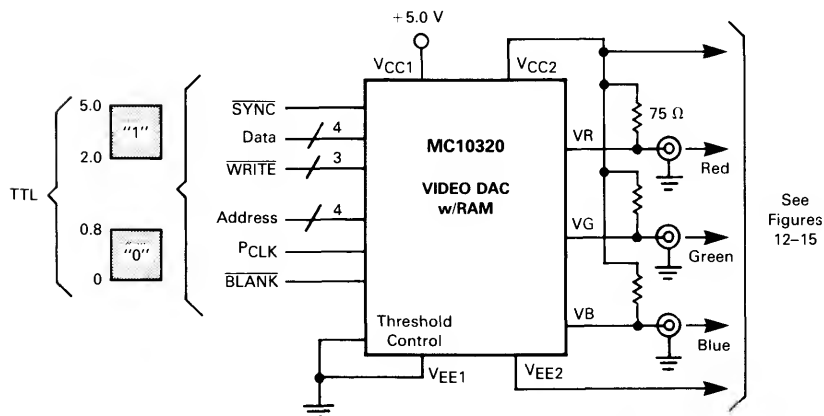
MC10320, MC10320-1

FIGURE 6 — OUTPUT LEVELS



Note: $R_{SET} = 1.0\text{ k}$, $R_L = 37.5\ \Omega$, above values are typical.

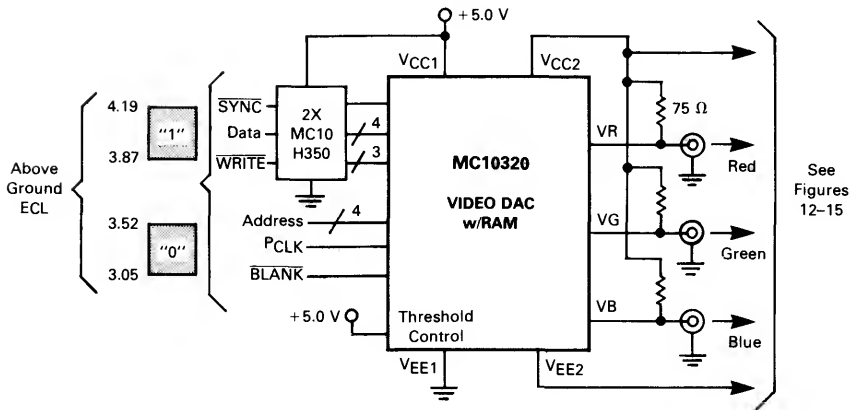
FIGURE 7 — TTL INPUTS



Note: V_{CC2} , V_{EE2} may be above or below ground.

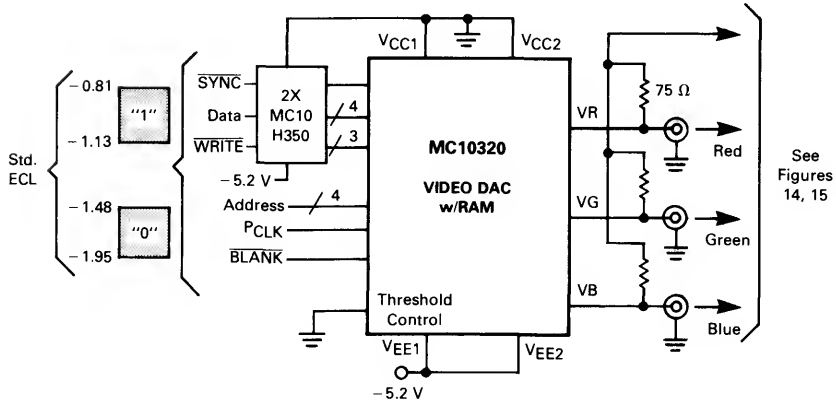
MC10320, MC10320-1

FIGURE 8 — ABOVE GROUND ECL INPUTS



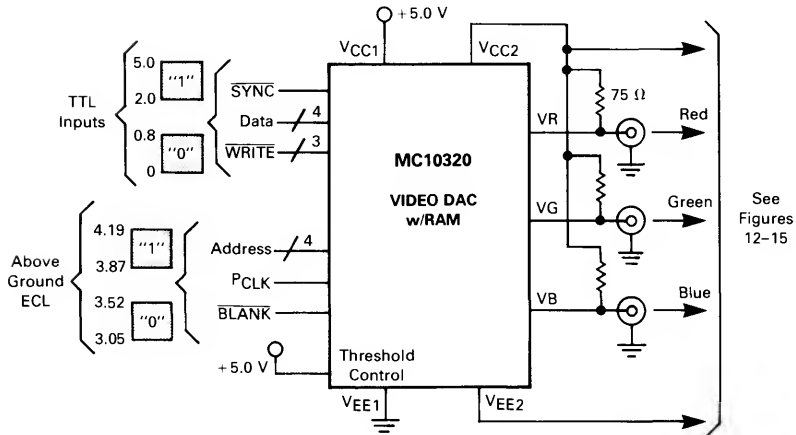
Note: V_{CC2}/V_{EE2} may be above or below ground.

FIGURE 9 — STANDARD ECL INPUTS



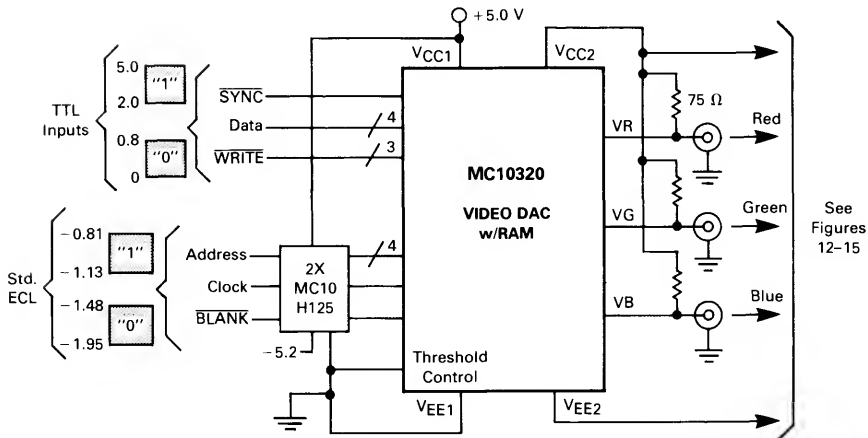
MC10320, MC10320-1

**FIGURE 10 — LOW SPEED INPUTS @ TTL,
HIGH SPEED INPUTS @ ABOVE GROUND ECL**



Note: VCC2 VEE2 may be above or below ground.

**FIGURE 11 — LOW SPEED INPUTS @ TTL,
HIGH SPEED INPUTS @ STANDARD ECL**



Note: VCC2 VEE2 may be above or below ground.

MC10320, MC10320-1

FIGURE 12 — SINGLE +5.0 VOLT SUPPLY,
OUTPUTS ABOVE GROUND

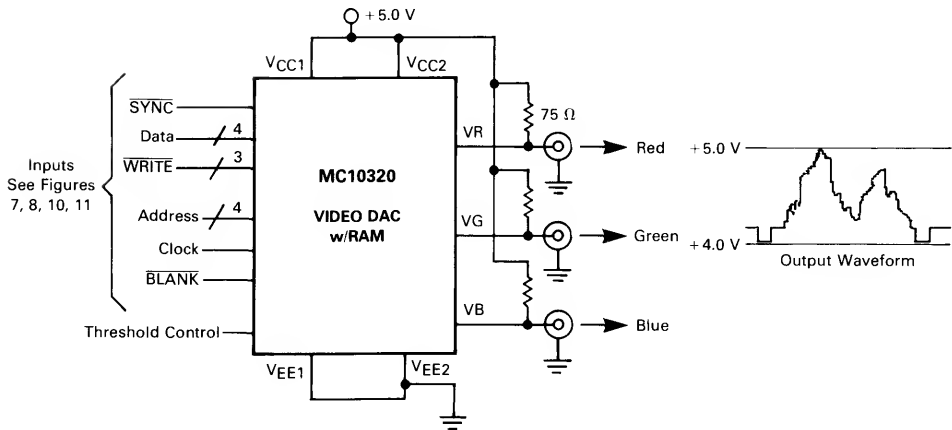
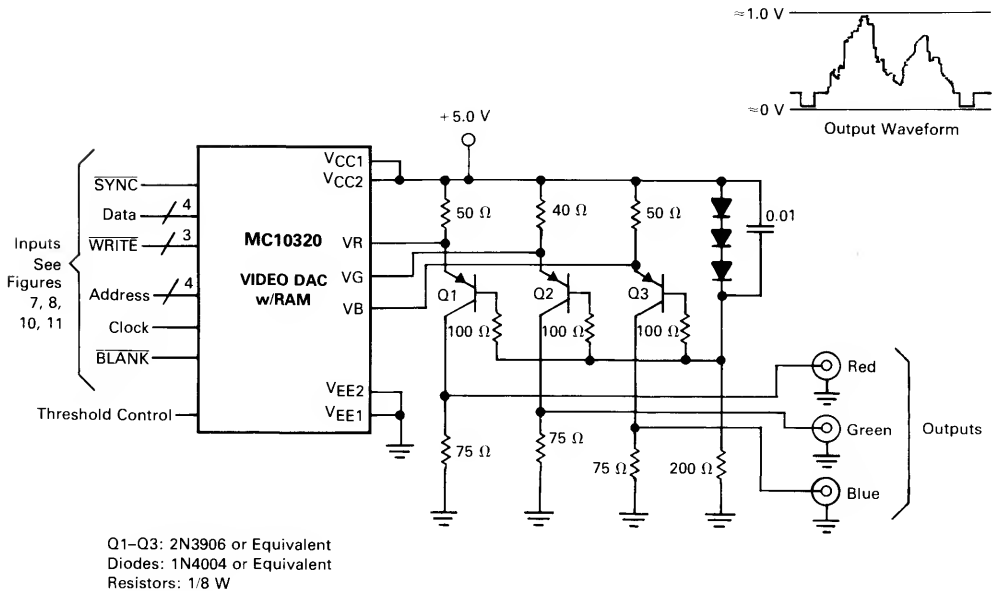


FIGURE 13 — SINGLE +5.0 VOLT SUPPLY, OUTPUTS
REFERENCED TO GROUND



MC10320, MC10320-1

FIGURE 14 — SINGLE OR DUAL SUPPLY,
OUTPUTS BELOW GROUND

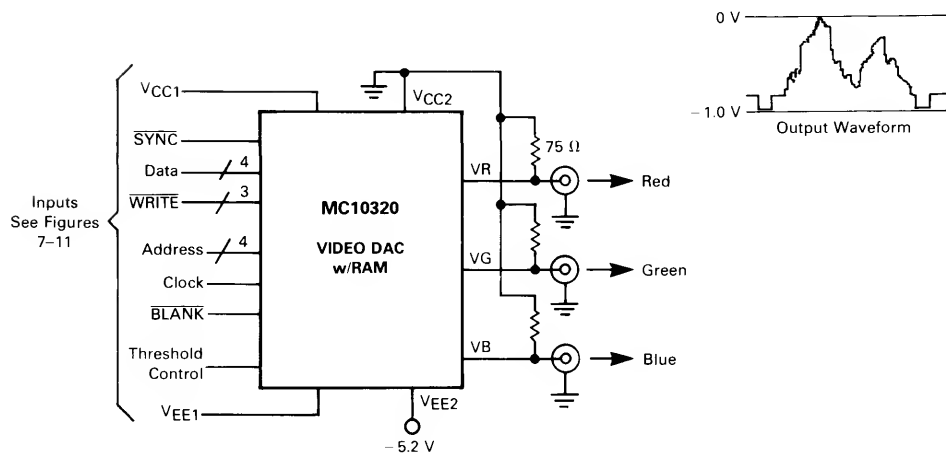
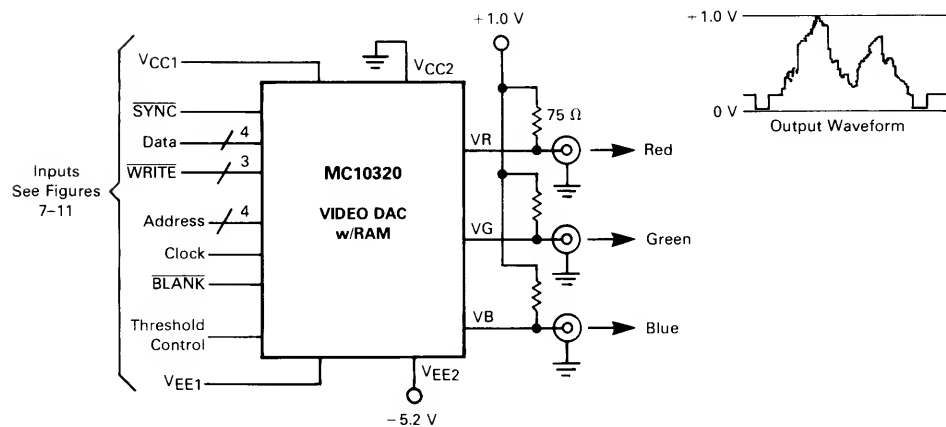


FIGURE 15 — SINGLE OR DUAL SUPPLY, OUTPUTS ABOVE
GROUND, REFERENCED TO GROUND



GLOSSARY

BANDGAP REFERENCE — A temperature stable voltage reference circuit based on the predictable base-emitter voltage of a transistor.

BIPOLAR INPUT/OUTPUT — A mode of operation whereby the analog input (of an A/D), or output (of a DAC), includes both negative and positive values. Examples are -5.0 to $+5.0$ V, -2.0 to $+8.0$ V, etc.

DAC CURRENT GAIN — The internal gain the DAC applied to the reference current to determine the full scale output current. The actual maximum current out of a DAC is one LSB less than the full scale current.

DIFFERENTIAL GAIN — In video systems, differential gain is a component's change in gain as a function of luminance level. In a color picture, saturation will be distorted if the differential gain is not zero.

DIFFERENTIAL NONLINEARITY — The maximum deviation in the actual step size (one transition level to another) from the ideal step size. The ideal step size is defined as the Full Scale Range divided by 2^n . This error must be within ± 1 LSB for proper operation.

DIFFERENTIAL PHASE — In video systems, differential phase is the change in the phase modulation of the chrominance signal as a function of the luminance level. The hue in a color picture will be distorted if the differential phase is not zero.

ECL — Emitter coupled logic.

FULL SCALE RANGE (Actual) — The difference between the actual minimum and maximum end points of the analog input (of an A/D), or output (of a DAC).

FULL SCALE RANGE (Ideal) — The difference between the actual minimum and maximum end points of the analog input (of an A/D), or output (of a DAC), plus one LSB.

GAIN ERROR — The difference between the actual and theoretical gain (end point to end point), with respect to the reference, of a data converter. The gain error is usually expressed in LSBs.

GLITCH AREA — The energy content of a glitch, specified in volt-seconds. It is the area under the curve of the glitch waveform.

GRAY CODE — Also known as **reflected binary code**, it is a digital code such that each code differs from adjacent codes by only one bit. Since more than one bit is never changed at each transition, race condition errors are eliminated.

INTEGRAL NON-LINEARITY — The maximum error of an A/D, or DAC, transfer function from the ideal straight line connecting the analog end points. This parameter is sensitive to dynamics, and test conditions must be specified in order to be meaningful. This parameter is the best overall indicator of the device's performance.

LSB — Least Significant Bit. It is the lowest order bit of a binary code.

LINE REGULATION — The ability of a voltage regulator to maintain a certain output voltage as the input to the regulator is varied. The error is typically expressed as a percent of the nominal output voltage.

LOAD REGULATION — The ability of a voltage regulator to maintain a certain output voltage as the load current is varied. The error is typically expressed as a percent of the nominal output voltage.

MONOTONICITY — The characteristic of the transfer function whereby increasing the input code (of a DAC), or the input signal (of an A/D), results in the output never decreasing. Non-monotonicity occurs if the differential non-linearity exceeds -1 LSB.

MSB — Most Significant Bit. It is the highest order bit of a binary code.

NATURAL BINARY CODE — A binary code defined by:

$$N = A_n 2^n + \dots + A_3 2^3 + A_2 2^2 + A_1 2^1 + A_0 2^0$$

where each "A" coefficient has a value of 1 or 0.

NYQUIST THEORY — See Sampling Theorem.

OFFSET BINARY CODE — Applicable only to bipolar input (or output) data converters, it is the same as Natural Binary, except that all zeroes corresponds to the most negative output voltage (of an DAC), while all ones corresponds to the most positive output.

OUTPUT COMPLIANCE — The maximum voltage range to which the DAC outputs can be subjected, and still meet all of the specifications.

POWER SUPPLY REJECTION RATIO — The ability of a device to reject noise and/or ripple on the power supply pins from appearing at the outputs. An ac measurement, this parameter is usually expressed in dB rejection.

POWER SUPPLY SENSITIVITY — The change in a data converters performance with changes in the power supply voltage(s). A dc measurement, this parameter is usually expressed in percent of full scale versus a percent change in the power supply voltage.

PROPAGATION DELAY — For a video DAC, the time from when the clock input crosses its threshold to when the DAC output(s) reach the 50% point of the transition.

QUANTITIZATION ERROR — Also known as digitization error or uncertainty. It is the inherent error involved in digitizing an analog signal due to the finite number of steps at the digital output versus the infinite number of values at the analog input. This error is a minimum of $\pm 1/2$ LSB.

RESOLUTION — The smallest change which can be discerned by an A/D converter, or produced by a DAC. It is usually expressed as the number of bits, n , where the converter has 2^n possible states.

SAMPLING THEOREM — Also known as the Nyquist Theorem. It states that the sampling frequency of an A/D must be no less than $2x$ the highest frequency (of

interest) of the analog signal to be digitized in order to preserve the information of that analog signal.

SETTLING TIME — For a video DAC, the time required for the output to change (and settle in) from an initial $\pm 1/2$ LSB error band to the final $\pm 1/2$ LSB error band.

TTL — Transistor-transistor logic.

TWO'S COMPLEMENT CODE — A binary code applicable to bipolar operation, in which the positive and negative codes of the same analog magnitude sum to all zeroes, plus a carry. It is the same as Offset Binary Code, with the MSB inverted.

UNIPOLAR INPUT — A mode of operation whereby the analog input range (of an A/D), or output range (of a DAC), includes values of a single polarity. Examples are 0 to +10 V, 0 to -5.0 V, +2.0 to +8.0 V, etc.

MC13001XP
MC13002XP

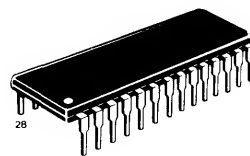
MONOMAX BLACK AND WHITE TV SUBSYSTEM

The MONOMAX is a single-chip IC that will perform the electronic functions of a monochrome TV receiver, with the exception of the tuner, sound channel, and power output stages. The MC13001XP and MC13002XP will function as drop-in replacements for MC13001P and MC13002P, but some external IF components can be removed for maximum benefit. IF AGC range has been increased, video output impedance lowered, and horizontal driver output current capability increased.

- Full Performance Monochrome Receiver with Noise and Video Processing — Black Level Clamp, DC Contrast, Beam Limiter
- Video IF Detection on Chip — No Coils, No Pins, except Inputs
- Noise Filtering on Chip — Minimum Pins and Externals
- Oscillator Components on Chip — No Precision Capacitors Required
- MC13001XP for 525 Line NTSC and MC13002XP for 625 Line CCIR
- Low Dissipation in All Circuit Sections
- High-Performance Vertical Countdown
- 2-Loop Horizontal System with Low Power Start-Up Mode
- Noise Protected Sync and Gated AGC System
- Designed to work with TDA1190P or TDA3190P Sound IF and Audio Output Devices
- Reverse RF AGC Types are Available: MC13008XP, MC13009XP

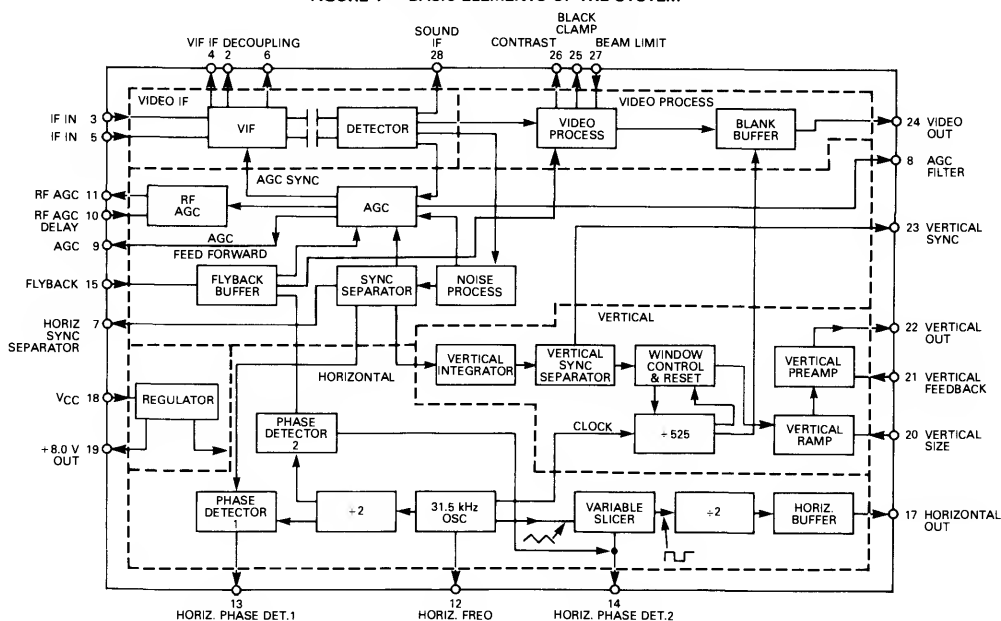
MONOMAX
BLACK AND WHITE TV
SUBSYSTEM

SILICON MONOLITHIC
INTEGRATED CIRCUITS



P SUFFIX
PLASTIC PACKAGE
CASE 710

FIGURE 1 — BASIC ELEMENTS OF THE SYSTEM



MC13001XP, MC13002XP

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage — Pin 18	V_{CC}	+16	Vdc
Power Dissipation	P_D	1.0	Watts
Horizontal Driver Current — Pin 17	I_{HOR}	-20	mA
RF AGC Current — Pin 11	I_{RFAGC}	20	mA
Video Detector Current — Pin 24	I_{VID}	5.0	mA
Vertical Driver Current — Pin 22	I_{VERT}	5.0	mA
Auxiliary Regulator Current — Pin 19	I_{REG}	35	mA
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	60	$^\circ\text{C/W}$
Maximum Junction Temperature	T_J	150	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Temperature Range	T_A	0° to +70	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Horizontal Output Drive Current	I_{HOR}	≤ 10	mA
RF AGC Current	I_{RFAGC}	≤ 10	mA
Regulator Current	I_{REG}	≤ 20	mA

ELECTRICAL CHARACTERISTICS ($V_{CC} = 11.3\text{ V}$, $T_A = 25^\circ\text{C}$)

Characteristics	Symbol	Min	Typ	Max	Unit
Power Supply Current Pins 18 & 19	I_{CC}	44	—	76	mA
Regulator Voltage Pin 19	V_{REG}	7.2	8.2	8.8	Vdc

HORIZONTAL SPECIFICATIONS

Oscillator Frequency (Nominal) Pin 12	$f_{HOR(NOM)}$	13	—	19	kHz
Oscillator Sensitivity		—	230	—	Hz/ μA
Start-Up Frequency ($I_{18} = 4.0\text{ mA}$)	f_{HOR}	-10	—	+10	%
Oscillator Temperature Stability ($0 \leq T_A \leq 75^\circ\text{C}$)	f_{HOR}	—	50	—	Hz
Phase Detector 1 (Charge/Discharge Current) (Non Standard Frame) (Standard Frame)	$I_{\phi 1}$		± 900 ± 400		μA
Phase Detector 1 (Output Voltage Limits)	$V_{\phi 1}$	—	7.5 (Max) 2.5 (Min)	—	Vdc
Phase Detector 1 (Leakage Current)		—	—	2.0	μA
Phase Detector 2 (Charge/Discharge Current)	$I_{\phi 2}$	—	+1.0 -0.6		mA
Phase Detector 2 (Output Voltage Limits)	$V_{\phi 2}$		7.7 (Max) 1.5 (Min)		Vdc
Phase Detector 2 (Leakage Current)		—	—	3.0	μA
Horizontal Delay Range (Sync to Flyback)			18 (Max) 5.0 (Min)		μs
Horizontal Output Saturation Voltage ($I_{17} = 15\text{ mA}$)	$V_{17(SAT)}$	—	—	0.3	Vdc
Phase Detector 1 (Gain Constant) (Out-of-Lock) (In-Lock)		—	5.0 10	—	$\mu\text{A}/\mu\text{s}$
Horizontal Pull-In Range		± 500	± 750		Hz

MC13001XP, MC13002XP

VERTICAL SPECIFICATIONS

Characteristics		Symbol	Min	Typ	Max	Unit
Output Current	Pin 22	I_{22}	-0.6	—	—	mA
Feedback Leakage Current	Pin 21	I_{21}	—	—	6.0	μ A
Ramp Retrace Current	Pin 20	I_{20}	500	—	900	μ A
Ramp Leakage Current	Pin 20	—	—	—	0.3	μ A
Feedback Maximum Voltage		V_{21}	—	5.1	—	Vdc

IF SPECIFICATIONS

Regulator Voltage	V_4	—	7.5	—	Vdc
Input Bias Voltage	$V_{2,6}$	—	4.2	—	Vdc
Input Resistance	R_{IN}	—	6.0	—	k Ω
Input Capacitance (V_{AGC} Pin 8 = 4.0 V)	C_{IN}	—	2.0	—	pF
Sensitivity ($V_g = 0$ V, 400 Hz 30% MOD, $V_{28} = 0.8$ V _{pp})		—	80	—	μ V _{RMS}
Bandwidth		—	75	—	MHz

VIDEO SPECIFICATIONS

Zero Carrier Voltage (See Figure 5)	Pin 28		—	7.0	—	Vdc
Output Voltage (See Figure 6) White to Back Porch	Pin 24		—	1.4	—	V
Differential Gain			—	6	—	%
Differential Phase (IRE Test Method)			—	4	—	Degrees
Contrast Bias Current	Pin 26	I_{26}	—	10	—	μ A
Contrast Control Range			—	14:1	—	
Beam Limiting Voltage	Pin 27	V_{27}	—	1.0	—	Vdc

AGC & SYNC

R.F. (Tuner) AGC Output Current ($V_{11} = 5.5$ V)	I_{11}	5.0	—	—	—	mA
AGC Delay Bias Current	I_{10}	—	-10	—	—	μ A
AGC Feedforward Current	I_9	—	1.0	—	—	mA
AGC Threshold (Sync Tip at Pin 28)	V_{28}	4.7	—	5.1	—	Vdc
Sync Separator Operating Point	V_7	—	4.2	—	—	Vdc
Sync Separator Charge Current	I_7	—	5.0	—	—	mA

FIGURE 2 — MONOMAX AGC CHARACTERISTICS

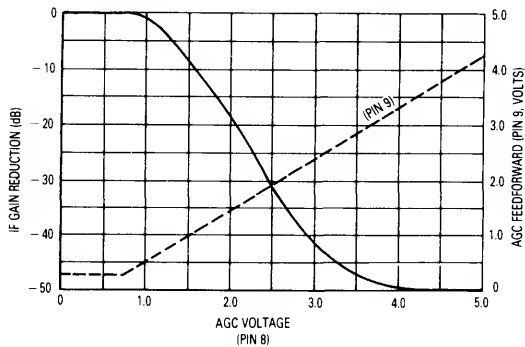
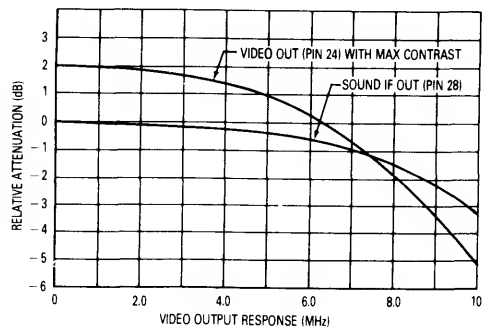
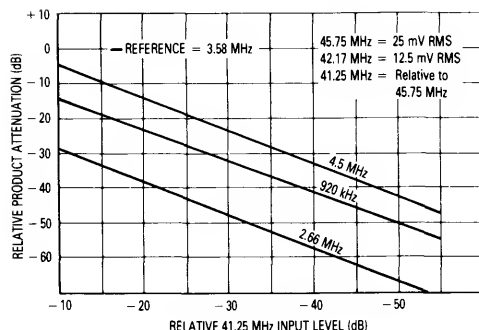


FIGURE 3 — VIDEO OUTPUT RESPONSE



MC13001XP, MC13002XP

FIGURE 4 — DETECTOR PRODUCTS



GENERAL DESCRIPTION

The Video IF Amplifier is a four-stage design with 80 μ V sensitivity. It uses a 6.2 V supply decoupled at Pin 4. The first two stages are gain controlled, and to ensure optimum noise performance, the first stage control is delayed until the second stage has been gain reduced by 15 dB. To bias the amplifier, balanced dc feedback is used which is decoupled at Pins 2 and 6 and then fed to the input Pins 3 and 5 by internal 3.9 k resistors. The nominal bias voltage at these input pins is approximately 4.2 Vdc. The input, because of the high IF gain, should be driven from a balanced differential source. For the same reason, care must be taken with the IF decoupling.

The IF output is rectified in a full wave envelope detector and detector nonlinearity is compensated by using a similar nonlinear element in a feedback output buffer amplifier. The detected 1.9 V_{p-p} video at Pin 28 contains the sound intercarrier signal, and Pin 28 is normally used as the sound takeoff point. The video frequency response, detector to Pin 28, is shown in Figure 3 and the detector intermodulation performance can be seen by reference to Figure 4. Typical Pin 28 video waveforms and voltage levels are shown in Figure 5.

The video processing section of Monomax contains a contrast control, black level clamp, a beam current

limiter and composite blanking. The video signal first passes through the contrast control. This has a range of 14:1 for a 0 V to 5.0 V change of voltage on Pin 26, which corresponds to a change of video amplitude at Pin 24 of 1.4 V to 0.1 V (black to white level). The beam current limiter operates on the contrast control, reducing the video signal when the beam current exceeds the limit set by external components. As the beam current increases, the voltage at Pin 27 moves negatively from its normal value of 1.5 V, and at 1.0 V operates the contrast control, thus initiating beam limiting action. After the contrast control, the video is passed through a buffer amplifier and dc restored by the black level clamp circuit before being fed to Pin 24 where it is blanked. The black level clamp, which is gated "on" during the second half of the flyback, maintains the video black level at 2.4 V \pm 0.1 V under all conditions, including changes in contrast, temperature and power supply. The loop integrating capacitor is at Pin 25 and is normally at a voltage of 3.3 V. The frequency response of the video at Pin 24 is shown in Figure 3 and it is blanked to within 0.5 V of ground.

The AGC loop is a gated system, and for all normal variations of the IF input signal maintains the sync tip of a noise filtered video signal at a reference voltage

FIGURE 5 — PIN 28 SOUND OUTPUT

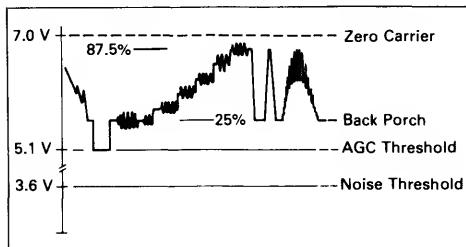
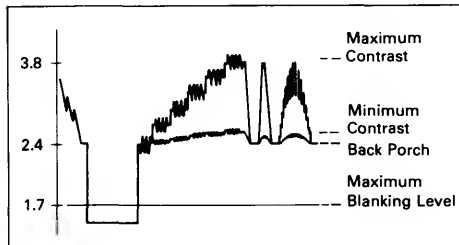


FIGURE 6 — PIN 24 — VIDEO OUTPUT



(5.1 V Pin 28). The strobe for the AGC error amplifier is formed by gating together the flyback pulse with the separated sync pulse. Integration of the error signal is performed by the capacitor at Pin 8, which forms the dominant AGC time constant. Improved noise performance is obtained by the use of a gated AGC system, noise protected by a dc coupled noise canceling circuit. The false AGC lock conditions, which can result from this combination, are prevented by an anti lockout circuit connected to the sync separator at Pin 7. AGC lockout conditions, which occur due to large rapid changes of signal level are detected at Pin 7 and recovery is ensured under these conditions by changing the AGC into a mean level system. The voltage at Pin 10 sets the point at which tuner AGC takeover occurs and positive going tuner control, suitable for an NPN RF transistor, is available at Pin 11. The maximum output is 5.5 V at 5.0 mA. A feed-forward output is provided at Pin 9. This enables the AGC control voltage to be ac coupled into the tuner takeover control at Pin 10. The coupling allows additional IF gain reduction during signal transient conditions, thus compensating for variations of AGC loop gain at the tuner AGC takeover point. In this way the AGC system stability and response are not degraded.

The previously mentioned noise protection is effected by detecting negative-going noise spikes at the video detector output. A dc coupled detector is used which turns on when a noise spike exceeds the video sync tip by 1.4 V. This pulse is then stretched and used to cancel the noise present on the delayed video at the input to the sync separator. Cancellation is performed by blanking the video to ground. Complete cancellation of the noise spike results from the stretching of the blanking pulse and the delay of the noise spike at the input to the sync separator. Protection of both the horizontal PLL and the AGC stems from the fact that both circuits use the noise cancelled sync for gating.

The composite sync is stripped from a delayed and filtered video in a peak detecting type of sync separator.

The components connected to Pin 7 determine the slice and tilt levels of the sync separator. For ideal horizontal sync separation and to ensure correct operation of AGC anti-lockup circuit, a relatively short time constant is required at Pin 7. This time constant is less than optimum for good noise free vertical separation, giving rise to a vertical slice level near sync tip. An additional, longer, time-constant is therefore coupled to the first via a diode. With the correct choice of time constants, the diode is non conducting during the horizontal sync period, but conducts during the longer vertical period. This connects the longer time constant to the sync separator for the vertical period and stops the slice level from moving up to the sync tip. The separated composite sync is integrated internally, and the time constant is such that only the longer period vertical pulses produce a significant output pulse. The output is then fed to the vertical sync separator, which further processes the vertical pulse and provides increased noise protection. The selection of the external components connected to the vertical separator at Pin 23 permits a wide range of performance options. A simple resistor divider from the 8.2 V regulated supply gives adequate performance for most conditions. The addition of an RC network will make the slice level adapt to varying sync amplitude and give improved weak signal performance. A resistor to the AGC voltage on Pin 9 enables the sync slice level to be changed as a function of signal level. This further improves the low signal level separation while at the same time giving increased impulse noise protection on strong signals.

HORIZONTAL OSCILLATOR

The horizontal PLL (see Figure 7) is a 2-loop system using a 31.5 kHz oscillator which after a divider stage is locked to the sync pulse using phase detector 1. The control signal derived from this phase detector on Pin 13 is fed via a high-value resistor to the frequency-control point on Pin 12. The same divided oscillator

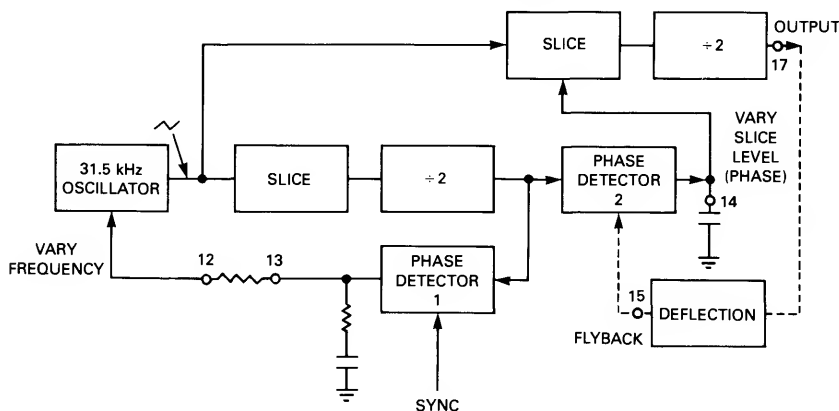


FIGURE 7 — HORIZONTAL OSCILLATOR SYSTEMS

frequency is also fed to phase detector 2, where the flyback pulse is compared with it and the resulting error used to change a variable slice level on the oscillator ramp waveform. This therefore changes the timing of the output square wave from the slicer and hence the timing of the buffered horizontal output on Pin 17 (see Figure 8). The error on phase detector 2 is reduced until the phasing of the flyback pulse is correct with respect to the divided oscillator waveform, and hence with respect to the sync pulse.

To improve the pull-in and noise characteristics of the first PLL, the phase detector current is increased when the vertical lock indicator signals an unlocked condition and is decreased when locked. This increases the loop bandwidth and pull-in range when out of lock and decreases the loop bandwidth when in lock, thus improving the noise performance. In addition, the phase detector current during the vertical period is reduced in order to minimize the disturbance to the horizontal caused by the longer period vertical phase detector pulses.

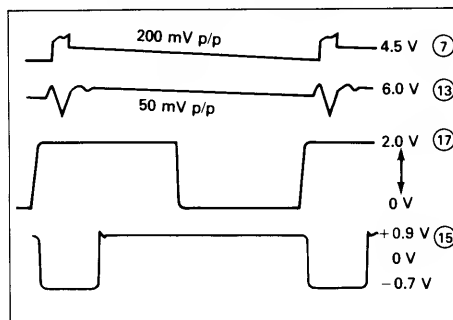
The oscillator itself is a novel design using an on-chip 50 pF silicon nitride capacitor which has a temperature drift of only 70 ppm/°C and negligible long term drift. This, in conjunction with an external resistor, gives a drift of horizontal frequency of less than 1 Hz/°C — i.e., less than 100 Hz over the full operating temperature range of the chip. The pull-in range of the PLL is about ± 750 Hz, so normally this would eliminate the need for any customer adjustment of the frequency.

The second significant feature of this design is the use of a virtual ground at the frequency control point which floats at a potential derived from a divider across the power supply and this is the same divider which determines the end-points of the oscillator ramp. The frequency adjustment which is necessary to take up tolerances in the on-chip capacitor is fed in as a current to this virtual ground and when this adjustment current is derived from an external potentiometer across the same supply there is no frequency variation with supply voltage. Moreover, using the voltage from a potentiometer for the adjustment instead of the simple variable resistor normally used in RC oscillators makes the frequency independent of the value of the potentiometer and hence its temperature coefficient. The frequency control current from the first phase detector is fed into this same virtual ground and as the sensitivity of the control is about 230 Hz/ μ A a high value resistor can be used (680 k Ω) and this can be directly connected to the phase detector filter without significant loading.

This oscillator operates with almost constant frequency to below 4.0 volts and as the total PLL system consumes less than 4.0 mA at this voltage, this gives an ideal start-up characteristic for receivers using deflection-derived power supplies.

The flyback gating input is on Pin 15 which is internally clamped to 0.7 V in both directions and requires a negative input current of 0.6 mA to operate the gate circuit. This input can be a raw flyback pulse simply fed via a suitable resistor.

FIGURE 8 — HORIZONTAL WAVEFORMS



VERTICAL SYSTEM

An output switching signal is taken from the 31.5 kHz oscillator to clock the vertical counter which is used in place of a conventional vertical oscillator circuit. The counter is reset by the vertical sync pulse but the period during which it is permitted to reset is controlled by the window control. Normally, when the counter is running synchronously, the window is narrow to give some protection against spurious noise pulses in the sync signal. If the counter output is not coincident with sync however, after a short period the window opens to give reset over a much wider count range, leading to a fast picture roll towards lock. At weak signal, i.e., less than 200 μ V IF input, the vertical system is forced to narrow mode to give a steadier picture for commonly occurring types of noise. The vertical sync, gated by the counter, then resets a ramp generator on Pin 20 and the 1.5 volt p-p ramp is buffered to Pin 22 by the vertical preamplifier. A differential input to the preamp on Pin 21 compares the signal generated across the resistor in series with the deflection coils with the generated ramp and thus controls shape and amplitude of the coil current.

The basic block diagram of the countdown system is shown in Figure 9. The 31.5 kHz (2 FH) clock from the horizontal oscillator drives a 10-stage counter circuit which is normally reset by the vertical sync pulse via the sync gate, OR gate and D flip-flop. This D input is also used to initiate discharge of the ramp capacitor and hence causes picture flyback.

The period during which sync can reset the counter and cause flyback is determined by the window control which defines a count range during which the gate is open. One of two ranges is selected according to the condition of the signal. The normal "narrow" range is 514 to 526 counts for a 525 line system and is selected after the coincidence detector indicates that the reset is coincident, twice in succession, with the 525 count from the counter. When the detector indicates non-coincidence 8 times in succession, then the window control switches to the "wide" mode (384 to 544 counts) to achieve rapid re-synchronization. For the 625 line version the counts are 614 to 626 for narrow mode and

9

The diagram illustrates a digital logic circuit for a 2FHz clock system. The main components and their interconnections are as follows:

- 10-STAGE COUNTER:** Receives a $2 F_H$ CLOCK input. It has two outputs: a "384-544" "WIDE" signal and a "514-526" "NARROW" signal. It also receives a "COUNTER RESET" signal.
- BLANKING LATCH:** Receives a "0" input and produces a "BLANKING PULSE" output.
- H/4 DELAY:** Receives the $2 F_H$ CLOCK input and outputs a "COINC." signal to the COINCIDENCE DETECTOR.
- COINCIDENCE DETECTOR:** Receives the "COINC." signal from the H/4 DELAY and the "VERTICAL SYNC" input. It outputs two "COINC." signals to the 8H/2 DELAY and 2H/2 DELAY blocks.
- 8H/2 DELAY:** Receives the "COINC." signal from the COINCIDENCE DETECTOR and outputs a signal "TO 'WIDE'" to the WINDOW CONTROL block.
- 2H/2 DELAY:** Receives the "COINC." signal from the COINCIDENCE DETECTOR and outputs a signal "TO 'NARROW'" to the WINDOW CONTROL block.
- WINDOW CONTROL:** Receives the "TO 'WIDE'" and "TO 'NARROW'" signals. It outputs a "DEFINE WINDOW FOR SYNC" signal to the SYNC GATE AND RAMP LATCH block and a signal to an AND gate.
- SYNC GATE AND RAMP LATCH:** Receives the "DEFINE WINDOW FOR SYNC" signal and the "VERTICAL SYNC" input. It outputs a signal "TO RAMP PULL-DOWN" and a signal to the AND gate.
- AND gate:** Receives signals from the WINDOW CONTROL and SYNC GATE AND RAMP LATCH blocks. Its output is labeled "D".
- D FLIP FLOP (DELAY):** Receives the "D" signal from the AND gate and the "CLOCK" input. It produces the final output signal.

The blanking output is provided from a latch which is set by the counter reset pulse and terminated by count 20 from the counter chain.

Figure 10 shows four waveforms (23, 20, 22, 21) illustrating the effect of increasing the input signal level. The waveforms are labeled with their peak-to-peak voltages: 7.0 V, 6.0 V, 2.5 V, 2.0 V, and 0 V. The vertical scale is 1V p/p, and the horizontal scale is 500 mV p/p.

The power supply regulator, although of simple design, provides two independent power supplies — one for the horizontal PLL section and the other for the remainder of the chip. The supplies share the same reference voltage but the design of the main regulator is such that it can be switched on independently to give minimum loading on the "bleed" voltage source during start-up phase of a deflection-derived supply system.

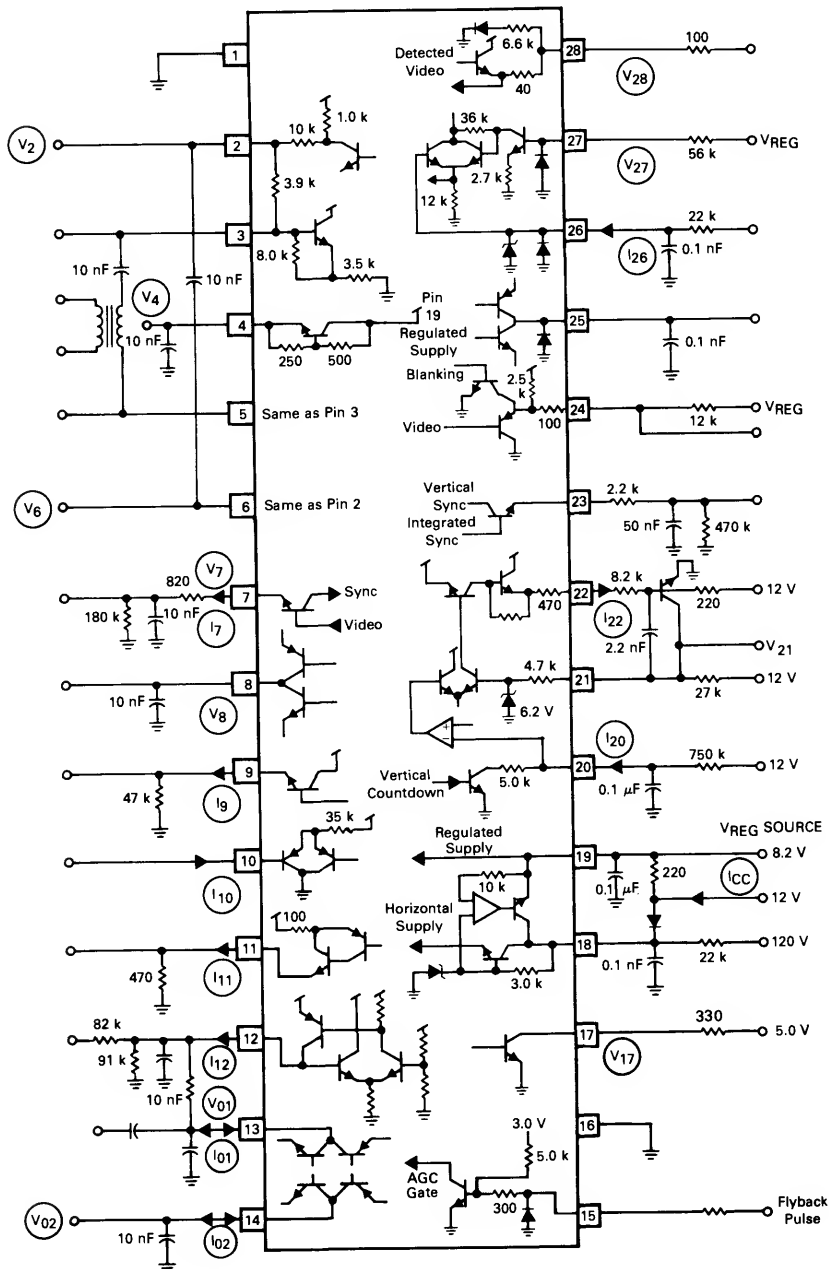
$$R_{BL} = \frac{V_{BL} - 8}{4 \times 10^{-3}}$$

12 V SUPPLY
 10k
 8.2 V TO EXTERNAL CIRCUITS
 8.2 V TO ALL MONOMAX CIRCUITS EXCEPT HORIZONTAL
 8.2 V TO HORIZONTAL SYSTEM
 HORIZONTAL START-UP BLEED
 MAIN
 I_{EXT}
 R_{BL}
 R₆
 R₁, R₂, R₃, R₄, R₅
 Q₁, Q₂, Q₃, Q₄, Q₅
 D₁, D₂
 Z₁, Z₇

I _{EXT} mA	R ₆ Ohms
<5	150
20	82
35	68

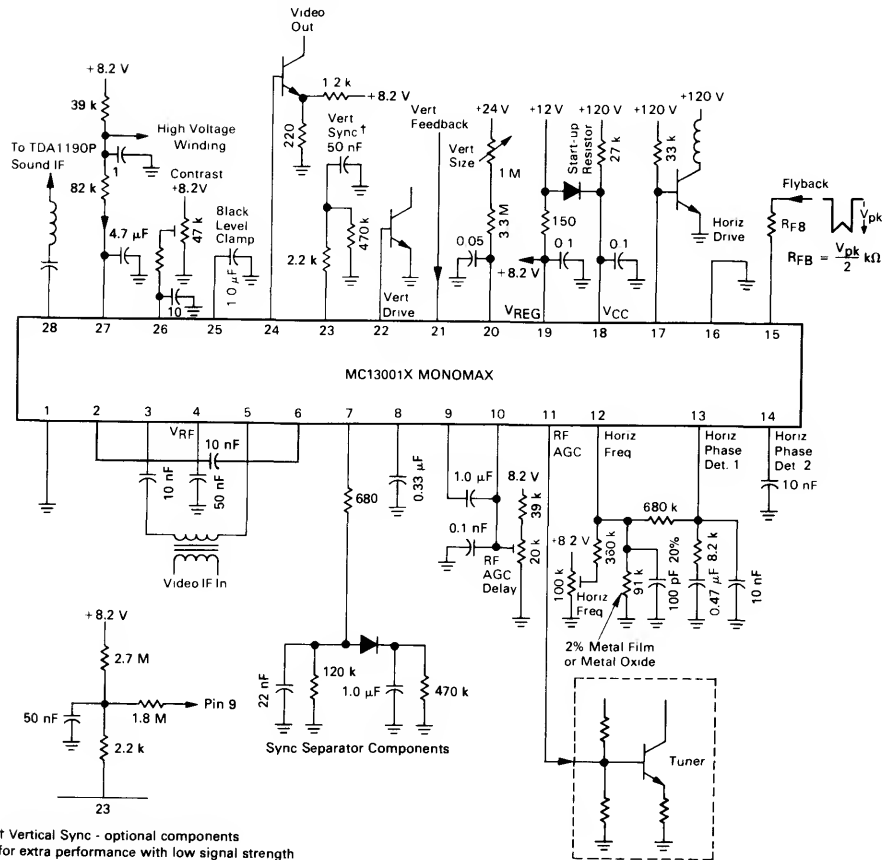
MC13001XP, MC13002XP

FIGURE 12 — TEST CIRCUIT DIAGRAM



MC13001XP, MC13002XP

FIGURE 13 — TYPICAL APPLICATION

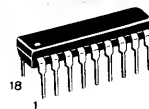


See Application Note AN879 for further information.

MC13010P

TV PARALLEL SOUND IF/AFT

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**



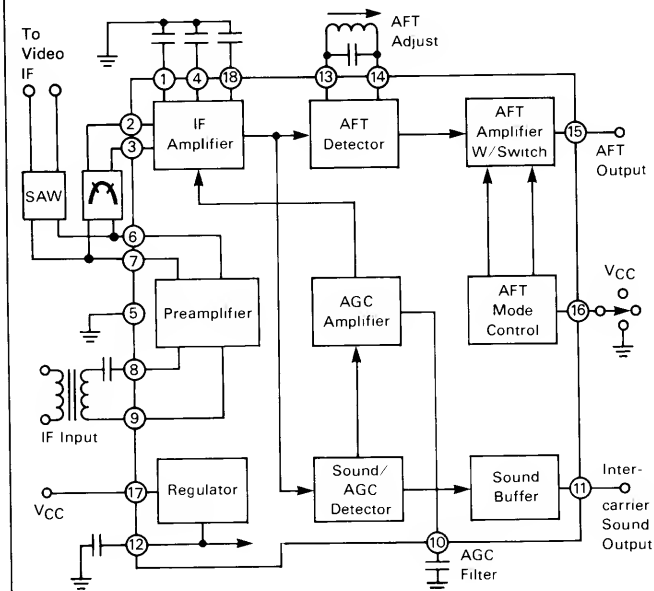
P SUFFIX
PLASTIC PACKAGE
CASE 707

TV PARALLEL SOUND IF AND AFT

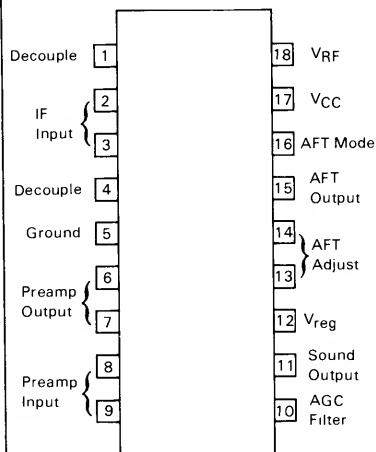
The PSIF is a single-chip IC that enhances the performance of a color TV, audio and video/chroma system. It eliminates band-pass compromises which normally tradeoff 920 kHz video beat with sound performance. The chip also includes a surface wave filter preamplifier and an AFT circuit.

- Low Noise Preamplifier for SAW Filter
- Wideband IF Amplification with Mean Level AGC
- Intercarrier Detector for Sound Carrier Output
- Reduces 920 kHz Beat
- AFT Discriminator with Output Polarity Selection
- Internal Voltage Regulator 8.2 V
- 30 mA Available from 8.2 V Internal Regulator

FIGURE 1 — BLOCK DIAGRAM



PIN CONNECTIONS



9

Rating	Symbol	Value	Unit
Power Supply Voltage	V _{CC}	16	V _{dc}
Regulator Output Current	I _{reg}	30	mA _{dc}
Thermal Resistance	R _{θJA}	70	°C/W
Power Dissipation (Package Limitation)	P _D	1.1	W
Maximum Junction Temperature	T _{J(max)}	150	°C
Storage Temperature Range	T _{stg}	− 65 to + 150	°C
Operating Temperature Range	T _A	0 to + 70	°C

Static Characteristics	Symbol	Min	Typ	Max	Unit
Supply Current	I _{CC}	30	—	60	mAdc
Regulator Voltage, Pin 12	V _{reg}	7.6	8.2	8.8	Vdc
RF Supply Voltage, Pin 18	V _{RF}	5.8	6.5	7.2	Vdc
Preamplifier Current, Pins 6, 7		4.0	6.6	7.5	mAdc

Preamp Gain (Differential Output, 50 Ω Loads)	A_v	—	− 3.0	—	dB
IF Sensitivity, Output 1.5 V_{pp} Input 45.75 MHz, 30% AM @ 1.0 kHz Differential Pins 2, 3		—	80	—	μV_{rms}
AGC Range, Input CW for Output Change of ± 0.25 Vdc		—	48	—	dB
Intercarrier Sound Output (Beat), Input 45.75 MHz, 7.0 mV_{rms} ; 41.25 MHz, 2.2 mV_{rms}		100	200	400	mV_{rms}
IF Bandwidth (3.0 dB)	f_{max}	—	80	—	MHz
Preamplifier Input Resistance	R_{in}	—	1.5	—	k Ω
Preamplifier Input Capacitance	C_{in}	—	11.5	—	pF
IF Input Resistance	R_{in}	—	2.2	—	k Ω
IF Input Capacitance	C_{in}	—	4.0	—	pF
Preamplifier Max Input Signal (Single Ended)	V_{in}	—	50	—	mV_{rms}
IF Max Input Signal (Differential)	V_{in}	—	50	—	mV_{rms}
Noise Figure IF, Max Gain		—	6.0	—	dB
Noise Figure Preamplifier		—	5.0	—	
AFT Center-Frequency Slope		—	4.0	—	$\mu A/kHz$
AFT Output Max, 1.0 MHz Detuning		—	± 300	—	μA

[illegible]

MC13010P

DESCRIPTION

The MC13010 TV Parallel Sound IF/AFT is designed to be part of a high performance color television system. Its primary function is to provide a complete separate IF amplifier for sound, leaving the normal IF to be concerned only with video. Secondary functions include an AFT detector and a SAW preamp.

In most present day color television receivers, sound and video are processed by the same IF amplifier and, in many cases, the same synchronous or pseudosynchronous detector. This imposes undesirable compromises in video and sound performance. Particularly in the U.S., the avoidance of a color/sound beat product (920 kHz) can only be achieved at the expense of sound quieting and sensitivity. Earlier solutions involved a single IF amplifier driving two detectors, with numerous interstage alignments required.

A method of solving these problems is to process the sound and video separately, directly from the tuner output. The MC13010 provides the second complete IF channel, with its own wideband detector and AGC. This permits both video IF and sound IF to be free of tuned elements, except at their inputs. (See Figure 3.)

requiring only one external filter. The general characteristic of the IF gain and gain control are given in Figure 4. The intercarrier sound output (Pin 11) is typically about 200 mV_{rms}, which easily overcomes a lossy intercarrier filter and meets the input needs of even the least sensitive FM sound IF ICs.

AFT

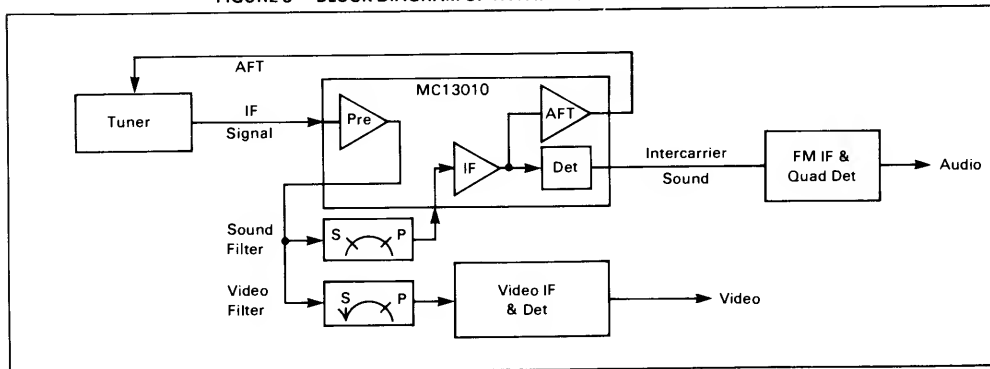
The AFT detector is a quadrature type operating at the picture IF frequency, with only one external L-C to be aligned. The polarity of the AFT output may be changed by taking the mode control (Pin 16) high or low. If the control pin is left open, the AFT is defeated.

ADDITIONAL APPLICATIONS

The MC13010 is an ideal part for stand-alone AFT. It contains the entire active system to provide a tuner with "self control". (See Figure 6.)

This device performs AM detection at the intercarrier sound output. Therefore, AM modulated digital data may be recovered. This function may be useful in cable systems where digital coding is employed.

FIGURE 3 — BLOCK DIAGRAM OF T.V. APPLICATION OF MC13010



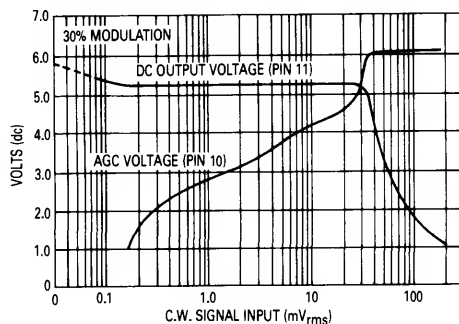
PREAMPLIFIER

The preamp is included to compensate for the high insertion loss of a Surface Acoustic Wave filter. This SAW filter may have two outputs with different responses, or it may serve only the video signal path. The preamp is optional if an LC filter is used. In any case, the selectivity ahead of the video IF must provide deep trapping of the sound carrier, while the sound bandpass is relatively broad and flat between the picture and sound carriers.

THE SOUND IF

The overall gain of 80 dB and gain control range of 48 dB equals the video IF's of earlier designs. This allows the full improvement of the system architecture to be realized. The AGC in the MC13010 is a peak-detecting type, driven internally from the sound detector, and re-

FIGURE 4 — GAIN AND AGC CHARACTERISTICS

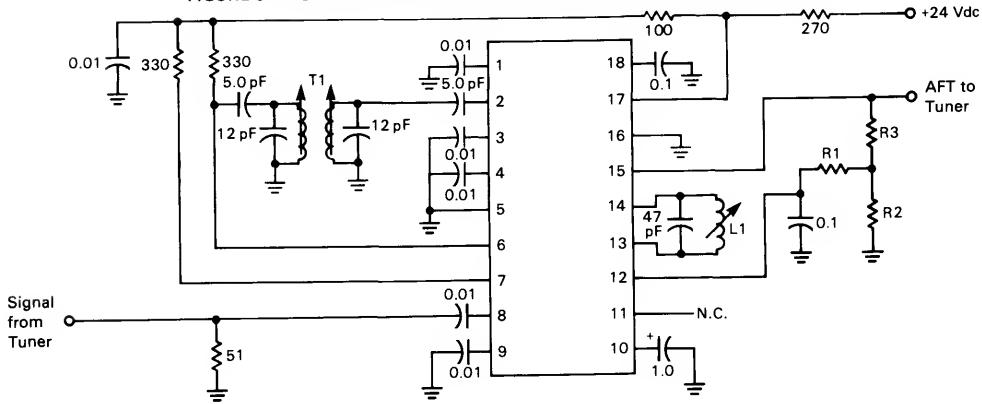


9

Experimental values for 45 MHz IF:

- T2 — Video IF Surface Acoustic Wave (SAW)
Filter: muRata, SAF 45MC02Z
- T3 — Ceramic Intercarrier Output Filter: muRata SFE
4.5 MB
- T4 — TOKO KANAS-K7060EK
- L1 — TOKO E502LN-4000034 J.W. Miller 48A147MPC
with shield case, tuned to 45.75, $L \approx 0.12 \mu\text{H}$.
- L2 — Same part as L1, except tuned to 44 MHz and
loaded with 270Ω
- R1 and R2 — Adjust for nominal tuning voltage
- R3 — Chosen for tuning voltage swing required. Note
that Pin 15 can source or sink $300 \mu\text{A}$ (typ) at the
extremes of control range

FIGURE 6 — "STAND-ALONE" AUTOMATIC FINE TUNING (AFT) APPLICATION

**Channel 3 Component Values**

T1 — Made from two coils positioned side by side, without shields, on 0.38" centers. Coils are COILCRAFT part no. T7-142 (violet 7-1/2 turns), each with its own slug, Carbonal E, adjusted to 63 MHz ($\approx 0.4 \mu\text{H}$). This should give a slightly overcoupled response. A shield to surround the coils may be required.

L1 — COILCRAFT UNI-7/150 (blue 6-1/2 turns) or UNI-10/144 (green 5-1/2 turns) shielded, adjusted to 61.25 MHz ($\approx 0.14 \mu\text{H}$)

R1 and R2 — Adjust for nominal tuning voltage

R3 — Chosen for tuning voltage swing required. Note that Pin 15 can source or sink 300 μA (typ) at the extremes of control range

MC13020P

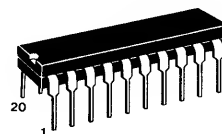
MOTOROLA C-QUAM® AM STEREO DECODER

This circuit is a complete one chip, full feature AM stereo decoding and pilot detection system. It employs full-wave envelope signal detection at all times for the L + R signal, and decodes L - R signals only in the presence of valid stereo transmission.

- No Adjustments, No Coils
- Few Peripheral Components
- True Full Wave Envelope Detection for L + R
- PLL Detection For L - R
- 25 Hz Pilot Presence Required To Receive L - R
- Pilot Acquisition Time 300 ms For Strong Signals, Time Extended For Noise Conditions To Prevent "Falsing"
- Internal Level Detector Can Be Used As AGC Source

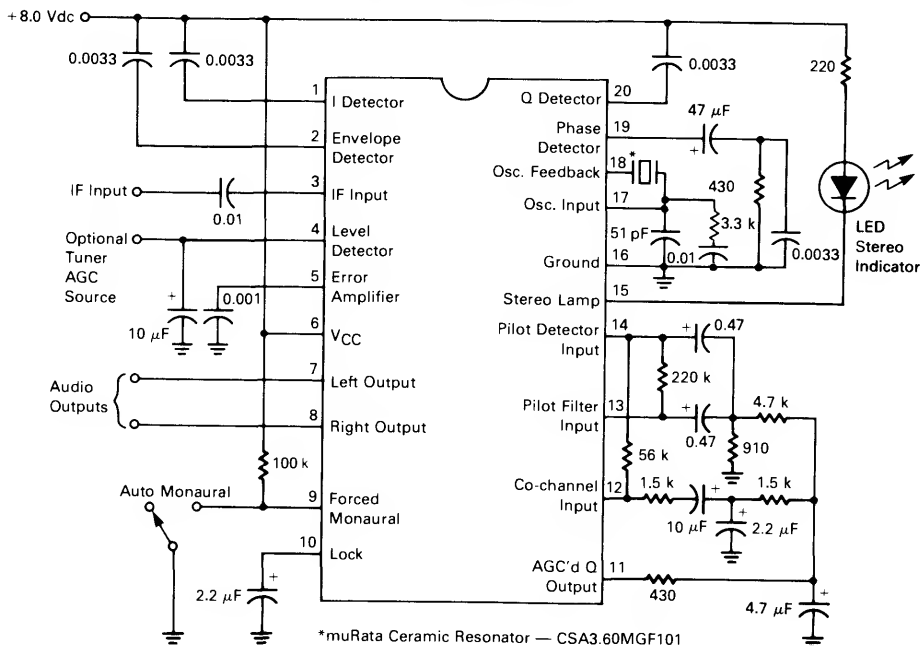
MOTOROLA C-QUAM® AM STEREO DECODER

SILICON MONOLITHIC
INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 738

FIGURE 1 — TYPICAL APPLICATION



*muRata Ceramic Resonator — CSA3.60MGF101

The purchase of the Motorola C-QUAM® AM Stereo Decoder does not carry with such purchase any license by implication, estoppel or otherwise, under any patent rights of Motorola or others covering any combination of this decoder with other elements including use in a radio receiver. Upon application by an interested party, licenses are available from Motorola on its patents applicable to AM Stereo radio receivers.

MC13020P

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	14	Vdc
Pilot Lamp Current, Pin 15		50	mAdc
Operating Temperature	T_A	-40 to +85	°C
Storage Temperature	T_{stg}	-65 to +150	°C
Junction Temperature	$T_{J(max)}$	150	°C
Power Dissipation	P_D	1.25	W
Derate above 25°C		10	mW/°C

ELECTRICAL CHARACTERISTICS ($V_{CC} = 8.0$ Vdc, $T_A = 25^\circ\text{C}$, Input Signal = 200 mVRMS. Unmodulated carrier, circuit of Figure 1, unless otherwise noted.)

Characteristic	Min	Typ	Max	Unit
Supply Line Current Drain, Pin 6	20	30	40	mAdc
Input Signal Level, Unmodulated, Pin 3, for Full Operation	100	200	357	mVRMS
Audio Output Level, 50% Modulation, L only or R only	160	220	280	mVRMS
Audio Output Level, 50% Modulation, Monaural	80	110	140	mVRMS
Channel Balance, 50% Modulation, Monaural	—	—	± 1.0	dB
Output THD, 50% Modulation	—	—	0.5	%
Output THD, 90% Modulation	—	—	1.0	%
Channel Separation, L only or R only, 50% Modulation	23	30	—	dB
Input Impedance	R_{in} C_{in}	20 6.0	—	k Ω pF
Output Impedance	—	100	150	Ω
Pilot Acquisition Time, VCO locked, after release of forced monaural	—	280	300	ms
Pilot Acquisition Time, Bad Signal Condition	1.48	—	—	sec
Lock Detector Filter Voltage, Pin 10	In Lock Out of Lock	7.7 0.8	8.0 1.0	Vdc
Force to Monaural, Pin 9, Pull Down for Monaural Mode	2.0 —	2.5 0.15	— 1.0	Vdc μA
Force to Monaural, Pin 9, Pull Up for Automatic Mode	— —	3.5 <0.001	3.7 1.0	Vdc μA

FIGURE 2 — BASIC QUADRATURE AM (QUAM)

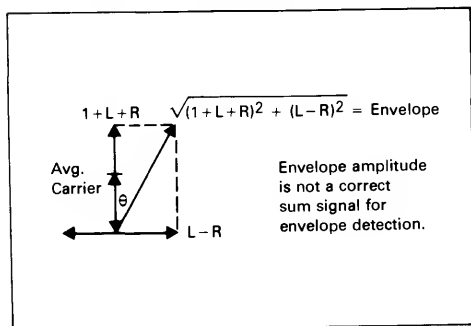
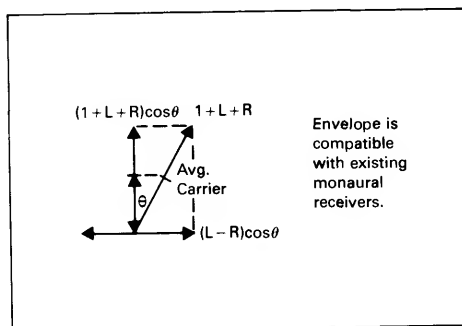


FIGURE 3 — MOTOROLA C-QUAM®



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[illegible]

INTRODUCTION

chronously detected by conventional means. The I and Q detectors are held at 0° and 90° relative demodulation angles by reference signals from the phase-locked, divided-down VCO. The output of the I DET is $1 + L + R$, with the added benefit (over the Env DET) of being able to produce a negative output on strong co-channel or noise interference. This is used to tell the Lock circuit to go to monaural operation. The output of the Q DET is the $L - R$ and pilot information.

THE DECODER

THE VCO

The MC13020P decodes the stereo information by first converting the C-QUAM® signal to QUAM, and then detecting QUAM. The conversion is accomplished by comparing the output of the Env DET and the I DET in the Err AMP. This provides the $1/\cos\theta$ correction factor, which is then multiplied by the C-QUAM® incoming signal in the Var Gain block. Thus, the output of the Var Gain block is a QUAM signal, which can then be syn-

The VCO operates at 8 times the IF input frequency, which ensures that it is out-of-band, even when a 260 kHz IF frequency is used. Typically a 450 kHz IF frequency is used with synthesized front ends. This places the VCO at 3.6 MHz, which permits economic crystal and ceramic resonators. A crystal VCO is very stable, but cannot be pulled very far to follow front-end mistuning. Pull-in capability of ± 100 kHz at 450 kHz is typical, and de-Q-ing with a resistor (see Figure 7) can increase the range only slightly. Therefore, the crystal approach can only be used with very accurate, stable front-ends. By comparison, ceramic and L-C VCO circuits offer pull-in range in the order of ± 2.5 kHz (at 450 kHz). Ceramic devices accurate enough to avoid trimming adjustment can be obtained with a matched capacitor for Cs (see Figures 1 and 5).

In the PLL filter circuit on Pin 19, C1 is the primary factor in setting a loop corner frequency of 8–10 Hz, in-lock. An internally controlled fast pull-in is provided. R2 is selected to slightly overdamp the control loop, and C2 prevents high frequency instability.

The Level DET block senses carrier level and provides an optional tuner AGC source. It also operates on the Q AGC block to provide a constant amplitude of 25 Hz pilot at Pin 11, and it delivers information to the pilot decoder regarding signal strength.

PILOT AND CO-CHANNEL FILTERS

The Q AGC output drives a low pass filter, made up of 400 Ω internal, and 430 Ω and 5 μ F external. From this point, an active 25 Hz band-pass filter is coupled to the Pilot Decoder, Pin 14, and another low-pass filter is connected to the Co-channel Input, Pin 12. A 2:1 reduction of 25 Hz pilot level to the Pilot Decode circuit will cause the system to go monaural, with the components shown. Refer to Figure 8 for the formulas governing the active band-pass filter. The co-channel input signal contains any low frequency intercarrier beat notes, and, at the selected level, prevents the Pilot Decode circuit from going into stereo. The co-channel input, Pin 12, gain can be adjusted by changing the external 1.5 k resistor. The values shown set the "trip" level at about 7% modulation. The 25 Hz pilot signal at the output of the active filter is opposite in phase to the pilot signal coming from the second low-pass filter. The 56 k resistor from Pin 14 to Pin 12 causes the pilot to be cancelled at the co-channel input. This allows a more sensitive setting of the co-channel trip level.

THE PILOT DECODER

The Pilot Decoder has two modes of operation. When signal conditions are good, the decoder will switch to stereo after 7 consecutive cycles of the 25 Hz pilot tone. When signal conditions are bad, the detected interference changes the pilot counter so as to require 37 consecutive cycles of pilot to go to stereo. In a frequency synthesized radio, the logic that mutes the audio when tuning can be connected to Pin 9. When this pin is held low it holds the decoder in monaural mode and switches it to the short count. This pin should be held low until the synthesizer and decoder have both locked onto a new station. A 300 ms delay should be sufficient. If the synthesizer logic does not provide sufficient delay, the circuit shown in Figure 9 may be added. Once Pin 9 goes high, the Pilot Decoder starts counting. If no pilot is detected for seven consecutive counts, it is assumed to be a good monaural station and the decoder is switched to the long count. This reduces the possibility of false stereo triggering due to signal level fluctuation or noise. If the PLL goes out of lock, or interference is detected by the co-channel protection circuit before seven cycles are counted, the decoder goes into the long count mode. Each disturbance will reset the counter to zero. The Level Detector will keep the decoder from going into stereo if the IF input level drops 10 dB, but will not change the operation of the pilot counter.

Once the decoder has gone into the stereo mode, it will go instantly back to monaural if either the lock detector on Pin 10 goes low, or if the carrier level drops

below the preset threshold. Seven consecutive counts of no pilot will also put the decoder in monaural. In stereo, the co-channel input is disabled, and co-channel or other noise is detected by negative excursions of the I DET, as mentioned earlier. When these excursions reach a level caused by approximately 20% modulation of co-channel, the lock detector puts the system in monaural, even though the PLL may still actually be locked. This higher level of co-channel tolerance provides the hysteresis to prevent chattering in and out of stereo on a marginal signal.

When all inputs to the Pilot Decode block are correct, and it has completed its count, it turns on the Switch, sending the L–R to the Matrix, and switches the pilot lamp pin to a low impedance to ground.

SUMMARY

It should be noted that in C-QUAM®, with both channels AM modulated, the noise increase in stereo is a maximum of 3.0 dB, less on program material. Therefore, this is not the major concern in the choice of monaural to stereo switching point as it was in FM, and blend is not needed.

PIN DESCRIPTIONS

- Pin 1, 2 — Detector Filters, $R_{out} = 4.3$ k, recommend 0.0033 μ F to V_{CC} to filter 450 kHz components.
- Pin 3 — IF Signal Input
- Pin 4 — Level Detector filter pin, $R_{out} = 8.2$ k, 10 μ F to ground sets the AGC time constant. High impedance output, needs buffer.
- Pin 5 — Error Amp compensation to stabilize the Var Gain feedback loop
- Pin 6 — V_{CC} , 6–10 Vdc, suitable for low V_{batt} automotive operation, but must be protected from "high line" condition.
- Pin 7, 8 — Left and Right Outputs, NPN emitter followers
- Pin 9 — Forced Monaural, MOS or TTL controllable
- Pin 10 — Lock detector filter, $R_{out} = 27$ k, recommend 2.2 μ F to ground.
- Pin 11 — AGC'd Q output, NPN emitter follower with 400 Ω from emitter to Pin 11
- Pin 12 — Co-channel Input, 2.0 k series in and 47 k feedback
- Pin 13 — Pilot Filter Input to op amp, see Figure 8
- Pin 14 — Pilot Decode Input (op amp output) emitter follower, $R_{out} = 100$ Ω
- Pin 15 — Stereo Lamp, open-collector of an NPN common emitter stage, can sink 50 mA, $V_{sat} = 0.3$ V at 5.0 mA
- Pin 16 — Ground
- Pin 17 — Oscillator input, $R_{in} = 10$ k, do not dc connect to Pin 18 or ground
- Pin 18 — Oscillator feedback, NPN emitter, $R_{out} = 100$ Ω
- Pin 19 — Phase Detector Output, current source to filter
- Pin 20 — Detector Filter, $R_{out} = 4.3$ k, recommend 0.0033 μ F to V_{CC} to filter 450 kHz

FIGURE 5 — CERAMIC VCO

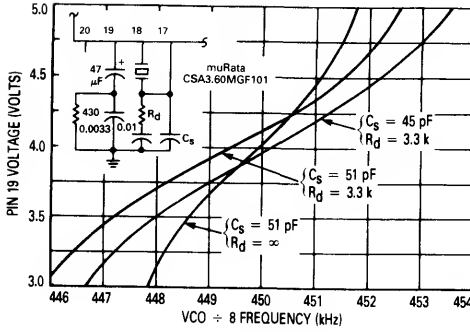


FIGURE 6 — L-C VCO

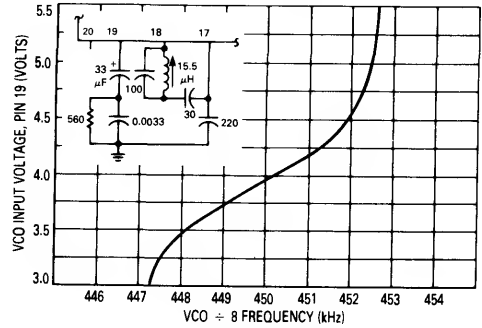


FIGURE 7 — CRYSTAL VCO

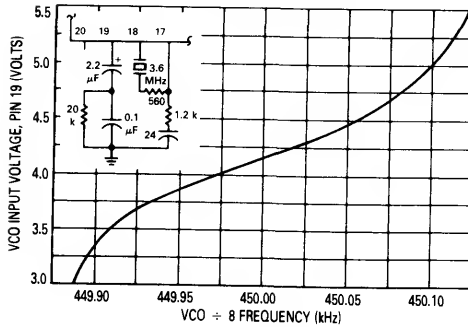


FIGURE 9 — FORCED MONAURAL
OPTIONAL DELAY CIRCUIT

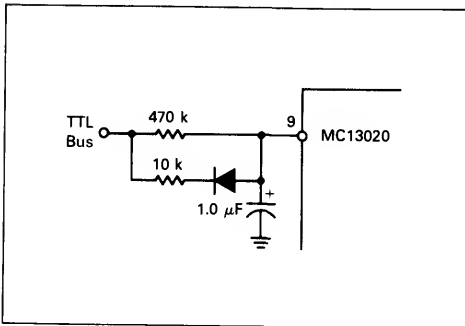
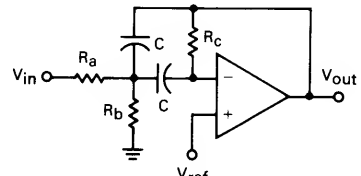


FIGURE 8 — ACTIVE BAND-PASS FILTER



$$R_C = \frac{Q}{\pi f_o C}$$

$$R_A = \frac{R_C}{2 A_o}$$

$$R_B = \frac{R_A R_C}{4Q^2 R_A - R_C}$$

where, in this application:
 f_o = center frequency = 25 Hz
 A_o = gain at $f_o \leq 25$
 $Q \leq 10$

Choose values for f_o , A_o , Q , and convenient C , solve for resistors

$C \pm 5\%$	$R_A \pm 5\%$	$R_B \pm 1\%$	$R_C \pm 1\%$
0.47 μF	4.7 k	910	220 k
0.33 μF	8.2 k	1.3 k	330 k

Note: Capacitor C should be a good grade, low ESR.

MC13022

Advance Information

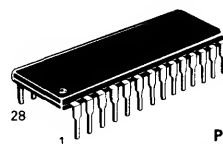
ADVANCED, MEDIUM VOLTAGE AM STEREO DECODER

The MC13022 is designed for home, portable, and automotive AM stereo radio applications. The circuits and functions included in the design allow implementation of a full-featured C-QUAM® AM stereo radio with relatively few, inexpensive external parts. It is available in either 28-lead DIP or EIAJ compatible wide-bodied 28-lead SOIC.

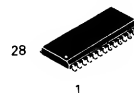
- Operation from 4.0 V to 10 V Supply with Current Drain of 18 mA Typ
- IF Amplifier with Two Speed AGC
- Post Detection Filters with 10 kHz Notch that Allow User or Automatic Adjustable Audio Bandwidth Control
- Signal Quality Controlled Stereo Blend and Noise Reduction
- Noise and Co-Channel Discriminating Stop-On-Station
- Signal Strength Indicator Output for RF AGC and/or Meter Drive
- Signal Strength Controlled IF Bandwidth
- Noise Immune Pilot Detector Needs no Precision Filter Components
- MC13023 Complementary Tuning System IC

C-QUAM® ADVANCED, MEDIUM VOLTAGE AM STEREO DECODER

SILICON MONOLITHIC
INTEGRATED CIRCUIT

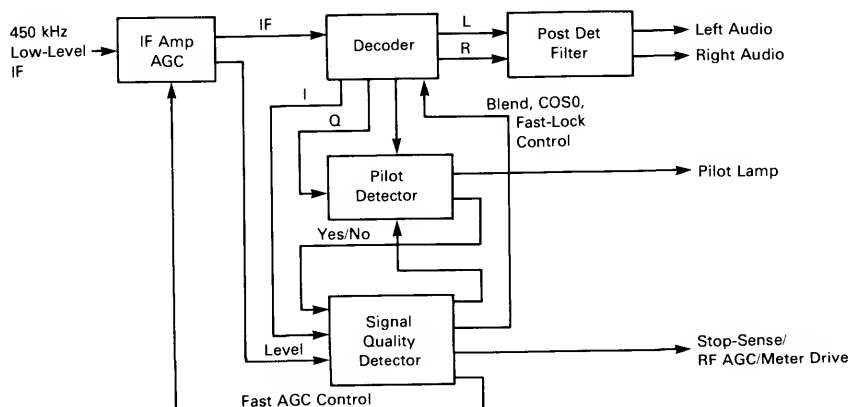


P SUFFIX
PLASTIC PACKAGE
CASE 710



DW SUFFIX
PLASTIC PACKAGE
CASE 751F
(SO-28L)

FIGURE 1 — BASIC ELEMENTS OF THE SYSTEM



The purchase of the Motorola C-QUAM® AM Stereo Decoder does not carry with such purchase any license by implication, estoppel or otherwise, under any patent rights of Motorola or others covering any combination of this decoder with other elements including use in a radio receiver. Upon application by an interested party, licenses are available from Motorola on its patents applicable to AM Stereo radio receivers.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MC13022

MAXIMUM RATING

Rating	Symbol	Value	Unit
Supply Voltage	V _{CC}	12	Vdc
Stereo Indicator Lamp Current, Pin 21		30	mAdc
Operating Temperature	T _A	- 40 to + 85	°C
Storage Temperature	T _{stg}	- 65 to + 150	°C
Junction Temperature	T _{J(max)}	150	°C
Power Dissipation Derate above 25°C	P _D	1.25 10	W mW/°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 8.0 V, T_A = 25°C)

Characteristic	Min	Typ	Max	Unit
Power Supply Operating Range	4.0	8.0	10	Vdc
Supply Line Current Drain, Pin 25	11	16	22	mAdc
Minimum Input Signal Level, Unmodulated, Pin 5, for Full Operation	—	5.0	—	mVrms
Audio Output Level, 50% Modulation, L only or R only	Stereo 100	140	180	mVrms
Audio Output Level, 50% Modulation	Monaural 50	70	90	mVrms
Output THD, 50% Modulation	Monaural Stereo —	0.3 0.5	0.5 2.0	%
Channel Separation, L only or R only, 50% Modulation	Stereo 22	35	—	dB
Pilot Acquisition Time Following BLEND Reset to 0.3 Vdc	—	—	600	mSec
Audio Output Impedance at 1.0 kHz, Pin 7, 14	—	300	—	Ohms
Stereo Indicator Lamp Pin Saturation Voltage at 3.0 mA Load Current — VSAT Pin 21	—	—	200	mVdc
Stereo Indicator Lamp Pin Leakage Current Pin 21	—	—	1.0	μAdc
Notch Filter Control Pin 15 Response versus Voltage	(See Figure 3)			

EXPLANATION OF FEATURES

BLEND AND NOISE REDUCTION

Although AM stereo does not have the extreme difference in S/N between mono and stereo that FM does (typically less than 3.0 dB versus greater than 20 dB for FM), sudden switching between mono and stereo is quite apparent. Some forms of interference such as co-channel have a large L - R component that makes them more annoying than would ordinarily be expected for the measured level. The MC13022 measures the interference level and reduces L - R as interference increases, blending smoothly to mono. The pilot indicator remains on as long as a pilot signal is detected, even when interference is severe, to minimize annoying pilot light flickering.

RF AGC/METER DRIVE

A dc voltage proportional to the log of signal strength is provided at Pin 6. This can be used for RF AGC, signal strength indication, and/or control of the post detection filter. Normal operation is above 2.2 V as shown in Figure 4.

STOP SENSE

Multiplexed with the signal strength information is the stop sense signal. The stop sense is activated when scanning by externally pulling the blend capacitor on Pin 23 below 0.5 V. This would typically be done from the mute line in a frequency synthesizer.

If at any time Pin 23 is low and there is either no signal in the IF or a noisy signal of a predetermined interfer-

ence level, Pin 6 will go low. This low can be used to tell the frequency synthesizer to immediately scan to the next channel. The interference detection prevents stopping on many unlistenable stations, a feature particularly useful at night when many frequencies may have strong signals from multiple co-channel stations.

IF BANDWIDTH CONTROL

IF AGC attenuates the signal by shunting the signal at the IF input. This widens the IF bandwidth by decreasing the loaded Q of the input coupling coil as signal strength increases.

POST DETECTION FILTERING

With weak, noisy signals, high frequency rolloff greatly improves the sound. Conventional tone controls do not attenuate the highs sufficiently to control noise without also significantly affecting the mid-range. Also, notch filters are necessary with any wide-band AM radio to eliminate the 10 kHz whistle from adjacent stations.

By using a twin-T filter with variable feedback to the normally grounded center leg, a variable Q notch filter is formed that provides both the 10 kHz notch and variable high frequency rolloff functions. Typical range of response is shown in Figure 3. Response is controlled by the dc voltage on Pin 15.

Pin 15 could interface with a dc operated tone control such as the TDA1524, or could be tied to Pin 6 for automatic audio bandwidth control as a function of signal strength.

MC13022

FIGURE 2 — TEST CIRCUIT

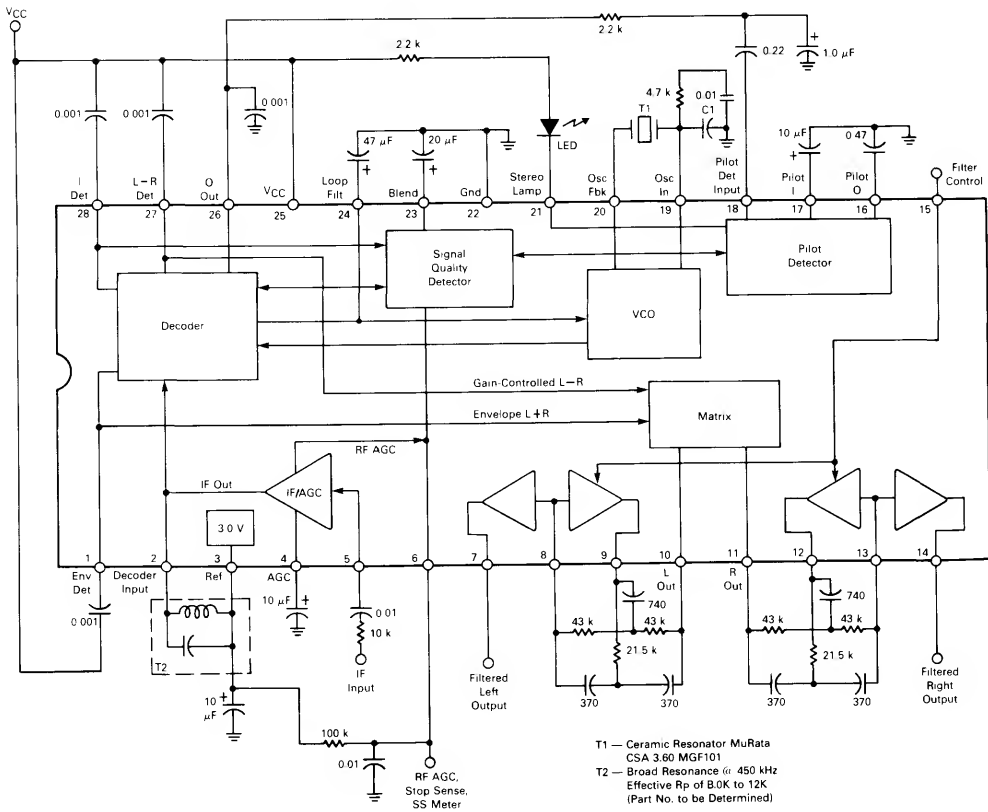


FIGURE 3 — OVERALL SELECTIVITY OF A TYPICAL RECEIVER versus FILTER CONTROL VOLTAGE

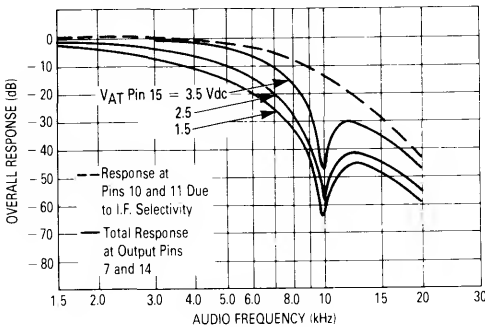
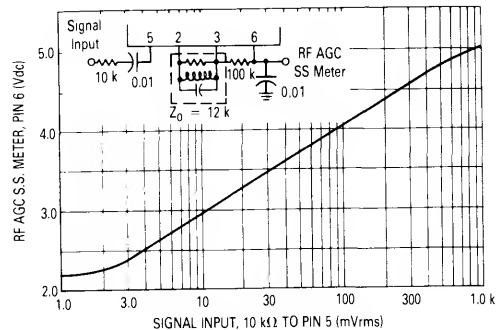
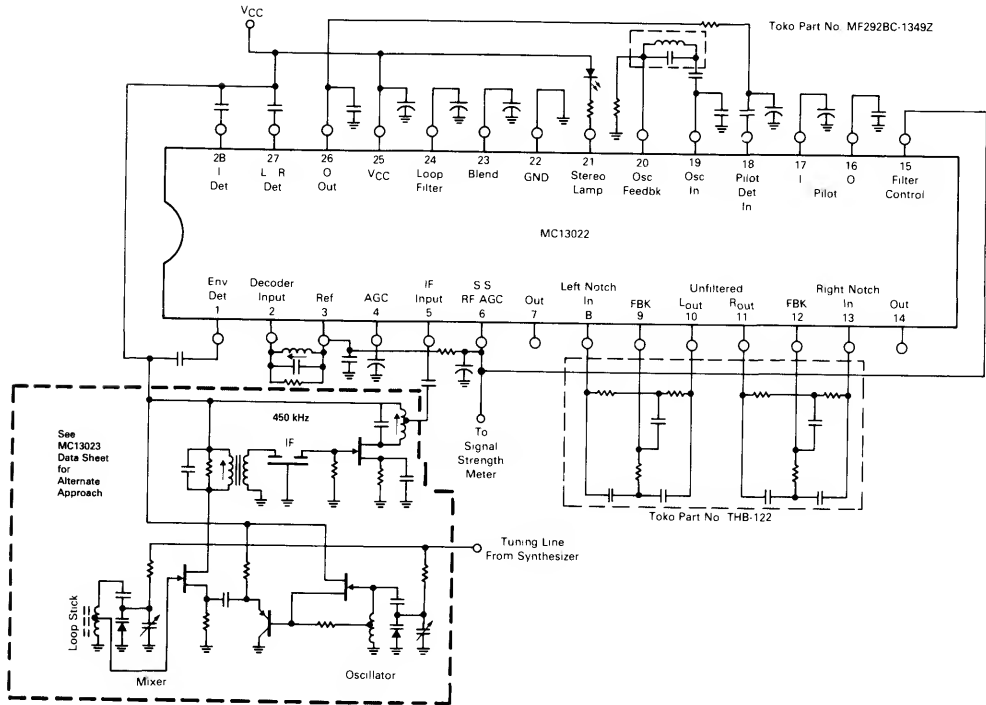


FIGURE 4 — RF AGC/SIGNAL STRENGTH OUTPUT versus INPUT SIGNAL



MC13022

FIGURE 5 — HIGH PERFORMANCE HOME TYPE AM STEREO RECEIVER



MC13023

Advance Information

AM STEREO FRONT END AND TUNER STABILIZER

The MC13023 is a companion part to the MC13022 C-QUAM® AM Stereo Decoder. It provides the mixer, local oscillator, and IF amplifier to make a complete AM stereo tuner system. Also included is all circuitry needed to provide the tuning function for high performance manually tuned radios, and a wideband RF AGC circuit for very wide dynamic range systems. The wideband AGC can be disabled to save current in battery powered applications where it is not needed.

For Manually and Electronically Tuned Radios:

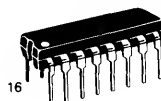
- Operation from 4.0 V to 10 V Supply
- Complete "Front End" for Home and Portable Radios
- Wideband AGC for External RF Amplifier in Automotive Type Radios
- Local Oscillator Unaffected by RF Signal Variations

For Manually Tuned Radios:

- Provides AFC for Tuning Ease and Accuracy
- Eliminates Microphonic Responses
- Provides Tuned Lock Indication
- Uses Existing Mechanical Tuning Elements
- Narrows Audio Bandwidth in MC13022 While Tuning to Reduce Interstation Noise

MOTOROLA C-QUAM® AM RECEIVER FRONT END AND TUNER STABILIZER

**SILICON MONOLITHIC
 INTEGRATED CIRCUIT**

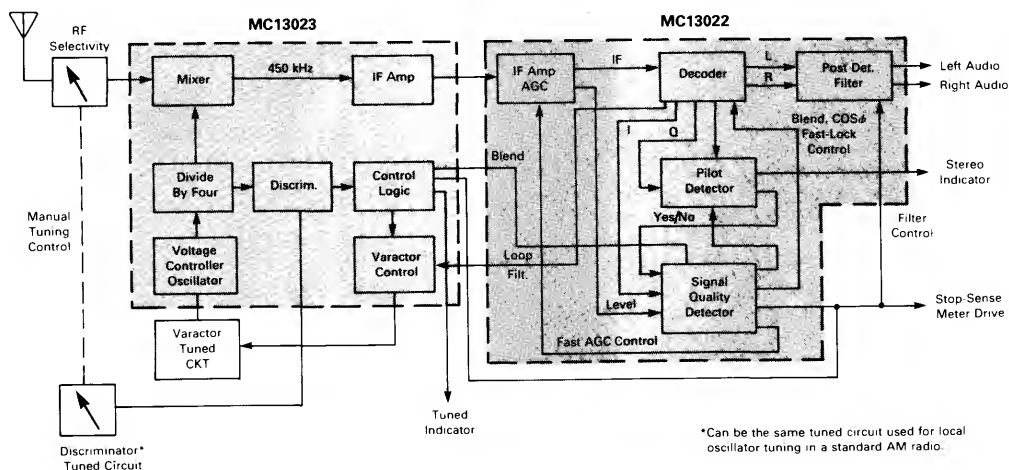


P SUFFIX
 PLASTIC PACKAGE
 CASE 648

D SUFFIX
 PLASTIC PACKAGE
 CASE 751B
 (SO-16)



FIGURE 1 — MANUALLY TUNED SYSTEM



The purchase of the Motorola C-QUAM® AM Stereo Decoder does not carry with such purchase any license by implication, estoppel or otherwise, under any patent rights of Motorola or others covering any combination of this decoder with other elements including use in a radio receiver. Upon application by an interested party, licenses are available from Motorola on its patents applicable to AM Stereo radio receivers.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MC13023

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V _{CC}	12	Vdc
Tuned Lamp Current		20	mAdc
Operating Temperature	T _A	-40 to +85	°C
Storage Temperature	T _{stg}	-65 to +150	°C
Junction Temperature	T _{J(max)}	150	°C
Power Dissipation	P _D	1.25	W
Derate above 25°C		10	mW/°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 8.0 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Min	Typ	Max	Unit
Power Supply Operating Range, Pin 1	4.0	8.0	10	Vdc
Supply Line Current Drain, Pin 1 I _{DD1} (Pin 2 Grounded) I _{DD2} (Pin 2 Open)	5.0 6.0	7.5 9.0	9.0 11	mAdc
Reference Current (α -3.0 V (Drain/Supply), Pin 7)	-100	0	+100	μ Adc
Wideband AGC Output Voltage Into 5.1 k Ohm Load Connected to 5.0 V, Pin 16				Vdc
	α -120 dBV	4.7	—	
	α -45 dBV	3.5	—	
	α -36 dBV	2.1	—	
Varactor Tuning Current (Out of Tuning Window), Pin 12	—	180	—	μ Adc
Varactor Tuning Current (In Tuning Window), Pin 12	—	3.7	—	μ Adc
Varactor Tuning Voltage Range, Pin 12	0.5 Vdc from V _{CC} and Ground			
Loop Filter Input Current, Pin 15	—	—	100	μ Adc
IF Output Pin 8, 3.3 k Ohm Load	310	375	450	mVrms
IF Input Pin 3, -30 dBV, 1.7 MHz	—	—	—	
IF dc Current Drain, Pin 8	—	1.0	—	mAdc
Mixer dc Current Drain, Pin 4	—	0.8	—	mAdc
Mixer Input Impedance, Pin 3	—	—	—	k Ohms
Mixer Output Impedance, Pin 4	—	—	—	k Ohms
"Tuned" Lamp Indicator Leakage Current, Pin 9	—	—	1.0	μ Adc

CIRCUIT DESCRIPTION

MIXER

The mixer is doubly balanced and has an extended dynamic range. The output is single ended and works into a resistive load, which gives a better impedance match to a ceramic IF filter than a tuned circuit and simplifies alignment.

IF AMPLIFIER

The first IF amplifier is a wide dynamic range design that needs no AGC. All IF AGC is done in the MC13022 by a shunt attenuator preceding the second IF stage. The shunt attenuator has the additional benefit of providing a variable load on the IF coupling coil, which reduces the bandwidth at low signal amplitudes.

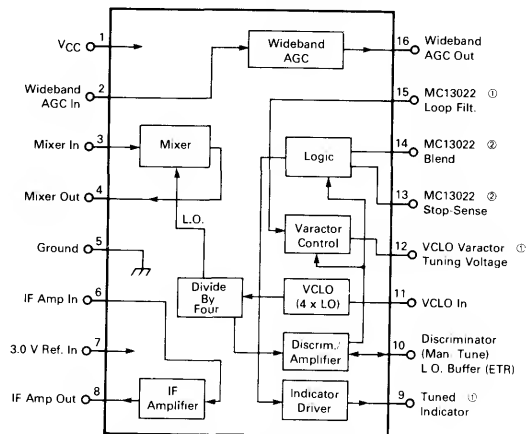
OSCILLATOR

The single pin oscillator runs at four times the local oscillator mixer injection frequency. The VCLO is varactor tuned by the frequency synthesizer in electronically tuned applications and by internal varactor drive control in manually tuned applications. The frequency divider isolates the VCLO from any load changes caused by varying incoming RF signal strength. There is also a local oscillator buffered output for driving a frequency synthesizer in electronically tuned applications. This output drives a discriminator coil in manually tuned applications.

WIDEBAND AGC

The wideband AGC is used to prevent receiver front end overload in very wide dynamic range applications such as automotive radios. The wideband AGC has an

FIGURE 2 — PIN DESCRIPTION



① Manually Tuned Application only — not used for ETR

② Manually Tuned Application only — disabled by 100 k Ohm to 3.0 V for ETR

independent input and a current drive output to allow maximum flexibility of application. Grounding the input will turn off most of the circuit to save current in battery powered applications where the wideband AGC is not needed.

MANUAL TUNING, GENERAL DESCRIPTION

The local oscillator, consisting of a VCLO and four times frequency divider, is varactor controlled. When stopped on a station, the varactor is controlled by the

MC13023

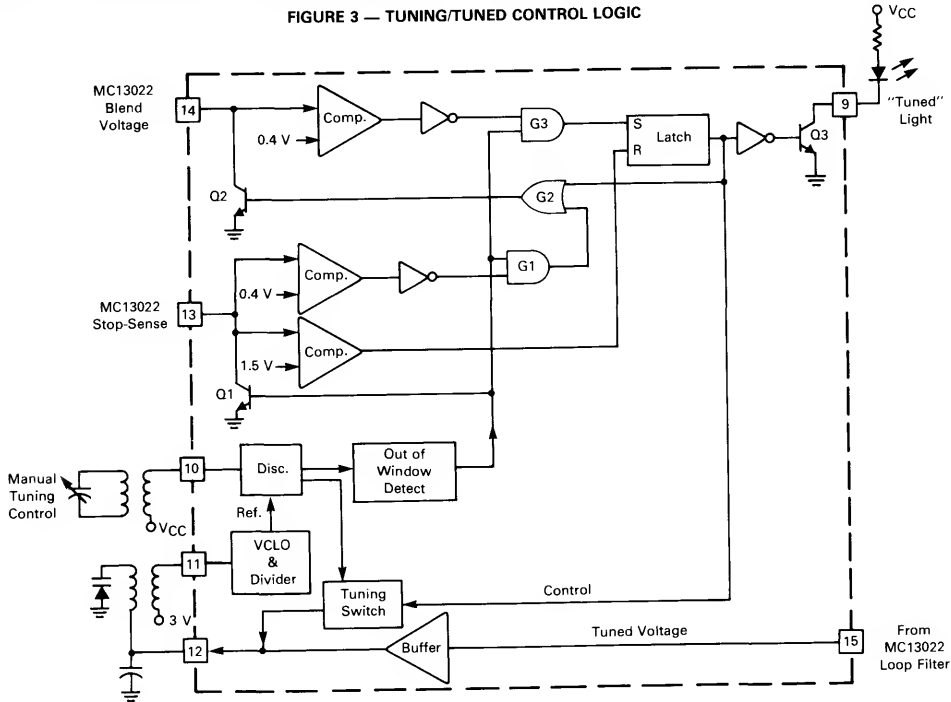
same loop filter voltage that controls the VCO in the MC13022. In this mode the local oscillator is completely immune from mechanical vibration of the tuning elements.

The mechanical input for manual tuning changes the center frequency of a wide-band discriminator. The reference frequency for the discriminator comes from the VCLO divider. When the discriminator has been tuned more than ± 7.0 kHz from the reference, a high current drive from the discriminator to the VCLO is switched on

to rapidly retune the local oscillator frequency so as to follow the center of the discriminator. At the same time the MC13022 is forced into the mono mode, via connection to the MC13022 blend line, to prevent any audible effects from tuning.

When tuning is stopped and the MC13022 locks on the new station, the discriminator VCLO control current is switched off and the "tuned" indicator is turned on. The MC13022 VCO loop filter control voltage will then AFC the VCLO to put the IF frequency on center.

FIGURE 3 — TUNING/TUNED CONTROL LOGIC



MANUAL TUNING, DESCRIPTION OF CONTROL SEQUENCE

Assuming that the radio has been tuned to a stereo station, the MC13022 blend voltage would be at 3.6 V and the stop-sense voltage greater than 2.3 V. The MC13023 VCLO, see Figure 3, would have the varactor controlled through a buffer from the MC13022 VCO control. Q1 and Q2 are off and the "tuned" light is on, the latch being in the reset condition from the high on the stop-sense line. When the mechanical tuning control is moved to change to a new station the discriminator is tuned to a new frequency. The out-of-window detector immediately turns on Q1 to pull down the stop-sense/meter drive line of the MC13022. Where this line is also used to provide automatic audio bandwidth control, the pull-down reduces the bandwidth to approximately 2.0 kHz, thereby minimizing the annoying interstation noise.

As the stop-sense goes below 0.4 V, the blend line of the MC13022 is pulled down by Q2, controlled by the signal through gates G1 and G2. Between 2.2 V and 1.5 V on the blend line, the MC13022 blends the audio from stereo to mono. Below 0.7 V the pilot detector is turned off.

When the blend line goes below 0.4 V, the latch is set through Gate 3, the "tuned" light is turned off, and the control of the VCLO is switched to the discriminator.

In the MC13022 the low blend voltage activates the fast AGC on the 2nd IF amplifier, sets a latch that will allow fast acquisition of stereo when pilot is detected, and activates the stop-sense. With the blend held low the stop-sense will act as a lock detector, staying low until the MC13022 VCO locks.

With the discriminator in control, the VCLO will be pulled to center the local oscillator frequency in the discriminator. Once within the tuned window, the window detector will release the pull-down on the stop-sense line. If the discriminator was not tuned on a station the MC13022 will not lock and will hold the stop-sense low, preventing any further action.

Assuming that the MC13022 does lock on to a station, the stop-sense will rise. At 1.5 V the latch will be reset, turning on the "tuned" light, releasing the pull-down on the blend line, and switching off the discriminator control of the VCLO.

The MC13022 decoder PLL will AFC the VCLO to put the IF frequency in the center of the IF as determined by the tuning of the VCO coil of the MC13022. The tuning control can now be adjusted within the ± 7.0 kHz tuned window to fine tune the RF selectivity.

FIGURE 4 — MANUALLY TUNED APPLICATION

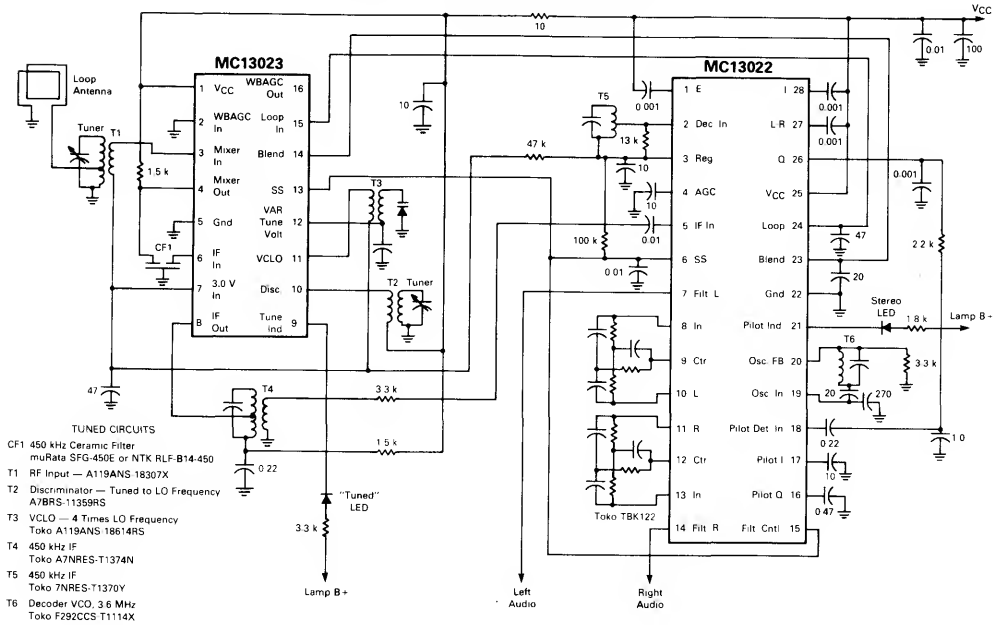
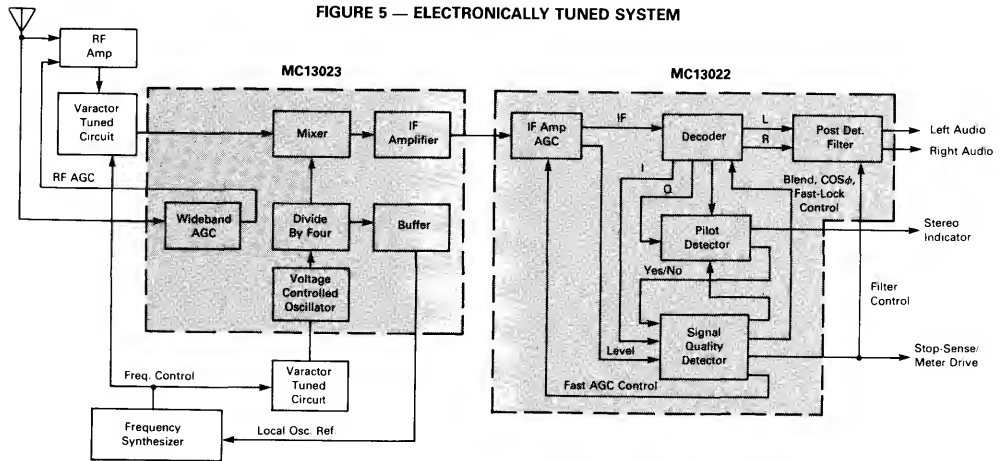


FIGURE 5 — ELECTRONICALLY TUNED SYSTEM



ELECTRONICALLY TUNED RECEIVERS

Figure 5 is a block diagram showing the MC13023 in an electronically tuned system. Except for the four times oscillator and divider, it is similar to most standard AM radio systems. The RF stage and wideband AGC would typically be used in automobile radios. A home type receiver with loop antenna would not normally require the RF stage.

TYPICAL ETR APPLICATION

The performance of AM radios is limited primarily by overload problems such as desensitization, cross-modulation and intermodulation. Problems are caused by nonlinearities in the front end of the radio.

The most severe signal environment is seen by automotive radios as they pass through strong RF fields of nearby stations, and, for this reason, most applications

use some form of front end AGC. A typical front end design is shown in Figure 6. This system uses a FET RF stage with AGC applied to a cascode transistor in series with the FET. The wideband AGC turns down the RF gain any time there is a strong signal present in a wide band of frequencies determined only by the selectivity of the first RF coil.

A HIGH PERFORMANCE ETR TUNER

Improvement in overload performance requires multiple solutions. Subsequently, when one element of the circuit is improved another part of the circuit will overload a few dBs higher.

In the MC13023, the mixer, which is normally the first element to overload and become nonlinear on nearby signals, has been degenerated to give 8.0 to 10 dB improvement over a normal mixer. The mixer is protected by the total amount of RF selectivity for signals further out in frequency.

The next most vulnerable element is usually the tuning varactor on the first RF coil, followed by the wideband AGC elements and RF stage. Figure 7 shows a high performance front end circuit that is much better

for overload than the circuit of Figure 6. The circuitry around the MC13022 remains the same.

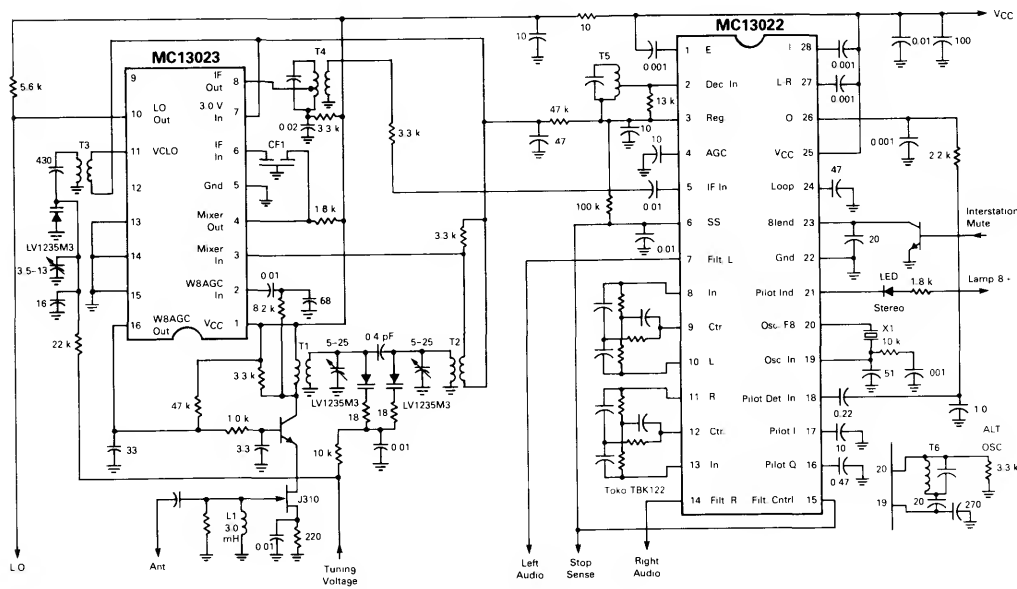
A light dependent resistor (LDR) is used in front of the RF amplifier for attenuation. The LDR is much more linear and has a greater dynamic range than diodes or transistors that are sometimes used for RF AGC. The current through the LED, which in turn controls the resistance of the LDR, is varied by the wideband AGC.

The first RF coil is tuned with two back-to-back varactors, as is typically done in FM receivers, to make the circuit more linear. The second RF coil varactor is sufficiently protected by the first coil so that two varactors are not needed.

With the above improvements, the wideband AGC input can be taken after the second RF coil. This will prevent strong signals, distant in frequency from a weak desired station from causing unnecessary attenuation or drop-out.

The performance with the above improvements is now limited by overload in the FET RF amplifier. Slight degeneration with unbypassed source resistance greatly improves the overload performance with only a slight reduction in sensitivity.

FIGURE 6 — ELECTRONICALLY TUNED APPLICATION



TUNED CIRCUITS

CF1 450 kHz Ceramic Filter
muRata SFG-450E or NTK RLF-814-450
L1 3.0 mH RF Amp. Input
Toko 126ANS-7594HM
T1 RF Input — A119ANS-18307X
T2 Discriminator-Tuned to LO Frequency
A78RS-11359RS
T3 VCO — 4 Times LO Frequency
Toko A119ANS-18614RS

T4 450 kHz IF
Toko A7NRES-T1374N
T5 450 kHz IF
Toko 7NRES-T1370Y
T6 Decoder VCO, 3.6 MHz
Toko F292CCS-T1114X
X1 3.6 MHz Resonator

9

[illegible]

CF1 450 kHz Ceramic Filter
muRata SFG-450E

L1 3.0 mH RF Amp Input
Toko 126ANS-7594HM

T1 RF Input — A119ANS-18307X

T2 Discriminator Tuned to LO
Frequency A78RS-11359S

T3 VCL0 — 4 Times LO Frequency
Toko A119ANS-18614RS

T4 450 kHz IF
Toko A78RS-11148N

Advance Information

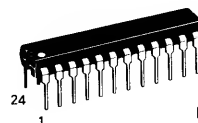
LOW VOLTAGE MOTOROLA C-QUAM® AM STEREO RECEIVER

The MC13024 is intended to serve the manually tuned portable and pocket radio mass market. This part includes all receiver and stereo decoding functions, from antenna to Left and Right audio outputs.

- Full Operation from 1.8 V to 8.0 Vdc Supply
- Low Power, Current Drain (typ) 5.0 mA
- Typical Distortion <1% at 90% L + R or 50% Single Channel
- Typical Channel Separation >25 dB
- Pilot Tone Detector
- Combined Two Level Tuning and Stereo Indicator
- "Blend On" Stereo Mode
- High Accuracy, Fast Locking VCLO
- Controlled Return to Monaural Under Adverse Conditions
- Minimized "Tweets and Birdies"
- Minimized Tuning Transients

LOW VOLTAGE MOTOROLA C-QUAM® AM STEREO RECEIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT

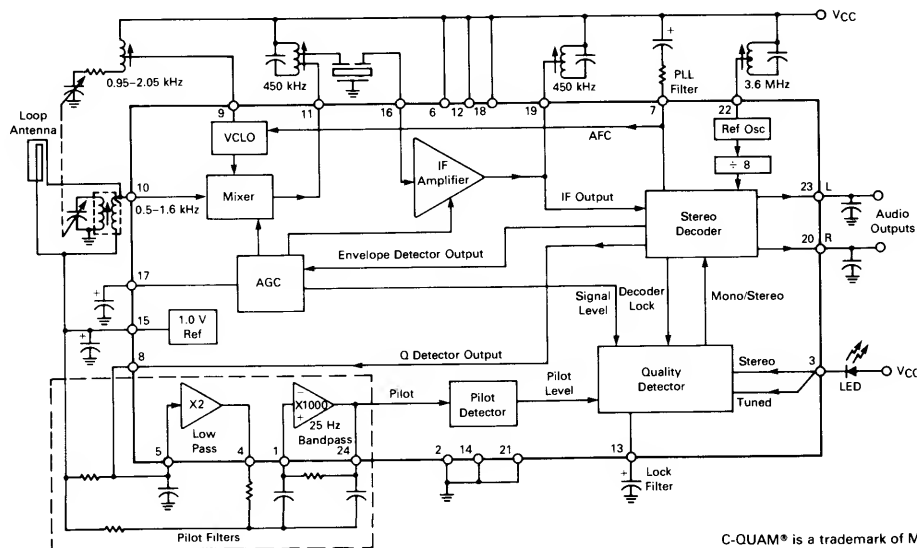


P SUFFIX
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 CASE 724



DW SUFFIX
 PLASTIC PACKAGE
 CASE 751E
 (SO-24L)

FIGURE 1 — FUNCTIONAL BLOCK DIAGRAM



C-QUAM® is a trademark of Motorola.

The purchase of the Motorola C-QUAM® AM Stereo Decoder does not carry with such purchase any license by implication, estoppel or otherwise, under any patent rights of Motorola or others covering any combination of this decoder with other elements including use in a radio receiver. Upon application by an interested party, licenses are available from Motorola on its patents applicable to AM Stereo radio receivers.

This document contains information on a new product. Motorola reserves the right to change or discontinue this product without notice.

MC13024

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	10	Vdc
Operating Temperature	T_A	0 to +70	$^\circ\text{C}$
Storage Temperature	T_{stg}	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($V_{CC} = 2.2\text{ Vdc}$, $T_A = 25^\circ\text{C}$, Input RF signal = 40 dB μV at 1.0 MHz directly fed to the receiver, Modulating signal = 1.0 kHz sine wave at 30% modulation, unless otherwise noted.)

Characteristic	Min	Typ	Max	Unit
Power Supply Voltage	—	1.8 to 8.0	—	Vdc
Supply Current, Excluding Current LEDs				mA
No Signal	4.0	5.4	6.5	
Monaural	5.0	6.0	6.8	
Stereo	5.0	6.0	6.8	
LED Driving Current				mA
Monaural	0.8	1.2	1.8	
Stereo	2.5	4.0	5.5	
Sensitivity, Monaural				μV
Maximum	—	5.0	—	
20 dB S/N	—	8.0	—	
S/N Ratio				dB
Monaural	30	38	—	
Stereo	28	34	—	
Channel Separation				dB
L to R	17	25	—	
R to L	17	25	—	
Recovered Audio (L or R)	9.0	13	16	mVRMS
Stereo Channel Balance	—	-32	—	dB
Distortion				%
Monaural	—	0.9	1.3	
Stereo	—	1.1	2.5	

NOTE: 1. A 200 Hz high-pass filter is required at the recovered audio output to filter out the residual 25 Hz pilot frequency.

[illegible]

[illegible]

T1	Input Transformer	A78RS-10952X — TOKO
T2	Local Oscillator	A78RS-T1342AIX — TOKO
T3	Mixer Oscillator	7MCS-T1464X — TOKO
T4	IF Input (Ceramic)	ALFC 450E / ACMF-450ST / NTKRL-B12-450
T5	IF Output	7MCS-T1463BS — TOKO
T6	Reference Oscillator	MF251ACS-3688VL — TOKO
C1	Tuning Capacitor	HU2212A-N000-0

GENERAL DESCRIPTION

The MC13024 is a complete C-QUAM® AM stereo receiver, from the antenna to low level audio. All that is needed make a complete AM stereo radio is the addition of the appropriate audio output amplifier. The MC13024 is intended for use in most types of manually tuned receivers: pocket portables, "boom boxes," table radios, etc. It will operate from 1.8 Vdc to 8.0 Vdc and requires typically 5.0 mA (not including LED). This broad supply voltage tolerance and low power consumption makes it ideal for portables using as few as 2 battery cells. The radios which can be built using this part can be quite low in cost, while still benefiting from a high degree of functional sophistication.

FEATURES

The MC13024 contains a wide dynamic range mixer, IF, AGC, AFC, C-QUAM® decoder, stereo pilot tone detector, and a signal quality detector. The stereo decoding and pilot detection are similar to the well-established MC13020, except for reduced peripheral components, and the phase-locked loop used for the L-R detection now is looped around the entire receiver. In other words, the PLL controls the tuner local oscillator (VCO) rather than a detector loop after the IF. The advantage of this, in manually tuned AM stereo, is significant, because it assures that the signal will always be properly centered in the IF bandpass, which is critical to good channel separation. This architecture also gives the radio an AFC tuning behavior which makes it easy to tune. The PLL has two "speeds," provided by current ratios of 50:1, which give fast lock and low distortion, respectively.

A signal quality detector circuit monitors lock condition, excess in-phase modulation due to interference, pilot presence and amplitude, and the movement of the

tuning element by the user. A proper level of pilot must be present for several cycles before stereo mode will be enabled. When all conditions are correct, the transition from monaural to stereo is done gradually to prevent a transient "pop." Under aberrated conditions, the audio may either blend to mono or make an immediate change to mono, depending on the detected condition. The LED pin drives a dual purpose indicator: low current for PLL lock, and full current for stereo mode. Again, the switching is done "softly" to prevent transient loading of a weak battery.

The IF gain and the mixer RF gain are each reduced, in turn, as signal strength increases, to optimize S/N and prevent overload. The receiver is capable of 20 dB S/N at 2.5 μ V/50 ohm input. At weak signals, the reference oscillator and quadrature divider are shut off to minimize "tweets and birdies."

RADIO CONSTRUCTION

Layout is not much more critical than any high performance AM receiver. Care must be taken to provide a good ground plane and short leads on signal paths. Take special care to keep the reference oscillator components close to Pin 22 and protected from coupling from the pilot bandpass output, Pin 24. Also take care with the ever present threat of RF radiation from the audio output back into the antenna. This can be controlled by proper component location and good (close) RF bypass on the amplifier V_{CC} and good snubbers on the audio outputs. Keeping in mind that this is a phase-detecting receiver, it is important to mount coils securely and avoid movable wires in tuned circuits. A lot of individual preference will go into each implementation; the components shown here are only intended to provide a good working start.

MC13041

Product Preview

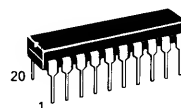
AM RECEIVER SUBSYSTEM

This circuit is the core of an AM broadcast receiver. The MC13041 is ideal as the front end for AM stereo radios using electronic tuning. The scan detection system operates with both frequency and signal amplitude data for "no false" tuning.

- Electrically Equivalent to ULN3841
- Full AM Receiver Function Including: L.O., Balanced Mixer, IF Amp, AM Detector, Scan Control Detectors, and an Internal Switchable Voltage Regulator
- Companion Device to MC13020 C-QUAM® AM Stereo Decoder
- Wideband (RF) Delayed AGC
- Optional Narrowband FM Output
- Tailored to Interface with Synthesizers in Scanning E.T.R. Applications
- Stop Detection Independent of AGC Time Constant

AM RECEIVER SUBSYSTEM

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**



P SUFFIX
PLASTIC PACKAGE
CASE 738

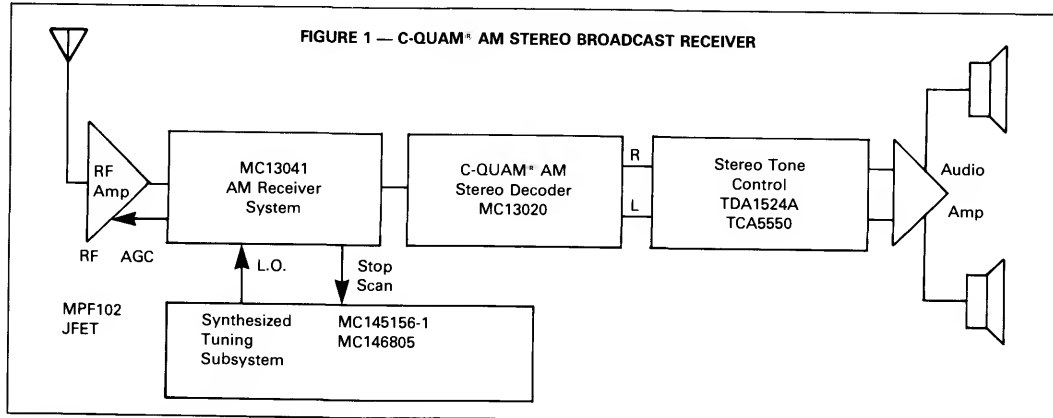
PIN CONNECTIONS

IF In	1	20	IF AGC
IF Bypass	2	19	Mixer Out
IF Bias	3	18	Mixer In
Gnd	4	17	Mixer Bias
Audio Out	5	16	RF AGC In
VCC	6	15	Osc
Det. In	7	14	Osc Gnd
IF Out	8	13	L.O. Gnd
V Reg	9	12	RF AGC Out
AFC Out	10	11	Stop Out

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage Pin 6	VCC	18	Vdc
Thermal Resistance, Junction to Ambient	R _{θJA}	75	°C/W
Operating Ambient Temperature Range	T _A	-40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

FIGURE 1 — C-QUAM® AM STEREO BROADCAST RECEIVER



This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

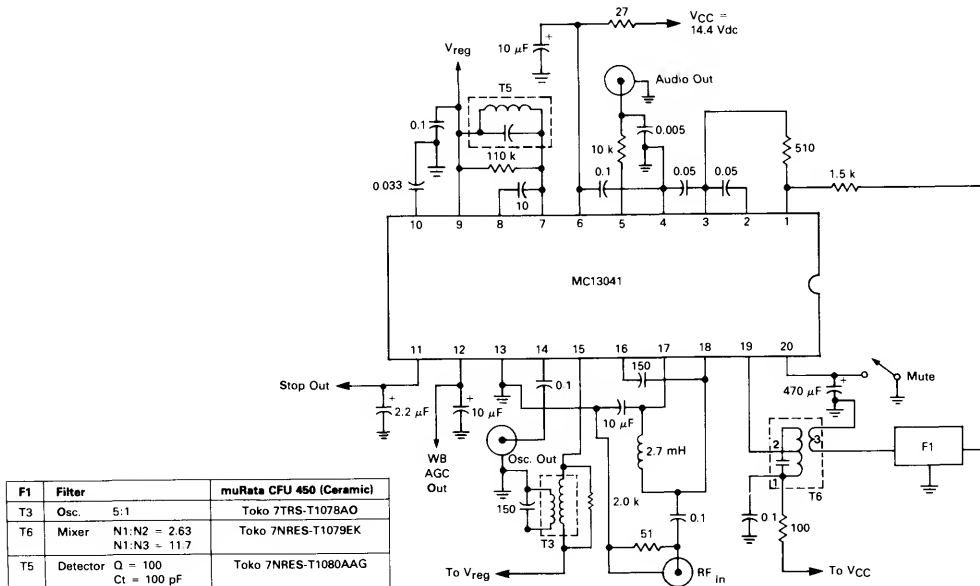
MC13041

ELECTRICAL CHARACTERISTICS ($V_{CC} = 14.4$ Vdc, $T_A = +25^\circ\text{C}$, RF Input Frequency = 1.0 MHz, $I_f = 450$ kHz, FMOD = 1.0 kHz, Modulation = 30%, Test Circuit of Figure 2, unless otherwise noted.)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage Range	V_{CC}		—	6.5–16.5	—	Vdc
Supply Current	I_{CC}	No Input Signal	—	25	33	mAdc
RF Sensitivity	RF In to Pin 18	Pin 5 Audio Out Equals 50 mV	—	2.6	10	μVrms
Usable Sensitivity	RF In to Pin 18	At Pin 5 $\frac{S+N}{N} = 20$ dB	—	5.6	10	μVrms
Recovered Audio	Audio Out at Pin 5	1.0 mV RF In at Pin 18	173	240	346	mVrms
Total Harmonic Distortion	THD at Pin 5	1.0 mV RF In 80% modulation at Pin 5	—	0.5	3.0	%
Oscillator Output	V_{OSC}	RF Out at Pin 14	—	330	—	mVrms
Stop Voltage	V_{STOP} Pin 11	No Input at Pin 18	4.3	5.2	—	Vdc
Stop Sensitivity	V_{STOP} SEN Pin 18 RF	Pin 11 Equals 1.5 Vdc	27	40	80	μVrms
Stop Bandwidth	V_{STOP} BW	Pin 18 = 1.0 mVrms Pin 11 = 1.5 Vdc	—	± 4.7	—	kHz
RF AGC	V_{AGC} Pin 12	RF Pin 16 = 0 mVrms	—	—	0.15	Vdc
		RF Pin 16 = 20 mVrms	0.8	—	—	
Overload	THD at Pin 5 Audio Out	RF In at Pin 18 = 25 mVrms Modulation = 80%	—	1.2	—	%
AGC Figure of Merit	Pin 5 Audio Drop to 10 dB Below Ref	RF In at Pin 18 dB Below 30 mV	—	75	—	dB

NOTE: Pin 9 voltage regulator output for local oscillator only.

FIGURE 2 — TEST CIRCUIT



TAKEN IN TEST CIRCUIT OF FIGURE 2

FIGURE 3 — RECOVERED AUDIO

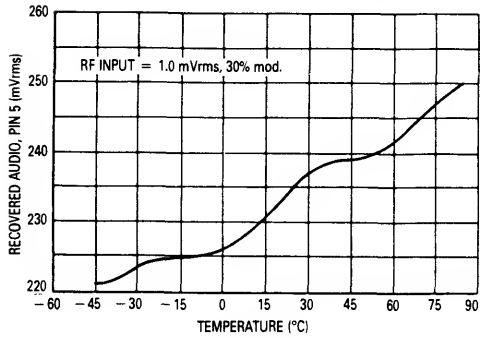


FIGURE 4 — RF INPUT AT AUDIO OUTPUT = 50 mVrms

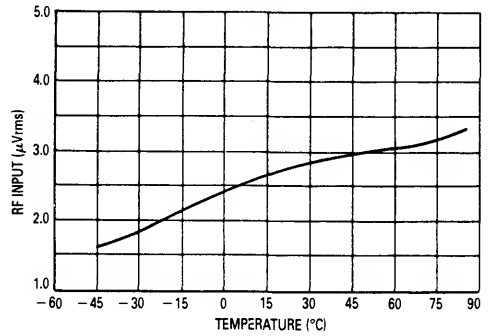


FIGURE 5 — AM AFC

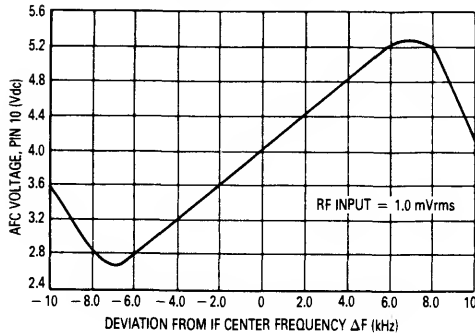


FIGURE 6 — STOP LEVEL

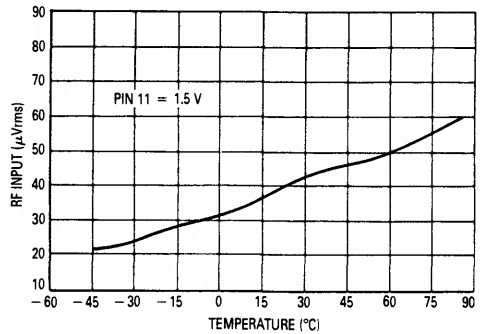


FIGURE 7 — FREQUENCY WINDOW

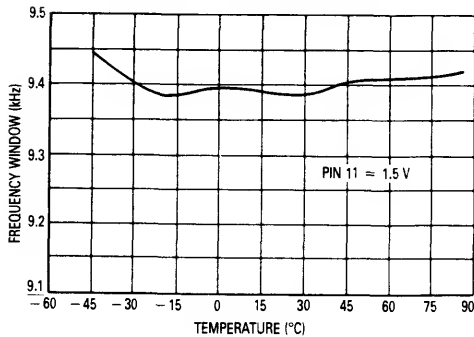
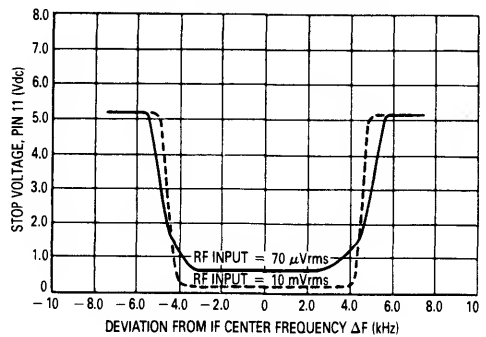


FIGURE 8 — FREQUENCY WINDOW



MC13041

FIGURE 9 — MC13041 BLOCK DIAGRAM

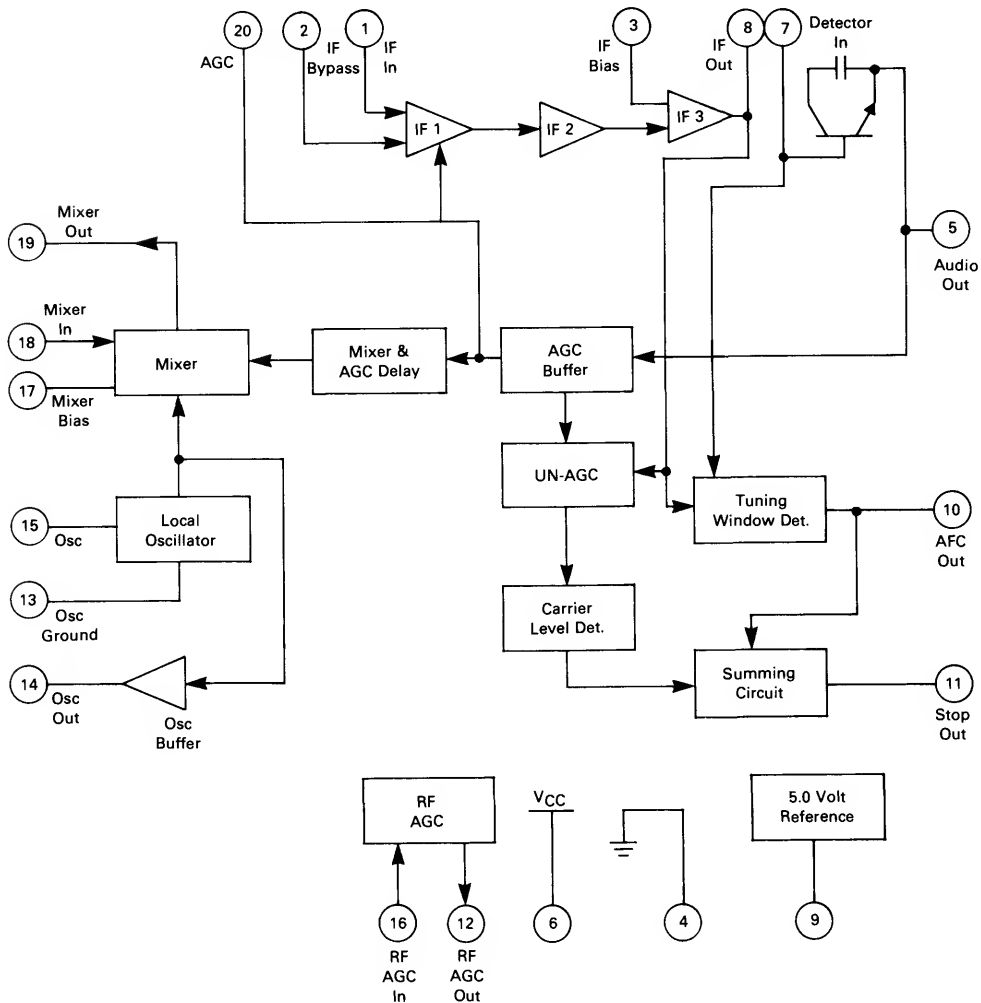
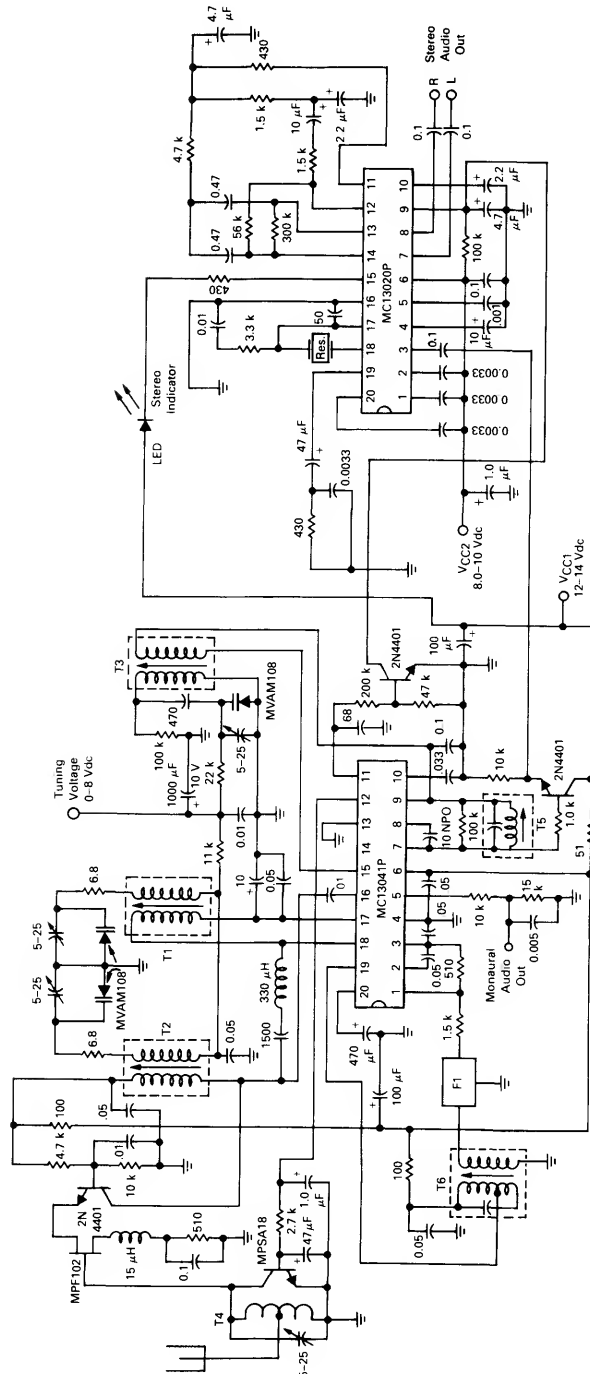


FIGURE 10 — APPLICATION SCHEMATIC



T1, T2	RF	Toko RW056A7894AO
T3	Osc	Toko 7TRS-T1078AO
T4	Ant	Toko 7HN-60064CY
T5	Det	Toko 7NRES-T1080AAG
T6	Mix	Toko 7NRES-T1079EK
F1	IF	muRata SFG450F — 6.0 kHz or SFG450E — 7.5 kHz or SFG450D — 10 kHz muRata CSA3.60MGF101
Res		

MC13041

FIGURE 11 — RECEIVER GAIN-REDUCTION VOLTAGES

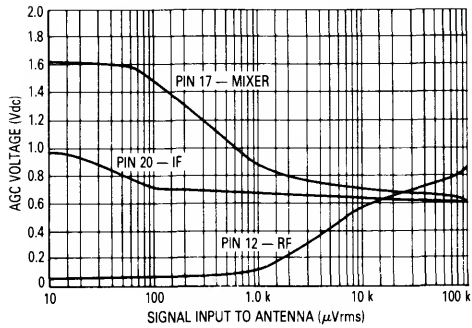
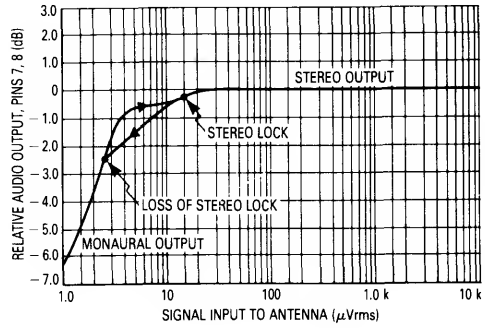


FIGURE 12 — RECEIVER RECOVERED AUDIO



MC13060

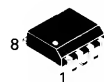
MINI-WATT AUDIO OUTPUT

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**

MINI-WATT AUDIO OUTPUT

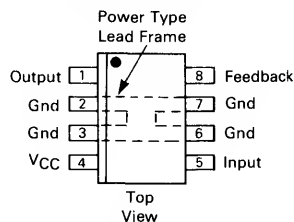
... a rugged and versatile power amplifier in a remarkable plastic power package.

- Supply Voltages from 6.0–35 Vdc
- 2.0 Watts Output @ 70°C Ambient on P.C. Board with Good Copper Ground Plane
- Self Protecting Thermal Shutdown
- Easy to Apply, Few Components
- Gain Externally Determined
- Output is Independent of Supply Voltage Over a Wide Range



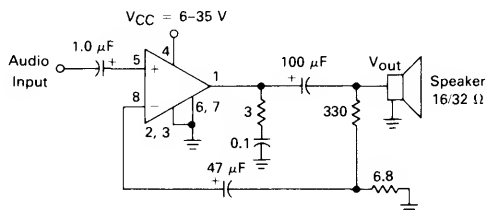
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SOP-8)

PIN CONNECTIONS

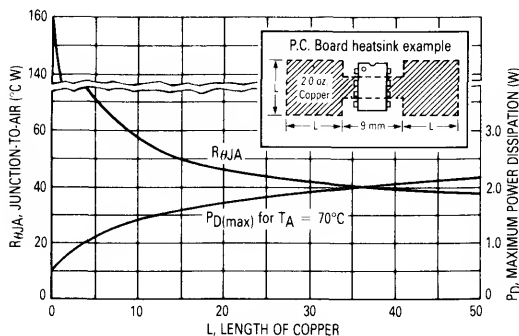


9

FIGURE 1 — TYPICAL APPLICATION



**FIGURE 2 — THERMAL RESISTANCE AND MAXIMUM POWER
DISSIPATION versus P.C. BOARD COPPER**



MC13060

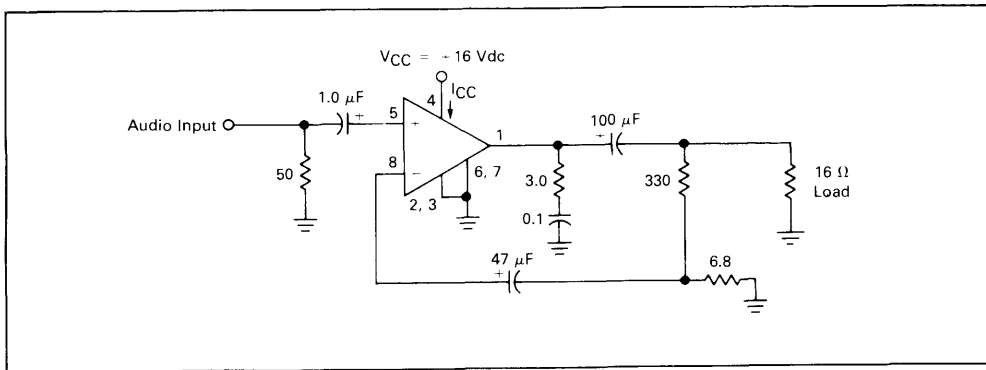
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	35	V
Audio Input, Pin 5		1.0	V_{p-p}
Thermal Resistance, Junction to Air	$R_{\theta JA}$	160	$^{\circ}C/W$
Thermal Resistance, Junction to Case	$R_{\theta JC}$	25	$^{\circ}C/W$
Junction Temperature	T_J	150	$^{\circ}C$
Operating Ambient Temperature Range	T_A	-40 to +85	$^{\circ}C$
Storage Temperature Range	T_{stg}	-65 to +150	$^{\circ}C$

ELECTRICAL CHARACTERISTICS — AUDIO SECTION ($T_A = 25^{\circ}C$, Circuit of Figure 3 unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Current, No Signal	I_{CC}	—	13	—	mAdc
Gain	A_O	—	50	—	V/V
Distortion at 62.5 mW Output, 1.0 kHz	THD	—	0.2	1.0	%
Distortion at 900 mW Output, 1.0 kHz	THD	—	0.5	3.0	%
Quiescent Output Voltage, No Signal	$V_{Pin 1}$	—	8.4	—	Vdc
Input Bias	$V_{Pin 5}, V_{Pin 8}$	—	0.7	—	Vdc
Input Resistance	$R_{in}, Pin 5$	—	28	—	k Ω
Output Noise (50 Hz–15 kHz) Input 50 Ω	V_{out}	—	0.5	4.0	mVrms

FIGURE 3 — TEST CIRCUIT



DESCRIPTION

The MC13060 is a quasi-complementary audio power amplifier, mounted in the SOP 8 (power SOIC package). It is well suited to a variety of 1.0 and 2.0 watt applications in radio, TV, intercoms, and other speaker driving tasks. It requires the usual external components for high frequency stability and for gain adjustment.

The output signal voltage and the power supply drain current are very linearly related, as shown in Figure 5. Both are quite constant over wide variation of the power supply voltage (above min V_{CC} for clipping, of course).

The amplifier can best be described as a voltage source with about 1.0 A_{p-p} capability. On a good heat sink, it can deliver over 2.0 watts at 70 $^{\circ}C$ ambient.

The MC13060 will automatically go into shut-down at a die temperature of about 150 $^{\circ}C$, effectively protecting itself, even on fairly stiff power supplies. This eliminates the need for decoupling the power supply, which degrades performance and requires extra components.

Input Pins 5 and 8 are internally biased at 0.7 Vdc and should not be driven below ground.

ALL CURVES TAKEN IN THE TEST CIRCUIT OF FIGURE 3 UNLESS OTHERWISE NOTED

**FIGURE 4 — QUIESCENT SUPPLY CURRENT AND OUTPUT VOLTAGE
versus SUPPLY VOLTAGE**

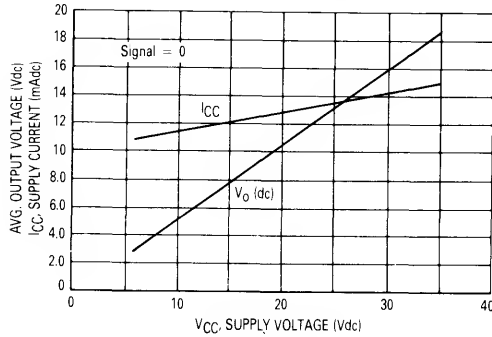


FIGURE 5 — SUPPLY CURRENT versus OUTPUT

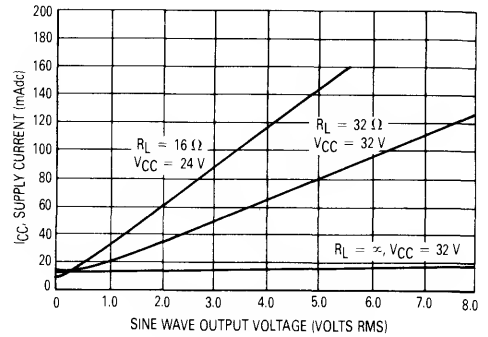


FIGURE 6 — DISTORTION AND GAIN versus FREQUENCY

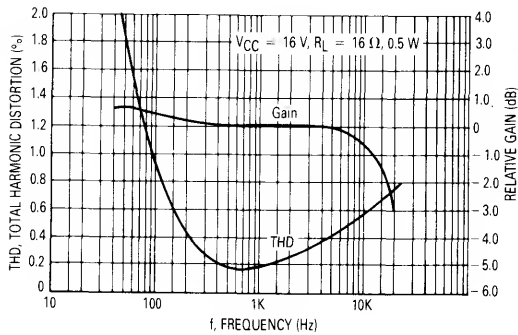


FIGURE 7 — DISTORTION versus POWER OUTPUT

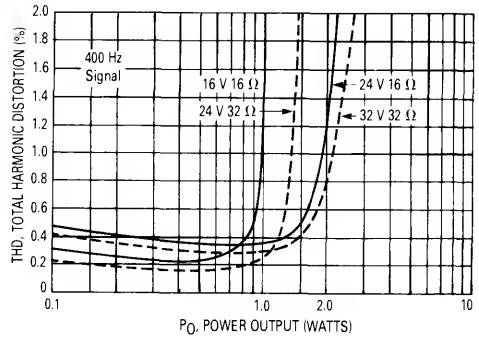


FIGURE 8 — DISSIPATION versus OUTPUT POWER — 32 Ω LOAD

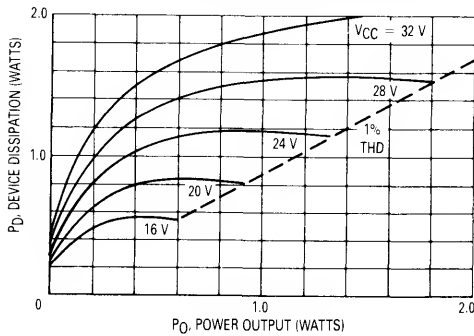
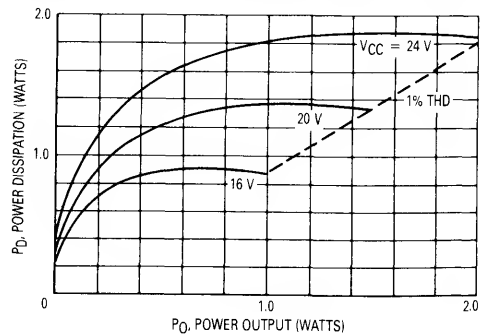
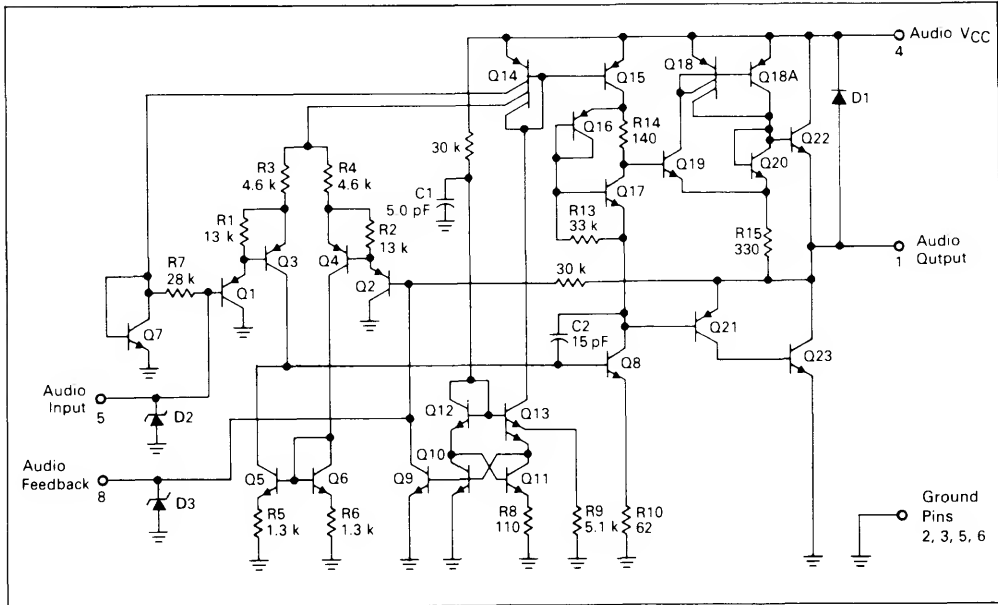


FIGURE 9 — DISSIPATION versus OUTPUT POWER — 16 Ω LOAD



MC13060

FIGURE 10 — INTERNAL SCHEMATIC

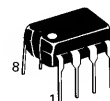


MC34119

LOW POWER AUDIO AMPLIFIER

The MC34119 is a low power audio amplifier integrated circuit intended (primarily) for telephone applications, such as in speakerphones. It provides differential speaker outputs to maximize output swing at low supply voltages (2.0 volts minimum). Coupling capacitors to the speaker are not required. Open loop gain is 80 dB, and the closed loop gain is set with two external resistors. A Chip Disable pin permits powering down and/or muting the input signal. The MC34119 is available in a standard 8-pin DIP or a surface mount package.

- Wide Operating Supply Voltage Range (2–16 volts) — Allows Telephone Line Powered Applications
- Low Quiescent Supply Current (2.7 mA Typical) for Battery Powered Applications
- Chip Disable Input to Power Down the IC
- Low Power-Down Quiescent Current (65 μ A Typical)
- Drives a Wide Range of Speaker Loads (8 Ohms and Up)
- Output Power Exceeds 250 mW with 32 Ohm Speaker
- Low Total Harmonic Distortion (0.5% Typical)
- Gain Adjustable from <0 dB to >46 dB for Voice Band
- Requires Few External Components

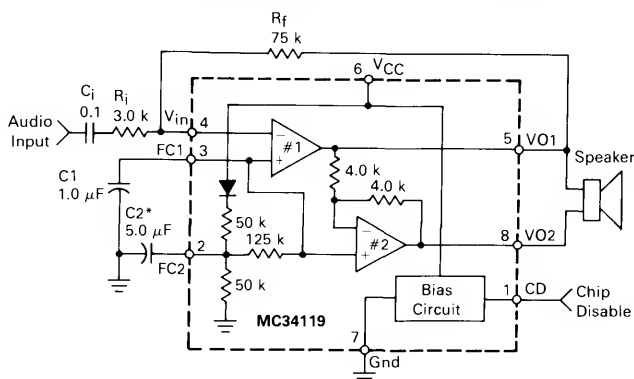


P SUFFIX
 PLASTIC PACKAGE
 CASE 626



D SUFFIX
 PLASTIC PACKAGE
 CASE 751
 (SO-8)

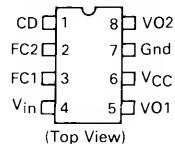
BLOCK DIAGRAM AND TYPICAL APPLICATION CIRCUIT



* = Optional

$$\text{Differential Gain} = 2 \times \frac{R_f}{R_i}$$

PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
MC34119P	–20°C to +70°C	Plastic DIP
MC34119D	–20°C to +70°C	Plastic SOIC

MC34119

ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Units
Supply Voltage	-1.0 to +18	Vdc
Maximum Output Current at VO1, VO2	± 250	mA
Maximum Voltage @ V_{in} , FC1, FC2, CD	-1.0, $V_{CC} + 1.0$	Vdc
Applied Output Voltage to VO1, VO2 when disabled	-1.0, $V_{CC} + 1.0$	Vdc
Junction Temperature	-55, +140	°C

Devices should not be operated at these values. The "Recommended Operating Limits" provide for actual device operation.

RECOMMENDED OPERATING LIMITS

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	V_{CC}	+2.0	—	+16	Vdc
Load Impedance	R_L	8.0	—	100	Ω
Peak Load Current	I_L	—	—	± 200	mA
Differential Gain (5.0 kHz bandwidth)	A_{VD}	0	—	46	dB
Voltage @ CD (Pin 1)	VCD	0	—	V_{CC}	Vdc
Ambient Temperature	T_A	-20	—	+70	°C

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

Characteristics	Symbol	Min	Typ	Max	Units
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AMPLIFIERS (AC CHARACTERISTICS)

AC Input Resistance (@ V_{in})	r_i	—	>30	—	M Ω
Open Loop Gain (Amplifier #1, $f < 100$ Hz)	A_{VOL1}	80	—	—	dB
Closed Loop Gain (Amplifier #2) ($V_{CC} = 6.0$ V, $f = 1.0$ kHz, $R_L = 32$ Ω)	A_{V2}	-0.35	0	+0.35	dB
Gain Bandwidth Product	GBW	—	1.5	—	MHz
Output Power, $V_{CC} = 3.0$ V, $R_L = 16$ Ω , THD $\leq 10\%$ $V_{CC} = 6.0$ V, $R_L = 32$ Ω , THD $\leq 10\%$ $V_{CC} = 12$ V, $R_L = 100$ Ω , THD $\leq 10\%$	P_{out3} P_{out6} P_{out12}	55 250 400	— — —	— — —	mW
Total Harmonic Distortion ($f = 1.0$ kHz) ($V_{CC} = 6.0$ V, $R_L = 32$ Ω , $P_{out} = 125$ mW) ($V_{CC} \geq 3.0$ V, $R_L = 8.0$ Ω , $P_{out} = 20$ mW) ($V_{CC} \geq 12$ V, $R_L = 32$ Ω , $P_{out} = 200$ mW)	THD	— — —	0.5 0.5 0.6	1.0 — —	%
Power Supply Rejection ($V_{CC} = 6.0$ V, $\Delta V_{CC} = 3.0$ V) ($C1 = \infty$, $C2 = 0.01$ μ F) ($C1 = 0.1$ μ F, $C2 = 0$, $f = 1.0$ kHz) ($C1 = 1.0$ μ F, $C2 = 5.0$ μ F, $f = 1.0$ kHz)	PSRR	50 — —	— 12 52	— — —	dB
Muting ($V_{CC} = 6.0$ V, 1.0 kHz $\leq f \leq 20$ kHz, CD = 2.0 V)	GMT	—	>70	—	dB

AMPLIFIERS (DC CHARACTERISTICS)

Output DC Level @ VO1, VO2, $V_{CC} = 3.0$ V, $R_L = 16$ Ω ($R_f = 75$ k) $V_{CC} = 6.0$ V $V_{CC} = 12$ V	VO(3) VO(6) VO(12)	1.0 — —	1.15 2.65 5.65	1.25 — —	Vdc
Output High Level ($I_{out} = -75$ mA, 2.0 V $\leq V_{CC} \leq 16$ V)	V_{OH}	—	$V_{CC} - 1.0$	—	Vdc
Output Low Level ($I_{out} = 75$ mA, 2.0 V $\leq V_{CC} \leq 16$ V)	V_{OL}	—	0.16	—	Vdc
Output DC Offset Voltage (VO1-VO2) ($V_{CC} = 6.0$ V, $R_f = 75$ k Ω , $R_L = 32$ Ω)	ΔV_O	-30	0	+30	mV
Input Bias Current @ V_{in} ($V_{CC} = 6.0$ V)	I_{IB}	—	-100	-200	nA
Equivalent Resistance @ FC1 ($V_{CC} = 6.0$ V)	R_{FC1}	100	150	220	k Ω
Equivalent Resistance @ FC2 ($V_{CC} = 6.0$ V)	R_{FC2}	18	25	40	k Ω

CHIP DISABLE (Pin 1)

Input Voltage — Low	V_{IL}	—	—	0.8	Vdc
Input Voltage — High	V_{IH}	2.0	—	—	Vdc
Input Resistance ($V_{CC} = V_{CD} = 16$ V)	R_{CD}	50	90	175	k Ω

POWER SUPPLY

Power Supply Current ($V_{CC} = 3.0$ V, $R_L = \infty$, CD = 0.8 V) ($V_{CC} = 16$ V, $R_L = \infty$, CD = 0.8 V) ($V_{CC} = 3.0$ V, $R_L = \infty$, CD = 2.0 V)	I_{CC3} I_{CC16} I_{CCD}	— — —	2.7 3.3 65	4.0 5.0 100	mA μ A
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Note: Currents into a pin are positive, currents out of a pin are negative.

MC34119

PIN DESCRIPTION

Symbol	Pin	Description
CD	1	Chip Disable — Digital input. A Logic "0" (<0.8 V) sets normal operation. A Logic "1" (≥2.0 V) sets the power down mode. Input impedance is nominally 90 k Ω .
FC2	2	A capacitor at this pin increases power supply rejection, and affects turn-on time. This pin can be left open if the capacitor at FC1 is sufficient.
FC1	3	Analog Ground for the amplifiers. A 1.0 μ F capacitor at this pin (with a 5.0 μ F capacitor at Pin 2) provides (typically) 52 dB of power supply rejection. Turn-on time of the circuit is affected by the capacitor on this pin. This pin can be used as an alternate input.
V _{in}	4	Amplifier input. The input capacitor and resistor set low frequency rolloff and input impedance. The feedback resistor is connected to this pin and VO1.
VO1	5	Amplifier Output #1. The dc level is $\approx (V_{CC} - 0.7 \text{ V})/2$.
V _{CC}	6	DC supply voltage (+2.0 to +16 volts) is applied to this pin.
GND	7	Ground pin for the entire circuit.
VO2	8	Amplifier Output #2. This signal is equal in amplitude, but 180° out of phase with that at VO1. The dc level is $\approx (V_{CC} - 0.7 \text{ V})/2$.

TYPICAL TEMPERATURE PERFORMANCE (−20° < T_A < +70°C)

Function	Typical Change	Units
Input Bias Current (αV_{in})	+40	pA/°C
Total Harmonic Distortion (V _{CC} = 6.0 V, R _L = 32 Ω , P _{out} = 125 mW, f = 1.0 kHz)	+0.003	%/°C
Power Supply Current (V _{CC} = 3.0 V, R _L = ∞ , CD = 0 V) (V _{CC} = 3.0 V, R _L = ∞ , CD = 2.0 V)	−2.5 −0.03	μ A/°C

DESIGN GUIDELINES

GENERAL

The MC34119 is a low power audio amplifier capable of low voltage operation (V_{CC} = 2.0 V minimum) such as that encountered in line-powered speakerphones. The circuit provides a differential output (VO1–VO2) to the speaker to maximize the available voltage swing at low voltages. The differential gain is set by two external resistors. Pins FC1 and FC2 allow controlling the amount of power supply and noise rejection, as well as providing alternate inputs to the amplifiers. The CD pin permits powering down the IC for muting purposes and to conserve power.

AMPLIFIERS

Referring to the block diagram, the internal configuration consists of two identical operational amplifiers. Amplifier #1 has an open loop gain of ≥80 dB (at f ≤ 100 Hz), and the closed loop gain is set by external resistors R_f and R_i. The amplifier is unity gain stable, and has a unity gain frequency of approximately 1.5 MHz. In order to adequately cover the telephone voice band (300–3400 Hz), a maximum closed loop gain of 46 dB is recommended. Amplifier #2 is internally set to a gain of −1.0 (0 dB).

The outputs of both amplifiers are capable of sourcing and sinking a peak current of 200 mA. The outputs can typically swing to within ≈0.4 volts above ground, and to within ≈1.3 volts below V_{CC}, at the maximum current. See Figures 18 and 19 for V_{OH} and V_{OL} curves.

The output dc offset voltage (VO1–VO2) is primarily a function of the feedback resistor (R_f), and secondarily due to the amplifiers' input offset voltages. The input offset voltage of the two amplifiers will generally be

similar for a particular IC, and therefore nearly cancel each other at the outputs. Amplifier #1's bias current, however, flows out of V_{in} (Pin 4) and through R_f, forcing VO1 to shift negative by an amount equal to [R_f × I_B]. VO2 is shifted positive an equal amount. The output offset voltage specified in the Electrical Characteristics is measured with the feedback resistor shown in the Typical Application Circuit, and therefore takes into account the bias current as well as internal offset voltages of the amplifiers. The bias current is constant with respect to V_{CC}.

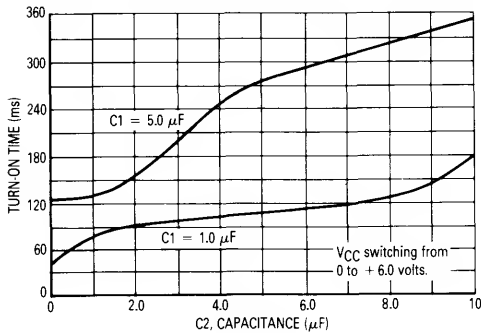
FC1 and FC2

Power supply rejection is provided by the capacitors (C1 and C2 in the Typical Application Circuit) at FC1 and FC2. C2 is somewhat dominant at low frequencies, while C1 is dominant at high frequencies, as shown in the graphs of Figures 4–7. The required values of C1 and C2 depend on the conditions of each application. A line powered speakerphone, for example, will require more filtering than a circuit powered by a well regulated power supply. The amount of rejection is a function of the capacitors, and the equivalent impedance looking into FC1 and FC2 (listed in the Electrical Characteristics as R_{FC1} and R_{FC2}).

In addition to providing filtering, C1 and C2 also affect the turn-on time of the circuit at power-up, since the two capacitors must charge up through the internal 50 k Ω and 125 k Ω resistors. The graph of Figure 1 indicates the turn-on time upon application of V_{CC} of +6.0 volts. The turn-on time is ≈60% longer for V_{CC} = 3.0 volts, and ≈20% less for V_{CC} = 9.0 volts. Turn-off time is <10 μ s upon removal of V_{CC}.

MC34119

FIGURE 1 — TURN-ON TIME versus C1, C2 AT POWER-ON



CHIP DISABLE

The Chip Disable (Pin 1) can be used to power down the IC to conserve power, or for muting, or both. When at a Logic "0" (0 to 0.8 volts), the MC34119 is enabled for normal operation. When Pin 1 is at a Logic "1" (2.0 to V_{CC} volts), the IC is disabled. If Pin 1 is open, that is equivalent to a Logic "0," although good design practice dictates that an input should never be left open. Input impedance at Pin 1 is a nominal 90 k Ω . The power supply current (when disabled) is shown in Figure 15.

Muting, defined as the change in differential gain from normal operation to muted operation, is in excess of 70 dB. The turn-off time of the audio output, from the application of the CD signal, is <2.0 μ s, and turn-on time is 12–15 ms. Both times are independent of C1, C2, and V_{CC} .

When the MC34119 is disabled, the voltages at FC1 and FC2 do not change as they are powered from V_{CC} . The outputs, VO1 and VO2, change to a high impedance condition, removing the signal from the speaker. If signals from other sources are to be applied to the outputs (while disabled), they must be within the range of V_{CC} and Ground.

POWER DISSIPATION

Figures 8–10 indicate the device dissipation (within the IC) for various combinations of V_{CC} , R_L , and load

power. The maximum power which can safely be dissipated within the MC34119 is found from the following equation:

$$P_D = (140^\circ\text{C} - T_A)/\theta_{JA}$$

where T_A is the ambient temperature;

and θ_{JA} is the package thermal resistance (100°C/W for the standard DIP package, and 180°C/W for the surface mount package.)

The power dissipated within the MC34119, in a given application, is found from the following equation:

$$P_D = (V_{CC} \times I_{CC}) + (I_{RMS} \times V_{CC}) - (R_L \times I_{RMS}^2)$$

where I_{CC} is obtained from Figure 15;

and I_{RMS} is the RMS current at the load;

and R_L is the load resistance.

Figures 8–10, along with Figures 11–13 (distortion curves), and a peak working load current of ≈ 200 mA, define the operating range for the MC34119. The operating range is further defined in terms of allowable load power in Figure 14 for loads of 8.0 Ω , 16 Ω , and 32 Ω . The left (ascending) portion of each of the three curves is defined by the power level at which 10% distortion occurs. The center flat portion of each curve is defined by the maximum output current capability of the MC34119. The right (descending) portion of each curve is defined by the maximum internal power dissipation of the IC at 25°C. At higher ambient temperatures, the maximum load power must be reduced according to the above equations. Operating the device beyond the current and junction temperature limits will degrade long term reliability.

LAYOUT CONSIDERATIONS

Normally a snubber is not needed at the output of the MC34119, unlike many other audio amplifiers. However, the PC board layout, stray capacitances, and the manner in which the speaker wires are configured, may dictate otherwise. Generally the speaker wires should be twisted tightly, and be not more than a few inches in length.

9

TYPICAL CHARACTERISTICS

FIGURE 2 — AMPLIFIER #1 OPEN LOOP GAIN AND PHASE

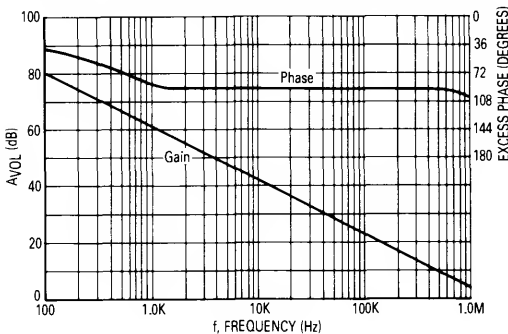
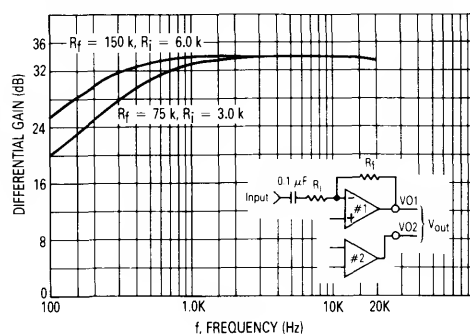
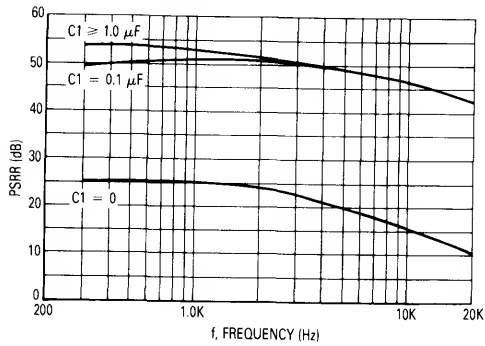
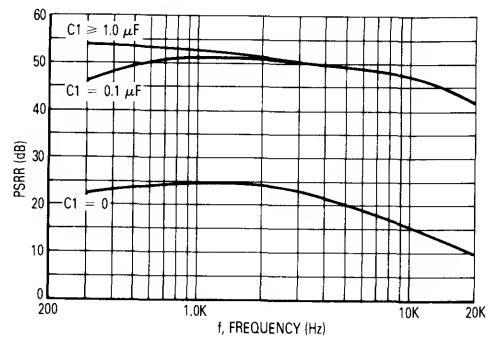
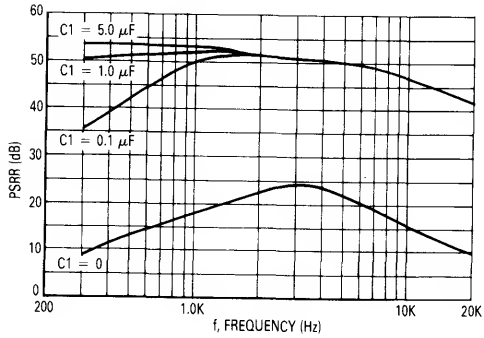
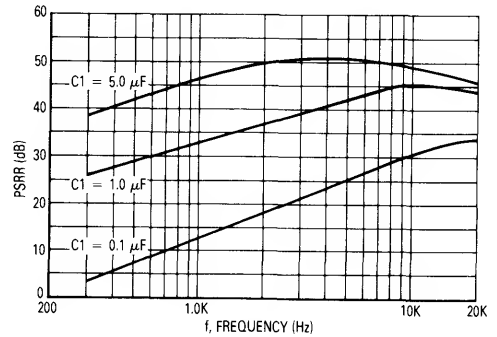


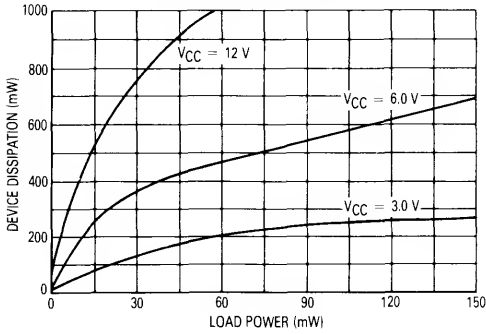
FIGURE 3 — DIFFERENTIAL GAIN versus FREQUENCY



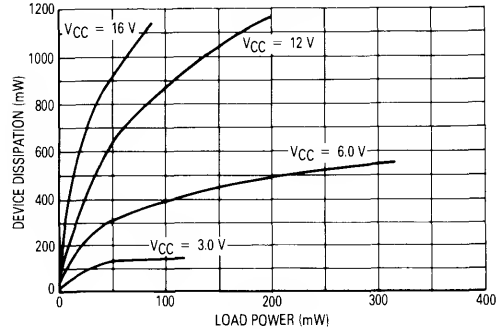
POWER SUPPLY REJECTION versus FREQUENCY

FIGURE 4 — $C_2 = 10 \mu F$ FIGURE 5 — $C_2 = 5.0 \mu F$ FIGURE 6 — $C_2 = 1.0 \mu F$ FIGURE 7 — $C_2 = 0$ 

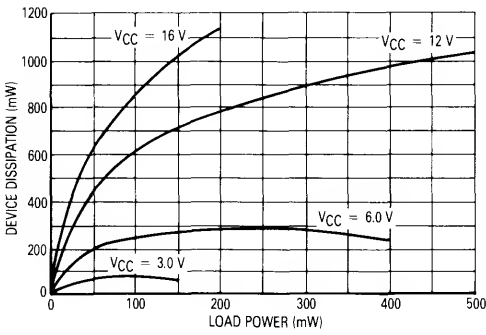
**FIGURE 8 — DEVICE DISSIPATION
8.0 Ω LOAD**



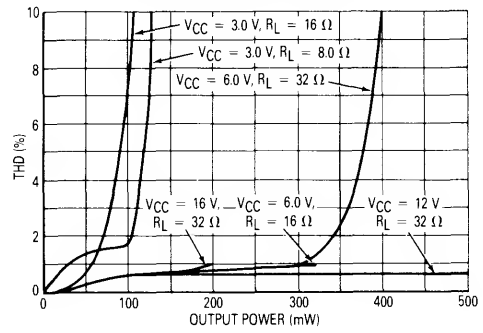
**FIGURE 9 — DEVICE DISSIPATION
16 Ω LOAD**



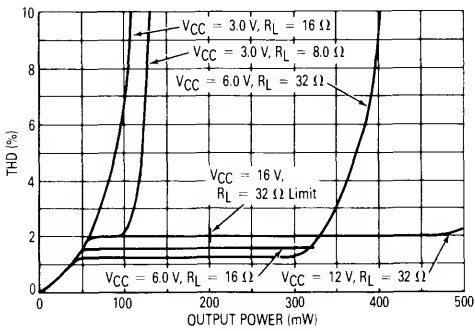
**FIGURE 10 — DEVICE DISSIPATION
32 Ω LOAD**



**FIGURE 11 — DISTORTION versus POWER
 $f = 1.0$ kHz, AVD = 34 dB**



**FIGURE 12 — DISTORTION versus POWER
 $f = 3.0$ kHz, AVD = 34 dB**



**FIGURE 13 — DISTORTION versus POWER
 $f = 1, 3.0$ kHz, AVD = 12 dB**

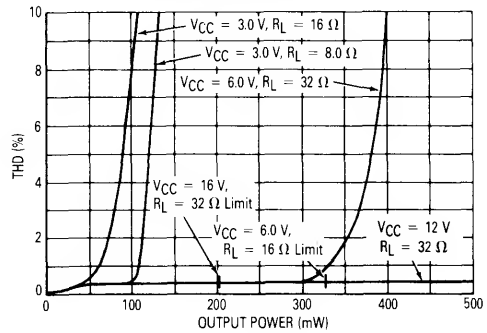


FIGURE 14 — MAXIMUM ALLOWABLE LOAD POWER

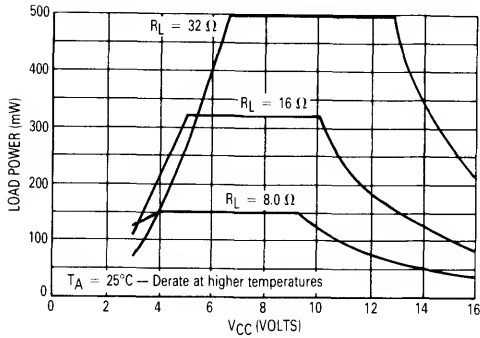


FIGURE 15 — POWER SUPPLY CURRENT

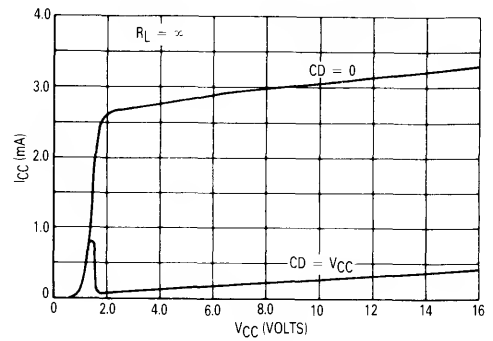


FIGURE 16 — SMALL SIGNAL RESPONSE

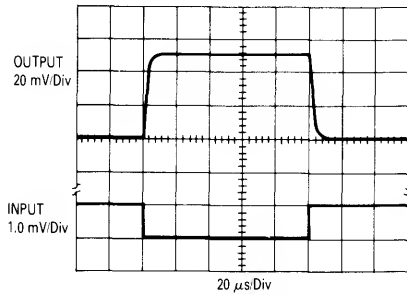
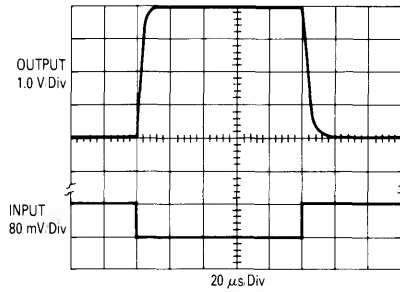
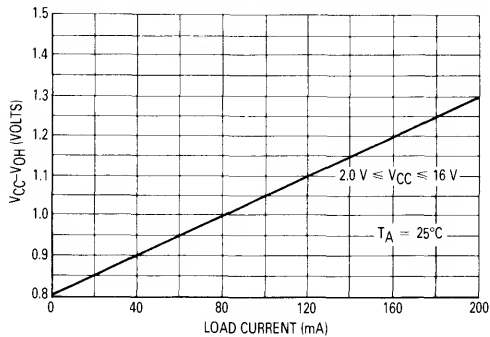
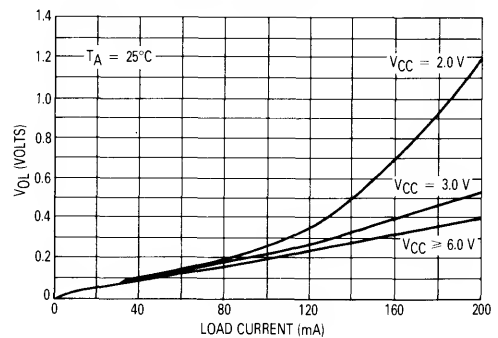


FIGURE 17 — LARGE SIGNAL RESPONSE

FIGURE 18 — $V_{CC}-V_{OH}$ @ $VO1, VO2$ versus LOAD CURRENTFIGURE 19 — V_{OL} @ $VO1, VO2$ versus LOAD CURRENT

MC34119

FIGURE 20 — INPUT CHARACTERISTICS @ CD (PIN 1)

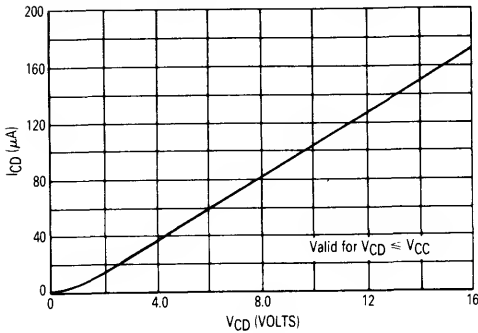


FIGURE 21 — AUDIO AMPLIFIER WITH HIGH INPUT IMPEDANCE

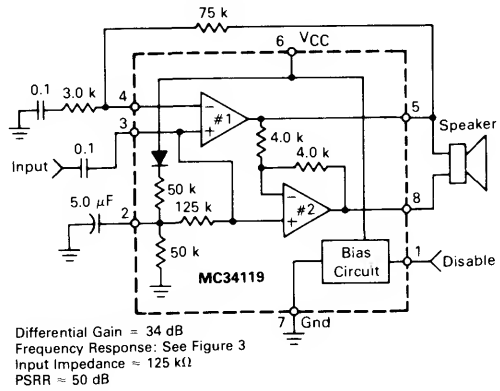


FIGURE 22 — AUDIO AMPLIFIER WITH BASS SUPPRESSION

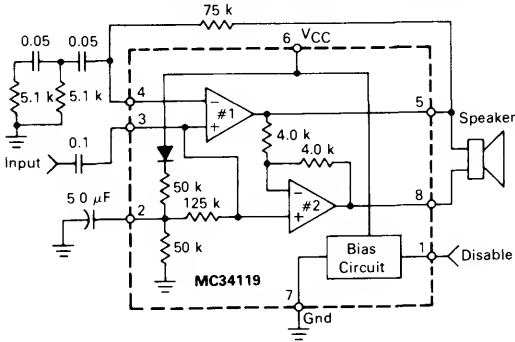


FIGURE 23 — FREQUENCY RESPONSE OF FIGURE 22

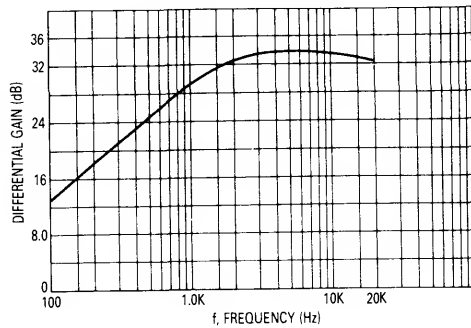


FIGURE 24 — AUDIO AMPLIFIER WITH BANDPASS

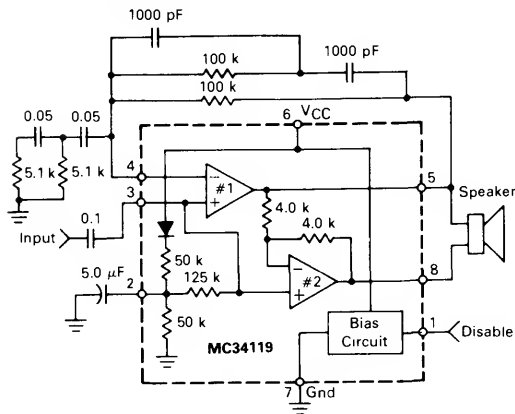
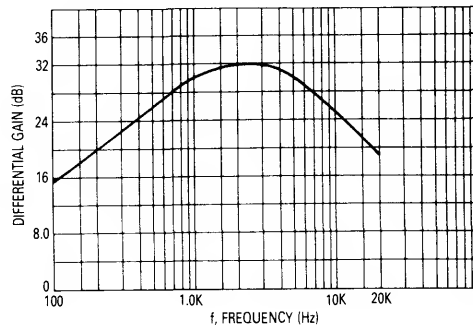
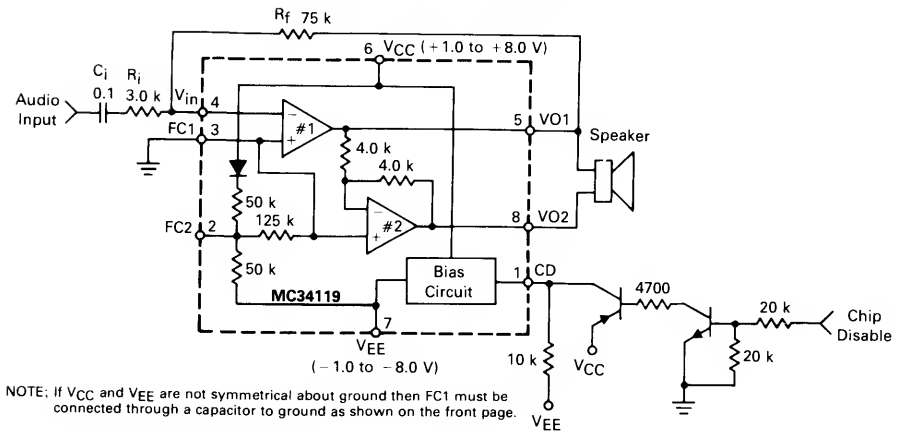


FIGURE 25 — FREQUENCY RESPONSE OF FIGURE 24



MC34119

FIGURE 26 — SPLIT SUPPLY OPERATION



MC44301

Product Preview

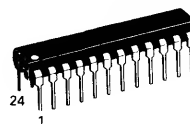
SYSTEM 4 HIGH PERFORMANCE COLOR TV IF

The MC44301 is a single channel TV IF and PLL detector system for all standard transmission systems. This device enables the designer to produce a high quality IF system with white spot inversion, AFT and AGC. The MC44301 was designed with an emphasis on linearity to minimize sound/picture intermodulation.

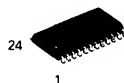
- Single Coil Adjustment for AFT and PLL
- VCO at 1/2 IF for Minimum Beats
- Simple Circuitry for Low System Cost
- White Spot Inversion
- Symmetrical ± 2.0 MHz Pull-In
- Detects Positive or Negative Modulation
- Auxiliary AM Detector for AM Sound
- Simple Alignment Procedure

SYSTEM 4 HIGH PERFORMANCE COLOR TV IF

SILICON MONOLITHIC INTEGRATED CIRCUIT

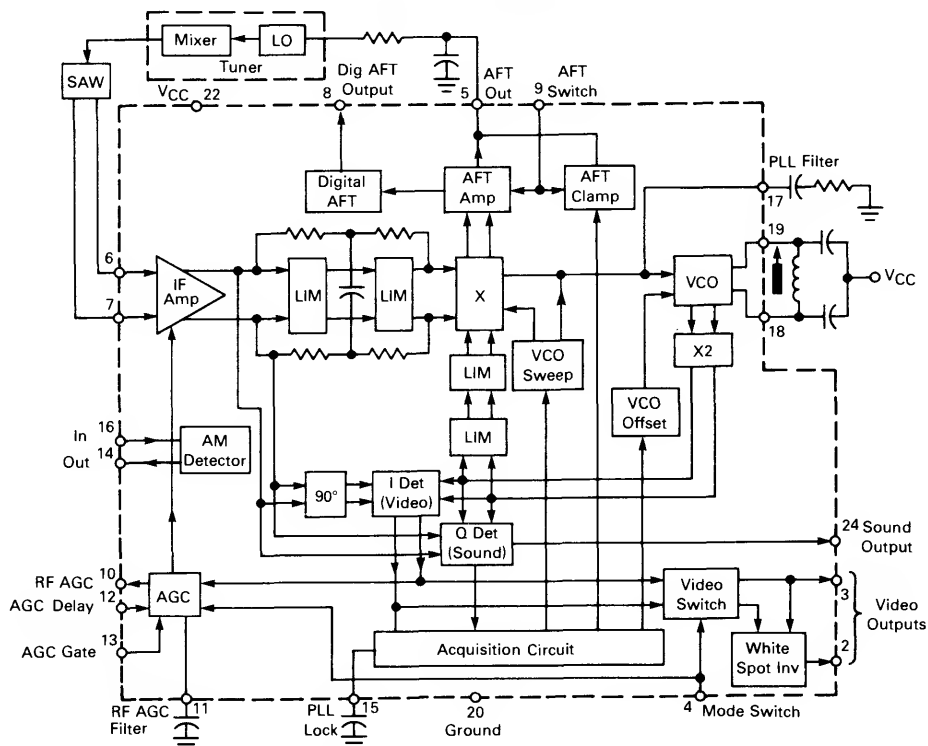


P SUFFIX
PLASTIC PACKAGE
CASE 724



DW SUFFIX
PLASTIC PACKAGE
CASE 751E
(SO-24L)

FIGURE 1 — BLOCK DIAGRAM



This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MOTOROLA LINEAR/INTERFACE DEVICES

9

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0 \text{ Vdc}$, $T_A = 25^\circ\text{C}$ unless noted)

FIGURE 2 — TEST CIRCUIT



CIRCUIT DESCRIPTION

Design Aims

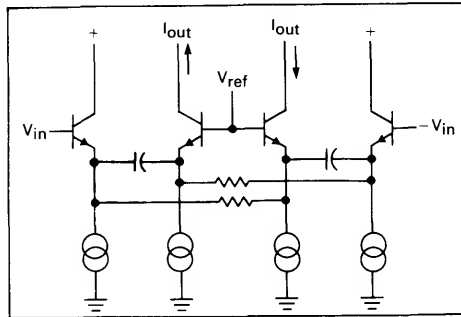
The MC44301 performs the functions of IF amplification, AGC, AFT and demodulation of a TV IF signal for both positive and negative modulation systems. In this respect it is similar to other circuits already on the market. However, in the means of obtaining these functions the MC44301 is very different compared to traditional designs. A unique approach was needed for several reasons. Tuned circuits associated with the IF amplifier output had to be eliminated to enable the part to be easy to use with the minimum of adjustments and external components. With this approach a high degree of IF stability could be obtained with a reduction in cost. Secondly, new techniques were required to improve performance in certain critical areas (differential phase and gain, etc.). This was especially so in view of the removal of the above mentioned tuned circuits. The basic idea therefore, was to produce an advanced, high performance multistandard IF system which would be economical and easy to use. Such a device can successfully compete with the already established IF amplifiers now available.

System Description

Despite the extra complications compared to pseudo synchronous demodulation, true synchronous demodulation seemed to be the only way in which enhanced performance could be achieved. The basic system is shown in Figure 1 in block diagram form. The IF amplifier is a four stage, AC coupled design having a sensitivity of about $20 \mu\text{V}$. With a low loss SAW filter and 3.0 to 6.0 dB extra gain in the tuner, there is no need for a SAW preamp. The TV set signal to noise performance is acceptable, while the net savings in cost is considerable. The AGC is a conventional gated system with the usual RF AGC output and RF AGC adjustment. Three stages of the amplifier are gain controlled to give an extended AGC range of 80 dB with improved intermodulation, signal handling, and differential phase and gain performance. The AGC reference is switched when positive modulation is selected, via the mode switch, to ensure the video level remains constant. Under these circumstances the AGC must be gated by a pulse which will sample the back porch, as opposed to negative modulation where flyback can be used. In both cases a positive or negative-going pulse may be used. To ensure that the improvements in performance mentioned above were not lost elsewhere, great care was taken in the design of the video demodulator and video amplifiers. An example of this care is the placing of the phase shift required by the video demodulator on the signal side instead of on the oscillator side of the demodulator as is common practice. The 90° phase shift is produced by replacing the usual emitter resistors by capacitors in the differential amplifier (Figure 3) feeding the video demodulator. The output currents are 90° with respect to the input voltage over a wide band of frequencies and the small phase errors caused by the tran-

sistor small signal emitter resistances (r_e) are corrected by the cross-coupled resistors. This arrangement leads to a simpler design, the ability to adjust the demodulation angle, and lower distortion than is normal at the IF amplifier/demodulator interface. The dynamic emitter resistances, which can give rise to distortion, are now in quadrature with the capacitive reactance and, therefore, contribute very little to the resultant output.

FIGURE 3 — 90° PHASE SHIFT AMPLIFIER



Following the IF amplifier and preceding the PLL phase detector is a two stage limiter with a gain of 100 and overall dc feedback. This contrasts with the usual single stage of limiting with no dc feedback and a tuned circuit with diodes at its output. With two stages of limiting, the minimum gain required to remove signal amplitude modulation can be designed-in without the large voltage swings of a single stage with the same gain. Large voltage swings lead to poor differential phase and gain performance, hence the need for a tuned circuit and diodes as used in previous designs. The dc feedback removes the effects of input offsets which are another source of differential phase and gain problems. The combination of low swing per stage and dc feedback removes the need for having a tuned circuit at the output of the limiter and reduces the danger of IF instability and radiation. The only problem in using this technique is the potential for extra static phase shift and resultant errors in the demodulating angles at the video and sound demodulators. However, by putting a similar two stage limiter, with matching phase shift, on the oscillator side of the phase detector, the demodulating angles can be restored to the correct phases (0° , 90°). Having processed the signal in this way, the VCO is then phase locked at 90° to the nonlimited signal. The only unusual feature of the loop just described is that the VCO runs at half frequency, and is frequency doubled on-chip. This means radiation from the external frequency determining components will be at "half IF" and so will not desensitize the system even if picked up by the amplifier input leads (this could cause what is known as PLL push-off). Running the oscillator at twice IF frequency and dividing down, which is another way of

solving this problem has several disadvantages. First and foremost, radiation into the antenna at twice IF produces channel 6 and channel 8 problems in the USA. Secondly, it is easier to produce a stable VCO at half IF.

After attaining phase lock, demodulation of the video is achieved by multiplying the signal (nonlimited) with the regenerated vision carrier (VCO) in a double balanced multiplier, the phase relationship between the two waveforms being zero degrees. Both positive and negative sync video outputs are produced.

FIGURE 4 — PIN 2 VIDEO OUTPUT WITH WHITE SPOT INVERSION

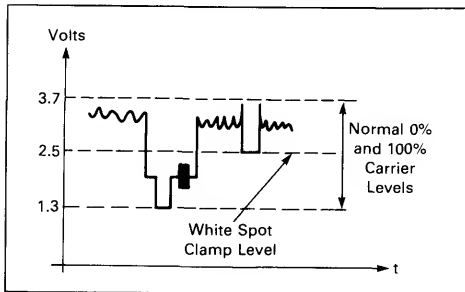
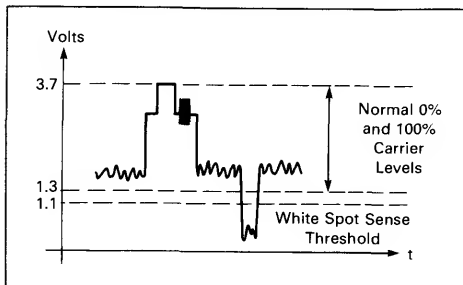


FIGURE 5 — PIN 3 VIDEO OUTPUT FOR DRIVE TO A SYNC SEPARATOR



The negative sync output is intended to be used as the actual video and is acted upon by the white spot noise inverter. This effectively removes the "whiter than white" noise produced by a true synchronous demodulator and prevents the CRT from being over driven and defocused. The positive sync video output is not acted on by a white spot noise inverter and of course the noise output from a synchronous detector does not contain a dc component. Hence, this drive should be used as the sync separator drive because a simple pre-separator low pass noise filter will produce optimum sync performance. Note the sense of the video signals at the outputs remain the same whether positive or negative modulation is being received. Positive or negative modulation is selected externally by the mode switch pin. The sound intercarrier is recovered by

another demodulator similar to the video, except that the phase relationship between the signal and the VCO is 90° instead of 0° . A consequence of this phase relationship is that video interference of the intercarrier signal at the detector output is minimized by suppression of the lower frequency video components. Should the sound carrier contain amplitude information, as in the French TV system or as in some scrambled cable signals, this information can be recovered by feeding the sound intercarrier output back into the circuit through a bandpass filter if so desired, to the amplitude detector provided on chip.

The AFT portion of the circuit is the most unconventional in form. Essentially, AFT is derived by amplifying the error signal driving the VCO after phase lock, and applying this to the local oscillator in the tuner, thus eliminating a coil and a potential IF instability problem. After acquisition, and when the circuit has settled down, due to the much higher gain in the LO loop, the VCO will have moved a small amount (Δf_v) from its nominal frequency, and almost all the original error frequency (Δf_e) between LO and VCO will have been corrected by the change in LO frequency (Δf_l). In this way, provided the PLL can be initially locked to the incoming IF signal, the VCO can be used as the frequency reference for the AFT system. It follows from the above therefore, because the system is phase locked, that $\Delta f_e = (\Delta f_l + \Delta f_v)$. The combination of the local VCO loop and the loop produced by feedback to the LO forms a double loop PLL. Analysis shows that overall system stability can be assured by treating the VCO loop as a stand alone PLL, provided its bandwidth is much wider than the LO loop. The VCO loop therefore is a low gain wide-band loop which guarantees initial capture, while the LO loop is basically a high gain dc loop used to keep frequency and phase offsets to a minimum. Large phase offsets can also be caused by dc offsets in the phase detector and AFT amplifier. These are removed by the use of commutation on both the phase and AFT outputs. This eliminates the need for external phase adjustment, while at the same time minimizing distortion by maintaining the correct phase angles at the demodulators.

The AFT system has been designed to acquire the vision carrier, without false locking to the sound or adjacent sound carriers, with an initial LO frequency error of ± 2.0 MHz, reducing this initial error to 3.0 to 10 kHz when locked. This contrasts to the discriminator type of AFT's which have highly asymmetric lock characteristics (-2.0 MHz $+ 1.0$ MHz), because of the effects of the IF filter, and large frequency errors caused by limited loop gain. To achieve this level of performance without encountering the normal AFT problems associated with high loop gain, a novel approach has been taken to locking up to the PLL. In the absence of an IF signal, the acquisition circuitry examines the state of the video (I) and sound (Q) demodulators and detects the lack of a signal. It then clamps the LO drive to a reference dc level and applies a -2.0 MHz offset to the VCO. This is done so that the nominal IF (should a signal appear), and the VCO, are sitting in the center of the IF filter passband. Therefore, even if the LO drifts high by $+2.0$

MHz, the signal will not be significantly attenuated by the filter. When the acquisition circuit detects the appearance of a signal, beat notes are produced at the output of the demodulators, a sweep generator is switched on, and immediately sweeps the VCO an additional -2.0 MHz from its out of lock nominal frequency.

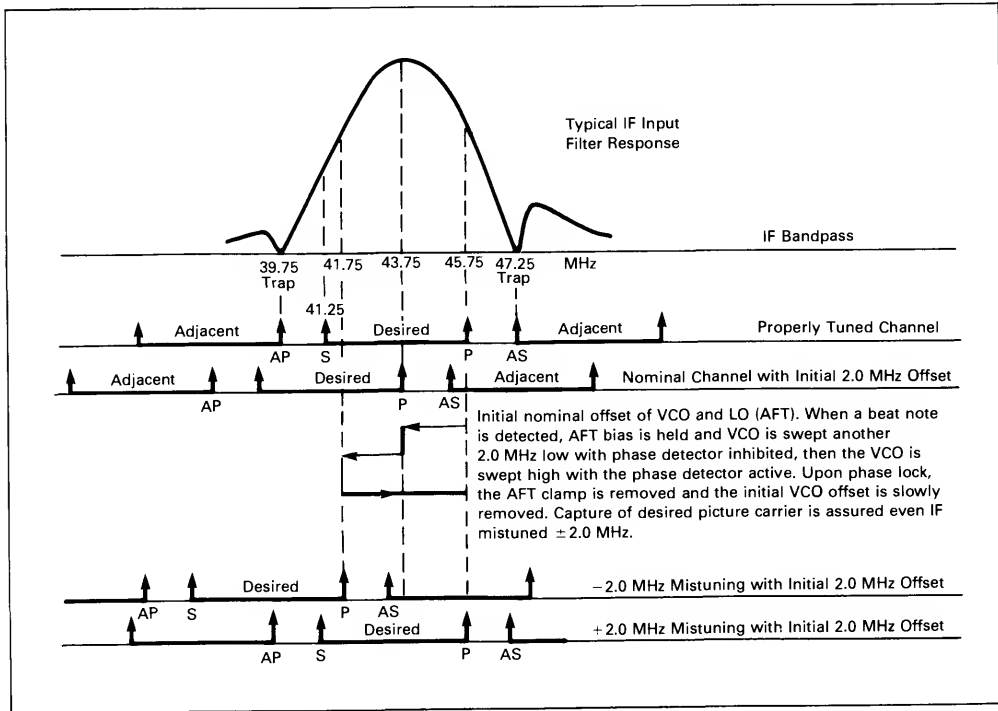
During this negative sweep, the PLL phase detector is switched off so phase lock cannot be obtained. The VCO is then swept positive from -2.0 MHz to $+2.0$ MHz of nominal with the phase detector switched on. The PLL will therefore lock to the first carrier it encounters. This in fact must be the vision carrier because the sound carrier is more negative than -2.0 MHz from nominal and the adjacent sound carrier is higher than the vision carrier. On achieving phase lock, the AFT clamp is released, the VCO offset is slowly removed, the sweep is inhibited and the phase detector remains enabled. With the AFT clamp removed, a large error voltage appears at the AFT output, driving the system back towards the correct frequency. Since the LO loop is slow and the VCO is fast, the IF changes slowly and the VCO tracks it, maintaining phase lock until the final static conditions are reached. For large frequency errors during this period the slew rate of the LO loop is increased,

but not to the extent where it would cause any VCO tracking problems. This technique allows the acquisition time of the circuit to be considerably shortened while still using a larger than normal time constant in the LO loop. To accommodate all types of tuners and LO's, positive or negative LO drive can be selected externally by operation of the AFT switch. The AFT switch also has a third position which disconnects the drive to the tuner. Under this condition the TV set can be tuned in the normal manner and so appears to have a conventional type of AFT. Other PLL AFT systems cannot be manually tuned in this way having an abrupt capture characteristic when tuned, and because of this, have not gained general acceptance in industry.

ALIGNMENT

The alignment is very simple and inexpensive compared to other IF amplifier circuits, especially those using a PLL. With a CW input signal of correct picture carrier frequency, the LO side of the 22 k resistor in series with the loop is connected to a dc supply. The dc supply (approximately 2.5 V) is adjusted until the output of the tuner is 45.75 MHz. The VCO coil is adjusted until lock is obtained and the voltage across the 22 k resistor

FIGURE 6 — THE AFT SYSTEM IN ACTION



MC44301

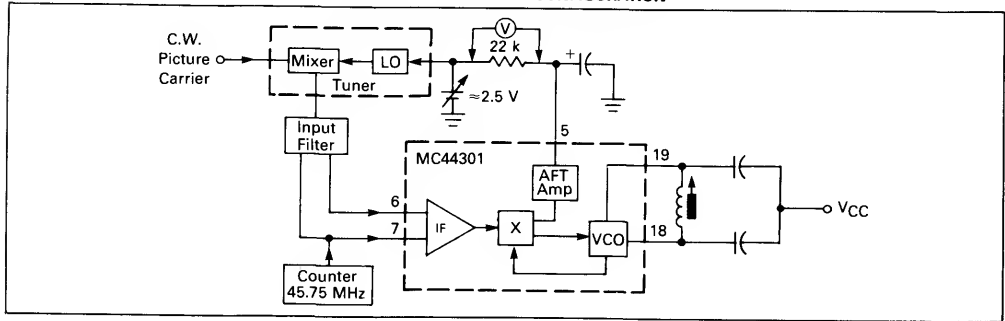
is zero. The dc supply is then removed.

A digital AFT up/down output having a ± 30 kHz dead zone is also provided by the circuit. Again, as in the case of the analog output, the digital output polarity can be controlled externally by the AFT switch.

Note:

Most pins on the IC have electrostatic protection diodes to V_{CC} and ground. It is therefore imperative that no pin is taken below ground or above V_{CC} by more than one diode drop without current limiting.

FIGURE 7 — ALIGNMENT CONFIGURATION



MC44802

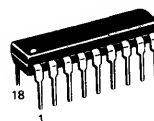
PLL TUNING CIRCUIT WITH 1.3 GHz PRESCALER

The MC44802 is a tuning circuit for TV applications. It contains, on one chip, all the functions required for PLL control of a VCO. This integrated circuit also contains a high frequency prescaler (which can be bypassed by software control) and thus can handle frequencies up to 1.3 GHz.

The MC44802 is manufactured on a single silicon chip using Motorola's high density bipolar, MOSAIC (Motorola Oxide Self Aligned Implanted Circuits) process.

- Complete Single Chip System for MPU Control (I²C Bus)
- Selectable Divide-by-8 Prescaler Accepts Frequencies up to 1.3 GHz
- 15-Bit Programmable Divider Accepts Input Frequencies up to 165 MHz
- Programmable Reference Divider
- Tri-State Phase/Frequency Comparator
- Op Amp for Direct Tuning Voltage Output (33 V)
- Seven High Current Output Buffers (10 mA, 12 V)
- Output Options for 62.5 kHz, Reference Frequency and the Programmable Divider
- Software Compatible with MC44810

PLL TUNING CIRCUIT WITH 1.3 GHz PRESCALER



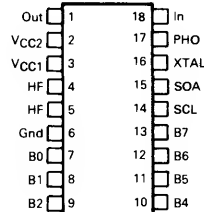
P SUFFIX
 PLASTIC PACKAGE
 CASE 707



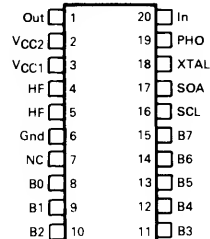
DW SUFFIX
 PLASTIC PACKAGE
 CASE 751D
 (SO-20L)

PIN ASSIGNMENTS

18 PIN DIP



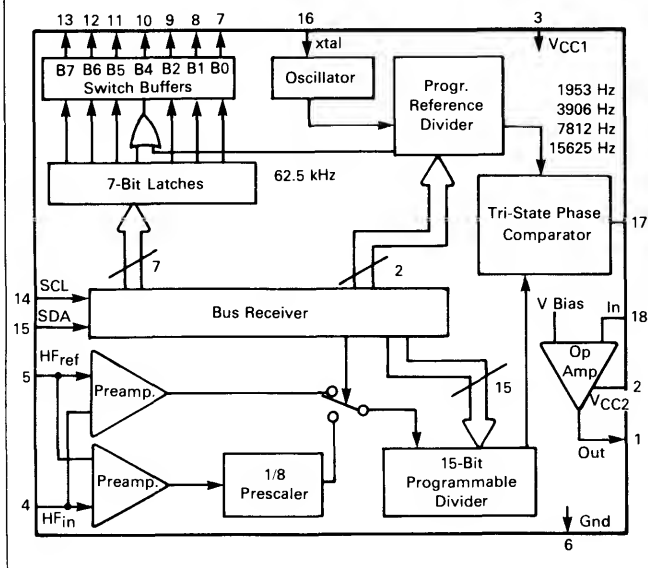
SO-20L



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC44802P	0°C to 70°C	18-Pin DIP
MC44802DW		20-Pin SOIC

SIMPLIFIED BLOCK DIAGRAM



MOSAIC is a trademark of Motorola Inc.

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Ratings	Pin	Value	Unit
Power Supply Voltage V_{CC1}	3	6.0	V
Band Buffer "OFF" Voltage	7 to 13	15	V
Band Buffer "ON" Current	7 to 13	15	mA
Op Amp Power Supply Voltage V_{CC2}	2	36	V
Op Amp Short Circuit Duration (0 to V_{CC2})	1	Continuous	V
Storage Temperature		-65 to +150	$^\circ\text{C}$
Operating Temperature Range		0 to +70	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($V_{CC1} = 5.0\text{ V}$, $V_{CC2} = 32\text{ V}$, $T_A = 25^\circ\text{C}$ unless otherwise specified)

Characteristic	Pin	Min	Typ	Max	Unit
V_{CC1} Supply Voltage Range	3	4.5	5.0	5.5	V
V_{CC1} Supply Current ($V_{CC1} = 5.0\text{ V}$) (Note 1)	3	—	60	90	mA
V_{CC2} Supply Voltage Range	2	25	30	35	V
V_{CC2} Supply Current (Output Open)	2	—	0.8	2.0	mA
Band Buffer Leakage Current When "OFF" at 12 V	7 to 13	—	0.01	1.0	μA
Band Buffer Saturation Voltage When "ON" at 10 mA	7 to 13	—	0.6	1.0	V
Data/Clock Current at 0 V	14, 15	-10	—	0	μA
Clock Current at 5.0 V	14	0	—	1.0	μA
Data Current at 5.0 V Acknowledge "OFF"	15	0	—	1.0	μA
Data Saturation Voltage at 15 mA Acknowledge "ON"	15	—	—	1.0	V
Data/Clock Input Voltage Low	14, 15	—	—	1.5	V
Data/Clock Input Voltage High	14, 15	3.0	—	—	V
Clock Frequency Range	14	0	—	100	kHz
Phase Detector Tri-State Current	17	-15	0	15	nA
Phase Detector High-State Source Current ($I_{OH} 1.5\text{ V}$)	17	-3.0	-2.2	-1.5	mA
Phase Detector Low-State Sink Current ($I_{OL} 3.5\text{ V}$)	17	2.0	3.0	4.0	mA
Op Amp Internal Reference Voltage	—	2.0	—	3.0	V
Op Amp Input Current	18	-15	0	15	nA
DC Open Loop Gain	—	5000	—	—	
Gain Bandwidth Product ($R_L = 10\text{ k}$, $C_L = 20\text{ pF}$)	—	0.3	—	—	MHz
Phase Margin ($R_L = 10\text{ k}$, $C_L = 20\text{ pF}$)	—	50	—	—	Deg.
V_{out} Low, Sinking 50 μA	1	—	0.1	0.3	V
V_{out} High, Sourcing 50 μA , $V_{out} - V_{CC2}$	1	-4.0	-3.0	—	V
V_{CC1} Supply Ripple Rejection (See Figure 1a)	—	—	-54	-45	dB

HF CHARACTERISTICS (See Figure 1b)

HF In/Ref DC Bias	4, 5	—	1.6	—	V
HF Voltage Range Prescaler "OFF" 10–150 MHz	5	20	—	1500	mVrms
HF Voltage Range Prescaler "ON" 50–950 MHz	5	30	—	1500	mVrms
HF Voltage Range Prescaler "ON" 950–1300 MHz	5	50	—	1000	mVrms

NOTE

1. When prescaler "OFF," typical supply current is decreased by 20 mA.

MC44802

FIGURE 1a — RIPPLE REJECTION — MEASUREMENT SCHEMATIC

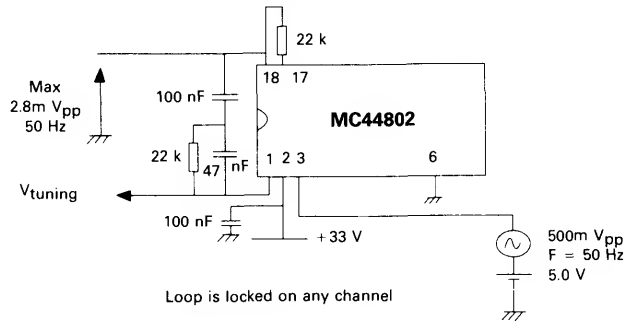


FIGURE 1b — HF SENSITIVITY TEST CIRCUIT

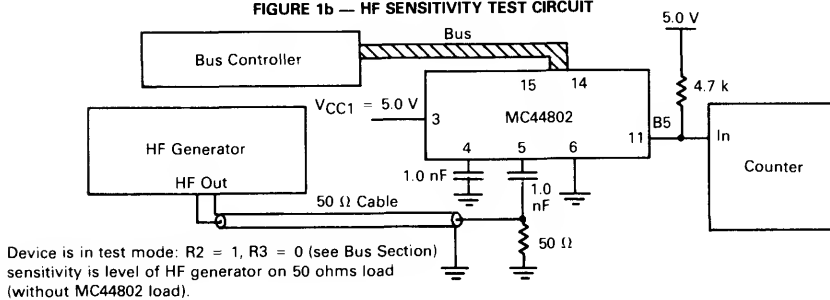
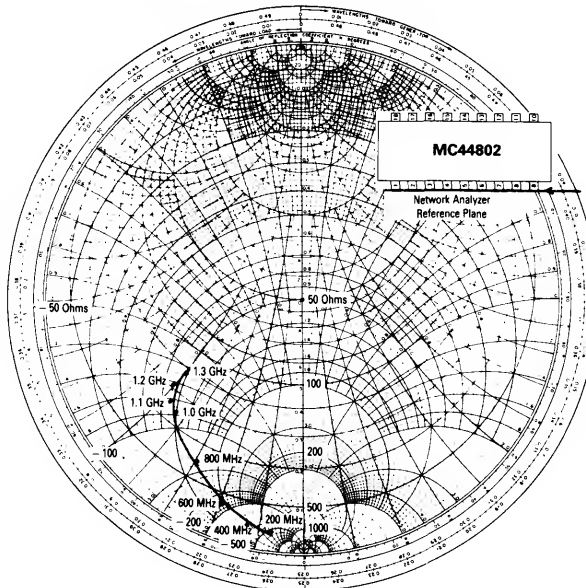


FIGURE 2 — PIN 5 INPUT IMPEDANCE (TYP)

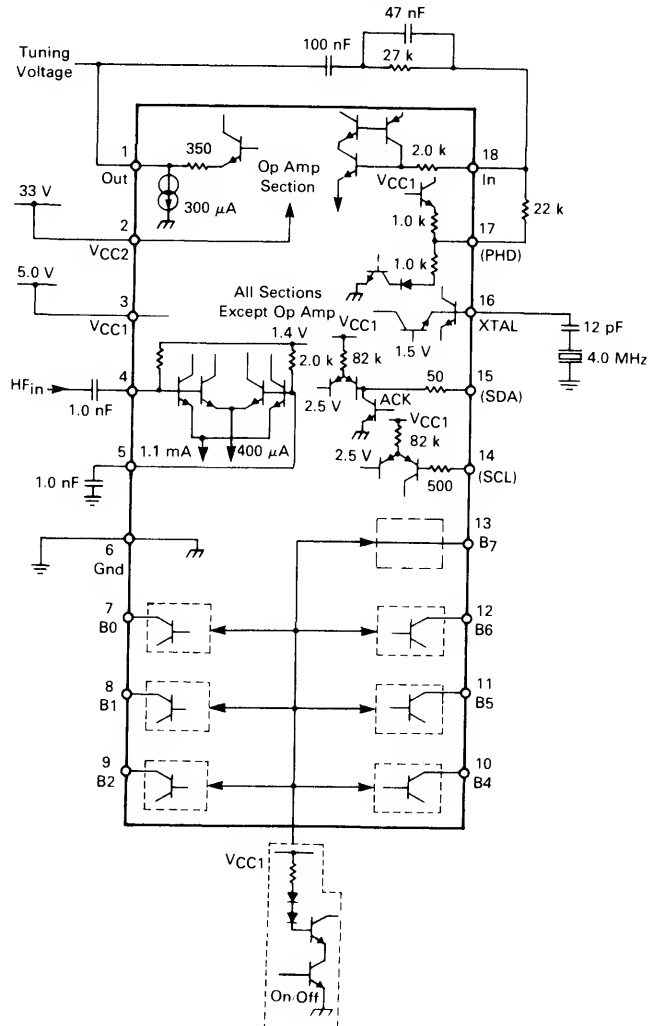


MC44802

PIN FUNCTION DESCRIPTION (See Figure 3a)

Pin	Function	Description
1	Out	Operational amplifier output which provides the tuning voltage
2	VCC2	Operational amplifier positive supply
3	VCC1	Positive supply of the circuit (except op amp)
4	HF _{in}	HF inputs from local oscillator
5	HF _{ref}	
6	Gnd	
7, 8, 9, 10, 11, 12, 13	B0, B1,.....B7	Ground
14	SCL	Band buffer output can drive up to 10 mA
15	SDA	Clock Input (supplied by the microprocessor via I ² C Bus)
16	XTAL	Data Input (I ² C Bus)
17	PHD	Crystal Input (Typ: 4.0 MHz)
18	In	Phase Comparator Output
	In	Negative Operational Amplifier Input

FIGURE 3a — PIN CIRCUIT SCHEMATIC FOR MC44802P

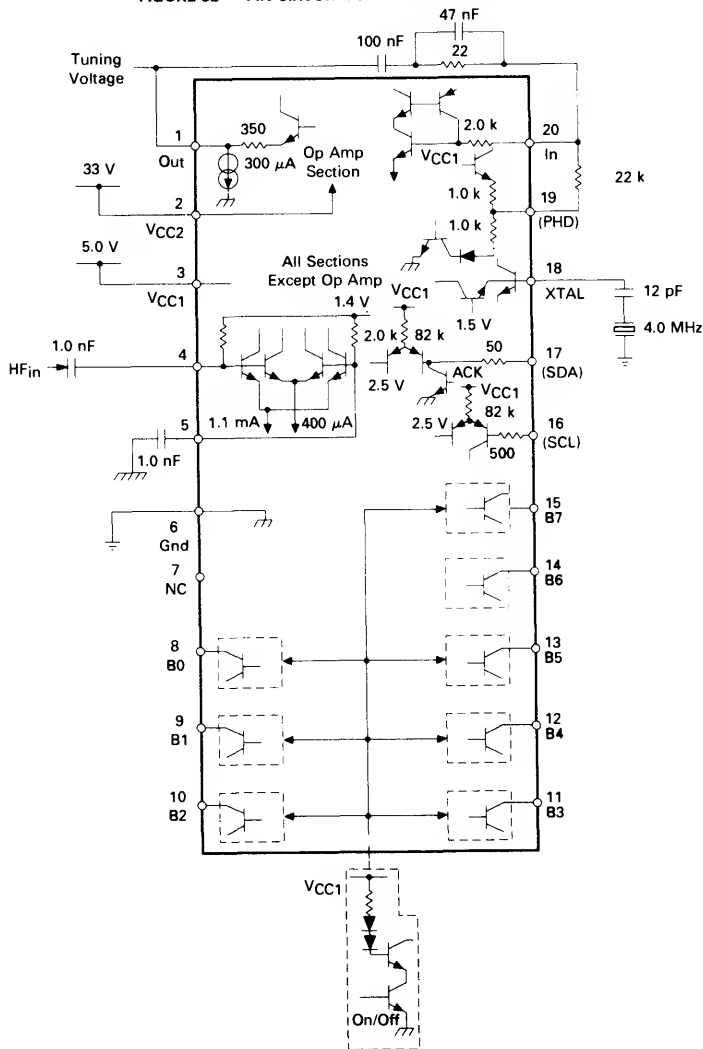


MC44802

PIN FUNCTION DESCRIPTION FOR MC44802DW (See Figure 3b)

Pin	Function	Description
1	Out	Operational amplifier output which provides the tuning voltage
2	VCC2	Operational amplifier positive supply
3	VCC1	Positive supply of the circuit (except op amp)
4	HF _{in}	HF inputs from local oscillator
5	HF _{ref}	
6	Gnd	
7	NC	Ground
8, 9, 10, 11, 12, 13, 14, 15	B0, B1.....B7	No Connection
16	SCL	Band buffer output can drive up to 10 mA
17	SDA	Clock Input (supplied by the microprocessor via I ² C Bus)
18	XTAL	Data Input (I ² C Bus)
19	PHD	Crystal Input (Typ: 4.0 MHz)
20	In	Phase Comparator Output
	In	Negative Operational Amplifier Input

FIGURE 3b — PIN CIRCUIT SCHEMATIC FOR MC44802DW



FUNCTIONAL DESCRIPTION

A representative block diagram and a typical system application are shown in Figures 4 and 5. A discussion

of the features and function of each of the internal blocks is given below.

FIGURE 4 — BLOCK DIAGRAM (18 PIN)

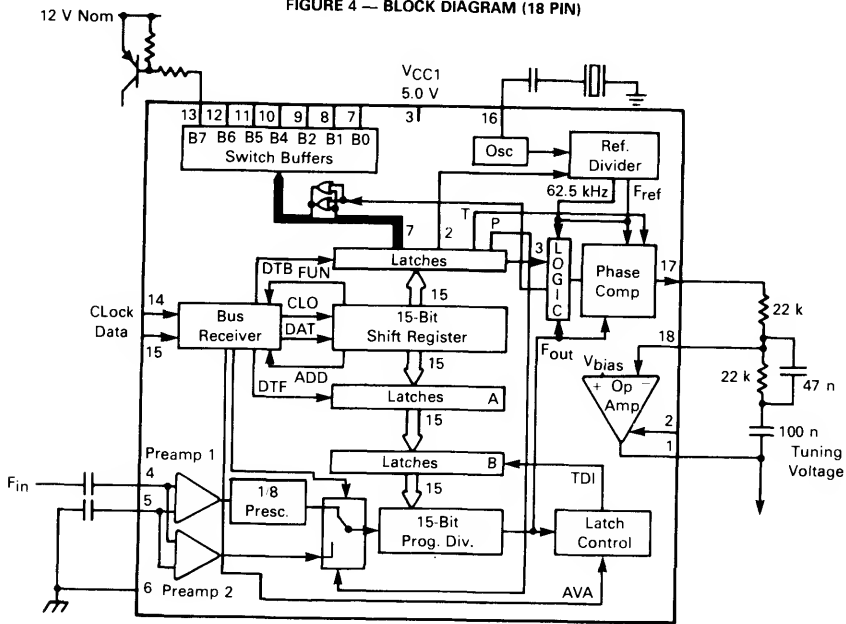
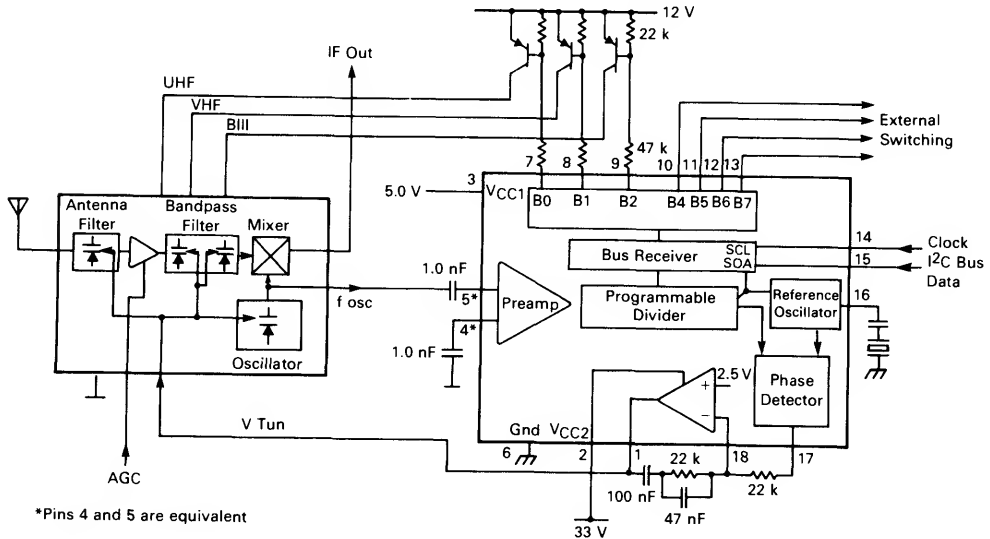


FIGURE 5 — TYPICAL TUNER APPLICATION



DATA FORMAT AND BUS RECEIVER

The circuit receives the information for tuning and control via the I²C Bus. The incoming information, consisting of a chip address byte followed by two or four data bytes, is treated in the I²C Bus receiver. The definition of the permissible bus protocol is shown below:

```

1__STA  CA  CO  BA  STO
2__STA  CA  FM  FL  STO
3__STA  CA  CO  BA  FM   FL  STO
4__STA  CA  FM  FL  CO   BA  STO
  
```

STA = Start Condition
 STO = Stop Condition
 CA = Chip Address Byte
 CO = Data Byte for Control Information
 FM = Data Byte for Frequency Information (MSBs)
 FL = Data Byte for Frequency Information (LSBs)
 BA = Band Information

Frequency information is preceded by a Logic "0." If the function bit is Logic "1" the two following bytes contain control and band information where the bits have the following functions:

- Bit R0 and R1
Define the reference divider division ratio. Four ratios are available (see Table 1).
- Bit R2 and R3
Are used to switch internal signals to the buffer outputs. Pin 10 and 11 (see Table 2).
- Bit R2, R6 and T
Are used to control the phase comparator output stage (see Table 3).
- Bit P
Switches the prescaler in and out. At Logic "1" the prescaler is bypassed and the power supply of the prescaler is switched off.

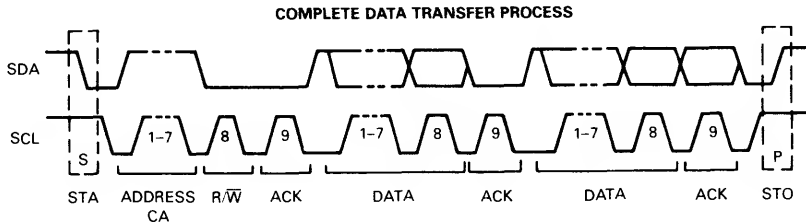


Figure 6 shows the five bytes of information that are needed for circuit operation: there is the chip address, two bytes of control and band information and two bytes of frequency information.

After the chip address, two or four data bytes may be received: if three data bytes are received the third data byte is ignored.

If five or more data bytes are received the fifth and following data bytes are ignored and the last acknowledge pulse is sent at the end of the fourth data byte.

The first and the third data bytes contain a function bit which allow the IC to distinguish between frequency information and control plus band information.

FIGURE 6 — DEFINITION OF BYTES

CA__Chip Address	1	1	0	0	0	0	1	0	ACK
CO__Information	1	R6	T	P	R3	R2	R1	R0	ACK
BA__Band Info.	B7	B6	B5	B4	X	B2	B1	B0	ACK
FM__Frequency Info.	0	N14	N13	N12	N11	N10	N9	N8	ACK
FL__Frequency Info.	N7	N6	N5	N4	N3	N2	N1	B0	ACK

TABLE 1

Input Data		Reference Divider
R1	R0	Division Ratio
0	0	2048
0	1	1024
1	0	512
1	1	256

TABLE 2

Input Data		Test Outputs on Buffers	
R2	R3	Pin 10	Pin 11
0	0	—	—
0	1	62.5 kHz	—
1	0	F _{ref}	FBY2
1	1	—	—

Bit B4 has to be "zero" when Pin 10 is used to output 62.5 kHz.

Bit 4 and B5 have to "zero" to output F_{ref} and FBY2. FBY2 is the programmable divider output frequency divided by two.

TABLE 3

Input Data			Output State of the Phase Comparator
R2	R6	T	
0	0	0	Normal Operation
0	0	1	Off (High Impedance)
0	1	0	High
0	1	1	Low
1	0	0	Normal Operation
1	0	1	Off
1	1	0	Normal Operation
1	1	1	Off

THE BAND BUFFERS

BA_Band Information

20 Pin Version

B7	B6	B5	B4	B3	B2	B1	B0	ACK
----	----	----	----	----	----	----	----	-----

18 Pin Version

B7	B6	B5	B4	X	B2	B1	B0	ACK
----	----	----	----	---	----	----	----	-----

The band buffers are open collector transistors and are active "low" at $B_n = 1$. They are designed for 10 mA with a typical on-resistance of 70 ohms. These buffers are designed to withstand relative high output voltage in the off-state.

B4 and B5 buffers (Pins 10 and 11) may also be used to output internal IC signals (reference frequency and programmable divider output frequency divided by 2) for tests purposes.

Buffer B4 may also be used to output a 62.5 kHz frequency for an intermediate stage of the reference divider. The bit B4 and/or B5 have to be zero if the buffers are used for these additional functions.

THE PROGRAMMABLE DIVIDER

The programmable divider is a presettable down counter. When it has counted to zero it takes its required division ratio out of the latches B. Latches B are loaded from latches A by means of signal TDI which is synchronous to the programmable divider output signal.

Since latches A receive the data asynchronously with the programmable divider, this double latch scheme is needed to assure correct data transfer to the counter.

The division ratio definition is given by:

$$N = 16384 \times N14 + 8132 \times N13 + \dots + 4 \times N2 + 2 \times N1 + N0$$

Max Ratio 32767

Min Ratio 17

Where $N0, \dots, N14$ are the different bits for frequency information.

The counter may be used for any ratio between 17 and 32767 and reloads correctly as long as its output frequency does not exceed 1.0 MHz.

The data transfer between latches A and B (signal TDI) is also initiated by any start condition on the IIC bus.

At power-on the whole bus receiver is reset and the programmable divider is set to a counting ratio of $N = 256$ or higher.

THE PRESCALER

The prescaler has a preamplifier which guarantees high input sensitivity. The prescaler may be bypassed (Bit P) and the signal then passes through preamp 2.

THE PHASE COMPARATOR

The phase comparator is phase and frequency sensitive and has very low output leakage current in the high impedance state.

THE OPERATIONAL AMPLIFIER

The operational amplifier is designed for very low noise, low input bias current and high power supply rejection. The positive input is biased internally. The op amp needs 31 V supply (V_{CC2}) as minimum voltage for a guaranteed maximum tuning voltage of 28 V.

Figure 1 shows a possible filter arrangement. The component values depend very much on the application (tuner characteristic, reference frequency, etc.);

As a starting point for optimization, the components values in Figure 1 may be used for 7.8125 kHz reference frequency in a multiband TV tuner.

THE OSCILLATOR

The oscillator uses a 4.0 MHz crystal tied to ground or V_{CC1} through a capacitor, used in the series resonance mode.

The voltage at Pin 16, "crystal," has low amplitude and low harmonic distortion.

SYSTEM APPLICATION

Table 4 is a summary of the circuit applications using a 4.0 MHz crystal.

TABLE 4

Input Data R1 R0		Reference Divider Div. Ratio	Reference Frequency Hz (1)	With Internal Prescaler P = 0		Without Internal Prescaler P = 1	
				Frequency Steps kHz	Max. Input Frequency MHz	Frequency Steps kHz	Max. Input Frequency MHz
0	0	2048	1953.125	15.625	512	1.953125	64
0	1	1024	3906.25	31.25	1024	3.90625	128
1	0	512	7812.5	62.5	1300(2)	7.8125	165(3)
1	1	256	15625.0	125	1300(2)	15.625	165(3)

(1) With 4.0 MHz Crystal

(2) Limit of Prescaler

(3) Limit of Programmable Divider

TDA1524A

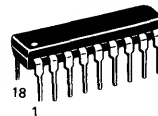
STEREO TONE CONTROL

The TDA1524A is an active balance, volume, bass and treble control for use in car radios, stereo TV receivers and audio systems. Functions are controlled by four non-critical single potentiometers with excellent channel to channel tracking characteristics. Bass and treble contours are defined by a single capacitor per control per channel. Volume control can be linear across the audio spectrum, or a loudness contour can be used.

- Low Noise
- Low Distortion
- High Signal Handling Capability
- Wide Supply Range
- Popular Multi-Sourced Device

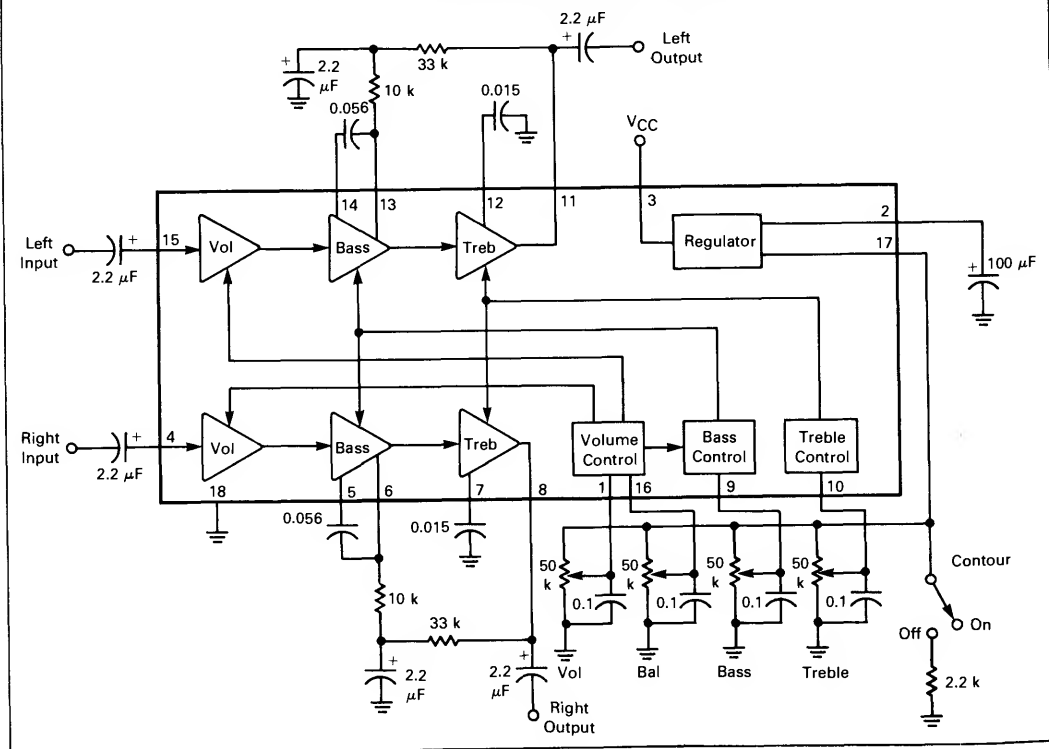
STEREO TONE CONTROL SYSTEM

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
 PLASTIC PACKAGE
 CASE 707

FIGURE 1 — BLOCK DIAGRAM AND TYPICAL APPLICATION



TDA1524A

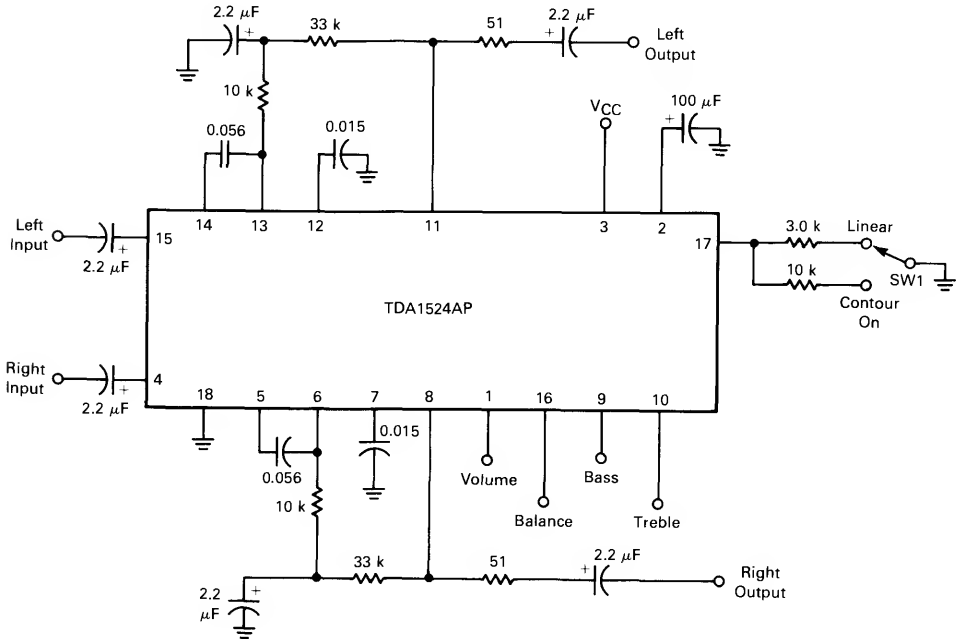
MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$)

Rating	Value	Units
Power Supply Voltage	20	V
Power Dissipation Derate above 25°C	1250 10	mW mW/ $^\circ\text{C}$
Operating Temperature Range	-40 to $+85$	$^\circ\text{C}$
Storage Temperature Range	-65 to $+150$	$^\circ\text{C}$

DC CHARACTERISTICS ($T_A = 25^\circ\text{C}$, circuit of Figure 2, SW1 at "contour on", $V_1, V_9, V_{10}, V_{16} = 1.9\text{ V}$, unless otherwise noted)

Characteristic	Pin	V_{CC} (Vdc)	Min	Typ	Max	Units
Supply Voltage, V_{CC}	3	—	7.5	—	16.5	Vdc
Supply Current	3	8.5 12 15	19 — —	27 35 43	35 — —	mA
DC Input Level	4, 15	8.5 12 15	3.8 — —	4.25 5.9 7.3	4.7 — —	Vdc
DC Output Level	8, 11	8.5 12 15	3.3 — —	4.25 6.0 7.5	5.2 — —	Vdc
Regulator Output Voltage	17	8.5 12 15	3.5 — —	3.75 3.8 3.85	4.0 — —	Vdc
Regulator Output Voltage, SW1 in "Linear" Position	17	8.5	3.5	3.75	4.0	Vdc

FIGURE 2 — TEST CIRCUIT



TDA1524A

AC CHARACTERISTICS ($V_{CC} = 8.5$ Vdc, $T_A = 25^\circ\text{C}$, circuit of Figure 2, contour switch (SW1) to "Linear" position, frequency 1.0 kHz, gains expressed as $20 \log [\text{voltage ratio}]$ unless otherwise noted)

Characteristic	V_1	V_9	V_{10}	V_{16}	Measure Pin(s)	Min	Typ	Max	Units
Gain at Max Volume Control (Input = 50 mVrms)	V_{17}	$\frac{V_{17}}{2}$	$\frac{V_{17}}{2}$	$\frac{V_{17}}{2}$	8, 11	20	20	24	dB
Distortion at 1.8 Vrms Output (Output signal handling)					8, 11	—	—	0.5	%
AC Input Resistance					4, 15	10	—	—	k Ω
Output to Output Separation, One Input Driven (100 mVrms)					8, 11	60	—	—	dB
Noise Output (20 Hz–20 kHz, Inputs are Grounded)					8, 11	—	250	400	μVrms
Gain at Mid Volume, Left Channel (Input = 100 mVrms)	$\frac{V_{17}}{2}$	$\frac{V_{17}}{2}$	$\frac{V_{17}}{2}$	$\frac{V_{17}}{2}$	8, 11	–12	–9.0	–6.0	dB
Gain Difference Left to Right						—	—	1.5	dB
70 Hz Gain Difference Output to Output (Input = 100 mVrms)	2.1	$\frac{V_{17}}{2}$	$\frac{V_{17}}{2}$	$\frac{V_{17}}{2}$	8, 11	—	—	2.5	dB
70 Hz Gain at Mid Bass Setting (Input = 100 mVrms)						—	0	—	dB
70 Hz Bass Control — Boost		V_{17}				10	—	—	dB
— Cut		0				10	—	—	dB
16 kHz Gain at Mid Treble Setting (Input = 100 mVrms)	2.1	$\frac{V_{17}}{2}$	$\frac{V_{17}}{2}$	$\frac{V_{17}}{2}$	8, 11	—	0	—	dB
16 kHz Gain Difference Output to Output						—	—	2.5	dB
16 kHz Treble Control — Boost			V_{17}			12	—	—	dB
— Cut			0			12	—	—	dB
Balance Control Range of Right Channel	2.1	$\frac{V_{17}}{2}$	$\frac{V_{17}}{2}$	Adj* $\frac{V_{17}}{2}$	8	35	—	—	dB
Balance Control Range of Left Channel				Adj* $\frac{V_{17}}{2}$	11	35	—	—	dB
Output Ripple (No Signal, 200 mVrms @ 120 Hz Added to V_{CC})				$\frac{V_{17}}{2}$	8, 11	—	—	3.5	mVrms
1.0 kHz Gain (Input = 1.8 Vrms)	1.6	$\frac{V_{17}}{2}$	$\frac{V_{17}}{2}$	$\frac{V_{17}}{2}$	8, 11	—	–20	—	dB
Noise Output (20 Hz–20 kHz, Inputs ac Grounded)						—	75	120	μVrms
Distortion (Input = 1.4 Vrms) (Input Signal Handling)	2.0					—	—	0.5	%
Distortion (Input = 1.8 Vrms)						—	—	0.7	%
1.0 kHz Gain (Input = 2.0 Vrms)	1.3	$\frac{V_{17}}{2}$	$\frac{V_{17}}{2}$	$\frac{V_{17}}{2}$	8, 11	—	–40	—	dB
Gain Difference Output to Output						—	—	6.0	dB
Contour Boost at 70 Hz (Contour Switch in "Contour On" Position)						8	—	—	dB
Gain at Minimum Volume (Input 2.0 Vrms)	0	$\frac{V_{17}}{2}$	$\frac{V_{17}}{2}$	$\frac{V_{17}}{2}$	8, 11	—	—	–70	dB

Adj* — means vary the control over the full range from V_{17} to 0.

(All curves taken in the test circuit of Figure 2, $V_{CC} = 8.5$ Vdc, unless otherwise noted)

FIGURE 3 — VOLUME CONTROL CHARACTERISTIC

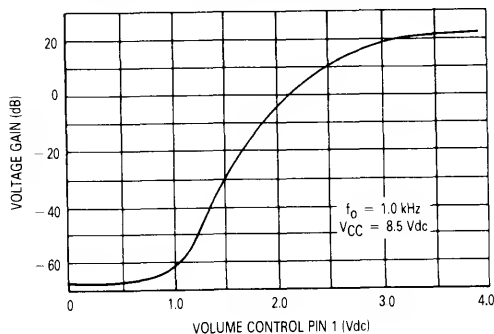


FIGURE 4 — BALANCE CONTROL CHARACTERISTIC

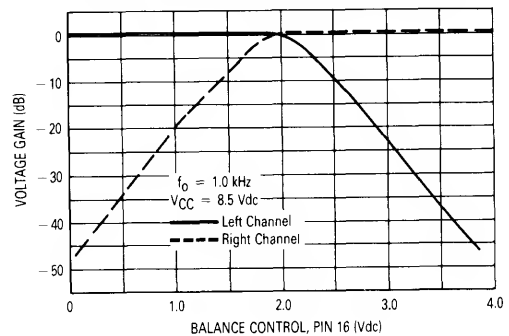


FIGURE 5 — BASS CONTROL CHARACTERISTIC

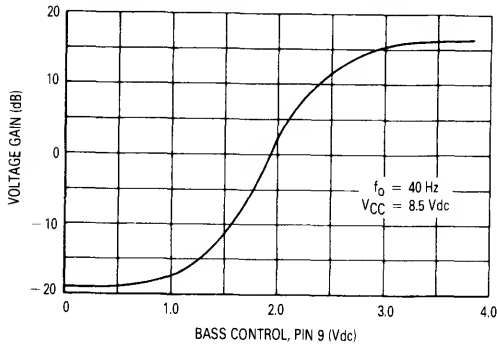


FIGURE 6 — TREBLE CONTROL CHARACTERISTIC

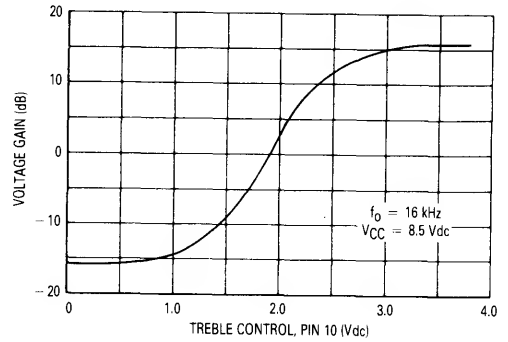


FIGURE 7 — TOTAL HARMONIC DISTORTION versus FREQUENCY

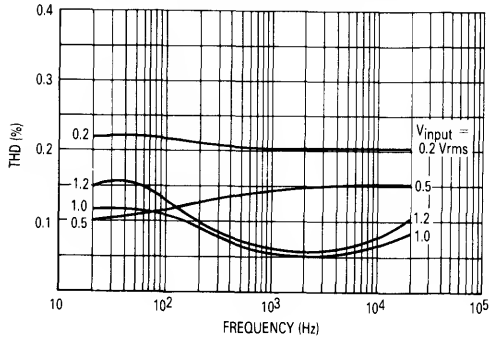


FIGURE 8 — TOTAL HARMONIC DISTORTION versus OUTPUT

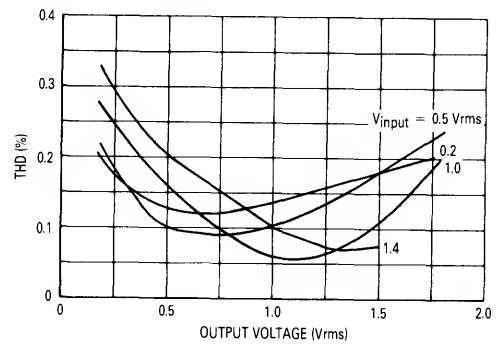


FIGURE 9 — TONE CONTROL RESPONSE WITH SINGLE POLE LOW-PASS FILTER

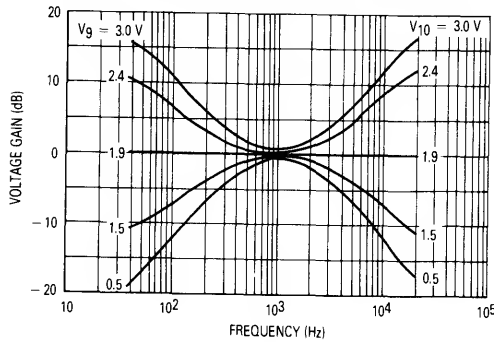
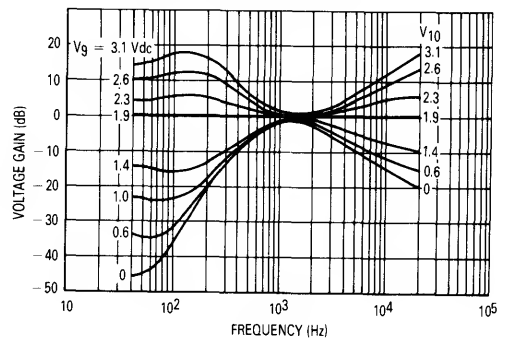


FIGURE 10 — TONE CONTROL RESPONSE WITH DOUBLE POLE LOW-PASS FILTER



TDA1524A

FIGURE 11 — SINGLE POLE LOW-PASS FILTER

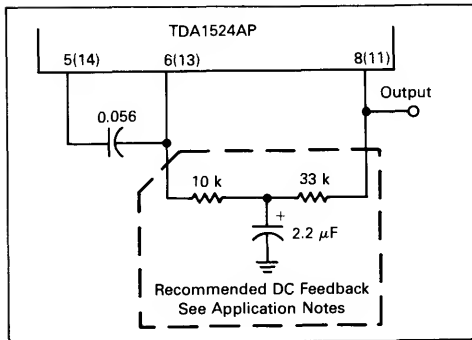


FIGURE 12 — DOUBLE POLE LOW-PASS FILTER

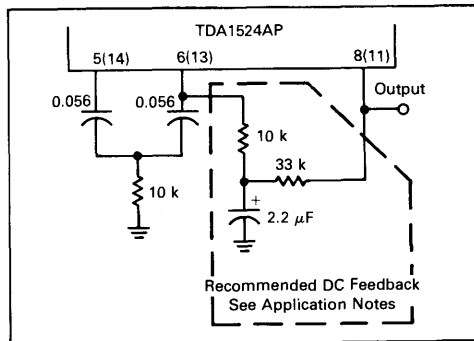


FIGURE 13 — VOLUME CONTROL RESPONSE WITH SINGLE POLE LOW-PASS FILTER

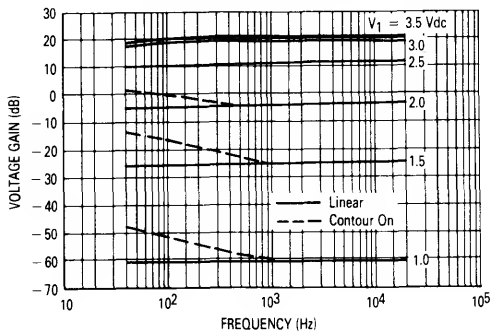


FIGURE 14 — VOLUME CONTROL RESPONSE WITH DOUBLE POLE LOW-PASS FILTER

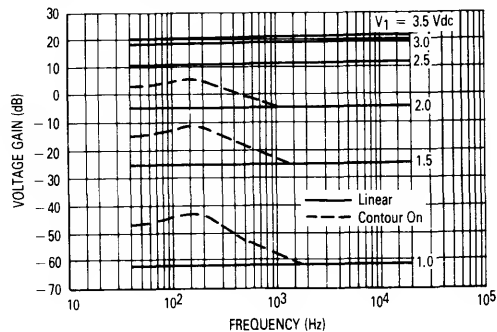
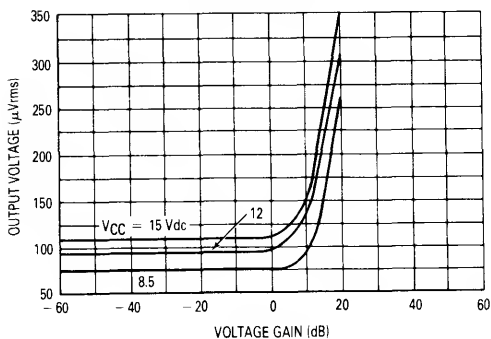


FIGURE 15 — NOISE OUTPUT VOLTAGE
(20 Hz to 20 kHz)



APPLICATION NOTES

The use of dc feedback stabilizes the dc output voltage at approximately $V_{CC}/2$ and assures large output swing capability without distortion. If this dc feedback is not used, the dc output will vary from part to part and available headroom will be somewhat reduced.

The loading of the regulator output, Pin 17 has an abrupt effect on switching the contour function and is not intended to be applied in any intermediate degree. The tests assure that the part is in linear mode for total loading of Pin 17 less than 3.0 k Ω , and is in contour mode for a total load on Pin 17 greater than 10 k Ω .

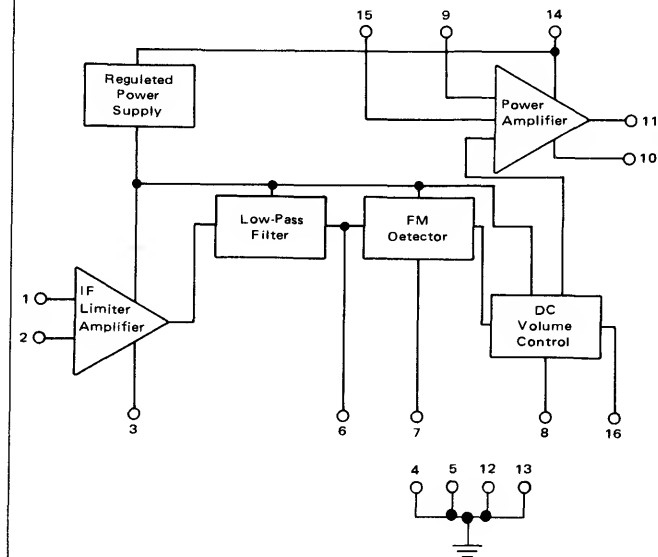
MOTOROLA SEMICONDUCTOR TECHNICAL DATA

TV SOUND SYSTEM

The TDA3190P 4.2-watt sound system is designed for television and related applications. Functions performed by this device includes: IF Limiting, IF amplifier, low pass filter, FM detector, DC volume control, audio preamplifier, and audio power amplifier.

- 4.2 Watts Output Power — TDA3190P
($V_{CC} = 24\text{ V}$, $R_L = 16\ \Omega$)
- Linear Volume Control
- High AM Rejection
- Low Harmonic Distortion
- High Sensitivity

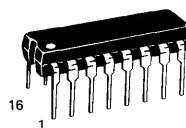
BLOCK DIAGRAM



TDA3190P

TV SOUND SYSTEM

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 648C

PIN CONNECTIONS

IF Input	1	16	Deemphasis
Decoupling	2	15	Ripple Rejection
Decoupling	3	14	Supply Voltage
Ground	4	13	Ground
Ground	5	12	Ground
Phase Shift	6	11	Output
Phase Shift	7	10	Compensation
DC Volume Control	8	9	Gain

TDA3190P

MAXIMUM RATINGS

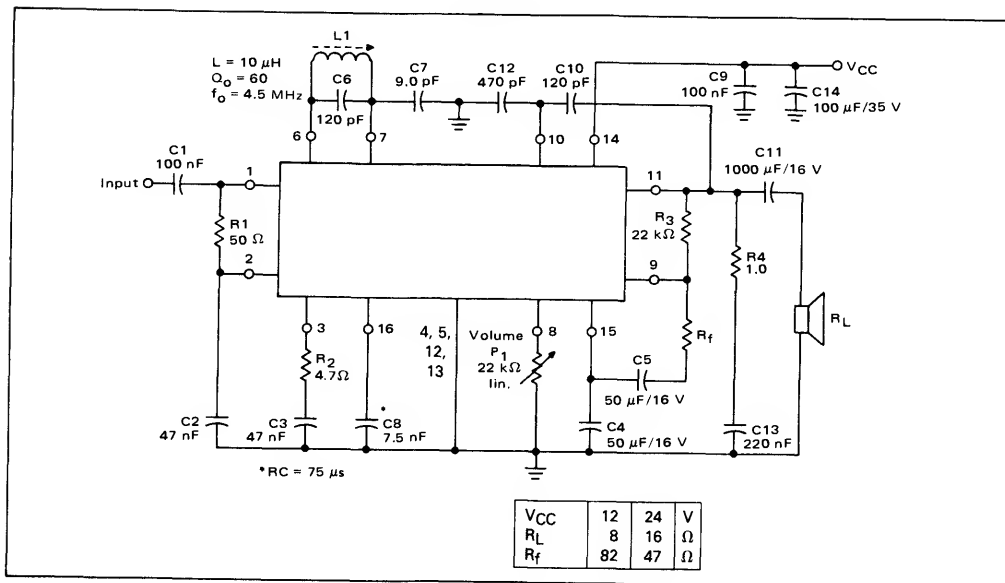
Rating	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	9.0 to 28	V
Output Peak Current (Nonrepetitive) (Repetitive)	I_o	2.0 1.5	A
Input Signal Voltage	V_i	1.0	V
Operating Temperature Range	T_A	0 to +75	°C
Junction Temperature	T_J	150	°C

ELECTRICAL CHARACTERISTICS ($V_{CC} = 24$ V, $f_o = 4.5$ MHz, $\Delta f = \pm 25$ kHz, $T_A = 25^\circ\text{C}$ unless otherwise noted.)

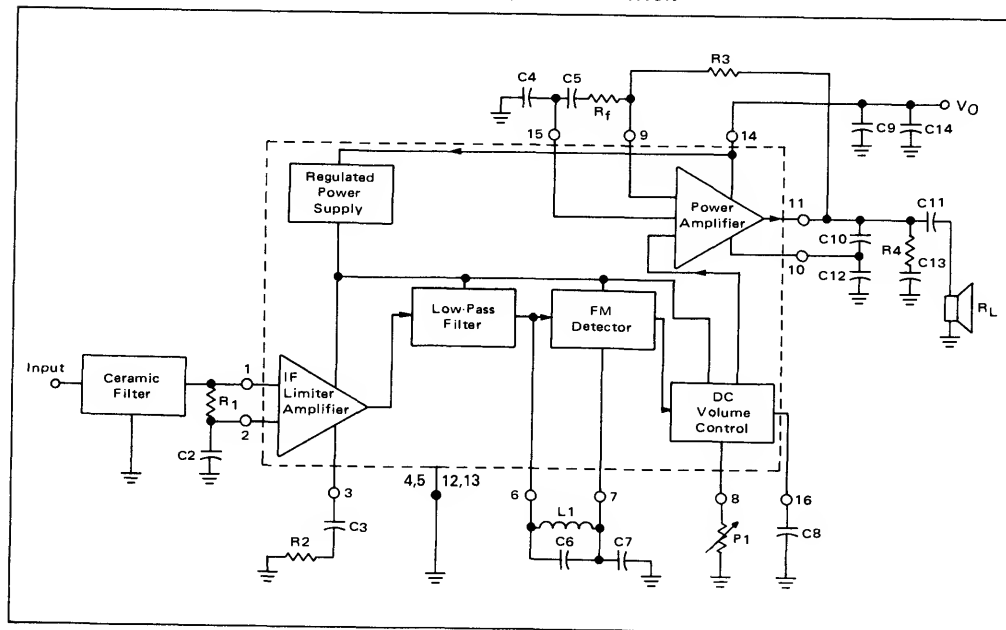
Characteristic	Symbol	Min	Typ	Max	Unit
Quiescent Output Voltage (Pin 11) $V_{CC} = 24$ V	V_O	11	12	13	V
Quiescent Drain Current ($P_1 = 22$ k Ω) $V_{CC} = 24$ V	I_D	11	22	35	mA
Output Power ($d = 10\%$, $f_m = 400$ Hz) $V_{CC} = 24$ V, $R_L = 16$ Ω $V_{CC} = 12$ V, $R_L = 8.0$ Ω ($d = 2\%$, $f_m = 400$ Hz) $V_{CC} = 24$ V, $R_L = 16$ Ω $V_{CC} = 12$ V, $R_L = 8.0$ Ω	P_O	— — — —	4.2 1.5 3.5 1.4	— — — —	W
Input Limiting Threshold Volts (-3.0 dB) at Pin 1 $\Delta f = \pm 7.5$ kHz, $f_m = 400$ Hz, set P_1 for 2.0 Vrms on Pin 11	V_i	—	40	100	μV
Distortion ($P_O = 50$ mW, $f_m = 400$ Hz, $\Delta f = \pm 7.5$ kHz) $V_{CC} = 24$ V, $R_L = 16$ Ω		—	0.75	—	%
Frequency Response of Audio Amplifier (-3.0 dB) ($R_L = 16$ Ω , $C_{10} = 120$ pF, $C_{12} = 470$ pF, $P_1 = 22$ k Ω) $R_f = 82$ Ω $R_f = 47$ Ω	B	— —	70 to 12 k 70 to 7.0 k	— —	Hz
Recovered Audio Voltage (Pin 16) ($V_i \geq 1.0$ mV, $f_m = 400$ Hz, $\Delta f = \pm 7.5$ kHz, $P_1 = 0$)	V_o	—	120	—	mV
Amplitude Modulation Rejection ($V_i \geq 1.0$ mV, $f_m = 400$ Hz, $m = 30\%$)	AMR	—	55	—	dB
Signal and Noise to Noise Ratio ($V_i \geq 1.0$ mV, $V_o = 4.0$ V, $f_m = 400$ Hz)	$\frac{S + N}{N}$	50	65	—	dB
Input Resistance (Pin 1) ($V_i = 1.0$ mV)	r_i	—	30	—	k Ω
Input Capacitance (Pin 1) ($V_i = 1.0$ mV)	C_i	—	5.0	—	pF
DC Volume Control Attenuation ($P_1 = 12$ k Ω)		—	90	—	dB

TDA3190P

TEST CIRCUIT



TYPICAL CIRCUIT CONFIGURATION



TDA3301B
TDA3303

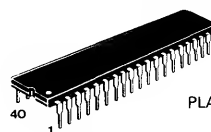
TV COLOR PROCESSOR

These devices will accept a PAL or NTSC composite video signal and output the three color signals, needing only a simple driver amplifier to interface to the picture tube. The provision of high bandwidth on-screen display inputs makes them suitable for text display, TV games, cameras, etc. The TDA3301B differs from the TDA3303 in its user control laws, and also a phase shift control which operates in PAL, as well as NTSC.

- Automatic Black Level Setup
- Beam Current Limiting
- Uses Inexpensive 4.43/3.58 MHz Crystal
- No Oscillator Adjustment Required
- Three OSD Inputs Plus Fast Blanking Input
- Four DC, High Impedance User Controls
- Interfaces with TDA3030B SECAM Adaptor
- Single 12 V Supply
- Low Dissipation, Typically 600 mW

TV COLOR PROCESSOR

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**



P SUFFIX
PLASTIC PACKAGE
CASE 711



FN SUFFIX
PLASTIC PACKAGE
CASE 777
(PLCC-44)

FIGURE 1 — PIN ASSIGNMENT

Chroma Input	1 (1)	(44) 40	Hue Control/NTSC Switch
ACC Capacitor	2 (2)	(43) 39	+ 12 V
Chroma DL Driver, Emitter	3 (3)	(42) 38	Ground
Chroma DL Driver, Collector	4 (4)	(41) 37	1.0 V Composite Video Input
Saturation Control	5 (5)	(40) 36	Delayed Luma Input
Identification Capacitor	6 (6)	(39) 35	Luma DL Drive and 3.0 Inverted Output
V Input	7 (10)	(38) 34	Luma Emitter Load
U Input	8 (11)	(37) 33	Luma Collector Load
90° Loop Capacitor	9 (12)	(36) 32	Contrast Control
Oscillator Loop Filter	10 (13)	(35) 31	Black Level Clamp
Crystal Drive	11 (14)	(34) 30	Brightness Control
Crystal Feedback	12 (15)	(33) 29	Peak Beam Limit Adjust
Ground	13 (16)	(32) 28	Frame Pulse Input
Blue Output	14 (18)	(31) 27	Sandcastle Pulse Input
Blue Output Clamp Capacitor	15 (19)	(30) 26	OSD Input Green
Blue Output Feedback	16 (20)	(29) 25	OSD Input Red
Green Output	17 (21)	(28) 24	OSD Input Blue
Green Output Clamp Capacitor	18 (22)	(27) 23	OSD Input Fast Blanking
Green Output Feedback	19 (23)	(26) 22	Red Output Feedback
Red Output	20 (24)	(25) 21	Red Output Clamp Capacitor

* () PLCC Pin Assignment

TDA3301B, TDA3303

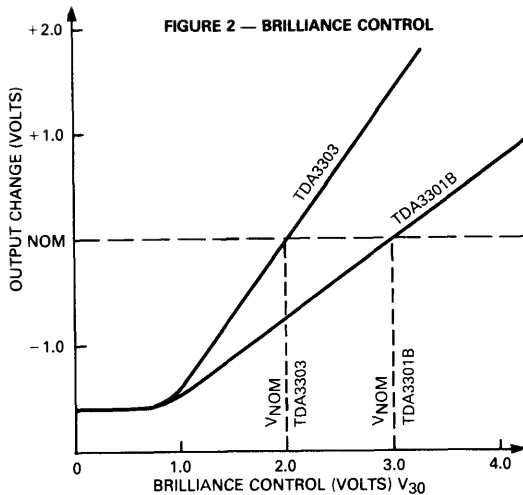
MAXIMUM RATINGS (T_A = +25°C unless otherwise stated)

Rating	Pin	Value	Unit
Supply Voltage	39	14	V _{dc}
Operating Temperature Range		0 to +70	°C
Storage Temperature Range		-65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 12 V)

Characteristic	Pin	Min	Typ	Max	Unit
Supply Voltage	39	10.8	12	13.2	V
Supply Current		—	45	60	mA
Composite Video Input	37	—	1.0	—	V _{p-p}
Video Input Resistance		13	18	23	kΩ
Video Gain to Pin 35		2.7	3.2	3.6	V _{p-p}
Input Window		0.8–3	0.7–3.2	—	V
Chroma Input (Burst)	1	10	100	200	mV _{p-p}
Input Resistance	1	—	5.0	—	kΩ
ACC Effectiveness	4	—	1.2	3.0	dB
OSD Input	24,25,26	0.5	0.7	1.0	V
OSD Drive Impedance		—	—	180	Ω
OSD Frequency Response (–3.0 dB)		9.0	—	—	MHz
OSD Max Gain		—	7.2	—	MHz
Gain Difference Between Any Two		—	—	15	%
Beam Current Ref. Threshold	16,19,22	1.7	2.0	2.3	V
Differential Voltage		—	—	20	mV
Beam Current Ref. Input Current		—	—	+1.5/–0.5	μA
Differential Current		—	—	1.0	μA
Luminance Gain Between Pin 36 and Outputs (depends on R ₃₃ and R ₃₄)	14,17,20	—	4.7	—	
Luminance Bandwidth (–3.0 dB)		9.0	—	—	MHz
Output Resistance		120	170	300	Ω
Residual Carrier (4.43 Mc/s)		—	30	150	mV _{p-p}
PAL Offset (H/2)		—	—	50	mV _{p-p}
Difference in Gain Between Y Input and any RGB o/p		—	5.0	—	%
U Input Sensitivity for 5.0 V Blue Output	8	—	340	—	mV _{p-p}
Matrix Error	14,17,20	—	—	10	%
Oscillator Capture Range		350	—	—	Hz
U Ref. Phase Error		—	—	5.0	Degrees
V Ref. Phase Error		—	—	5.0	Degrees
Color Kill Attenuation	14,17,20	50	—	—	dB
Contrast Tracking OSD/Luma/Chroma	14,17,20	—	—	—	dB
OSD Contrast Tracking	14,17,20	—	—	±2.0	dB
OSD Enable Slice Level	23	—	0.7	—	V
Sandcastle Slice Level	27	—	—	—	V
Burst Gate		6.5	7.2	8.0	V
Line Blanking		2.0	2.6	3.0	V
R Input V ₂₇ > 7.0 V		—	5.0	—	kΩ
V ₂₇ < 7.0 V		—	22	—	kΩ
Frame Slice Level	28	2	2.8	3.6	V
R Input		—	15	—	kΩ
Peak Beam Limiter Threshold (I ₂₉ Min = 250 μA)		3.4 × I ₂₉	4 × I ₂₉	4.6 × I ₂₉	
Pin 29 Input Resistance	29	—	5.0	—	kΩ
Pin 29 Open Circuit Voltage	29	—	10.6	—	V

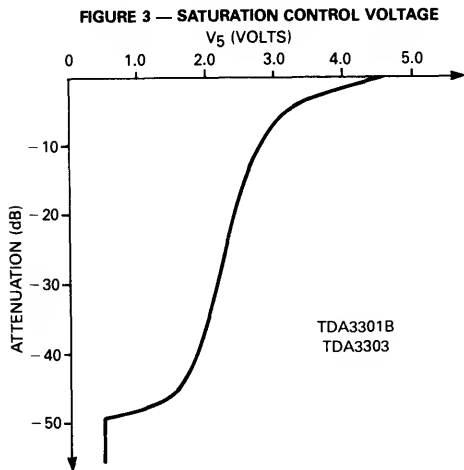
INPUT/OUTPUT FUNCTIONS



The brilliance control operates by adding a pedestal to the output signals. The amplitude of the pedestal is controlled by Pin 30.

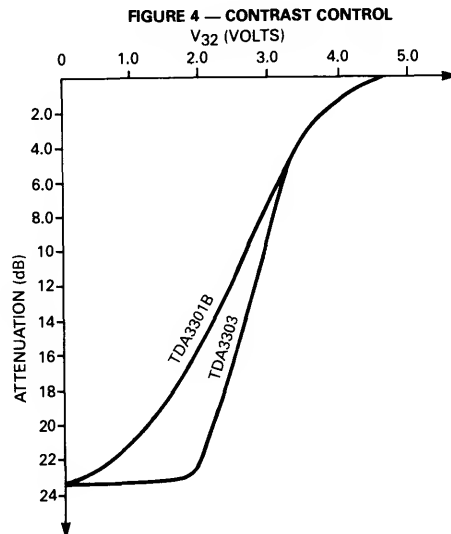
During CRT beam current sampling a standard pedestal is substituted, its value being equivalent to the value given by V_{30} Nom. Brightness at black level with V_{30} Nom is given by the sum of three gun currents at the sampling level, i.e. $3 \times 20 \mu\text{A}$ with 100 k reference resistors on Pins 16, 19, and 22.

During picture blanking the brilliance pedestal is zero; therefore the output voltage during blanking is always the minimum brilliance black level (Note: Signal channels are also gain blanked).



Pin 5 is automatically pulled to ground with a mis-identified PAL signal.

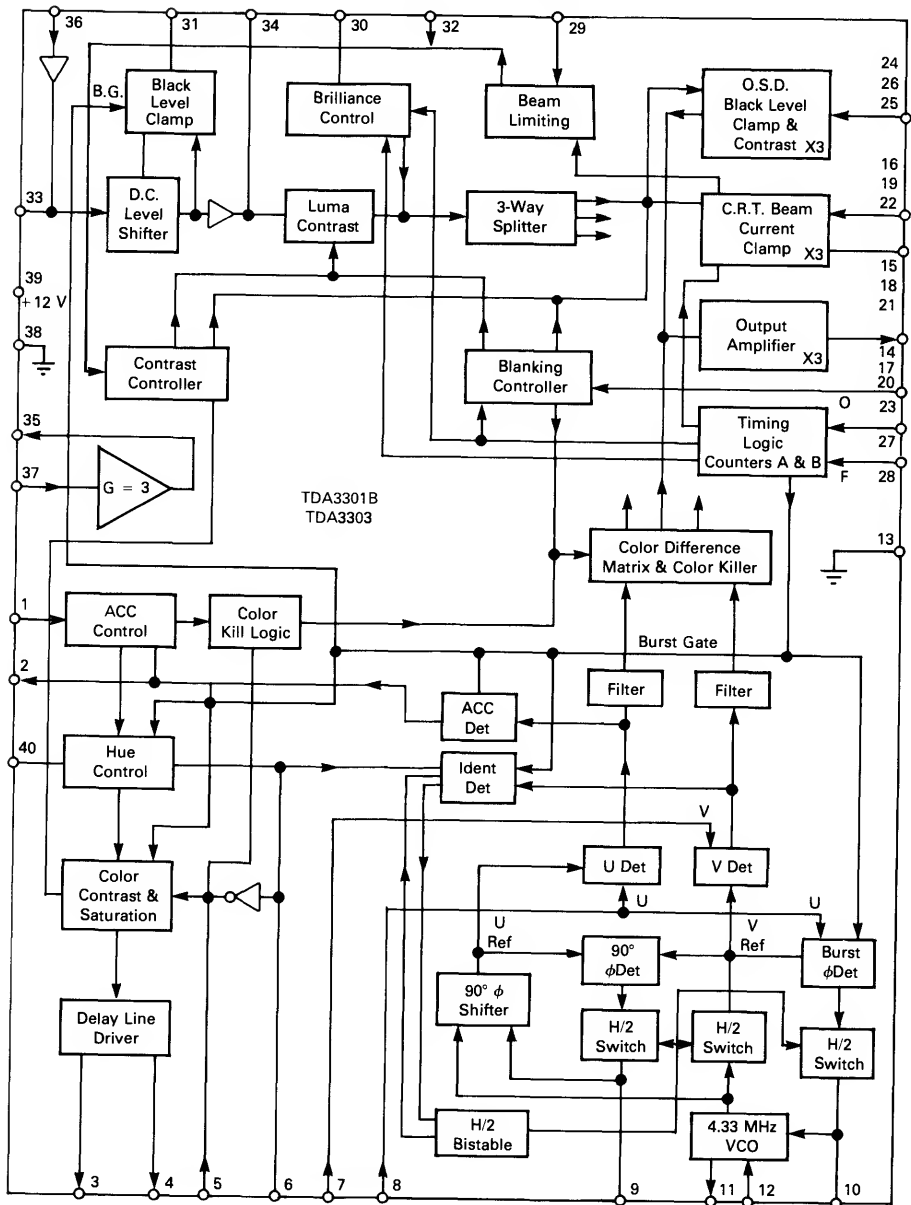
Note: Nominal 100% saturation point is given by choice of R_2 which sets ACC operating point.



Note: Pin 32 is pulled down by the operation of the peak beam limiter.

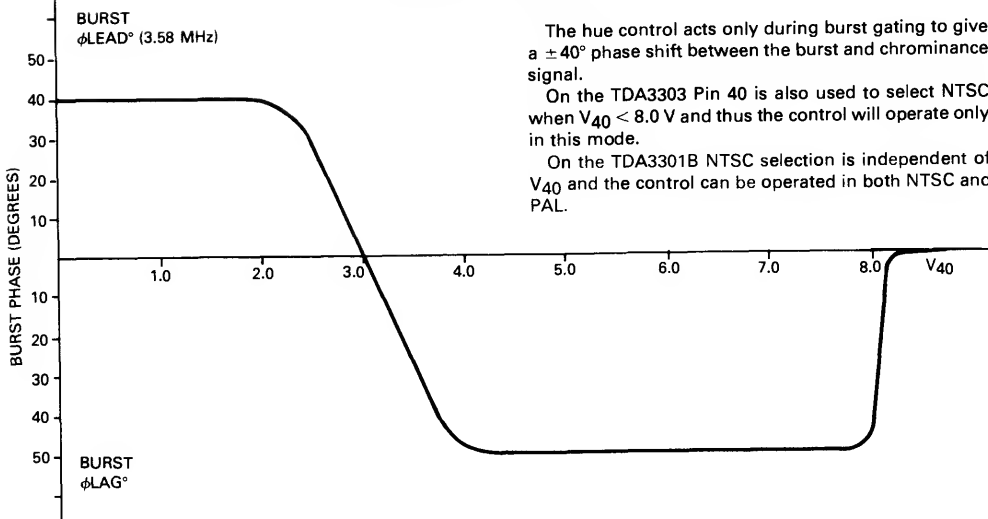
TDA3301B, TDA3303

FIGURE 5 — BLOCK DIAGRAM



TDA3301B, TDA3303

FIGURE 6 — HUE CONTROL



The hue control acts only during burst gating to give a $\pm 40^\circ$ phase shift between the burst and chrominance signal.

On the TDA3303 Pin 40 is also used to select NTSC when $V_{40} < 8.0$ V and thus the control will operate only in this mode.

On the TDA3301B NTSC selection is independent of V_{40} and the control can be operated in both NTSC and PAL.

CIRCUIT OPERATION

CHROMINANCE DECODER SECTION

The chrominance decoder section of the TDA3301B consists of the following blocks:

Phase-locked reference oscillator — Figures 7, 8 and 9
Phase-locked 90 degree servo loop — Figures 9 and 10
U and V axis decoders

ACC detector and identification detector — Figure 11

Identification circuits and PAL bistable — Figure 12
Color difference filters and matrixes with fast blanking circuits.

The major design considerations apart from optimum performance were:

- a minimum number of factory adjustments
- a minimum number of external components
- compatibility with the SECAM adapter TDA3030B
- low dissipation
- use of a standard 4.433618 MHz Crystal rather than a 2.0 mc Crystal with divider.

REFERENCE REGENERATION

The crystal VCO is of the phase shift variety in which the frequency is controlled by varying the phase of the feedback. A great deal of care was taken to ensure that the oscillator loop gain and the crystal loading impedance were held constant in order to ensure that the circuit functions well with low grade crystal (crystals having high magnitude spurious responses can cause bad phase jitter). It is also necessary to ensure that the gain at third harmonic is low enough to ensure absence of oscillation at this frequency.

FIGURE 7 — VOLTAGE CONTROLLED OSCILLATOR (VCO)

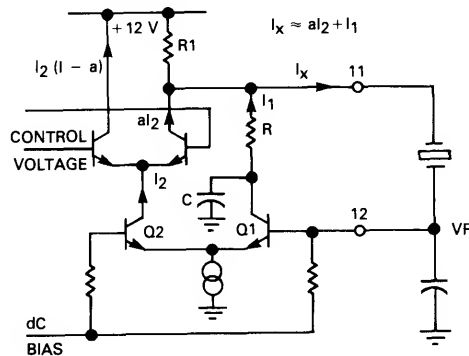
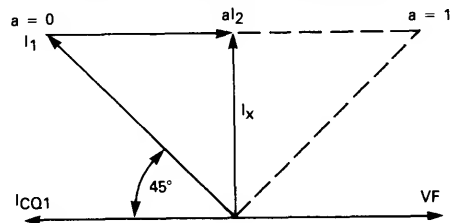


FIGURE 8 — VECTOR DIAGRAM FOR VCO



By referring to Figures 7 and 8 it can be seen that the necessary $\pm 45^\circ$ phase shift is obtained by variable addition of two currents I_1 and I_2 which are then fed into the load resistance of the crystal tuned circuit R_1 . Feedback is taken from the crystal load capacitance which gives a voltage V_F lagging the crystal current by 90° .

The RC network in T_1 collector causes I_1 to lag the collector current of T_1 by 45° .

For SECAM operation the currents I_1 and I_2 are added together in a fixed ratio giving a frequency close to nominal.

When decoding PAL there are two departures from normal chroma reference regeneration practice:

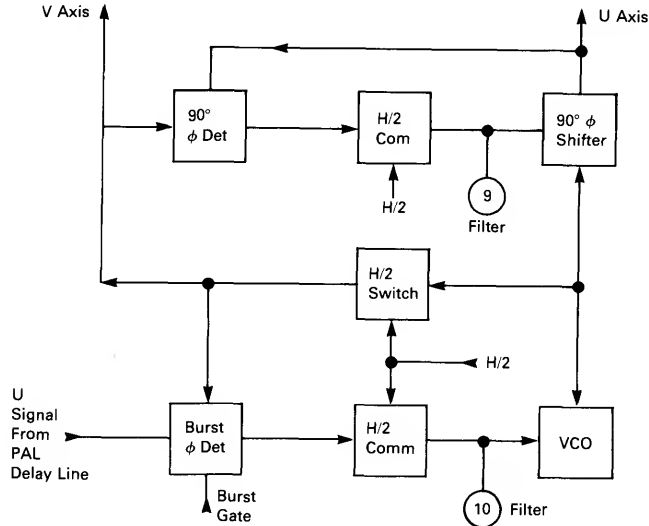
- a) The loop is locked to the burst entering from the PAL delay line matrix U channel and hence there is no alternating component. A small improvement in signal noise ratio is gained but more important

is that the loop filter is not compromised by the 7.8 kHz component normally required at this point for PAL identification.

- b) The H/2 switching of the oscillator phase is carried out before the phase detector. This implies any error signal from the phase detector is a signal at 7.8 kHz and not dc. A commutator at the phase detector output also driven from the PAL bistable converts this ac signal to a dc prior to the loop filter. The purpose of this is that constant offsets in the phase detector are converted by the commutator to a signal at 7.8 kHz which is integrated to zero and does not give a phase error.

When used for decoding NTSC the bistable is inhibited, and slightly less accurate phasing is achieved; however, as a hue control is used on NTSC this cannot be considered to be a serious disadvantage.

FIGURE 9 — BLOCK DIAGRAM OF REFERENCE SECTION



90° REFERENCE GENERATION

To generate the U axis reference a variable all-pass network is utilized in a servo loop. The output of the all-pass network is compared with the oscillator output with a phase detector of which the output is filtered and corrects the operating point of the variable all-pass network (see Figure 10).

As with the reference loop the oscillator signal is taken after the H/2 phase switch and a commutator inserted before the filter so that constant phase detector errors are cancelled.

For SECAM operation the loop filter is grounded causing near zero phase shift so that the two synchronous detectors work in phase and not in quadrature.

The use of a 4.4 MHz oscillator and a servo loop to generate the required 90° reference signal allows the use of a standard, high volume, low cost crystal and gives an extremely accurate 90° which may be easily switched to 0° for decoding AM SECAM generated by the TDA3030B adapter.

FIGURE 10 — VARIABLE ALL-PASS NETWORK

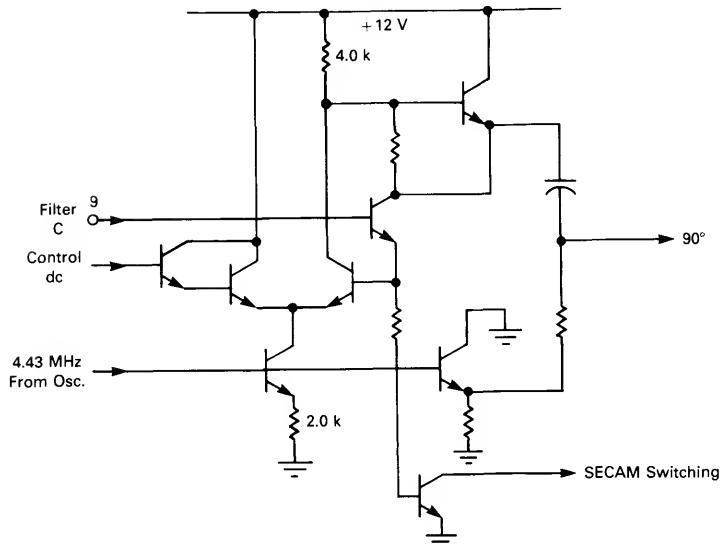
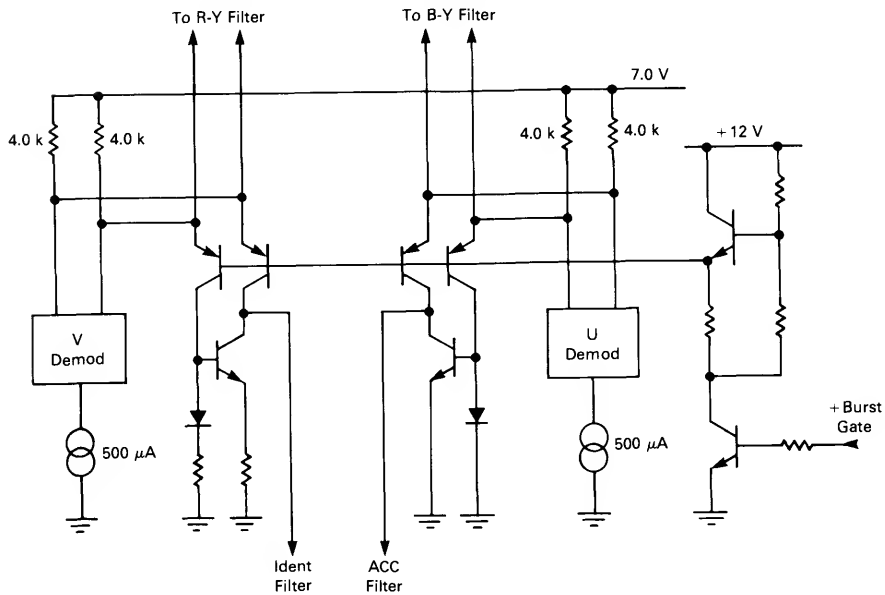


FIGURE 11 — ACC AND IDENTIFICATION DETECTORS



ACC AND IDENTIFICATION DETECTORS

During burst gate time the output components of the U and also the V demodulators are steered into PNP emitters. One collector current of each PNP pair is mirrored and balanced against its twin giving push-pull current sources for driving the ACC and the identification filter capacitors.

The identification detector is given an internal offset by making the NPN current mirror emitter resistors unequal. The resistors are offset by 5% such that the identification detector pulls up on its filter capacitor with zero signal.

IDENTIFICATION

See Figure 12 for definitions.

Monochrome $I_1 > I_2$

PAL ident. OK $I_1 < I_2$

PAL ident. X $I_1 > I_2$

NTSC $I_3 > I_2$

Only for correctly identified PAL signal is the capacitor voltage held low since I_2 is then greater than I_1 .

For monochrome and incorrectly identified PAL signals $I_1 > I_2$ hence voltage V_C rises with each burst gate pulse.

When V_{ref1} is exceeded by 0.7 V latch 1 is made conducting which increases rate of voltage rise on C. Maximum current is limited by R_1 .

When V_{ref2} is exceeded by 0.7 V then latch 2 is made conducting until C is completely discharged and the current drops to a value insufficient to hold on latch 2.

As latch 2 turns on latch 1 must turn off.

Latch 2 turning on gives extra trigger pulse to bistable to correct identification.

The inhibit line on latch 2 restricts latch 2 conduction to alternate lines as controlled by the bistable. This function allows the SECAM switching line to inhibit the bistable operation by firing latch 2 in the correct phase for SECAM. For NTSC latch 2 is fired by current injected on Pin 6.

If the voltage on C is greater than 1.4 V then the saturation is held down. Only for SECAM/NTSC with latch 2 on or correctly identified PAL can the saturation control be anywhere but minimum.

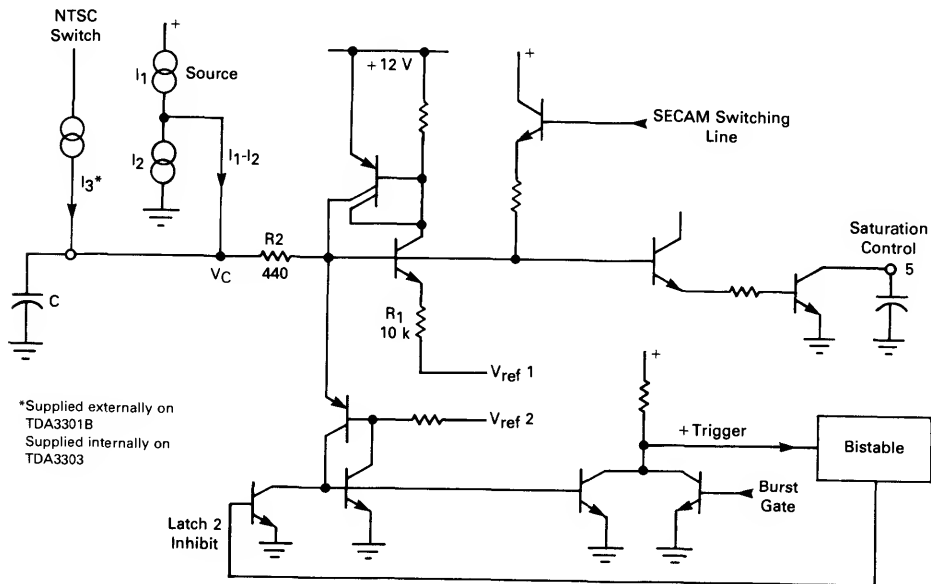
NTSC SWITCH

NTSC operation is selected when current (I_3) is injected into Pin 6.

On the TDA3301B this current must be derived externally by connecting Pin 6 to +12 V via a 27 k resistor (as on TDA3300B).

On the TDA3303 I_3 is supplied internally when V_{40} falls below 8.0 V.

For normal PAL operation on both versions Pin 40 should be connected to +12 V and Pin 6 to the filter capacitor.

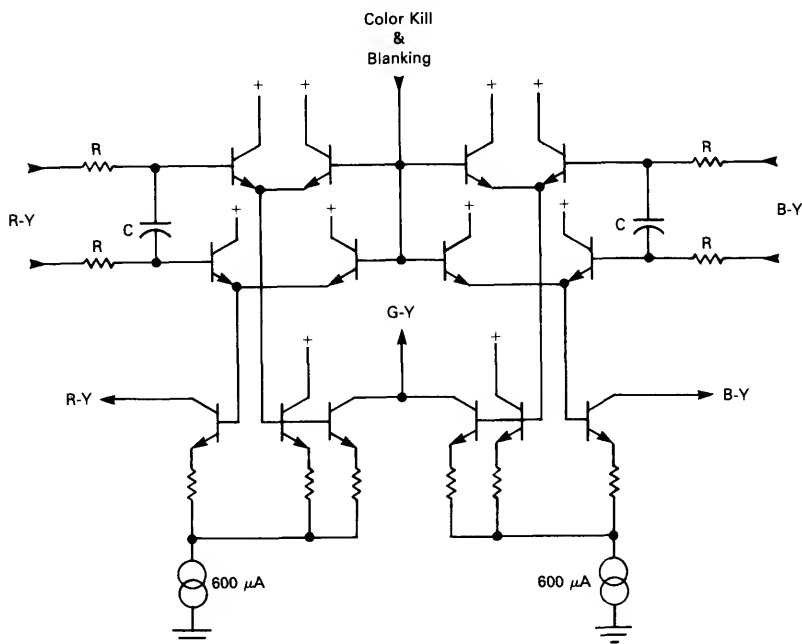
FIGURE 12 — IDENTIFICATION CIRCUIT

COLOR DIFFERENCE MATRIXING, COLOR KILLING, AND CHROMA BLANKING

During picture time the two demodulators feed simple RC filters with emitter follower outputs. Color killing and blanking is performed by lifting these outputs to a voltage above the maximum value that the color difference signal could supply.

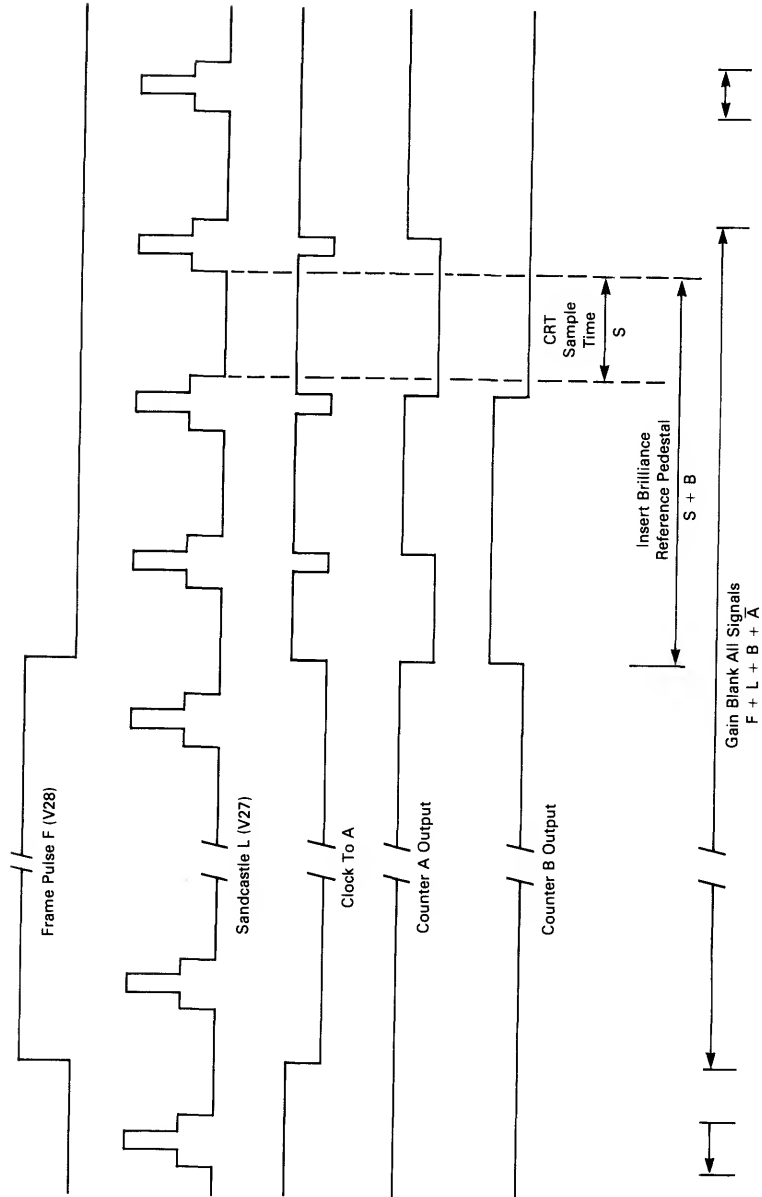
The color difference matrixing is performed by 2 differential amplifiers each with one side split to give the correct values of the $-(B-Y)$ and $-(R-Y)$ signals. These are added to give the $(G-Y)$ signal.

The 3 color difference signals are then taken to the virtual earths of the video output stages together with luminance signal.

FIGURE 13 — COLOR DIFFERENCE STAGES**SANDCASTLE SELECTION**

The TDA3301B/3303 may be used with a two level sandcastle and a separate frame pulse to Pin 28, or with only a 3 level (super) sandcastle. In the latter case a resistor of $1\text{ M}\Omega$ is necessary from +12 volts to Pin 28 and a 470 pF capacitor from Pin 28 to ground.

FIGURE 14 — TIMING DIAGRAM



TDA3301B, TDA3303

TIMING COUNTER FOR SAMPLE CONTROL

In order to control the beam current sampling at the beginning of each frame scan two edge triggered flip-flops are used.

The output \bar{A} of the first flip-flop A is used to clock the second flip-flop B. Clocking of A by the burst gate is inhibited by a count of A.B.

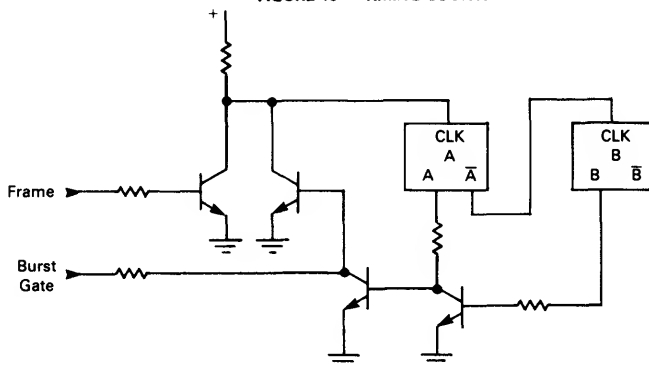
The count sequence can only be initiated by the trail-

ing edge of the frame pulse. In order to provide control signals for:

- Luma/Chroma blanking,
- Beam current sampling,
- On-screen display blanking,
- Brilliance control.

The appropriate flip-flop outputs are matrixed with sandcastle and frame signals by an emitter follower matrix.

FIGURE 15 — TIMING COUNTER

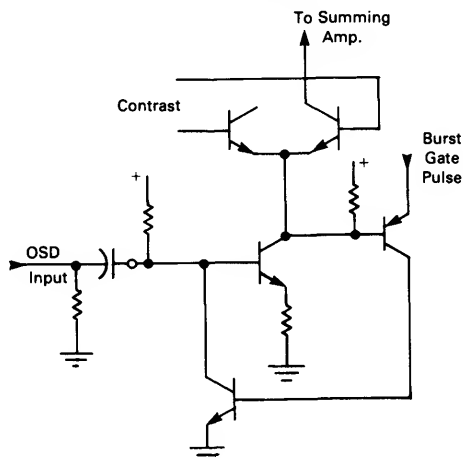


ON-SCREEN DISPLAY INPUTS

Each section of the OSD stages consists of a common emitter input stage feeding a diversion gate controlled by the contrast control. During burst gate time a feedback loop is activated which clamps the signal at the

input coupling capacitor. This ensures that the current in the diversion gate is zero at black level and makes the OSD black level insensitive to contrast control, also the inputs ignore signals below black, e.g. sync, pulses.

FIGURE 16 — OSD STAGE



TDA3301B, TDA3303

FIGURE 17 — VIDEO OUTPUT SECTION

Each video output stage consists of a feedback amplifier in which the input signal is a current drive to the virtual earth from the luminance, color difference and on-screen display stages.

A further drive current is used to control the dc operating point; this is derived from the sample and hold stage which samples the beam current after frame flyback.

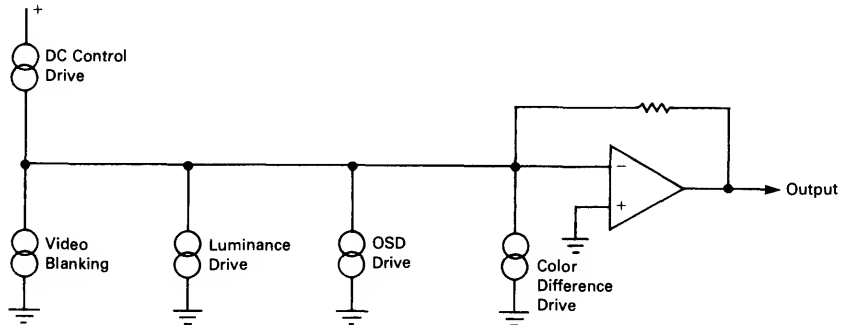


FIGURE 18 — COMPLETE VIDEO OUTPUT SECTIONS

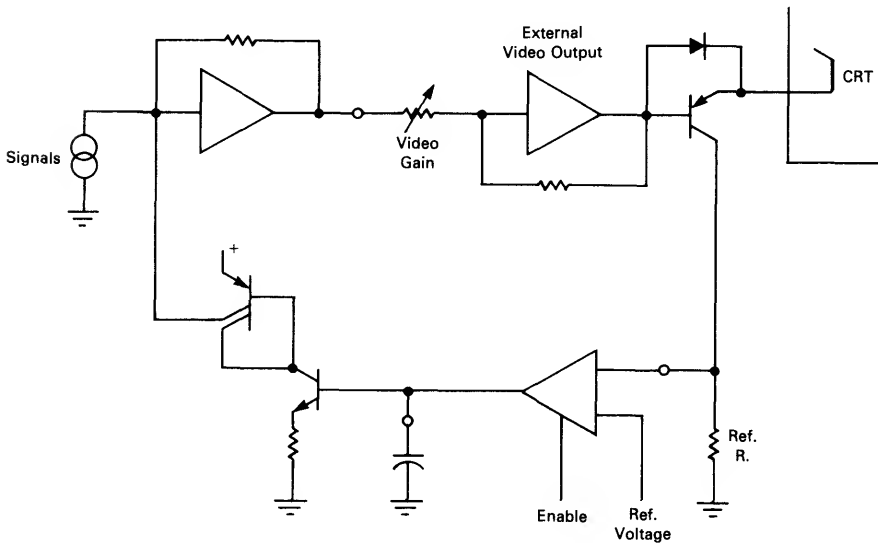


FIGURE 19 — TYPICAL VIDEO OUTPUT STAGE

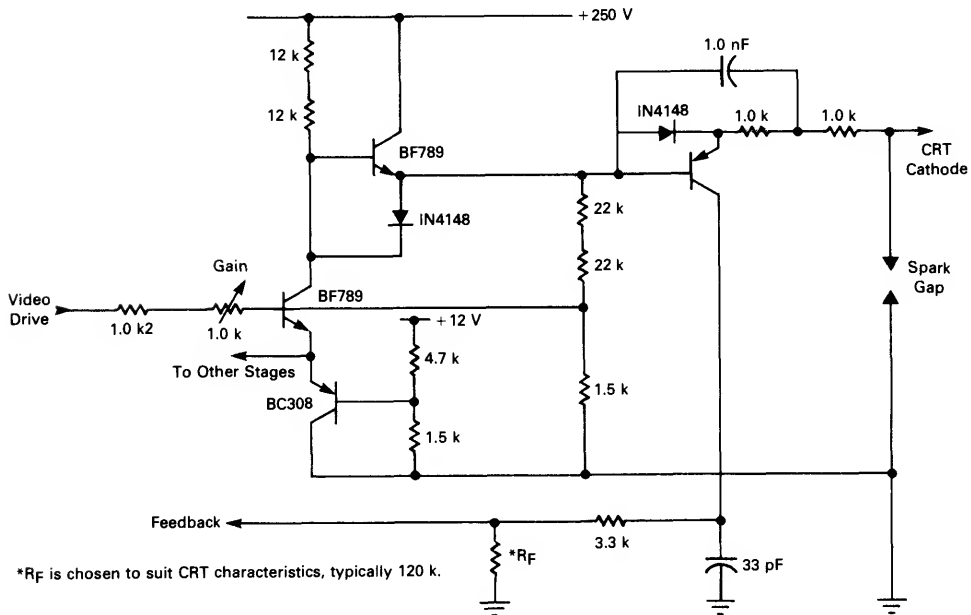


FIGURE 20 — CLASS A VIDEO OUTPUT STAGE WITH DIRECT FEEDBACK

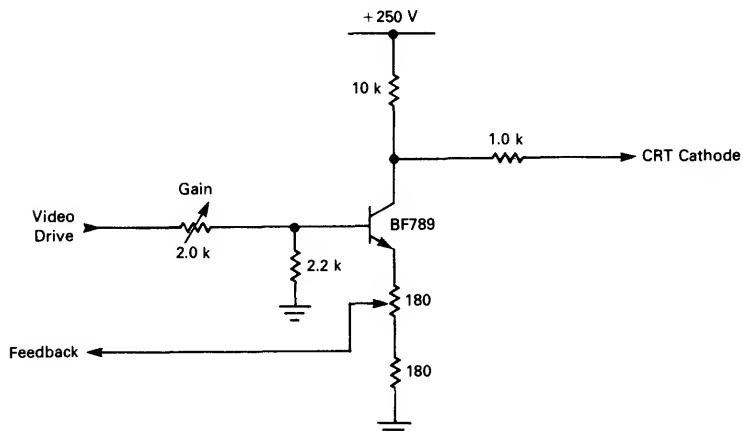
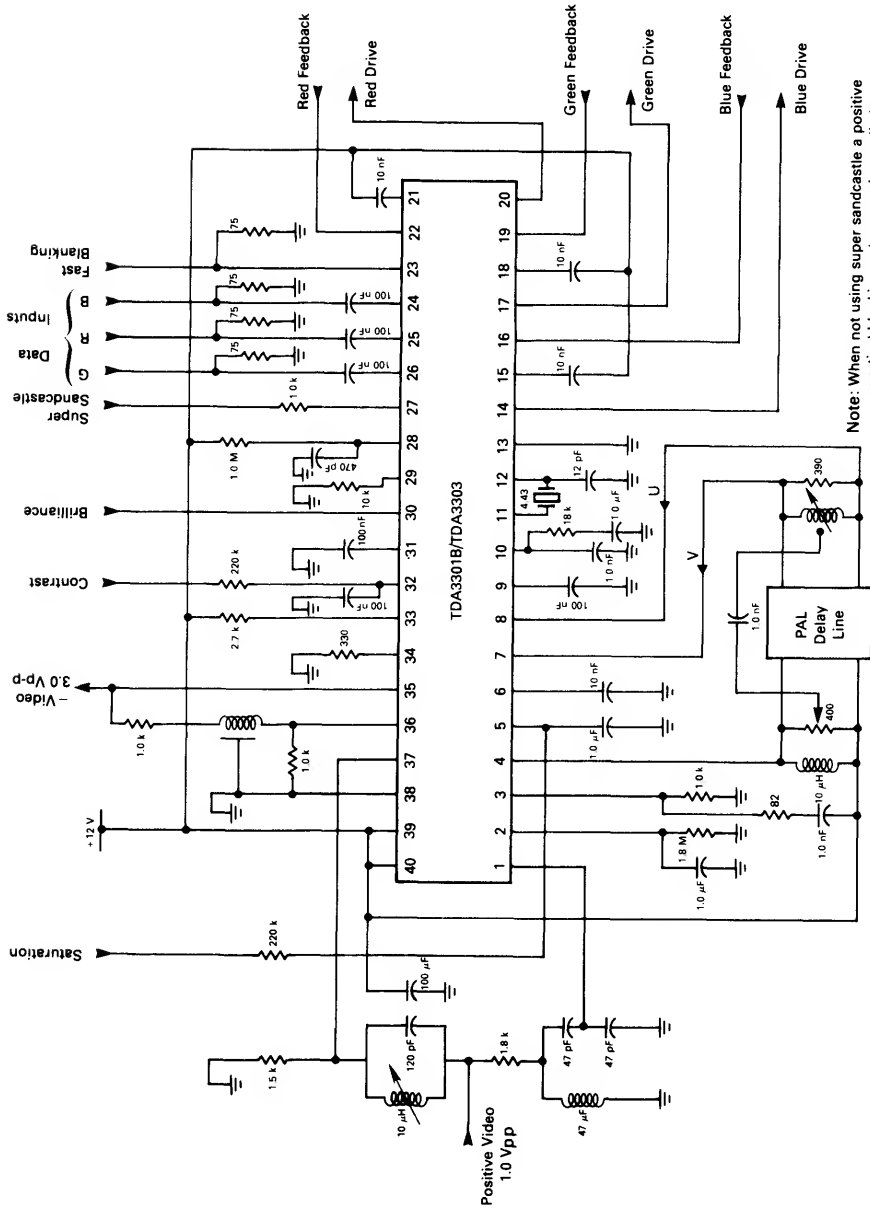


FIGURE 21 — TYPICAL PAL APPLICATION



Note: When not using super sandcastle a positive vertical blanking pulse must be applied to Pin 28.

TDA3330

TV COLOR PROCESSOR

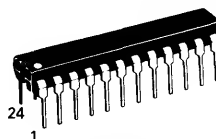
This device will accept a PAL or NTSC composite video signal and output the three color signals, needing only a simple driver amplifier to interface to the picture tube.

Its simplified approach makes it particularly suitable for low cost CTV systems.

- No Oscillator Adjustment Required
- Four dc High Impedance User Controls
- Uses Inexpensive 4.43/3.58 MHz Crystals
- Interfaces With TDA3030B SECAM Adaptor
- Uses Horizontal Flyback or Super Sandcastle Pulse
- Single 12 V Supply
- Low Dissipation

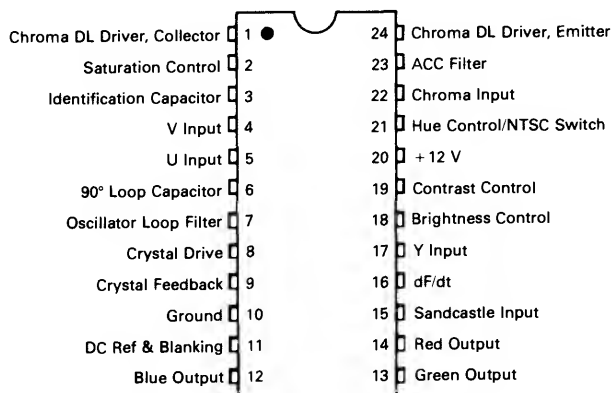
TV COLOR PROCESSOR

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**



**P SUFFIX
PLASTIC PACKAGE
CASE 724**

FIGURE 1 — PIN ASSIGNMENT



TDA3330

MAXIMUM RATINGS (T_A = +25°C unless otherwise stated)

Rating	Pin	Value	Unit
Supply Voltage	20	14	V _{dc}
Operating Temperature Range		0 to +70	°C
Storage Temperature Range		-65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 12 V)

Characteristic	Pin	Min	Typ	Max	Unit
Supply Voltage	20	10.8	12	13.2	V
Supply Current		—	—	50	mA
Composite Video Input	17	—	1.0	—	V _{p-p}
Video Input Resistance		—	—	—	—
Burst Gate On		—	5.0	—	kΩ
Burst Gate Off		—	1.5	—	MΩ
Chroma Input (Burst)	22	10	100	200	mV _{p-p}
Input Resistance	22	—	5.0	—	kΩ
ACC Effectiveness	1	-1.5	0	+1.5	dB
Luminance Gain between Pin 17 and Outputs (Contrast max)		—	8.0	—	—
Luminance Bandwidth (-3.0 dB)	12, 13, 14	—	5.0	—	MHz
Output Resistance		—	170	—	Ω
Residual Carrier (4.43 MHz)		—	—	200	mV _{p-p}
PAL Offset (H/2)		—	—	50	mV _{p-p}
U Input Sensitivity for 5.0 V Blue Output	5	—	340	—	mV _{p-p}
Matrix Error	12, 13, 14	—	—	10	%
Oscillator Capture Range		300	500	—	Hz
U Reference Phase Error		—	—	5.0	Degrees
V Reference Phase Error		—	—	5.0	Degrees
Color Kill Attenuation	12, 13, 14	50	—	—	dB
Contrast Tracking Luma/Chroma	12, 13, 14	—	0	2.0	dB
Sandcastle Slice Level	15	—	—	—	—
Burst Gate		—	7.2	8.0	V
Line Blanking		0.5	1.5	2.5	V
R Input V ₁₅ > 7.0 V		—	5.0	—	kΩ
V ₁₅ < 7.0 V		—	10	—	kΩ

INPUT/OUTPUT FUNCTIONS

FIGURE 2 — BRIGHTNESS CONTROL

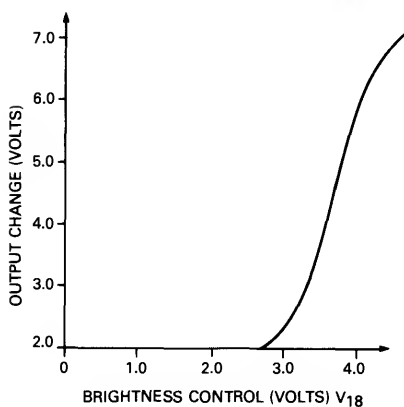
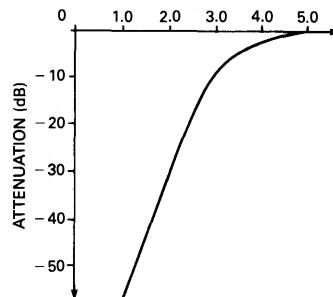


FIGURE 3 — SATURATION CONTROL VOLTAGE V₂ (VOLTS)



Pin 2 is automatically pulled to ground with a mis-identified PAL signal.

Note: Nominal 100% saturation point is given by choice of R_{pin 23} which sets ACC operating point.

TDA3330

FIGURE 4 — CONTRAST CONTROL
V₁₉ (VOLTS)

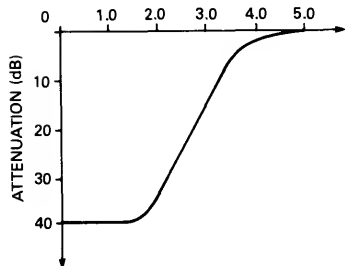
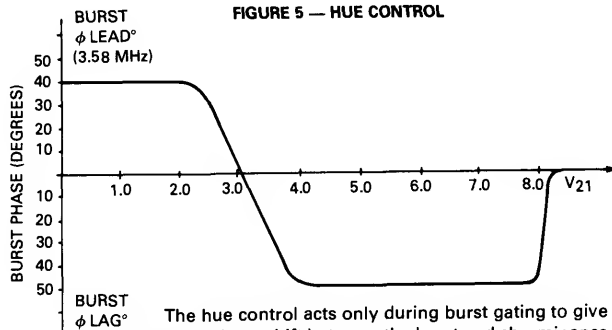


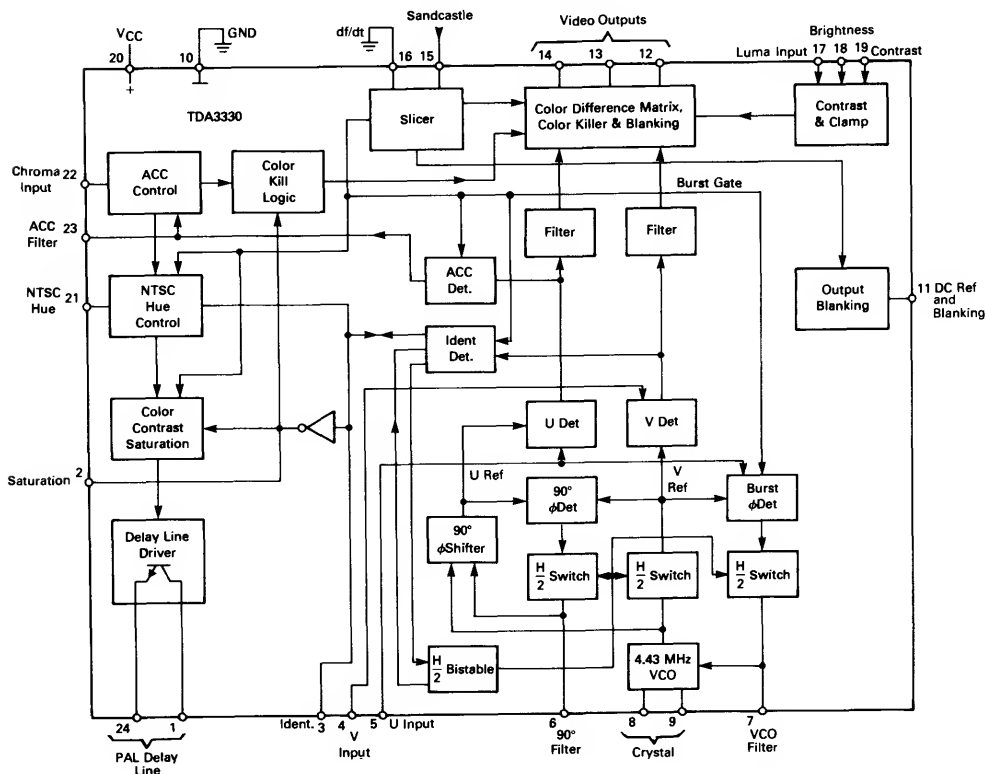
FIGURE 5 — HUE CONTROL



The hue control acts only during burst gating to give a $\pm 40^\circ$ phase shift between the burst and chrominance signal.

Pin 21 is also used to select NTSC when V₂₁ < 8.0 V and thus the control will operate only in this mode. NTSC selection means the PAL phase switching is turned off. Delay-line and filter switching must be implemented externally.

FIGURE 6 — BLOCK DIAGRAM



CIRCUIT OPERATION

CHROMINANCE DECODER SECTION

The chrominance decoder section of the TDA3330 consists of the following blocks:

- Phase-locked reference oscillator — Figures 7, 8 and 9
- Phase-locked 90 degree servo loop — Figures 9 and 10
- U and V axis decoders
- ACC detector and identification detector — Figure 11
- Identification circuits and PAL bistable — Figure 12
- Color difference filters and matrixes with fast blanking circuits.

The major design considerations apart from optimum performance were:

- a minimum number of factory adjustments
- a minimum number of external components
- compatibility with the SECAM adapter TDA3030B
- low dissipation
- use of a standard 4.433618 MHz crystal rather than a 2.0 mc crystal with divider, (or standard 3.579545 MHz for NTSC).

REFERENCE REGENERATION

The crystal VCO is of the phase shift variety in which the frequency is controlled by varying the phase of the feedback. Much care was taken to ensure that the oscillator loop gain and the crystal loading impedance were held constant in order to ensure that the circuit functions well with low grade crystals (crystals having high magnitude spurious responses can cause bad phase jitter). It is also necessary to ensure that the gain at third harmonic is low enough to ensure absence of oscillation at this frequency.

By referring to Figures 7 and 8 it can be seen that the necessary $\pm 45^\circ$ phase shift is obtained by variable addition of two currents I_1 and I_2 which are then fed into the load resistance of the crystal tuned circuit R_1 . Feedback is taken from the crystal load capacitance which gives a voltage V_F lagging the crystal current by 90° .

The RC network in Q1 collector causes I_1 to lag the collector current of Q1 by 45° .

For SECAM operation the currents I_1 and I_2 are added together in a fixed ratio giving a frequency close to nominal.

When decoding PAL there are two departures from normal chroma reference regeneration practice:

- a) The loop is locked to the burst entering from the PAL delay line matrix U channel and hence there is no alternating component. A small improvement in signal noise ratio is gained but more important is that the loop filter is not compromised by the 7.8 kHz component normally required at this point for PAL identification.

FIGURE 7 — VOLTAGE CONTROLLED OSCILLATOR (VCO)

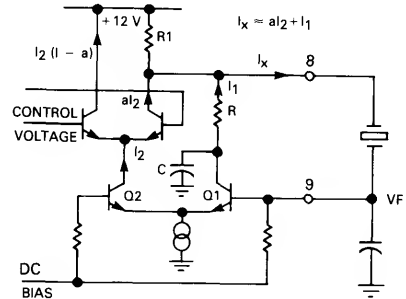
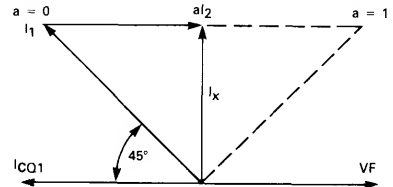


FIGURE 8 — VECTOR DIAGRAM FOR VCO



- b) The H/2 switching of the oscillator phase is carried out before the phase detector. This implies any error signal from the phase detector is a signal at 7.8 kHz and not DC. A commutator at the phase detector output also driven from the PAL bistable converts this AC signal to a DC prior to the loop filter. The purpose of this is that constant offsets in the phase detector are converted by the commutator to a signal at 7.8 kHz which is integrated to zero and does not give a phase error.

When used for decoding NTSC the bistable is inhibited, and slightly less accurate phasing is achieved; however, as a hue control is used on NTSC this cannot be considered to be serious disadvantage.

90° REFERENCE GENERATION

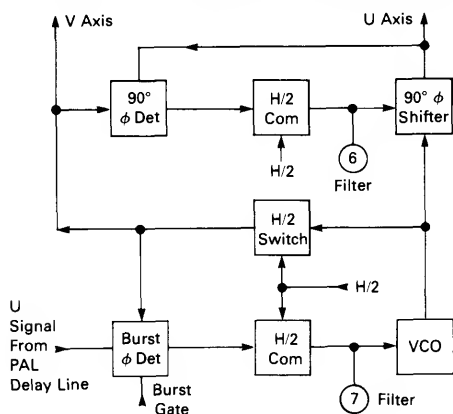
To generate the U axis reference a variable all-pass network is utilized in a servo loop. The output of the all-pass network is compared with the oscillator output with a phase detector of which the output is filtered and corrects the operating point of the variable all-pass network. (See Figure 10.)

As with the reference loop the oscillator signal is taken after the H/2 phase switch and a commutator inserted before the filter so that constant phase detector errors are cancelled.

For SECAM operation with TDA3030B the loop filter is grounded causing near zero phase shift so that the two synchronous detectors work in phase and not in quadrature.

The use of a 4.4 MHz oscillator and a servo loop to generate the required 90° reference signal allows the use of a standard, high volume, low cost crystal and gives an extremely accurate 90° which may be easily switched to 0° for decoding AM SECAM generated by the TDA3030B adapter.

FIGURE 9 — BLOCK DIAGRAM OF REFERENCE SECTION



ACC AND IDENTIFICATION DETECTORS

During burst gate time the output components of the U and also the V demodulators are steered into PNP emitters. One collector current of each PNP pair is mirrored and balanced against its twin giving push pull current sources for driving the ACC and the identification filter capacitors.

The identification detector is given an internal offset by making the NPN current mirror emitter resistors unequal. The resistors are offset by 5% such that the identification detector pulls up on its filter capacitor with zero signal.

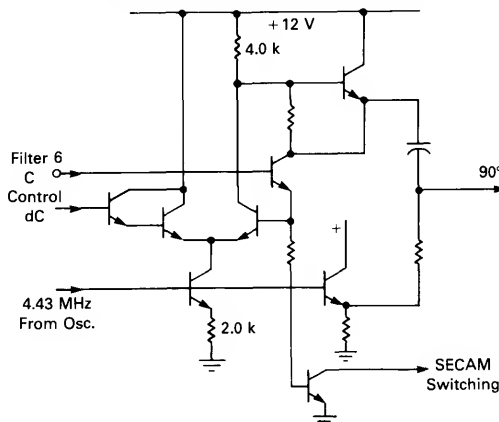
IDENTIFICATION

See Figure 12 for definitions.

Monochrome	$I_1 > I_2$
PAL ident. OK	$I_1 < I_2$
PAL ident. X	$I_1 > I_2$
NTSC	$I_3 > I_2$

Only for correctly identified PAL signal is the capacitor voltage held low since I_2 is then greater than I_1 .

FIGURE 10 — VARIABLE ALL-PASS NETWORK



For monochrome and incorrectly identified PAL signals $I_1 > I_2$ hence voltage V_C rises with each burst gate pulse.

When V_{ref1} is exceeded by 0.7 V latch 1 is made conducting which increases rate of voltage rise on C. Maximum current is limited by R_1 .

When V_{ref2} is exceeded by 0.7 V then latch 2 is made conducting until C is completely discharged and the current drops to a value insufficient to hold on latch 2.

As latch 2 turns on latch 1 must turn off.

Latch 2 turning on gives extra trigger pulse to bistable to correct identification.

The inhibit line on latch 2 restricts latch 2 conduction to alternate lines as controlled by the bistable. This function allows the SECAM switching line to inhibit the bistable operation by firing latch 2 in the correct phase for SECAM. For NTSC latch 2 is fired by current (I_3) injected into Pin 3 by the NTSC switch. This is supplied internally when V_{21} falls below 8.0 V.

If the voltage on C is greater than 1.4 V then the saturation is held down. Only for SECAM/NTSC with latch 2 on or correctly identified PAL can the saturation control be anywhere but minimum.

FIGURE 11 — ACC AND IDENTIFICATION DETECTORS

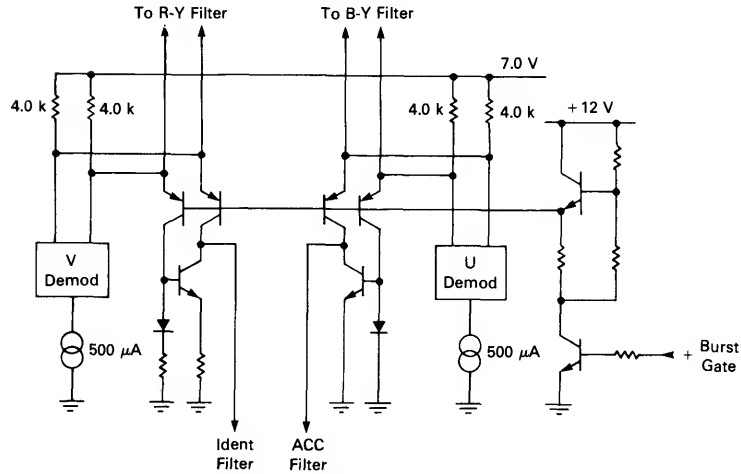
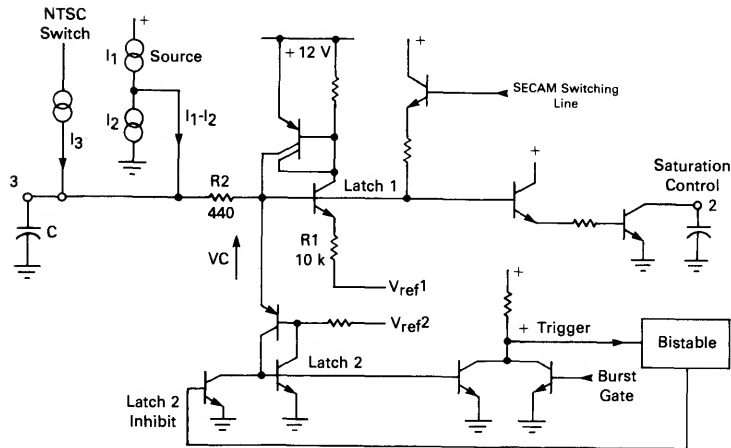


FIGURE 12 — IDENTIFICATION CIRCUIT



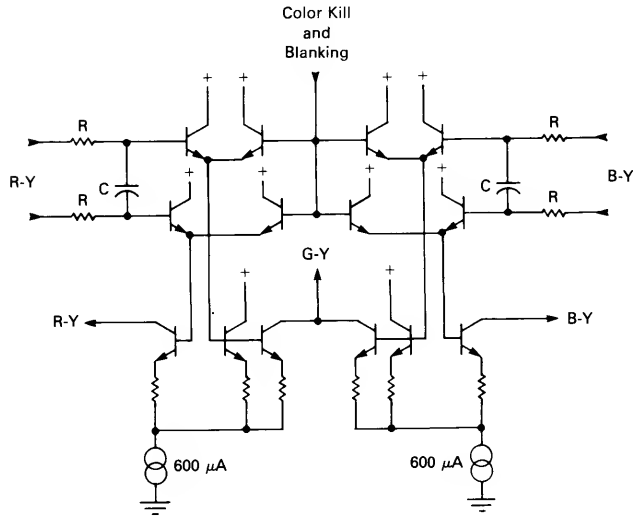
COLOR DIFFERENCE MATRIXING, COLOR KILLING, AND CHROMA BLANKING

During picture time the two demodulators feed simple RC filters with emitter follower outputs. Color killing and blanking is performed by lifting these outputs to a voltage above the maximum value that the color difference signal could supply.

The color difference matrixing is performed by 2 differential amplifiers each with one side split to give the correct values of the $-(B-Y)$ and $-(R-Y)$ signals. These are added to give the $(G-Y)$ signal.

The 3 color difference signals are then taken to the virtual earths of the video output stages together with luminance signal.

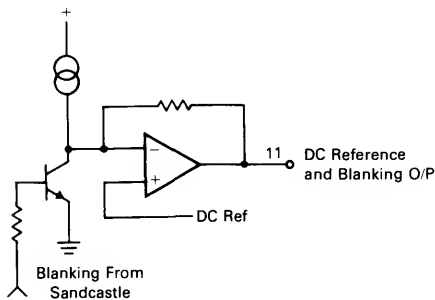
FIGURE 13 — COLOR DIFFERENCE STAGES

**SANDCASTLE SECTION**

The input signal is sliced at 2 levels, 1.5 V and 7.2 V. Above 1.5 V is used for blanking, above 7.2 V for burst gating provided level on Pin 16 is below 0.7 V. If a normal Sandcastle is used, it is recommended to ground the

Pin 16. This input is used to inhibit the burst gate. This is used if a true Sandcastle is not available; in this case horizontal flyback may be used instead and differentiated flyback applied to the $\frac{df}{dt}$ pin (input resistance 1.0 k Ω).

FIGURE 14 — DC REFERENCE AND BLANKING SECTION



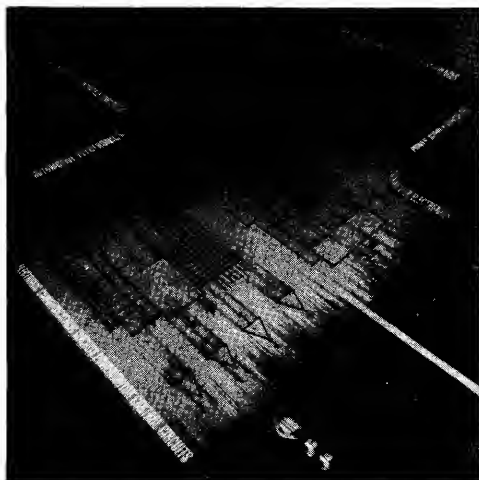
The DC Reference and Blanking section is used to bias the Video output stages. The temperature coefficient is arranged to be a V_{BE} drift less than the Red, Green and Blue outputs.

9

[illegible]

R₁ — Should be selected to give approximately 10–12 V pulse at Pin 15 (approximately 5.0 k internal resistance).

R₂ — Should be selected to give approximately 4.0 to 5.0 V pulse at Pin 15 (approximately 10 k internal resistance).



In Brief . . .

Motorola Linear has established itself as the leader in custom bipolar integrated circuits in the American and European automotive markets. These products are key elements in the rapidly growing engine control and body electronics portions of modern automobiles. Today, based on this new technology, Motorola offers a wide array of standard products to serve the broad base of manufacturers who support this industry. These products range from rugged high current "smart" fuel injector drivers which control and protect the fuel management system, through the rigors of the underhood environment, to the latest in BiMOS switches and series transient protectors. Several devices are targeted to support microprocessor housekeeping and data line protection. A wide range of packaging is available, from die and SOICs for high density layouts, to low thermal resistance multi-pin, single-in-line types for high power control ICs.

Automotive Electronic Circuits

Selector Guide

Voltage Regulators 10-2

Electronic Ignition 10-2

Special Functions 10-2

Alphanumeric Index 10-5

Data Sheets 10-6

Automotive Electronic Circuits

Voltage Regulators

Function	Features	Package Suffix	Device
Automotive Voltage Regulator	Designed for use with NPN Darlington, Overvoltage Protection; "Open Sense" Shut Down; Selectable Temperature Coefficient for Use in a Floating Field Alternator Charging System	P/646	MC3325
Low Dropout Voltage Regulator	Positive fixed and adjustable output voltage regulators which maintain regulation with very low input to output voltage differential.	Z/29, T/221A, T/314D	LM2931,C
Low Dropout Dual Regulator	Positive low voltage differential regulator which features dual 5 V outputs, with currents in excess of 750 mA and 10 mA standby, and a low quiescent current of 3 mA or less.	T/314D	LM2935

Electronic Ignition

Electronic Ignition Circuit	Designed for Use in High Energy Variable Dwell Electronic Ignition Systems with Variable Reluctance Sensors. Dwell and Spark Energy are Externally Adjustable	P/626, D/751	MC3334
Flip-Chip Electronic Ignition Circuit	Same as MC3334 — Mirror Image Die for Inverted "Bumped" Mounting to Substrate	—	MCCF3334

Special Functions

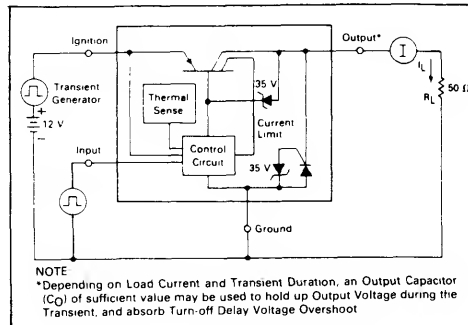
Injector Driver	Power Driver for Automotive Fuel Injection Systems, Reduced Hold Current MC3484S2 — 2 Amps MC3484S4 — 4 Amps	S/314D	MC3484
Transient Suppressor	Series Transient, opens circuit to protect	T/314D	MC3397T
High Side Driver Switch	Drives loads from positive side of power supply and protects against high-voltage transients.	T/314D	MC3399T
Automotive Direction Indicator	Detects defective lamps and protects against overvoltage and short circuit hazards.	P/626	UAA1041
Peripheral Clamping Array	Protects up to six MPU I/O lines against voltage transients.	626	TCF6000

SPECIAL FUNCTIONS (continued)

Automotive High-Side Driver Switch

MC3399T — $T_J = -40^\circ$ to $+150^\circ\text{C}$, Case 314D

The MC3399T is a High-Side Driver Switch that is designed to drive loads from the positive side of the power supply. The output is controlled by a TTL compatible Enable pin. In the ON state, the device exhibits very low saturation voltages for load currents in excess of 750 mA. The device also protects the load from positive or negative going high voltage transients by becoming an open circuit and isolating the transient for its duration from the load.

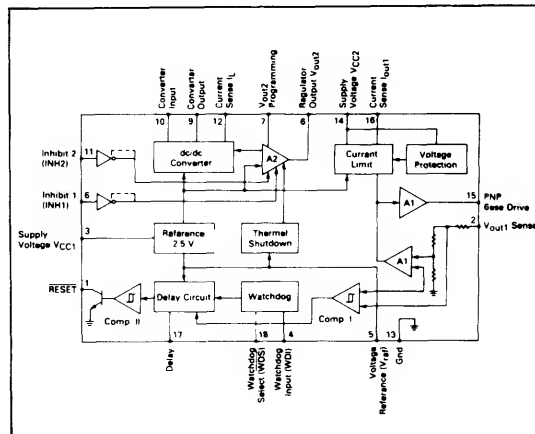


Universal Microprocessor Power Supply Controller

TCA5600 — $T_A = -40^\circ$ to $+85^\circ\text{C}$, Case 707

This device is a versatile power supply control circuit for microprocessor based systems and mainly intended for automotive applications and battery powered instruments. To cover a wide range of applications, the device offers high circuit flexibility with minimum of external components.

Functions included in this IC are a temperature compensated voltage reference, on-chip dc/dc converter, programmable and remote controlled voltage regulator, fixed 5.0 V supply voltage regulator with external PNP power device, undervoltage detection circuit, power-on RESET delay and watchdog feature for orderly microprocessor operations.

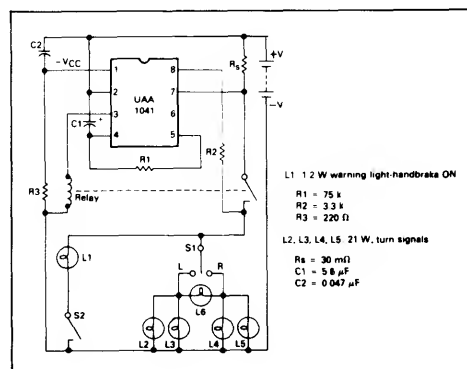


Automotive Direction Indicator

UAA1041,D — $T_A = -40^\circ$ to $+100^\circ\text{C}$, Case 626, 751

... designed for use in conjunction with a relay in automotive applications. It is also applicable for other warning lamps like "handbrake on" etc.

- Defective Lamp Detection
- Overvoltage Protection
- Short Circuit Detection and Relay Shutdown to Prevent Risk of Fire
- Reverse Battery Connection Protection
- Integrated Suppression Clamp Diode



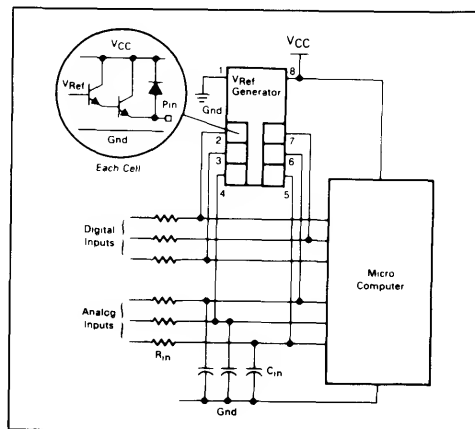
SPECIAL FUNCTIONS (continued)

Peripheral Clamping Array

TCF6000D — $T_A = -40^\circ$ to $+85^\circ\text{C}$, Case 751

... designed to protect input/output lines of microprocessor systems against voltage transients.

- Optimized for HMOS System
- Minimal Component Count
- Low Board Space Requirement
- No P.C.B. Track Crossovers Required
- Other Applications Include Industrial, Telecommunications and Consumer Goods



AUTOMOTIVE ELECTRONIC CIRCUITS

VOLTAGE REGULATORS

Device	Function	Page
LM2931 Series	Low Dropout Voltage Regulator	See Chapter 3
MC3325	Automotive Voltage Regulator	10-6

ELECTRONIC IGNITION

Device	Function	Page
MC3334P	High Energy Ignition Circuit	10-10
MCC3334	High Energy Ignition Circuit	10-10
MCCF3334	High Energy Ignition Circuit	10-10

SPECIAL FUNCTIONS

Device	Function	Page
MC3397T	Transient Suppressor	10-14
MC3399T	Automotive High Side Driver Switch	10-18
MC3484S2-2	Integrated Solenoid Driver	10-21
MC3484S4-2	Integrated Solenoid Driver	10-21
TCA5600/TCF5600	Universal Microprocessor Power Supply Controller	See Chapter 3
TCF6000	Peripheral Clamping Array	10-27
UAA1041	Automotive Direction Indicator	10-31

MC3325

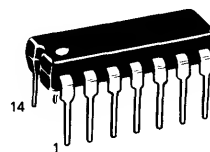
AUTOMOTIVE VOLTAGE REGULATOR

SILICON MONOLITHIC
INTEGRATED CIRCUIT

AUTOMOTIVE VOLTAGE REGULATOR

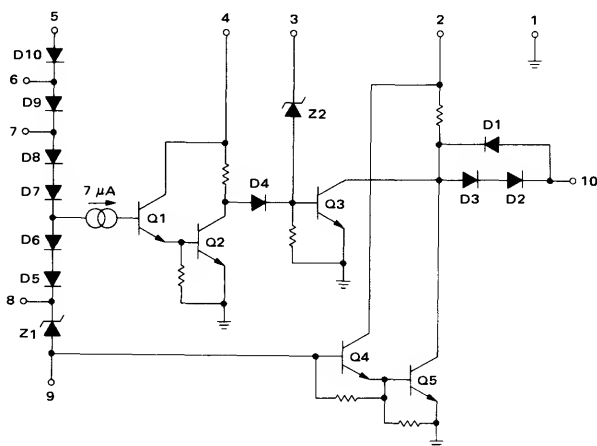
... designed for use in conjunction with an NPN Darlington transistor in a floating field alternator charging system.

- Overvoltage Protection
- Shut-Down on Loss of Battery Sense
- Selectable Temperature Coefficient
- Available in Chip Form for Hybrid Assembly

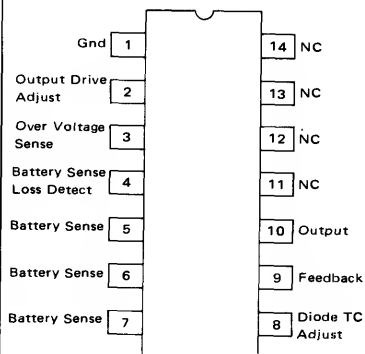


P SUFFIX
PLASTIC PACKAGE
CASE 646

CIRCUIT SCHEMATIC



PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
MC3325P	-40 to +85°C	Plastic DIP

MC3325

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Current Into Pins 5, 6, and 7	$I_{5, 6, \text{ or } 7}$	50	mA
Current Into Pin 3	I_3	20	mA
Current Into Pin 4	I_4	20	mA
Current Into Pin 2	I_2	120	mA
Current Into Pin 8	I_8	50	mA
Current Into Pin 9	I_9	50	mA
Current Into Pin 10	I_{10}	50	mA
Junction Temperature	T_J	150	$^{\circ}\text{C}$
Operating Temperature Range	T_A	-40 to +85	$^{\circ}\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS ($T_A = 25^{\circ}\text{C}$ unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit
Diode TC Adjust: Threshold Voltage on Pin 8 (Figure 1)	V_8	7.9	—	8.95	V
Battery Sense: Threshold Voltage on Pin 5 (Figure 1)	V_5	11.8	—	13.45	V
Battery Sense: Threshold Voltage on Pin 6 (Figure 1)	V_6	11.1	—	12.75	V
Battery Sense: Threshold Voltage on Pin 7 (Figure 1)	V_7	10.5	—	11.9	V
Battery Sense Loss Detect: Threshold Current Into Pin 4 (Figure 2)	I_4	—	—	600	μA
Battery Sense Loss Detect: Threshold Voltage at Pin 4 ($I_4 \leq 400 \mu\text{A}$, Figure 2)	V_4	1.3	—	1.7	V
Overvoltage Sense: Threshold Current Into Pin 3 (Figure 2)	I_3	—	—	600	μA
Overvoltage Sense: Threshold Voltage at Pin 3 ($I_3 \leq 400 \mu\text{A}$, Figure 2)	V_3	6.7	—	9.0	V
Output Drive Adjust: Voltage Drop from Pin 2 to Pin 10 ($I_2 = 10 \text{ mA}$, Figure 3)	V_2	1.9	—	2.4	V
Low State Output Voltage at Pin 10 ($I_3 = 12 \text{ mA}$, $I_2 = 120 \text{ mA}$, Figure 4)	V_{10}	—	—	0.7	V

10

MC3325

TEST CIRCUITS

FIGURE 1

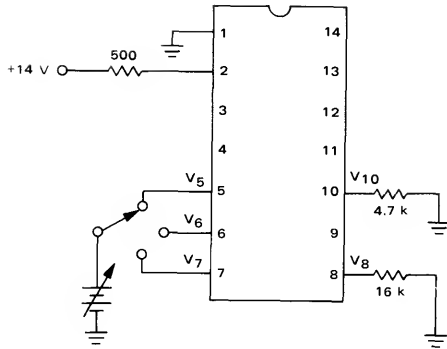


FIGURE 2

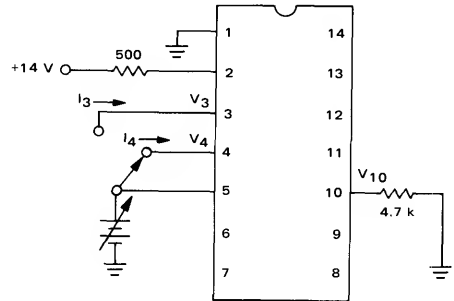


FIGURE 3

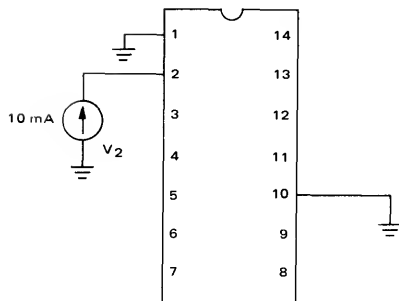
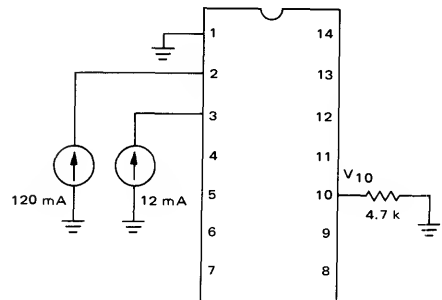
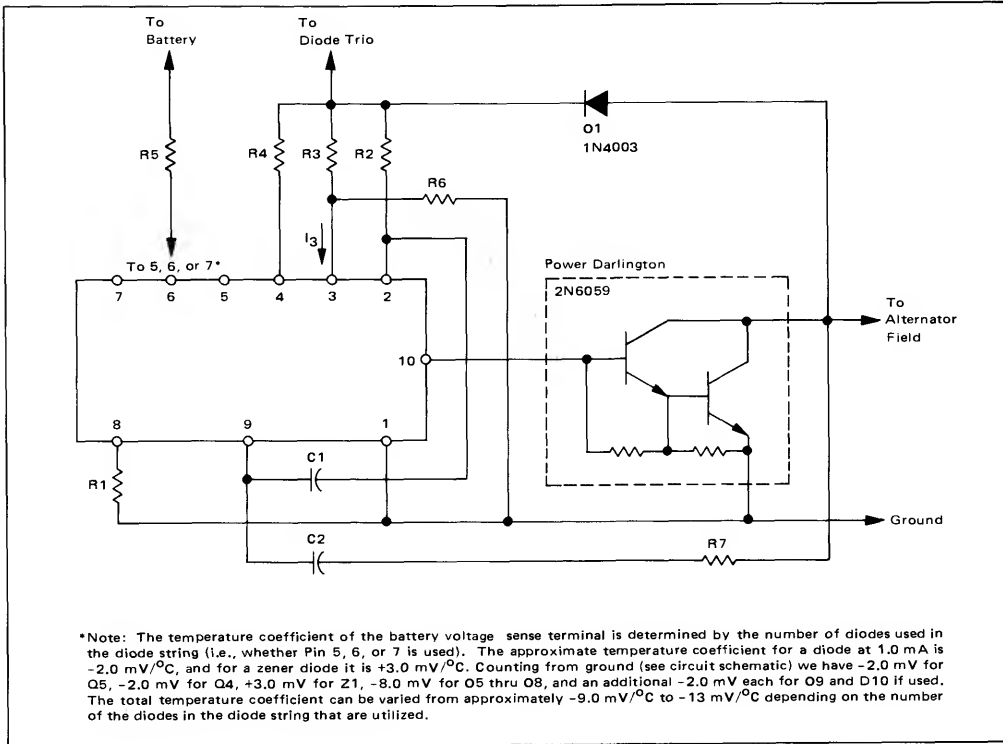


FIGURE 4



10

FIGURE 5 – APPLICATION CIRCUIT



APPLICATIONS CIRCUIT INFORMATION

(See Figure 5)

- R1 Determines the temperature coefficient by setting the value of current in the diode string. As the value of R1 decreases, so does the effective TC. R1 should be chosen so that the current in the diode string is between 0.5 mA and 1.0 mA.
- R5 This resistor determines the V_{reg} voltage as defined by the following equation:
- $$V_{\text{reg}} = \left(1 + \frac{R5}{R1}\right) 8.4 + \left(n + \frac{R5}{5K}\right) (0.7)$$
- n = number of diodes used in diode string ($4 \leq n \leq 6$)
- R4 Used as a current limiting resistor on Pin 4 in case of an open battery voltage sense lead.
- R3 Used as a current limiting resistor on Pin 3 in case of overvoltage at the diode trio. Voltage at Pin 3 will run approximately 7.5 volts. R3 should be chosen so that the current (I_3) at maximum over-

voltage is between 2.0 mA and 6.0 mA.

- R2 This resistor determines the output drive current. Refer to specifications for the darlington driver and select the value for R2 that will provide enough drive to the output when the diode trio voltage is at a minimum.

$$I_{\text{Drive}} \cong \frac{V_{\text{min}} - 2.8 \text{ V}}{R2 + 50 \Omega}$$

- R6 This resistor in conjunction with R3 is used to set the threshold of overvoltage action.

$$\text{Threshold} \cong \frac{R3 + R6}{R6} (7.5)$$

- R7 Used for compensation (Approximately $3.0 \text{ k}\Omega$)
- C1, C2 Used for compensation (Approximately $0.01 \mu\text{F}$)

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

MC3334P MCC3334 MCCF3334

HIGH ENERGY IGNITION CIRCUIT

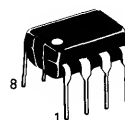
... designed to use the signal from a reductor type ignition pickup to produce a well controlled output from a power Darlington output transistor.

- Very Low Peripheral Component Count
- No Critical System Resistors
- Wide Supply Voltage Operating Range (4.0–24 V)
- Overvoltage Shutdown (30 V)
- Dwell Automatically Adjusts To Produce Optimum Stored Energy Without Waste
- Externally Adjustable Peak Current
- Available in Chip and Flip Chip Form
- Transient Protected Inputs and Outputs

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage — Steady State	V_{BATT}	24	Volts
Transient 300 ms or less		90	
Output Sink Current — Steady State	I_{out}	300	mA
Transient 300 ms or less		1.0	Amps
Junction Temperature	$T_{J(max)}$	150	°C
Operating Temperature Range	T_A	–40 to +125	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Power Dissipation, Package	P_D	1.25	Watts
Derate above 25°C		10	mW/°C

HIGH ENERGY IGNITION CIRCUIT SILICON MONOLITHIC INTEGRATED CIRCUIT

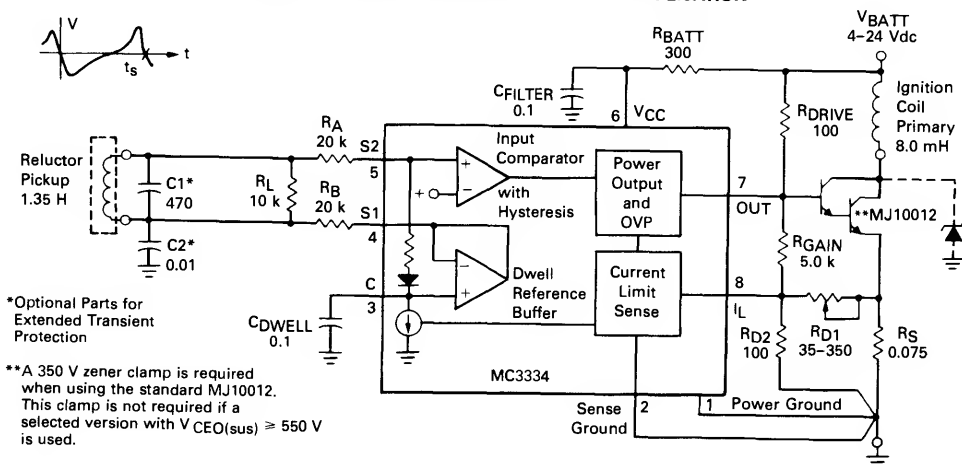


P SUFFIX
PLASTIC PACKAGE
CASE 626

ORDERING INFORMATION

Device	Temperature Range	Package
MC3334P	–40 to +125	Plastic DIP
MCC3334		Chip
MCCF3334		Flip-Chip

FIGURE 1 — BLOCK DIAGRAM AND TYPICAL APPLICATION

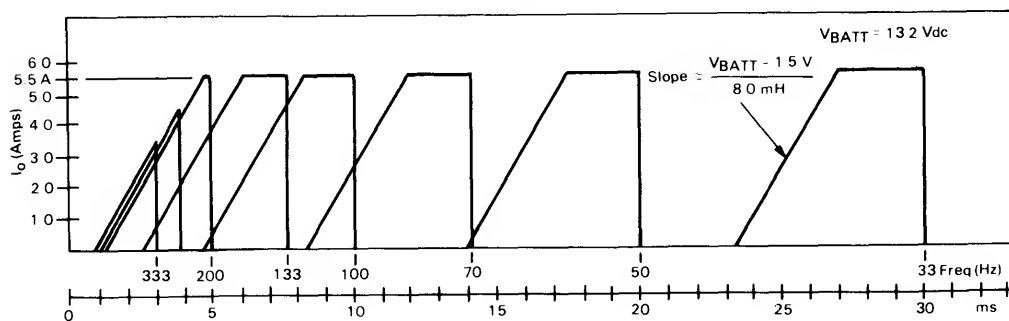


MC3334P, MCC3334, MCCF3334

ELECTRICAL CHARACTERISTICS ($T_A = -40$ to $+125^\circ\text{C}$, $V_{BATT} = 13.2$ Vdc, circuit of Figure 1, unless noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Internal Supply Voltage, Pin 6 $V_{BATT} = 4.0$ Vdc 8.0 Vdc 12.0 14.0	V_{CC}	— — — —	3.5 7.2 10.4 11.8	— — — —	Vdc
Ignition Coil Current Peak, Cranking RPM 2.0 – 27 Hz $V_{BATT} = 4.0$ Vdc 6.0 8.0 10.0	$I_o(pk)$	3.0 4.0 4.6 5.1	3.4 5.2 5.3 5.4	— — — —	A pk
Ignition Coil Current Peak, Normal RPM Freq. = 33 Hz 133 Hz 200 Hz 267 Hz 333 Hz	$I_o(pk)$	5.1 5.1 4.2 3.4 2.7	5.5 5.5 5.4 4.4 3.4	— — — — —	A pk
Ignition Coil On-Time, Normal RPM Range Freq. = 33 Hz 133 Hz 200 Hz 267 Hz 333 Hz	t_{on}	— — — — —	7.5 5.0 4.0 3.0 2.3	14.0 5.9 4.6 3.6 2.8	ms
Shutdown Voltage	V_{BATT}	25	30	35	Vdc
Input Threshold (Static Test) Turn-on Turn-off	$V_{S2}-V_{S1}$	— —	360 90	— —	mVdc
Input Threshold Hysteresis	$V_{S2}-V_{S1}$	75	—	—	mVdc
Input Threshold (Active Operation) Turn-on Turn-off	V_{S2}	— —	1.8 1.5	— —	Vdc
Total Circuit Lag from t_s (Figure 1) until Ignition Coil Current Falls to 10%		—	60	120	μs
Ignition Coil Current Fall Time (90%–10%)		—	4.0	—	μs
Saturation Voltage I.C. Output (Pin 7) ($R_{DRIVE} = 100 \Omega$) $V_{BATT} = 10$ Vdc 30 Vdc 50 Vdc	$V_{CE(sat)}$	— — —	120 280 540	— — —	mVdc
Current Limit Reference, Pin 8	V_{ref}	120	160	190	mVdc

FIGURE 2 — IGNITION COIL CURRENT versus FREQUENCY/PERIOD



MC3334P, MCC3334, MCCF3334

The MC3334 high energy ignition circuit was designed to serve aftermarket Delco five terminal ignition applications. This device, driving a high voltage Darlington transistor, offers an ignition system which optimizes spark energy at minimum power dissipation. The IC is pinned out to permit thick film or printed circuit module design without any crossovers.

CIRCUIT DESCRIPTION

The basic function of an ignition circuit is to permit build-up of current in the primary of a spark coil, and then to interrupt the flow at the proper firing time. The resulting flyback action in the ignition coil induces the required high secondary voltage needed for the spark. In the simplest systems, fixed dwell angle produces a fixed duty cycle, which can result in too little stored energy at high RPM, and/or wasted power at low RPM. The MC3334 uses a variable dc voltage reference, stored on CDWELL, and buffered to the bottom end of the reluctor pickup (S1) to vary the duty cycle at the spark coil. At high RPM, the MC3334 holds the output "off" for approximately 1.0 ms to permit full energy discharge from the previous spark; then it switches the output Darlington transistor into full saturation. The current ramps up at a slope dictated by VBATT and the coil L. At very high RPM the peak current may be less than desired, but it is limited by the coil itself.

As the RPM decreases, the ignition coil current builds up and would be limited only by series resistance losses. The MC3334 provides adjustable peak current regulation sensed by RS and set by RD1, in this case at 5.5 A, as shown in Figure 2. As the RPM decreases further, the coil current is held at 5.5 A for a short period. This provides a reserve for sudden acceleration, when discharge may suddenly occur earlier than expected. The peak hold period is about 20% at medium RPM, decreasing to about 10% at very low RPM. (Note: 333 Hz = 5000 RPM for an eight cylinder four stroke engine.) At lower VBATT, the "on" period automatically stretches to accommodate the slower current build-up. At very low VBATT and low RPM, a common condition during cold starting, the "on" period is nearly the full cycle to permit as much coil current as possible.

The output stage of the IC is designed with an OVP circuit which turns it on at VBATT ≈ 30 V (VCC ≈ 22 V), holding the output Darlington off. This protects the IC and the Darlington from damage due to load dump or other causes of excessive VBATT.

COMPONENT VALUES

- PICKUP** — series resistance = $800 \Omega \pm 10\%$ @ 25°C
inductance = $1.35 \text{ H} @ 1.0 \text{ kHz} @ 15 \text{ Vrms}$.
- COIL** — leakage L = 0.6 mH
primary R = $0.43 \Omega \pm 5\%$ @ 25°C
primary L = $7.5 \text{ to } 8.5 \text{ mH} @ 5.0 \text{ A}$
- RL** — load resistor for pick-up = $10 \text{ k}\Omega \pm 20\%$

- RA, RB** — input buffer resistors, provide additional transient protection to the already clamped inputs = $20 \text{ k} \pm 20\%$
- C1, C2** — for reduction of high frequency noise and spark transients induced in pick-up and leads; optional and non-critical
- RBATT** — provides load dump protection (but small enough to allow operation at VBATT = $4.0 \text{ V} = 300 \Omega \pm 20\%$)
- CFILTER** — transient filter on VCC, non-critical
- CDWELL** — stores reference, circuit designed for $0.1 \mu\text{F} \pm 20\%$
- RGAIN** — RGAIN/RD1 sets the dc gain of the current regulator = $5.0 \text{ k} \pm 20\%$
- RD2** — RD2/RD1 set up voltage feedback from RS
- RS** — sense resistor (PdAg in thick film techniques) = $0.075 \Omega \pm 30\%$
- RDRIVE** — low enough to supply drive to the output Darlington, high enough to keep VCE(sat) of the IC below Darlington turn-on during load dump = $100 \Omega \pm 20\%$, 5.0 W
- RD1** — starting with 35Ω assures less than 5.5 A, increasing as required to set 5.5 A

$$RD1 = \frac{I_{o(pk)} RS - V_{ref}}{\frac{V_{ref}}{RD2} - \frac{1.4}{RGAIN}} \approx 100 \Omega (\text{nom})$$

GENERAL LAYOUT NOTES

The major concern in the substrate design should be to reduce ground resistance problems. The first area of concern is the metallization resistance in the power ground to module ground and the output to the RDRIVE resistor. This resistance directly adds to the VCE(sat) of the IC power device and if not minimized could cause failure in load dump. The second concern is to reference the sense ground as close to the ground end of the sense resistor as possible in order to further remove the sensitivity of ignition coil current to ground I.R. drops.

All versions were designed to provide the same pin-out order viewed from the top (component side) of the board or substrate. This was done to eliminate conductor cross-overs. The standard MC3334 plastic device is numbered in the industry convention, counter-clockwise viewed from the top. The MCC3334 chip version is made from the same die artwork, so it is also counter-clockwise viewed from the top, or bonding pad side. The MCCF3334 "flip" or "bump" chip is made from reversed artwork, so it is numbered clockwise viewed from its bump side. Since this chip is mounted face down, the resulting assembly still has the same counter-clockwise order viewed from above the component surface. All chips have the same size and bonding pad spacing. See Figure 4 for dimensions.

MC3334P, MCC3334, MCCF3334

FIGURE 3 — INTERNAL SCHEMATIC

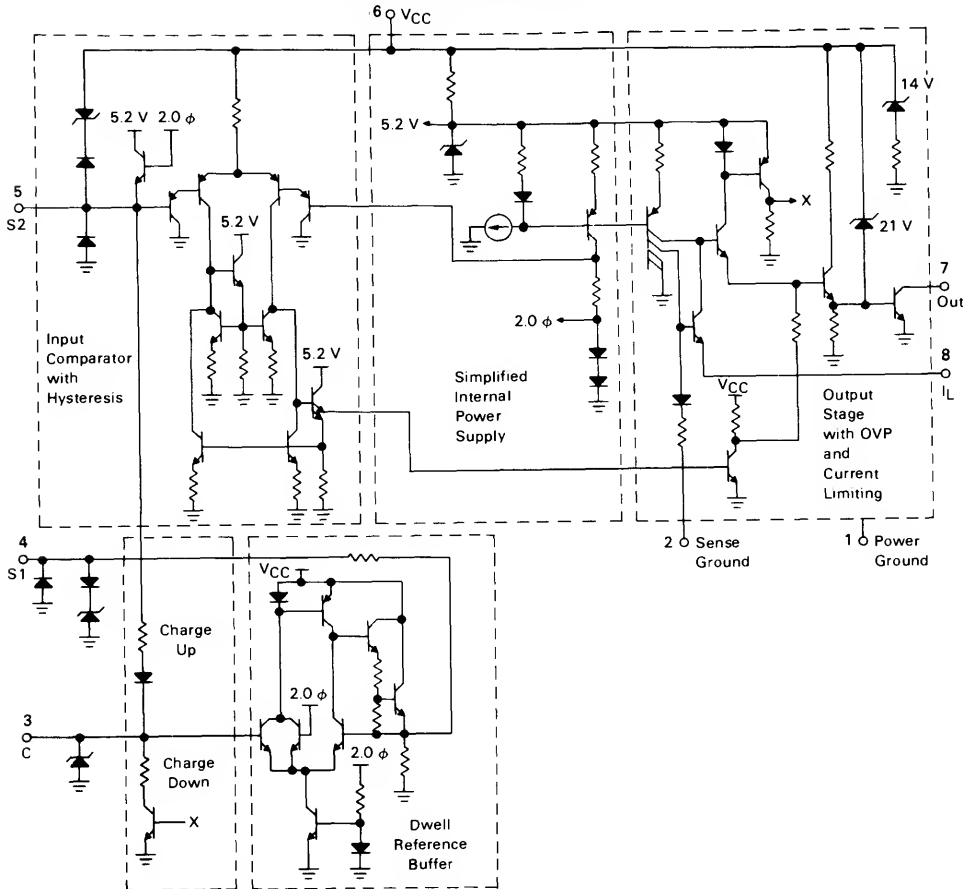
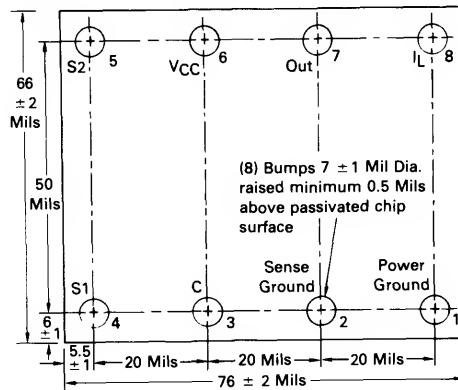


FIGURE 4 — MCCF3334 IGNITION CIRCUIT BUMP SIDE VIEW



MC3397T

Advanced Information

SERIES SWITCH TRANSIENT PROTECTOR

The MC3397T is a Series Switch Transient Protection Circuit. Under normal operating voltage conditions, the device acts as a saturated series pass device with a very low voltage drop for load currents in excess of 750 mA. In the event of an overvoltage condition (≥ 17.5 V typ) or high voltage transient of either polarity, the MC3397T switches to an open circuit (OFF) state, interrupting power to the load and protecting it during this potentially destructive condition. The device will automatically reset to an ON state when the supply voltage falls within the normal range again.

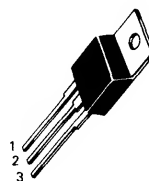
The MC3397T is fabricated on a power BiMOS process which combines the best features of Bipolar and MOS technologies. The mixed technology provides higher gain PNP output devices and results in Power Integrated Circuits with reduced quiescent current.

The device operates in its ON state over a wide voltage range of 4.5 V to 16 V and can withstand voltage transients of ± 85 V. A rugged PNP output stage along with current limiting permits driving all types of loads, including incandescent and inductive. The MC3397T is specified over a wide junction temperature range of -40°C to $+125^{\circ}\text{C}$ and is ideally suited for industrial and automotive applications where harsh environments exist.

- Transient Protection up to ± 85 V
- Load Currents in Excess of 750 mA
- Low Voltage Drop
- Fast Shutdown and Recovery to Transients
- Transient Energy Passed to the Load is Minimized (10 μJ Typ)
- On-Chip Current Limiting
- Capacitor May Be Used to Support Load During Transient
- Extended Operating Temperature Range
- Power BiMOS Technology

SERIES SWITCH TRANSIENT PROTECTOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

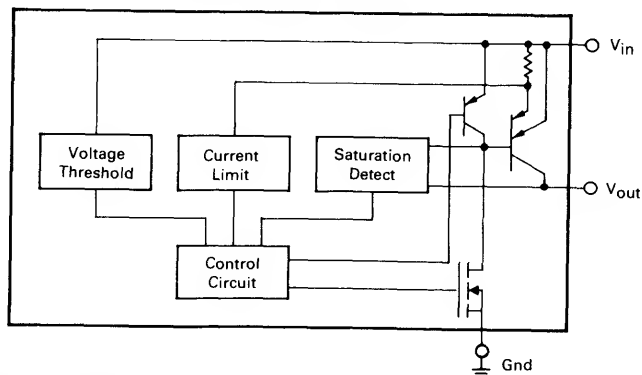


T SUFFIX
 PLASTIC PACKAGE
 CASE 221A

PIN 1. Input
 2. Output
 3. Ground

(Heatsink surface
 connected to Pin 2)

FIGURE 1 — BLOCK DIAGRAM



This document contains information on a new product. Specifications and information here are subject to change without notice.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage, Continuous	V_{in}	± 85	Vdc
Output Current	I_O	Internally Limited	A

THERMAL CHARACTERISTICS

Rating	Symbol	Min	Max	Unit
Junction Temperature	T_J	-40	+125	$^{\circ}\text{C}$
Operating Storage	T_{stg}	-65	+150	
Thermal Resistance	θ_{JA}	—	62.5	$^{\circ}\text{C/W}$
Junction to Ambient	θ_{JC}	—	1.6	
Junction to Case				

DEFINITION OF CURRENTS AND VOLTAGES Positive current is defined as conventional current flow into the device. Negative current is defined as flow out of the device. All voltages are referenced to ground. Both currents and voltages are compared as absolute values (i.e., -10 volts is greater than -1.0 volt).

ELECTRICAL CHARACTERISTICS ($V_{in} = +12\text{ V}$, $I_L = -150\text{ mA}$, $-40^{\circ}\text{C} \leq T_J \leq +125^{\circ}\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Minimum Operating Voltage	$V_{in(min)}$	—	2.5	4.5	V
Quiescent Current $I_L = -150\text{ mA}$, $V_{in} = 4.5\text{ V}$ $I_L = -500\text{ mA}$, $V_{in} = 12\text{ V}$ $I_L = -750\text{ mA}$, $V_{in} = 16\text{ V}$	I_B	— — —	-8.0 -24 -39	-15 -40 -50	mA
Switch Voltage Drop $I_L = -150\text{ mA}$, $V_{in} = 4.5\text{ V}$ $I_L = -500\text{ mA}$, $V_{in} = 12\text{ V}$ $I_L = -750\text{ mA}$, $V_{in} = 16\text{ V}$	$V_{in}-V_O$	— — —	150 250 320	250 500 800	mV
Output Current Limit	I_{OSC}	-0.8	-1.5	-2.2	A
Output Leakage Current $18\text{ V} < V_{in} < 85\text{ V}$, $V_O = 14\text{ V}$	I_{LEAK}	—	-10	-45	mA
Over Voltage Shutdown Threshold	$V_{in(OV)}$	16	17.5	18.5	V
Output Turn-Off Delay Time V_{in} stepped from 12 V to 40 V, $V_O = 10.5\text{ V}$ (Figure 2)	t_{DLY}	—	10	50	μs
Output Recovery Delay Time V_{in} stepped from 40 V to 12 V, $V_O = 10.5\text{ V}$ (Figure 2)	t_{RCVY}	—	7.0	30	μs

FIGURE 2 — RESPONSE TIME DIAGRAM

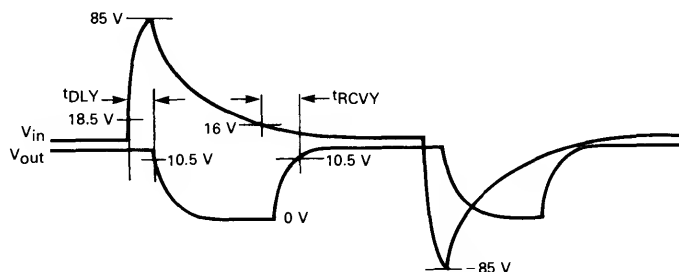


FIGURE 3 — RESPONSE TIME TEST CIRCUIT

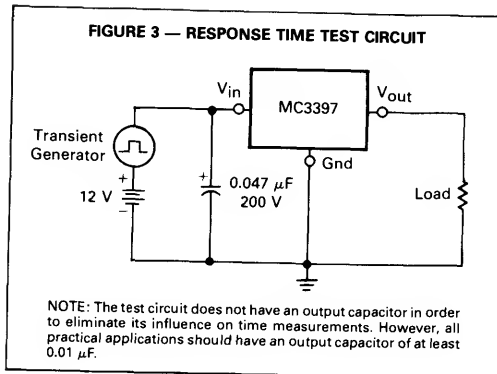


FIGURE 4 — DELAY AND RECOVERY TIME versus LOAD CURRENT

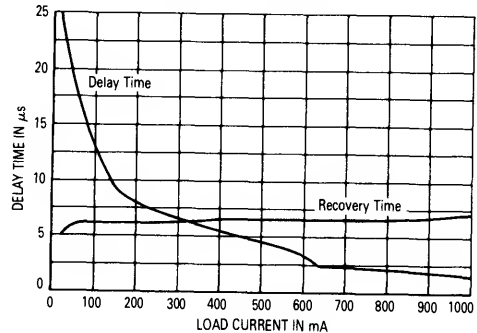


FIGURE 5 — SWITCH DROP versus LOAD CURRENT

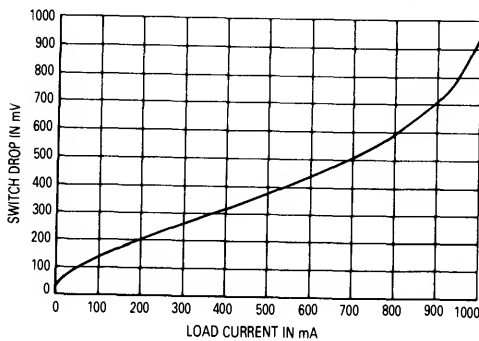
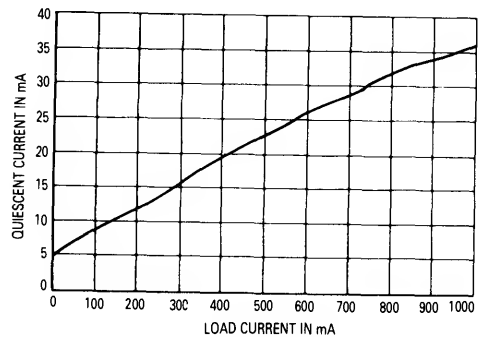


FIGURE 6 — QUIESCENT CURRENT versus LOAD CURRENT



SERIES TRANSIENT PROTECTION

Zener diodes and other devices are often used as shunt mode transient protectors. The MC3397 provides series mode protection which has some advantages over shunt mode. The first advantage is that series mode protection is more precise. There is a very small variation in trip voltage due to temperature or the magnitude of the transient, compared to the variations found in power devices used for shunt protection. A disadvantage of shunt mode, is that the load continues to operate during the transient at the shunt device's breakdown voltage. The amount of excess energy the load has to absorb is significant in some cases. Series mode protection results in less excess energy passed to the load. An 85 volt transient will cause only 10 μJ (typical) of excess energy to be passed on to the load regardless of the transient's duration.

INPUT CAPACITOR

A capacitor of at least 0.01 μF or larger, is required to be connected from the MC3397's input pin to its ground pin. The capacitor should have sufficient voltage

rating to withstand the largest possible transient voltage and good ESR characteristics. It should also be located as close to the MC3397 as possible.

OUTPUT CAPACITOR

A 0.01 μF capacitor should also be connected from Output to Ground on the MC3397. A larger capacitor has no advantage or effect on the device, but may be desirable for the load. There are two possible advantages for the load. The most common one is that the output capacitor can serve as a power source to keep the load operating during a transient. Since the MC3397 switches to an open circuit during a transient, there will be no power supplied to the load. A capacitor on the output pin can be sized to store enough energy to keep the load operating. The output capacitor will act in the same manner as a power supply filter capacitor. The size of the required capacitor is calculated as follows:

$$C = \frac{I(\Delta T)}{\Delta V}$$

Where; C = The required capacitor value in farads
 I = The constant current drain in amps
 ΔT = The duration of the transient in seconds
 ΔV = The allowable voltage drop in volts

The second advantage of a larger capacitor does not apply to most loads. When a high voltage transient occurs, the MC3397 will take a finite amount of time to switch off. During the switching time there is a certain amount of energy that will pass through the MC3397 to the Output. Typically, this is only a few microjoules. However, energy will be stored in the output capacitor according to the formula;

$$E = \frac{C (V^2)}{2}$$

Where; E = Energy in microjoules
 C = Capacitance in microfarads
 V = Voltage rise across the capacitor in volts

Loads which are extremely sensitive to higher voltages regardless of their time duration can be protected by increasing the value of the capacitor. For most loads a 22 μ F capacitor will reduce the size of the voltage transient so that it becomes virtually undetectable.

THERMAL

In most applications, the MC3397 does not need an external heatsink. If it is operated only in its saturated mode then the low saturation voltage, combined with the good thermal characteristics of the TO-220 package, allow it to operate in ambient temperatures above 80°C without an additional heatsink.

If the MC3397 will be used in a very high ambient temperature, or if it will be operated in a current limiting mode, then a heatsink may be required. Current limiting requires special care. The power dissipation of the device increases very rapidly in the current limit mode and can quickly become three times or more the power dissipation in the saturated mode.

VARYING VOLTAGE THRESHOLDS

The MC3397 determines when to shut down and open the circuit by measuring the voltage between its input and ground pins. A zener diode inside the MC3397, between the input and ground pins, is the main component involved. When current starts to flow through this zener diode the MC3397 switches to an open circuit (OFF) state.

The apparent trip voltage can be changed by adding an additional voltage drop between the ground pin and true ground. For example, inserting a 6.8 V zener diode between the ground pin and true ground would change the voltage threshold from the MC3397's 17.5 V to 17.5 + 6.8 or 24.3 V. If a -5.0 V supply is available in the system then the ground pin could be connected to this supply which would change the trip voltage at the input to +12.5 V. Note that changing the trip points by the use of zener diodes will also change its maximum voltage ratings. If a 6.8 V zener is used then 6.8 V will be added to its maximum positive voltage and 0.7 V will be added to its maximum negative voltage. The only constraint on any device connected to the MC3397's ground to change its trip point is that the quiescent current must be able to flow through it freely.

It may be possible to have the input and output capacitors connected to system ground rather than the MC3397's ground, but the most reliable operation will be achieved if there are capacitors connected between the input and output pins and the MC3397's ground pin.

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

AUTOMOTIVE HIGH-SIDE DRIVER SWITCH

The MC3399T is a High-Side Driver Switch that is designed to drive loads from the positive side of the power supply. The output is controlled by a TTL compatible Enable pin. In the ON state, the device exhibits very low saturation voltages for load currents in excess of 750 mA. The device also protects the load from positive or negative going high voltage transients by becoming an open circuit and isolating the transient for its duration from the load.

The MC3399T is fabricated on a power BIMOS process which combines the best features of Bipolar and MOS technologies. The mixed technology provides higher gain PNP output devices and results in Power Integrated Circuits with reduced quiescent current.

The device operates over a wide power supply voltage range and can withstand voltage transients (positive or negative) of ± 100 V. A rugged PNP output stage along with active clamp circuitry, current limit and thermal shutdown permits driving of all types of loads including inductive. The MC3399T is specified over a wide junction temperature of -40°C to $+125^{\circ}\text{C}$ and is ideally suited for industrial and automotive applications where harsh environments exist.

- Low Switch Voltage Drop
- Load Currents in Excess of 750 mA
- Low Quiescent Current
- Transient Protection Up to ± 100 V
- TTL Compatible Enable Input
- On-Chip Current Limit and Thermal Shutdown Circuitry

MAXIMUM RATINGS

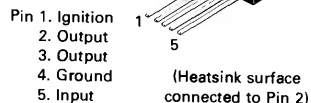
Rating	Symbol	Value	Unit
Ignition Input Voltage — Continuous	V_{IGN}	+25 -12	Vdc
Ignition Input Voltage — Transient $t = 100$ ms $t = 1.0$ ms	V_{IGN}	± 60 ± 100	V
Input Voltage	V_{in}	-0.3 to +7.0	V
Output Current	I_O	Internally Limited	A
Power Dissipation and Thermal Characteristics $T_A = +25^{\circ}\text{C}$ Derate above $T_A = +25^{\circ}\text{C}$	P_D $1/\theta_{JA}$	2.0 16	Watts $\text{mW}/^{\circ}\text{C}$
Thermal Resistance Junction to Ambient $T_C = +25^{\circ}\text{C}$ Derate above $T_C = +25^{\circ}\text{C}$	θ_{JA} P_D $1/\theta_{JA}$	65 25 200	$^{\circ}\text{C}/\text{W}$ Watts $\text{mW}/^{\circ}\text{C}$
Thermal Resistance Junction to Case	θ_{JC}	5.0	$^{\circ}\text{C}/\text{W}$
Operating Junction Temperature Range	T_J	-40 to +125	$^{\circ}\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^{\circ}\text{C}$

MC3399T

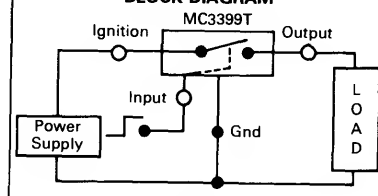
AUTOMOTIVE HIGH-SIDE DRIVER SWITCH

SILICON MONOLITHIC INTEGRATED CIRCUIT

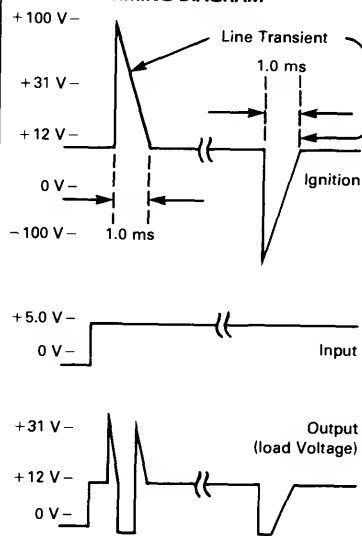
T SUFFIX
PLASTIC PACKAGE
CASE 314D



BLOCK DIAGRAM



TIMING DIAGRAM



MC3399T

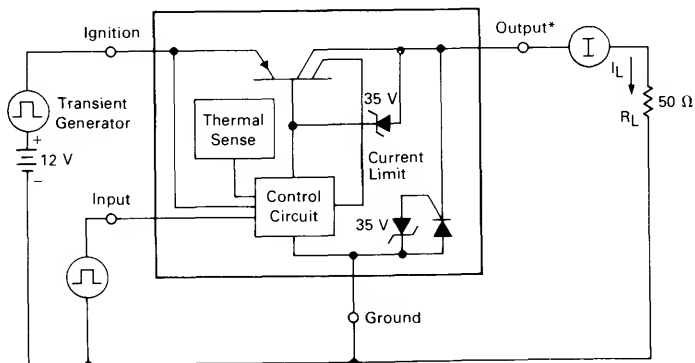
ELECTRICAL CHARACTERISTICS ($V_{IGN} = +12\text{ V}$, $I_L = 150\text{ mA}$, $-40^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$, $V_{\text{Input}} = "1"$ unless noted)*

Characteristic	Symbol	Min	Typ	Max	Unit
Operating Voltage	$V_{IGN(min)}$	4.5	—	—	V
Switch Voltage Drop (Saturation) $V_{IGN} = 4.5\text{ V}$ $I_O = 150\text{ mA}$ $T_J = 25^\circ\text{C}$ $I_O = 200\text{ mA}$ $T_J = -40^\circ\text{C}$ $I_O = 125\text{ mA}$ $T_J = 125^\circ\text{C}$ $V_{IGN} = 12\text{ V}$ $I_O = 425\text{ mA}$ $T_J = 25^\circ\text{C}$ $I_O = 550\text{ mA}$ $T_J = -40^\circ\text{C}$ $V_{IGN} = 16\text{ V}$ $I_O = 375\text{ mA}$ $T_J = 125^\circ\text{C}$	V_{IGN-VO}	— — — — — —	0.2 0.3 0.3 0.3 0.3 0.4	0.5 0.5 0.5 0.7 0.7 0.7	V
Quiescent Current $V_{IGN} = 12\text{ V}$ $I_O = 150\text{ mA}$ $T_J = 25^\circ\text{C}$ $I_O = 550\text{ mA}$ $T_J = -40^\circ\text{C}$ $I_O = 300\text{ mA}$ $T_J = 125^\circ\text{C}$	I_{GND}	— — —	12 25 10	50 100 50	mA
Output Current Limit $V_O = 0\text{ V}$	I_{SC}	—	1.6	2.5	A
Output Leakage Current $V_{IGN} = 12\text{ V}$, Input = "0"	I_{Leak}	—	10	150	μA
Input Voltage High Logic State Low Logic State	V_{IH} V_{IL}	2.0 —	— —	— 0.8	V
Input Current High Logic State ($V_{IH} = 5.5\text{ V}$) Low Logic State ($V_{IL} = 0.4\text{ V}$)	I_{IH} I_{IL}	— —	120 20	— —	μA
Output Turn-On Delay Time Input = "0" \rightarrow "1," $T_J = +25^\circ\text{C}$ (Figures 1 and 2)	$t_{DLY(on)}$	—	50	—	μs
Output Turn-Off Delay Time Input = "1" \rightarrow "0," $T_J = +25^\circ\text{C}$ (Figures 1 and 2)	$t_{DLY(off)}$	—	5.0	—	μs
Over Voltage Shutdown Threshold	$V_{in(OV)}$	26	31	36	V
Output Turn-Off Delay Time ($T_J = +25^\circ\text{C}$) to Over Voltage Condition, V_{in} stepped from 12 V to 40 V, $V \leq 0.9 V_O$ (Figures 1 and 2)	t_{DLY}	—	2.0	—	μs
Output Recovery Delay Time ($T_J = +25^\circ\text{C}$) V_{IGN} stepped from 40 V to 12 V, $V \geq 0.9 V_O$ (Figures 1 and 2)	t_{RCVY}	—	5.0	—	μs

NOTE:

*Typical Values Represent Characteristics of Operation at $T_J = -25^\circ\text{C}$.

FIGURE 1 — TRANSIENT RESPONSE TEST CIRCUIT



NOTE:

*Depending on Load Current and Transient Duration, an Output Capacitor (C_O) of sufficient value may be used to hold up Output Voltage during the Transient, and absorb Turn-off Delay Voltage Overshoot.

FIGURE 2 — RESPONSE TIME DIAGRAM

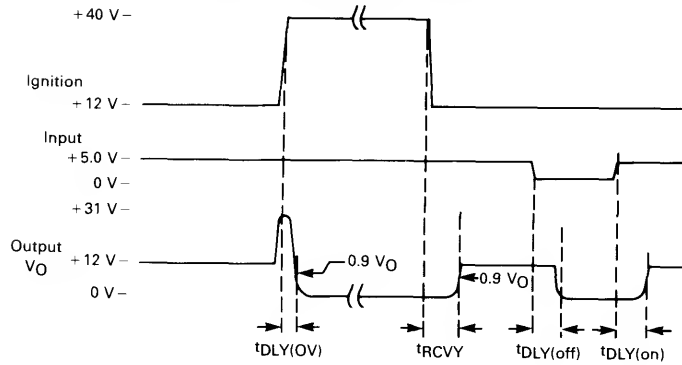


FIGURE 3 — SWITCH VOLTAGE DROP versus LOAD CURRENT

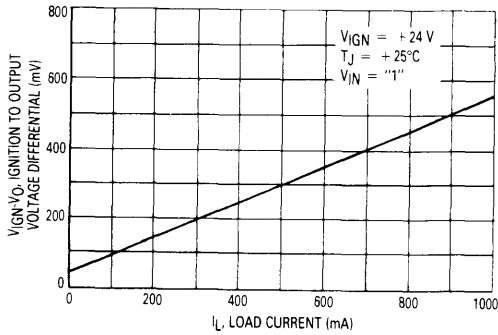
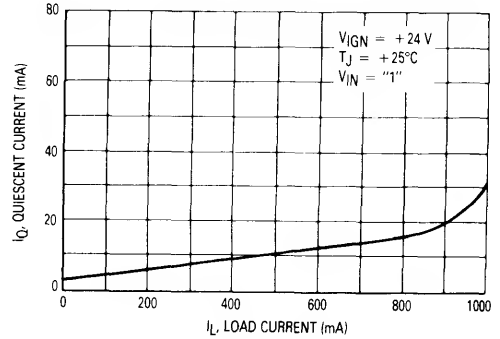


FIGURE 4 — QUIESCENT CURRENT versus LOAD CURRENT



MC3484S2-2, MC3484S4-2

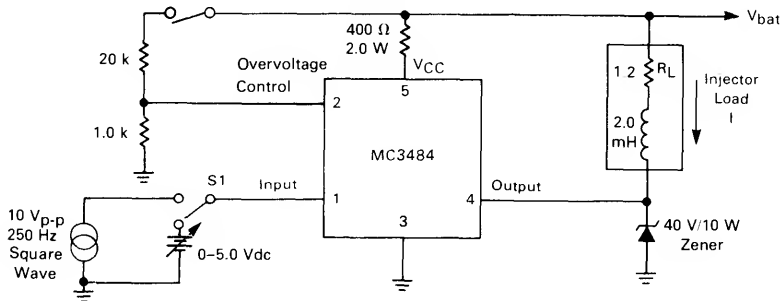
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{bat})	V_{bat}	24	Volts
Input (Pin 1)	V_{in}	-0.3 to +6.0	V
Control (Pin 2)	V_{cont}	0 to +5.0	V
Internal Regulator (Pin 5)	—	50	mA
Junction Temperature	T_J	150	°C
Operating Temperature (T_A Temperature)	T_A	-40 to +105	°C
Storage Temperature	T_{stg}	-65 to +150	°C
Thermal Resistance, Junction to Case	θ_{JC}	2.5	°C/W

ELECTRICAL CHARACTERISTICS ($V_{bat} = 12$ Vdc, $T_C = -40^\circ$ to $+85^\circ$ C, test circuit of Figure 2, unless noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Peak Current S4-2	$I_{pk}(\text{sense})$	3.6 1.7	4.0 2.4	5.2 2.9	A
Output Sustaining Current	I_{sus}	0.95 0.50	1.0 0.6	1.3 0.7	A
$V_{CEO}(\text{sus})$ @ 2.0 A	—	42	50	—	V
Output Voltage in Saturated Mode S2 @ 1.5 A S4 @ 3.0 A	V_{out}	— —	1.2 1.6	— —	V
Internal Regulated Voltage (V_{CC} , Figure 2)	V_{reg}	—	7.1	—	V
Input "On" Threshold Voltage	V_{on}	—	1.4	2.0	V
Input "Off" Threshold Voltage	V_{off}	0.7	1.3	—	V
Input "On" Current @ $V_I = 2.0$ Vdc @ $V_I = 5.0$ Vdc	I_{in}	— —	50 220	— —	μ A
Control "On" Threshold Voltage (Pin 2)	V_{cont}	—	1.5	—	V
Control "On" Current	I_{in2}	—	75	—	μ A
Control Pin Impedance	V_I Low	—	10	—	k Ω
Input Turn On Delay	t_i	—	0.5	—	μ s
I_{pk} sense to I_{sus} delay	t_p	—	60	—	μ s
Control Signal Delay	t_t	—	15	—	μ s
Input Turn Off from Saturated Mode Delay	t_s	—	1.0	—	μ s
Input Turn Off from Sustain Mode Delay	t_d	—	0.2	—	μ s
Output Voltage Rise Time	t_v	—	0.4	—	μ s
Output Current Fall Time 2.0 A 4.0 A	t_f	— —	0.3 0.6	— —	μ s

FIGURE 2 — TEST CIRCUIT



MC3484S2-2, MC3484S4-2

GENERAL INFORMATION

Inductive actuators such as automotive electronic fuel injectors, relays, solenoids and hammer drivers can be powered more efficiently by providing a high current drive until actuation (pull-in) occurs and then decreasing the drive current to a level which will sustain actuation. Pull-in and especially drop-out times of the actuators are also improved.

The fundamental output characteristic of the MC3484 provides a low impedance saturated power switch until the load current reaches a predetermined high-current level and then changes to a current source of lower magnitude until the device is turned off. This output characteristic allows the inductive load to control its actuation time during turn-on while minimizing power and stored energy during the sustain period, thereby promoting a fast turn-off time.

Automotive injectors at present come in two types. The large throttle body injectors have an impedance of about 2.0 mH and 1.2 Ω and require the MC3484S4 driver. The smaller type, popular world-wide, has an impedance of 4.0 mH and 2.4 Ω and needs about a 2.0 A pulse for good results. Some designs are planned which employ two of the smaller types in parallel. The inductance of an injector is much larger at low current, decreasing due to armature movement and core saturation to the values above at rated current.

Operating frequencies range from 5.0 Hz to 250 Hz depending on the injector location and engine type. Duty cycle in some designs reaches 80%.

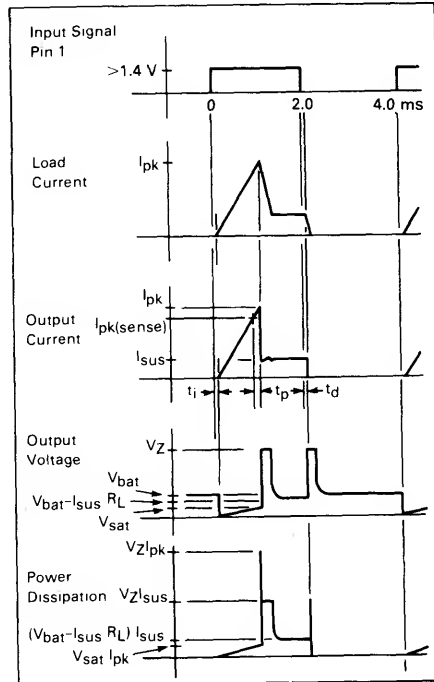
APPLICATIONS INFORMATION

The MC3484 is provided with an input pin (Pin 1) which turns the injector driver "on" and "off." This pin has a nominal trip level of 1.4 V and an input impedance of 20 k Ω . It is internally protected against negative voltages and is compatible with TTL and most other logic.

There is also a control pin (Pin 2) which may be used as an overvoltage, load dump, shutdown. When a nominal 1.5 V is applied to Pin 2, via a 20:1 voltage divider the driver and circuit are set in a safe off state at 30 V (V_{bat}).

Figure 3 shows the operating waveforms for the simplest mode, i.e., with control Pin 2 grounded. When the driver is turned on, the current ramps up to the peak current sense level, where some overshoot occurs because of internal delay. The MC3484 then reduces its output to I_{sus} . The fall time of the device is very rapid ($\leq 1.0 \mu s$), but the decay of the load current takes 150 to 220 μs while dumping the load energy into the protection zener clamp. It is essential that the zener voltage

FIGURE 3 — OPERATING WAVEFORMS
(Max Frequency 250 Hz, Pin 2 Grounded)



be lower than the $V_{CE0(sus)}$, but not so low as to greatly stretch the load current decay time. Without the zener, the discharge of the load energy would be totally into the MC3484, which, for the high current applications, could cause the device to fail. (See SOA, Figure 11.)

Also in Figure 3 is the graphically derived instantaneous power dissipation of the MC3484. It shows that, for practical purposes, the worst case dissipation is less than $(I_{sus})(V_{bat})$ (duty cycle).

Provided in Figures 3 and 4 are definitions of the switching intervals specified in the Electrical Characteristics. Figure 5 shows that the critical switching parameters stay under control at elevated temperatures.

MC3484S2-2, MC3484S4-2

FIGURE 4 — SWITCHING WAVEFORMS
(Expanded Time Scale)

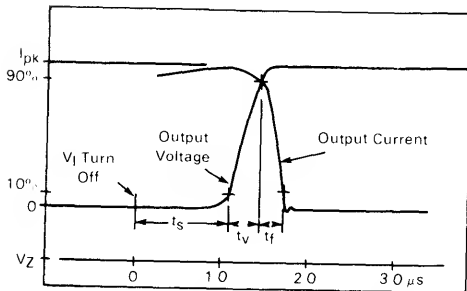
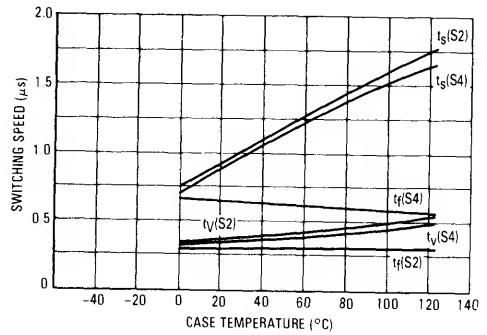


FIGURE 5 — SWITCHING SPEED versus TEMPERATURE



TYPICAL CHARACTERISTICS

(Unless otherwise noted: Test circuit of Figure 2, $V_{bat} = 12 \text{ Vdc}$, $T_C = -40^\circ \text{ to } +85^\circ \text{C}$, 250 Hz square wave input)

FIGURE 6 — OUTPUT CURRENT versus TEMPERATURE

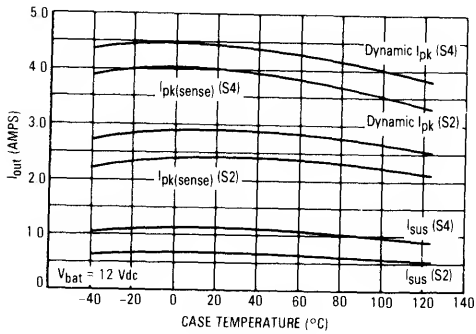
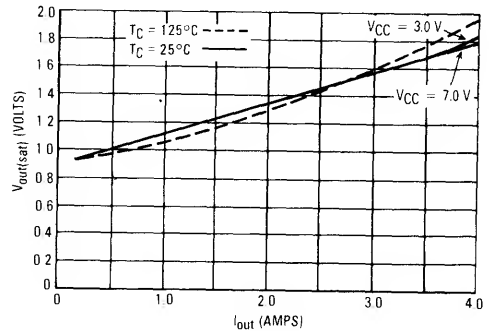


FIGURE 7 — SATURATION VOLTAGE



MC3484S2-2, MC3484S4-2

TYPICAL CHARACTERISTICS

(Unless otherwise noted: Test circuit of Figure 2, $V_{bat} = 12$ Vdc, $T_C = -40^\circ$ to $+85^\circ\text{C}$, 250 Hz square wave input)

FIGURE 8 — OUTPUT CURRENT versus SUPPLY VOLTAGE

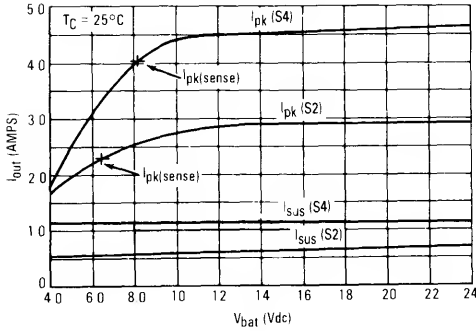


FIGURE 9 — OPERATING VOLTAGES

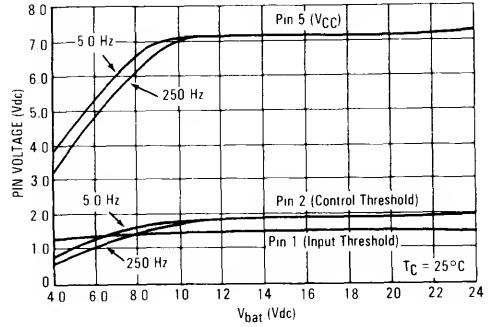


FIGURE 10 — BREAKDOWN VOLTAGE versus TEMPERATURE

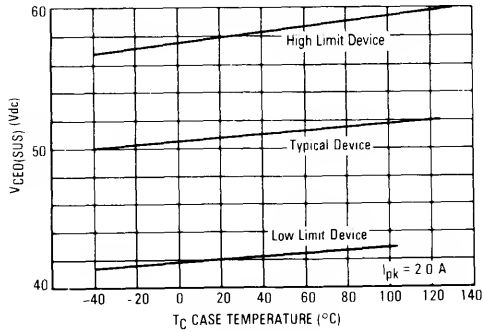


FIGURE 11 — SAFE OPERATING AREA

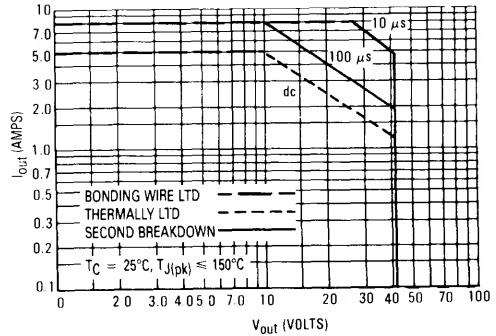
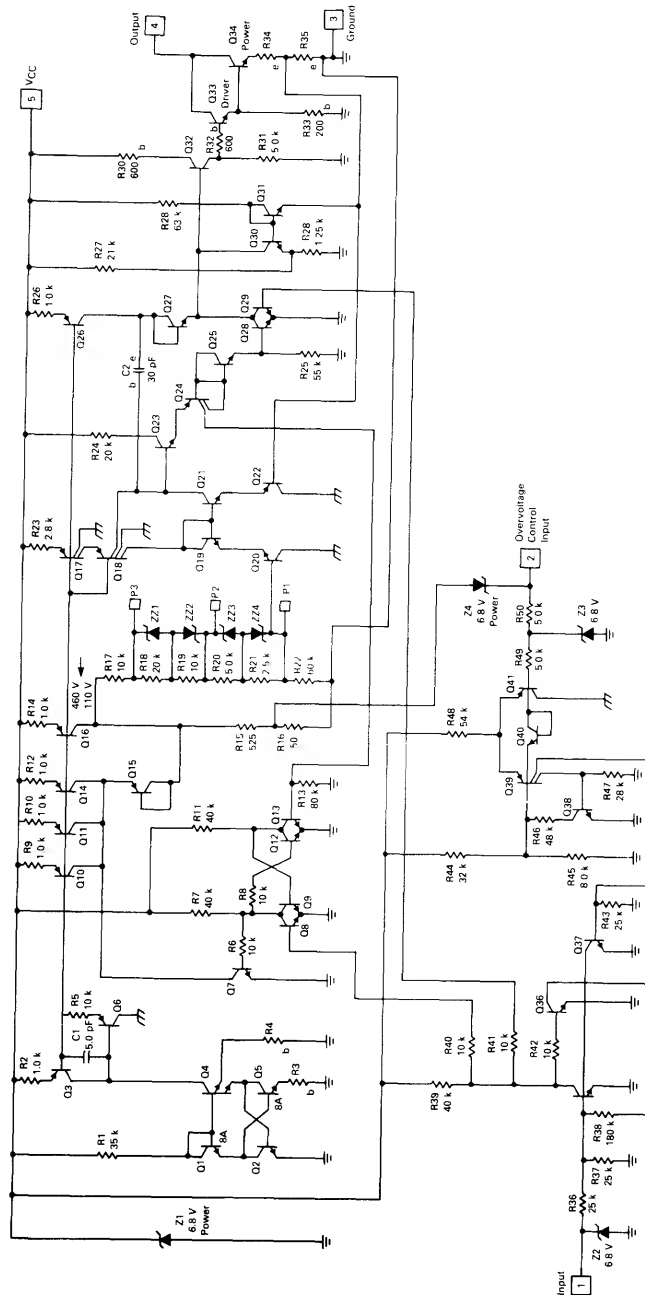


FIGURE 12 — INTERNAL SCHEMATIC



TCF6000

PERIPHERAL CLAMPING ARRAY

SILICON MONOLITHIC
 INTEGRATED CIRCUIT

PERIPHERAL CLAMPING ARRAY

... designed to protect input/output lines of microprocessor systems against voltage transients.

- Optimized for HMOS System
- Minimal Component Count
- Low Board Space Requirement
- No P.C.B. Track Crossovers Required
- Applications Areas Include Automotive, Industrial, Telecommunications and Consumer Goods

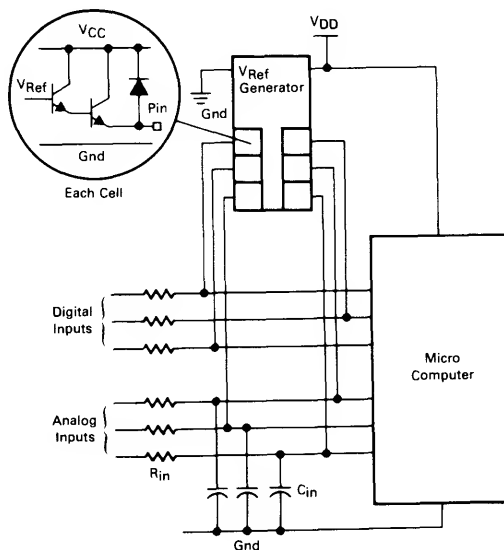
D SUFFIX
 PLASTIC PACKAGE
 CASE 751
 (SO-8)



PIN ASSIGNMENT

Gnd	1	8	VCC
Clamp	2	7	Clamp
Clamp	3	6	Clamp
Clamp	4	5	Clamp

FIGURE 1 — BLOCK DIAGRAM AND TYPICAL APPLICATION



TCF6000

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted, Note 1.)

Rating	Symbol	Value	Unit
Supply Voltage	V _{CC}	6.0	V
Supply Current	I _i	300	mA
Clamping Current	I _{IK}	± 50	mA
Junction Temperature	T _J	150	°C
Power Dissipation (T _A = +85°C)	P _D	400	mW
Thermal Resistance (Junction-Ambient)	θ _{JA}	100	°C/W
Operating Ambient Temperature Range	T _A	-40 to +85	°C
Storage Temperature Range	T _{stg}	-55 to +150	°C

Note 1: Values beyond which damage may occur.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, 4.5 ≤ V_{CC} ≤ 5.5 V; if not otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
Positive Clamping Voltage (Note 2) (I _{IK} = 10 mA, -40°C ≤ T _A ≤ +85°C)	V _(IK)	—	V _{CC} + 1.0	V
Positive Peak Clamping Current	I _{IK(P)}	—	20	mA
Negative Peak Clamping Voltage (I _{IK} = -10 mA, -40°C ≤ T _A ≤ +85°C)	V _(IK)	-0.3	—	V
Negative Peak Clamping Current	I _{IK(P)}	-20	—	mA
Output Leakage Current (0 V ≤ V _{in} ≤ V _{CC}) (0 V ≤ V _{in} ≤ V _{CC} , -40°C ≤ T _A ≤ +85°C)	I _L I _{LT}	— —	1.0 5.0	μA
Channel Crosstalk (A _{CT} = 20 log I _L /I _{IK})	A _{CT}	100	—	dB
Quiescent Current (Package)	I _B	—	2.0	mA

Note 2: The device might not give 100% protection in CMOS applications.

CIRCUIT DESCRIPTION

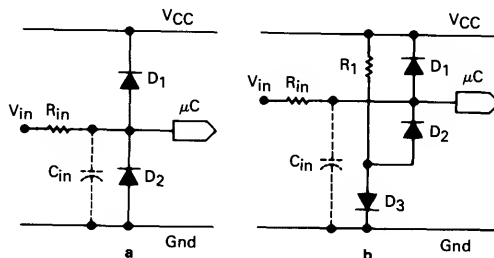
To ensure the reliable operation of any integrated circuit based electronics system, care has to be taken that voltage transients do not reach the device I/O pins. Most NMOS, HMOS and Bipolar integrated circuits are particularly sensitive to negative voltage peaks which can provoke latch-up or otherwise disturb the normal functioning of the circuit, and in extreme cases may destroy the device.

Generally the maximum rating for a negative voltage transients on integral circuits is -0.3 V over the whole temperature range. Classical protection units have consisted of diode/resistor networks as shown in Figures 2a and 2b.

The arrangement in Figure 2a does not, in general, meet the specification and is therefore inadequate.

The problem with the solution shown in Figure 2b lies mainly with the high current drain through the biasing devices R₁ and D₃. A second problem exists if the input line carries an analog signal. When V_{in} is close to the ground potential, currents arising from leakage and mismatch between D₃ and D₂ can be sourced into the input line, thus disturbing the reading.

FIGURE 2 — CLASSICAL PROTECTION CIRCUITS

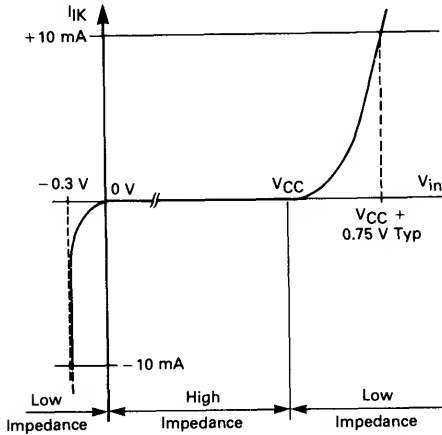


TCF6000

Figure 3 shows the clamping characteristics which are common to each of the six cells in the Peripheral Clamping Array.

As with the classical protection circuits, positive voltage transients are clamped by means of a fast diode to the V_{CC} supply line.

FIGURE 3 — CLAMPING CHARACTERISTICS



APPLICATIONS INFORMATION

Figure 4 depicts a typical application in a microcomputer based automotive ignition system.

The TCF6000 is being used not only to protect the system's normal inputs but also the (bidirectional) serial diagnostics port.

The value of the input resistors, R_{in} , is determined by the clamping current and the anticipated value of the spikes.

Thus:

$$R_{in} = \frac{V}{I_{IK}} \text{ Ohms}$$

where V = Peak volts (Volts)
 I_{IK} = Clamping current (Amps)

So, taking

$$V = 300 \text{ V typically (SAE J1211)}$$

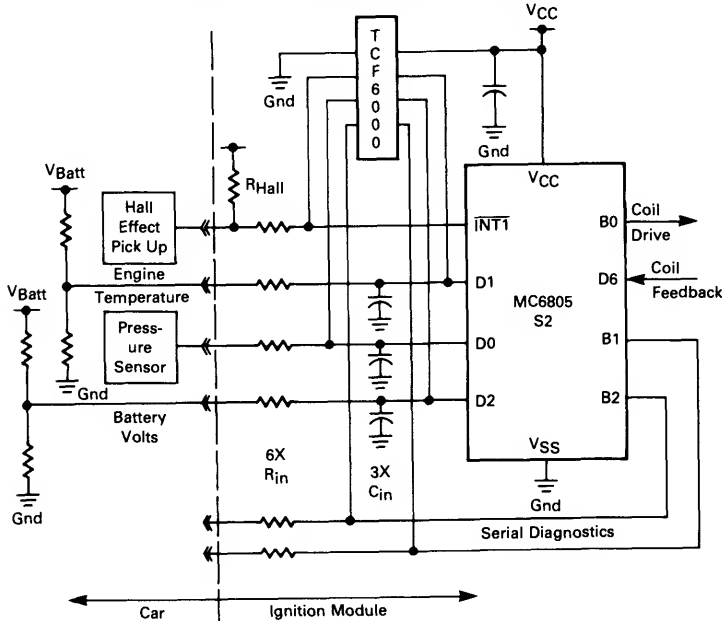
$$I_{IK} = 10 \text{ mA (recommended)}$$

gives

$$R_{in} = 30 \text{ k}$$

Resistors of this value will not usually cause any problems in MOS systems, but their presence needs to be taken into account by the designer. Their effect will normally need to be compensated for in Bipolar systems.

FIGURE 4 — TYPICAL AUTOMOTIVE APPLICATION



The use of C_{in} is not mandatory, and is not recommended where the lines to be protected are used for output or for both input and output. For digital input lines, the use of a small capacitor in the range of 50 to 220 pF is recommended as this will reduce the rate of rise of voltage seen by the TCF6000 and hence the possibility of overshoot.

In the case of the analog inputs, such as that from the pressure sensor, the capacitor C_{in} is necessary for devices, such as the MC6805S2 shown, which present a low impedance during the sampling period. The maximum value for C_{in} is determined by the accuracy required, the time taken to sample the input and the input impedance during that time, while the maximum value is determined by the required frequency response and the value of R_{in} .

Thus for a resistive input A/D converter where:

- T_S = Sample time (Seconds)
- R_D = Device input resistance (Ohms)
- V_{in} = Input voltage (Volts)
- k = Required accuracy (%)
- Q_1 = Charge on capacitor before sampling
- Q_2 = Charge on capacitor after sampling
- I_D = Device input current (Amps)

Thus:

$$Q_1 - Q_2 = \frac{k \cdot Q_1}{100}$$

but $Q_1 = C_{in} V_{in}$

and $Q_1 - Q_2 = I_D \cdot T_S$

so that $I_D T_S = \frac{k \cdot C_{in} \cdot V_{in}}{100}$

and $C_{in} (\text{min}) = \frac{I_D \cdot T_S}{V_{in} \cdot k} \text{ Farad}$

so $C_{in} (\text{min}) = \frac{100 \cdot T_S}{k \cdot R_D} \text{ Farad}$

The calculation for a sample and hold type converter is even simpler:

k = Required accuracy (%)

C_H = Hold capacitor (Farad)

$$C_{in} (\text{min}) = \frac{100 \cdot C_H}{k} \text{ Farad}$$

For the MC6805S2 this comes out at:

$$C_{in} (\text{min}) = \frac{100 \cdot 25 \text{ pF}}{0.25} = 10 \text{ nF for } 1/4\% \text{ accuracy}$$

AUTOMOTIVE DIRECTION INDICATOR

... designed for use in conjunction with a relay in automotive applications. It is also applicable for other warning lamps such as "handbrake ON," etc.

- Defective Lamp Detection
- Overvoltage Protection
- Short Circuit Detection and Relay Shutdown to Prevent Risk of Fire
- Reverse Battery Connection Protection
- Integrated Suppression Clamp Diode

UAA1041

AUTOMOTIVE DIRECTION INDICATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

PIN CONNECTIONS

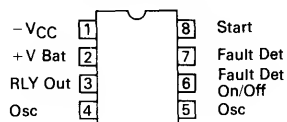
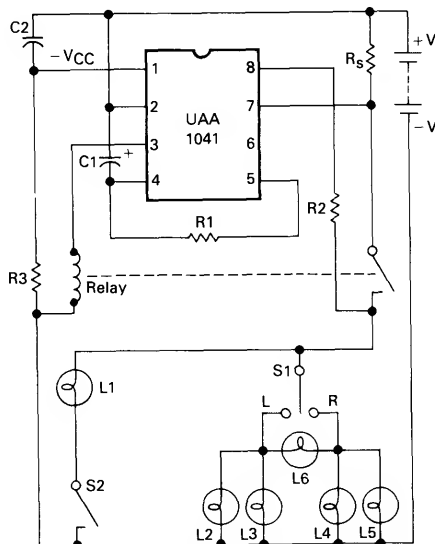
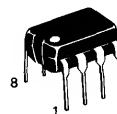


FIGURE 1 — TYPICAL AUTOMOTIVE SYSTEM



L1: 1.2 W warning light handbrake ON L2, L3, L4, L5: 21 W, turn signals

R1 = 75 k Rs = 30 mΩ
R2 = 3.3 k C1 = 5.6 μF
R3 = 220 Ω C2 = 0.047 μF



P SUFFIX
 PLASTIC PACKAGE
 CASE 626



D SUFFIX
 PLASTIC PACKAGE
 CASE 751
 (SO-8)

ORDERING INFORMATION

Device	Ambient Temperature Range	Package
UAA1041D	-40°C to +100°C	SO-8
UAA1041P		Plastic DIP

MAXIMUM RATINGS

Rating	Pin	Value	Unit
Current: Continuous/Pulse*	1	+150/+500 -35/-500	mA
	2	+/-350/1900	
	3	+/-300/1400	
	8	+/-25/50	
Junction Temperature	T _J	150	°C
Operating Ambient Temperature Range	T _A	-40 to +100	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

*One pulse with an exponential decay and with a time constant of 500 ms.

ELECTRICAL CHARACTERISTICS (T₁ = 25°C)

Characteristics	Symbol	Min	Typ	Max	Unit
Battery Voltage Range (normal operation)	V _B	8.0	—	18	V
Overvoltage Detector Threshold (V _{Pin2} - V _{Pin1})	D _{th(OV)}	19	20.2	21.5	V
Clamping Voltage (V _{Pin2} - V _{Pin1})	V _{IK}	29	31.5	34	V
Short Circuit Detector Threshold (V _{Pin2} - V _{Pin7})	D _{th(SC)}	0.63	0.7	0.77	V
Output Voltage (I _{relay} = -250 mA) (V _{Pin2} - V _{Pin3})	V _O	—	—	1.5	V
Starter Resistance R _{st} = R ₂ + R _{Lamp}	R _{st}	—	—	3.6	kΩ†
Oscillator Constant (normal operation)	K _n	1.4	1.5	1.6	—
Temperature Coefficient of K _n	k _n	—	-1.5x10 ⁻³	—	1/°C
Duty Cycle (normal operation)	—	45	50	55	%
Oscillator Constant — (1 lamp defect of 21 W)	K _F	0.63	0.68	0.73	—
Duty Cycle (1 lamp defect of 21 W)	—	35	40	45	%
Oscillator Constant	K ₁	0.167	0.18	0.193	—
	K ₂	0.25	0.27	0.29	
	K ₃	0.126	0.13	0.14	
Current Consumption (relay off) Pin 1; at V _{Pin2} - V _{Pin1} = 8.0 V = 13.5 V = 18 V	I _{CC}	—	-0.9	—	mA
		-2.5	-1.6	-1.0	
		—	-2.2	—	
Current Consumption (relay on) Pin 1; at V _{Pin2} - V _{Pin1} = 8.0 V = 13.5 V = 18 V	—	—	-3.8	—	mA
		—	-5.6	—	
		—	-6.9	—	
Defect Lamp Detector Threshold at V _{Pin2} to - V _B = 8.0 V and R ₃ = 220 Ω = 13.5 V = 18 V	V _{Pin2} - V _{Pin7}	—	67	—	mV
	V _{Pin2} - V _{Pin7}	79	85.3	91	
	V _{Pin2} - V _{Pin7}	—	100	—	

†See Note 1 of Application Information

CIRCUIT DESCRIPTION

The circuit is designed to drive the direction indicator flasher relay. Figure 2 shows the typical system configuration with the external components. It consists of a network (R_1 , C_1) to determine the oscillator frequency, shunt resistor (R_S) to detect defective bulbs and short circuits in the system, and two current limiting resistors (R_2 / R_3) to protect the IC against load dump transients. The circuit can be used either with or without short-circuit detection.

The lightbulbs L2, L3, L4, L5 are the turn signal indicators with the dashboard-light L6. When switch S1 is closed, after a time delay of t_1 (in our example $t_1 = 75$ ms), the relay will be actuated. The corresponding lightbulbs L2, L3 (or L4, L5) will flash at the oscillator frequency, independent of the battery voltage of 8.0 V to 18 V. The flashing cycle stops and the circuit is reset to the initial position when the switch S1 is open.

The circuit features overvoltage, defective lamp and short circuit detection.

Overvoltage detection:

Senses the battery voltage. When this voltage exceeds 20.2 V (this is the case when two batteries are connected in series), the relay will be turned off to protect the lightbulbs.

Lightbulb defect detector:

Senses the current through the shunt resistor R_S . When one of the lightbulbs is defective, the failure is indicated by doubling the flashing frequency.

Short circuit detector:

Detects excessive current ($I_{sh} > 25$ A) flowing in the shunt resistor R_S . The detection takes place after a time delay of t_3 ($t_3 = 55$ ms). In this case, the relay will be turned off. The circuit is reset by switching S1 to the off position.

Operation with short circuit detection:

Pin 6 has to be left open and a capacitor C_2 has to be connected between Pin 1 and Pin 2.

Operation without short circuit detection:

Pin 6 has to be connected to Pin 2 and the use of capacitor C_2 is not necessary.

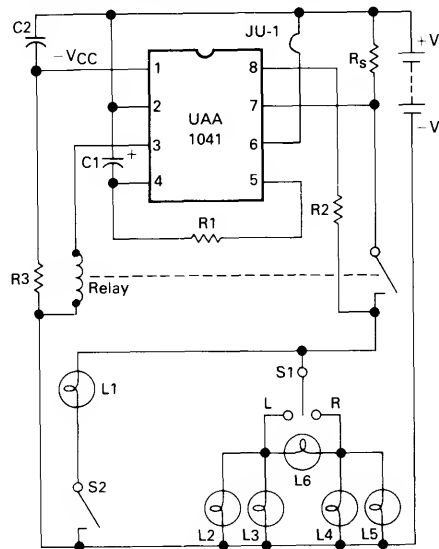
The circuit can also be used for other warning flashers. In our example, handbrake engaged is signaled by the light L1.

APPLICATION INFORMATION

- The flashing cycle is started by closing S1. The switch position is sensed across resistor R_2 and R_{Lamp} by input 8.
 $R_{st} = R_2 + R_{Lamp}$
 The condition for the start is: $R_{st} < 3.6$ k Ω
 For correct operation leakage resistance from Pin 8 to ground must be greater than 5.6 k Ω .

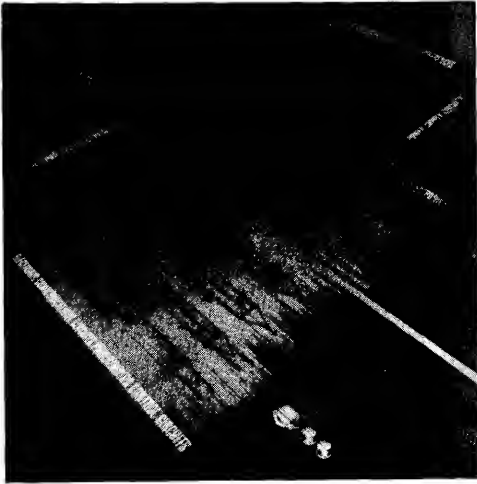
- Flashing frequency: $f_n = \frac{1}{R_1 C_1 K_n}$
- Flashing frequency in the case of one defective lightbulb of 21 W
 $f_F = \frac{1}{R_1 C_1 K_F} K_n = 2.2 K_F$
- t_1 : delay at the moment when S1 is closed and first flash $t_1 = K_1 R_1 C$
- t_2 : defective lightbulb detection delay $t_2 = K_2 R_1 C_1$
- t_3 : short circuit detection delay $t_3 = K_1 R_1 C_1$
 In the case of short circuit:
 — it is assumed that the voltage $V_{Pin2} - V_{Pin1} \geq 8.0$ V.
 — The relay will be turned off after delay t_3 .
 — The circuit is reset by switching S1 to the off position.
- The capacitor C_2 is not obligatory when the short circuit detector is not used. In this case Pin 6 has to be connected to Pin 2.
- When overvoltage is sensed ($V_{Pin2} - V_{Pin1}$) the relay is turned off to protect the relay and the lightbulbs against excessive currents.

FIGURE 2 — TYPICAL SYSTEM CONFIGURATION



PARTS LIST

$R_1 = 75$ k Ω	Relay — Coil Resistance
$R_2 = 3.3$ k Ω	Range 60 to 800 Ω
$R_3 = 220$ Ω	
$R_4 = 30$ m Ω	Note: Per text connect
Wire Resistor	jumper JU-1 to bypass
$C_1 = 5.6$ μ F	short circuit detector.
$C_2 = 0.047$ μ F	C_2 may be deleted also.



In Brief . . .

A variety of other analog circuits are provided for special applications with both bipolar and CMOS technologies. These circuits range from the industry-standard analog timing circuits and multipliers to specialized CMOS smoke detectors and encoder/decoder functions. Other circuits include a transmitter-receiver pair and a single chip receiver/transmitter. These products provide key functions in a wide range of applications, including data transmission, commercial smoke detectors, and various industrial controls.

Other Linear Circuits

Selector Guide

Timing Circuits	11-2
Multipliers	11-2
Alphanumeric Listing	11-3
Related Application Notes	11-3
Data Sheets	11-4

Other Linear Circuits

Timing Circuits

These highly stable timers are capable of producing accurate time delays or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and the

Singles

MC1455G,P1,U $T_A = 0^\circ \text{ to } +70^\circ\text{C}$, Case 601, 626, 693

MC1455BP1 $T_A = -40^\circ \text{ to } +85^\circ\text{C}$, Case 626

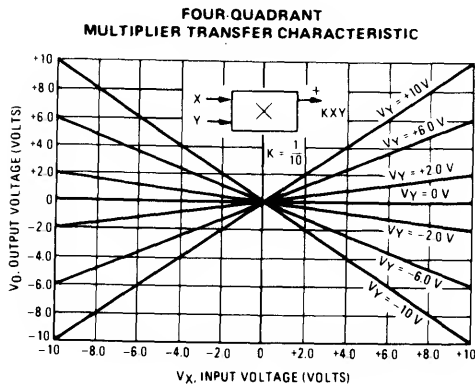
Dual

MC3456L,P $T_A = 0^\circ \text{ to } +70^\circ\text{C}$, Case 632, 646

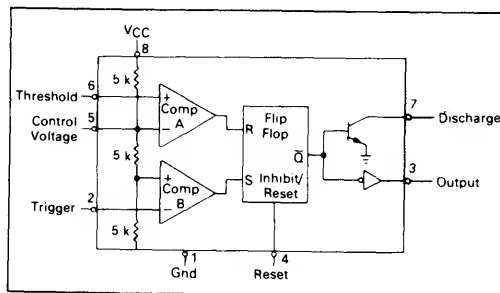
Multipliers

Linear Four-Quadrant Multipliers

Multipliers are designed for use where the output voltage is a linear product of two input voltages. Typical applications include: multiply, divide, square, root-mean-square, phase detector, frequency doubler, balanced modulator/demodulator, electronic gain control.



duty cycle are both accurately controlled with two external resistors and one capacitor. The output structure can source or sink up to 200 mA or drive TTL circuits. Timing intervals from microseconds through hours can be obtained.



MC1594L $T_A = -55^\circ \text{ to } +125^\circ\text{C}$, Case 620

MC1494L $T_A = 0^\circ \text{ to } +70^\circ\text{C}$, Case 620

The MC1594/MC1494 is a Variable Transconductance Multiplier with internal level-shift circuitry and voltage regulator. Scale factor, input offsets and output offset are completely adjustable with the use of four external potentiometers. Two complementary regulated voltages are provided to simplify offset adjustment and improve power-supply rejection.

MC1595L $T_A = -55^\circ \text{ to } +125^\circ\text{C}$, Case 632

MC1495L $T_A = 0^\circ \text{ to } +70^\circ\text{C}$, Case 632

... designed for uses where the output is a linear product of two input voltages. Maximum versatility is assured by allowing the user to select the level shift method. Typical applications include: multiply, divide*, square root*, mean square*, phase detector, frequency doubler, balanced modulator/demodulator, electronic gain control.

*When used with an operational amplifier.

OTHER LINEAR CIRCUITS

TIMING CIRCUITS

Device	Function	Page
MC1455	Timing Circuit	11-4
MC3456	Dual Timing Circuit	11-40
MC3556	Dual Timing Circuit	11-40

MULTIPLIERS

Device	Function	Page
MC1494L	Four-Quadrant Multiplier	11-11
MC1495L	Four-Quadrant Multiplier	11-25
MC1496	Balanced Modulator-Demodulator	See Chapter 8
MC1594L	Four-Quadrant Multiplier	11-11
MC1595L	Four-Quadrant Multiplier	11-25
MC1596	Balanced Modulator-Demodulator	See Chapter 8

RELATED APPLICATION NOTES

Application Note	Title	Related Device
AN489	Analysis and Basic Operation of the MC1595	MC1595L
AN531	MC1596 Balanced Modulator	MC1596

MC1455

TIMING CIRCUIT

The MC1455 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200 mA or drive MTTL circuits.

- Direct Replacement for NE555 Timers
- Timing From Microseconds Through Hours
- Operates in Both Astable and Monostable Modes
- Adjustable Duty Cycle
- High Current Output Can Source or Sink 200 mA
- Output Can Drive MTTL
- Temperature Stability of 0.005% per °C
- Normally "On" or Normally "Off" Output

FIGURE 1 — 22-SECOND SOLID-STATE TIME DELAY RELAY CIRCUIT

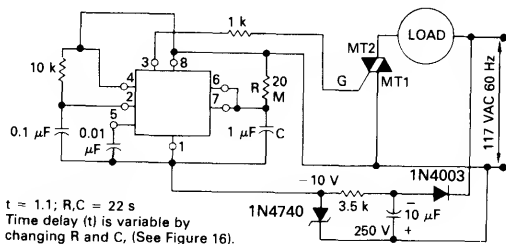
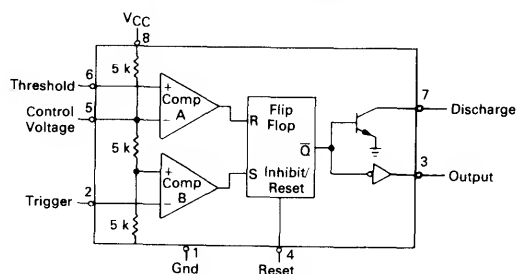


FIGURE 2 — BLOCK DIAGRAM



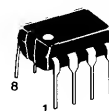
TIMING CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT



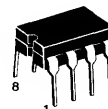
G SUFFIX
 METAL PACKAGE
 CASE 601

- | | |
|------------|--------------------|
| 1. Ground | 5. Control Voltage |
| 2. Trigger | 6. Threshold |
| 3. Output | 7. Discharge |
| 4. Reset | 8. VCC |



P1 SUFFIX
 PLASTIC PACKAGE
 CASE 626

U SUFFIX
 CERAMIC PACKAGE
 CASE 693



D SUFFIX
 PLASTIC PACKAGE
 CASE 751
 (SO-8)



ORDERING INFORMATION

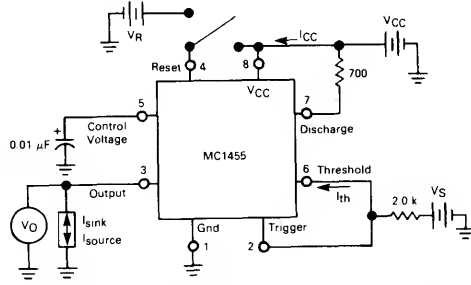
Device	Alternate	Temperature Range	Package
MC1455G	—	0°C to +70°C	Metal Can Plastic DIP SO-8 Ceramic DIP
MC1455P1	NE555V		
MC1455D	—		
MC1455U	—		
MC1455BP1	—	-40°C to +85°C	Plastic DIP

MC1455

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V _{CC}	+18	Vdc
Discharge Current (Pin 7)	I ₇	200	mA
Power Dissipation (Package Limitation)	P _D		
Metal Can		680	mW
Derate above T _A = +25°C		4.6	mW/°C
Plastic Dual In-Line Package		625	mW
Derate above T _A = +25°C		5.0	mW/°C
Operating Temperature Range (Ambient)	T _A		°C
MC1455B		-40 to +85	
MC1455		0 to +70	
Storage Temperature Range	T _{stg}	-65 to +150	°C

FIGURE 3 — GENERAL TEST CIRCUIT



Test Circuit for Measuring dc Parameters (to set output and measure parameters)

- a) When V_S < 2.3 V_{CC}, V_O is low
b) When V_S = 1.3 V_{CC}, V_O is high
c) When V_O is low, pin 7 sinks current. To test for Reset, set V_O high, apply Reset voltage, and test for current flowing into pin 7. When Reset is not in use, it should be tied to V_{CC}.

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = +5.0 V to +15 V unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Operating Supply Voltage Range	V _{CC}	4.5	—	16	V
Supply Current V _{CC} = 5.0 V, R _L = ∞ V _{CC} = 15 V, R _L = ∞ Low State, (Note 1)	I _{CC}	—	3.0 10	6.0 15	mA
Timing Error (Note 2) R = 1.0 kΩ to 100 kΩ Initial Accuracy C = 0.1 μF Drift with Temperature Drift with Supply Voltage		—	1.0 50 0.1	—	% PPM/°C %/Volt
Threshold Voltage	V _{th}	—	2/3	—	xV _{CC}
Trigger Voltage V _{CC} = 15 V V _{CC} = 5.0 V	V _T	—	5.0 1.67	—	V
Trigger Current	I _T	—	0.5	—	μA
Reset Voltage	V _R	0.4	0.7	1.0	V
Reset Current	I _R	—	0.1	—	mA
Threshold Current (Note 3)	I _{th}	—	0.1	0.25	μA
Discharge Leakage Current (Pin 7)	I _{dis}	—	—	100	nA
Control Voltage Level V _{CC} = 15 V V _{CC} = 5.0 V	V _{CL}	9.0 2.6	10 3.33	11 4.0	V
Output Voltage Low (V _{CC} = 15 V) I _{sink} = 10 mA I _{sink} = 50 mA I _{sink} = 100 mA I _{sink} = 200 mA (V _{CC} = 5.0 V) I _{sink} = 8.0 mA I _{sink} = 5.0 mA	V _{OL}	—	0.1 0.4 2.0 2.5	0.25 0.75 2.5 —	V
Output Voltage High (I _{source} = 200 mA) V _{CC} = 15 V (I _{source} = 100 mA) V _{CC} = 15 V V _{CC} = 5.0 V	V _{OH}	—	12.5 12.75 2.75	— 13.3 3.3	V
Rise Time of Output	t _{OLH}	—	100	—	ns
Fall Time of Output	t _{OHL}	—	100	—	ns

NOTES:

- Supply current when output is high is typically 1.0 mA less.
- Tested at V_{CC} = 5.0 V and V_{CC} = 15 V.
Monostable mode
- This will determine the maximum value of R_A + R_B for 15 V operation.
The maximum total R = 20 megohms.

MC1455

TYPICAL CHARACTERISTICS

($T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 4 — TRIGGER PULSE WIDTH

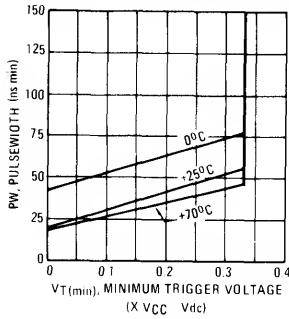


FIGURE 5 — SUPPLY CURRENT

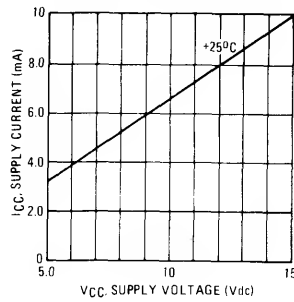


FIGURE 6 — HIGH OUTPUT VOLTAGE

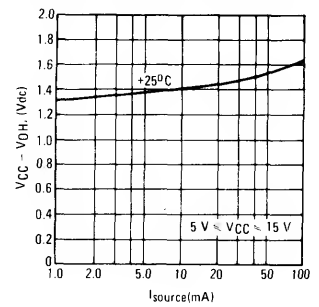


FIGURE 7 — LOW OUTPUT VOLTAGE
@ $V_{CC} = 5.0\text{ Vdc}$

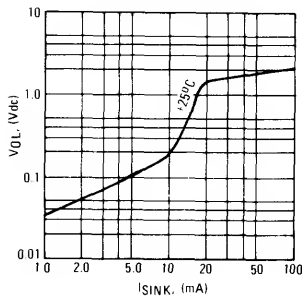


FIGURE 8 — LOW OUTPUT VOLTAGE
@ $V_{CC} = 10\text{ Vdc}$

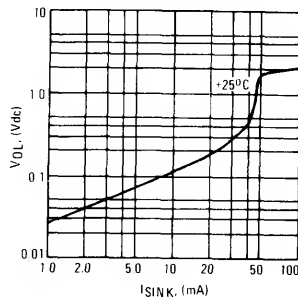


FIGURE 9 — LOW OUTPUT
VOLTAGE @ $V_{CC} = 15\text{ Vdc}$

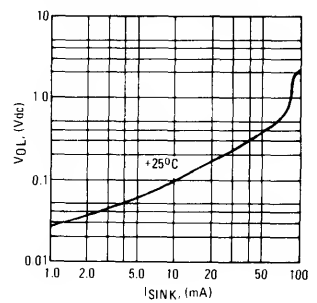


FIGURE 10 — DELAY TIME
versus SUPPLY VOLTAGE

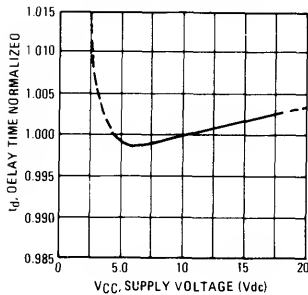


FIGURE 11 — DELAY TIME
versus TEMPERATURE

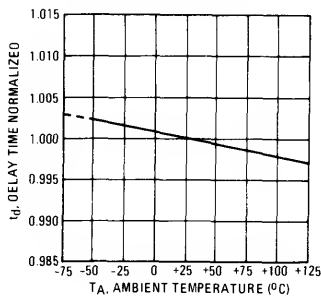
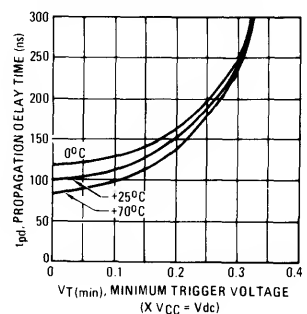
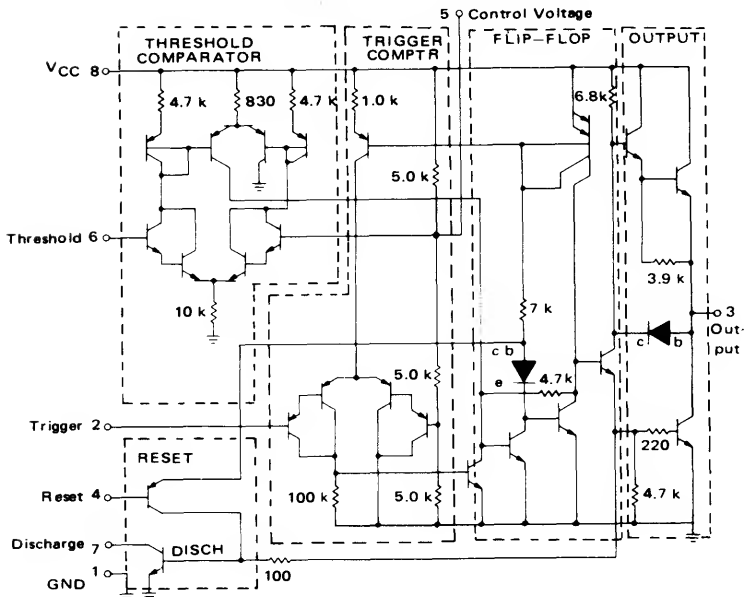


FIGURE 12 — PROPAGATION DELAY
versus TRIGGER VOLTAGE



MC1455

FIGURE 13 — REPRESENTATIVE CIRCUIT SCHEMATIC



GENERAL OPERATION

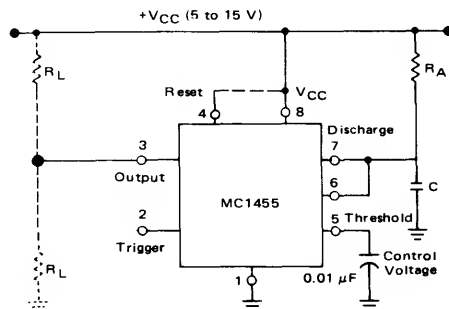
The MC1455 is a monolithic timing circuit which uses as its timing elements an external resistor — capacitor network. It can be used in both the monostable (one-shot) and astable modes with frequency and duty cycle controlled by the capacitor and resistor values. While the timing is dependent upon the external passive components, the monolithic circuit provides the starting circuit, voltage comparison and other functions needed for a complete timing circuit. Internal to the integrated circuit are two comparators, one for the input signal and the other for capacitor voltage; also a flip-flop and digital output are included. The comparator reference voltages are always a fixed ratio of the supply voltage thus providing output timing independent of supply voltage.

Monostable Mode

In the monostable mode, a capacitor and a single resistor are used for the timing network. Both the threshold terminal and the discharge transistor terminal are connected together in this mode, refer to circuit Figure 14. When the input voltage to the trigger comparator falls below $1/3 V_{CC}$ the comparator output triggers the flip-flop so that its output sets low. This turns the capacitor discharge transistor "off" and drives the digital output to the high state. This condition allows the capacitor to charge at an exponential rate which is set by the RC time constant. When the capacitor voltage reaches $2/3 V_{CC}$ the threshold comparator resets the flip-flop. This action discharges the timing capacitor and returns the digital output to the low state. Once the flip-flop has been triggered by an input signal, it cannot be retrigged until the present timing period has been completed. The time that the output is high is given by the equation $t = 1.1 R_A C$. Various combinations of R and C and their associated times are shown in Figure 16. The trigger pulse width must be less than the timing period.

A reset pin is provided to discharge the capacitor thus interrupting the timing cycle. As long as the reset pin is low, the capacitor discharge transistor is turned "on" and prevents the capacitor from charging. While the reset voltage is applied the digital output will remain the same. The reset pin should be tied to the supply voltage when not in use.

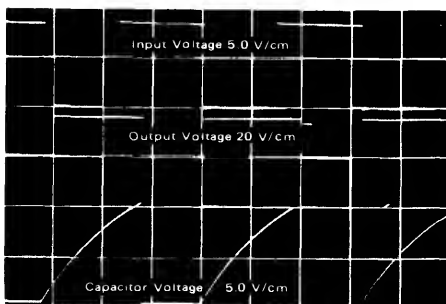
FIGURE 14 — MONOSTABLE CIRCUIT



MC1455

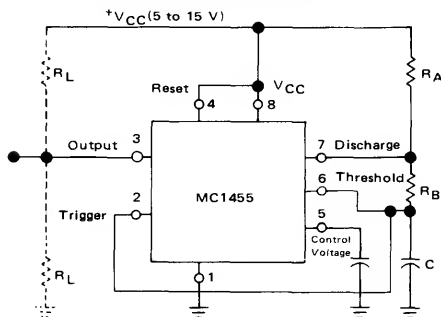
GENERAL OPERATION (continued)

FIGURE 15 — MONOSTABLE WAVEFORMS



($R_A = 10 \text{ k}\Omega$, $C = 0.01 \text{ }\mu\text{F}$, $R_L = 1.0 \text{ k}\Omega$, $V_{CC} = 15 \text{ V}$)

FIGURE 17 — ASTABLE CIRCUIT



Astable Mode

In the astable mode the timer is connected so that it will retrigger itself and cause the capacitor voltage to oscillate between $1/3 V_{CC}$ and $2/3 V_{CC}$. See Figure 17.

The external capacitor charges to $2/3 V_{CC}$ through R_A and R_B and discharges to $1/3 V_{CC}$ through R_B . By varying the ratio of these resistors the duty cycle can be varied. The charge and discharge times are independent of the supply voltage.

The charge time (output high) is given by: $t_1 = 0.695 (R_A + R_B) C$

The discharge time (output low) by: $t_2 = 0.695 (R_B) C$

Thus the total period is given by: $T = t_1 + t_2 = 0.695 (R_A + 2R_B) C$

The frequency of oscillation is then: $f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B) C}$

and may be easily found as shown in Figure 19.

The duty cycle is given by: $DC = \frac{R_B}{R_A + 2R_B}$

To obtain the maximum duty cycle R_A must be as small as possible; but it must also be large enough to limit the discharge current (pin 7 current) within the maximum rating of the discharge transistor (200 mA).

The minimum value of R_A is given by:

$$R_A \geq \frac{V_{CC} (V_{dc})}{I_7 (A)} \geq \frac{V_{CC} (V_{dc})}{0.2}$$

FIGURE 16 — TIME DELAY

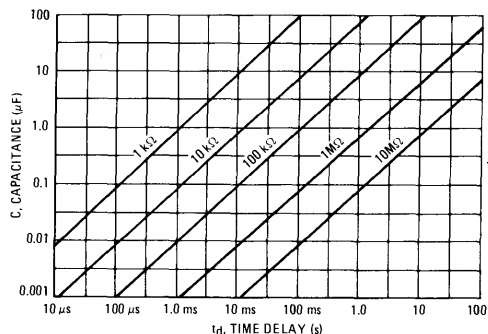
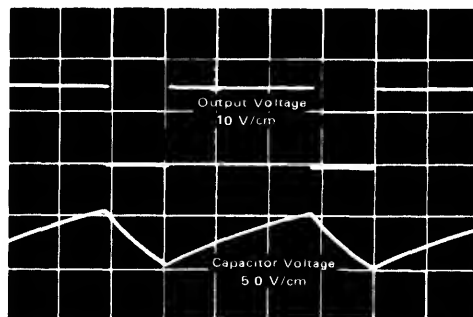
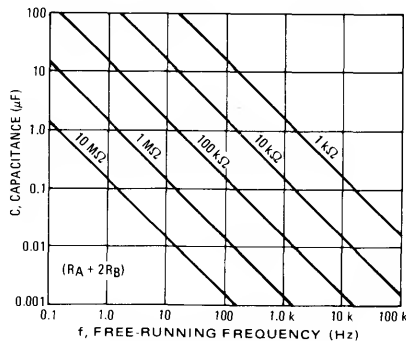


FIGURE 18 — ASTABLE WAVEFORMS



($R_A = 5.1 \text{ k}\Omega$, $C = 0.01 \text{ }\mu\text{F}$, $R_L = 1.0 \text{ k}\Omega$;
 $R_B = 3.9 \text{ k}\Omega$, $V_{CC} = 15 \text{ V}$)

FIGURE 19 — FREE-RUNNING FREQUENCY



MC1455

APPLICATIONS INFORMATION

Linear Voltage Ramp

In the monostable mode, the resistor can be replaced by a constant current source to provide a linear ramp voltage. The capacitor still charges from 0 to $2/3 V_{CC}$. The linear ramp time is given by

$$t = \frac{2}{3} \frac{V_{CC}}{I}$$

where $I = \frac{V_{CC} - V_B - V_{BE}}{R_E}$. If V_B is much larger than V_{BE} , then t can be made independent of V_{CC} .

FIGURE 20 — LINEAR VOLTAGE SWEEP CIRCUIT

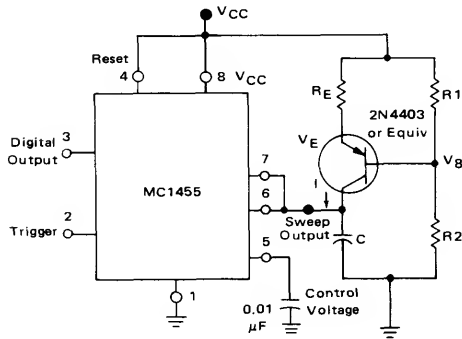
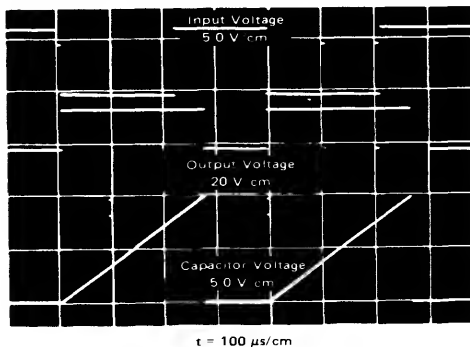


FIGURE 21 — LINEAR VOLTAGE RAMP WAVEFORMS
($R_E = 10 \text{ k}\Omega$, $R_2 = 100 \text{ k}\Omega$, $R_1 = 39 \text{ k}\Omega$, $C = 0.01 \text{ }\mu\text{F}$, $V_{CC} = 15 \text{ V}$)



Missing Pulse Detector

The timer can be used to produce an output when an input pulse fails to occur within the delay of the timer. To accomplish this, set the time delay to be slightly longer than the time between successive input pulses. The timing cycle is then continuously reset by the input pulse train until a change in frequency or a missing pulse allows completion of the timing cycle, causing a change in the output level.

FIGURE 22

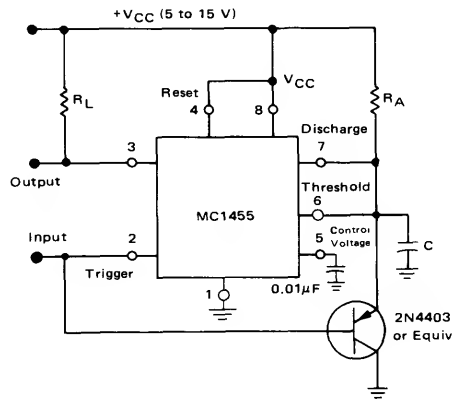
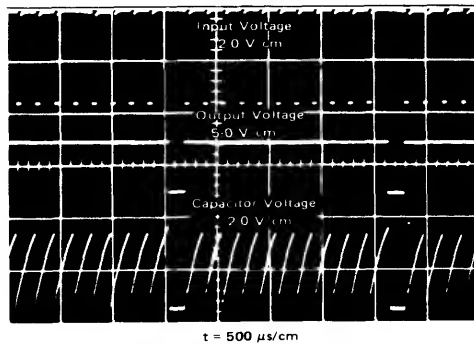


FIGURE 23 — MISSING PULSE DETECTOR WAVEFORMS
($R_A = 2.0 \text{ k}\Omega$, $R_L = 1.0 \text{ k}\Omega$, $C = 0.1 \text{ }\mu\text{F}$, $V_{CC} = 15 \text{ V}$)

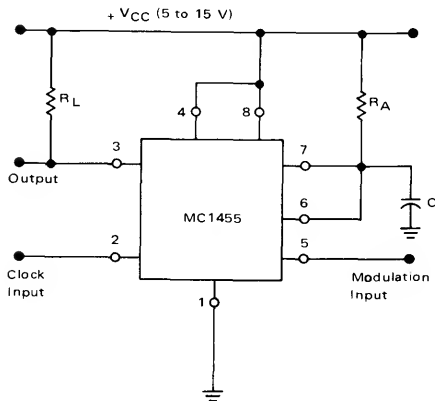
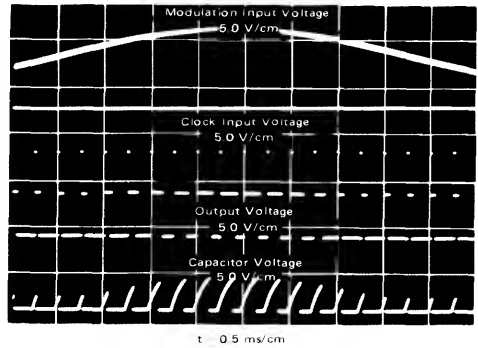


APPLICATIONS INFORMATION (continued)

Pulse Width Modulation

If the timer is triggered with a continuous pulse train in the monostable mode of operation, the charge time of the capacitor can be varied by changing the control voltage at pin 5. In this manner, the output pulse width can be modulated by applying a modulating signal that controls the threshold voltage.

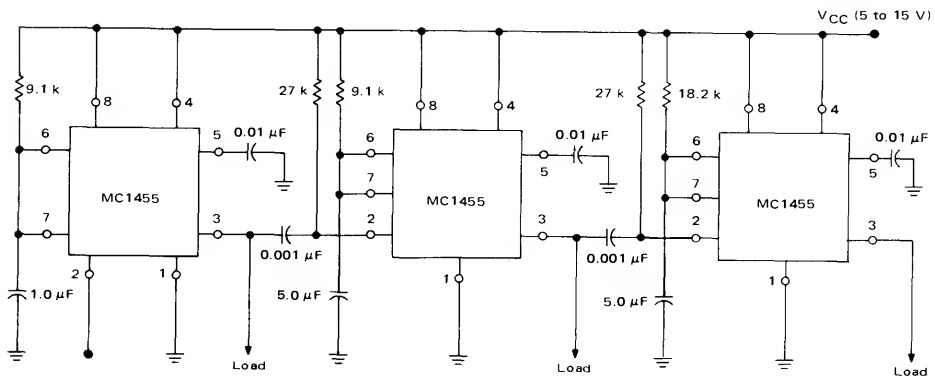
FIGURE 24

FIGURE 25 — PULSE WIDTH MODULATION WAVEFORMS
($R_A = 10\text{ k}\Omega$, $C = 0.02\text{ }\mu\text{F}$, $V_{CC} = 15\text{ V}$)

Test Sequences

Several timers can be connected to drive each other for sequential timing. An example is shown in Figure 26 where the sequence is started by triggering the first timer which runs for 10 ms. The output then switches low momentarily and starts the second timer which runs for 50 ms and so forth.

FIGURE 26



MC1494L
MC1594L

MONOLITHIC FOUR-QUADRANT MULTIPLIER

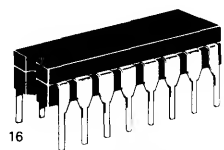
... designed for use where the output voltage is a linear product of two input voltages. Typical applications include: multiply, divide, square root, mean square, phase detector, frequency doubler, balanced modulator/demodulator, electronic gain control.

The MC1594/1494 is a variable transconductance multiplier with internal level-shift circuitry and voltage regulator. Scale factor, input offsets and output offset are completely adjustable with the use of four external potentiometers. Two complementary regulated voltages are provided to simplify offset adjustment and improve power-supply rejection.

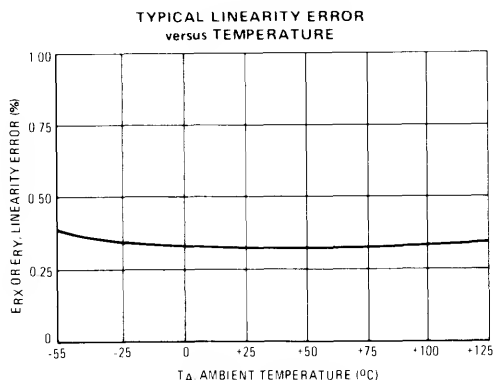
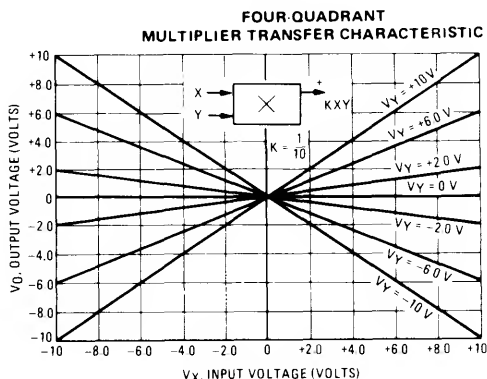
- Operates With ± 15 V Supplies
- Excellent Linearity — Maximum Error (X or Y): $\pm 0.5\%$ (MC1594)
 $\pm 1.0\%$ (MC1494)
- Wide Input Voltage Range — ± 10 volts
- Adjustable Scale Factor, K (0.1 nominal)
- Single-Ended Output Referenced to Ground
- Simplified Offset Adjust Circuitry
- Frequency Response (3 dB Small-Signal) — 1.0 MHz
- Power Supply Sensitivity — 30 mV/V typical

**LINEAR FOUR-QUADRANT
MULTIPLIER INTEGRATED
CIRCUIT**

**SILICON MONOLITHIC
EPITAXIAL PASSIVATED**



L SUFFIX
CERAMIC PACKAGE
CASE 620



MC1494L, MC1594L

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V ⁺ V ⁻	+18 -18	Vdc
Differential Input Signal	V _g -V ₆ V ₁₀ -V ₁₃	± 6+I ₁ R _Y <30 ± 6+I ₁ R _X <30	Vdc
Common-Mode Input Voltage V _{CMY} = V _g = V ₆ V _{CMX} = V ₁₀ = V ₁₃	V _{CMY} V _{CMX}	±11.5 ±11.5	Vdc
Power Dissipation (Package Limitation) T _A = +25°C Derate above T _A = +25°C	P _D 1/θ _{JA}	750 5.0	mW mW/°C
Operating Temperature Range MC1594 MC1494	T _A	-55 to +125 0 to +70	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V⁺ = +15 V, V⁻ = -15 V, T_A = +25°C, R₁ = 16 kΩ, R_X = 30 kΩ, R_Y = 62 kΩ, R_L = 47 kΩ, unless otherwise noted)

Characteristic	Fig.	Symbol	MC1594			MC1494			Unit
			Min	Typ	Max	Min	Typ	Max	
Linearity Output error in Percent of full scale -10 V < V _X < +10 V (V _Y = ±10 V) -10 V < V _Y < +10 V (V _X = ±10 V) T _A = +25°C T _A = T _{high} ① T _A = T _{low}	1	ER _X or ER _Y	—	±0.3	±0.5	—	±0.5	±1.0	%
Input Voltage Range (V _X = V _Y = V _{in}) Resistance (X or Y Input) Offset Voltage (X Input) (Note 1) Offset Voltage (Y Input) (Note 1) Bias Current (X or Y Input) Offset Current (X or Y Input)	2,3,4	V _{in} R _{in} V _{ioX} V _{ioY} I _b I _o	±10 — — — — —	— 300 0.1 0.4 0.5 28	— — 1.6 1.6 1.5 150	±10 — — — — —	— 300 0.2 0.8 1.0 50	— — 2.5 2.5 2.5 400	V _{pk} MΩ V μA nA
Output Voltage Swing Capability Impedance Offset Voltage (Note 1) Offset Current (Note 1)	3,4	V _o R _o V _{oo} I _{oo}	±10 — — —	— 850 0.8 17	— — 1.6 34	±10 — — —	— 850 1.2 25	— — 2.5 52	V _{pk} kΩ V μA
Temperature Stability (Drift) T _A = T _{high} to T _{low} Output Offset (X = 0, Y = 0) Voltage Current X Input Offset (Y = 0) Y Input Offset (X = 0) Scale Factor Total dc Accuracy Drift (X = 10, Y = 10)		TCV _{oo} TCI _{oo} TCV _{ioX} TCV _{ioY} TCK TCE	— — — — — —	1.3 27 0.3 1.5 0.07 0.09	— — — — — —	— — — — — —	1.3 27 0.3 1.5 0.07 0.09	— — — — — —	mV/°C nA/°C mV/°C — — %/°C
Dynamic Response Small Signal (3.0 dB) X Y Power Bandwidth (47 k) 3° Relative Phase Shift 1% Absolute Error	5	BW _{3 dB} (X) BW _{3 dB} (Y) PBW f _φ f _θ	— — — — —	0.8 1.0 440 240 30	— — — — —	— — — — —	0.8 1.0 440 240 30	— — — — —	MHz kHz
Common Mode Input Swing (X or Y) Gain (X or Y)	6	CMV ACM	±10.5 —	— -65	— —	±10.5 —	— -65	— —	V _{pk} dB
Power Supply Current Quiescent Power Dissipation Sensitivity	7	I _d + I _d - P _d S ⁺ S ⁻	— — — — —	6.0 6.5 185 13 30	9.0 9.0 260 50 100	— — — — —	6.0 6.5 185 13 30	12 12 350 100 200	mAdc mW mV/V
Regulated Offset Adjust Voltages Positive Negative Temperature Coefficient (V _R + or V _R -) Power Supply Sensitivity (V _R + or V _R -)	7	V _R + V _R - TCV _R S _R +, S _R -	+3.5 -3.5 — —	+4.3 -4.3 0.03 0.6	+5.0 -5.0 — —	+3.5 -3.5 — —	+4.3 -4.3 0.03 0.6	+5.0 -5.0 — —	Vdc mV/°C mV/V

Note 1: Offsets can be adjusted to zero with external potentiometers.

T_{high} = +125°C for MC1594
+70°C for MC1494

T_{low} = -55°C for MC1594
0°C for MC1494

MC1494L, MC1594L

TEST CIRCUITS

FIGURE 1 - LINEARITY

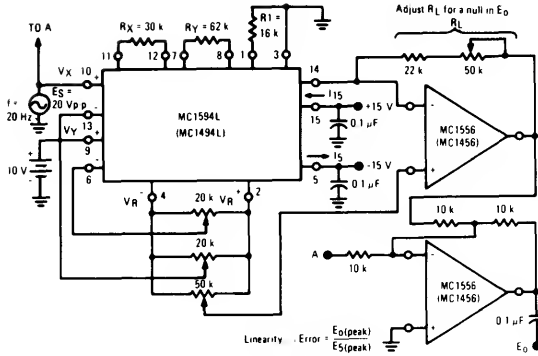


FIGURE 2 - INPUT RESISTANCE

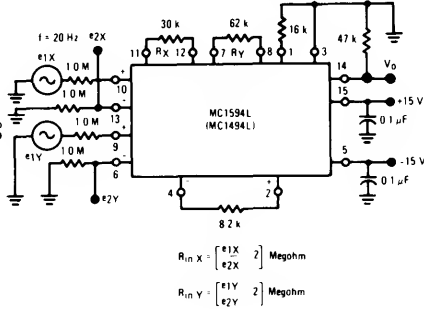


FIGURE 3 - OFFSET VOLTAGES, GAIN

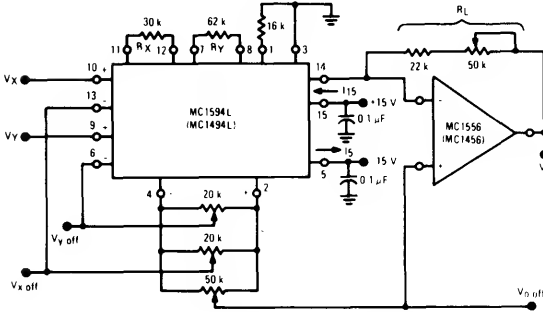


FIGURE 4 - INPUT BIAS CURRENT/INPUT OFFSET CURRENT, OUTPUT RESISTANCE

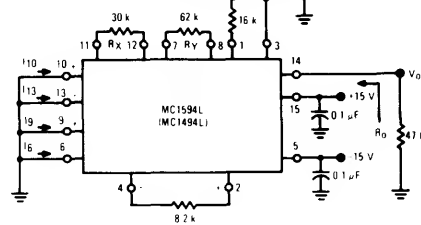


FIGURE 5 - FREQUENCY RESPONSE

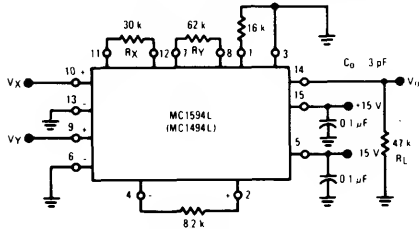


FIGURE 6 - COMMON MODE

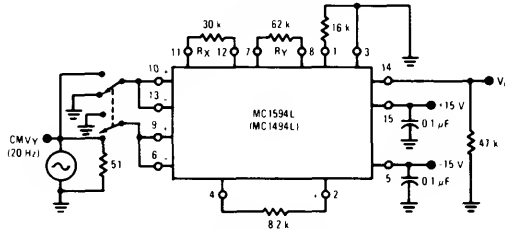


FIGURE 7 - POWER SUPPLY SENSITIVITY

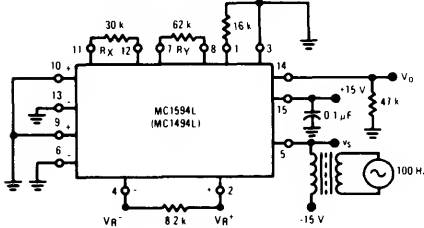
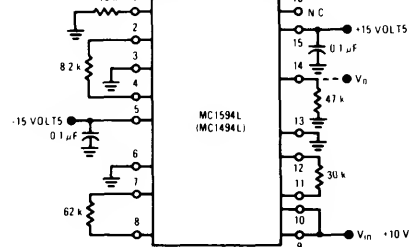


FIGURE 8 - BURN-IN



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TYPICAL CHARACTERISTICS

(Unless otherwise noted, $V^+ = +15\text{ V}$, $V^- = -15\text{ V}$, $R_1 = 16\text{ k}\Omega$, $R_X = 30\text{ k}\Omega$, $R_Y = 62\text{ k}\Omega$, $R_L = 47\text{ k}\Omega$, $T_A = +25^\circ\text{C}$)

FIGURE 9 – FREQUENCY RESPONSE OF Y INPUT
versus LOAD RESISTANCE

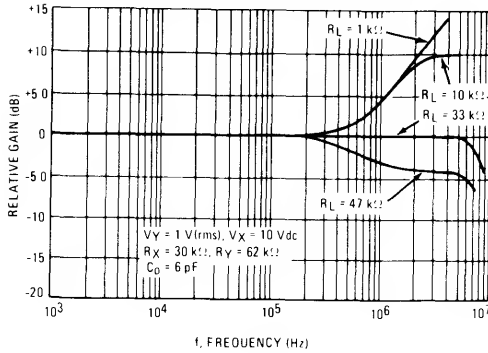


FIGURE 10 – FREQUENCY RESPONSE OF
X INPUT versus LOAD RESISTANCE

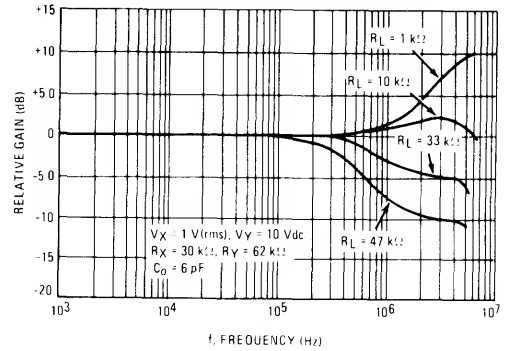


FIGURE 11 – LARGE SIGNAL VOLTAGE versus FREQUENCY

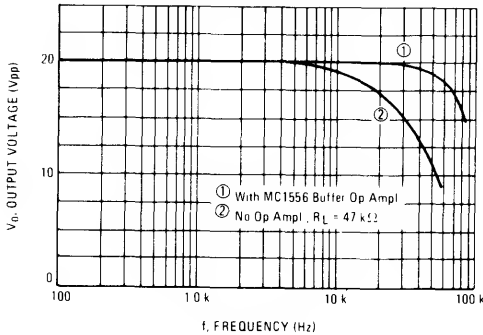


FIGURE 12 – LINEARITY versus R_X OR R_Y WITH $K = 1/10$

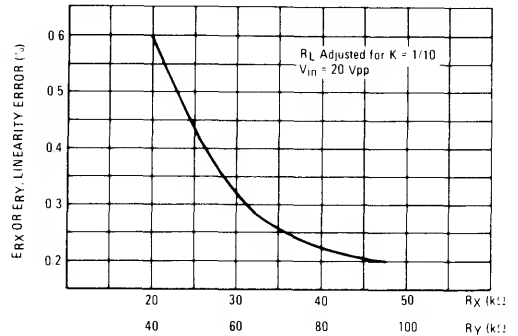


FIGURE 13 – LINEARITY versus R_X OR R_Y WITH $K = 1$

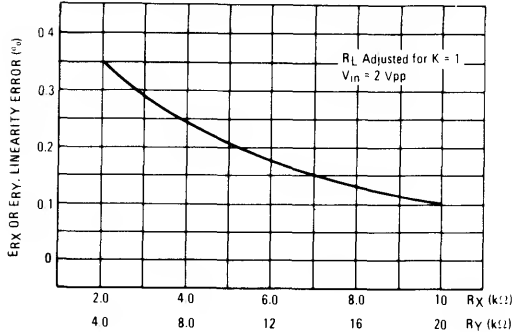
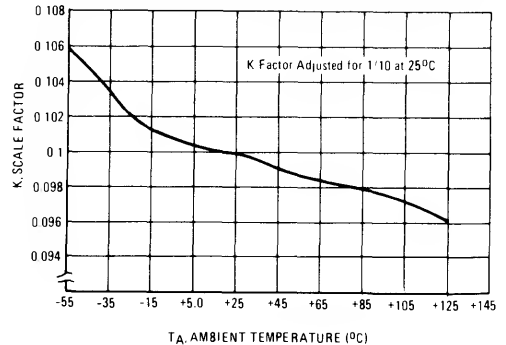


FIGURE 14 – SCALE FACTOR (K) versus TEMPERATURE



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GENERAL INFORMATION

CIRCUIT DESCRIPTION

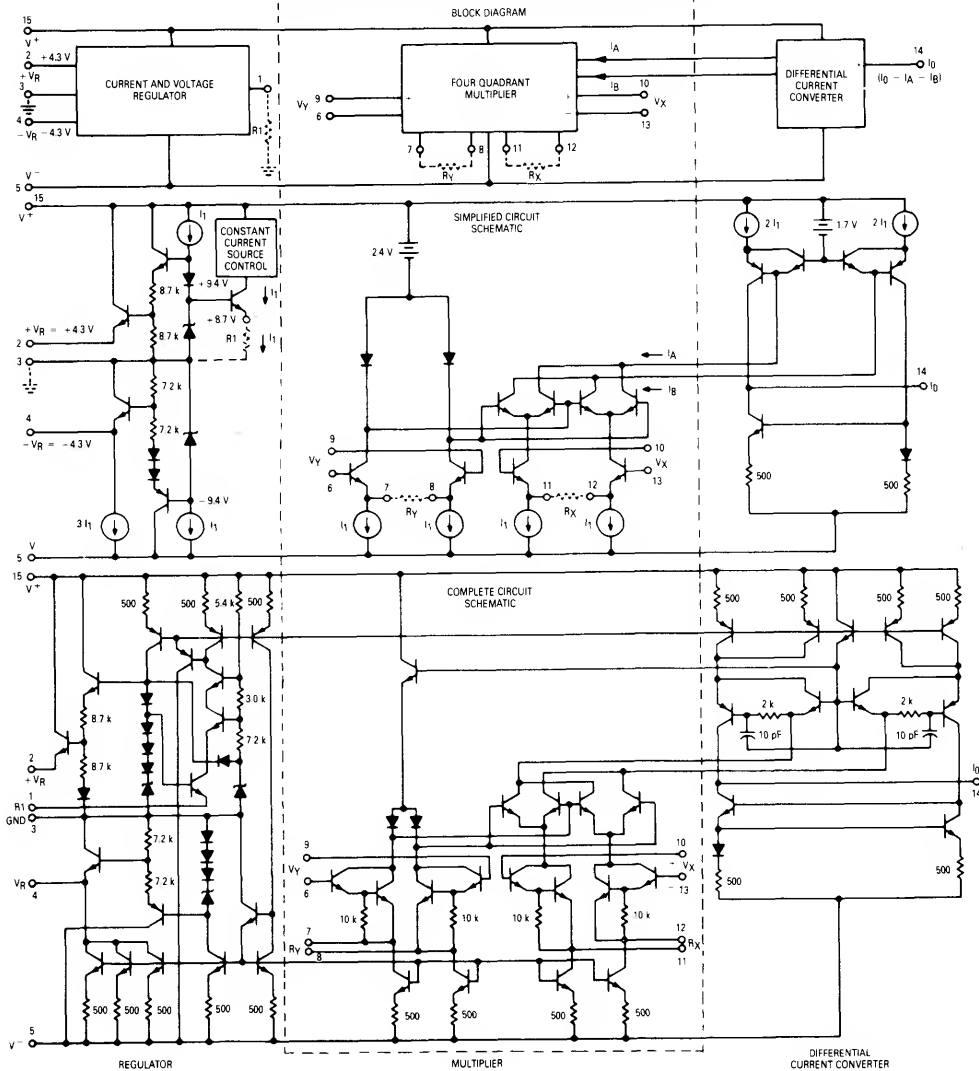
Introduction

The MC1594 is a monolithic, four-quadrant multiplier that operates on the principle of variable transconductance. It features a single-ended current output referenced to ground and provides two complementary regulated voltages for use

with the offset adjust circuits to virtually eliminate sensitivity of the offset voltage nulls to changes in supply voltage.

As shown in Figure 15, the MC1594 consists of a multiplier proper and associated peripheral circuitry to provide these features

FIGURE 15
(Recommended External Circuitry is Depicted With Dotted Lines)



MC1494L, MC1594L

Regulator (Figure 15)

The regulator biases the entire MC1594 circuit making it essentially independent of supply variation. It also provides two convenient regulated supply voltages which can be used in the offset adjust circuitry. The regulated output voltage at pin 2 is approximately +4.3 V while the regulated voltage at pin 4 is approximately -4.3 V. For optimum temperature stability of these regulated voltages, it is recommended that $|I_2| = |I_4| = 1.0 \text{ mA}$ (equivalent load of 8.6 k Ω). As will be shown later, there will normally be two 20 k-ohm potentiometers and one 50 k-ohm potentiometer connected between pins 2 and 4.

The regulator also establishes a constant current reference that controls all of the constant current sources in the MC1594. Note that all current sources are related to current I_1 which is determined by R_1 . For best temperature performance, R_1 should be 16 k Ω so that $I_1 \approx 0.5 \text{ mA}$ for all applications.

Multiplier (Figure 15)

The multiplier section of the MC1594 (center section of Figure 15) is nearly identical to the MC1595 and is discussed in detail in Application Note AN-489, "Analysis and Basic Operation of the MC1595". The result of this analysis is that the differential output current of the multiplier is given by:

$$I_A - I_B \approx \Delta I \approx \frac{2V_X V_Y}{R_X R_Y I_1}$$

Therefore, the output is proportional to the product of the two input voltages.

Differential Current Converter (Figure 15)

This portion of the circuitry converts the differential output current ($I_A - I_B$) of the multiplier to a single-ended output current (I_O).

$$I_O = I_A - I_B$$

or

$$I_O = \frac{2V_X V_Y}{R_X R_Y I_1}$$

The output current can be easily converted to an output voltage by placing a load resistor R_L from the output (pin 14) to ground (Figure 17) or by using an op-amp as a current-to-voltage converter (Figure 16). The result in both circuits is that the output voltage is given by:

$$V_O = \frac{2R_L V_X V_Y}{R_X R_Y I_1} = K V_X V_Y$$

$$\text{where } K (\text{scale factor}) = \frac{2R_L}{R_X R_Y I_1}$$

DC OPERATION

Selection of External Components

For low frequency operation the circuit of Figure 16 is recommended. For this circuit, $R_X = 30 \text{ k}\Omega$, $R_Y = 62 \text{ k}\Omega$, $R_1 = 16 \text{ k}\Omega$ and hence $I_1 \approx 0.5 \text{ mA}$. Therefore, to set the scale factor, K , equal to 1/10, the value of R_L can be calculated to be:

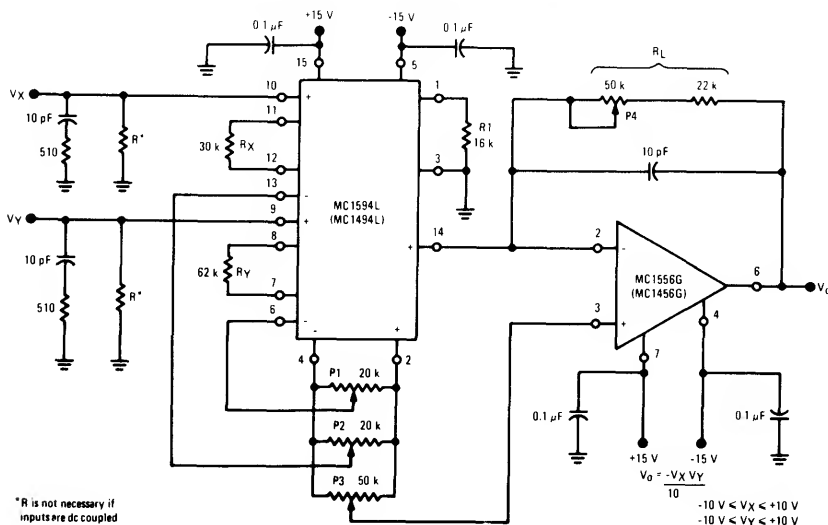
$$K = \frac{1}{10} = \frac{2R_L}{R_X R_Y I_1}$$

$$\text{or } R_L = \frac{R_X R_Y I_1}{(2)(10)} = \frac{(30 \text{ k})(62 \text{ k})(0.5 \text{ mA})}{20}$$

$$R_L = 46.5 \text{ k}$$

Thus, a reasonable accuracy in scale factor can be achieved by making R_L a fixed 47 k Ω resistor. However, if it is desired

FIGURE 16 - TYPICAL MULTIPLIER CONNECTION



that the scale factor be exact, R_L can be comprised of a fixed resistor and a potentiometer as shown in Figure 16. It should be pointed out that there is nothing magic about setting the scale factor to 1/10. This is merely a convenient factor to use if the V_X and V_Y input voltages are expected to be large, say ± 10 V. Obviously with $V_X = V_Y = 10$ V and a scale factor of unity, the device could not hope to provide a 100 V output, so the scale factor is set to 1/10 and provides an output scaled down by a factor of ten. For many applications it may be desirable to set $K = 1/2$ or $K = 1$ or even $K = 100$. This can be accomplished by adjusting R_X , R_Y and R_L appropriately.

The selection of R_L is arbitrary and can be chosen after resistors R_X and R_Y are found. Note in Figure 16 that R_Y is 62 k Ω while R_X is 30 k Ω . The reason for this is that the "Y" side of the multiplier exhibits a second order non-linearity whereas the "X" side exhibits a simple non-linearity. By making the R_Y resistor approximately twice the value of the R_X resistor, the linearity on both the "X" and "Y" sides are made equal. The selection of the R_X and R_Y resistor values is dependent upon the expected amplitude of V_X and V_Y inputs. To maintain a specified linearity, resistors R_X and R_Y should be selected according to the following equations

$$R_X \geq 3 V_X (\text{max}) \text{ in k}\Omega \text{ when } V_X \text{ is in volts}$$

$$R_Y \geq 6 V_Y (\text{max}) \text{ in k}\Omega \text{ when } V_Y \text{ is in volts}$$

For example, if the maximum input on the "X" side is ± 1 volt, resistor R_X can be selected to be 3 k Ω . If the maximum input on the "Y" side is also ± 1 volt, then resistor R_Y can be selected to be 6 k Ω (6.2 k Ω nominal value). If a scale factor of $K = 10$ is desired, the load resistor is found to be 47 k Ω . In this example, the multiplier provides a gain of 20 dB.

Operational Amplifier Selection

The operational amplifier connection in Figure 16 is a simple but extremely accurate current-to-voltage converter. The output current of the multiplier flows through the feedback resistor R_L to provide a low impedance output voltage from the op-amp. Since the offset current and bias currents of the op-amp will cause errors in the output voltage, particularly with temperature, one with very low bias and offset currents is recommended. The MC1556/MC1456 or MC1741/MC1741C are excellent choices for this application.

Since the MC1594 is capable of operation at much higher frequencies than the op-amp, the frequency characteristics of the circuit in Figure 16 will be primarily dependent upon the op-amp.

Stability

The current-to-voltage converter mode is a most demanding application for an operational amplifier. Loop gain is at its maximum and the feedback resistor in conjunction with stray or input capacitance at the multiplier output adds additional phase shift. It may therefore be necessary to add (particularly in the case of internally compensated op-amps.) a small feedback capacitor to reduce loop gain at the higher frequencies. A value of 10 pF in parallel with R_L should be adequate to insure stability over production and temperature variations, etc.

An externally compensated op-amp. might be employed using slightly heavier compensation than that recommended for unity-gain operation.

Offset Adjustment

The non-inverting input of the op-amp. provides a convenient point to adjust the output offset voltage. By connecting this point to the wiper arm of a potentiometer (P3), the output

offset voltage can be adjusted to zero (see offset and scale factor adjustment procedure).

The input offset adjustment potentiometers, P1 and P2 will be necessary for most applications where it is desirable to take advantage of the multiplier's excellent linearity characteristics. Depending upon the particular application, some of the potentiometers can be omitted (see Figures 17, 19, 22, 24 and 25).

Offset and Scale Factor Adjustment Procedure

The adjustment procedure for the circuit of Figure 16 is:

- A. X Input Offset
 - (a) connect oscillator (1 kHz, 5 Vpp sine wave) to the "Y" input (pin 9)
 - (b) connect "X" input (pin 10) to ground
 - (c) adjust X-offset potentiometer, P2 for an ac null at the output
- B. Y Input Offset
 - (a) connect oscillator (1 kHz, 5 Vpp sine wave) to the "X" input (pin 10)
 - (b) connect "Y" input (pin 9) to ground
 - (c) adjust Y-offset potentiometer, P1 for an ac null at the output
- C. Output Offset
 - (a) connect both "X" and "Y" inputs to ground
 - (b) adjust output offset potentiometer, P3, until the output voltage V_O is zero volts dc
- D. Scale Factor
 - (a) apply +10 Vdc to both the "X" and "Y" inputs
 - (b) adjust P4 to achieve -10.00 V at the output
 - (c) apply -10 Vdc to both "X" and "Y" inputs and check for $V_O = -10.00$ V
- E. Repeat steps A through D as necessary.

The ability to accurately adjust the MC1594 is dependent on the offset adjust potentiometers. Potentiometers should be of the "infinite" resolution type rather than wirewound. Fine adjustments in balanced-modulator applications may require two potentiometers to provide "coarse" and "fine" adjustment. Potentiometers should have low temperature coefficients and be free from backlash.

Temperature Stability

While the MC1594 provides excellent performance in itself, overall performance depends to a large degree on the quality of the external components. Previous discussion shows the direct dependence on R_X , R_Y , and R_L and indirect dependence on R_1 (through I_1). Any circuit subjected to temperature variations should be evaluated with these effects in mind.

Bias Currents

The MC1594 multiplier, like most linear IC's, requires a dc bias current into its input terminals. The device cannot be capacitively coupled at the input without regard for this bias current. If inputs V_X and V_Y are able to supply the small bias current (≈ 0.5 μ A) resistors, R (Figure 16) can be omitted. If the MC1594 is used in an ac mode of operation and capacitive coupling is used the value of resistor R can be any reasonable value up to 100 k Ω . For minimum noise and optimum temperature performance, the value of resistor R should be as low as practical.

Parasitic Oscillation

When long leads are used on the inputs, oscillation may occur. In this event, an RC parasitic suppression network similar to the ones shown in Figure 16 should be connected directly to each input using short leads. The purpose of the network

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is to reduce the "Q" of the source-tuned circuits which cause the oscillation.

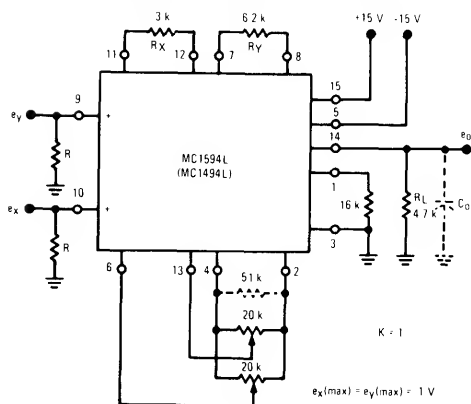
Inability to adjust the circuit to within the specified accuracy may be an indication of oscillation.

AC OPERATION

General

For ac operation, such as balanced modulation, frequency doubler, AGC, etc., the op-amp. will usually be omitted as well as the output offset adjust potentiometer. The output offset adjust potentiometer is omitted since the output will normally be ac-coupled and the dc voltage at the output is of no concern providing it is close enough to zero volts that it will not cause clipping in the output waveform. Figure 17

FIGURE 17 — WIDEBAND MULTIPLIER



shows a typical ac multiplier circuit with a scale factor $K \approx 1$. Again, resistor R_X and R_Y are chosen as outlined in the previous section, with R_L chosen to provide the required scale factor.

The offset voltage then existing at the output will be equal to the offset current times the load resistance. The output offset current of the MC1594 is typically $17 \mu A$ and $35 \mu A$ maximum. Thus, the maximum output offset would be about 160 mV.

Bandwidth

The bandwidth of the MC1594 is primarily determined by two factors. First, the dominant pole will be determined by the load resistor and the stray capacitance at the output terminal. For the circuit shown in Figure 17, assuming a total output capacitance (C_0) of 10 pF, the 3 dB bandwidth would be approximately 3.4 MHz. If the load resistor were $47 k\Omega$, the bandwidth would be approximately 340 kHz.

Secondly, a "zero" is present in the frequency response characteristic for both the "X" and "Y" inputs which causes the output signal to rise in amplitude at a 6 dB/octave slope at frequencies beyond the breakpoint of the "zero". The "zero" is caused by the parasitic and substrate capacitance which is related to resistors R_X and R_Y and the transistors associated with them. The affect of these transmission

"zeros" is seen in Figures 9 and 10. The reason for this increase in gain is due to the bypassing of R_X and R_Y at high frequencies. Since the R_Y resistor is approximately twice the value of the R_X resistor, the zero associated with the "Y" input will occur at approximately one octave below the zero associated with the "X" input. For $R_X = 30 k\Omega$ and $R_Y = 62 k\Omega$, the zeros occur at 1.5 MHz for the "X" input and 700 kHz for the "Y" input. These two measured breakpoints correspond to a shunt capacitance of about 3.5 pF. Thus, for the circuit of Figure 17, the "X" input zero and "Y" input zero will be at approximately 15 MHz and 7 MHz respectively.

It should be noted that the MC1594 multiplies in the time domain, hence, its frequency response is found by means of complex convolution in the frequency (Laplace) domain. This means that if the "X" input does not involve a frequency, it is not necessary to consider the "X" side frequency response in the output product. Likewise, for the "Y" side. Thus, for applications such as a wideband linear AGC amplifier which has a dc voltage as one input, the multiplier frequency response has one zero and one pole. For applications which involve an ac voltage on both the "X" and "Y" side, such as a balanced modulator, the product voltage response will have two zeros and one pole, hence, peaking may be present in the output.

From this brief discussion, it is evident that for ac applications; (1) the value of resistors R_X , R_Y and R_L should be kept as small as possible to achieve maximum frequency response, and (2) it is possible to select a load resistor R_L such that the dominant pole ($R_L C_0$) cancels the input zero ($R_X 3.5 pF$ or $R_Y 3.5 pF$) to give a flat amplitude characteristic with frequency. This is shown in Figures 9 and 10. Examination of the frequency characteristics of the "X" and "Y" inputs will demonstrate that for wideband amplifier applications, the best tradeoff with frequency response and gain is achieved by using the "Y" input for the ac signal.

For ac applications requiring bandwidths greater than those specified for the MC1594, two other devices are recommended. For modulator-demodulator applications, the MC1596 may be used up to 100 MHz. For wideband multiplier applications, the MC1595 (using small collector loads and ac coupling) can be used.

Slew-Rate

The MC1594 multiplier is not slew-rate limited in the ordinary sense that an op-amp. is. Since all the signals in the multiplier are currents and not voltages, there is no charging and discharging of stray capacitors and thus no limitations beyond the normal device limitations. However, it should be noted that the quiescent current in the output transistors is 0.5 mA and thus the maximum rate of change of the output voltage is limited by the output load capacitance by the simple equation:

$$\text{Slew-Rate} \frac{\Delta V_O}{\Delta T} = \frac{I_O}{C}$$

Thus, if C_0 is 10 pF, the maximum slew-rate would be:

$$\frac{\Delta V_O}{\Delta T} = \frac{0.5 \times 10^{-3}}{10 \times 10^{-12}} = 50 V/\mu s$$

This can be improved if necessary by addition of an emitter-follower or other type of buffer.

Phase-Vector Error

All multipliers are subject to an error which is known as the phase-vector error. This error is a phase error only and does not contribute an amplitude error per se. The phase-vector

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error is best explained by an example. If the "X" input is described in vector notation as

$$X = A \angle 0^\circ$$

and the "Y" input is described as

$$Y = B \angle \phi$$

then the output product would be expected to be

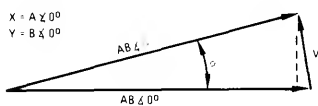
$$V_O = AB \angle \phi \text{ (see Figure 18)}$$

However, due to a relative phase shift between the "X" and "Y" channels, the output product will be given by

$$V_O = AB \angle \phi$$

Notice that the magnitude is correct but the phase angle of the product is in error. The vector, V , associated with this error is the "phase-vector error". The startling fact about the phase-vector error is that it occurs and accumulates much more rapidly than the amplitude error associated with frequency response. In fact, a relative phase shift of only 0.57° will result in a 1% phase-vector error. For most applications, this error is meaningless. If phase of the output product is not important, then neither is the phase-vector error. If phase is important, such as in the case of double sideband modulation or demodulation, then a 1% phase-vector error will represent a 1% amplitude error at the phase angle of interest.

FIGURE 18 — PHASE-VECTOR ERROR



Circuit Layout

If wideband operation is desired, careful circuit layout must be observed. Stray capacitance across R_X and R_Y should be avoided to minimize peaking (caused by a zero created by the parallel RC circuit).

DC APPLICATIONS

Squaring Circuit

If the two inputs are connected together, the resultant function is squaring:

$$V_O = KV^2$$

where K is the scale factor (see Figure 19).

However, a more careful look at the multiplier's defining equation will provide some useful information. The output voltage, without initial offset adjustments is given by:

$$V_O = K(V_X + V_{IOX} - V_{X\text{ off}})(V_Y + V_{IOY} - V_{Y\text{ off}}) + V_{OO}$$

(See "Definitions" for an explanation of terms).

With $V_X = V_Y = V$ (squaring) and defining

$$\epsilon_X = V_{IOX} - V_{X\text{ off}}$$

$$\epsilon_Y = V_{IOY} - V_{Y\text{ off}}$$

The output voltage equation becomes

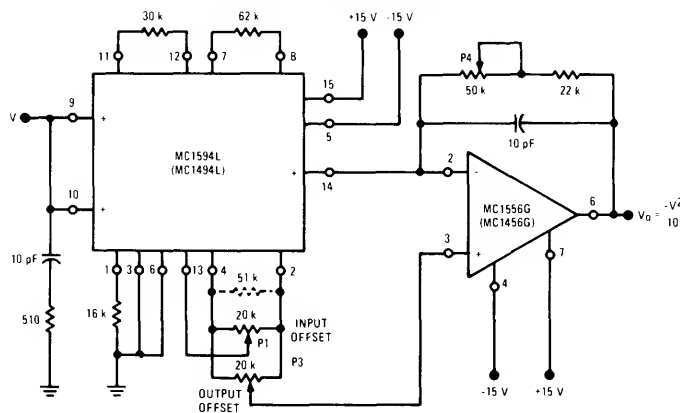
$$V_O = K V_X^2 + K V_X (\epsilon_X + \epsilon_Y) + K \epsilon_X \epsilon_Y + V_{OO}$$

This shows that all error terms can be eliminated with only three adjustment potentiometers, eliminating one of the input offset adjustments. For instance, if the "X" input offset adjustment is eliminated, ϵ_X is determined by the internal offset, V_{IOX} , but ϵ_Y is adjustable to the extent that the $(\epsilon_X + \epsilon_Y)$ term can be zeroed. Then the output offset adjustment is used to adjust the V_{OO} term and thus zero the remaining error terms. An ac procedure for nulling with three adjustments is:

A. AC Procedure

1. Connect oscillator (1 kHz, 15 Vpp) to input
2. Monitor output at 2 kHz with tuned voltmeter and adjust P4 for desired gain. (Be sure to peak response of voltmeter)
3. Tune voltmeter to 1 kHz and adjust P1 for a minimum output voltage
4. Ground input and adjust P3 (output offset) for zero volts dc out
5. Repeat steps 1 through 4 as necessary.

FIGURE 19 — MC1594 SQUARING CIRCUIT



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B. DC Procedure:

1. Set $V_X = V_Y = 0$ V and adjust P3 (output offset potentiometer) such that $V_O = 0.0$ Vdc
2. Set $V_X = V_Y = 1.0$ V and adjust P1 (Y input offset potentiometer) such that the output voltage is -0.100 volts
3. Set $V_X = V_Y = 10$ Vdc and adjust P4 (load resistor) such that the output voltage is -10.00 volts
4. Set $V_X = V_Y = -10$ Vdc and check that $V_O = -10$ V. Repeat steps 1 through 4 as necessary.

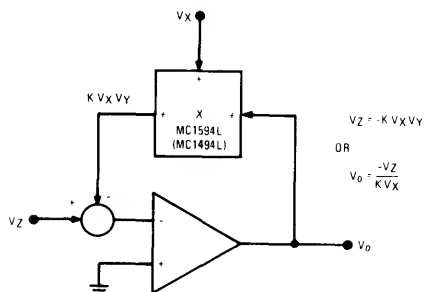
Divide

Divide circuits warrant a special discussion as a result of their special problems. Classic feedback theory teaches that if a multiplier is used as a feedback element in an operational amplifier circuit, the divide function results. Figure 20 illustrates the theoretical simplicity of such an approach and a practical realization is shown in Figure 21.

The characteristic "failure" mode of the divide circuit is latch-up. One way it can occur is if V_X is allowed to go negative or, in some cases, if V_X approaches zero.

Figure 20 illustrates why this is so. For $V_X > 0$ the transfer function through the multiplier is non-inverting. Its output is fed to the inverting input of the op-amp. Thus, operation is in the negative feedback mode and the circuit is dc stable.

FIGURE 20 — BASIC DIVIDE CIRCUIT USING MULTIPLIER



Should V_X change polarity, the transfer function through the multiplier becomes inverting, the amplifier has positive feedback and latch-up results. The problem resulting from V_X being near zero is a result of the transfer through the multiplier being near zero. The op-amp. is then operating with a very high closed loop gain and error voltages can thus become effective in causing latch-up.

The other mode of latch-up results from the output voltage of the op-amp. exceeding the rated common-mode input voltage of the multiplier. The input stage of the multiplier becomes saturated, phase reversal results, and the circuit is latched up. The circuit of Figure 21 protects against this happening by clamping the output swing of the op-amp. to approximately ± 10.7 volts. Five-percent tolerance, 10-volt zeners are used to assure adequate output swing but still limit the output voltage of the op-amp. from exceeding the common-mode input range of the MC1594.

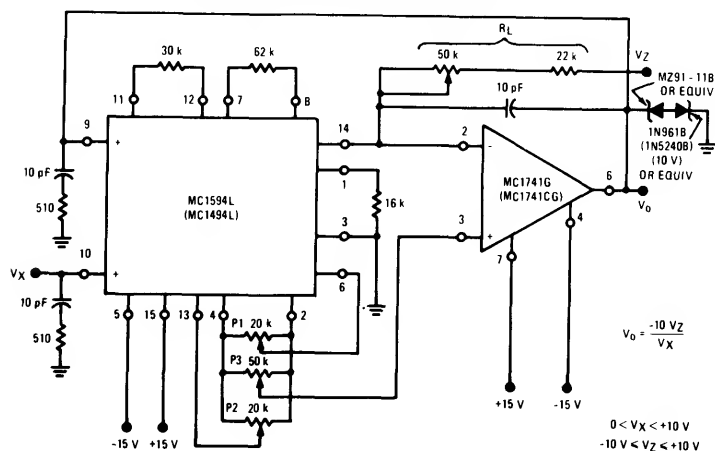
Setting up the divide circuit for reasonably accurate operation is somewhat different from the procedure for the multiplier itself. One approach, however, is to break the feedback loop, null out the multiplier circuit, and then close the loop.

A simpler approach, since it does not involve breaking the loop (thus making it more practical on a production basis), is:

1. Set $V_Z = 0$ volts and adjust the output offset potentiometer (P3) until the output voltage (V_O) remains at some (not necessarily zero) constant value as V_X is varied between $+1.0$ volt and $+10$ volts.
2. Maintain V_Z at 0 volts, set V_X at $+10$ volts and adjust the Y input offset potentiometer (P1) until $V_O = 0$ volts.
3. With $V_X = V_Z$, adjust the X input offset potentiometer (P2) until the output voltage remains at some (not necessarily -10 volts) constant value as $V_Z = V_X$ is varied between $+1.0$ volt and $+10$ volts.
4. Maintain $V_X = V_Z$ and adjust the scale factor potentiometer (R_L) until the average value of V_O is -10 volts as $V_Z = V_X$ is varied between $+1.0$ volt and $+10$ volts.
5. Repeat steps 1 through 4 as necessary to achieve optimum performance.

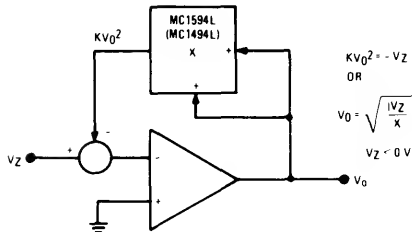
Users of the divide circuit should be aware that the accuracy to be expected decreases in direct proportion to the denomi-

FIGURE 21 — PRACTICAL DIVIDE CIRCUIT



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FIGURE 22 – BASIC SQUARE ROOT CIRCUIT



nator voltage. As a result, if V_X is set to 10 volts and 0.5% accuracy is available, then 5% accuracy can be expected when V_X is only 1 volt.

In accordance with an earlier statement, V_X may have only one polarity, positive, while V_Z may be either polarity.

Square Root

A special case of the divide circuit in which the two inputs to the multiplier are connected together results in the square root function as indicated in Figure 22. This circuit too may suffer from latch-up problems similar to those of the divide circuit. Note that only one polarity of input is allowed and diode clamping (see Figure 23) protects against accidental latch-up.

This circuit too, may be adjusted in the closed-loop mode

1. Set $V_Z = -0.01$ Vdc and adjust P3 (output offset) for $V_O = 0.316$ Vdc.
2. Set V_Z to -0.9 Vdc and adjust P2 ("X" adjust) for $V_O = +3$ Vdc.
3. Set V_Z to -10 Vdc and adjust P4 (gain adjust) for $V_O = +10$ Vdc.

Steps 1 through 3 may be repeated as necessary to achieve desired accuracy.

Note: Operation near zero volts input may prove very inaccurate, hence, it may not be possible to adjust V_0 to 0 but rather only to within 100 to 400 mV of zero.

AC APPLICATIONS

Wideband Amplifier With Linear AGC

If one input to the MC1594 is a dc voltage and a signal voltage is applied to the other input, the amplitude of the output signal can be controlled in a linear fashion by varying the dc voltage. Hence, the multiplier can function as a dc coupled, wideband amplifier with linear AGC control.

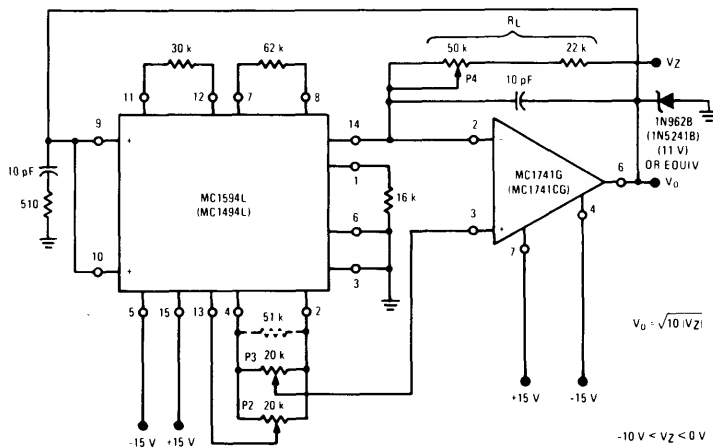
In addition to the advantage of Linear AGC control, the multiplier has three other distinct advantages over most other types of AGC systems. First, the AGC dynamic range is theoretically infinite. This stems from the basic fact that with zero volts dc applied to the AGC, the output will be zero regardless of the input. In practice, the dynamic range is limited by the ability to adjust the input offset adjust potentiometers. By using cermet multi-turn potentiometers, a dynamic range of 80 dB can be obtained. The second advantage of the multiplier is that variation of the AGC voltage has no effect on the signal handling capability of the signal port, nor does it alter the input impedance of the signal port. This feature is particularly important in AGC systems which are phase sensitive. A third advantage of the multiplier is that the output-voltage-swing capability and output impedance are unchanged with variations in AGC voltage.

The circuit of Figure 24 demonstrates the linear AGC amplifier. The amplifier can handle 1 V(rms) and exhibits a gain of approximately 20 dB. It is AGC'd through a 60 dB dynamic range with the application of an AGC voltage from 0 Vdc to 1 Vdc. The bandwidth of the amplifier is determined by the load resistor and output stray capacitance. For this reason, an emitter-follower buffer has been added to extend the bandwidth in excess of 1 MHz.

Balanced Modulator

When two-time variant signals are used as inputs, the result-

FIGURE 23 – SQUARE ROOT CIRCUIT



MC1494L, MC1594L

ing output is suppressed-carrier double-sideband modulation. In terms of sinusoidal inputs, this can be seen in the following equation:

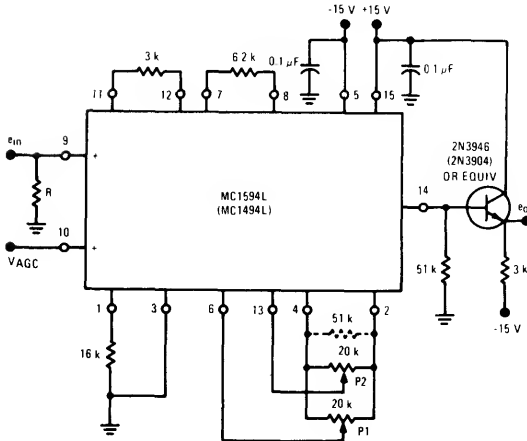
$$V_o = K(e_1 \cos \omega_m t)(e_2 \cos \omega_c t)$$

where ω_m is the modulation frequency and ω_c is the carrier frequency. This equation can be expanded to show the suppressed carrier or balanced modulation:

$$V_o = \frac{K e_1 e_2}{2} [\cos(\omega_c + \omega_m)t + \cos(\omega_c - \omega_m)t]$$

Unlike many modulation schemes, which are non-linear in nature, the modulation which takes place when using the MC1594 is linear. This means that for two sinusoidal inputs, the output will contain only two frequencies, the sum and difference, as seen in the above equation. There will be no spectrum centered about the second harmonic of the carrier, or any multiple of the carrier. For this reason, the filter requirements of a modulation system are reduced to the minimum. Figure 25 shows the MC1594 configuration to perform this function.

FIGURE 24 – WIDEBAND AMPLIFIER
WITH LINEAR AGC

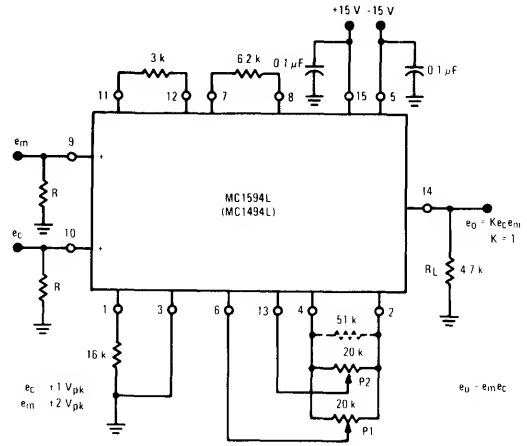


Notice that the resistor values for R_X , R_Y , and R_L have been modified. This has been done primarily to increase the bandwidth by lowering the output impedance of the MC1594 and then lowering R_X and R_Y to achieve a gain of 1. The e_c can be as large as 1 volt peak and e_m as high as 2 volts peak. No output offset adjust is employed since we are interested only in the ac output components.

The input R 's are used to supply bias current to the multiplier inputs as well as provide matching input impedance. The output frequency range of this configuration is determined by the 4.7 k ohm output impedance and capacitive loading. Assuming a 6 pF load, the small-signal bandwidth is 5.5 MHz.

The circuit of Figure 25 will provide a typical carrier rejection of ≥ 70 dB from 10 kHz to 1.5 MHz.

FIGURE 25 – BALANCED MODULATOR



The adjustment procedure for this circuit is quite simple.

(1) Place the carrier signal at pin 10. With no signal applied to pin 9, adjust potentiometer P1 such that an ac null is obtained at the output.

(2) Place a modulation signal at pin 9. With no signal applied to pin 10, adjust potentiometer P2 such that an ac null is obtained at the output.

Again, the ability to make careful adjustment of these offsets will be a function of the type of potentiometers used for P1 and P2. Multiple turn cermet type potentiometers are recommended.

Frequency Doubler

If for Figure 25 both inputs are identical:

$$e_m = e_c = E \cos \omega t$$

Then the output is given by

$$e_o = e_m e_c = E^2 \cos^2 \omega t$$

which reduces to

$$e_o = \frac{E^2}{2} (1 + \cos 2\omega t)$$

This equation states that the output will consist of a dc term equal to one half the peak voltage squared and the second harmonic of the input frequency. Thus, the circuit acts as a frequency doubler. Two facts about this circuit are worthy of note. First, the second harmonic of the input frequency is the only frequency appearing at the output. The fundamental does not appear. Second, if the input is sinusoidal, the output will be sinusoidal and requires no filtering.

The circuit of Figure 25 can be used as a frequency doubler with input frequencies in excess of 2 MHz.

Amplitude Modulator

The circuit of Figure 25 is also easily used as an amplitude modulator. This is accomplished by simply varying the input offset adjust potentiometer (P1) associated with the modu-

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lation input. This procedure places a dc offset on the modulation input of the multiplier such that the carrier still passes thru the multiplier when the modulating signal is zero. The result is amplitude modulation. This is easily seen by examining the basic mathematical expression for amplitude modulation given below. For the case under discussion, with $K = 1$,

$$e_o = (E + E_m \cos \omega_m t) (E_c \cos \omega_c t)$$

where E is the dc input offset adjust voltage. This expression can be written as:

$$e_o = E_o [1 + M \cos \omega_c t] \cos \omega_c t$$

where $E_o = EE_c$

and $M = \frac{E_m}{E} = \text{modulation index}$

This is the standard equation for amplitude modulation. From this, it is easy to see that 100% modulation can be achieved by adjusting the input offset adjust voltage to be exactly equal to the peak value of the modulation, E_m . This is done by observing the output waveform and adjusting the input offset potentiometer, P1, until the output exhibits the familiar amplitude modulation waveform.

Phase Detector

If the circuit of Figure 25 has as its inputs two signals of identical frequency but having a relative phase shift the output will be a dc signal which is directly proportional to the cosine of phase difference as well as the double frequency term

$$e_c = E_c \cos \omega_c t$$

$$e_m = E_m \cos(\omega_c t + \phi)$$

$$e_o = e_c e_m = E_c E_m \cos \omega_c t \cos(\omega_c t + \phi)$$

$$\text{or } e_o = \frac{E_c E_m}{2} [\cos \phi + \cos(2\omega_c t + \phi)]$$

The addition of a simple low pass filter to the output (which eliminates the second cosine term) and return of R_L to an offset adjustment potentiometer will result in a dc output voltage which is proportional to the cosine of the phase difference. Hence, the circuit functions as a synchronous detector.

DEFINITIONS OF SPECIFICATIONS

Because of the unique nature of a multiplier, i.e., two inputs and one output, operating specifications are difficult to define and interpret. Indeed the same specification may be defined in several completely different ways depending upon which manufacturer is doing the defining. In order to clear up some of this mystery, the following definitions and examples are presented.

Multiplier Transfer Function

The output of the multiplier may be expressed by this equation:

$$V_o = K(V_x \pm V_{ioX} - V_{x\text{off}})(V_y \pm V_{ioY} - V_{y\text{off}}) \pm V_{oo} \quad (1)$$

where K = scale factor (see 6.5)

V_x = "x" input voltage

V_y = "y" input voltage

V_{ioX} = "x" input offset voltage

V_{ioY} = "y" input offset voltage

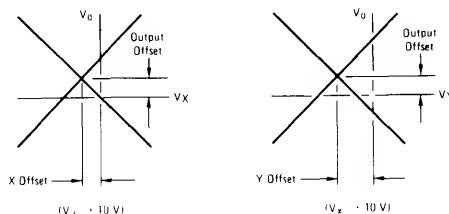
$V_{x\text{off}}$ = "x" input offset adjust voltage

$V_{y\text{off}}$ = "y" input offset adjust voltage

V_{oo} = output offset voltage

The voltage transfer characteristic below indicates "X", "Y" and output offset voltages.

FIGURE 26



Linearity

Linearity is defined to be the maximum deviation of output voltage from a straight line transfer function. It is expressed as a percentage of full-scale output and is measured for V_x and V_y separately either using an "X-Y" plotter (and checking the deviation from a straight line) or by using the method shown in Figure 1. The latter method nulls the output signal with the input signal, resulting in distortion components proportional to the linearity.

Example: 0.35% linearity means

$$V_o = \frac{V_x V_y}{10} \pm (0.0035) (10 \text{ volts})$$

Input Offset Voltage

The input offset voltage is defined from Equation (1). It is measured for V_x and V_y separately and is defined to be that dc input offset adjust voltage ("x" or "y") that will result in minimum ac output when ac (5 Vpp, 1 kHz) is applied to the other input ("y" or "x" respectively). From Equation (1) we have

$$V_o(\text{ac}) = K(1 \pm V_{ioX} - V_{x\text{off}})(\sin \omega t)$$

adjust $V_{x\text{off}}$ so that $(1 \pm V_{ioX} - V_{x\text{off}}) = 0$.

Output Offset Current and Voltage

Output offset current (I_{oo}) is the dc current flowing in the output lead when $V_x = V_y = 0$ and "X" and "Y" offset voltages are adjusted to zero.

Output offset voltage (V_{oo}) is

$$V_{oo} = I_{oo} R_L$$

where R_L is the load resistance.

Note: Output offset voltage is defined by many manufacturers with all inputs at zero but without adjusting "X" and "Y" offset voltages to zero. Thus it includes input offset terms, an output offset term and a scale factor term.

Scale Factor

Scale factor is the K term in Equation (1). It determines the "gain" of the multiplier and is expressed approximately by the following equation:

$$K = \frac{2R_L}{R_x R_y I_1} \text{ where } R_x \text{ and } R_y \gg \frac{kT}{qI_1}$$

and I_1 is the current out of pin 1.

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Total DC Accuracy

The total dc accuracy of a multiplier is defined as error in multiplier output with dc (± 10 Vdc) applied to both inputs. It is expressed as a percent of full scale. Accuracy is not specified for the MC1594 because error terms can be nulled by the user.

Temperature Stability (Drift)

Each term defined above will have a finite drift with temperature. The temperature specifications are obtained by re-adjusting the multiplier offsets and scale factor at each new temperature (see previous definitions and the adjustment procedure) and noting the change.

Assume inputs are grounded and initial offset voltages have been adjusted to zero. Then output voltage drift is given by

$$\Delta V_O = \pm [K \pm K (TCK) (\Delta T)] \pm [(TCV_{IOX}) (\Delta T)] \pm [(TCV_{IOY}) (\Delta T)] \pm (TCV_{OO}) (\Delta T)$$

Total DC Accuracy Drift

This is the temperature drift in output voltage with 10 volts applied to each input. The output is adjusted to 10 volts at $T_A = +25^\circ\text{C}$. Assuming initial offset voltages have been adjusted to zero at $T_A = +25^\circ\text{C}$, then

$$V_O = [K \pm K (TCK) (\Delta T)] [10 \pm (TCV_{IOX}) (\Delta T)] [10 \pm (TCV_{IOY}) (\Delta T)] \pm (TCV_{OO}) (\Delta T)$$

Power Supply Rejection

Variation in power supply voltages will cause undesired variation of the output voltage. It is measured by superimposing a 1-volt, 100-Hz signal on each supply (± 15 V) with each input grounded. The resulting change in the output is expressed in mV/V.

Output Voltage Swing

Output voltage swing capability is the maximum output voltage swing (without clipping) into a resistive load (note: output offset is adjusted to zero).

If an op-amp is used, the multiplier output becomes a virtual ground — the swing is then determined by the scale factor and the op-amp selected.

MC1495L
MC1595L

**WIDEBAND MONOLITHIC
FOUR-QUADRANT MULTIPLIER**

... designed for uses where the output is a linear product of two input voltages. Maximum versatility is assured by allowing the user to select the level shift method. Typical applications include: multiply, divide*, square root*, mean square*, phase detector, frequency doubler, balanced modulator/demodulator, electronic gain control.

*When used with an operational amplifier.

- Wide Bandwidth
- Excellent Linearity – 1% max Error on X-Input, 2% max Error on Y-Input – MC1595L
- Excellent Linearity – 2% max Error on X-Input, 4% max Error on Y-Input – MC1495L
- Adjustable Scale Factor, K
- Excellent Temperature Stability
- Wide Input Voltage Range – ± 10 Volts
- ± 15 Volt Operation

**LINEAR FOUR-QUADRANT
MULTIPLIER**

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

L SUFFIX
CERAMIC PACKAGE
CASE 632



**FIGURE 1 – FOUR-QUADRANT
MULTIPLIER TRANSFER CHARACTERISTIC**

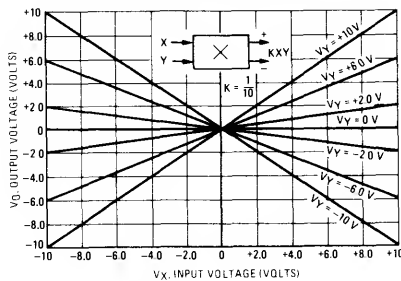


FIGURE 2 – TRANSCONDUCTANCE BANDWIDTH

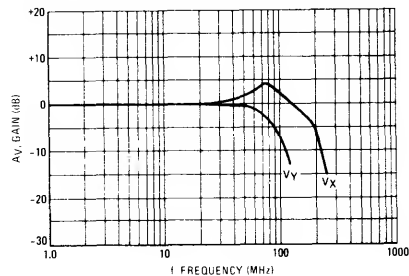
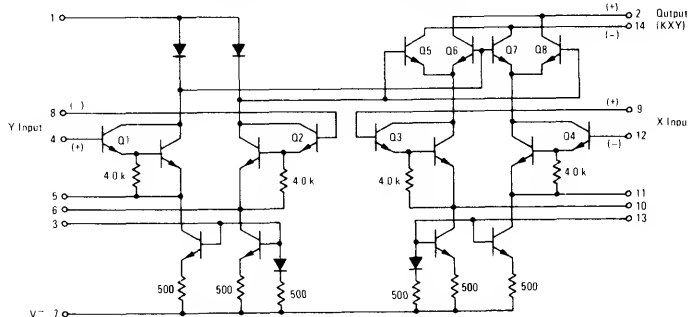


FIGURE 3 – CIRCUIT SCHEMATIC



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ELECTRICAL CHARACTERISTICS ($V^+ = +32\text{ V}$, $V^- = -15\text{ V}$, $T_A = +25^\circ\text{C}$, $I_3 = I_{13} = 1.0\text{ mA}$, $R_X = R_Y = 15\text{ k}\Omega$, $R_L = 11\text{ k}\Omega$ unless otherwise noted)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Linearity: Output Error in Percent of Full Scale: $T_A = +25^\circ\text{C}$ $-10 < V_X < +10$ ($V_Y = \pm 10\text{ V}$) $-10 < V_Y < +10$ ($V_X = \pm 10\text{ V}$) $T_A = 0\text{ to }+70^\circ\text{C}$ $-10 < V_X < +10$ ($V_Y = \pm 10\text{ V}$) $-10 < V_Y < +10$ ($V_X = \pm 10\text{ V}$) $T_A = -55^\circ\text{C to }+125^\circ\text{C}$ $-10 < V_X < +10$ ($V_Y = \pm 10\text{ V}$) $-10 < V_Y < +10$ ($V_X = \pm 10\text{ V}$)	5	ERX ERY ERX ERY ERX ERY	— — — — — —	± 1.0 ± 0.5 ± 2.0 ± 1.0 ± 1.5 ± 3.0	± 2.0 ± 1.0 ± 4.0 ± 2.0 — —	%
Squaring Mode Error: Accuracy in Percent of Full Scale After Offset and Scale Factor Adjustment $T_A = +25^\circ\text{C}$ $T_A = 0\text{ to }+70^\circ\text{C}$ $T_A = -55^\circ\text{C to }+125^\circ\text{C}$	5	ESQ	— — —	± 0.75 ± 0.5 ± 1.0 ± 0.75	— — —	%
Scale Factor (Adjustable) $(K = \frac{2R_L}{I_3 R_X R_Y})$	—	K	—	0.1	—	
Input Resistance ($f = 20\text{ Hz}$)	7	R_{INX} R_{INY}	— — —	30 35 20 35	— — —	M Ω
Differential Output Resistance ($f = 20\text{ Hz}$)	8	R_O	—	300	—	k Ω
Input Bias Current $I_{bx} = \frac{(I_9 + I_{12})}{2}$, $I_{by} = \frac{(I_4 + I_8)}{2}$	6	I_{bx} I_{by}	— — —	2.0 2.0 2.0 2.0	12 8.0 12 8.0	μA
Input Offset Current $ I_9 - I_{12} $ $ I_4 - I_8 $	6	$ I_{iox} $ $ I_{ioy} $	— — —	0.4 0.2 0.4 0.2	2.0 1.0 2.0 1.0	μA
Average Temperature Coefficient of Input Offset Current ($T_A = 0\text{ to }+70^\circ\text{C}$) ($T_A = -55^\circ\text{C to }+125^\circ\text{C}$)	6	$ TC_{Iio} $	— —	2.5 2.5	— —	nA/ $^\circ\text{C}$
Output Offset Current $ I_{14} - I_2 $	6	$ I_{oo} $	—	20 10	100 50	μA
Average Temperature Coefficient of Output Offset Current ($T_A = 0\text{ to }+70^\circ\text{C}$) ($T_A = -55^\circ\text{C to }+125^\circ\text{C}$)	6	$ TC_{Ioo} $	— —	20 20	— —	nA/ $^\circ\text{C}$
Frequency Response 3.0 dB Bandwidth, $R_L = 11\text{ k}\Omega$ 3.0 dB Bandwidth, $R_L = 50\text{ }\Omega$ (Transconductance Bandwidth) 3° Relative Phase Shift Between V_X and V_Y 1% Absolute Error Due to Input-Output Phase Shift	9,10	BW _{3dB} TBW _{3 dB} f_ϕ f_θ	— — — —	3.0 80 750 30	— — — —	MHz MHz kHz kHz
Common Mode Input Swing (Either Input)	11	CMV	± 10.5 ± 11.5	± 12 ± 13	— —	Vdc
Common Mode Gain (Either Input)	11	ACM	-40 -50	-50 -60	— —	dB
Common Mode Quiescent Output Voltage	12	V_{O1} V_{O2}	— —	21 21	— —	Vdc
Differential Output Voltage Swing Capability	9	V_O	—	± 14	—	V _{peak}
Power Supply Sensitivity	12	S^+ S^-	— —	5.0 10	— —	mV/V
Power Supply Current	12	I_7	—	6.0	7.0	mA
DC Power Dissipation	12	P_D	—	135	170	mW

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MAXIMUM RATINGS ($T_A = +25^{\circ}\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Applied Voltage ($V_2-V_1, V_{14}-V_1, V_1-V_9, V_1-V_{12}, V_1-V_4, V_1-V_8, V_{12}-V_7, V_9-V_7, V_8-V_7, V_4-V_7$)	ΔV	30	Vdc
Differential Input Signal	$V_{12}-V_9$ V_4-V_8	$\pm(6+1/3 R_X)$ $\pm(6+1/3 R_Y)$	Vdc Vdc
Maximum Bias Current	I_3 I_{13}	10 10	mA
Power Dissipation (Package Limitation) Ceramic Package Derate above $T_A = +25^\circ\text{C}$	P_D	750 5.0	mW mW/ $^\circ\text{C}$
Operating Temperature Range MC1495 MC1595	T_A	0 to +70 -55 to +125	$^\circ\text{C}$ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

TEST CIRCUITS

FIGURE 4 – LINEARITY (USING NULL TECHNIQUE)

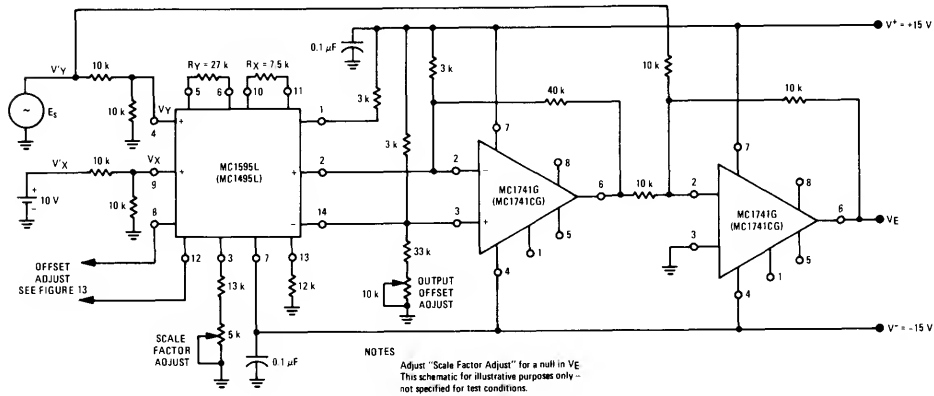
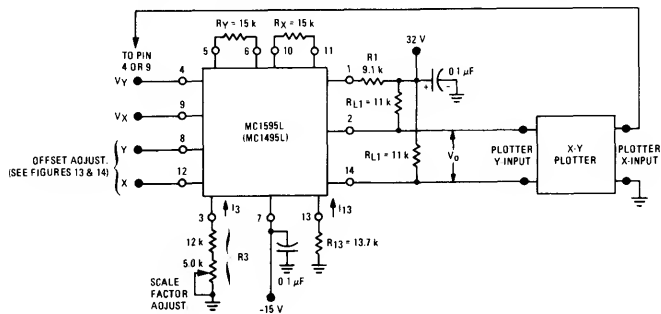


FIGURE 5 – LINEARITY (USING X-Y PLOTTER TECHNIQUE)



TEST CIRCUITS (continued)

FIGURE 7 – INPUT RESISTANCE

$e_1 = 1.0 \text{ V (rms)}$
20 Hz

$R_{INX} = R_{INY} = R \left| \frac{e_1}{e_2} - 2 \right|$

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TEST CIRCUITS (continued)

FIGURE 12 – POWER SUPPLY SENSITIVITY

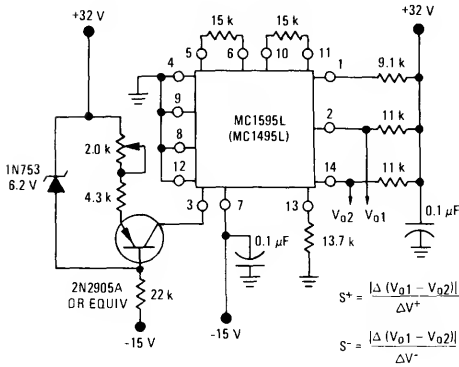


FIGURE 13 – OFFSET ADJUST CIRCUIT

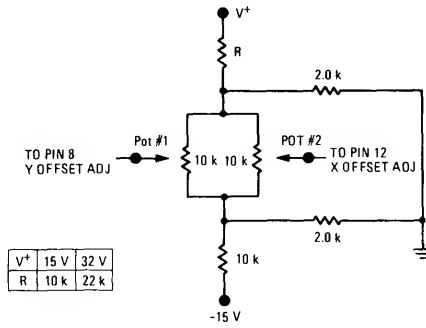
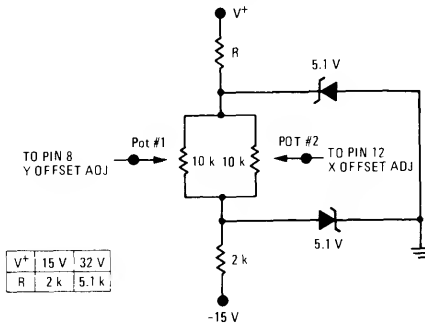


FIGURE 14 – OFFSET ADJUST CIRCUIT (ALTERNATE)



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TYPICAL CHARACTERISTICS

FIGURE 15 – LINEARITY versus TEMPERATURE

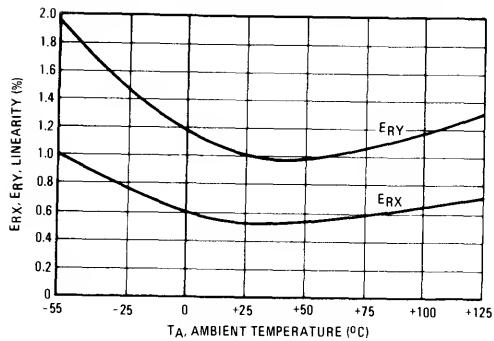


FIGURE 16 – SCALE FACTOR versus TEMPERATURE

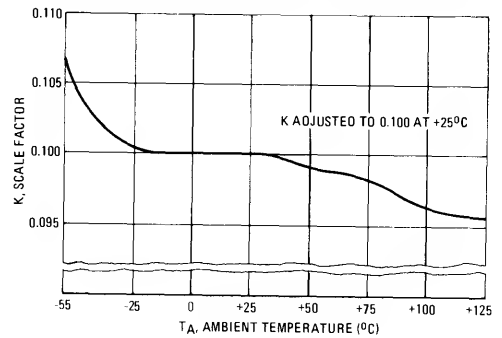


FIGURE 17 – ERROR CONTRIBUTED BY INPUT DIFFERENTIAL AMPLIFIER

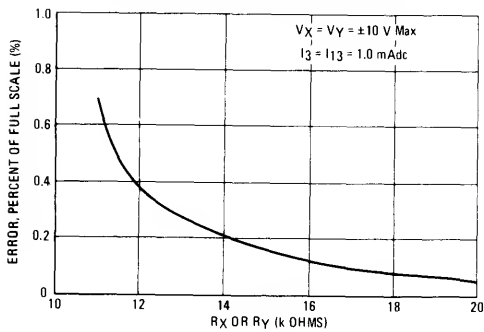


FIGURE 18 – ERROR CONTRIBUTED BY INPUT DIFFERENTIAL AMPLIFIER

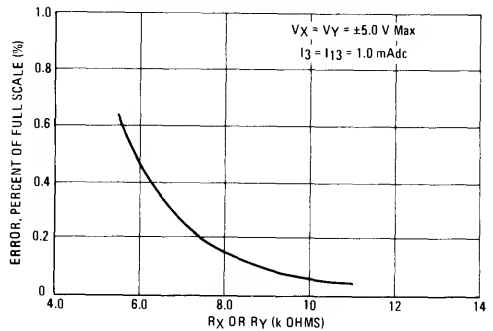
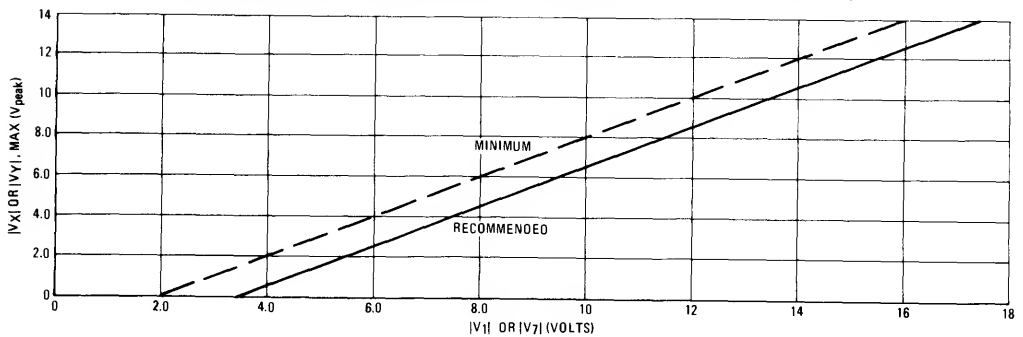


FIGURE 19 – MAXIMUM ALLOWABLE INPUT VOLTAGE versus VOLTAGE AT PIN 1 OR PIN 7



OPERATION AND APPLICATIONS INFORMATION

THEORY OF OPERATION

The MC1595 (MC1495) is a monolithic, four-quadrant multiplier which operates on the principle of variable transconductance. The detailed theory of operation is covered in Application Note AN-489, Analysis and Basic Operation of the MC1595. The result of this analysis is that the differential output current of the multiplier is given by

$$I_A - I_B = \Delta I = \frac{2V_X V_Y}{R_X R_Y I_{13}}$$

where I_A and I_B are the currents into pins 14 and 2, respectively, and V_X and V_Y are the X and Y input voltages at the multiplier input terminals.

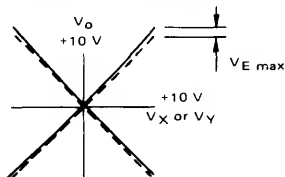
DESIGN CONSIDERATIONS

General

The MC1595 (MC1495) permits the designer to tailor the multiplier to a specific application by proper selection of external components. External components may be selected to optimize a given parameter (e.g. bandwidth) which may in turn restrict another parameter (e.g. maximum output voltage swing). Each important parameter is discussed in detail in the following paragraphs.

Linearity, Output Error, ER_X or ER_Y

Linearity error is defined as the maximum deviation of output voltage from a straight line transfer function. It is expressed as error in percent of full scale (see figure below).



For example, if the maximum deviation, $V_E(\text{max})$, is $\pm 100 \text{ mV}$ and the full scale output is 10 volts, then the percentage error is

$$ER = \frac{V_E(\text{max})}{V_O(\text{max})} \times 100 = \frac{100 \times 10^{-3}}{10} \times 100 = \pm 1.0\%$$

Linearity error may be measured by either of the following methods:

1. Using an X - Y plotter with the circuit shown in Figure 5, obtain plots for X and Y similar to the one shown above.
2. Use the circuit of Figure 4. This method nulls the level shifted output of the multiplier with the original input. The peak output of the null operational amplifier will be equal to the error voltage, $V_E(\text{max})$.

One source of linearity error can arise from large signal non-linearity in the X and Y-input differential amplifiers. To avoid introducing error from this source, the emitter degeneration resistors R_X and R_Y must be chosen large enough so that non-linear base-emitter voltage variation can be ignored. Figures 17 and 18 show the error expected from this source as a function of the values of R_X and R_Y with an operating current of 1.0 mA in each side of the differential amplifiers (i.e., $I_{13} = I_{13} = 1.0 \text{ mA}$).

3 dB Bandwidth and Phase Shift

Bandwidth is primarily determined by the load resistors and the stray multiplier output capacitance and/or the operational amplifier used to level shift the output. If wideband operation is desired, low value load resistors and/or a wideband operational amplifier should be used. Stray output capacitance will depend to a large extent on circuit layout.

Phase shift in the multiplier circuit results from two sources: phase shift common to both X and Y channels (due to the load resistor-output capacitance pole mentioned above) and relative phase shift between X and Y channels (due to differences in transadmittance in the X and Y channels). If the input to output phase shift is only 0.6° , the output product of two sine waves will exhibit a vector error of 1%. A 3° relative phase shift between V_X and V_Y results in a vector error of 5%.

Maximum Input Voltage

$V_X(\text{max})$, $V_Y(\text{max})$ maximum input voltages must be such that:

$$V_X(\text{max}) < I_{13} R_Y$$

$$V_Y(\text{max}) < I_{13} R_X$$

Exceeding this value will drive one side of the input amplifier to "cutoff" and cause non-linear operation.

Currents I_{13} and I_{13} are chosen at a convenient value (observing power dissipation limitation) between 0.5 mA and 2.0 mA, approximately 1.0 mA. Then R_X and R_Y can be determined by considering the input signal handling requirements.

$$\text{For } V_X(\text{max}) = V_Y(\text{max}) = 10 \text{ volts:}$$

$$R_X = R_Y > \frac{10 \text{ V}}{1.0 \text{ mA}} = 10 \text{ k}\Omega$$

$$\text{The equation } I_A - I_B = \frac{2V_X V_Y}{R_X R_Y I_{13}}$$

$$\text{is derived from } I_A - I_B = \frac{2V_X V_Y}{(R_X + \frac{2kT}{qI_{13}})(R_Y + \frac{2kT}{qI_{13}}) I_{13}}$$

$$\text{with the assumption } R_X \gg \frac{2kT}{qI_{13}} \text{ and } R_Y \gg \frac{2kT}{qI_{13}}$$

$$\text{At } T_A = +25^\circ\text{C and } I_{13} = I_{13} = 1 \text{ mA,}$$

$$\frac{2kT}{qI_{13}} = \frac{2kT}{qI_{13}} = 52 \Omega$$

Therefore, with $R_X = R_Y = 10 \text{ k}\Omega$ the above assumption is valid. Reference to Figure 19 will indicate limitations of $V_X(\text{max})$ or $V_Y(\text{max})$ due to V_{11} and V_{17} . Exceeding these limits will cause saturation or "cutoff" of the input transistors. See Step 4 of Section 3 (General Design Procedure) for further details.

Maximum Output Voltage Swing

The maximum output voltage swing is dependent upon the factors mentioned below and upon the particular circuit being considered.

For Figure 20 the maximum output swing is dependent upon V^+ for positive swing and upon the voltage at pin 1 for negative swing. The potential at pin 1 determines the quiescent level for transistors Q_5 , Q_6 , Q_7 , and Q_8 . This potential

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OPERATION AND APPLICATIONS INFORMATION (continued)

should be related so that negative swing at pins 2 or 14 does not saturate those transistors. See Section 3 for further information regarding selection of these potentials.

If an operational amplifier is used for level shift, as shown in Figure 21, the output swing (of the multiplier) is greatly reduced. See Section 3 for further details.

GENERAL DESIGN PROCEDURE

Selection of component values is best demonstrated by the following example: assume resistive dividers are used at the X and Y inputs to limit the maximum multiplier input to ± 5.0 volts ($V_X = V_Y(\max)$) for a ± 10 -volt input ($V_X' = V_Y'(\max)$). (See Figure 21). If an overall scale factor of $1/10$ is desired, then

$$V_o = \frac{V_X' V_Y'}{10} = \frac{(2V_X)(2V_Y)}{10} = 4/10 V_X V_Y.$$

Therefore, $K = 4/10$ for the multiplier (excluding the divider network).

Step 1. The first step is to select current I_3 and current I_{13} . There are no restrictions on the selection of either of these currents except the power dissipation of the device. I_3 and I_{13} will normally be one or two milliamperes. Further, I_3 does not have to be equal to I_{13} , and there is normally no need to make them different. For this example, let

$$I_3 = I_{13} = 1 \text{ mA.}$$

To set currents I_3 and I_{13} to the desired value, it is only necessary to connect a resistor between pin 13 and ground, and between pin 3 and ground. From the schematic shown in Figure 3,

FIGURE 20 — BASIC MULTIPLIER

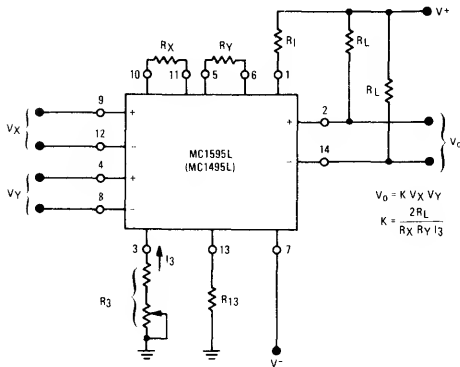
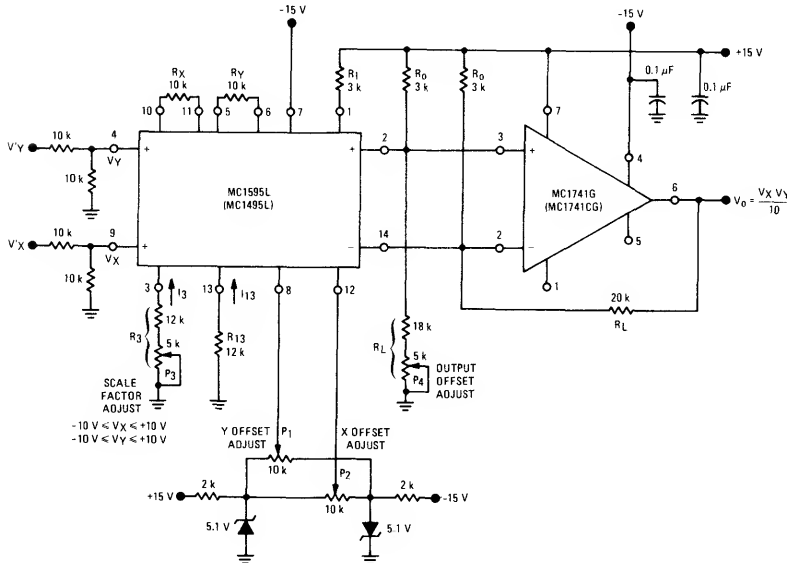


FIGURE 21 — MULTIPLIER WITH OP-AMPL. LEVEL SHIFT



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OPERATION AND APPLICATIONS INFORMATION (continued)

it can be seen that the resistor values necessary are given by:

$$R_{13} + 500 \Omega = \frac{|V^-| - 0.7 \text{ V}}{I_{13}}$$

$$R_3 + 500 \Omega = \frac{|V^-| - 0.7 \text{ V}}{I_3}$$

Let $V^- = -15 \text{ V}$

$$\text{Then } R_{13} + 500 = \frac{14.3 \text{ V}}{1 \text{ mA}} \text{ or } R_{13} = 13.8 \text{ k}\Omega$$

Let $R_{13} = 12 \text{ k}\Omega$

Similarly, $R_3 = 13.8 \text{ k}\Omega$

Let $R_3 = 15 \text{ k}\Omega$

However, for applications which require an accurate scale factor, the adjustment of R_3 and consequently, I_3 , offers a convenient method of making a final trim of the scale factor. For this reason, as shown in Figure 21, resistor R_3 is shown as a fixed resistor in series with a potentiometer.

For applications not requiring an exact scale factor (balanced modulator, frequency doubler, AGC amplifier, etc.), pins 3 and 13 can be connected together and a single resistor from pin 3 to ground can be used. In this case, the single resistor would have a value of one-half the above calculated value for R_{13} .

Step 2. The next step is to select R_X and R_Y . To insure that the input transistors will always be active, the following conditions should be met:

$$\frac{V_X}{R_X} < I_{13} \quad \frac{V_Y}{R_Y} < I_3$$

A good rule of thumb is to make $I_3 R_Y \geq 1.5 V_{Y(\text{max})}$ and $I_{13} R_X \geq 1.5 V_{X(\text{max})}$.

The larger the $I_3 R_Y$ and $I_{13} R_X$ product in relation to V_Y and V_X respectively, the more accurate the multiplier will be (see Figures 17 and 18).

$$\text{Let } R_X = R_Y = 10 \text{ k}\Omega$$

$$\text{Then } I_3 R_Y = 10 \text{ V}$$

$$I_{13} R_X = 10 \text{ V}$$

since $V_{X(\text{max})} = V_{Y(\text{max})} = 5.0 \text{ volts}$ the value of $R_X = R_Y = 10 \text{ k}\Omega$ is sufficient.

Step 3. Now that R_X , R_Y and I_3 have been chosen, R_L can be determined:

$$K = \frac{2R_L}{R_X R_Y I_3} = \frac{4}{10}$$

$$\text{or } \frac{(2)(R_L)}{(10 \text{ k})(10 \text{ k})(1 \text{ mA})} = \frac{4}{10}$$

$$\text{Thus } R_L = 20 \text{ k}\Omega$$

Step 4. To determine what power-supply voltage is necessary for this application, attention must be given to the circuit schematic shown in Figure 3. From the circuit schematic it can be seen that in order to maintain transistors Q_1 , Q_2 , Q_3 and Q_4 in an active

region when the maximum input voltages are applied ($V_X' = V_Y' = 10 \text{ V}$ or $V_X = 5.0 \text{ V}$, $V_Y = 5.0 \text{ V}$), their respective collector voltage should be at least a few tenths of a volt higher than the maximum input voltage. It should also be noticed that the collector voltage of transistors Q_3 and Q_4 are at a potential which is two diode-drops below the voltage at pin 1. Thus, the voltage at pin 1 should be about two volts higher than the maximum input voltage. Therefore, to handle $+5.0 \text{ volts}$ at the inputs, the voltage at pin 1 must be at least $+7.0 \text{ volts}$. Let $V_1 = 9.0 \text{ Vdc}$.

Since the current following into pin 1 is always equal to $2I_3$, the voltage at pin 1 can be set by placing a resistor, R_1 from pin 1 to the positive supply:

$$R_1 = \frac{V^+ - V_1}{2I_3}$$

$$\text{Let } V^+ = +15 \text{ V}$$

$$\text{Then } R_1 = \frac{15 \text{ V} - 9 \text{ V}}{(2)(1 \text{ mA})}$$

$$R_1 = 3 \text{ k}\Omega$$

Note that the voltage at the base of transistors Q_5 , Q_6 , Q_7 and Q_8 is one diode-drop below the voltage at pin 1. Thus, in order that these transistors stay active, the voltage at pins 2 and 14 should be approximately halfway between the voltage at pin 1 and the positive-supply voltage. For this example, the voltage at pins 2 and 14 should be approximately 11 volts.

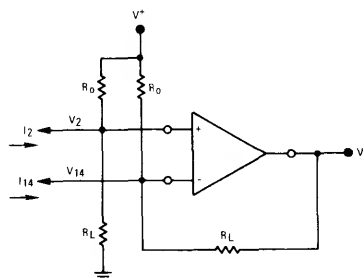
Step 5. For dc applications, such as the multiply, divide and square-root functions, it is usually desirable to convert the differential output to a single-ended output voltage referenced to ground. The circuit shown in Figure 22 performs this function. It can be shown that the output voltage of this circuit is given by:

$$V_O = (I_2 - I_{14}) R_L$$

$$\text{And since } I_A - I_B = I_2 - I_{14} = \frac{2I_X I_Y}{I_3} = \frac{2V_X V_Y}{I_3 R_X R_Y}$$

$$\text{Then } V_O = \frac{2R_L V_X' V_Y'}{4R_X R_Y I_3} \text{ where } V_X' V_Y' \text{ is the voltage at the input to the voltage dividers.}$$

FIGURE 22 — LEVEL SHIFT CIRCUIT

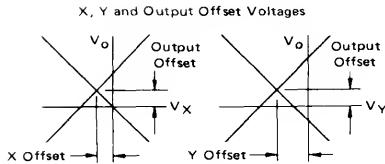


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11

11-34

OPERATION AND APPLICATIONS INFORMATION (continued)



For most dc applications, all three offset adjust potentiometers (P_1 , P_2 , P_4) will be necessary. One or more offset adjust potentiometers can be eliminated for ac applications (See Figures 28, 29, 30, 31).

If well regulated supply voltages are available, the offset adjust circuit of Figure 13 is recommended. Otherwise, the circuit of Figure 14 will greatly reduce the sensitivity to power supply changes.

Scale Factor

The scale factor, K , is set by P_3 (Figure 21). P_3 varies I_3 which inversely controls the scale factor K . It should be noted that current I_3 is one-half the current through R_1 . R_1 sets the bias level for Q_5 , Q_6 , Q_7 , and Q_8 (See Figure 3). Therefore, to be sure that these devices remain active under all conditions of input and output swing, care should be exercised in adjusting P_3 over wide voltage ranges (see Section 3, General Design Procedure).

Adjustment Procedures

The following adjustment procedure should be used to null the offsets and set the scale factor for the multiply mode of operation. (See Figure 21)

1. X Input Offset
 - (a) Connect oscillator (1 kHz, 5 Vpp sine wave) to the "Y" input (pin 4)
 - (b) Connect "X" input (pin 9) to ground
 - (c) Adjust X offset potentiometer, P_2 , for an ac null at the output
2. Y Input Offset
 - (a) Connect oscillator (1 kHz, 5 Vpp sine wave) to the "X" input (pin 9)
 - (b) Connect "Y" input (pin 4) to ground
 - (c) Adjust "Y" offset potentiometer, P_1 , for an ac null at the output
3. Output Offset
 - (a) Connect both "X" and "Y" inputs to ground
 - (b) Adjust output offset potentiometer, P_4 , until the output voltage V_O is zero volts dc
4. Scale Factor
 - (a) Apply +10 Vdc to both the "X" and "Y" inputs
 - (b) Adjust P_3 to achieve +10.00 V at the output.
5. Repeat steps 1 through 4 as necessary.

The ability to accurately adjust the MC1595 (MC1495) depends upon the characteristics of potentiometers P_1 through P_4 . Multi-turn, infinite resolution potentiometers with low-temperature coefficients are recommended.

DC APPLICATIONS

Multiply

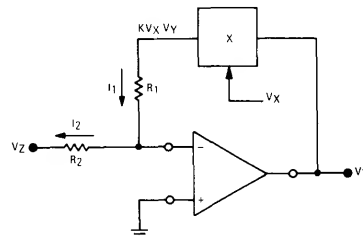
The circuit shown in Figure 21 may be used to multiply signals from dc to 100 kHz. Input levels to the actual multiplier are 5.0 V (max). With resistive voltage dividers the maximum could be very large — however, for this application two-to-one dividers have been used so that the maximum input level is 10 V. The maximum output level has also been designed for 10 V (max).

Squaring Circuit

If the two inputs are tied together, the resultant function is squaring; that is $V_O = KV^2$ where K is the scale factor. Note that all error terms can be eliminated with only three adjustment potentiometers, thus eliminating one of the input offset adjustments. Procedures for nulling with adjustments are given as follows:

1. AC Procedure:
 - (a) Connect oscillator (1 kHz, 15 Vpp) to input
 - (b) Monitor output at 2 kHz with tuned voltmeter and adjust P_3 for desired gain (be sure to peak response of the voltmeter)
 - (c) Tune voltmeter to 1 kHz and adjust P_1 for a minimum output voltage
 - (d) Ground input and adjust P_4 (output offset) for zero volts dc output
 - (e) Repeat steps a through d as necessary.
2. DC Procedure:
 - (a) Set $V_X = V_Y = 0$ V and adjust P_4 (output offset potentiometer) such that $V_O = 0.0$ Vdc
 - (b) Set $V_X = V_Y = 1.0$ V and adjust P_1 (Y input offset potentiometer) such that the output voltage is +0.100 volts
 - (c) Set $V_X = V_Y = 10$ Vdc and adjust P_3 such that the output voltage is +10.00 volts
 - (d) Set $V_X = V_Y = -10$ Vdc. Repeat steps a through d as necessary.

FIGURE 24 — BASIC DIVIDE CIRCUIT



Divide Circuit

Consider the circuit shown in Figure 24 in which the multiplier is placed in the feedback path of an operational amplifier. For this configuration, the operational amplifier will maintain a "virtual ground" at the inverting (-) input. Assuming that the bias current of the operational amplifier is negligible, then $I_1 = I_2$ and

$$\frac{KV_X V_Y}{R_1} = \frac{-V_Z}{R_2} \quad (1)$$

$$\text{Solving for } V_Y, \quad V_Y = \frac{-R_1}{R_2 K} \frac{V_Z}{V_X} \quad (2)$$

If $R_1 = R_2$

$$V_Y = \frac{-V_Z}{KV_X} \quad (3)$$

If $R_1 = KR_2$

$$V_Y = \frac{-V_Z}{V_X} \quad (4)$$

Hence, the output voltage is the ratio of V_Z to V_X and provides a divide function. This analysis is, of course, the ideal condition. If the multiplier error is taken into account, the output voltage is found to be

where ΔE is the error voltage at the output of the multiplier. From this equation, it is seen that divide accuracy is strongly dependent upon the accuracy at which the multiplier can be set, particularly at small values of V_Y . For example, assume that $R_1 = R_2$, and $K = 1/10$. For these conditions the output of the divide circuit is given by:

From equation 6, it is seen that only when $V_X = 10$ V is the error voltage of the divide circuit as low as the error of the multiply circuit. For example, when V_X is small, (0.1 volt) the error voltage of the divide circuit can be expected to be a hundred times the error of the basic multiplier circuit.

or from equation (5),

From equation 7, the percentage error is inversely related to voltage V_Z (i.e., for increasing values of V_Z , the percentage error decreases).

Two things should be emphasized concerning Figure 25.

1. The input voltage (V_X) must be greater than zero and must be positive. This insures that the current out of pin 2 of the multiplier will always be in a direction compatible with the polarity of V_Z .
2. Pins 2 and 14 of the multiplier have been interchanged in respect to the operational amplifiers input terminals. In this instance, Figure 25 differs from the circuit connection shown in Figure 21; necessitated to insure negative feedback around the loop.

1. Set $V_Z = 0$ volts and adjust the output offset potentiometer (P_4) until the output voltage (V_O) remains at some (not necessarily zero) constant value as V_X is varied between +1.0 volt and +10 volts.

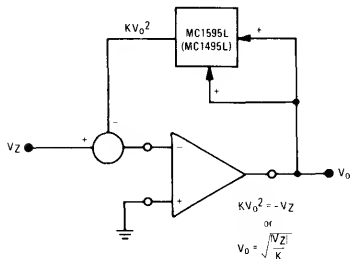
- ### Square Root

A special case of the divide circuit in which the two inputs to the multiplier are connected together is the square root function

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OPERATION AND APPLICATIONS INFORMATION (continued)

FIGURE 26 – BASIC SQUARE ROOT CIRCUIT



as indicated in Figure 26. This circuit may suffer from latch-up problems similar to those of the divide circuit. Note that only one polarity of input is allowed and diode clamping (see Figure 27) protects against accidental latch-up.

This circuit also may be adjusted in the closed-loop mode as follows:

1. Set V_Z to -0.01 volts and adjust P_4 (output offset) for $V_O = +0.316$ volts, being careful to approach the output from the positive side to preclude the effect of the output diode clamping.
2. Set V_Z to -0.9 volts and adjust P_2 (X adjust) for $V_O = +3.0$ volts.
3. Set V_Z to -10 volts and adjust P_3 (scale factor adjust) for $V_O = +10$ volts.
4. Steps 1 through 3 may be repeated as necessary to achieve desired accuracy.

AC APPLICATIONS

The applications that follow demonstrate the versatility of the monolithic multiplier. If a potted multiplier is used for these cases, the results generally would not be as good because the potted units have circuits that, although they optimize dc multiplication operation, can hinder ac applications.

Frequency doubling often is done with a diode where the fundamental plus a series of harmonics are generated. However, extensive filtering is required to obtain the desired harmonic, and the second harmonic obtained under this technique usually is small in magnitude and requires amplification.

When a multiplier is used to double frequency the second harmonic is obtained directly, except for a dc term, which can be removed with ac coupling.

$$e_{\text{rms}} = KE^2 \cos^2 \omega t$$

$$e = \frac{KE^2}{2} (1 + \cos 2\omega t).$$

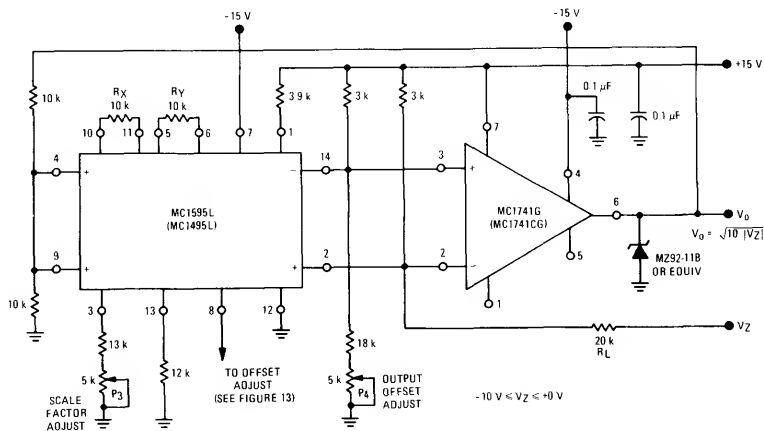
A potted multiplier can be used to obtain the double frequency component, but frequency would be limited by its internal level-shift amplifier. In the monolithic units, the amplifier is omitted.

In a typical doubler circuit, conventional ± 15 -volt supplies are used. An input dynamic range of 5.0 volts peak-to-peak is allowed. The circuit generates wave-forms that are double frequency; less than 1% distortion is encountered without filtering. The configuration has been successfully used in excess of 200 kHz; reducing the scale factor by decreasing the load resistors can further expand the bandwidth.

A slightly modified version of the MC1595 (MC1495) — the MC1596 (MC1496) — has been successfully used as a doubler to obtain 400 MHz. (See Figure 28.)

Figure 29 represents an application for the monolithic multiplier as a balanced modulator. Here, the audio input signal is 1.6 kHz and the carrier is 40 kHz.

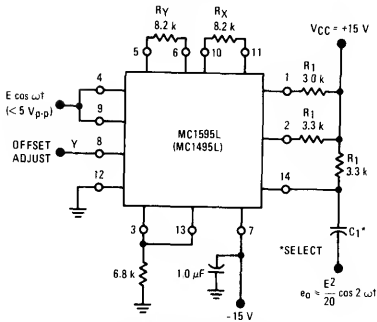
FIGURE 27 – SQUARE ROOT CIRCUIT



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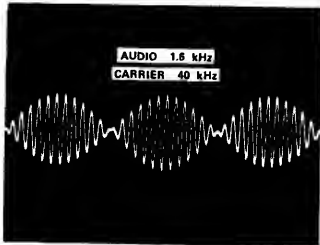
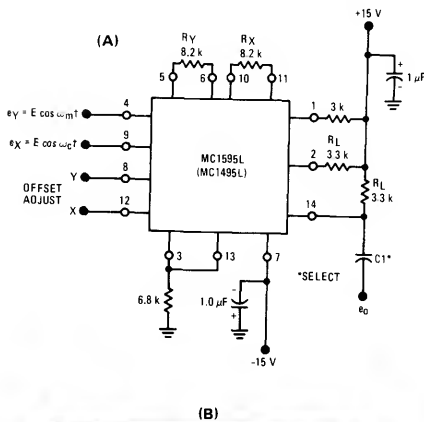
OPERATION AND APPLICATIONS INFORMATION (continued)

FIGURE 28 — FREQUENCY DOUBLER



When two equal cosine waves are applied to X and Y, the result is a wave shape of twice the input frequency. For this example the input was a 10 kHz signal, output was 20 kHz.

FIGURE 29 — BALANCED MODULATOR



The defining equation for balanced modulation is

$$K(E_m \cos \omega_m t)(E_c \cos \omega_c t) = \frac{KE_c E_m}{2} [\cos(\omega_c + \omega_m)t + \cos(\omega_c - \omega_m)t]$$

where ω_c is the carrier frequency, ω_m is the modulator frequency and K is the multiplier gain constant.

AC coupling at the output eliminates the need for level translation or an operational amplifier; a higher operating frequency results.

A problem common to communications is to extract the intelligence from single-sideband received signal. The ssb signal is of the form

$$e_{ssb} = A \cos(\omega_c + \omega_m)t$$

and if multiplied by the appropriate carrier waveform, $\cos \omega_c t$,

$$e_{ssb} e_{carrier} = \frac{AK}{2} [\cos(2\omega_c + \omega_m)t + \cos(\omega_c)t].$$

If the frequency of the band-limited carrier signal, ω_c , is ascertained in advance the designer can insert a low-pass filter and obtain the $(AK/2) \cos \omega_c t$ term with ease. He also can use an operational amplifier for a combination level shift-active filter, as an external component. But in potted multipliers, even if the frequency range can be covered, the operational amplifier is inside and not accessible, so the user must accept the level shifting provided, and still add a low-pass filter.

Amplitude Modulation

The multiplier performs amplitude modulation, similar to balanced modulation, when a dc term is added to the modulating signal with the Y offset adjust potentiometer. (See Figure 30.)

Here, the identity is

$$E_m(1 + m \cos \omega_m t)E_c \cos \omega_c t = KE_m E_c \cos \omega_c t + \frac{KE_m E_c m}{2} [\cos(\omega_c + \omega_m)t + \cos(\omega_c - \omega_m)t]$$

where m indicates the degree of modulation. Since m is adjustable, via potentiometer P1, 100% modulation is possible. Without extensive tweaking, 96% modulation may be obtained where ω_c and ω_m are the same as in the balanced-modulator example.

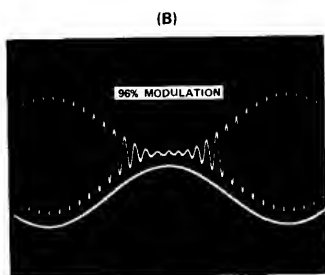
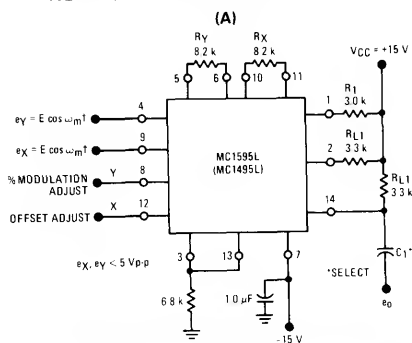
Linear Gain Control

To obtain linear gain control, the designer can feed to one of the two MC1595 (MC1495) inputs a signal that will vary the unit's gain. The following example demonstrates the feasibility of this application. Suppose a 200 kHz sine wave, 1.0 volt peak-to-peak, is the signal to which a gain control will be added. The dynamic range of the control voltage V_C is 0 to +1.0 volt. These must be ascertained and the proper values of R_X and R_Y can be selected for optimum performance. For the 200-kHz operating frequency, load resistors of 100 ohms were chosen to broaden the operating bandwidth of the multiplier, but gain was sacrificed. It may be made up with an amplifier operating at the appropriate frequency. (See Figure 31.)

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OPERATION AND APPLICATIONS INFORMATION (continued)

FIGURE 30 — AMPLITUDE MODULATION



The signal is applied to the unit's Y input. Since the total input range is limited to 1.0 volt p-p, a 2.0-volt swing, a current source of 2.0 mA and an R_Y value of 1.0 kilohm is chosen. This takes best advantage of the dynamic range and insures linear operation in the Y-channel.

Since the X input varies between 0 and +1.0 volt, the current source selected was 1.0 mA and the R_X value chosen was 2.0 kilohms. This also insures linear operation over the X input dynamic range.

Choosing $R_L = 100$ assures wide-bandwidth operation. Hence, the scale factor for this configuration is

$$K = \frac{R_L}{R_X R_Y I_3}$$

$$= \frac{100}{(2k)(1k)(2 \times 10^{-3})} V^{-1}$$

$$= \frac{1}{40} V^{-1}$$

The 2 in the numerator of the equation is missing in this scale-factor expression because the output is single-ended and ac coupled.

DUAL TIMING CIRCUIT

The MC3556/MC3456 dual timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor per timer. For astable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor per timer. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200 mA or drive MTTL circuits.

- Direct Replacement for NE555/SE555 Timers
- Timing From Microseconds Through Hours
- Operates in Both Astable and Monostable Modes
- Adjustable Duty Cycle
- High Current Output Can Source or Sink 200 mA
- Output Can Drive MTTL
- Temperature Stability of 0.005% per °C
- Normally "On" or Normally "Off" Output
- Dual Version of the Popular MC1455 Timer

FIGURE 1 — 22-SECOND SOLID-STATE TIME DELAY RELAY CIRCUIT

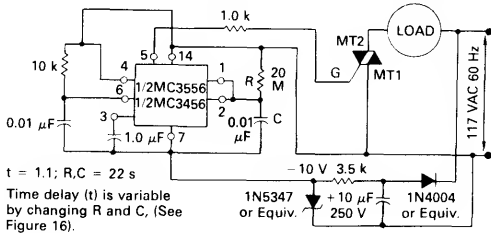
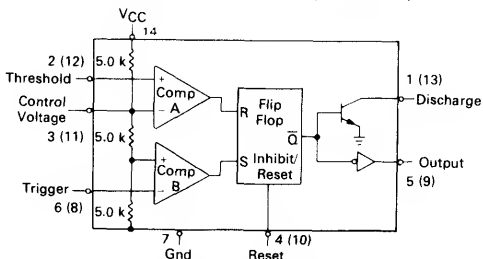


FIGURE 2 — BLOCK DIAGRAM (1/2 SHOWN)



ORDERING INFORMATION

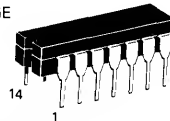
Device	Alternate	Temperature Range	Package
MC3456L MC3456P	— NE556A	0°C to +70°C	Ceramic DIP Plastic DIP
MC3556L	—	–55°C to +125°C	Ceramic DIP
NE556D	—	0°C to +70°C	SO-14

MC3456
MC3556

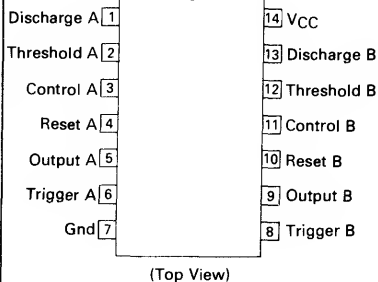
DUAL TIMING CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT

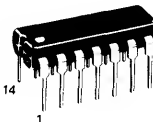
L SUFFIX
CERAMIC PACKAGE
CASE 632



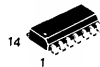
PIN CONNECTIONS



P SUFFIX
PLASTIC PACKAGE
CASE 646



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-14)



TYPICAL APPLICATIONS

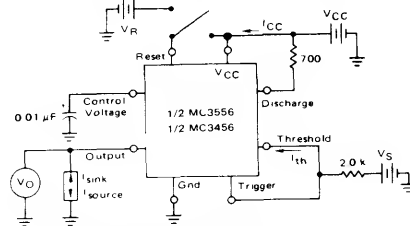
- Time Delay Generation
- Sequential Timing
- Linear Sweep Generation
- Precision Timing
- Pulse Generation
- Pulse Shaping
- Missing Pulse Detection
- Pulse Width Modulation
- Pulse Position Modulation

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MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+18	Vdc
Discharge Current	I_{dis}	200	mA
Power Dissipation (Package Limitation)	P_D		
Ceramic Dual-In-Line Package		1000	mW
Derate above $T_A = +25^\circ\text{C}$		6.6	mW/ $^\circ\text{C}$
Plastic Dual In-Line Package		625	mW
Derate above $T_A = +25^\circ\text{C}$		5.0	mW/ $^\circ\text{C}$
Operating Ambient Temperature Range	T_A	-55 to +125	$^\circ\text{C}$
	MC3556	0 to +70	
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

FIGURE 3 – GENERAL TEST CIRCUIT



Test Circuit for Measuring IIC Parameters (to set output and measure parameters)
a. When $V_S = 2/3 V_{CC}$, V_O is low
b. When $V_S = 1/3 V_{CC}$, V_O is high
c. When V_O is low, pin 7 sinks current. To test for Reset set V_O high, apply Reset voltage and test for current flowing into discharge pin. When Reset is not in use, it should be tied to V_{CC} .

ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$, $V_{CC} = +5.0\text{ V}$ to $+15\text{ V}$ unless otherwise noted.)

Characteristics	Symbol	MC3556			MC3456			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	—	18	4.5	—	16	V
Supply Current	I_{CC}	—	6.0	10	—	6.0	12	mA
$V_{CC} = 5.0\text{ V}$, $R_L = \infty$ $V_{CC} = 15\text{ V}$, $R_L = \infty$ Low State, (Note 1)		—	20	24	—	20	30	
Timing Error (Note 2)								
Monostable Mode								
$R_A = 2.0\text{ k}\Omega$ to $100\text{ k}\Omega$		—	0.5	1.5	—	0.75	—	%
Initial Accuracy $C = 0.1\text{ }\mu\text{F}$		—	30	100	—	50	—	PPM/ $^\circ\text{C}$
Drift with Temperature		—	0.15	0.2	—	0.1	—	%/Volt
Drift with Supply Voltage								
Astable Mode								
$R_A = R_B = 2.0\text{ k}\Omega$ to $100\text{ k}\Omega$		—	1.5	—	—	2.25	—	%
$C = 0.01\text{ }\mu\text{F}$		—	90	—	—	150	—	PPM/ $^\circ\text{C}$
Initial Accuracy		—	15	—	—	0.3	—	%/Volt
Drift with Temperature		—	90	—	—	150	—	
Drift with Supply Voltage		—	0.15	—	—	0.3	—	
Threshold Voltage	V_{th}	—	2/3	—	—	2/3	—	$\times V_{CC}$
Trigger Voltage	V_T	4.8	5.0	5.2	—	5.0	—	V
$V_{CC} = 15\text{ V}$ $V_{CC} = 5.0\text{ V}$		1.45	1.67	1.9	—	1.67	—	
Trigger Current	I_T	—	0.5	—	—	0.5	—	μA
Reset Voltage	V_R	0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current	I_R	—	0.1	—	—	0.1	—	mA
Threshold Current (Note 3)	I_{th}	—	0.03	0.1	—	0.03	0.1	μA
Control Voltage Level	V_{CL}	9.6	10	10.4	9.0	10	11	V
$V_{CC} = 15\text{ V}$ $V_{CC} = 5.0\text{ V}$		2.9	3.33	3.8	2.6	3.33	4.0	
Output Voltage Low	V_{OL}	—	0.1	0.15	—	0.1	0.25	V
$V_{CC} = 15\text{ V}$ $I_{sink} = 10\text{ mA}$ $I_{sink} = 50\text{ mA}$ $I_{sink} = 100\text{ mA}$ $I_{sink} = 200\text{ mA}$ $V_{CC} = 5.0\text{ V}$ $I_{sink} = 8.0\text{ mA}$ $I_{sink} = 5.0\text{ mA}$		—	0.4	0.5	—	0.4	0.75	
		—	2.0	2.25	—	2.0	2.75	
		—	2.5	—	—	2.5	—	
		—	0.1	0.25	—	—	—	
		—	—	—	—	0.25	0.35	
Output Voltage High	V_{OH}	—	12.5	—	—	12.5	—	V
$I_{source} = 200\text{ mA}$ $V_{CC} = 15\text{ V}$ $I_{source} = 100\text{ mA}$ $V_{CC} = 15\text{ V}$ $V_{CC} = 5.0\text{ V}$		13	13.3	—	12.75	13.3	—	
		3.0	3.3	—	2.75	3.3	—	
Toggle Rate (Figures 17, 19)	—	—	100	—	—	100	—	kHz
$R_A = 3.3\text{ k}\Omega$, $R_B = 6.8\text{ k}\Omega$, $C = 0.003\text{ }\mu\text{F}$								
Discharge Leakage Current	I_{dis}	—	20	100	—	20	100	nA
Rise Time of Output	t_{OLH}	—	100	—	—	100	—	ns
Fall Time of Output	t_{OHL}	—	100	—	—	100	—	ns
Matching Characteristics Between Sections (Monostable)								
Initial Timing Accuracy		—	0.5	1.0	—	1.0	2.0	%
Timing Drift with Temperature		—	+10	—	—	+10	—	ppm/ $^\circ\text{C}$
Drift with Supply Voltage		—	0.1	0.2	—	0.2	0.5	%/V

NOTES: 1. Supply current is typically 1.0 mA less for each output which is high.
2. Tested at $V_{CC} = 5.0\text{ V}$ and $V_{CC} = 15\text{ V}$.

3. This will determine the maximum value of $R_A + R_B$ for 15 V operation. The maximum total $R = 20\text{ megohms}$.

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TYPICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 4 – TRIGGER PULSE WIDTH

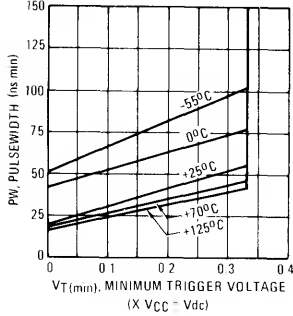


FIGURE 5 – SUPPLY CURRENT

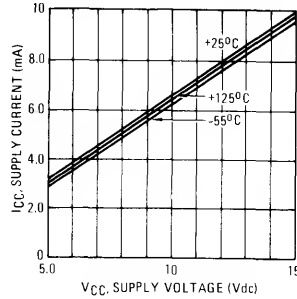


FIGURE 6 – HIGH OUTPUT VOLTAGE

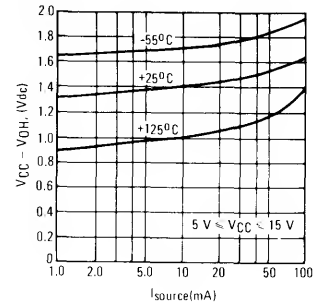


FIGURE 7 – LOW OUTPUT VOLTAGE
@ $V_{CC} = 5.0\text{ Vdc}$

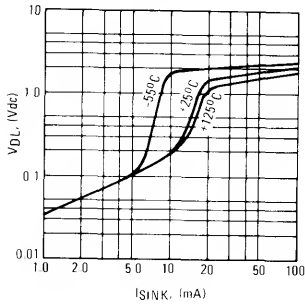


FIGURE 8 – LOW OUTPUT VOLTAGE
@ $V_{CC} = 10\text{ Vdc}$

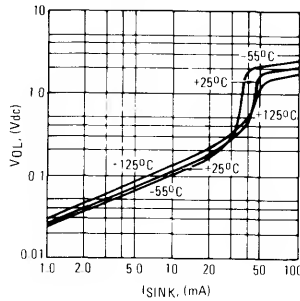


FIGURE 9 – LOW OUTPUT
VOLTAGE @ $V_{CC} = 15\text{ Vdc}$

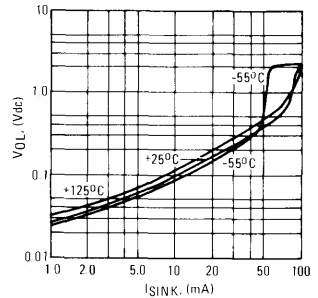


FIGURE 10 – DELAY TIME
versus SUPPLY VOLTAGE

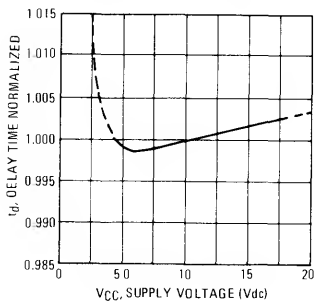


FIGURE 11 – DELAY TIME
versus TEMPERATURE

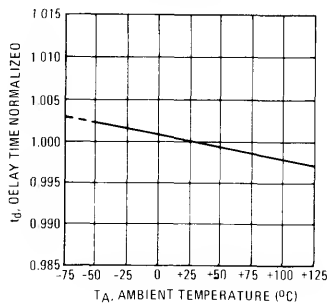
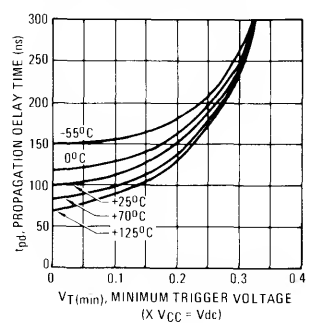
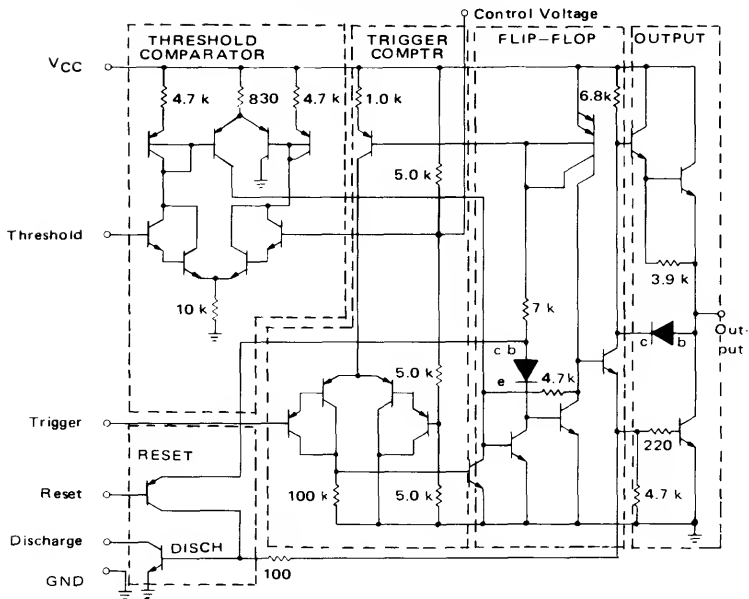


FIGURE 12 – PROPAGATION DELAY
versus TRIGGER VOLTAGE



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FIGURE 13 – 1/2 REPRESENTATIVE
CIRCUIT SCHEMATIC



GENERAL OPERATION

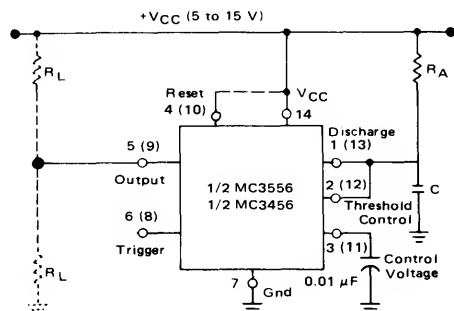
The MC3556 is a dual timing circuit which uses as its timing elements an external resistor – capacitor network. It can be used in both the monostable (one-shot) and astable modes with frequency and duty cycle controlled by the capacitor and resistor values. While the timing is dependent upon the external passive components, the monolithic circuit provides the starting circuit, voltage comparison and other functions needed for a complete timing circuit. Internal to the integrated circuit are two comparators, one for the input signal and the other for capacitor voltage; also a flip-flop and digital output are included. The comparator reference voltages are always a fixed ratio of the supply voltage thus providing output timing independent of supply voltage.

A reset pin is provided to discharge the capacitor thus interrupting the timing cycle. As long as the reset pin is low, the capacitor discharge transistor is turned "on" and prevents the capacitor from charging. While the reset voltage is applied the digital output will remain the same. The reset pin should be tied to the supply voltage when not in use.

FIGURE 14 – MONOSTABLE CIRCUIT

Monostable Mode

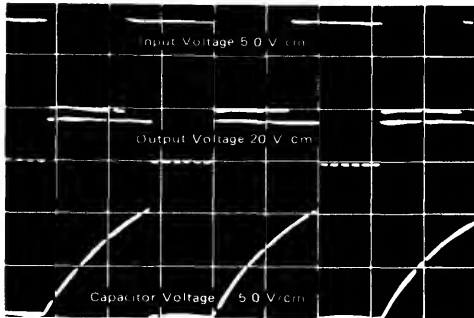
In the monostable mode, a capacitor and a single resistor are used for the timing network. Both the threshold terminal and the discharge transistor terminal are connected together in this mode, refer to circuit Figure 14. When the input voltage to the trigger comparator falls below $1/3 V_{CC}$ the comparator output triggers the flip-flop so that its output sets low. This turns the capacitor discharge transistor "off" and drives the digital output to the high state. This condition allows the capacitor to charge at an exponential rate which is set by the RC time constant. When the capacitor voltage reaches $2/3 V_{CC}$ the threshold comparator resets the flip-flop. This action discharges the timing capacitor and returns the digital output to the low state. Once the flip-flop has been triggered by an input signal, it cannot be retriggered until the present timing period has been completed. The time that the output is high is given by the equation $t = 1.1 R_A C$. Various combinations of R and C and their associated times are shown in Figure 16. The trigger pulse width must be less than the timing period.



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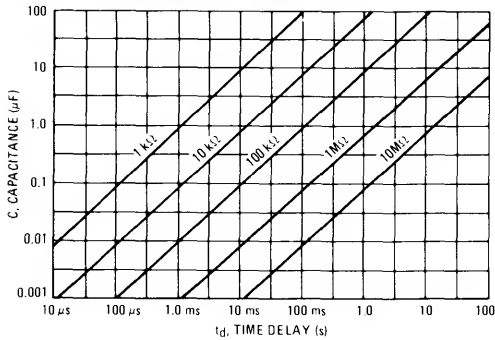
GENERAL OPERATION (continued)

FIGURE 15 — MONOSTABLE WAVEFORMS



$t = 50 \mu\text{s/cm}$
 $(R_A = 10 \text{ k}\Omega, C = 0.01 \mu\text{F}, R_L = 1.0 \text{ k}\Omega, V_{CC} = 15 \text{ V})$

FIGURE 16 — TIME DELAY



Astable Mode

In the astable mode the timer is connected so that it will retrigger itself and cause the capacitor voltage to oscillate between $1/3 V_{CC}$ and $2/3 V_{CC}$. See Figure 17.

The external capacitor charges to $2/3 V_{CC}$ through R_A and R_B and discharges to $1/3 V_{CC}$ through R_B . By varying the ratio of these resistors the duty cycle can be varied. The charge and discharge times are independent of the supply voltage.

The charge time (output high) is given by: $t_1 = 0.695 (R_A + R_B) C$

The discharge time (output low) by: $t_2 = 0.695 (R_B) C$

Thus the total period is given by: $T = t_1 + t_2 = 0.695 (R_A + 2R_B) C$

The frequency of oscillation is then: $f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B) C}$

and may be easily found as shown in Figure 19.

The duty cycle is given by: $DC = \frac{R_B}{R_A + 2R_B}$

To obtain the maximum duty cycle R_A must be as small as possible; but it must also be large enough to limit the discharge current (pin 7 current) within the maximum rating of the discharge transistor (200 mA).

The minimum value of R_A is given by:

$$R_A \geq \frac{V_{CC} (V_{dc})}{I_7 (A)} \geq \frac{V_{CC} (V_{dc})}{0.2}$$

FIGURE 17 — ASTABLE CIRCUIT

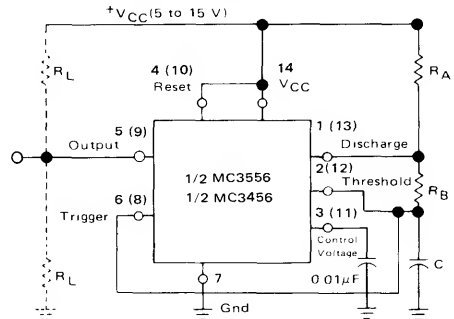
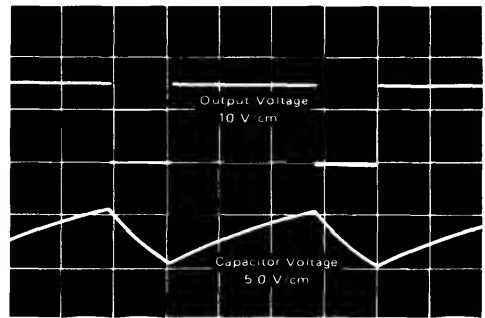
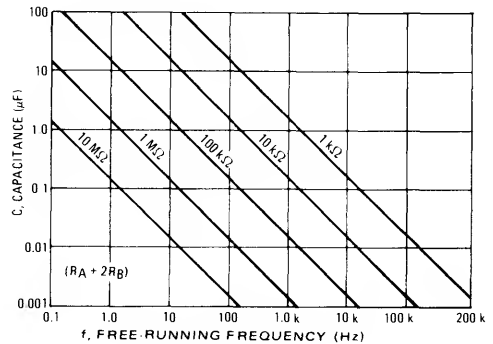


FIGURE 18 — ASTABLE WAVEFORMS



$t = 20 \mu\text{s/cm}$
 $(R_A = 5.1 \text{ k}\Omega, C = 0.01 \mu\text{F}, R_L = 1.0 \text{ k}\Omega;$
 $R_B = 3.9 \text{ k}\Omega, V_{CC} = 15 \text{ V})$

FIGURE 19 — FREE-RUNNING FREQUENCY



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APPLICATIONS INFORMATION

TONE BURST GENERATOR

For a tone burst generator the first timer is used as a monostable and determines the tone duration when triggered by a positive pulse at Pin 6. The second timer is enabled by the high output of the monostable. It is connected as an astable and determines the frequency of the tone.

DUAL ASTABLE MULTIVIBRATOR

This dual astable multivibrator provides versatility not available with single timer circuits. The duty cycle can be adjusted from 5% to 95%. The two outputs provide two phase clock signals often required in digital systems. It can also be inhibited by use of either reset terminal.

FIGURE 20 – TONE BURST GENERATOR

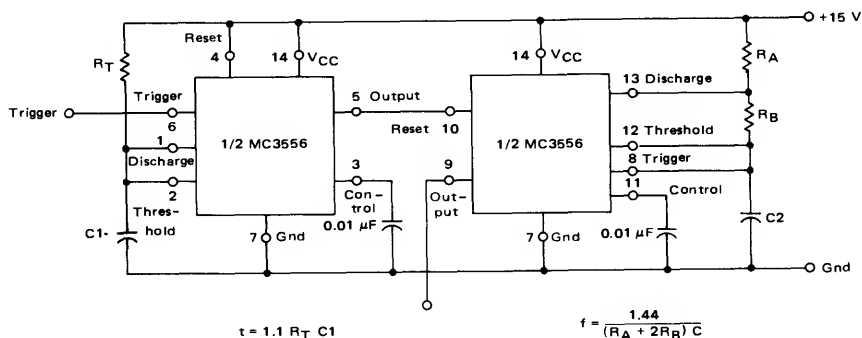
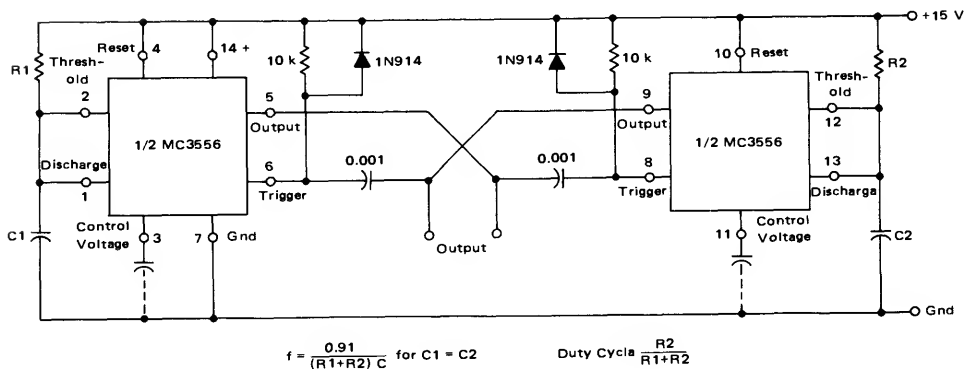


FIGURE 21 – DUAL ASTABLE MULTIVIBRATOR



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APPLICATIONS INFORMATION (continued)

Pulse Width Modulation

If the timer is triggered with a continuous pulse train in the monostable mode of operation, the charge time of the capacitor can be varied by changing the control voltage at pin 3. In this manner, the output pulse width can be modulated by applying a modulating signal that controls the threshold voltage.

FIGURE 22

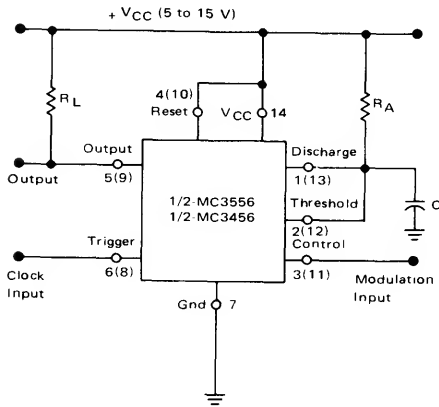
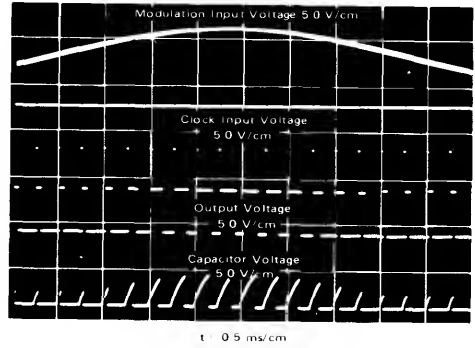


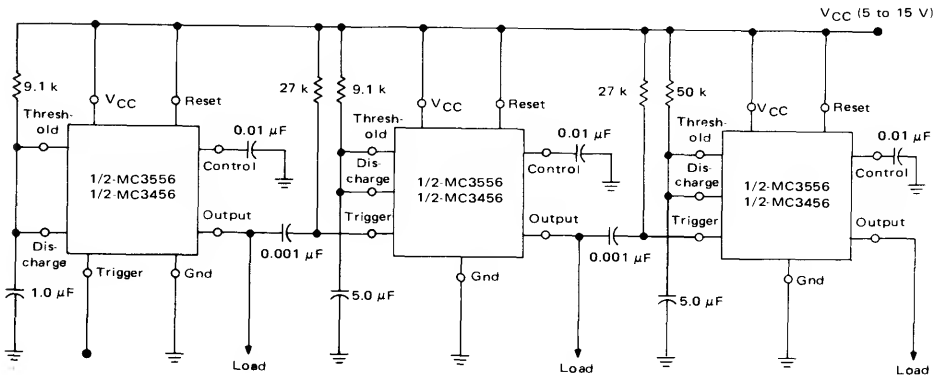
FIGURE 23 — PULSE WIDTH MODULATION WAVEFORMS
($R_A = 10\text{ k}\Omega$, $C = 0.02\text{ }\mu\text{F}$, $V_{CC} = 15\text{ V}$)

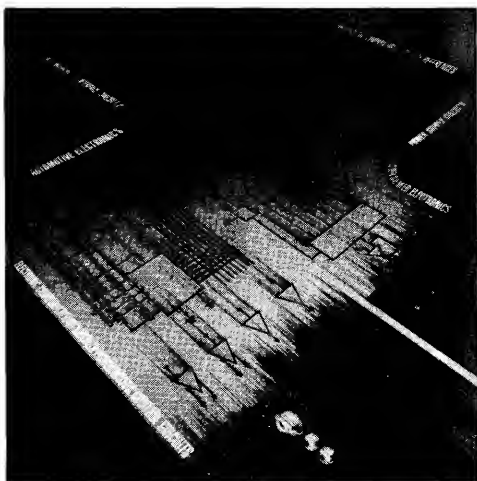


Test Sequences

Several timers can be connected to drive each other for sequential timing. An example is shown in Figure 24 where the sequence is started by triggering the first timer which runs for 10 ms. The output then switches low momentarily and starts the second timer which runs for 50 ms and so forth.

FIGURE 24





In Brief . . .

Surface Mount Technology is now being utilized to offer answers to many problems that have been created in the use of insertion technology.

Limitations have been reached with insertion packages and PC board technology. Surface Mount Technology offers the opportunity to continue to advance the State-of-the-Art designs that cannot be accomplished with Insertion Technology.

Surface Mount Packages allow more optimum device performance with the smaller Surface Mount configuration. Internal lead lengths, parasitic capacitance and inductance that placed limitations on chip performance has been reduced.

The lower profile of Surface Mount Packages allows more boards to be utilized in a given amount of space. They are stacked closer together and utilize less total volume than insertion populated PC boards.

Printed circuit costs are lowered with the reduction of the number of board layers required. The elimination or reduction of the number of plated through holes in the board, contribute significantly to lower PC board prices.

Surface Mount assembly does not require the preparation of components that are common on insertion technology lines. Surface Mount components are sent directly to the assembly line, eliminating an intermediate step.

Automatic placement equipment is available that can place Surface Mount components at the rate of a few thousand per hour to hundreds of thousands of components per hour.

Surface Mount Technology is cost effective, allowing the manufacturer the opportunity to produce smaller units and offer increased functions with the same size product.

Linear and Interface Devices. 12-2

Tape and Reel 12-5

**Surface Mount
Technology**

12

Surface Mount Technology

Linear and Interface

Bipolar

All the major bipolar analog families are now represented in surface mount packaging. Standard SOIC and PLCC packages are augmented by SOP-8 and DPAK for

Linear regulators. In addition, tape and reel shipping to the updated EIA-481A is now on line for the industry's largest array of op-amps, regulators, interface, data conversion, consumer, telecom and automotive Linear ICs.

Device	Function	Package
CA3146D	Transistor Array	SO-14
DAC-08CD,ED	High-Speed 8-Bit Multiplying D-to-A Converter	SO-16
LF351D	Single BIFET Operational Amplifier	SO-8
LF353D	Dual BIFET Operational Amplifiers	SO-8
LF411CD	Single/Dual JFET Operational Amplifier	SO-8
LF412CD	Dual BIFET High Power Operational Amplifiers	SO-8
LF441CD	Single BIFET Low Power Operational Amplifier	SO-8
LF442CD	Dual BIFET Low Power Operational Amplifiers	SO-8
LF444CD	Quad BIFET Low Power Operational Amplifiers	SO-14
LM201AD	General Purpose Adjustable Operational Amplifier	SO-8
LM208D,AD	Precision Operational Amplifier	SO-8
LM211D	High Performance Voltage Comparator	SO-8
LM224D	Quad Low Power Operational Amplifiers	SO-14
LM239D,AD	Quad Single Supply Comparators	SO-14
LM258D	Dual Low Power Operational Amplifiers	SO-8
LM285D-1.2	Micropower Voltage Reference Diodes	SO-8
LM285D-2.5	Micropower Voltage Reference Diodes	SO-8
LM293D	Dual Comparators	SO-8
LM301AD	General Purpose Adjustable Operational Amplifier	SO-8
LM308D,AD	Precision Operational Amplifier	SO-8
LM311D	High Performance Voltage Comparator	SO-8
LM317LD	Positive Adjustable 100 mA Voltage Regulator	SOP-8
LM317MDT	Positive Adjustable 500 mA Voltage Regulator	DPAK
LM324D,AD	Quad Low Power Operational Amplifiers	SO-14
LM339D,AD	Quad Single Supply Comparators	SO-14
LM348D	Quad MC1741 Operational Amplifiers	SO-14
LM358D	Dual Low Power Operational Amplifiers	SO-8
LM385D-1.2	Micropower Voltage Reference Diodes	SO-8
LM385D-2.5	Micropower Voltage Reference Diodes	SO-8
LM393D	Dual Comparators	SO-8
LM833D	Dual Audio Amplifiers	SO-8
LM2901D	Quad Single Supply Comparators	SO-14
LM2902D	Quad Low Power Operational Amplifiers	SO-14
LM2903D	Dual Comparators	SO-8
LM2904D	Dual Low Power Operational Amplifiers	SO-8
LM2931AD-5.0,D-5.0	Low Dropout Voltage Regulator	SOP-8
LM2931CD	Adjustable Low Dropout Voltage Regulator	SOP-8
LM3900D	Quad Single Supply Operational Amplifiers	SO-14
MC1350D	IF Amplifier	SO-8
MC1357D	FM IC with Quadrature Detector	SO-14
MC1377DW*	Color Television RGB to PAL/NTSC Encoder	SO-20L
MC1378FN	Video Overlay Synchronizer	PLCC-44
MC1381FB*	Multimode Monitor Processor	QFP-44
MC1382DW	Multimode Monitor TTL To Analog Video	SO-24L
MC1403D	Precision Low Voltage Reference	SO-8
MC1413D	Peripheral Driver Array	SO-16
MC1436D,CD	High Voltage Operational Amplifier	SO-8
MC1455D	Timing Circuit	SO-8
MC1458D,CD	Dual Operational Amplifiers	SO-8
MC1458SD	High Slew Rate Dual Operational Amplifiers	SO-8
MC1488D	Quad EIA-232C Drivers	SO-14
MC1489D	Quad EIA-232C Receivers	SO-14
MC1495D	Four-Quadrant Multiplier	SO-14
MC1496D	Balanced Modulator-Demodulator	SO-14
MC1723CD	Adjustable Positive Or Negative Voltage Regulator	SO-14

*To Be Introduced.

LINEAR AND INTERFACE (continued)

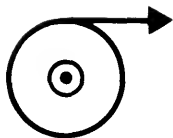
Device	Function	Package
MC1733CD	Differential Video Amplifier	SQ-14
MC1741CD	General Purpose Operational Amplifier	SQ-8
MC1741SCD	High Slew Rate Operational Amplifier	SQ-8
MC1747CD	Dual MC1741 Operational Amplifiers	SO-14
MC1776CD	Programmable Operational Amplifier	SQ-8
MC26LS31D	Quad EIA-422/3 Drivers	SQ-16
MC26LS32D	Quad EIA-422 Receivers	SQ-16
MC26S10D	Quad Bus Transceiver	SQ-16
MC2831AD	FM Transmitter	SQ-16
MC3303D	Quad Differential-Input Operational Amplifier	SQ-14
MC3335DW	Basic Dual Conversion Receiver	SQ-20L
MC3346D	General Purpose Transistor Array	SQ-14
MC3356DW	FSK Receiver	SO-20L
MC3359DW	Low Power Narrowband FM IF Amplifier	SO-20L
MC3361AD	Low Voltage Narrowband FM IF Amplifier	SQ-16
MC3362DW	Dual Conversion Receivers	SQ-28L
MC3363DW*	Dual Conversion Receivers	SO-28L
MC3367DW	Low Voltage VHF Receiver	SQ-28L
MC3371D*	Low Voltage FM Receiver with RSSI	SQ-16
MC3401D	Quad Operational Amplifiers	SO-14
MC3403D	Quad Differential-Input Operational Amplifier	SQ-14
MC3423D	Overvoltage Sensing Circuit	SO-8
MC3448AD	Quad GPIB Transceivers	SO-16
MC3450D	Quad Line Receivers	SO-16
MC3452D	Quad Line Receivers	SO-16
MC3456D	Dual Timing Circuit	SQ-14
MC3458D	Dual Low Power Operational Amplifiers	SO-8
MC3486D	Quad EIA-422/3 Receivers	SO-16
MC3487D	Quad EIA-422 Drivers	SQ-16
MC4558CD	Dual High Frequency Operational Amplifiers	SO-8
MC4741CD	Quad MC1741 Operational Amplifiers	SQ-14
MC78L05ACD	Positive Voltage Regulator, 5 V, 100 mA	SQP-8
MC78L08ACD	Positive Voltage Regulator, 8 V, 100 mA	SQP-8
MC78L12ACD	Positive Voltage Regulator, 12 V, 100 mA	SQP-8
MC78L15ACD	Positive Voltage Regulator, 15 V, 100 mA	SQP-8
MC78M05CDT	Positive Voltage Regulator, 5 V, 500 mA	DPAK
MC78M08CDT	Positive Voltage Regulator, 8 V, 500 mA	DPAK
MC78M12CDT	Positive Voltage Regulator, 12 V, 500 mA	DPAK
MC78M15CDT	Positive Voltage Regulator, 15 V, 500 mA	DPAK
MC79L05ACD	3-Terminal Negative Fixed Voltage Regulator, -5 V, 100 mA	SQP-8
MC79L12ACD	3-Terminal Negative Fixed Voltage Regulator, -12 V, 100 mA	SQP-8
MC79L15ACD	3-Terminal Negative Fixed Voltage Regulator, -15 V, 100 mA	SQP-8
MC79M05CDT	3-Terminal Negative Fixed Voltage Regulator, -5 V, 500 mA	DPAK
MC79M12CDT	3-Terminal Negative Fixed Voltage Regulator, -12 V, 500 mA	DPAK
MC79M15CDT	3-Terminal Negative Fixed Voltage Regulator, -15 V, 500 mA	DPAK
MC10319DW	8-Bit A/D Flash Converter	SQ-28L
MC10321D	7-Bit A/D Flash Converter	SQ-20L
MC13022DW	Medium Voltage AM Stereo C-QUAM Decoder	SQ-28L
MC13023D*	AM Front End/Tuning Stabilizer	SQ-16
MC13024DW	Low Voltage C-QUAM Receiver	SQ-24L
MC13055D	VHF LAN Receiver — FSK	SQ-16L
MC13060D	1 Watt Audio Amp	SQP-8
MC33033DW	Brushless DC Motor Controller	SQ-20L
MC33034DW20,DW60	Brushless DC Motor Controller	SQ-24L
MC33035DW	Brushless DC Motor Controller	SQ-24L
MC33039D	Closed Loop Brushless Motor Adaptor	SQ-8
MC33064D-5	Undervoltage Sensing Circuit	SO-8
MC33065DW	Dual Current Mode PWM Controller	SQ-16L
MC33071D,AD	Single, High Speed Single Supply Operational Amplifiers	SQ-8
MC33072D,AD	Dual, High Speed Single Supply Operational Amplifiers	SQ-8
MC33074D,AD	Quad, High Speed Single Supply Operational Amplifiers	SQ-14
MC33077D	Dual, Low Noise High Frequency Operational Amplifiers	SQ-8
MC33078D	Dual Audio, Low Noise Operational Amplifiers	SQ-8
MC33079D	Low Power, Single Supply Operational Amplifier	SQ-14
MC33120DW*	SLIC II	SQ-20L
MC33164D-5	Micropower Undervoltage Sensing Circuit	SQ-8

*To Be Introduced.

LINEAR AND INTERFACE (continued)

Device	Function	Package
MC33171D	Single, Low Power, Single Supply Operational Amplifier	SO-8
MC33172D	Dual, Low Power, Single Supply Operational Amplifiers	SO-8
MC33174D	Quad, Low Power, Single Supply Operational Amplifiers	SO-14
MC33272D	Dual Precision Bipolar Operational Amplifier	SO-8
MC33274D	Quad Precision Bipolar Operational Amplifier	SO-14
MC33282D	Dual Precision Low Input JFET Operational Amplifiers (Trim-in-the-Package)	SO-8
MC33284D	Quad Precision JFET Operational Amplifiers (Trim-in-the-Package)	SO-14
MC34001D,BD	Single JFET Input Operational Amplifier	SO-8
MC34002D,BD	Dual JFET Input Operational Amplifiers	SO-8
MC34011AFN	Electronic Telephone Circuit	PLCC-44
MC34012-1D	Telephone Tone Ringer	SO-8
MC34012-2D	Telephone Tone Ringer	SO-8
MC34012-3D	Telephone Tone Ringer	SO-8
MC34013AFN	Speech Network and Tone Dialer	PLCC-28
MC34014FN,DW	Telephone Speech Network with Dialer Interface	PLCC-20, SO-20L
MC34017-1D	Telephone Tone Dialer	SO-8
MC34017-2D	Telephone Tone Dialer	SO-8
MC34017-3D	Telephone Tone Dialer	SO-8
MC34018DW	Voice Switched Speakerphone Circuit	SO-28L
MC34050D	EIA-422/23 Transceivers	SO-16
MC34051D	EIA-422/23 Transceivers	SO-16
MC34060AD*	Switchmode Pulse Width Modulation Control Circuit	SO-14
MC34063AD	Precision DC-to-DC Converter Control Circuit	SO-8
MC34064D-5	Undervoltage Sensing Circuit	SO-8
MC34065DW	Dual Current Mode PWM Controller	SO-16L
MC34071D,AD	Single, High Speed, Single Supply Operational Amplifier	SO-8
MC34072D,AD	Dual, High Speed, Single Supply Operational Amplifiers	SO-8
MC34074D,AD	Quad, High Performance, Single Supply Operational Amplifiers	SO-14
MC34080D	High Speed Decompensated ($A_{VCL} \geq 2$) JFET Input Operational Amplifier	SO-8
MC34081D	High Speed JFET Input Operational Amplifier	SO-8
MC34084DW,ADW	Quad High Speed, JFET Operational Amplifier	SO-16L
MC34085DW,ADW	Quad High Speed, JFET Operational Amplifier	SO-16L
MC34114DW	Speech Network II	SO-18L
MC34118DW	Speakerphone II	SO-28L
MC34119D	Telephone Speaker Amplifier	SO-8
MC34129D	Power Supply Controller	SO-14
MC34164D-5	Micropower Undervoltage Sensing Circuit	SO-8
MC34181D	Single, Low Power, High Speed JFET Operational Amplifier	SO-8
MC34182D	Dual, Low Power, High Speed JFET Operational Amplifiers	SO-8
MC34184D	Quad, Low Power, High Speed JFET Operational Amplifiers	SO-14
MC44301DW*	High Performance Video IF	SO-24L
MC44802DW	PLL Tuning Circuit w/1.3 GHz Prescaler	SO-20L
NE556D	Dual Timing Circuit	SO-14
NE592D	Video Amplifier	SO-14
TL061CD	Single BIFET Low Power Operational Amplifier	SO-8
TL064CD	Quad BIFET Low Power Operational Amplifiers	SO-14
TL071CD,ACD	Single, Low Noise JFET Input Operational Amplifier	SO-8
TL072CD,ACD	Dual, Low Noise JFET Input Operational Amplifiers	SO-8
TL081CD,ACD	Single, JFET Input Operational Amplifier	SO-8
TL082CD,ACD	Dual, JFET Input Operational Amplifiers	SO-8
TL431ACD,AID,CD,ID	Programmable Precision Reference	SOP-8
UAA1041D	Automotive Direction Indicator	SO-8
UC2842AD	Off-Line Current Mode PWM Controller	SO-14
UC2843AD	Current Mode PWM Controller	SO-14
UC2844D	Off-Line Current Mode PWM Controller (DC \leq 50%)	SO-14
UC2845D	Current Mode PWM Controller (DC \leq 50%)	SO-14
UC3842AD	Off-Line Current Mode PWM Controller	SO-14
UC3843AD	Current Mode PWM Controller	SO-14
UC3844D	Off-Line Current Mode PWM Controller (DC \leq 50%)	SO-14
UC3845D	Current Mode PWM Controller (DC \leq 50%)	SO-14

*To Be Introduced.



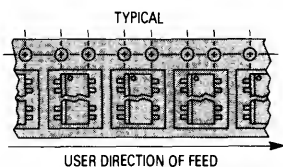
Tape and Reel

Standard Bipolar Logic, Bipolar Analog and MOS Integrated Circuits

Motorola has now added the convenience of Tape and Reel packaging for our growing family of standard Integrated Circuit products. Two reel sizes are available, for all but the largest types, to support the requirements of both first and

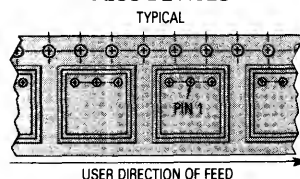
second generation pick-and-place equipment. The packaging fully conforms to the latest EIA-481A specification. The anti-static embossed tape provides a secure cavity, sealed with a peel-back cover tape.

SOIC DEVICES



Mechanical Polarization

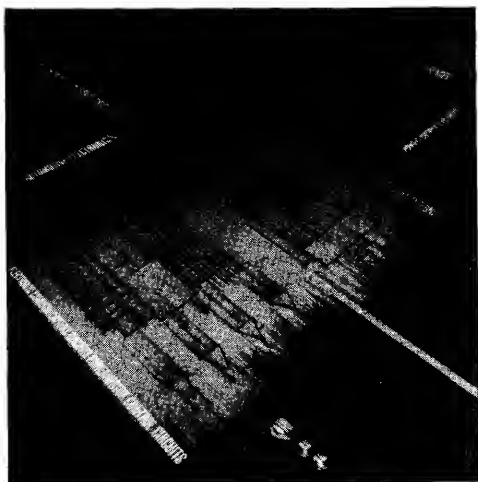
PLCC DEVICES



Package	Tape Width (mm)	Device ¹ per Reel	Reel Size (inch)	Device Suffix
SO-8, SOP-8	12	2,500	13	R2
SO-14	16	2,500	13	R2
SO-16	16	2,500	13	R2
SO-16L WIDE	16	1,000	13	R2
SO-20L WIDE	24	1,000	13	R2
SO-24L WIDE	24	1,000	13	R2
SO-28L WIDE	24	1,000	13	R2
PLCC-20	16	1,000	13	R2
PLCC-28	24	500	13	R2
PLCC-44	32	500	13	R2
PLCC-52	32	500	13	R2
PLCC-68	44	250	13	R2
PLCC-84	44	250	13	R2
TO-226AA (TO-92) ²	18	2000	13	RA, RB RE, RM, or RP (Ammo Pack) only

Notes: 1. Minimum order quantity is 1 reel. Distributors/OEM customers may break lots or reels at their option, however broken reels may not be returned.

2. Integrated Circuits in TO-226AA packages are available in Styles A, B and E only, with optional "Ammono Pack" (Suffix RM or RP). For ordering information please contact your local Motorola Semiconductor Sales Office.



Case Outline Dimensions

The packaging availability for each device type is indicated on the individual data sheets and the Selector Guide. All of the outline dimensions for the packages are given in this section.

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature can be found from the equation:

$$P_{D(TA)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}}$$

where: $P_{D(TA)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section. See individual data sheets for $T_{J(max)}$ information.

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

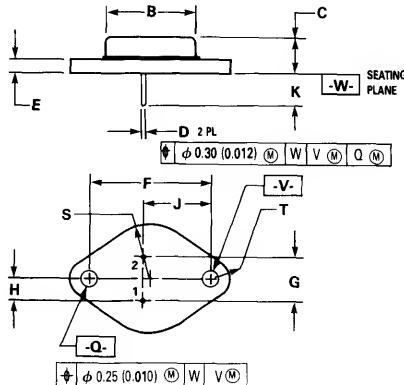
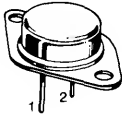
K SUFFIX

CASE 1-03

Metal Package

$R_{\theta JA} = 45^\circ \text{C/W(Typ)}$

(TO-3)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	22.23	—	0.875
B	6.35	11.43	0.250	0.450
C	0.97	1.09	0.038	0.043
D	—	3.43	—	0.135
E	30.15 BSC	—	1.187 BSC	—
F	10.92 BSC	—	0.430 BSC	—
G	5.46 BSC	—	0.215 BSC	—
H	16.89 BSC	—	0.665 BSC	—
J	7.92	—	0.312	—
K	3.84	4.09	0.151	0.161
S	—	13.34	—	0.525
T	—	4.78	—	0.188
V	3.84	4.09	0.151	0.161

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-244A OUTLINE SHALL APPLY.

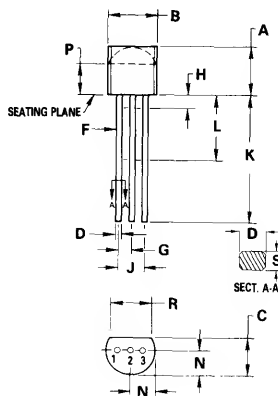
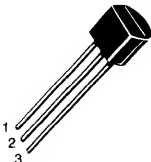
LP, P, Z SUFFIX

CASE 29-04

Plastic Package

$R_{\theta JA} = 200^\circ \text{C/W}$

(TO-226AA/TO-92)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.32	5.33	0.170	0.210
B	4.45	5.20	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.55	0.016	0.022
E	0.41	0.48	0.016	0.019
F	1.15	1.39	0.045	0.055
G	—	2.54	—	0.100
H	2.42	2.66	0.095	0.105
J	12.70	—	0.500	—
K	6.35	—	0.250	—
L	2.04	2.66	0.080	0.105
M	2.93	—	0.115	—
N	3.43	—	0.135	—
P	0.39	0.50	0.015	0.020
Q	—	—	—	—
R	—	—	—	—
S	—	—	—	—

NOTES:

1. CONTOUR OF PACKAGE BEYOND ZONE "P" IS UNCONTROLLED.
2. DIM "F" APPLIES BETWEEN "H" AND "L". DIM "D" & "S" APPLIES BETWEEN "L" & 12.70mm (0.5") FROM SEATING PLANE. LEAD DIM IS UNCONTROLLED IN "H" & BEYOND 12.70mm (0.5") FROM SEATING PLANE.
3. CONTROLLING DIM: INCH.

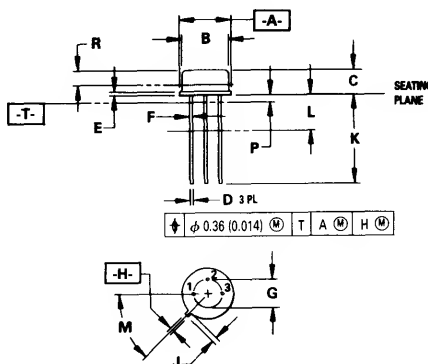
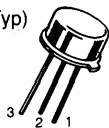
G, H SUFFIX

CASE 79-05

Metal Package

$R_{\theta JA} = 185^{\circ} \text{C/W(Typ)}$

(TO-39)



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION J MEASURED FROM DIMENSION A MAXIMUM.
4. DIMENSION B SHALL NOT VARY MORE THAN 0.25 (0.010) IN ZONE R. THIS ZONE CONTROLLED FOR AUTOMATIC HANDLING.
5. DIMENSION F APPLIES BETWEEN DIMENSION P AND L. DIMENSION D APPLIES BETWEEN DIMENSION L AND K MINIMUM. LEAD DIAMETER IS UNCONTROLLED IN DIMENSION P AND BEYOND DIMENSION K MINIMUM.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.02	9.29	0.355	0.368
B	8.01	8.50	0.315	0.335
C	4.20	4.57	0.165	0.180
D	0.44	0.53	0.017	0.021
E	0.44	0.88	0.017	0.035
F	0.41	0.48	0.016	0.019
G	5.08 BSC		0.200 BSC	
H	0.72	0.86	0.028	0.034
J	0.74	1.01	0.029	0.040
K	12.70	19.05	0.500	0.750
L	6.35	—	0.250	—
M	45° BSC		45° BSC	
P	—	1.27	—	0.050
R	2.54	—	0.100	—

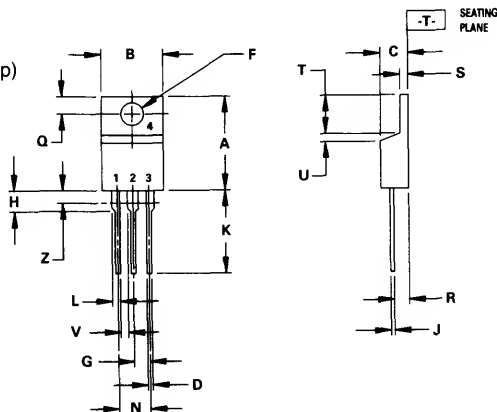
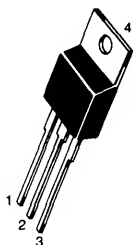
KC, T SUFFIX

CASE 221A-06

Plastic Package

$R_{\theta JA} = 65^{\circ} \text{C/W(Typ)}$

(TO-220AB)



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

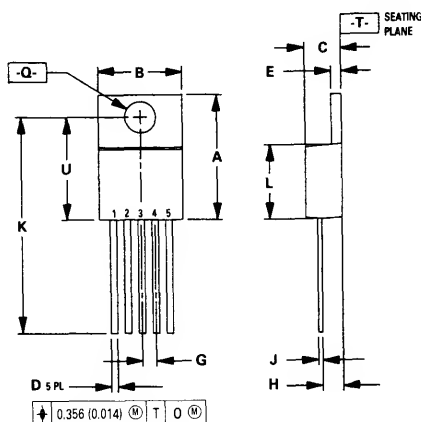
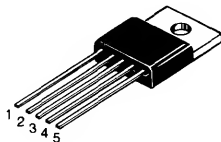
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.64	0.018	0.025
K	12.70	14.27	0.500	0.562
L	1.15	1.52	0.045	0.060
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

T SUFFIX

CASE 314D-02

Plastic Package

$R_{\theta JA} = 65^{\circ} \text{C/W(Typ)}$

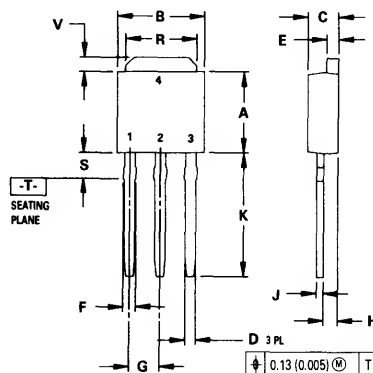
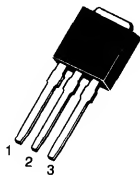


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.529	15.570	0.572	0.613
B	9.906	10.541	0.390	0.415
C	4.318	4.572	0.170	0.180
D	0.635	0.965	0.025	0.038
E	1.169	1.397	0.046	0.055
G	1.702 BSC		0.067 BSC	
H	2.109	2.717	0.083	0.107
J	0.381	0.635	0.015	0.025
K	25.807	26.670	1.016	1.050
L	8.052	9.398	0.317	0.370
Q	3.556	3.937	0.140	0.155
U	11.889	12.827	0.468	0.505

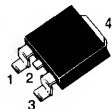
DT-1 SUFFIX
CASE 369-04
 Plastic Package



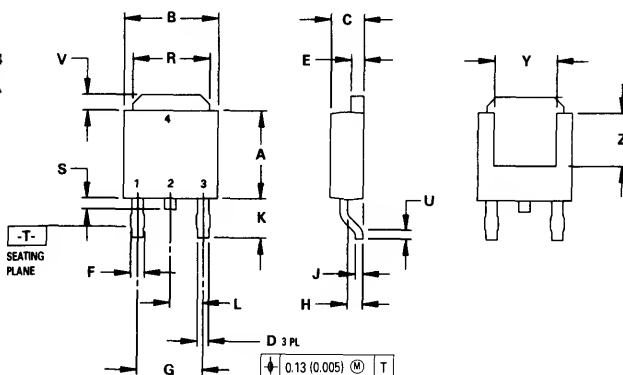
NOTES:
 1. DIMENSIONING AND TOLERANCING
 PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.69	0.88	0.027	0.035
E	0.84	1.01	0.033	0.040
F	0.77	1.14	0.030	0.045
G	2.29 BSC		0.090 BSC	
H	0.87	1.01	0.034	0.040
J	0.46	0.58	0.018	0.023
K	8.89	9.65	0.350	0.380
L	4.45	5.46	0.175	0.215
M	1.91	2.28	0.075	0.090
N	0.77	1.27	0.030	0.050

DT SUFFIX
CASE 369A-05
 Plastic Package
 DPAK

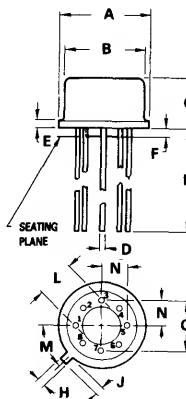
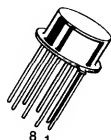


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.69	0.88	0.027	0.035
E	0.84	1.01	0.033	0.040
F	0.77	1.14	0.030	0.045
G	4.58 BSC		0.180 BSC	
H	0.87	1.01	0.034	0.040
J	0.46	0.58	0.018	0.023
K	2.60	2.89	0.102	0.114
L	2.29 BSC		0.090 BSC	
M	4.45	5.46	0.175	0.215
N	0.64	0.88	0.025	0.035
P	0.51	—	0.020	—
Q	0.77	1.27	0.030	0.050
R	4.32	—	0.170	—
S	3.69	—	0.145	—



NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI
 Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

H, G SUFFIX
CASE 601-04
 Metal Package
 $R_{\theta JA} = 160^{\circ} \text{C/W(Typ)}$
 (TO-5)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.51	9.40	0.335	0.370
B	7.75	8.51	0.305	0.335
C	4.19	4.70	0.165	0.185
D	0.41	0.48	0.016	0.019
E	0.25	1.02	0.010	0.040
F	0.25	1.02	0.010	0.040
G	5.08 BSC		0.200 BSC	
H	0.71	0.86	0.028	0.034
J	0.74	1.14	0.029	0.045
K	12.70	—	0.500	—
L	3.05	4.06	0.120	0.160
M	45° BSC		45° BSC	
N	2.41	2.67	0.095	0.105

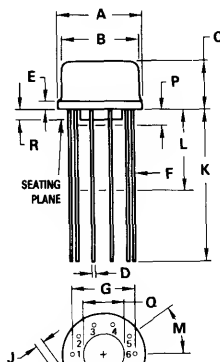
NOTE:
 1. LEADS WITHIN 0.25 mm (0.010)
 DIA OF TRUE POSITION AT
 SEATING PLANE AT MAXIMUM
 MATERIAL CONDITION.

H, G SUFFIX

CASE 603-04

Metal Can

$R_{\theta JA} = 160^{\circ} \text{ C/W}$
(TO-100)



(BOTTOM VIEW)

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.51	9.39	0.335	0.370
B	7.75	8.51	0.305	0.335
C	4.19	4.70	0.165	0.185
D	0.407	0.533	0.016	0.021
E	—	1.02	—	0.040
F	0.406	0.483	0.016	0.019
G	5.84 BSC		0.230 BSC	
H	0.712	0.864	0.028	0.034
J	0.737	1.14	0.029	0.045
K	12.70	—	0.500	—
L	6.35	12.70	0.250	0.500
M	36° BSC		36° BSC	
P	—	1.27	—	0.050
Q	3.56	4.06	0.140	0.160
R	0.254	1.02	0.010	0.040

All JEDEC Dimensions and Notes Apply.

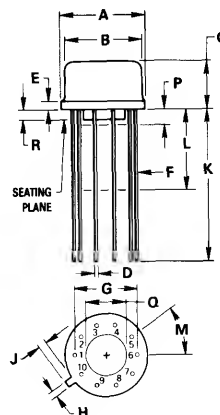
NOTE:
LEADS WITHIN 0.18 mm (0.007) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.

G SUFFIX

CASE 603C-01

Metal Can

$R_{\theta JA} = 150^{\circ} \text{ C/W(Typ)}$
(TO-100)



(BOTTOM VIEW)

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.51	9.39	0.335	0.370
B	7.75	8.51	0.305	0.335
C	4.19	6.73	0.165	0.265
D	0.407	0.533	0.016	0.021
E	—	1.02	—	0.040
F	0.406	0.483	0.016	0.019
G	5.84 BSC		0.230 BSC	
H	0.712	0.864	0.028	0.034
J	0.737	1.14	0.029	0.045
K	12.70	—	0.500	—
L	6.35	12.70	0.250	0.500
M	36° BSC		36° BSC	
P	—	1.27	—	0.050
Q	3.56	4.06	0.140	0.160
R	0.254	1.02	0.010	0.040

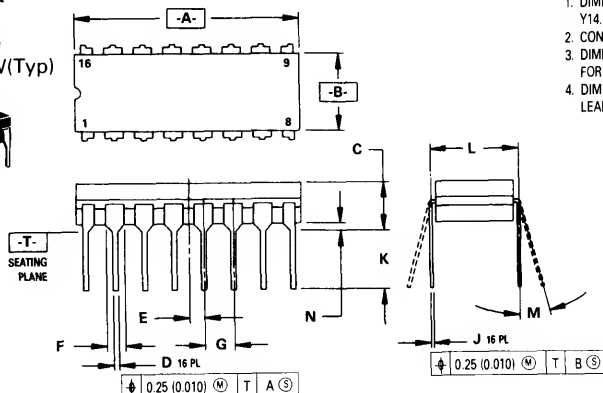
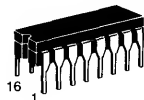
NOTES:
1. LEADS WITHIN 0.18 mm (0.007) RADIUS OF TRUE POSITION TO DIM. "A" & "H" AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. LEAD DIA UNCONTROLLED BEYOND DIM "K" MIN.

D, J, L, N SUFFIX

CASE 620-10

Ceramic Package

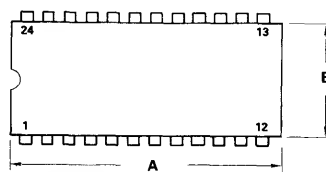
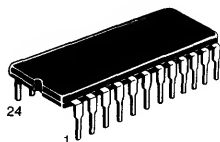
$R_{\theta JA} = 100^{\circ} \text{ C/W(Typ)}$



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.93	0.750	0.785
B	6.10	7.49	0.240	0.295
C	—	5.08	—	0.200
D	0.39	0.50	0.015	0.020
E	1.27 BSC		0.050 BSC	
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	3.18	4.31	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

L SUFFIX
CASE 623-05
 Ceramic Package
 $R\theta JA = 53^\circ \text{ C/W(Typ)}$

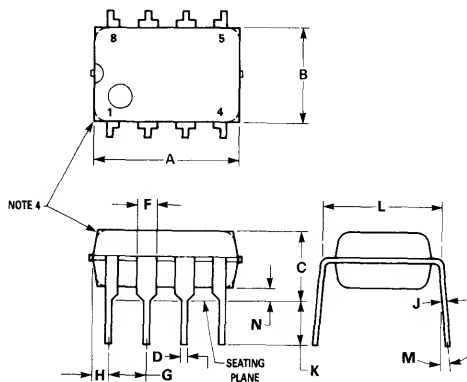
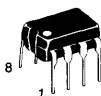


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.610
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

NOTES:

- DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL).

DP1, N, P, P1 SUFFIX
CASE 626-05
 Plastic Package
 $R\theta JA = 100^\circ \text{ C/W(Typ)}$

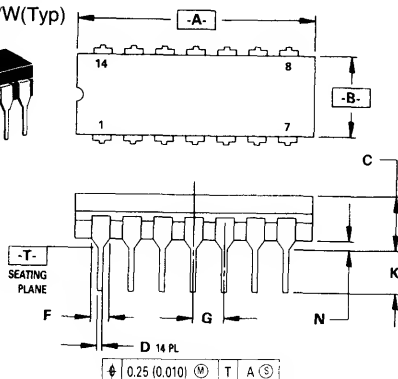
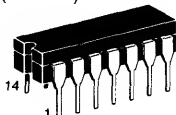


NOTES:

- LEAD POSITIONAL TOLERANCE:
 $\phi 0.13 (0.005) \text{ T A } \textcircled{B}$
- DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
- PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
- DIMENSIONS A AND B ARE DATUMS.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	—	10°	—	10°
N	0.76	1.01	0.030	0.040

J, F, L SUFFIX
CASE 632-08
 Ceramic Package
 $R\theta JA = 100^\circ \text{ C/W(Typ)}$
 (TO-116)

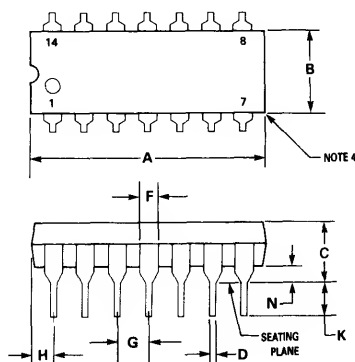
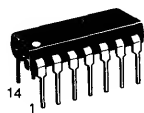


NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
- DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.23	7.11	0.245	0.280
C	3.94	5.08	0.155	0.200
D	0.39	0.50	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	3.18	4.31	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

N, P, N-14, P2 SUFFIX
CASE 646-06
 Plastic Package
 $R_{\theta JA} = 100^{\circ} \text{ C/W (Typ)}$

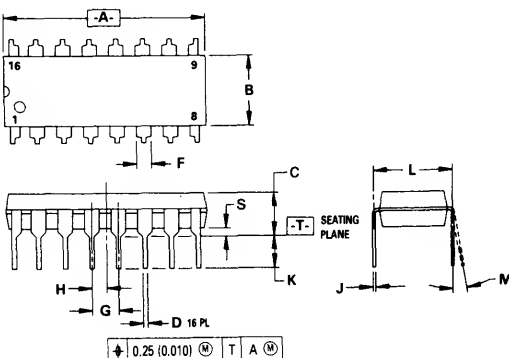
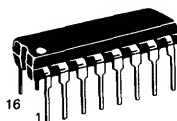


NOTES:

- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
- ROUNDED CORNERS OPTIONAL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.39	1.01	0.015	0.039

DP2, N, P SUFFIX
CASE 648-08
 Plastic Package
 $R_{\theta JA} = 67^{\circ} \text{ C/W (Typ)}$

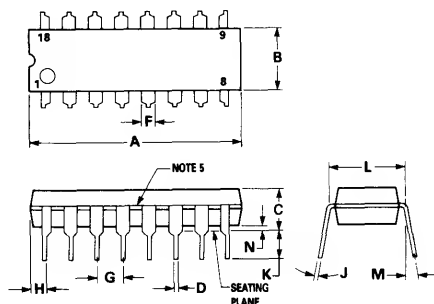
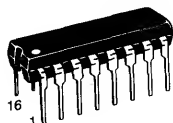


NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
- ROUNDED CORNERS OPTIONAL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	19.56	0.740	0.770
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.39	0.53	0.015	0.021
F	1.02	1.77	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.27 BSC		0.050 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.30	0.110	0.130
L	7.50	7.74	0.295	0.305
M	0°	10°	0°	10°
S	0.51	1.01	0.020	0.040

P SUFFIX
CASE 648C-02
 Plastic Package
 $R_{\theta JA} = 52^{\circ} \text{ C/W}$

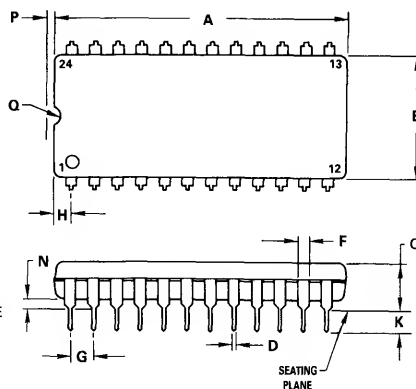
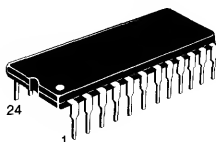


NOTES:

- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
- ROUNDED CORNERS OPTIONAL.
- INTERNAL LEAD CONNECTION, BETWEEN 4 AND 5, 12 AND 13.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	21.34	0.740	0.840
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.38	2.41	0.015	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.39	1.01	0.015	0.040

P SUFFIX
CASE 649-03
 Plastic Package
 $R_{\theta JA} = 90^{\circ} \text{ C/W(Typ)}$

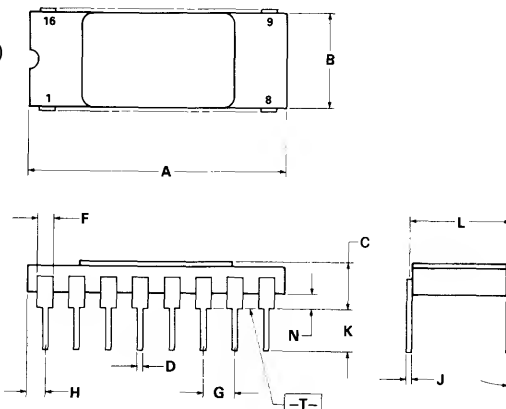
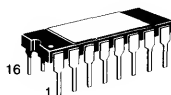


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.50	32.13	1.240	1.265
B	13.21	13.72	0.520	0.540
C	4.70	5.21	0.185	0.205
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54	8SC	0.100	8SC
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	14.99	15.49	0.590	0.610
M	—	10°	—	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

NOTES:

- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

L SUFFIX
CASE 690-13
 Ceramic Package
 $R_{\theta JA} = 100^{\circ} \text{ C/W(Typ)}$

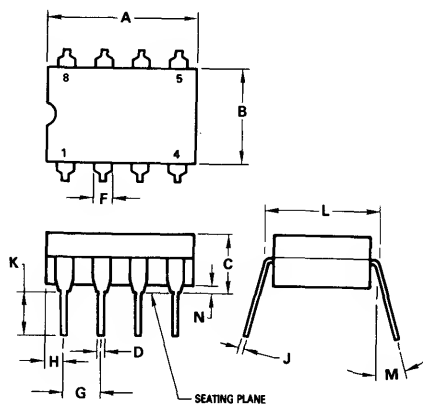


NOTES:

- A- AND -B- ARE DATUMS.
- T- IS SEATING PLANE
- POSITIONAL TOLERANCE FOR LEADS (D).
 $\phi 0.25 (0.010) \text{ M} \text{ T A } \text{M} \text{ B } \text{M}$
- DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.07	20.57	0.790	0.810
B	7.11	7.74	0.280	0.305
C	2.67	4.19	0.105	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.52	0.030	0.060
G	2.54	8SC	0.100	8SC
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	3.18	5.08	0.125	0.200
L	7.62	8SC	0.300	8SC
M	—	10°	—	10°
N	0.38	1.52	0.015	0.060

J-8, J, JG, U, Z SUFFIX
CASE 693-02
 Ceramic Package
 $R_{\theta JA} = 100^{\circ} \text{ C/W(Typ)}$

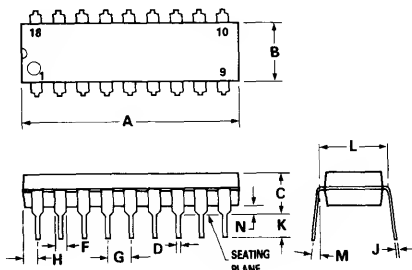
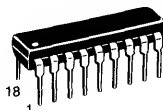


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.91	10.92	0.390	0.430
B	6.22	6.99	0.245	0.275
C	4.32	5.08	0.170	0.200
D	0.41	0.51	0.016	0.020
F	1.40	1.65	0.055	0.065
G	2.54	8SC	0.100	8SC
H	1.14	1.65	0.045	0.065
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.37	7.87	0.290	0.310
M	—	15°	—	15°
N	0.51	1.02	0.020	0.040

NOTES:

- LEADS WITHIN 0.13 mm (0.005) RAD OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

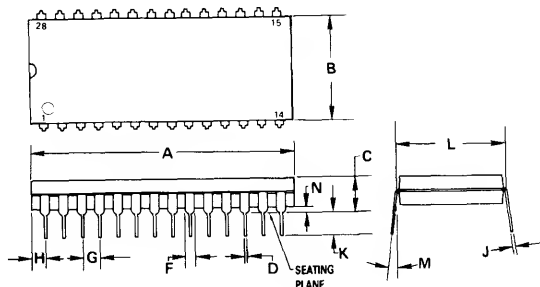
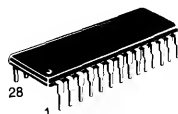
A, B, N, P SUFFIX
CASE 707-02
 Plastic Package
 $R_{\theta JA} = 100^{\circ} \text{ C/W(Typ)}$



- NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
 2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

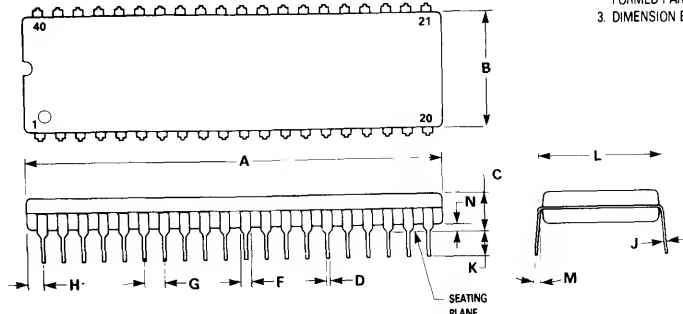
P SUFFIX
CASE 710-02
 Plastic Package



- NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
 2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

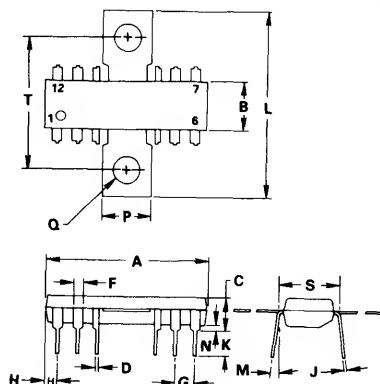
P SUFFIX
CASE 711-03
 Plastic Package



- NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
 2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

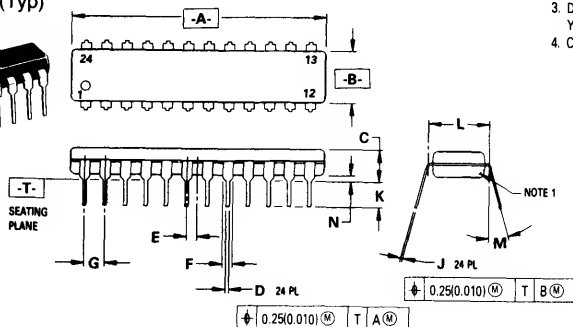
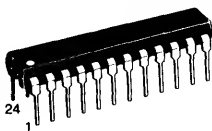
CASE 721-02
Plastic Package
 $R\theta_{JA} = 52^\circ \text{ C/W}$



- NOTES:
1. DIMENSION "S" TO CENTER OF LEADS WHEN FORMED PARALLEL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.70	21.34	0.815	0.840
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.43	0.56	0.017	0.022
F	1.02	1.52	0.040	0.060
G	2.41	2.67	0.095	0.105
H	1.32	1.83	0.052	0.072
J	0.33	0.46	0.013	0.018
K	3.30	3.94	0.130	0.155
L	25.15	27.94	0.990	1.100
M	—	10°	—	10°
N	0.51	1.02	0.020	0.040
P	6.27	6.53	0.247	0.257
Q	3.48	3.73	0.137	0.147
S	7.37	7.87	0.290	0.310
T	16.26	16.76	0.640	0.660

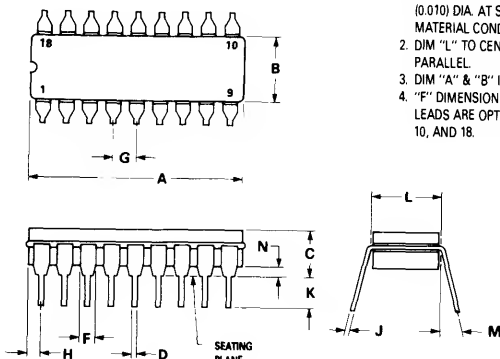
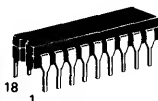
P-3, P-60, P-120 SUFFIX
CASE 724-03
Plastic Package
 $R\theta_{JA} = 100^\circ \text{ C/W(Typ)}$



- NOTES:
1. CHAMFERED CONTOUR OPTIONAL.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.25	32.13	1.230	1.265
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.38	0.51	0.015	0.020
E	1.27 BSC		0.050 BSC	
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
J	0.18	0.30	0.007	0.012
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

J, L SUFFIX
CASE 726-04
Ceramic Package
 $R\theta_{JA} = 100^\circ \text{ C/W(Typ)}$



- NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA. AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM "A" & "B" INCLUDES MENISCUS.
4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 9, 10, AND 18.

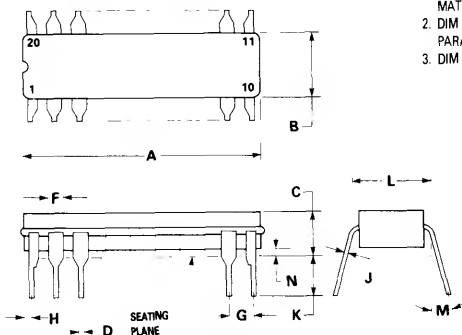
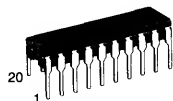
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.35	23.11	0.880	0.910
B	6.10	7.49	0.240	0.295
C	—	5.08	—	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.32	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

L SUFFIX

CASE 732-03

Ceramic Package

$R_{\theta JA} = 75^{\circ} \text{ C/W}$



NOTES

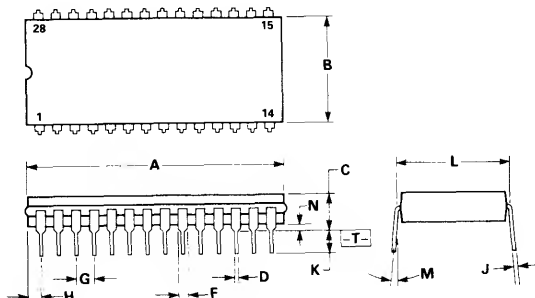
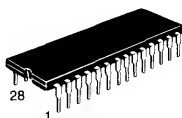
- LEADS WITHIN 0.25 mm (0.010) DIA., TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
- DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIM A AND B INCLUDES MENISCUS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	23.88	25.15	0.940	0.990
B	6.60	7.49	0.260	0.295
C	3.81	5.08	0.150	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC 0.100 BSC			
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC 0.300 BSC			
M	0°	15°	0°	15°
N	0.25	1.02	0.010	0.040

L SUFFIX

CASE 733-04

Ceramic Package



NOTES

- DIM [A] IS DATUM.
- POSITIONAL TOL FOR LEADS:
 $\phi 0.25 (0.010) \text{ (M) T A (M)}$
- [T] IS SEATING PLANE.
- DIM A AND B INCLUDES MENISCUS.
- DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIMENSIONING & TOLERANCING PER Y14.5, 1982.
- CONTROLLING DIM: INCH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	36.45	37.84	1.435	1.490
B	12.70	15.36	0.500	0.605
C	4.06	5.84	0.160	0.230
D	0.38	0.55	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54 BSC 0.100 BSC			
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC 0.600 BSC			
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

P SUFFIX

CASE 738-03

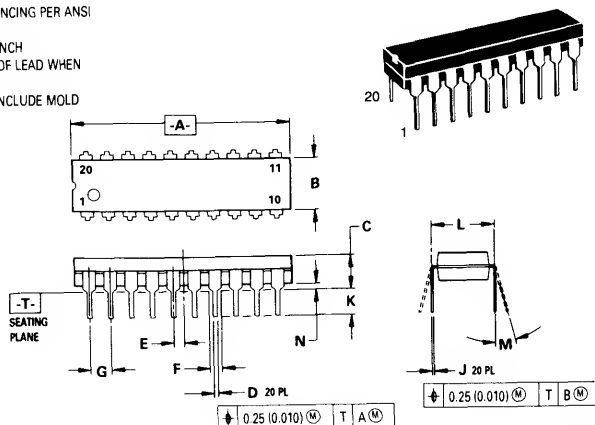
Plastic Package

$R_{\theta JA} = 75^{\circ} \text{ C/W}$

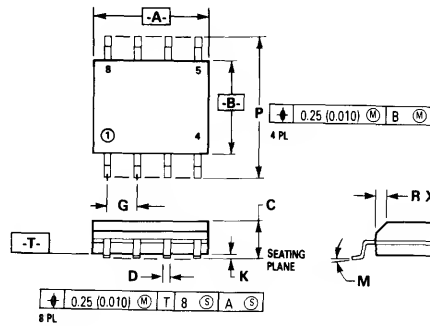
NOTES

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH
- DIMENSION "L" TO CENTER OF LEAD WHEN FORMED PARALLEL.
- DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	25.66	27.17	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.81	4.57	0.150	0.180
D	0.39	0.55	0.015	0.022
E	1.27 BSC 0.050 BSC			
F	1.27	1.77	0.050	0.070
G	2.54 BSC 0.100 BSC			
J	0.21	0.38	0.008	0.015
K	2.80	3.55	0.110	0.140
L	7.62 BSC 0.300 BSC			
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040



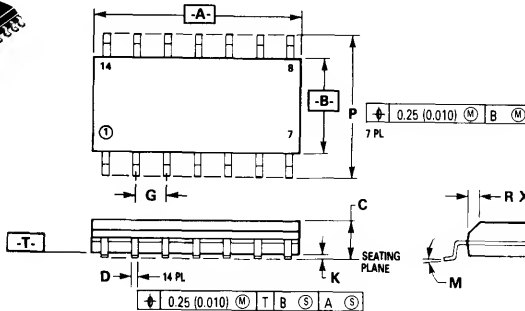
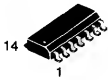
D SUFFIX
CASE 751-03
 Plastic Package
 (SO-8, SOP-8)



- NOTES:
1. DIMENSIONS "A" AND "B" ARE DATUMS AND "T" IS A DATUM SURFACE.
 2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 3. CONTROLLING DIM: MILLIMETER.
 4. DIMENSION "A" AND "B" DO NOT INCLUDE MOLD PROTRUSION.
 5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.18	0.25	0.007	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

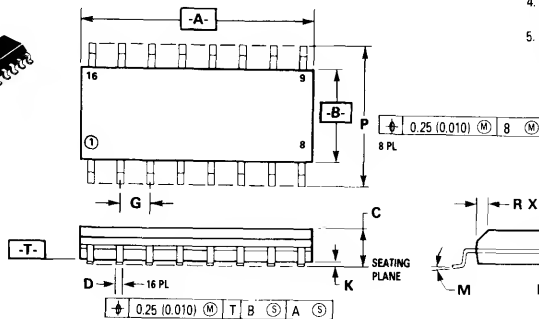
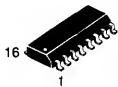
D SUFFIX
CASE 751A-02
 Plastic Package
 (SO-14)



- NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
 2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 3. CONTROLLING DIMENSION: MILLIMETER.
 4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

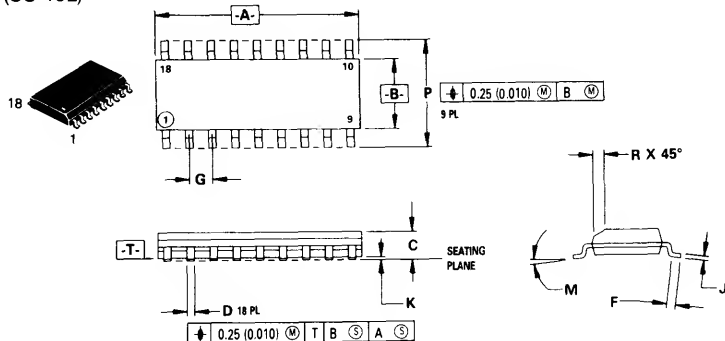
D SUFFIX
CASE 751B-03
 Plastic Package
 (SO-16)



- NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
 2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 3. CONTROLLING DIMENSION: MILLIMETER.
 4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

**DW SUFFIX
CASE 751C-03**
Plastic Package
(SO-18L)

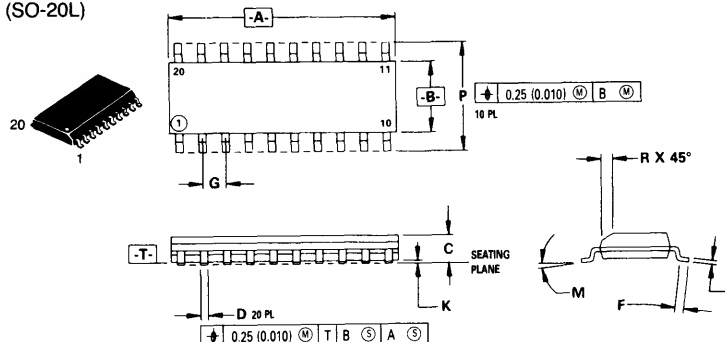


NOTES:

1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	11.40	11.70	0.449	0.460
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

**DW SUFFIX
CASE 751D-03**
Plastic Package
(SO-20L)

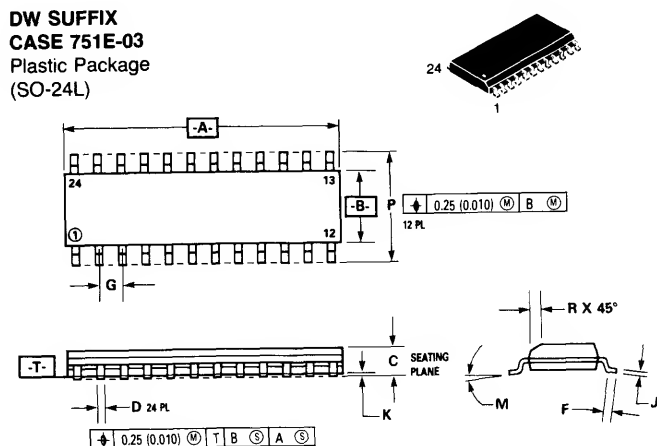


NOTES:

1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

**DW SUFFIX
CASE 751E-03**
Plastic Package
(SO-24L)

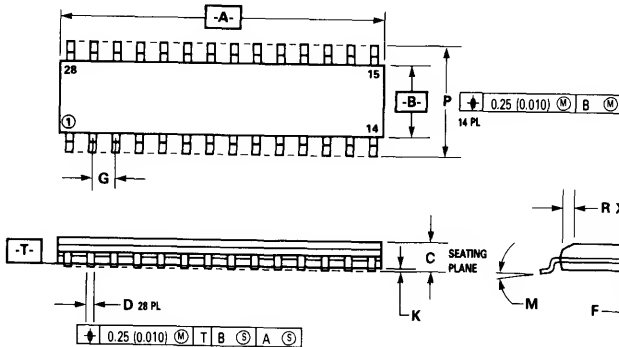
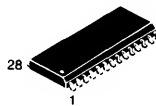


NOTES:

1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.229	0.317	0.0090	0.0125
K	0.127	0.292	0.0050	0.0115
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

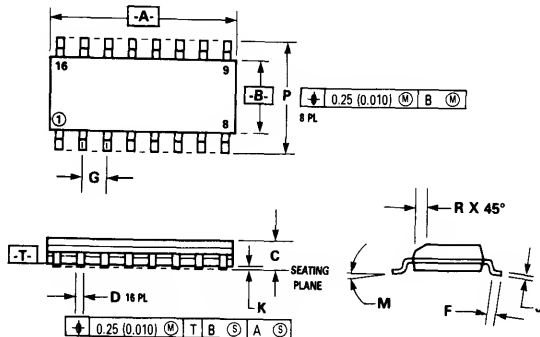
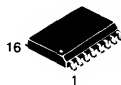
DW SUFFIX
CASE 751F-03
 Plastic Package
 (SO-28L)



- NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
 2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 3. CONTROLLING DIMENSION: MILLIMETER.
 4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.80	18.05	0.701	0.711
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27	BSC	0.050	BSC
J	0.229	0.317	0.0090	0.0125
K	0.127	0.292	0.0050	0.0115
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

DW SUFFIX
CASE 751G-01
 Plastic Package
 (SO-16L)



- NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
 2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 3. CONTROLLING DIMENSION: MILLIMETER.
 4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27	BSC	0.050	BSC
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

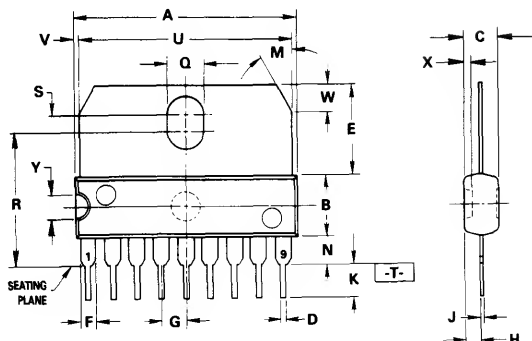
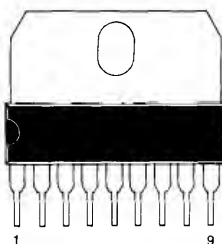
CASE 762-01

Plastic Medium Power Package

(SIP 9)

$R_{\theta JA} = 70^{\circ} \text{ C/W(Typ)}$

$R_{\theta JC} = 15^{\circ} \text{ C/W(Typ)}$



NOTES:

- DIMENSIONS A, AND C ARE DATUMS.
AND -T- IS A DATUM PLANE
- POSITIONAL TOLERANCE FOR
LEAD DIMENSION D:
 $\pm 0.25 (0.010) \text{ (M) } -T, A \text{ (M)}$
- POSITIONAL TOLERANCE FOR
LEAD DIMENSION J:
 $\pm 0.25 (0.010) \text{ (M) } -T, C \text{ (M)}$
- POSITIONAL TOLERANCE FOR LEAD
DIMENSION Q:
 $\pm 0.25 (0.010) \text{ (M) } -T, A \text{ (M)}$
- DIMENSIONING AND TOLERANCING PER ANSI
Y14.5, 1982.
- CONTROLLING DIMENSION: MILLIMETER.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.40	23.00	0.873	0.897
B	6.40	6.60	0.252	0.260
C	3.45	3.65	0.135	0.143
D	0.40	0.55	0.015	0.021
E	9.35	9.60	0.368	0.377
F	1.40	1.60	0.055	0.062
G	2.54 BSC		0.100 BSC	
H	1.51	1.71	0.059	0.067
J	0.360	0.400	0.014	0.015
K	3.95	4.20	0.155	0.165
M	30° BSC		30° BSC	
N	2.50	2.70	0.099	0.106
Q	3.15	3.45	0.124	0.135
R	13.60	13.90	0.535	0.547
S	1.65	1.95	0.064	0.076
U	22.00	22.20	0.866	0.874
V	0.55	0.75	0.021	0.029
W	2.89 BSC		0.113 BSC	
X	0.65	0.75	0.025	0.029
Y	2.70	2.80	0.106	0.110

FN SUFFIX

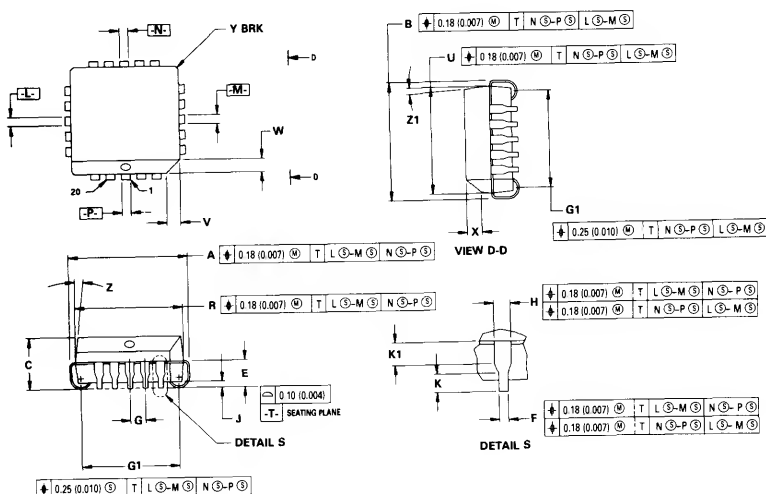
CASE 775-02

Plastic Package

(PLCC-20)

$R_{\theta JA} = 72^{\circ} \text{ C/W(Typ)}$

(5K SQML)



NOTES:

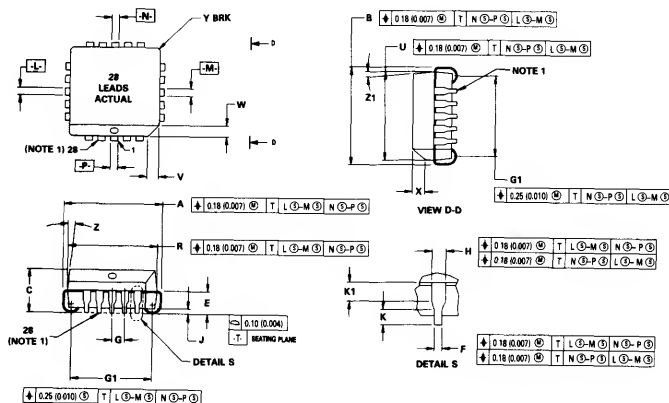
- DATUMS -L-, -M-, -N-, AND -P- DETERMINED
WHERE TOP OF LEAD SHOULDER EXIT PLASTIC
BODY AT MOLD PARTING LINE.
- DIM G1, TRUE POSITION TO BE MEASURED AT
DATUM -T-, SEATING PLANE.
- DIM R AND U DO NOT INCLUDE MOLD
PROTRUSION. ALLOWABLE MOLD PROTRUSION
IS 0.25 (0.010) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI
Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.78	10.03	0.385	0.395
B	9.78	10.03	0.385	0.395
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	—	0.020	—
K	0.84	—	0.025	—
R	8.89	9.04	0.350	0.356
U	8.89	9.04	0.350	0.356
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	—	0.50	—	0.020
Z	2°	10°	2°	10°
G1	7.88	8.38	0.310	0.330
K1	1.02	—	0.040	—
Z1	2°	10°	2°	10°

FN SUFFIX CASE 776-02

Plastic Package
(PLCC-28)

$R_{\theta JA} = 66^{\circ} \text{ C/W(Typ)}$
(5K SQML)



NOTES

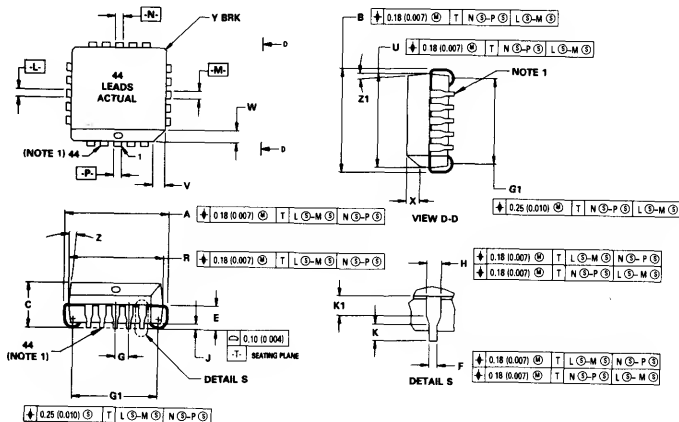
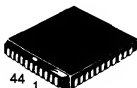
1. DUE TO SPACE LIMITATION, CASE 776-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 28 LEADS.
2. DATUMS L, M, N, AND P DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
3. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM T, SEATING PLANE.
4. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.32	12.57	0.485	0.495
B	12.32	12.57	0.485	0.495
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	—	0.020	—
K	0.64	—	0.025	—
R	11.43	11.58	0.450	0.456
U	11.43	11.58	0.450	0.456
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	—	0.50	—	0.020
Z	2"	10"	2"	10"
G1	10.42	10.92	0.410	0.430
K1	1.02	—	0.040	—
Z1	2"	10"	2"	10"

FN SUFFIX CASE 777-02

Plastic Package
(PLCC-44)

$R_{\theta JA} = 55^{\circ} \text{ C/W(Typ)}$
(10K SQML)



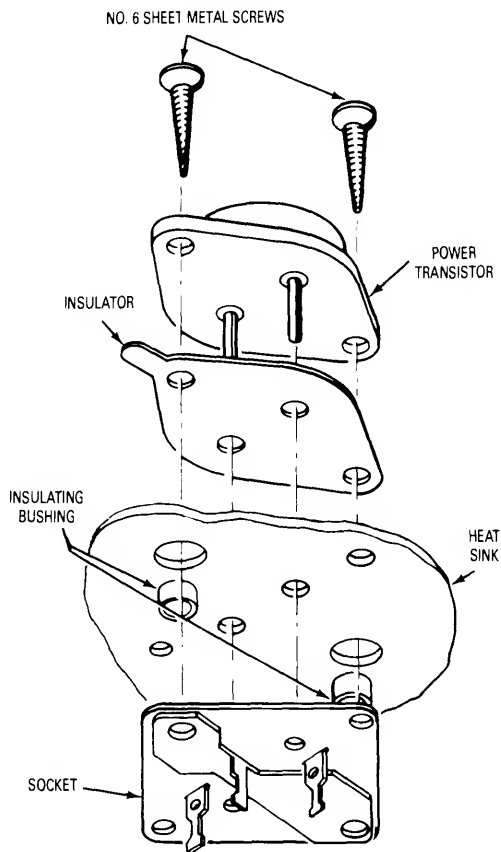
NOTES

1. DUE TO SPACE LIMITATION, CASE 777-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 44 LEADS.
2. DATUMS L, M, N, AND P DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
3. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM T, SEATING PLANE.
4. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	17.40	17.65	0.685	0.695
B	17.40	17.65	0.685	0.695
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	—	0.020	—
K	0.64	—	0.025	—
R	16.51	16.66	0.650	0.656
U	16.51	16.66	0.650	0.656
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	—	0.50	—	0.020
Z	2"	10"	2"	10"
G1	15.50	16.00	0.610	0.630
K1	1.02	—	0.040	—
Z1	2"	10"	2"	10"

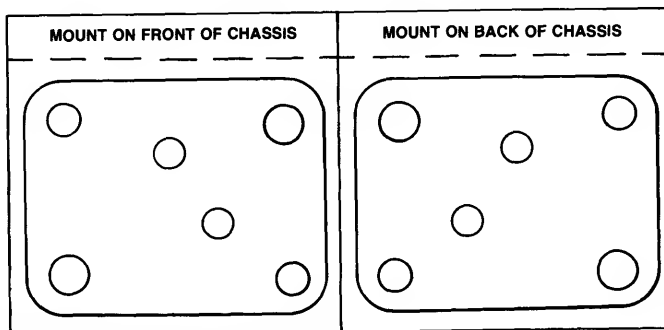
Mounting Arrangement For Flange Mount TO-204AA

Hardware Used for a TO-204AA (TO-3)
Flange Mount Part



DRAWINGS NOT
TO SCALE

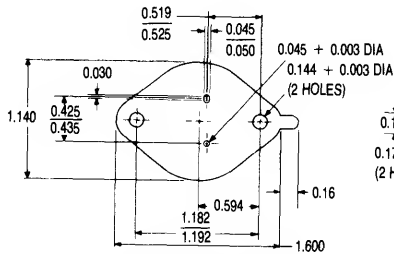
FRONT TEMPLATE



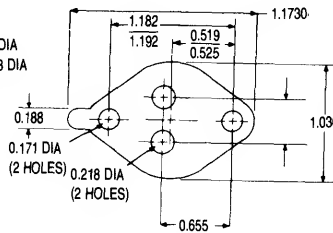
BACK TEMPLATE

For further information, please refer to Application Note AN1040.

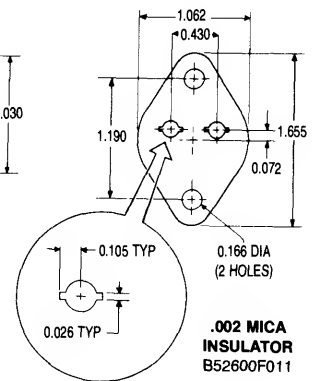
MOUNTING ARRANGEMENT FOR FLANGE MOUNT TO-204AA



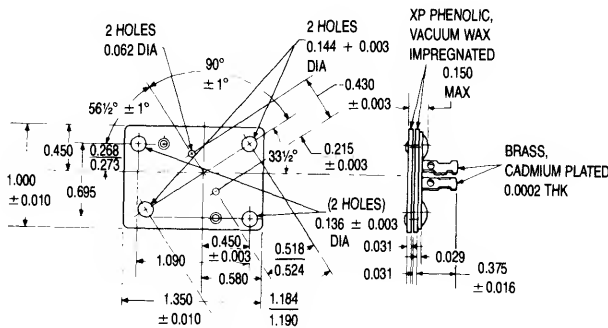
**0.003 TEFLON-COATED
FIBERGLASS INSULATOR**
B51080A001



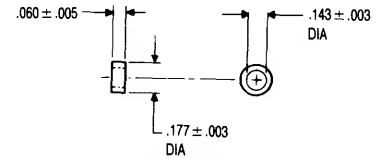
**.020 ALUMINUM
INSULATOR**
B51078A001



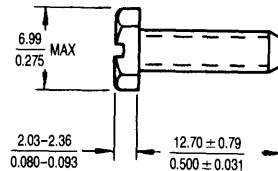
**.002 MICA
INSULATOR**
B52600F011



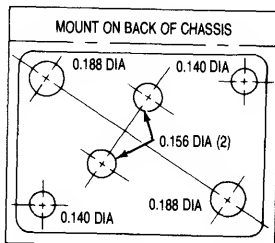
TRANSISTOR SOCKET
B51084A001



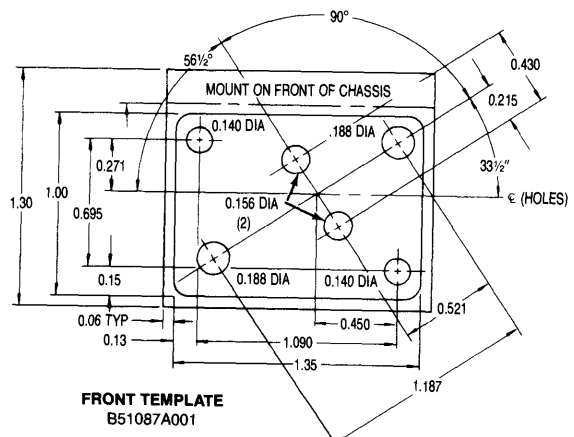
NYLON INSULATING BUSHING
B51547F002



NO. 6 SHEET METAL SCREW
B51564F003



BACK TEMPLATE
B51087A002



FRONT TEMPLATE
B51087A001

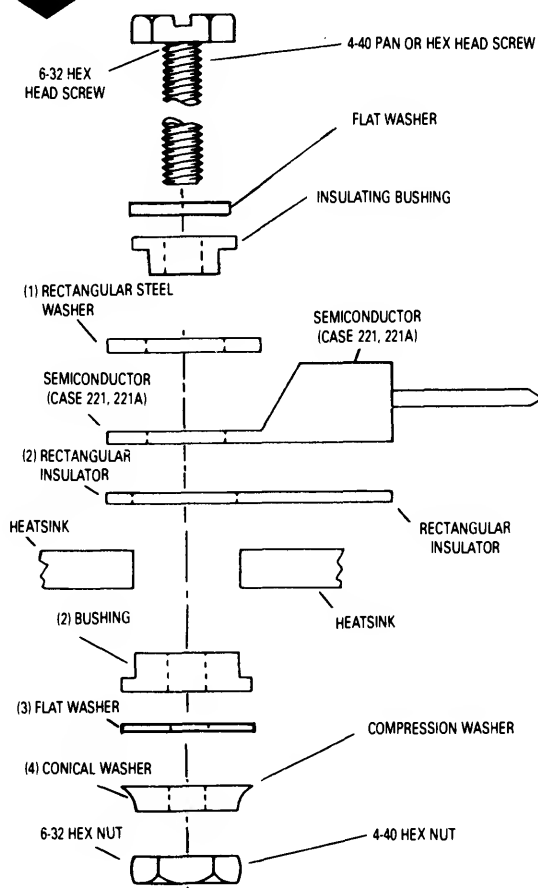
Mounting Arrangements For Tab Mount TO-220

a) Preferred Arrangement for Isolated or Non-isolated Mounting. Screw is at Semiconductor Case Potential. 6-32 Hardware is Used.

Choose from Parts Listed Below.

b) Alternate Arrangement for Isolated Mounting when Screw must be at Heatsink Potential. 4-40 Hardware is Used.

Use Parts Listed Below.

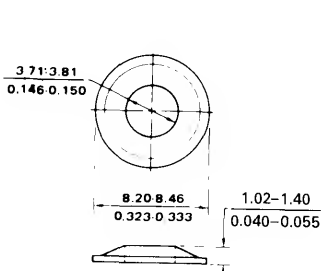


- (1) Used with thin chassis and/or large hole.
- (2) Used when isolation is required.
- (3) Required when nylon bushing is used.

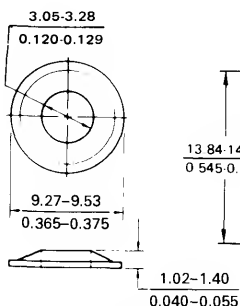
For further information, please refer to Application Note AN1040.

MOUNTING ARRANGEMENTS FOR TAB MOUNT TO-220

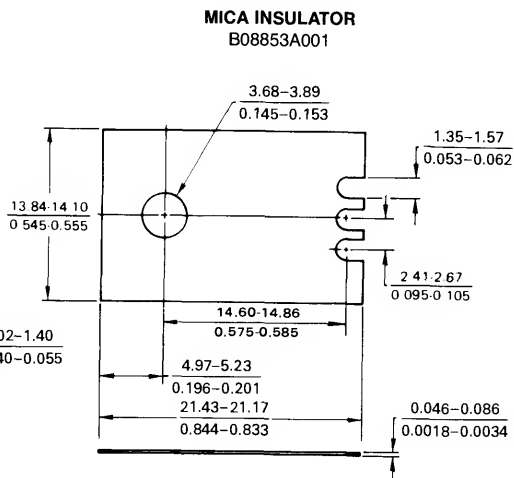
(DIMENSION — $\frac{\text{MILLIMETER}}{\text{INCH}}$)



**STEEL COMPRESSION
WASHER**
B52200F004

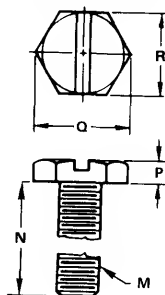


**STEEL COMPRESSION
WASHER**
B52200F005

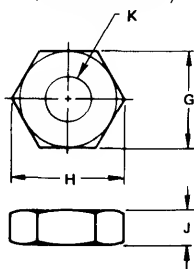


MICA INSULATOR
B08853A001

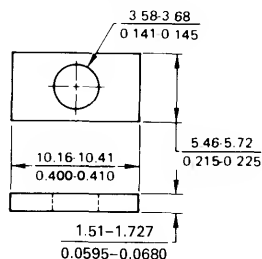
HEX HEAD SCREW
CARBON STEEL
CADMIUM-PLATED
(See table below.)



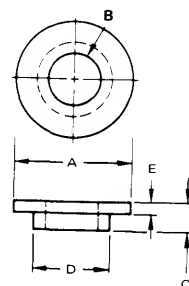
HEX NUT
CARBON STEEL
CADMIUM-PLATED
(See table below.)



**RECTANGULAR
STEEL WASHER**
B09002A001



**NYLON
INSULATING BUSHING**
(See table below.)



DIMENSIONS — MILLIMETER (INCH)

NYLON BUSHING

PART NO.	DIM A	DIM B	DIM C	DIM D	DIM E
851547F005	9.40-9.65 (0.370-0.380)	3.84-4.09 (0.151-0.161)	2.16-2.41 (0.085-0.095)	6.10-6.35 (0.240-0.250)	1.02-1.27 (0.040-0.050)
851547F019	5.59-6.10 (0.220-0.240)	3.05-3.15 (0.120-0.124)	1.73-1.91 (0.068-0.075)	3.61-3.68 (0.142-0.145)	0.51-0.64 (0.020-0.025)

HEX NUT

TYPE	PART NO.	DIM G	DIM H	DIM J	DIM K
4-40	B09490A005	6.12-6.35 (0.241-0.250)	6.98-7.34 (0.275-0.289)	2.21-2.49 (0.087-0.098)	2.84 NOM (0.112 NOM)
6-32	B09490A006	7.67-7.92 (0.302-0.312)	8.74-9.17 (0.344-0.361)	2.59-2.90 (0.102-0.114)	3.50 NOM (0.138 NOM)

HEX HEAD SCREW

TYPE	PART NO.	DIM M	DIM N	DIM P	DIM Q	DIM R
4-40	B09489A034	0.112-40	1.57 (0.62)	1.24-1.52 (0.049-0.060)	5.13 MIN (0.202 MIN)	4.60-4.75 (0.181-0.187)
6.32	B09489A035	0.138-32	1.57 (0.62)	2.03-2.36 (0.080-0.093)	6.91 MIN (0.272 MIN)	6.20-6.35 (0.244-0.250)

SOIC MINIATURE IC PLASTIC PACKAGE

Thermal Information

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P(DT_A) = \frac{T_{J(max)} - T_A}{R_{\theta JA} (Typ)}$$

Where: $P_D(T_A)$ = power dissipation allowable at a given operating ambient temperature.

$T_{J(max)}$ = Maximum operating junction temperature as listed in the maximum ratings section

T_A = Desired operating ambient temperature

$R_{\theta JA}(Typ)$ = Typical thermal resistance junction to ambient

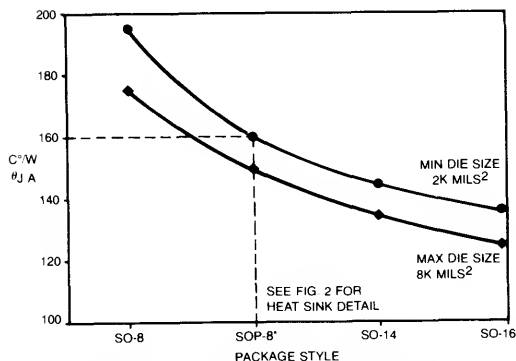
Maximum Ratings

Rating	Symbol	Value	Unit
Operating Ambient Temperature Range	T_A	0 to +70 -40 to +85	°C °C
Operating Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

THERMAL RESISTANCE OF SOIC PACKAGES

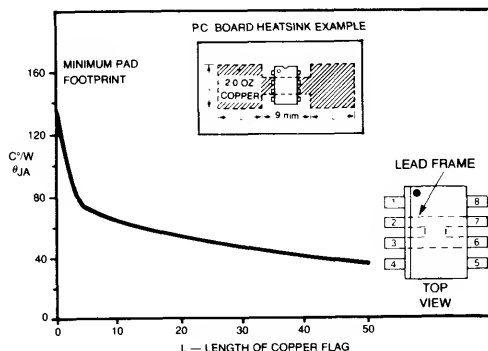
Measurement specimens are solder mounted on a Philips SO test board #7322-078, 80873 in still air. No auxiliary thermal conduction aids are used. As thermal resistance varies inversely with die area, a given package takes thermal resistance values between the max and min curves shown. These curves represent the smallest (2000 square mils) and largest (8000 square mils) die areas expected to be assembled in the SOIC package.

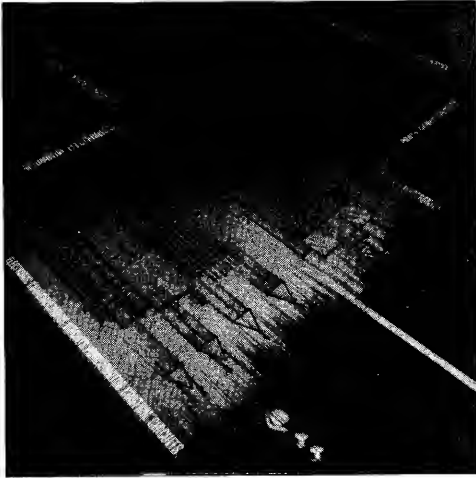
Figure 1. Thermal Resistance, Junction-to-Ambient (°C/W)



DATA TAKEN USING PHILIPS SO TEST BOARD #7322-078, 80873
*SOP-8 USING STANDARD SO-8 FOOTPRINT — MIN PAD SIZE

Figure 2. Thermal Resistance for SOP-8 Package Die 2K mils²





Quality and Reliability Assurance

Quality Concepts

The word **Quality** has been used to describe many things, such as fitness for use, customer satisfaction, customer enthusiasm, what the customer says quality is, etc. These descriptions convey important truths, however quality should be described in a way that precipitates immediate action. With that in mind **quality** can be described as **reduction of variability around a target, so that conformance to customer requirements/expectations can be achieved in a cost effective way**. This definition provides direction and potential for immediate action for a person desiring to improve quality. **Quality Improvement** for a task or a process can be quickly described in terms of the target, current status with respect to target (variability), reduction of variability (commitment to never ending improvement), customer requirements (who receives output, what are person's requirements/expectations) and economics (cost of nonconformance; loss function, etc.).

The definition of quality as described above can be applied to a task, process or a whole company. If we are to reap the benefits of quality and obtain a competitive advantage, quality must be applied to the whole company.

Application of quality to the whole company has come to be known by such names as "**Total Quality Control**" (TQC); "**Company Wide Quality Control**" (CWQC); "**Total Quality Excellence**" (TQE); "**Total Quality Involvement**" (TQI). These names attempt to convey the idea that quality is a process (a way of acting continuously) rather than a program (implying a beginning and an end). Nevertheless for this process to be successful it must be able to show measurable results.

Implementation of quality ideas, company, wide requires a quality plan showing: A philosophy (belief) of operation, measurable goals, training of individuals and methods of communicating this philosophy of operation to the whole organization.

Motorola, for example, believes that **quality** and **reliability** are the **responsibility of every person**. **Participative Management Program (PMP)** is the process by which problem solving and quality improvement are facilitated at all levels of the organization. **Continuous improvement** for the individual is facilitated by a broad educational program covering on-site, university and college courses. The **Motorola Training and Education Center (MTEC)** provides leadership and administers this educational effort on a company wide basis.

Another key belief is that **quality excellence** is accomplished by **people doing things right the first time and committed to never ending improvement**. The **Six Sigma (6 σ)** challenge is designed to convey and facilitate the idea of continuous improvement at all levels.

"**Six Sigma** is the required capability level to approach the standard. The **standard** is **zero defects**. Our goal is to be **Best-In-Class** in product, sales and service." (For a more detailed explanation, contact your Motorola Representative for a pamphlet of the Six Sigma Challenge.)

Quick insight into Six Sigma is obtained if we realize that a Six Sigma process has variability which is one half of the variation allowed (tolerance; spread) by the customer requirements (i.e. natural variation is one half of the customer spec-

ification range for a given characteristic). When Six Sigma is achieved, virtually zero defects are observed in the output of a process/product even allowing for potential process shifts (Figure 1).

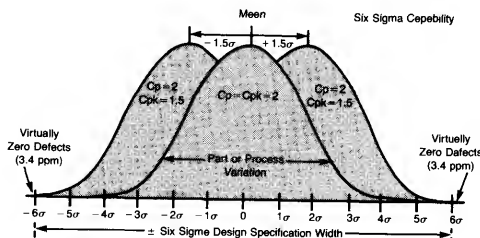


FIGURE 1 — A SIX SIGMA PROCESS HAS VIRTUALLY ZERO DEFECTS ALLOWING FOR 1.5 σ SHIFT

Policies, **objectives** and **five year plans** are the mechanisms for communicating the key beliefs and measurable goals to all personnel and continuously keeping them in focus. This is done at the corporate, sector, group, division, and department levels.

The Analog Division, for example, evaluates performance to the corporate goals of **10 Fold Improvement by 1989; 100 Fold Improvement by 1991** and achievement of **Six Sigma capability by 1992** by utilizing indices such as Outgoing Electrical and Visual Mechanical Quality (AOQ) in terms of PPM (parts per million or sometimes given in 'parts per billion'); **% of devices with zero PPB; product quality returns (RMR)**; number of processes/products with specified **capability indices (cp; cpk)**; **Six Sigma capability roadmaps; failure rates for various reliability tests** (operating life, temperature humidity bias, hast, temperature cycling, etc.); **on time delivery; customer product evaluation and failure analysis turnaround; cost of nonconformance; productivity improvement and personnel development**.

Figure 2 shows the improvement in electrical outgoing quality for bipolar analog products over recent years in a normalized form.

Documentation control is an important part of statistical process control. Process flow charting with documentation identified allows visualization and therefore optimization of the process. Figure 4 shows a portion of a flow chart for Wafer Fabrication. Control plans are an important part of Statistical Process Control, these plans identify in detail critical points where data for process control is taken, parameters measured, frequency of measurements, type of control device used, measuring equipment, responsibilities and reaction plans. Figure 5 shows a portion of a control plan for wafer fabrication. These flow charts and control plans exist for all product flows.

Six Sigma progress is tracked by roadmaps. A portion of a roadmap is shown for example on Figure 6.

On Time Delivery is of great importance, with the current emphasis on just-in-time systems. Tracking is done on an overall basis, and at the device level.

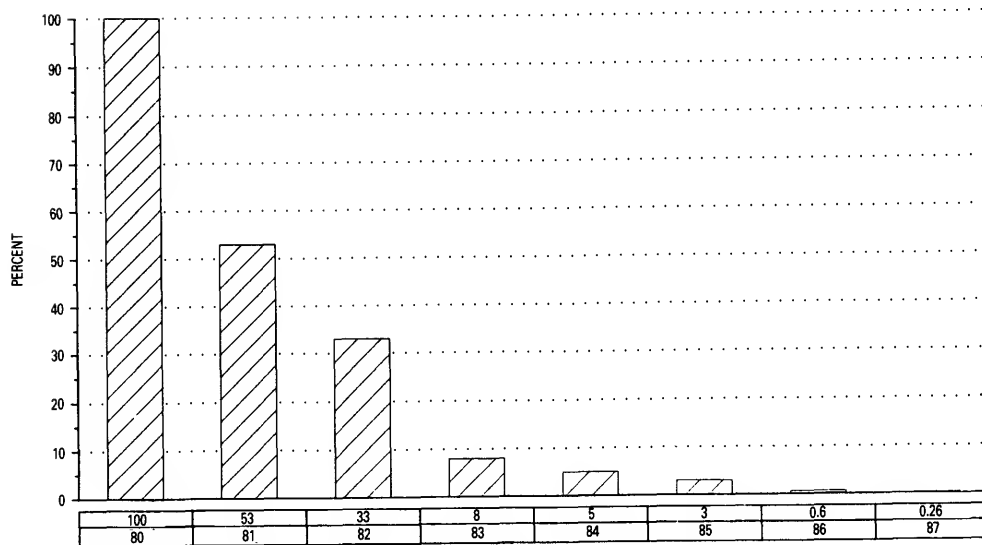


FIGURE 2 — OUTGOING ELECTRICAL QUALITY (AOQ) TREND/NORMALIZED 1980 = 100%

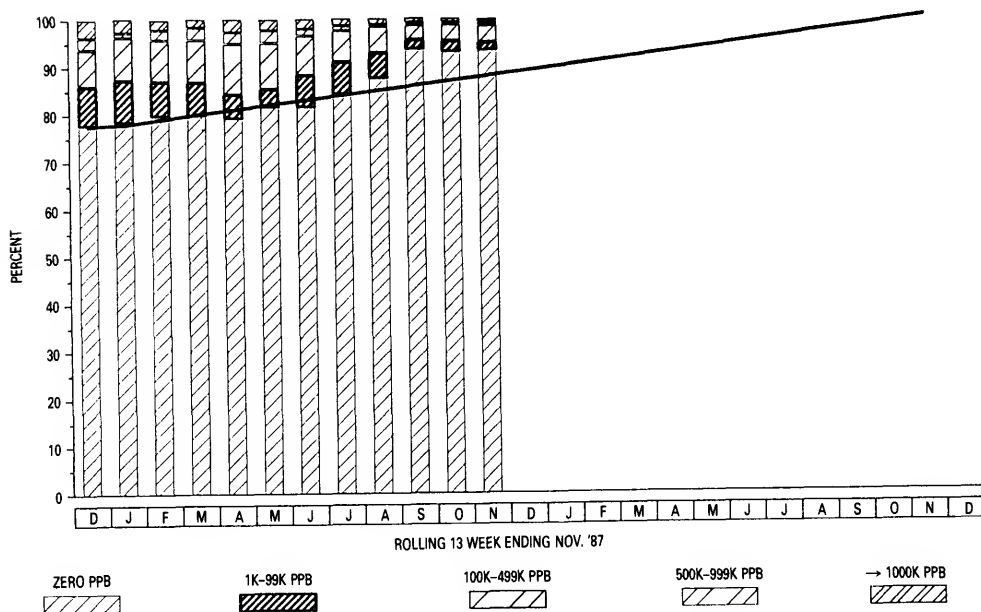
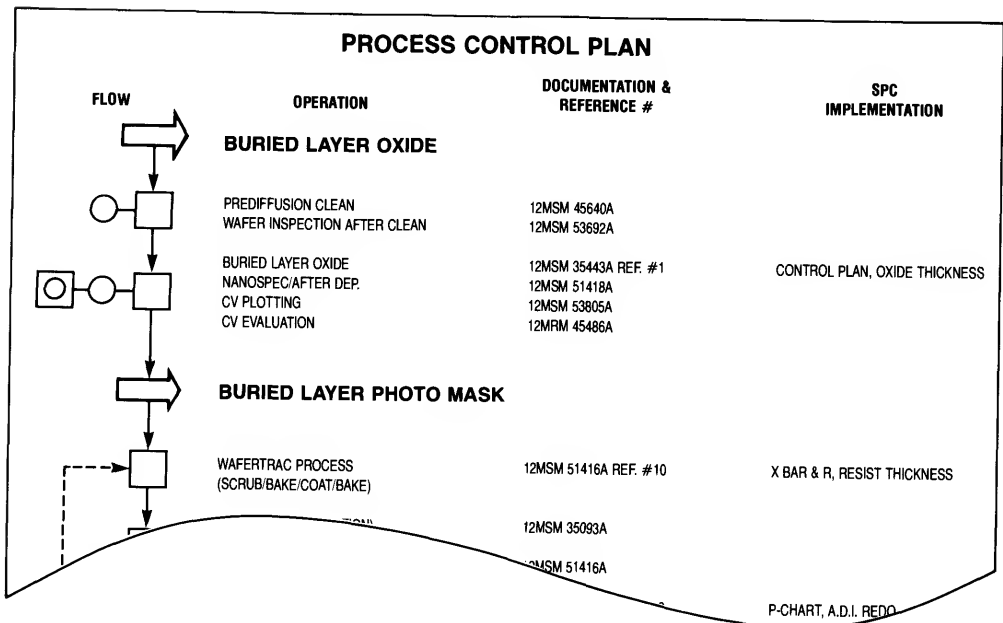


FIGURE 3 — PERCENT (%) OF DEVICES WITH ZERO PARTS PER BILLION (AOQ)



Characteristics:		Code	Description	Code	Description
	A.		VISUAL DEFECTS	E.	FILM SHEET RESISTANCE
	B.		VISUAL DEFECTS . . . MICROSCOPE	F.	REFRACTIVE INDEX
	C.		PARTICLE . . . MONITOR	G.	CRITICAL DIMENSION
	D.		FILM THICKNESS	H.	CV PLOT

Process Location	Ref. No.	Characteristic Affected	Part/Process Detail	Measurements Method	Analysis Methods	Frequency Sample Size	Reaction Plan: Point out of Limit (3) (4)
B.L. OXIDE	1	D	OXIDE THICKNESS	NANOMETRIC	CONTROL GRAPH	EVERY RUN 3 WFR/RUN	IMPOUND LOT (1) ADJUST TIME TO CENTER PROCESS PER SPEC
EPI	2	D	THICKNESS	DIGILAB	\bar{X} R CHART	EVERY RUN 5SITES/WFR	IMPOUND LOT (1) NOTIFY ENGR.
QA		D	THICKNESS	DIGILAB	\bar{X} R CHART	1WFR/SHIFT 5SITES/WFR	IMPOUND LOT (2) NOTIFY ENGR.
		E	FILM RESISTIVITY	4PT PROBE	\bar{X} R CHART	EVERY RUN 5SITES/WFR	IMPOUND LOT (1) NOTIFY ENGR.
QA		E	FILM RESISTIVITY	4PT PROBE	\bar{X} R CHART	1WFR/SHIFT 5SITES/WFR	IMPOUND LOT (2) NOTIFY ENGR.
DEEP				PROBE	MOVING R	EVERY LOT 1 CTRL WFR PER LOT	IMPOUND LOT NOTIFY ENGR.

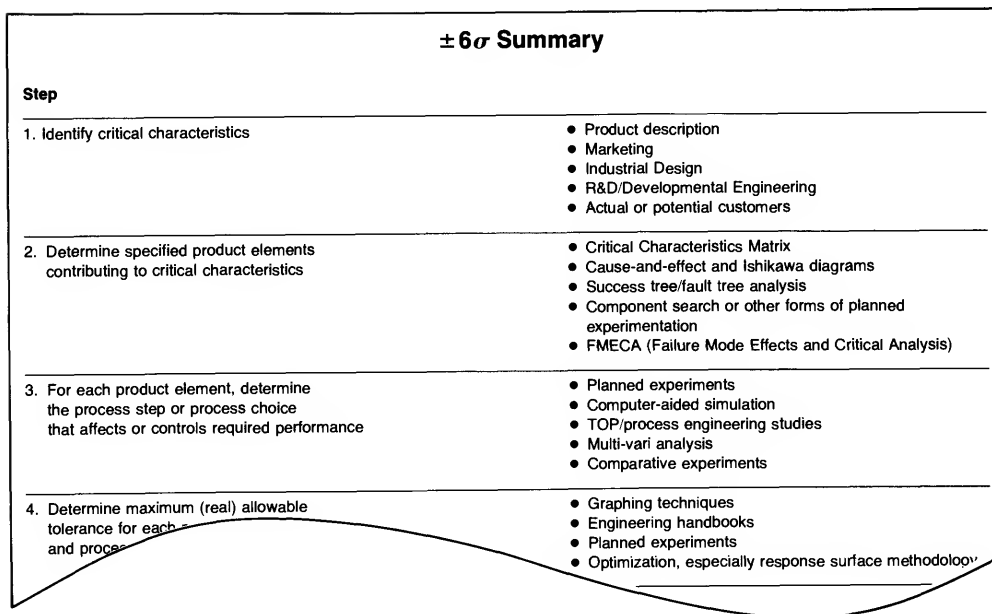


FIGURE 6 — PART OF SIX SIGMA (6σ) ROADMAP SHOWING STEPS TO SIX SIGMA CAPABILITY

Reliability Concepts

Reliability is the probability that a Linear integrated circuit will perform its specified function in a given environment for a specified period of time. This is the classical definition of reliability applied to Linear integrated circuits.

Another way of thinking about reliability is in relationship to quality. While quality is a measure of variability (extending to potential nonconformances-rejects) in the population domain, reliability is a measure of variability (extending to potential nonconformances-failures) in the population, time and environmental conditions domain. In brief **reliability** can be thought of as **quality over time and environmental conditions**.

The most frequently used reliability measure for integrated circuits is the **failure rate expressed** in percent per thousand device hours (%/1000 hrs.). If the time interval is small the failure rate is called "**Instantaneous Failure Rate**" [$\lambda(t)$] or "**Hazard Rate**." If the time interval is long (for example total operational time) the failure rate is called "**Cumulative Failure Rate**."

The number of failures observed, taken over the number of device hours accumulated at the end of the observation period and expressed as a percent is called the point estimate failure rate. This however, is a number obtained from observations from a sample of all integrated circuits. If we are to use this number to estimate the failure rate of all integrated circuits (total population), we need to say something about the risk we are taking by using this estimate. A **risk** statement is provided by the **confidence level** expressed together with the failure rate. For example, a 0.1% per 1000 device hours failure rate at 90% confidence level can be thought of as 90% of the integrated circuits will have a failure rate below 0.1%/1000 hours. Mathematically the failure rate at a given con-

fidence level is obtained from the point estimate and the **CHI square** (X^2) distribution. (The X^2 is a statistical distribution used to relate the observed and expected frequencies of an event.) In practice, a reliability calculator rule is used which gives the failure rate at the confidence level desired for the number of failures and device hours under question.

As the number of device hours increases, our confidence in the estimate increases. In integrated circuits, it is preferred to make estimates on the basis of failures per 1,000,000,000 (10^9) device hours (**FITS**) or more. If such large numbers of device hours are not available for a particular device, then the point estimate is obtained by pooling the data from devices that are similar in process, voltage, construction, design, etc., and for which we expect to see the same failure modes in the field.

The environment is specified in terms of the temperature, electric field, relative humidity, etc., by an **Eyring** type equation of the form:

$$\lambda = Ae - \frac{\phi}{KT} \dots e - \frac{B}{RH} \dots e - \frac{C}{E} \dots$$

Where A, B, C, ϕ & K are constants, T is temperature, RH is relative humidity, E is the electric field, etc.

The most familiar form of this equation deals with the first exponential which shows an **Arrhenious type** relationship of the **failure rate** versus the **junction temperature** of integrated circuits, while the causes of failure generally remain the same. Thus, we can test devices near their maximum junction temperatures, analyze the failures to assure that they are the types that are accelerated by temperature and then applying known acceleration factors, estimate the failure rates for lower junction temperatures. Figure 7 shows an

example of a curve which gives estimates of typical failure rates versus temperature for integrated circuits.

Arrhenius type of equation: $\lambda = Ae^{-\frac{\phi}{KT}}$

Where: λ = Failure Rate
 A = Constant
 e = 2.72
 ϕ = Activation Energy
 K = Boltzman's Constant
 T = Temperature in Degrees Kelvin

$$T_J = T_A + \theta_{JA} P_D \text{ or } T_J = T_C + \theta_{JC} P_D$$

Where: T_J = Junction Temperature
 T_A = Ambient Temperature
 T_C = Case Temperature
 θ_{JA} = Junction to Ambient Thermal Resistance
 θ_{JC} = Junction to Case Thermal Resistance
 P_D = Power Dissipation

Failure rate curves for equipment and devices can be represented by an idealized graph called the **Bathtub Curve** (Figure 8).

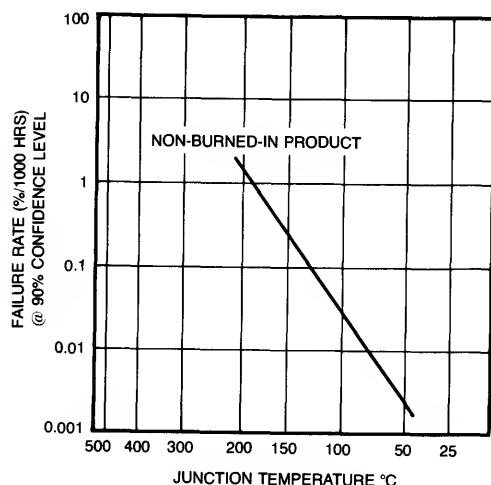


FIGURE 7 — TYPICAL FAILURE RATE versus JUNCTION TEMPERATURE

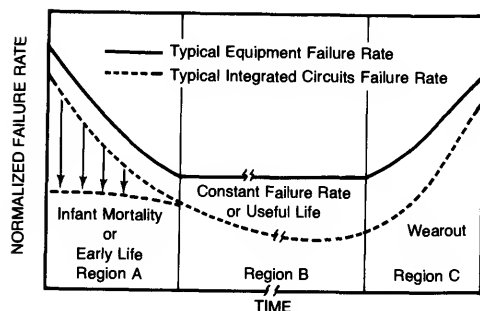


FIGURE 8 — FAILURE RATE versus TIME (BATHTUB CURVE)

There are three important regions identified on this curve. In Region A, the failure rate decreases with time and it is generally called **infant mortality** or early life failure region. In Region B, the failure rate has reached a relatively constant level and it is called **constant failure rate** or **useful life region**. In the third region, the failure rate increases again and it is called wearout region. Modern integrated circuits generally do not reach the wearout portion of the curve when operated under normal use conditions.

The **wearout** portion of the curve can usually be identified by using highly accelerated test conditions. For modern integrated circuits, even the useful life portion of the curve is characterized by so few failures compared to the accumulated device hours, that the **useful life** portion of the curve looks like a continuously decreasing failure rate curve (Figure 8, dotted line).

The **infant mortality** portion of the curve is of most interest to equipment manufacturers because of its impact on customer perception and potential warranty costs. In recent years the infant mortality portion of the curve for integrated circuits, and even equipment, has been drastically reduced (Figure 8, note arrows showing reduction of infant mortality). The reduction was accomplished by improvements in technology, emphasis on statistical process control, reliability modeling in design and reliability in manufacturing (wafer reliability, assembly reliability, etc.). In this respect many integrated circuit families have a continuously decreasing failure rate curve.

Does a user still need to consider burn-in? For this question to be answered properly the IC user must consider the **target failure rate** of the equipment, **apportioned** to the components used, application environment, maturity of equipment and components (new versus mature technology), the impact of a failure (i.e. safety versus casual entertainment), maintenance costs, etc. Therefore, if the IC user is going through these considerations for the first time, the question of burn-in at the component level should be discussed during a user-vendor interface meeting.

A frequently asked question is about the reliability differences between **plastic** versus **hermetic** packaged integrated circuits. In general, for all bipolar integrated circuits including linear, the field removal rates are the same for normal use environments, with many claims of plastic being better because of their "solid block" structure.

The tremendous increase in reliability of plastic packages has been accomplished by the continuous improvements in piece parts, materials and processes. Nevertheless differences can still be observed under highly accelerated environmental conditions. For example, if a bimetallic (gold wire and aluminum metallization) system is used in plastic packages and they are placed on a high temperature operating life test (125°C) then failures in the form of opens will be observed after 10,000 hours of continuous operating life at the gold to aluminum interface. Packages, whether plastic or hermetic, with a monometallic system (aluminum wire to aluminum metallization) will have no opens because of the absence of the gold to aluminum interface. As a result, a difference in failure rates will be observable.

Differences in failure rates between plastics and hermetics could be observed if devices from both packaging systems are placed in an environment of 85°C; 85% RH with bias applied. At some point in time plastic encapsulated ICs should fail since they are considered pervious by moisture, (the failure mechanism being corrosion of the aluminum metallization) while hermetic packages should not fail since they are considered impervious by moisture. The reason the word

"should" was used is because advances in plastic compounds, package piece parts, encapsulation processes and final chip passivation have made plastic integrated circuits capable of operating more than 5000 hours without failures in an 85°C, 85% RH environment. Differences in failure rates due to internal corrosion between plastic and hermetic packages may not be observable until well after 5000 operating hours.

The aforementioned two examples had environments substantially more accelerated than normal life so these two issues discussed are not even a factor under normal use conditions. In addition, mechanisms inherent in hermetic packages but absent in plastics were not even considered here. Improved reliability of plastic encapsulated ICs has decreased demand of hermetic packages to the point where many devices are offered only in plastic packages. The user then should feel comfortable in using the present plastic packaging systems.

A final question that is asked by the IC users is: how can one be assured that the reliability of standard product does not degrade over time? This is accomplished by our emphasis on statistical process control, in-line reliability assessment and reliability auditing by periodic and strategic sampling and accelerated testing of the various integrated circuit device packaging systems. A description of these audit programs follows below.

Linear Reliability Audit Program

The reliability of a product is a function of design and manufacturing. Inherent reliability is the reliability which a product would have if there were no imperfections in the materials, piece parts and manufacturing processes of the product. The presence of imperfections gives risk to the actual reliability of the product.

Motorola uses on-line and off-line reliability monitoring in an attempt to prevent situations which could degrade reliability. On-line reliability monitoring is at the wafer and assembly levels while off-line reliability monitoring involves reliability assessment of the finished product through the use of accelerated environmental tests.

Continuous monitoring of the reliability of Linear integrated circuits is accomplished by the Linear Reliability Audit Program, which is designed to compare the actual reliability to that specified. This objective is accomplished by periodic and strategic sampling of the various integrated circuit device packaging systems. The samples are tested by subjecting them to accelerated environmental conditions and the results are reviewed for unfavorable trends that would indicate a degradation of the reliability or quality of a particular packaging system. This provides the trigger mechanism for initiating an investigation for cause and corrective action. Concurrently, in order to provide a minimum of interruption of product flow and assure that the product is fit for use, a lot by lot sampling or a nondestructive type 100% screen is used to assure that a particular packaging system released for shipment does have the expected reliability. This rigorous surveillance is continued until there is sufficient proof (many consecutive lots) that the problem has been corrected.

The Standard Logic and Analog Integrated Circuits Group has used reliability audits since the late sixties. Such programs have been identified by acronyms such as CRP (Consumer Reliability Program), EPIIC (Environmental Package Indicators for Integrated Circuits), LAPP (Linear Accelerated

Punishment Program), and RAP (Reliability Audit Program).

Currently, the Bipolar Analog Reliability Audit Program consists of a Weekly Reliability Audit and a Quarterly Reliability Audit. The Weekly Reliability Audit consists of rapid (short time) types of tests used to monitor the production lines on a real time basis. This type of testing is performed at the assembly/test sites worldwide. It provides data for use as an early warning system for identifying negative trends and triggering investigations for causes and corrective actions.

The Quarterly Reliability Audit consists of long term types of tests and is performed at the U.S. Bipolar Analog Division Center. The data obtained from the Quarterly Reliability Audit is used to assure that the correlation between the short term weekly tests and long term quarterly tests has not changed, and a new failure mechanism has not appeared.

A large data base is established by combining the results from the Weekly Reliability Audit with the results from the Quarterly Reliability Audit. Such a data base is necessary for estimating long term failure rates and evaluating potential process improvement changes. Also, after a process improvement change has been implemented, the Linear Reliability Audit Program provides a system for monitoring the change and the past history data base for evaluating the effect of the change.

Weekly Reliability Audit

The Weekly Reliability Audit is performed by each assembly/test site worldwide. The site must have capability for final electrical and quality assurance testing; reliability testing and first level of failure analysis. The results are reviewed on a continuous basis and corrective action is taken when appropriate. The results are accumulated on a monthly basis and published.

The Reliability Audit test plan is as follows:

Electrical Measurements: Performed initially and after each reliability test, consists of critical parameters and functional testing at 25°C on a go-no-go basis.

High Temperature Operating Life: Performed to detect failure mechanisms that are accelerated by a combination of temperature and electric fields. Procedure and conditions are per the MIL-STD-883, Method 1015 with an ambient temperature of 145°C for 40 hours or equivalent based on a 1.0eV activation energy and the Arrhenius equation.

Approximate Accelerated Factors

	125°C	50°C
145°C	4	4000
125°C	1	1000

Temperature Cycling/Thermal Shock: Performed to detect mechanisms related to thermal expansion and contraction of dissimilar materials, etc. Procedures and conditions are per MIL-STD-883, Methods 1010 or 1011, with ambient temperatures of -65°C to +150°C or -40°C to +125°C (JEDEC-STD-22-A104), minimum of 100 cycles.

Pressure Temperature Humidity (Autoclave): Performed to measure the moisture resistance of plastic encapsulated packages. It detects corrosion type failure mechanisms due to free ionic contaminants that may have entered the package during the manufacturing processes. Conditions are per

JEDEC-STD-22, Method 102, a temperature of 121°C, steam environment and 15psig. The duration of the test is 48 hours.

Analysis Procedure: Devices failing to meet the electrical criteria after being subjected to an accelerated environment type test are verified and characterized electrically, then submitted for failure analysis.

Quarterly Reliability Audit

The Quarterly Bipolar Analog Reliability Audit Program is performed at the U.S. Bipolar Analog Division Center. This testing is designed to assure that the correlation between the short term weekly tests and the longer quarterly tests has not changed and that no new failure mechanisms have appeared. It also provides additional long term information for a data base for estimating failure rates and evaluation of potential process improvement changes.

Electrical Measurements: Performed initially and at interim readouts, consist of all standard dc and functional parameters at 25°C, measured on a go-no-go basis.

High Temperature Operating Life Test: Performed to detect failure mechanisms that are accelerated by a combination of temperature and electric fields. Procedure and conditions are per MIL-STD-883, Method 1015, with an ambient temperature of 145°C for 40 and 250 hours or equivalent, based on 1.0eV activation energy and the Arrhenius equation.

Approximate Acceleration Factors

	125°C	50°C
145°C	4	4000
125°C	1	1000

Temperature Cycling/Thermal Shock: Performed to detect mechanisms related to thermal expansion and contraction, mismatch effects, etc. Procedure and conditions are per MIL-STD-883, Methods 1010 or 1011, with ambient temperatures of -65°C to +150°C or -40°C to +125°C (JEDEC-STD-22-A104) for 100 and 1000 cycles. Temperature Cycling and Thermal Shock are used interchangeably.

Pressure Temperature Humidity (Autoclave): Performed to measure the moisture resistance of plastic encapsulated packages. It detects corrosion type failure mechanism due to free ionic contaminants that may have entered the package during the manufacturing processes. Conditions are per JEDEC-STD-22, Method 102, a temperature of 121°C, steam environment and 15psig. The duration of the test is for 96 hours, with a 48 hour interim readout.

Pressure Temperature Humidity Bias (Biased Autoclave): This test measures the moisture resistance of plastic encapsulated packages. It detects corrosion type failure mechanism due to free and bounded ionic contaminants that may have entered the package during the manufacturing processes, or they may be bound in the materials of the integrated circuit packaging system and activated by the moisture and the applied electric fields. Conditions are per JEDEC-STD-22, Method 102, with bias applied. Temperature is 121°C, steam environment and 15psig. Duration is for 32 hours, with a 16 hour interim readout. This test detects the same type of failures as the Temperature Humidity Bias (85°C, 85% RH, with bias) test, only faster. The acceleration factor between PTHB and THB is between 20 and 40 times, depending on the type of corrosion mechanism, electric field and packaging system.

Temperature, Humidity and Bias (THB): This test measures the moisture resistance of plastic encapsulated packages. It detects corrosion type failure mechanisms due to free and bounded ionic contaminants that may have entered the package during the manufacturing processes, or they may be bound in the materials of the integrated circuit packaging system and activated by moisture and the applied electric fields. Conditions are per JEDEC-STD-22, Method 102 (85°C, 85% RH), with bias applied. The duration is for 1008 hours, with a 504 hour interim readout. The acceleration factor between THB (85°C, 85% RH and bias) and the 30°C, 90% RH is typically 40–50 times, depending on the type of corrosion mechanism, electric field and packaging system.

Analysis Procedure: Devices failing to meet the electrical criteria after being subjected to an accelerated environment type test are verified and characterized electrically, then submitted for failure analysis.



Applications Literature

Applications Literature

The application literature listed in this section has been prepared to acquaint the circuits and systems engineer with Motorola Linear integrated circuits and their applications. To obtain copies of the notes, simply list the publication number or numbers and send your request on your company letterhead to: Literature Distribution Center, Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, Arizona 85036.

Application Note Abstracts

AN273A Getting More Value Out of an Integrated Operational Amplifier Data Sheet

The operational amplifier has become a basic building block in present day solid state electronic systems. The purpose of this application note is to provide a better understanding of the open loop characteristics of the amplifier and their significance to overall circuit operation. Also each parameter is defined and reviewed with respect to closed loop considerations. The importance of loop gain stability and bandwidth is discussed at length. Input offset voltage and current and resultant drift effects in the circuit are also reviewed with respect to closed loop operation.

AN489 Analysis and Basic Operation of the MC1595

The MC1595 monolithic linear four-quadrant multiplier is discussed. The equations for the analysis are given along with performance data that is characteristic of the device. A few basic applications are given to assist the designer in system design.

AN531 MC1596 Balanced Modulator

The MC1596 monolithic circuit is a highly versatile communications building block. In this note, both theoretical and practical information are given to aid the designer in the use of this part. Applications include modulators/demodulators for AM, SSB, and suppressed carrier AM; frequency doublers and HF/VHF double balanced mixers.

AN545A Television Video IF Amplifier Using Integrated Circuits

This applications note considers the requirements of the video IF amplifier section of a television receiver, and gives working circuit schematics using integrated circuits which have been specifically designed for consumer oriented products. The integrated circuits used are the MC1350, MC1352, and the MC1330.

AN587 Analysis and Design of the Op Amp Current Source

A voltage controlled current source utilizing an operational amplifier is discussed. Expressions for the transfer function and output impedances are developed using both the ideal and non-ideal op amp models. A section on analysis of the effects of op amp parameters and temperature variations on circuit performance is presented.

AN702 High Speed Digital-To-Analog And Analog-To-Digital Techniques

A brief overview of some of the more popular techniques for accomplishing D/A and A/D techniques. In particular those techniques which lead themselves to high speed conversion.

AN703 Designing Digitally-Controlled Power Supplies

This application note shows two design approaches; a basic low voltage supply using an inexpensive MC1723 voltage regulator and a high current, high voltage, supply using the MC1466 floating regulator with optoelectronic isolation. Various circuit options are shown to allow the designer maximum flexibility in an application.

AN708A Line Driver and Receiver Considerations

This report discusses many line driver and receiver design considerations such as system description, definition of terms, important parameter measurements, design procedures and application examples. An extensive line of devices is available from Motorola to provide the designer with the tools to implement the data transmission requirements necessary for almost every type of transmission system.

AN719 A New Approach To Switching Regulators

This article describes a 24 Volt, 3.0 Ampere switching mode supply. It operates at 20 kHz from a 120 Vac line with an overall efficiency of 70%. New techniques are used to shape the load line. The control circuit uses a quad comparator and an opto coupler and features short circuit protection.

AN781A Revised Data Interface Standards

This application note provides a brief overview and comparison of communication interface standards EIA-232-C, EIA-422A, EIA-423, EIA-449 and EIA-485 for the hardware designer. A listing of the standard's specifications and appropriate Motorola devices are included.

AN829 Application of the MC1374 TV Modulator

The MC1374 was designed for use in applications where separate audio and composite video signals are available, which need converting to a high quality VHF television signal. It's ideally suited as an output device for subscription TV decoders, video disk and video tape players.

AN879 Monomax — Application of the MC13001 Monochrome Television Integrated Circuit

This application note presents a complete 12" black and white line-operated television receiver, including artwork for the printed circuit board. It is intended to provide a good starting point for the first-time user. Some of the most common pitfalls are overcome, and the significance of component selections and locations are discussed.

AN917 Reading and Writing in Floppy Disk Systems Using Motorola Integrated Circuits

The floppy disk system has become a widely used means for storing and retrieving both programs and data. A floppy

APPLICATIONS LITERATURE (continued)

disk drive requires precision controls to position and load the head as well as defined read/write signals in order to be a viable system. This application note describes the use of the MC3469 and MC3471 Write Control ICs and the MC3470 Read Amplifier which provide the necessary head and erase control, timing functions, and filtering.

AN920 Rev 2 Theory and Applications of the MC34063 and μ A78S40 Switching Regulator Control Circuits

This paper describes in detail the principle of operation of the MC34063 and μ A78S40 switching regulator subsystems. Several converter design examples and numerous applications circuits with test data are included.

AN926 Techniques for Improving the Settling Time of a DAC & Op Amp Combination

This application note describes some techniques which were tested for the purpose of optimizing settling time of a DAC/op amp combination. The objective of the experimentation was to obtain a settling time of under 1.0 μ s for 12 bit ($\pm 0.012\%$) accuracy. Op amps chosen for this exercise are high speed, yet inexpensive monolithic devices.

AN932 Application of the MC1377 Color Encoder

The MC1377 is an economical, high quality, RGB encoder for NTSC or PAL applications. It accepts red, green, blue, and composite sync inputs and delivers I/Vpp composite NTSC or PAL video output into a 75 ohm load. It can provide its own color oscillator and burst gating, or it can be easily driven from external sources. Performance virtually equal to high cost studio equipment is possible with common color receiver components. The following note is intended to explain the operation of the device and guide the prospective user in selecting the optimum circuit for his needs.

AN933 A Variety of Uses for the MC34012 and MC34017 Tone Ringers

The MC34012 and MC34017 electronic tone ringers were developed to replace the bulky electromechanical bell assembly of a telephone, while providing the same basic function. When used in conjunction with a piezo ceramic transducer, these circuits will output a warbling sound in response to the applied ringing voltage. With some imagination, however, the circuits can be used in a variety of ways, including non-telephone applications, — wherever an alerting sound or indication is required. Applications include appliance buzzers, burglar alarms, safety alerting functions, special sound effects, visual ringing indicators, and others. The circuits in this application note show how a variety of effects can be obtained.

AN937 A Telephone Ringer Which Complies with FCC and EIA Impedance Standards

The MC34012 and MC34017 Tone Ringers are designed to replace the bulky bell assembly of a telephone, while providing the same function and performance under a variety of conditions. The operational requirements spelled out by the FCC and the EIA, simply stated, are that a ringer circuit MUST function when a ringing signal is provided, and MUST NOT ring when other signals (speech, dialing signals, noise) are

on the line. This application note discusses how the IC's operate, the specific operational requirements to be met, and how they are met. Only "on-hook" requirements are discussed since off-hook operation is not applicable.

AN957 Interfacing the Speakerphone to the MC34010/11/13 Speech Networks

Interfacing the MC34018 speakerphone circuit to the MC34010 series of telephone circuits is described in this application note. The series includes the MC34010, MC34011, MC34013, and the new "A" version of each of those. The interface is applicable to existing designs, as well as to new designs.

AN958 Transmit Gain Adjustments for the MC34014 Speech Network

The MC34014 telephone speech network provides for direct connection to an electret microphone and to Tip and Ring. In between, the circuit provides gain, drive capability, and determination of the ac impedance for compatibility with the telephone lines. Since different microphones have different sensitivity levels, different gain levels are required from the microphone to the Tip and Ring lines. This application note will discuss how to change the gain level to suit a particular microphone while not affecting the other circuit parameters.

AN959 A Speakerphone with Receive Idle Mode

The MC34018 speakerphone system operates on the principle of comparing the transmit and receive signals to determine which is stronger, and then switching the circuit into that mode. Under conditions where noise from the telephone line (in the receive path) exceeds the background noise in the transmit path, the speakerphone will switch easily, or even lock, into the receive mode. Under these conditions the conversation will sound "dead" to the party at the far-end. It will also be more difficult for the near-end party to activate the transmit channel since the transmit detection is at the output of the transmit attenuator, which will be at maximum attenuation during this time. The addition of a receive idle mode can alleviate this problem by ensuring that the transmit and receive gains will be approximately equal when no voice signals are present. This allows the far-end party to hear ambient noises, and also increases the sensitivity to transmit signals.

AN960 Equalization of DTMF Signals Using the MC34014

This application note will describe how to obtain equalization (line length compensation) of the DTMF dialing tones using the MC34014 speech network. While the MC34014 does not have an internal dialer, it has the interface for a dialer so as to provide the means for putting the DTMF tones onto the Tip & Ring lines. The Equalization amplifier, whose gain varies with loop current, was meant primarily to equalize the speech signals. However, by adding one resistor, it can be used to equalize the DTMF signals as well.

AN976 A New High Performance Current Mode Controller Teams Up with Current Sensing Power MOSFETs

A new current mode control IC that interfaces directly with current sensing power MOSFETs is described. Its second

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generation architecture is shown to provide a variety of advantages in current mode power supplies. The most notable of these advantages is a "lossless" current sensing capability that is provided when used with current sensing MOSFETs.

Included in the discussion are subtle factors to watch out for in practical designs, and an applications example.

AN980 Low Power FM Dual Conversion Receivers MC3362/3/4

Motorola has recently developed a series of low power FM dual conversion receivers in monolithic silicon integrated circuits. The MC3362/3/4 series is ideal for application in cordless phones, narrowband voice and data receivers, CB and amateur band radios, RF security devices, and other applications through 150 MHz.

AN983 A Simplified Power Supply Design Using the TL494 Control Circuit

This describes the operation and characteristics of the TL494 Switchmode™ Voltage Regulator and shows its application in a 400-watt off-line power supply.

The TL494 is a fixed-frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply.

AN1002 A Handsfree Featurephone Design Using the MC34114 Speech Network and the MC34018 Speakerphone ICs

This application note describes the procedure for combining the MC34114 speech network with the MC34018 speakerphone circuit into a featurephone which includes the following functions: ten number memory pulse/tone dialer, tone ringer, a "Privacy" (Mike Mute) function, and line length compensation for both handset and speakerphone operation.

Three circuits are developed in this discussion: a line-powered featurephone, a line-powered featurephone with a booster (for using the speakerphone on long lines), and one powered from a power supply. The circuits are nearly identical, except for the Tip/Ring interface. Their performance, however, differs noticeably, particularly in the low loop current range. Initially, the discussion will focus on the line-powered circuit.

AN1003 A Featurephone Design, with Tone Ringer and Dialer, Using the MC34118 Speakerphone IC

This application note describes how to add a handset, dialer and tone ringer to the MC34118 speakerphone circuit. Although any one of several speech networks could be used as an interface between the MC34118 and the phone line this application note covers the case where simplicity and low cost are paramount.

Two circuits are developed in this discussion: a line-powered featurephone and one powered from a power supply.

AN1004 A Handsfree Featurephone Design Using the MC34114 Speech Network and the MC34118 Speakerphone ICs

This application note describes the procedure for combining the MC34114 speech network with the MC34118 speakerphone circuit into a featurephone which includes

the following functions: ten number memory pulse/tone dialer, tone ringer, a "Privacy" (Mike Mute) function and line length compensation for both handset and speakerphone operation.

AN1006 Linearize the Volume Control of the MC34118 Speakerphone

The volume control level of the MC34118 speakerphone IC has a nonlinear relationship with respect to the position of the volume control potentiometer, evident in Figure 14 of the data sheet.

AN1019 NTSC Decoding Using the TDA3330, with Emphasis on Cable In/Cable Out Operation

This application note is intended to supplement the data sheet by providing circuits for video cable drive, such as used in video processing circuits, frame store, and other specialized applications, and to expand upon the functional details of the TDA3330.

AN1040 Mounting Considerations for Power Semiconductors

In this note, mounting procedures are discussed in general terms for several generic classes of packages. As newer packages are developed, it is probable that they will fit into the generic classes discussed in this note. Unique requirements are given on data sheets pertaining to the particular package.

AN1044 The MC1378 — A Monolithic Composite Video Synchronizer

The MC1378 was designed to enable an interface to be made between remote composite color video sources and a locally controlled RGB source of video. It contains the necessary synchronizing circuits, plus a complete color encoder.

AN1077 Adding Digital Volume Control To Speakerphone Circuits

This application note will describe how to replace the potentiometer with a digital circuit which allows control of the speaker volume from a set of "UP" and "DOWN" pushbutton switches.

AN1078 New Components Simplify Brush DC Motor Drives

A variety of new components are making brush motor drive design easier. One of these components is a brushless motor control IC that is easily set up to drive brush motors. The circuits described here illustrate how these components can be combined to make practical drive circuits.

AN1081 Minimize the "pop" in the MC34119 Low Power Audio Amplifier

This application note describes how to minimize the "pop" to satisfy the most demanding user. The remedy, fortunately is very simple and inexpensive.

ANE002 130 W Ringing Choke Power Supply Using TDA4601

The architecture is based on the fly-back mode working in a free switching mode. Frequency range varies between 20

APPLICATIONS LITERATURE (continued)

kHz at full load and 70 kHz in the standby condition (also called sleep-mode). Input power is from the line (220 Vac) and is completely isolated from the output. Control and regulation are achieved by the TDA4601.

The power supply presents a linear foldback characteristic and is short circuit proof. An undervoltage inhibit provides a protection against low line voltage.

The complete system is an excellent compromise between complexity, cost and performance.

ANE424 50W Current Mode Controlled Offline Switch Mode Power Supply Working over 50% duty cycle using the UC3842A

This application note describes a way to improve the dynamic characteristics of this power supply using a technique called "Current Controlled PWM." A dedicated bipolar integrated circuit, UC3842A, has been used to achieve the current control, regulation and safety features.

AN-HK-07 A High Performance Manually Tuned AM Stereo Receiver for Automotive Application Using MOTOROLA ICs MC13021, MC13020 and MC13041

This application note presents a high performance manually tuned automotive AM stereo receiver design using MOTOROLA AM stereo ICs; MC13021, MC13020 and the MC13041. It is intended to provide radio design engineers with a good start in automotive AM stereo receiver design. The note consists of two parts; the first describes all relative important principles of a manually tuned AM stereo receiver, and the second part details the AM stereo receiver design for automotive application.

Article Reprints

AR115

A bipolar quad op amp having a JFET-like 4.5 MHz bandwidth resolves common mode input voltages and sinks output current close to the ground rail — even with a single +5.0 V supply.

Engineering Bulletin Abstracts

EB20 Multiplier/Op Amp Circuit Detects True RMS

Two op amps and two multipliers are used in the circuit described in EB20 to obtain the true rms of an input voltage ranging from 2.0 to 10 Vpk.

EB51 Successive Approximation BCD A/D Converter

A successive approximation A/D converter in which a digital-to-analog converter in a feedback loop produces a BCD digital output from an analog input is described in EB51.

Product Literature

HB206 Rev 3 SG98 Rev 4



MOTOROLA LINEAR AND INTERFACE ICS



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